INTRODUCTION

The CD-ROM 48X 1 chip receives the input signal read from the CD-DA/VIDEO-CD/CD-ROM disc after handling by the RF amplifier. The signal is input into the digital servo block which has a built-in DSP core, and goes through focus and tracking adjustments. The RF signal input into a data path goes through the data slicer, PLL, EFM demodulator, C1/C2 ECC and the audio handling block. In the case of a CD-DA, the signal is output through the 1-bit DAC. In the case of a CD-ROM, the signal is input into an external CD-ROM controller for handling, then transmitted to the host through the ATAPI I/F. Also, if you operate the CD-DA in audio buffering mode while already in CAV mode, the signal is stored in the CD-ROM controller DRAM at high speed, then output at 1x from the CD-ROM controller, after passing through the 1-bit DAC built-in to the S5L9250B.

FEATURES

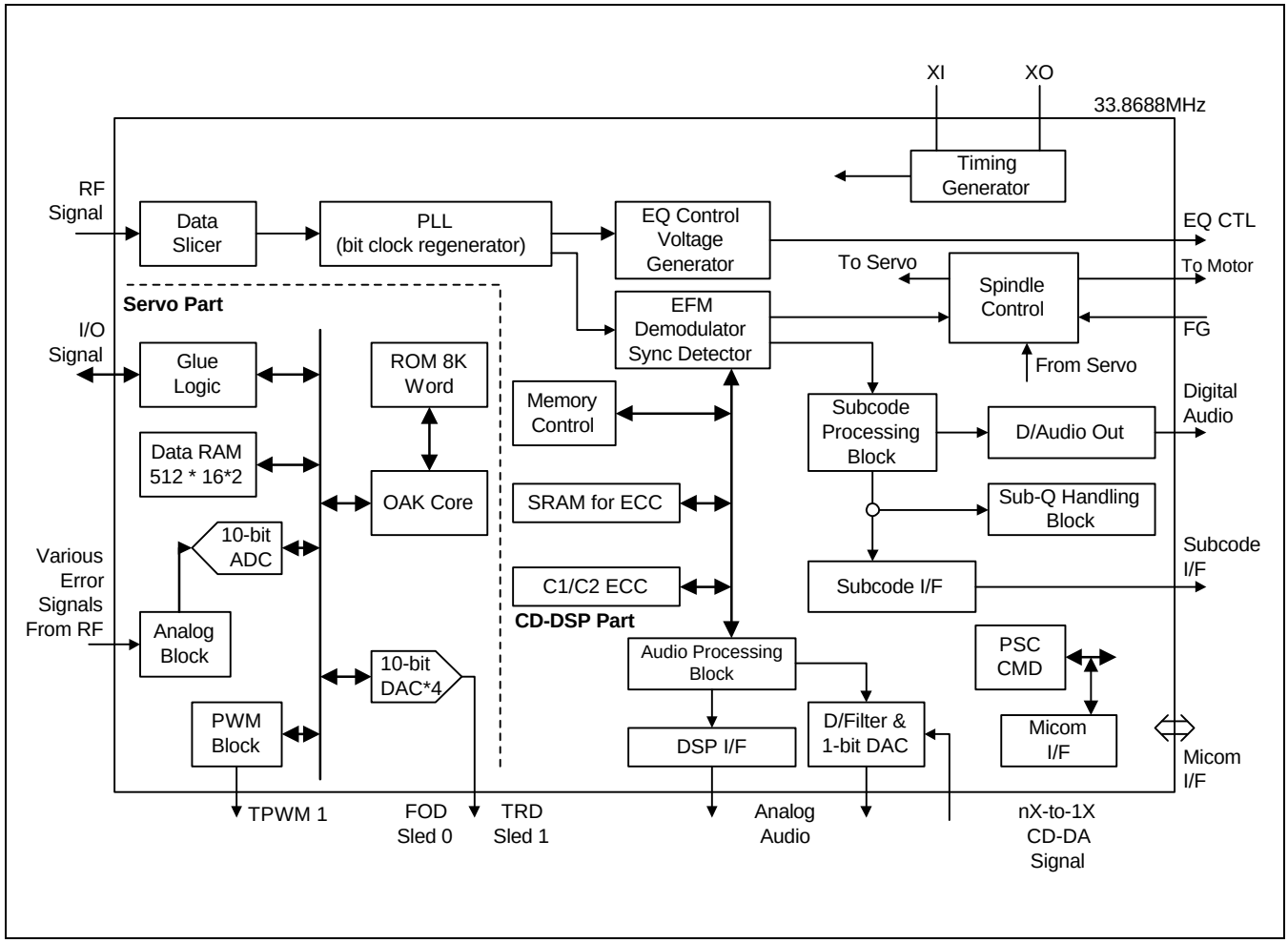
- Main Features
  - Digital servo, CD-DSP, 1-bit DAC.
  - 33.8688MHz crystal.
  - Supports CLV 4X and 8X.
  - Supports CAV MAX 16X, 20X, 24X, 32X, 40X, and 48X.
  - Interrupt (SINTB)
  - MICOM interface
- Digital Servo Block
  - Automatic adjusting feature (focus/tracking loop offset, balance, loop gain)
  - Built-in AGC feature that adapts to work optimally with various disc types
  - Built-in search algorithm for speed control
  - Servo monitor signal generation (FOK, MIRROR, TZC, ANTI-SHOCK)
  - Various loop filter coefficient selection by MICOM
  - Built-in algorithm for handling defects/shocks
  - Disc discriminating data out (FEpk, SBADpk)
  - RF IC and serial interface
  - Built-in 10-bit DAC (Focus/Tracking/SLD)
  - OAK DSP core
- CD Digital Signal Processing Block
  - Wide capture range analog PLL
  - Data Slicer using duty feedback method
  - EFM demodulation
  - Sync detection, protection, insertion
  - CLV, CAV disc spindle motor control
  - C1/C2 ECC
  - Built-in 16 K SRAM for ECC
  - Subcode P - W handling feature
  - CD-DA Audio handling feature
  - SUB-Q De-interleaving & CRC check
  - High speed data transmission support by CD-ROM decoder block for audio buffering (sync mode selection between subcode sync and CD-DA data)
  - Digital audio out block
  - Subcode sync. Insertion, Protection

- 1-Bit DAC
  - 16-bit ∑ Δ digital-to-analog converter
  - On-chip analog postfilter
  - Filtered line-level outputs, linear phase filtering
  - 90dB SNR
  - Sampling rate: 44.1kHz
  - Input rate 1Fs or 2Fs by normal mode/ double mode selection
  - Digital volume control by MICOM interface
  - On-chip voltage reference
  - Digital de-emphasis on/off, digital attenuation
  - Low clock jitter sensitivity
- Technology & Gate Density
  - 0.35um mixed mode CMOS technology
  - 3.3V power supply (internal core & analog)
  - 5.0V power supply (digital I/O)
  - Current used: 300mA
  - Package: 128QFP.
  - Core used: OAK DSP; ADC for servo use; DAC, 1-bit DAC; 16K SRAM.
  - Clock used:
    1) 33.8688MHz & PLL clock (4.3218MHz * speed coeff.) → DP part.
    2) 33.8688MHz or 40MHz synthesized frequency → servo part.
    3) 16.9344MHz → 1-bit DAC part.

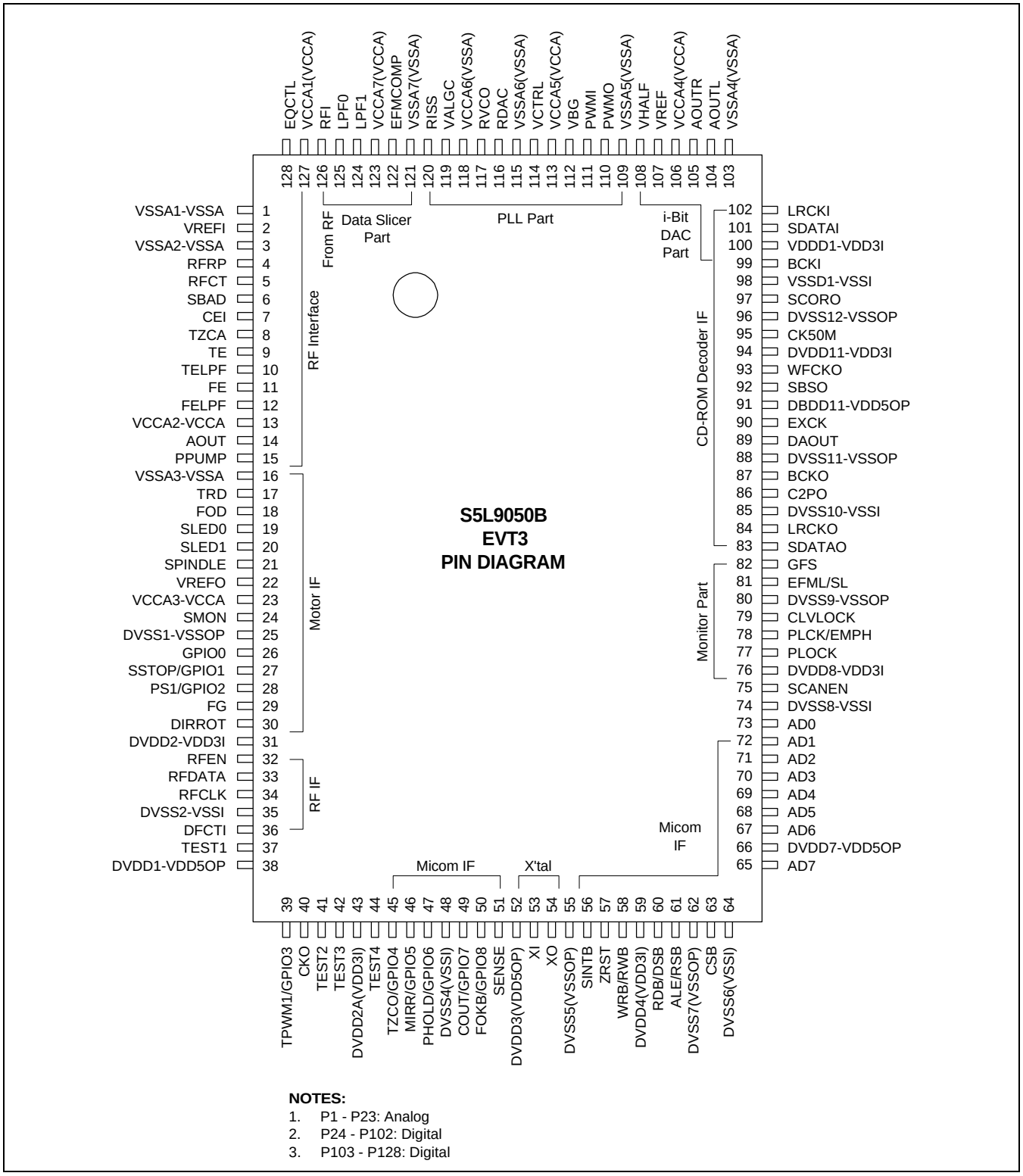
ORDERING INFORMATION

Device	Package	Operating Temperature
S5L9250B01-Q0R0	128-QFP-1420C	-20°C - +75°C

CD-ROM 48X 1 CHIP (DSP+SERVO+1-BIT DAC) BLOCK DIAGRAM



PIN CONFIGURATION



NOTES:

1. P1 - P23: Analog
2. P24 - P102: Digital
3. P103 - P128: Digital

SAMSUNG ELECTRONICS

PIN DESCRIPTION

Table 1. Pin Description

No	Name	Description	Related Block	I/O	Pad Type	To/From
1	VSSA1	Analog ground (EQ controller)	-	P	VSSA	-
2	VREFI	VREF input	SERVO	I	PICA	RF
3	VSSA2	Analog ground (for servo ADC use)	-	P	VSSA	-
4	RFRP	RF envelope signal	SERVO	I	PICA	RF
5	RFCT	RF envelope's center detection signal	SERVO	I	PICA	RF
6	SBAD	FOK, DFCT generating SUB-BEAM ADD signal (E+F)	SERVO	I	PICA	RF
7	CEI	ERROR signal for center servo use	SERVO	I	PICA	RF
8	TZCA	TZC signal generating signal (=TE)	SERVO	I	PICA	RF
9	TE	Tracking error signal	SERVO	I	PICA	RF
10	TELPF	TE defect holding pin	SERVO	I	PICA	-
11	FE	Focusing error signal	SERVO	I	PICA	RF
12	FELPF	FE defect holding pin	SERVO	I	PICA	-
13	VCCA2	Analog 3.3V power (for servo ADC use)	-	P	VCCA	-
14	AOUT	Analog out	SERVO	O	POBA	MONI
15	PPUMP	Pump out for PLL use (filter)	SERVO	O	POBA	-
16	VSSA3	Analog ground (for servo DAC use)	-	P	VSSA	-
17	TRD	Tracking drive signal (10-bit DAC)	SERVO	O	POBA	DRV
18	FOD	Focusing drive signal (10-bit DAC)	SERVO	O	POBA	DRV
19	SLED0	Stepping control signal 0/DC motor control signal	SERVO	O	POBA	DRV
20	SLED1	Stepping control signal 1	SERVO	O	POBA	DRV
21	SPINDLE	Spindle controlling PWM output	CLV	O	POBA	-
22	VREFO	VREF out for driver IC	SERVO	O	POBA	SLED
23	VCCA3	Analog 3.3V power (for DAC use)	-	P	VCCA	-
24	SMON	Spindle motor on/off	CLV	O	PHOB4	MOTOR
25	DVSS1	Digital GND (for output PAD + PRE driver)	-	P	VSSOP	-
26	GPIO0	General purpose I/O 0		B	PHBCT4	
27	STOP/GPIO	LIMIT switch/sled position sensor PS0/general purpose I/O	SERVO	B	PHBCT4	-
28	PS1/GPIO	Sled position sensor signal 1/general purpose I/O	SERVO	B	PHBCT4	-
29	FG	Frequency generator signal (for CAV)	CLV	I	PHIC	MOTOR

Table 1. Pin Description (Continued)

No	Name	Description	Related Block	I/O	Pad Type	To/From
30	DIRROT	Spindle disc rotation direction	CLV	I	PHIC	MOTOR
31	DVDD2	Digital 3.3 V power (for internal logic use)	-	P	VDD3I	-
32	RFEN	RF data enable	SERVO	O	PHOB4	RF
33	RFDATA	RF serial data	SERVO	O	PHOB4	RF
34	RFCLK	RF Interface clock	SERVO	O	PHOB4	RF
35	DVSS2	Digital ground (for internal logic use)	-	P	VSSI	-
36	DFCTI	Defect detection signal	SERVO	I	PHIS	RF
37	TEST1	Test mode select	TEST	I	PHICD50	-
38	DVDD1	Digital 5.0V power (for output PAD + PRE driver)	-	P	VDD5OP	-
39	PWM1/ GPIO	PWM (TPWM1) output (sled monitor)/general purpose I/O 3	SERVO	B	PHBCT4	
40	CKO	33.8688MHz CK out		O	PHOB8SM	
41	TEST2	Test mode select	TEST	I	PHICD50	-
42	TEST3	Test mode select	TEST	I	PHICD50	-
43	DVDD2A	Digital 3.3V power (for servo SRAM use)	-	P	VDD3I	-
44	TEST4	Test mode select	TEST	I	PHICD50	-
45	TZCO/GPIO	Track zero cross signal/general purpose I/O	SERVO	B	PHBCT4	MONI
46	MIRR/GPIO	MIRROR signal/general purpose I/O	SERVO	B	PHBCT4	MONI
47	PHOLD/ GPIO	ATSC+DFCT+KICK signal/general purpose I/O	SERVO	B	PHBCT4	MONI
48	DVSS4	Digital ground (for servo SRAM use)	-	P	VSSI	-
49	COUT/GPIO	COUT signal/L_MIRR signal/general purpose I/O	SERVO	B	PHBCT4	MONI
50	FOKB/ GPIO	FOCUSING ok signal/general purpose I/O	SERVO	B	PHBCT4	MICOM
51	SENSE	Servo processor's status monitor signal	SERVO	O	PHOD4U	MICOM
52	DVDD3	Digital 5.0V power (for output PAD + PRE driver)	-	P	VDD5OP	-
53	XI	System clock signal input pin	CLK	I	PHSOSCHF	OSC
54	XO	System clock signal output pin	CLK	O	PHSOSCHF	OSC
55	DVSS5	Digital ground (for output PAD + PRE driver)	-	P	VSSOP	-
56	SINTB	Microprocessor disc interrupt (data processor)	MICOM	O	PHOB4	MICOM

Table 1. Pin Description (Continued)

No	Name	Description	Related Block	I/O	Pad Type	To/From
57	ZRST	System reset	MICOM	I	PHIS	MICOM
58	WRB/RWB	Microprocessor write strobe (INTEL)/ read-write strobe (MOTOROLA)	MICOM	I	PHISU50	MICOM
59	DVDD4	Digital 3.3V power (for internal logic use)	-	P	VDD3I	-
60	RDB/DSB	Microprocessor read strobe (INTEL)/ data strobe signal (MOTOROLA)	MICOM	I	PHISU50	MICOM
61	ALE/RSB	Microprocessor address latch enable/ address register select in indirect mod	MICOM	I	PHISU50	MICOM
62	DVSS7	Digital ground (for output PAD + PRE driver)	-	P	VSSOP	-
63	CSB	Chip select	MICOM	I	PHISU50	MICOM
64	DVSS6	Digital ground (for internal logic use)	-	P	VSSI	-
65	AD7	Microprocessor address[7]/DATA BUS[7]	MICOM	B	PHBCT4	MICOM
66	DVDD5	Digital 5.0V power (for output PAD + PRE drive)	-	P	VDD5OP	-
67	AD6	Microprocessor address[6]/DATA BUS[6]	MICOM	B	PHBCT4	MICOM
68	AD5	Microprocessor address[5]/DATA BUS[5]	MICOM	B	PHBCT4	MICOM
69	AD4	Microprocessor address[4]/DATA BUS[4]	MICOM	B	PHBCT4	MICOM
70	AD3	Microprocessor address[3]/DATA BUS[3]	MICOM	B	PHBCT4	MICOM
71	AD2	Microprocessor Address[2]/DATA BUS[2]	MICOM	B	PHBCT4	MICOM
72	AD1	Microprocessor Address[1]/DATA BUS[1]	MICOM	B	PHBCT4	MICOM
73	AD0	Microprocessor Address[0]/DATA BUS[0]	MICOM	B	PHBCT4	MICOM
74	DVSS8	Digital ground (for internal SRAM: SRAM for DP ECC use)	-	P	VSSI	-
75	SCANEN	Enable pin during scan mode test	TEST	I	PHICD50	-
76	DVDD8	Digital 3.3V power (for internal SRAM use: SRAM for DP ECC)	-	P	VDD3I	-
77	PLOCK	PLL lock indicator with HYSTERISIS	PLL	O	PHBCT4	MONI
78	PLCK	Channel bit clock(O)/EMPH(I)	PLL	B	PHBCT12SM	MONI
79	CLVLOCK	CLV lock output	CLV	O	PHOB4	MONI
80	DVSS9	Digital ground (for output PAD + PRE drive)	-	P	VSSOP	-
81	EFML/SL	Latched EFM signal(O)	PLL	O	PHOB8SM	MONI
82	GFS	Good frame sync detection flag	EFM	O	PHOB4	MONI
83	SDATAO	Serial data output	AUDIO	O	PHOB12SM	ATAPI
84	LRCKO	Sample rate clock	AUDIO	O	PHOB4	ATAPI
85	DVSS10	Digital ground (for internal logic use)	-	P	VSSI	-

Table 1. Pin Description (Continued)

No	Name	Description	Related Block	I/O	Pad Type	To/From
86	C2PO	C2 error pointer	AUDIO	O	PHOB4	ATAPI
87	BCKO	Bit clock	AUDIO	O	PHOB12SM	ATAPI
88	DVSS11	Digital ground (for output PAD + PRE drive)	-	P	VSSOP	-
89	DAOUT	Digital audio out	D/AUDIO	O	PHOT8	-
90	EXCK	Subcode data readout clock	SUB	I	PHIC	ATAPI
91	DVDD11	Digital 5.0V power (for output PAD + PRE drive)	-	P	VDD5OP	-
92	SBSO	Subcode P TO W serial output	SUB	O	PHOB4	ATAPI
93	WFCKO	Delayed WFCK (write frame clock)	SUB	O	PHOB4	-
94	DVDD11	Digital 3.3V power (for internal logic use)	-	P	VDD3I	-
95	CK50M	1-BIT DAC system clock from KS9246	DAC	I	PHIC	ATAPI
96	DVSS12	Digital ground (for output PAD + PRE drive)	-	P	VSSOP	-
97	SCORO	When either S0 or S1 is detected, SCORO is high (subcode block sync)	SUB	O	PHOB4	ATAPI
98	VSSD1	Digital ground (1-bit DAC)	DAC	P	VSSI	-
99	BCKI	Bit clock input	DAC	I	PHIC	ATAPI
100	VDDD1	Digital 3.3V power (1-bit DAC)	DAC	P	VDD3I	-
101	SDATAI	Serial digital Input data	DAC	I	PHIC	ATAPI
102	LRCKI	Sample rate clock input	DAC	I	PHIC	ATAPI
103	VSSA4	Analog ground (1-bit DAC)	DAC	P	VSSA	-
104	AOUTL	Analog output for L-CH	DAC	O	POBA	SPEAKER
105	AOUTR	Analog output for R-CH	DAC	O	POBA	SPEAKER
106	VCCA4	Analog 3.3V power (1-bit DAC)	DAC	P	VCCA	-
107	VREF	Reference voltage output for bypass	DAC	O	POBA	-
108	VHALF	Reference voltage output for bypass	DAC	O	POBA	-
109	VSSA5	Analog ground (PLL_L)	PLL	P	VSSA	-
110	PWMO	ALGC carrier frequency controlling output	PLL	O	POBA	-
111	PWMI	ALGC carrier frequency controlling input	PLL	I	PICA	-
112	VBG	PLL band gap reference monitoring output	PLL	O	POBA	-
113	VCCA5	Analog 3.3V power (PLL_L)	PLL	P	VCCA	-
114	VCTRL	VCO control voltage	PLL	I	PICA	-
115	VSSA6	Analog ground (PLL_S)	PLL	P	VSSA	-

Table 1. Pin Description (Continued)

No	Name	Description	Related Block	I/O	Pad Type	To/From
116	RDAC	Biasing resistor for IDAC at charge pump	PLL	I	PICA	-
117	RVCO	VCO V/I converting resistor	PLL	I	PICA	-
118	VCCA6	Analog 3.3V power (PLL_S)	PLL	P	VCCA	-
119	VALGC	ALGC PWM LPF output (external, DC voltage, analog level)	PLL	I	PICA	-
120	RISS	VCO bias resistance	PLL	O	POBA	-
121	VSSA7	Analog ground (data slicer)	SLICER	P	VSSA	-
122	EFMCOMP	Duty feedback slicer output	SLICER	O	POBA	MONI
123	VCCA7	Analog 3.3V power (data slicer)	SLICER	P	VCCA	-
124	LPF1	LPF input (CD X20, X40)	SLICER	I	PICA	-
125	LFP0	LPF input (CD X1, X2, X4, X8)	SLICER	I	PICA	-
126	RFI	Eye pattern from RF	SLICER	I	PICA_25_ S5L9250B	RF
127	VCCA1	Analog 3.3V power (EQ controller + motor I/F (P1-5))	-	P	VCCA	-
128	EQCTL	EQ output voltage	EQCTL	O	POBA	RF

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Spec.	Unit
DC supply voltage	VDDmax	-0.3 to +7.0	V
DC input voltage: 3.3V (internal) : 5.0V I/O	Vin3	-0.3 to 3.6	V
	Vin5	-0.3 to 5.5	
DC input current	Iin	± 10	mA
Storage Temperature	Tstg	-40 to 125	°C

ELECTROSTATIC CHARACTERISTICS

Human Body Mode

Item	Spec.	Note
VDD positive/negative	± 2000V	
VSS positive/negative	± 2000V	

MM (Machine Model) Mode

Item	Spec.	Note
VDD positive/negative	± 300V	
VSS positive/negative	± 300V	

CDM Method

Item	Spec.	Note
VDD positive/negative	±800V	
VSS positive/negative	±800V	

RECOMMENDED OPERATING CONDITIONS

No	Item		Symbol	Spec.	Unit
1	Operating temperature		Topr	0 - 70	°C
2	DC supply voltage	3.3V	VDD3	3.0 - 3.6	V
		5.0V	VDD5	4.75 5.25	V

DC CHARACTERISTICS: (VDD = 5V, VSS= 0V, Ta = 25°C)

ITEM	Symbol	Test Condition	MIN	TYP	MAX	Unit	Note
'H' input voltage1	$V_{IH(1)}$		3.5	-	-	V	(1)
'L' input voltage1	$V_{IL(1)}$		-	-	1.5	V	(1)
'H' input voltage2	$V_{IH(2)}$		2.0	-		V	(2)
'L' input voltage2	$V_{IL(2)}$			-	0.8-	V	(2)
'H' input current1	$I_{IH(1)}$	Vin = VDD	-10		10	uA	(3)
'L' input current1	$I_{IL(1)}$	Vin = VSS	-10		10	uA	(3)
'H' input current2	$I_{IH(2)}$	Vin = VDD	10	100	200	uA	(4)
'L' input current2	$I_{IL(2)}$	Vin = VSS	-200	-100	-10	uA	(5)
'H' output voltage1	$V_{OH(1)}$	I_{OH} = -2/-4/-8mA	2.4	-	-	V	(6)
'L' output voltage1	$V_{OL(1)}$	I_{OL} = 2/4/8mA	-	-	0.4	V	(6)
Tri-state output leakage current	I_{OZ}	Vout = VSS or VDD	-10	-	10	uA	(7)
Quiescent supply current	IDS	Vin = VSS			100	uA	

NOTES:

1. Related pins: All CMOS interface input terminals (PHIC)
   All tri-state bi-directional pad's input terminals (PHBCT4)
2. Related pins: All CMOS schmitt trigger input terminals (PHIS, PHISU)
3. Related pins: All input terminals, bi-directional pad's input mode terminals.
4. Related pins: All input buffers with pull-down.
5. Related pins: All input buffers with pull-up.
6. Related pins: All output terminals.
7. Related pins: Tri-state output buffer (PHBCT4)

AC CHARACTERISTICS

DATA SLICER

Item	Symbol	Spec.				Conditions
		Min	Typ	Max	Unit	
RF input size	Vrf	0.5	1.0	1.5	V	
Input resistance	Rin0	1.05	1.5	1.95	Kohm	RES[2:0] = 0H
	Rin1	1.4	2	2.6	Kohm	RES[2:0] = 1H
	Rin2	1.75	2.5	3.25	Kohm	RES[2:0] = 2H
	Rin3	2.1	3	3.9	Kohm	RES[2:0] = 3H
	Rin4	3.5	5	6.5	Kohm	RES[2:0] = 4H
	Rin5	4.55	6.5	8.45	Kohm	RES[2:0] = 5H
	Rin6	7	10	13	Kohm	RES[2:0] = 6H
	Rin7	28	40	52	Kohm	RES[2:0] = 7H
Gain input resistance	Ra1	8	10	12	Kohm	
AMP offset	Vosa	-10	0	10	mV	
Comparator open						
Loop duty error	DTe	-2	0	2	%	
COMP output resistance	Roc	0	-	100	ohm	Output current = ±1m
Switch on resistance	Ron	0	-	100	ohm	Output current = ±1m
Slice level fix						
Output rang		1.24V - 2.04V				Vref ±15 Ls
AMP gain	Ra0	-	0	-	Kohm	INLG[2:0] = 0H
	Ra1	4	5	6	Kohm	INLG[2:0] = 1H
	Ra2	8	10	12	Kohm	INLG[2:0] = 2H
	Ra3	32	40	48	Kohm	INLG[2:0] = 3H
	Ra4	72	90	108	Kohm	INLG[2:0] = 4H
	Ra5	150	190	228	Kohm	INLG[2:0] = 5H
	Ra6	232	290	348	Kohm	INLG[2:0] = 6H
	Ra7	392	490	588	Kohm	INLG[2:0] = 7H

EQUALIZER CONTROL

Item	Symbol	Spec.				Conditions
		MIN	TYP	MAX	Unit	
F/V gain	Kfv	15.35	16.5	17.66	mV/%	
F/V linearity	FVlin	-7	-	7	%	
DAC resolution	ΔVLS		26		mV	DAC output range: 0.25 × VDD - 0.75 × VDD
DAC linearity	ΔLi	-2	-	2	LSB	
DAC velocity	Ts	2.17	-	14.76	uS	
Manual control voltage		Output range: 0V - 3.3V				

PLL

Item	Symbol	Spec				Conditions
		Min	Typ	Max	Unit	
Pump UP current absolute value	IPU	2.1	2.3	2.5	mA	
Pump DN current absolute value	IPD	-2.5	-2.3	-2.1	mA	
Pump UP/DN current matching 1	IP1	-	5	10	%	
Pump UP/DN current matching 2	IP2	-	5	10	%	
VCO oscillating frequency high	OSCH	200	-	250	MHz	
VCO oscillating frequency low	OSCL	20	-	50	MHz	
Frequency division ratio 1	f40	-	45	-	MHz	
Frequency division ratio 2	f32	-	45	-	MHz	
Frequency division ratio 3	f28	-	30	-	MHz	
Frequency division ratio 4	f24	-	30	-	MHz	
Frequency division ratio 5	f20	-	22.5	-	MHz	
Frequency division ratio 6	f16	-	22.5	-	MHz	
Frequency division ratio 7	f8	-	15	-	MHz	
Frequency division ratio 8	f4	-	7.5	-	MHz	
Frequency division ratio 9	f1	-	1.875		MHz	
CD lock check	CDOK	2.8	3.8	-	V	

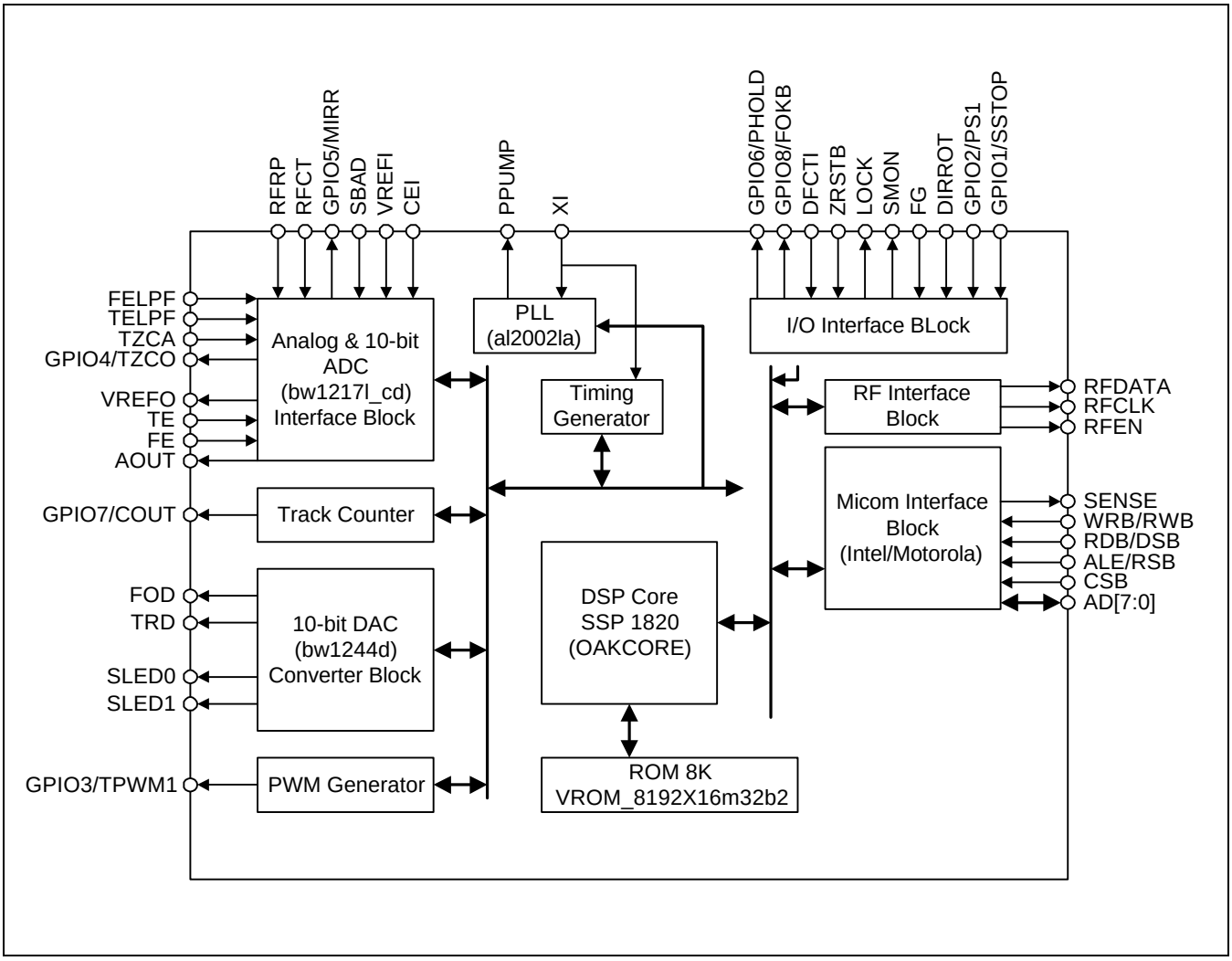
ARCHITECTURE DESCRIPTION

DIGITAL SERVO

Characteristics

- CD-ROM MAX 48X:
  CLV: 4X, 8X
  CAV: MAX 12X, 16X, 20X, 24X, 32X, 40X, 48X.
- Servo automatic adjustment:
  F/T/SBAD offset, tracking balance, focus bias, F/T loop gain
- F/T input AGC feature that adapts to work with various disc types at an optimum level
- Track search algorithm using speed control method
- Algorithm for handling defects and shocks
- Generates various servo monitor signals: FOK, MIRR, TZC, and ATSC.
- Built-in 10-bit ADC (8ch division):
  Samples FE/TE/various channels (1/16int.handling) three times at each fs.
- Built-in 4ch 10-bit DAC (for fod/trd/sled0, sled1 use)
- Disc discriminating data out (FEpk, SBADpk)
- Built-in 16-bit H/W track counter
- MICOM I/F feature: 8-bit parallel interface
- Serial interface with serial interface
  Various automatic adjusting control signals, LD on/off, etc.
- Each loop filter's coefficient selection possible through MICOM:
  focus normal/down, tracking normal/up, sled filter, various average value filter, BPF for ATSC use, BPF for loop gain automatic adjustment, etc.
- Sampling frequency: 176.4kHz
- System clock: 33.8688MHz
- 3.3V & 5.0V dual power

Block Diagram



Block Description

- Analog (A/D) interface block:
  This block receives servo errors such as focus and tracking errors, and carries out input gain control functions such as A/D conversion in order to heighten the rate of ADC deconstruction. It also has a TZC, a MIRR comparator feature, a VREF generating feature, and a built-in 8ch dividing MUX.
- Timing generator:
  The timing generator generates various timings used within the servo utilizing the external crystal 33.8688MHz. It also uses the built-in PLL's 40MHz as the basic signal for timing generation.
- I/O interface block:
  This block accepts externally generated signals such as lock and SSTOP, and outputs internally generated signals. It outputs various monitor signals such as ATSC and FOKB.
- RF interface block:
  This block transmits various automatic adjustment outputs and data needed by the RF, such as focus/tracking offset, TBAL output, AGC output, LD on/off, MICOM data, etc.
- MICOM interface block:
  This block relays data between MICOM and 8-bit parallel.
- Track counter:
  The track counter has a built-in 16-bit up/down counter to act as an accurate counter during jump.
  It is 16-bit, allowing for full stroke counting.
- DA converter block:
  This block uses a 10-bit DAC (R-string) to control the focus/tracking/sled0/sled1 at high resolution.
- Spindle PWM output:
  This output is a 1-channel PWM output for spindle control (possible with sled)
- ROM:
  This ROM is a servo program ROM with a built-in servo control program.
- DSP core for digital servo:
  This block is central to the servo. It digitally handles various emergencies such as focus/tracking loop filter handling, tracking jump, and sled move.

Register MAP and Bit Description

40x Servo Command Set for CD-ROM

Table 2. Register MAP and Bit Description

Name	Code	Description
STPcmd	00	Stop command: Stops jump or other auto adjustment-related actions.
DDTcmd	01	Disc detect command: Detects disc presence and carries out focus search.
FONcmd	02	Focus on command: Turns focus on through focus pull-in motion.
TONcmd	03	Track on command: Turns tracking on or off.
SLDcmd	04	Sled command: Controls the sled motor.
TRJcmd	05	Track jump command: Carries out track jump using the track counter.
SMVcmd	06	Sled move command: Carries out sled move using the track counter.
RPTcmd	07	Repeat jump command: Carries out interval jump using the track counter.
-	08	(Reserved).
-	09	(Reserved).
-	0A	(Reserved).
CJNCcmd	0B	CD jump number common command: Designates track number.
FGAcmd	0C	Focus gain adjustment command: Automatically adjusts focus gain.
TGAcmd	0D	Tracking gain adjustment command: Automatically adjusts tracking gain.
OFAcmd	0E	Offset adjustment command: Automatically adjusts offset of TE/FE/SBAD.
TBAcmd	0F	Tracking balance adjustment command: Automatically adjusts tracking balance.
HWofst	10	HWOFST (for center point control) adjustment command.
FBAcmd	11	Focus balance (= bias) adjustment command: Automatically adjusts focus balance.
ADScmd	12	Address setting command: Carries out upper address setting of RAM inside D-servo.
ADS1cmd	13	Address setting1 command: Sets and prepares to read lower address of RAM inside D-servo.
DScmd	14	Data setting command: Decides address status after RAM write within D-servo.
DS1cmd	15	Data setting1 command: Upper data write in RAM within D-servo.
DS2cmd	16	Data setting2 command: Lower data write in RAM within D-servo.
JMDcmd	17	Jump mode select command: Designate jump-related initial value.
JMD1cmd	18	Jump mode1 select command: Designate jump-related initial value.
JMD2cmd	19	Jump mode2 select command: Designate jump-related initial value.
JMD3cmd	1A	Jump mode3 select command: Designate jump-related initial value.
JMD4cmd	1B	Jump mode4 select command: Designate jump-related initial value.
-	1C	(Reserved).
EMEcmd	1D	Emergency command: Various emergency-related setting command.
SenLcmd	1E	If servo is active, sense is forcibly set to "L".

Table 2. Register MAP and Bit Description (Continued)

Name	Code	Description
CEoncmd	1F	Center point servo controlling command
RFcmd	20	RF command set: Transmits RF address to send serial data to the RF IC.
RF1cmd	21	RF1 command set: Transmits RF data to send serial data to the RF IC.
HWCcmd	22	Hardware control command: Controls D-servo's H/W.
HWC1cmd	23	Hardware control1 command: Controls D-servo's H/W.
-	24	(Reserved).
-	25	(Reserved).
-	26	(Reserved).
-	27	(Reserved).
-	28	(Reserved).
ECOcmd	29	Eccentricity counter command: Counters eccentricity when off track.
ECScmd	2A	Eccentricity compensation select command: Selects eccentricity compensation method when off track.
ECCcmd	2B	Eccentricity compensation control command: Controls eccentricity compensation on/off.
FTSTcmd	2C	Focus/tracking servo filter test command: Used for measuring the digital servo's filter characteristics.
DPRWcmd	2D	Direct port read/write command: Controls input/output of H/W inside D-servo.
DPWcmd	2E	Direct port write command: Writes upper 8-bit data on the H/W inside D-servo.
DPW1cmd	2F	Direct port write1 command: Writes lower 8-bit data on the H/W inside D-servo.

DETAILED BLOCK CHARACTERISTICS

Stop Command (STPcmd)

This command stops jump or auto adjustment-related servo activities, or enters into stop mode. The check priority is RST>STOP>ABRT. LDON and IDLE have the same priority.

Code	1'st byte							
00	D7	D6	D5	D4	D3	D2	D1	D0
	RST	STOP	ABRT	LDON	0	0	0	0

RST
- 0: Maintain current status.
- 1: Reset S/W (usually used during tray off).

STOP
- 0: Maintain current status.
- 1: Stop (automatically adjusted value does not change).

ABRT
- 0: Maintain current status.
- 1: Stop jump or adjustment-related servo activities.

LDON: Laser diode on/off bit (works only in stop mode).
- 0: Laser diode off.
- 1: Laser diode on.

D3-0: (Reserved). Must be set to "L".

Disc Detect Command (DDTcmd)

Laser diode is automatically turned on.
To detect if a disc is present, the focus actuator searches at the designated speed using the data RAM's FSSPD(0x20) and FSDELTA(0x21). After this command, the Fepk (S-curve/2) data and SBpk (SBAD/2)'s information are stored in the buffer so that SYSCON can read it.

Code	1'st byte							
01	D7	D6	D5	D4	D3	D2	D1	D0
	RPT	DTM1, 0		0	FPKU	0	0	0

RPT: Repeat focus search motion (only possible when DTM1, 0 = 0, 0).
0: Carry out focus search motion only once.
1: Continue focus search motion until RPT = 0, or when STOPcmd's abort bit = 1 is accepted (maintain sense = "L").

DTM1 -DTM0:
0: Carry out focus search once (auto).
01: Move the focus actuator to Vref position.
10: Raise focus actuator.
11: Lower focus actuator.

FPKU: S-curve detect location (set to 0 in manual mode).
0: Detect when down.
1: Detect when up.

- Search speed can be adjusted using the RAM's FSSPD(0x20), FSDELTA(0x21), FCNTmax(0x28), and FCNTmin(0x29).

  Search speed (1 period) = (FCNTmax-FCNTmin)*2*FSSPD/FSDELTA/Fs
- FE peak can be read through the MICOM interface after one search.
- The following are the data that MICOM can refer to after DDTcmd:
  - FEpk: FE peak data (S-curve/2).
  - SBpk: SBAD peak data (SBAD/2).

D15	D8	D7	D0
Fepk		SBpk	

Focus On Command (FONcmd)

This command carries out focus pull-in. The laser diode is turned on automatically. If focus is already on when this command is received, no further actions are taken.

Code	1'st byte							
02	D7	D6	D5	D4	D3	D2	D1	D0
	0	FONU	0	0	PIM	0	0	0

FONU: Focus pull-in location.
0: After actuator up, pull-in when down.
1: After actuator down, pull-in when up.

PIM: Pull-in method.
0: Recognize FE. Use pull-in level's absolute value.
1: Recognize FE. Use pull-in level's FEPK percentage (can be set freely using kFEok(0xfe3e) and kFEpi(0xfe3f)).

- Adjust search speed using the RAM's FSSPD(0x20), FSDELTA(0x21), FCNTmax(0x28), and FCNTmin (0x29).

  Search speed (1 period) = (FCNTmax-FCNTmin) * 2 * FSSPD/FSDELTA/Fs
- If FONcmd is accepted again during play (TRon), the tracking/sled is turned off.

Tracking On Command (TONcmd)

TONcmd is a tracking pull-in command.
If tracking is already on when this command is accepted, no further actions are taken.

Code	1'st byte							
03	D7	D6	D5	D4	D3	D2	D1	D0
	0	TON	SLDX	TFSB	TOLB1-0		0	KICK

TON: Track on/off.
0: Off.
1: On.

SLDX : Sled servo on/off.
0: Sled off.
1: Turn sled servo on after a certain time interval from tracking on.

TFSB: Eccentricity compensation pull-in control bit during track pull-in.
0: Normal pull-in.
1: Eccentricity compensation pull-in (count between the edges of TZC and pull-in where the frequency is low).

TOLB1-0: Lens brake during track pull-in and T/F gain control enable/disable.
Used for pull-in after jump using stepping motor.
0X: Off.
10: On (during normal pull-in, use the lens kick value for the lens brake time).
11: On (pull-in after the stepping motor feed kick).

KICK: KICK signal control (for stepping motor sled movement).
0: Set KICK signal to "L".
1: Set KICK signal to "H".

Sled On Command (SLDcmd)

SLDcmd is a sled motor control command. Bit check starts from the home bit.

Code	1'st byte							
04	D7	D6	D5	D4	D3	D2	D1	D0
	HOME	SMOV	SPLY	0	0	0	0	0

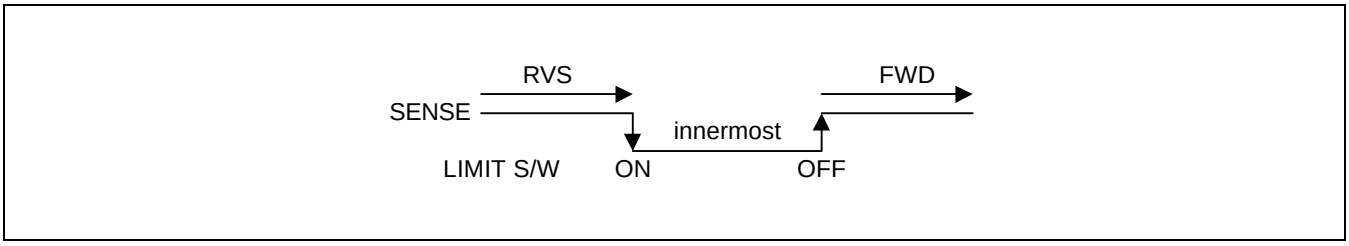
HOME: SLED HOME_IN mode select
- 0: Normal sled control mode.
- 1: Auto sled HOME_IN control mode.

When this bit is set, the sled motor moves backwards until it detects the LIMIT S/W. From then on, it moves forward for the time designated by tSLDhomein.

SMOV, SPLY: Sled on/off and sled move control bit.
- 00: Sled off
- 01: Sled on
- 10: Sled forward move
- 11: Sled backward move

D4 to 0: Reserved. Must be set to "L".

When HOME = 1 (auto sled control mode), the SENSE is as shown below.



All limit sensor data when not in auto mode are output when focus is off while the sled is moving in either direction. The limit sensor choice is made at JMD1cmd's JLIM1-0. It is "L" early in the command, but becomes

"H" when it reaches either the innermost or outermost circumference.

Track Jump Command (TRJcmd)

TRJcmd is a track jump command used for track kick/brake jump and track speed control jump.

Code	1'st byte							
05	D7	D6	D5	D4	D3	D2	D1	D0
	DIR	NUMS						

DIR: Direction you want to move in using the track counter (TC).
0: Outward movement.
1: Inward movement.

NUMS: Number of upper tracks you want to move (0x00 - 0x7F).

- The lower jump track number is designated by CJNCcmd (0B).

Sled Move Command (SMVcmd)

SMVcmd is a sled move command that is used for sled kick/brake movement and sled speed control movement.

Code	1'st byte							
06	D7	D6	D5	D4	D3	D2	D1	D0
	DIR	NUMS						

DIR: The direction you want to move in using the track counter (TC).
0: Outward movement.
1: Inward movement.

NUMS: Number of upper tracks you want to move (0x00 - 0x7F).

- The lower Jump track number is designated by CJNCcmd (0B).

1. Repeat Jump Command (RPTcmd): (Reserved).

RPTcmd is an Interval track jump command that is used during a repeating jump.

Code	1'st byte							
07	D7	D6	D5	D4	D3	D2	D1	D0
	DIR	NUMS						

DIR: Direction you want to move in using the track counter (TC).
0: Outward movement.
1: Inward movement.

DIR: Direction you want to move in using the track counter (TC).
0: Outward movement.
1: Inward movement.

NUMS: Number of upper tracks you want to move (0x00 - 0x7F).

- The lower Jump track number is designated by CJNCcmd (0B).
- The interval frequency is designated by MICOM as 16 bit (0xfeef). interval freq.= sampling freq (fs)/MICOM data
  Example) If MICOM data is h'4000, 176 kHz (fs)/h'4000 (d'16384) = 9.2 Hz

CD Jump Number Common Command (CJNCcmd)

CJNCcmd is a command that designates the track number of TRJcmd, RPTcmd (reserved), and the lower track number of SMVcmd.

Code	1'st byte							
08	D7	D6	D5	D4	D3	D2	D1	D0
	NUMS							

NUMS: The number of lower tracks you want to move (0x01 - 0xFF).

Command input method for CD when executing sled move using SMVcmd.
: Input in the order, 06xx → 0Bxx.

Focusing Gain Adjustment Command (FGAcmd)

FGAcmd is a command that adjusts the auto focus gain. Use when focus servo is on, and tracking servo on or off.

Code	1'st byte							
0C	D7	D6	D5	D4	D3	D2	D1	D0
	FGud	0	0	0	0	0	0	TFGA

FGud: Auto focus gain update
0: No update
1: When changing Kfo, Kfuo after automatic adjustment, update according to the rate of change during the automatic adjustment.

TFGA: Test mode for FGA
0: Normal FGA
1: Change focus gain once without regard to focus gain ok, then change back to the previous mode.

Tracking Gain Adjustment Command (TGAcmd)

TGAcmd is an auto tracking gain adjustment command.
Use while both focus servo and tracking servo are on.

Code	1'st byte							
0D	D7	D6	D5	D4	D3	D2	D1	D0
	TGud	0	0	0	0	0	0	TFGA

TGud: Auto tracking gain update
- 0: No update
- 1: When changing Kto, Ktuo after automatic adjustment, update according to the rate of change during the automatic adjustment.

TTGA : Test mode for TGA
- 0: Normal TGA
- 1: Change tracking gain once without regard to tracking gain ok, then change back to the previous mode.

Offset Adjustment Command (OFAcmd)

OFAcmd is an auto focus/tracking/SBAD offset Adjust command that measures and adjusts focus error, tracking error, and SBAD signal. Lens location is selected by DDTcmd's DTM1-0.

Code	1'st byte							
0E	D7	D6	D5	D4	D3	D2	D1	D0
	VREN	RFRP	SBEN	TRD0	FOD0	CEIEN	TEN	FEN

VREN: VREF offset measurement enable bit.
0: Do not measure VREF offset.
1: Measure VREF offset.

RFRP: RFRP offset measurement enable bit.
0: Do not measure RFRP offset.
1: Measure RFRP offset.

SBEN: SBAD offset measurement enable bit.
0: Do not measure SBAD offset.
1: Measure SBAD offset.

TRDO: Tracking DAC offset adjustment.
0: Do not adjust.
1: Adjust.

FODO: Focus DAC offset adjustment.
0: Do not adjust.
1: Adjust.

CEIEN: Center error offset adjustment enable bit for center point servo.
0: Do not adjust offset.
1: Adjust offset.

TEN: Tracking offset adjustment enable bit.
0: Do not adjust tracking offset.
1: Adjust tracking offset.

FEN: Focus offset adjustment enable bit.
0: Do not adjust focus offset.
1: Adjust focus offset.

- After offset measurement, subtract the Vref offset from TRD and FOD.

Tracking Balance Adjustment Command (TBAcmd)

TBAcmd averages the MAX and MIN values of TE using eccentricity while the focus is on and tracking is off. Always use before going into play (tracking on).

Code	1'st byte							
0F	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	TTBA

TTBA: Test mode for TBA

0: Normal TBA

1: Change tracking balance once without regard to tracking balance ok, then change back to previous mode.

Hardware Offset Adjust Command (HWOFSTcmd)

HWOFSTcmd is the offset adjustment command for CEI, an input signal for center point control.

Code	1'st byte							
10	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	THW0

Adjust the offset of RF's CEI output when HWOFSTcmd is accepted.

THWO: Test mode for HW offset.

0 : Normal HW offset

1: Carry out HW offset adjustment once without regard to HW offset OK, then change back to the previous mode.

Focus Balance Adjustment Command (FBAcmd)

FBAcmd uses the RF envelop signal to end focus balance adjust when the RF signal is at its maximum. Always use after focus pull-in.

Code	1'st byte							
11	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	TFBA

TFBA: Test mode for FBA.
0 : Normal FBA.
1: Carry out focus balance once without regard to focus balance ok, then change back to the previous mode.

Address Setting Command (ADScmd)

ADScmd directly accesses SRAM within the digital servo and sets the upper address during read/write. The lower address is designated by ADS1cmd.

Code	1'st byte							
12	D15	D14	D13	D12	D11	D10	D9	D8
	ADDRESS							

ADDRESS: Designates upper address of X,Y data memory.

- This command is used together with ADS1cmd that designates the lower address, and is thus always used as 2 bytes (ADScmd,ADS1cmd).

Address Setting1 Command (ADS1cmd)

ADS1cmd directly accesses SRAM within the digital servo and sets the lower address during read/write. It is always used after ADScmd.

Code	1'st byte							
13	D7	D6	D5	D4	D3	D2	D1	D0
	ADDRESS							

ADDRESS: Designates the lower address of X,Y data memory.

Data Setting Command (DScmd)

DScmd decides whether to maintain the current address or increase it by one (+1) after write, when writing data by directly accessing SRAM inside the digital servo. At this time, the SRAM address must be designated first using the ADScmd (12H).

Code	1'st byte							
14	D7	D6	D5	D4	D3	D2	D1	D0
	NEXT	0	0	0	0	0	0	0

NEXT: Determines X,Y data memory address status after data write.
0: X,Y data memory address becomes ADS1cmd and ADS2cmd's D15-0.
1: X,Y data memory address becomes ADS1cmd and ADS2cmd's D15-0 +1.

Data Setting1 Command (DS1cmd)

DS1cmd is a command that writes upper data by directly accessing SRAM, the digital servo's internal data.

Code	1'st byte							
15	D15	D14	D13	D12	D11	D10	D9	D8
	DATA							

DATA: Upper DATA selection (used together with DScmd and DS2cmd).

Data Setting2 Command (DS2cmd)

DS2cmd is a command that writes upper data by directly accessing SRAM, the Digital servo's internal data.

Code	1'st byte							
16	D15	D14	D13	D12	D11	D10	D9	D8
	ADDRESS							

DATA: Lower DATA selection (used together with DScmd and DS1cmd).

Jump Mode Select Command (JMDcmd)

JMDcmd is a jump-related initial value selection command.

Code	1'st byte							
17	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0

Jump Mode1 Select Command (JMD1cmd)

JMD1cmd is a jump-related initial value selection command.

Code	1'st byte							
18	D7	D6	D5	D4	D3	D2	D1	D0
	TCKS1-0		0	0	0	0	0	0

TCKS1-0: Clock selection bit for measuring the pull-in frequency during track pull-in.
- 00: TZC
- 01: MIRR
- 10: L_TZC
- 11: L_MIRR

Jump Mode2 Select Command (JMD2cmd)

JMD2cmd is a jump-related initial value selection command.

Code	1'st byte							
19	D7	D6	D5	D4	D3	D2	D1	D0
	LFKS	FKMOD	FSEQ	FNEQ	HYS	TGS	FDC	0

LFKS: Lens kick / Feed move select bit.
- 0: Lens kick.
- 1: Feed move.

FKMOD: When LFKS is "H", feed move type select.
- 0: Speed feedback type feed move.
- 1: Open control type feed move.

FSEQ: Usage feed search EQ in feed move.
- 0: Do not use
- 1: Use feed search EQ

FNEQ: Usage feed normal EQ in feed move.
- 0: Do not use
- 1: Use feed normal EQ

HYS: Usage hysterisis in the end of search.
- 0: Do not use
- 1: Use hysterisis

TGS: Usage tracking gain up in the end of search .
- 0: Do not use
- 1: Use tracking gain up

FDC: Add initial kick value(offset) to feed output in feed move .
- 0: Do not add
- 1: Add

Jump Mode3 Select Command (JMD3cmd)

JMD3cmd is a jump-related initial value selection command.

Code	1'st byte							
1A	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	HCRE	HCRC		HCRS

HCRE: Hardware counter reference edge.
- 0: Raising
- 1: Falling

HCRC: Hardware counter reference clock.
- 00: CK32(1.25MHz = 800ns)
- 01: CK16(2.5MHz = 400ns)
- 10: CK08(5MHz = 200ns)
- 11: CK04(10MHz = 100ns)

HCRS: Hardware counter reference signal.
- 0: TZC.
- 1: Mirr.

Jump Mode4 Select Command (JMD4cmd)

JMD4cmd is a jump-related initial value selection command.

Code	1'st byte							
1B	D15	D14	D13	D12	D11	D10	D9	D8
	RVSB	VCMP	VEDG		VPRDR		VCLKS	

RVSB: Reverse check selection during jump.
- 0: If there are less remaining tracks than RVSnum(0xbe) during reverse, stop the jump.
- 1: Do not carry out reverse check.

VCMP: 1 counter compensation (when count is "H").
- 0: Do not compensate.
- 1: Compensate.

VEDG: Standard edge selection for the velocity jump period counter.
- 00: Falling & Rising
- 01: Falling
- 10: Rising
- 11: Falling & Rising

VPRDR: Velocity jump period standard signal (H/W counter and kick/brake standard clock also change).
- 00: TZC
- 01: MIRR
- 10: L_TZC (L_MIRR selected for H/W counter and kick/brake standard clock).
- 11: L_MIRR

VCLKS: Velocity clock select
- 00: CK32 (1.25MHz = 800ns)
- 01: CK16 (2.5MHz = 400ns)
- 10: CK08 (5MHz = 200ns)
- 11: CK04 (10MHz = 100ns)

Jump Mode5 Select Command (JMD5cmd) : Reserved

JMD5cmd is a jump-related initial value selection command.

Code	1'st byte							
1C	D15	D14	D13	D12	D11	D10	D9	D8
	0	0	0	0	0	0	0	0

Emergency Command (EMEcmd)

EMEcmd handles emergencies such as shock.

Code	1'st byte							
1D	D7	D6	D5	D4	D3	D2	D1	D0
	FATS	TATS	LATS	SLOCK	0	0	0	0

FATS: The bit that decides whether or not to change focus gain during a shock.
- 0: Maintain focus gain at normal.
- 1: Change focus gain.

TATS: The bit that decides whether or not to change tracking gain during a shock.
- 0: Maintain tracking gain at normal.
- 1: Change tracking gain.

LATS: Lens brake control bit during anti-shock.
- 0: Lens brake off.
- 1: Lens brake on.

SLOCK: Sled control bit when lock signal is off.
- 0: Stop sled.
- 1: Do not stop sled.

Sense L Command (SenLcmd)

Forcibly sets sense to "L" during a servo command.

Code	1'st byte							
1E	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0

When a command is accepted to read internal RAM data while a servo command such as gain control is being executed, sense becomes "H" even when the servo command is not yet finished. In such a case, the SenLcmd checks the internal status and reconsiders sense status.

Center Point Servo Control Command (CEcmd)

CEcmd controls the center point servo.

Code	1'st byte							
1F	D7	D6	D5	D4	D3	D2	D1	D0
	CEonb	0	0	0	0	0	0	0

CEonb: Center point servo control bit.

0: Center point servo filter on.

1: Generate center point brake signal (output level and time are decided by CEbrklvl(170h) and CEbrkTM(171h)).

RF Command (RFcmd)

RFcmd transmits the RF address in order to send serial data to the RF IC.

Code	1'st byte							
20	D15	D14	D13	D12	D11	D10	D9	D8
	RF ADDRESS							

RF address 01H:
- RFEQ_SEL
- MODE_SEL (CD-ROM/CD-RW)
- ABCD_ATT

RF address 02H:
- EQG_CEN
- C48_SEL
- CAV_SEL
- AGC_LVL

RF address 03H:
- AGCON
- AGCIN_Z
- PUP_SEL

GAIN_PLLF

RF address 04H:
- TE_LPF
- TE_ATT

RF address 05H:
- FE_LPF
- FE_ATT

RF address 06H:
- SERVO_OFST

RF address 07H:
- TBAL

RF address 08H:
- RFRP_FREQ
- DFT_TH
- RFRP_TH

RF address 09H:
- SBAD_ATT

RF address 0AH:
- LD_ON

RF address 0BH:
- RFRP_SEL

RF address 0FH:
- PDMODE

- This command is used together with RF1cmd, and thus always used as 2 bytes (RFcmd,RF1cmd).

RF1 Command (RF1cmd)

RF1cmd transmits the RF address in order to send serial data to the RF IC.

Code	1'st byte							
21	D7	D6	D5	D4	D3	D2	D1	D0
	RF DATA							

When RF address = 01H:
- D7-4 (RFEQ_SEL): EQ speed selection bit.
- D2-0 (ABCD_ATT): ABCD ATT gain selection bit.

When RF address = 02H:
- D7 (reserved).
- D6-4 (EQG_CEN): Center gain detailed adjustment selection bit for EQ boost gain.
- D3 (C48_SEL): 4x, 8x selection bit.
  - 0: 4x
  - 1: 8x
- D2 (CAV_SEL): CAV, CLV selection bit.
  - 0: CAV
  - 1: CLV
- D1-0 (AGC_LVL): RFAGC amp output level selection bit.

When RF address = 03H:
- D7(AGCON) : RF AGC 0N/OFF selection bit.
  - 1: RFAGC ON
  - 0: RFAGC OFF
- D6-4(AGCIN_Z): RFAGC input impedance selection bit.
- D3 (PUP_SEL) : RF_SUM or A, B, C, D selection bit.
  - 0: RFSUM pick_up
  - 1: A, B, C, D pick_up
- D2-0 (GAIN_PLLF): Selection bit for RF EQPEAK frequency change sensitivity according to PLLF voltage.

When RF address = 04H:
- D7-6 (reserved).
- D5-4 (TE_LPF): TE LPF frequency selection bit.
- D3 (reserved).
- D2-0 (TE_ATT): TE ATT gain selection bit.

When RF address = 05H:
- D7-6 (reserved).
-D7-6 (FE_LPF): FE LPF frequency selection bit.
- D3 (reserved).
D2-0 (FE_ATT): FE ATT gain selection bit.

When RF address = 06H:
D7-0 (SERVO_OFST): Servo offset control bit.

When RF address = 07H:
- D7-0 (TBAL): Tracking balance control bit.

When RF address = 08H:
- D7-6 (RFRP_FREQ): RFRP peak-bottom hold frequency selection bit.
- D5-3 (DFT_TH): Defect slice level selection bit.
- D2-0 (RFRP_TH): RFRP slice level selection bit.

When RF address = 09H:
- D7-3 (reserved).
- D2-0 (SBAD_ATT): SBAD's output gain selection bit.

When RF address = 0AH:
- D7-1 (reserved).
- D5 (LD_ON) : LD's on/off selection bit.
  - 0: LD OFF
  - 1: LD ON

When RF address = 0BH:
- D7-1 (reserved).
- D0 (RFRP_SEL): RFRP block output selection bit.
  - 0: RFRP, RFCT
  - 1: ENVELOPE

When RF address = 0FH:
- D7-1 (reserved).
- D4 (MODE_SEL): CD-RW, CD-ROM selection bit.
  - 0: CD-RW
  - 1: CD-ROM
- D0 (PDMODE): Power down mode selection bit.
  - 0: Power down mode
  - 1: Normal mode

Hardware Control Command (HWCcmd)

HWCcmd controls the H/W inside the Digital Servo.

Code	1'st byte							
22	D7	D6	D5	D4	D3	D2	D1	D0
	0	SINT2-0			HTDEN1-0		HFDEN1-0	

FRSEL: (D7 reserved). Free running counter select.
0: INT1 select (4-bit counter)
1: INT2 select (3-bit or 2-bit counter according to INTSEL1)

SINT2-SINT0: INT1's division rate selection.
000: INT1b = XIN / 192 - default
001: INT1b = XIN / (192+16*1)
010: INT1b = XIN / (192+16*2)
-- : --
111: INT1b = XIN / (192+16*7)

HTDEN1-0: Tracking defect handling enable bit.
00: Do not use tracking defect handling.
01: Always use tracking defect handling when a defect is found.
10: Use tracking defect handling only when CLV lock.
11: Do not use tracking defect handling.

HFDEN1-0: Focus defect handling enable bit.
00: Do not use focus defect handling.
01: Always use focus defect handling when a defect is found.
10: Use focus defect handling only when CLV lock.
11: Do not use focus defect handling.

- This command is used together with HWC1cmd, and is always used as 2 bytes (HWCcmd, HWC1cmd).

Hardware Control1 Command (HWC1cmd)

HWC1cmd controls the H/W inside the digital servo.

Code	1'st byte							
23	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	DACEN	0	1	HDFMK	HKSMK	HSHMK

DACEN: DAC output enable.
- 0: VREF output to DAC.
- 1: Normal DAC.

HDFMK: Chooses whether or not to output the defect signal to the PHOLD pin.
- 0: Do not output defect signal (default).
- 1: OR the shock signal, kick and defect signal, then output.

HKSMK: Chooses whether or not to output the kick signal to the PHOLD pin.
- 0: Do not output kick signal (default).
- 1: OR the shock signal, defect and kick signal, then output.

HSHMK: Chooses whether or not to output the shock signal to the PHOLD pin.
- 0: Do not output shock signal (default).
- 1: OR the defect signal, kick and shock signal, then output.

Eccentricity Counter Command (ECOcmd)

ECOcmd counts tracking errors for one disc revolution, for the purpose of measuring the amount of eccentricity for eccentricity compensation during OFF track status.

Code	1'st byte							
29	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0

The counted value is stored in data RAM 49h.

Eccentricity Compensation Select Command (ECScmd)

ECScmd selects the eccentricity compensation method. The eccentricity compensation routine starts automatically when this command is accepted.

Code	1'st byte							
2A	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0

Stores and uses the eccentricity value for one disc revolution at each fs/N.

Eccentricity Compensation Control Command (ECCcmd)

ECCcmd controls the eccentricity compensation ON/OFF.

Code	1'st byte							
2B	D7	D6	D5	D4	D3	D2	D1	D0
	ECC	0	0	0	0	0	0	0

ECC: Eccentricity compensation ON/OFF control bit.
- 0: OFF.
- 1: ON.

Focus/Tracking Servo Filter Test Command (FTSTcmd)

FTSTcmd is a test command for measuring the digital servo's filter characteristics.

Code	1'st byte							
2C	D15	D14	D13	D12	D11	D10	D9	D8
	0	0	0	WTF	0	0	0	WFF

WTF: Tracking filter test.
- 0: Tracking filter normal test.
- 1: Tracking filter up test.

WFF: Focus filter test.
- 0: Focus filter normal test.
- 1: Focus filter down test.

- However, the input of the sled filter test becomes TE.

Direct Port Read/Write Command (DPRWcmd)

DPRWcmd is a command for directly reading the IN/OUT buffer within the digital servo, or writing DPWcmd and DPW1cmd's 16-bit data.

Code	1'st byte							
2D	D7	D6	D5	D4	D3	D2	D1	D0
	WRB	DPS6-0						

WRB: IN/OUT buffer read/write selection.
0: Read the IN/OUT buffer inside the digital servo.
1: Write DPWcmd and DPW1cmd's 16-bit data on the IN/OUT buffer inside the digital servo.

DPS6-0: Chooses which port to read/write, combined with WRB.

- This command inputs DPWcmd that shows the upper address and the DPW1cmd that shows the lower address, and uses them as a total of 3 bytes.
- Data Read

h'2D00: Read the value of the STRD1 (external status1 read) buffer.
h'2D01: Read the value of the STRD (external status read) buffer.
h'2D02: Read the value of the VCTRD (free running counter for 1/16 use) buffer.
h'2D03: Read the value of the VCTRD1(free running counter for Dfct use) buffer.
h'2D04: Read the value of the CMDRD (MICOM command read) buffer.
h'2D05: Read the value of the MDRD (MICOM data read) buffer.
h'2D06: Read the value of the TMCNTRD (TZC, MIRR's edge to edge counter value read for speed control) buffer.
h'2D07: (Reserved).
h'2D08: Read the value of the CNTRD (Hardware counter value read) buffer.
h'2D09: Read the value of the ADCRD (AD conversion value read) buffer.
h'2D0A: Read the value of the CLVFRD (CLV frequency data) buffer.
h'2D0B: Read the value of the CLVPRD (CLV phase data) buffer.
h'2D0C: Read the value of the FERD (FE AD conversion value read) buffer.
h'2D0D: Read the value of the TERD (TE AD conversion value read) buffer.
h'2D0E: Read the value of the CEIRD (CEI AD conversion value read) buffer.
h'2D0F: Read the value of the ADI1RD (ADI1 AD conversion value read) buffer.
h'2D10: Read the value of the ADI2RD (ADI2 AD conversion value read) buffer.
h'2D11: Read the value of the SBADRD (SBAD AD conversion value read) buffer.
h'2D12: Read the value of the RFRPRD (RFRP AD conversion value read) buffer.
h'2D13: Read the value of the VREFRD (VREF AD conversion value read) buffer.
h'2D14-h'2D18: (Reserved).
h'2D19: Read the value of the MODATRD(GPIO 8, 7, 6, 5, 4 input data read) buffer
h'2D1A-h'2D1E: (Reserved).

- Data Write Method

h'2D80: Write the value in the ASEL (Analog select and ADC start) buffer.
h'2D81: Write the value in the TRD (DAC out for tracking drive) buffer.
h'2D82: Write the value in the CTL1 (H/W control out1) buffer.
h'2D83: Write the value in the CTL (H/W control out) buffer.
h'2D84: Write the value in the FOD (DAC out for focus drive) buffer.
h'2D86: Write the value in the SPD (9-bit PWM out for spindle drive) buffer.
h'2D87: Write the value in the FIG (Focus input gain control) buffer.
h'2D88: Write the value in the TIG (Tracking input gain control) buffer.
h'2D89: Write the value in the SLEDO (10-bit DAC for test) buffer.
h'2D8A: Write the value in the CNTRB (Tracking counter reset) buffer.
h'2D8B: Write the value in the MDWR (MICOM data write) buffer.
h'2D8C: Write the value in the RFCMD (RF data out) buffer.
h'2D8D: Write the value in the TMCTL (TZC/MIRR divide control) buffer.
h'2D8E: Write the value in the PRCNT (Reference track number setting for jump) buffer.
h'2D91: Write the value in the TDFCT (Defect delay load) buffer.
h'2D92: Write the value in the TLD1 (INT0b down counter1 load) buffer.
h'2D93: Write the value in the TLD2 (INT0b down counter2 load) buffer.
h'2D94: Write the value in the TLD3 (INT0b down counter3 load) buffer.
h'2D95: Write the value in the TLD4 (INT0b down counter4 load) buffer.
h'2D96: Write the value in the TLD5 (INT0b down counter5 load) buffer.
h'2D97: Write the value in the TLD6 (INT0b down counter6 load) buffer.
h'2D98: Write the value in the TRD_AVR (TRD average data for H/W lens brake) buffer.
h'2D99: Write the value in the MODAT (GPIO 8, 7, 6, 5, 4 output write) buffer.
h'2D9A: Write the value in the HWCMD (H/W command out) buffer.
h'2D9B: Write the value in the SLED1 (10-bit DAC1 for test) buffer.
h'2D9C: Write the value in the PLLCMD (PLL divition ratio control out) buffer.
h'2D9D: Write the value in the MOCTL (GPIO 8, 7, 6, 5, 4 in/out control) buffer.
h'2D9E: Write the value in the MOSEL (GPIO 8, 7, 6, 5, 4 data select) buffer.
h'2D9F-2DFF: (Reserved).

Direct Port Write Command (DPWcmd)

DPWcmd is a command that shows the upper 8-bit address for writing on the IN/OUT buffer within the digital servo using DPRWcmd.

Code	1'st byte							
2E	D15	D14	D13	D12	D11	D10	D9	D8
	D15-8							

Direct Port Write1 Command (DPW1cmd)

DPW1cmd is a command that shows the lower 8-bit address for writing on the IN/OUT buffer within the digital servo using DPRWcmd.

Code	1'st byte							
2F	D7	D6	D5	D4	D3	D2	D1	D0
	D7-0							

General Purpose MICOM Control Port Command (GPIOmicmd)

The GPIOmicmd controls the IN/OUT of the general purpose PAD (GPIO3, GPIO2, GPIO1, GPIO0) through MICOM command.

D2, D1, D0 = 1 (H/W is set as GPIO2, 1, 0 input/default),
= 0 (GPIO2, 1, 0 output mode select)

D3 = 1 (H/W is set as GPIO3 input/default),
= 0 (GPIO3 output mode select)

D4 = 0 (H/W is set as internal GPIO3 PWM output/default/ D3 = 1),
= 1 (GPIO3 output mode by MICOM 3C register/ D3 = 0, mode select)

Code	1'st byte							
3B	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	gpio_pwm_en [4]	gpio3_towm1 [3]	gpio2_PS1 [2]	gpio1_SSTOP [1]	gpio0-en [0]
CONTROL					gpio_en_mi [3]	gpio_en_mi [2]	gpio_en_mi [1]	gpio_en_mi [0]

General Purpose MICOM Data Read/Write Command (GPIOdatcmd: R/W)

MICOM writes data on the 3-ch register and outputs DATA(md[3:0]) to the general purpose pad (GPIO3, GPIO2, GPIO1, GPIO0). (output mode is controlled by the 3Bh register.)

General purpose pad (GPIO3, GPIO2, GPIO1, GPIO0)'s input status (md[3:0)) is stored in the 3-ch register so that MICOM can read it (input mode is controlled by the 3Bh register).

* When reading the 3C register, GPIO3 is for PWM output and GPIO0 is for reserved Input.

Code	1'st byte							
3C	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	md[3]	md[2]	md[1]	md[0]

Sled DAC Output Control Command (SLDCTLcmd)

SLDCTLcmd controls the output of DAC (SLED0, SLED1).

D2 = 1(SERVO DATA), = 0 (MICOM DATA)/D1, D0 = 1 (DAC VREF), = 0 (DAC DATA) output

Code	1'st byte							
3D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	mi/servo	sld1	sld0

SLED0 DAC MICOM Data Write Command (SLED0micmd)

SLEDOmicmd writes DAC(SLED0)'s MICOM data.

Code	1'st byte							
3E	D7	D6	D5	D4	D3	D2	D1	D0
	SLED0miDATA[7:0]							

SLED1 DAC MICOM Data Write Command (SLED1micmd)

SLED1micmd writes DAC(SLED1)'s MICOM data.

code	1'st byte							
3F	D7	D6	D5	D4	D3	D2	D1	D0
	SLED1miDATA[7:0]							

DETAILED BLOCK CHARACTERISTICS

General Purpose Pad

< Control by MICOM Command >

— The control initial value is set to the default (H/W) input (address 'h3B, data 'h0F).

— When in input mode: Set to input mode by MICOM 'h3B0F/gpio3 PWM output, gpio2, 1, 0 input

PWM output by TPWM1 or sled0 (OAK command)/PS1, SSTOP(PS0) input/reserved input

— When in output mode: Set to output mode by MICOM 'h3B10, then output X DATA[3:0] by MICOM 'h3CX command.

PORT	gpio3	gpio2	gpio1	gpio0
Control	gpio_en_mi[3]	gpio_en_mi[2]	gpio_en_mi[1]	gpio_en_mi[0]
Input	TPWM1	PS1	SSTOP(PS0)	-
Output	gpio_md[3]	gpio_md[2]	gpio_md[1]	gpio_md[0]

< Control by OAK COMMAND >

— The control initial value is set to the default (H/W) input (MOCTL = 1).

— When in input mode: MOCTL = 1 (GPIO8, 7, 6, 5, 4 input).

After MOSEL = 1 (input data select), set to MODAT = 1 (data latch) so that MODATRD = 1 (data read).

— When in input mode: MOCTL = 0 (GPIO8, 7, 6, 5, 4 output).

Set to MOSEL = 0 (output data select) FOKB, COUT, PHOLD, MIRR, TZCO moniter.

PORT	gpio8	gpio7	gpio6	gpio5	gpio4
Control	MOCTL(db[12])	MOCTL(db[11])	MOCTL(db[10])	MOCTL(db[9])	MOCTL(db[8])
Input	Mo_data(db[4])	Mo_data(db[3])	Mo_data(db[2])	Mo_data(db[1])	Mo_data(db[0])
Output	FOKB	COUT	PHOLD	MIRR	TZCO

< OAK Address Decoding/Address Description >

Description	Address	Read (IORN)	DB_Out[15:0]	Write (IOWN)	DB_IN[15:0]
User IO EXT register EXT[5:0]	14 (ext0)	STRD1	dB[15:0]	ASEL	dB[2:0]
	15 (ext1)	STRD	dB[15:0]	TRD	dB[15:6]
	16 (ext2)	VCTRD	dB[15:0]	CTL1	dB[15:0]
	17 (ext3)	VCTRD1	dB[15:0]	CTL	dB[15:0]
Data bus address [15:0]	0800	CMDRD	dB[7:0]	FOD	dB[15:6]
	0801	MDRD	dB[15:8]	-	-
	0802	TMCNTRD	dB[15:0]	SPD	dB[15:8]
	0803	-	-	FIG	dB[14:10]
	0804	CNTRD	dB[15:0]	TIG	dB[14:10]
	0805	ADCRD	dB[15:6]	SLED0	dB[15:6]
	0806	CLVFRD	dB[15:0]	CNTRB	-
	0807	CLVPRD	dB[15:0]	MDWR	dB[15:0]
	0808	FERD	dB[15:6]	RFCMD	dB[15:0]
	0809	TERD	dB[15:6]	TMCTL	dB[12:0]
	080A	CEIRD	dB[15:6]	PRCNT	dB[15:0]
	080B	ADI1RD	dB[15:6]	-	-
	080C	ADI2RD	dB[15:6]	-	-
	080D	SBADRD	dB[15:6]	TDFCT	dB[15:0]
	080E	RFRPRD	dB[15:6]	TLD1	dB[15:0]
	080F	VREFRD	dB[15:6]	TLD2	dB[15:0]
	0810	-	-	TLD3	dB[15:0]
	0811	-	-	TLD4	dB[15:0]
	0812	-	-	TLD5	dB[15:0]
	0813	-	-	TLD6	dB[15:0]
	0814	-	-	TRD_AVR	dB[15:6]
	0815	MODATRD	dB[4:0]	MODAT	dB[12:8]
	0816	-	-	HWCMD	dB[15:0]
	0817	-	-	SLED1	dB[15:6]
	0818	-	-	PLLCMD	dB[15:0]
	0819	-	-	MOCTL	dB[12:8]
	081A	-	-	MOSEL	dB[12:8]

RF Serial Interface

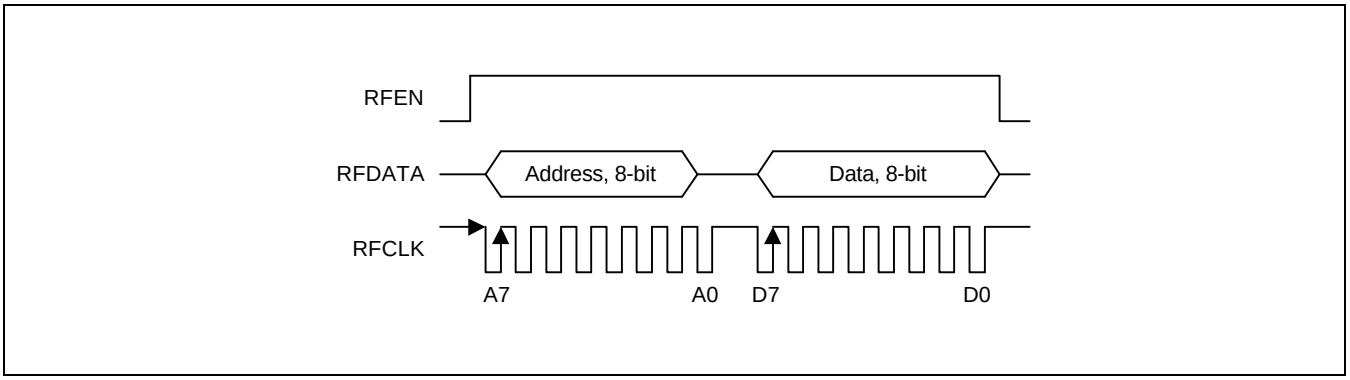
There are 2 methods of sending data to the RF IC:

- MICOM: If you send 16-bit data to the XXh address of the MICOM interface within the servo, the DSP uses the RFCcmd through the RF interface to transmit data.
- Servo: If you write data from the servo CPU to the RFcmd, the data is transmitted through the RF interface.

However, the RF interface is a serial interface, so when you send the next RF command, you must make sure that the sense is "H" for MICOM, or that you write to RFcmd after CK6 * 20 clocks for servo.

Address	Data																Notes
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
XXh	RF Address								RF data								

— Serial Port Data Transfer Format



Serial Port Data Transfer Format

HOME IN

Summary

When using the REVERSE SLED MOVE to move the P/U from the starting point to the innermost circumference, and the PS signal does not occur after a certain amount of time, HOME IN is assumed. If so, the P/U goes into FORWARD MOVE long enough to escape the LEAD IN area and finishes the task.

— Input signal : PS0, PS1

— Output signal : SLD

Command (0x04hh)

Code	1'st byte							
04	D7	D6	D5	D4	D3	D2	D1	D0
	HOME	SMOV	SPLY	0	0	0	0	0

HOME : SLED HOME_IN MODE selection
0 : Normal SLED CONTROL MODE.
1 : AUTO SLED HOME_IN CONTROL MODE.
When this bit is set, the Sled Motor continues BACKWARD MOVE until it detects LIMIT S/W. From then on, it carries out FORWARD MOVE for the time designated by tSLDhomein.

SMOV,SPLY : Controls Sled On/Off and Sled move.
00 : Sled Off
01 : Sled On
10 : Sled Forward move
11 : Sled Backward move

D4 to 0 : Reserved. Must set to "L".

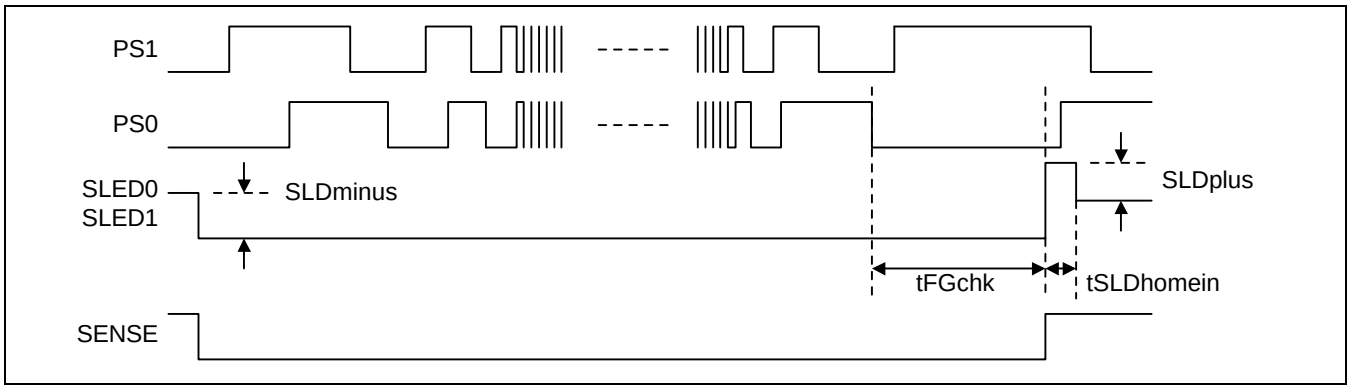
→ For sense output excepting AUTO mode, the limit sensor data is output in focus off status during the sled's inward/outward movement. The limit sensor selection is made by JMD1cmd's JLIM1 - 0. It is "L" early in the command, but becomes "H" once it reaches the innermost/outermost circumference.

Related Memory

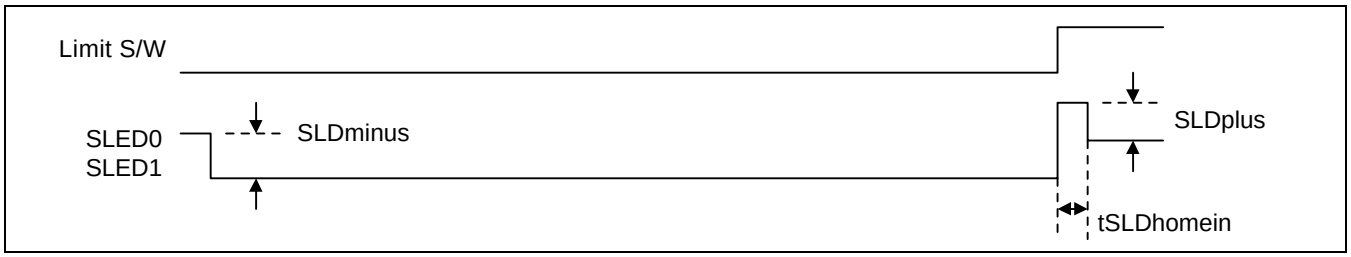
NAME	ADDR.	FUNCTION	Data	Value
SLDminus	00A0	Sled minus kick level	0 × F800	188mV
SLDplus	00A1	Sled plus kick level	0 × 0800	188mV
tSLDhomein	0031	Forward jump time after sled home in	0 × 0010	5.6 µs*16
tFGchk	0032	FG limit time	0 × 1000	22.9 ms
JMD01buf	001C	Jump mode buffer (FG,L s/w select)		

Operation Description

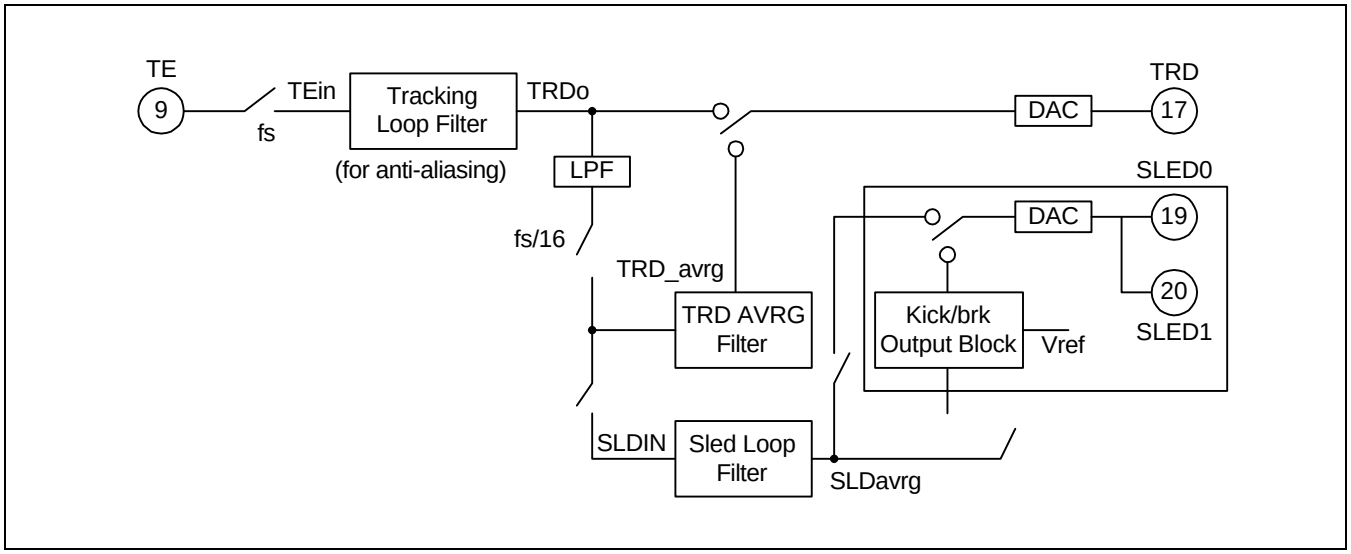
— The sled is moved in reverse direction. If there is no signal change in FG1 or FG0 (present) for a period of time (tFGchk), the Sled output is put into Forward Kick for the length of tSLDhomein, and reverted to Vref.



— HOME IN Detection by LIMIT S/W (When you have no Sled Encoder):
LIM is set to "H" (sled stopped by LIMIT S/W) when there is LIMIT S/W. DSSP's PS0 pin changes its function to SSTOP, and LIMIT S/W becomes connected to this block.



· **Home In Block Diagram**



SAMSUNG ELECTRONICS

OFFSET ADJUST

- **Summary**

The DSSP measures and averages the FE/TE Offset between the SERVO+DSAP chip (S5L9250B) and RF chip (KS9251), stores it in the Register, then uses it in later filter operations to reduce remaining error deviations caused by offset.

— Output Register : Each register

Command (0x0Ehh)

Code	1'st byte							
0E	D7	D6	D5	D4	D3	D2	D1	D0
	VREV	RFRP	SBEN	TRDO	FODO	CEIEN	TEN	FEN

VREV : VREF offset measurement enable bit.
0 : Do not measure VREF offset.
1 : Measure VREF offset.

RFRP : RFRP offset adjustment enable bit.
0 : Do not adjust RFRP offset.
1 : Adjust RFRP offset.

SBEN : SBAD offset adjustment enable bit.
0 : Do not adjust SBAD offset.
1 : Adjust SBAD offset.

TRDO : Tracking DAC offset adjustment bit.
0 : Do not adjust tracking DAC offset.
1 : Adjust tracking DAC offset.

FODO : Focus DAC offset adjustment bit.
0 : Do not adjust focus DAC offset.
1 : Adjust focus DAC offset.

CEIEN : Center error offset adjustment enable bit for center point servo use.
0 : Do not adjust offset.
1 : Adjust offset.

TEN : Tracking offset adjustment enable bit.
0 : Do not adjust Tracking offset.
1 : Adjust Tracking offset.

FEN : Focus offset adjustment enable bit.
0 : Do not adjust Focus offset.
1 : Adjust Focus offset.

→ Subtract Vref offset from TRD and FOD after measuring the offset.

Related Memory

Name	Addr.	Function	Data	Value
FEofst	0090	FE offset		
TEofst	0091	TE offset		
CEIofst	0092	CEI offset		
SBADofst	0093	SBAD offset		
RFRPofst	0094	RFRP offset		
FODofst	0068	FOD offset		
TRDofst	0069	TRD offset		
Vref	0035	VREF DATA		
OFSTwt	004E	offset stable time	0×0040	
OFSTacc	004F	offset acculating time	0×0100	
Kofstg	FEF4	offset input gain	0×0400	
Kofst	FEF5	K1	$0 \times 7C00$	
Sofst	FEF6	Shift (select) offset	0×0007	

DISC DETECTION

Summary

The Laser diode is automatically turned On. To detect disc presence, the Focus Actuator searches at a designated speed (FSSPD (0x20), FSDELTA (0x21)). The FOD outputs delta waves to move the Actuator up and down. After this command, information such as FEpk (S-curve/2)data and SBpk (SBAD/2) are stored in the buffer so that SYSCON can read it.

— Input signal : FE,SBAD

— Output signal : FOD, FOKB, MIOUT (data)

Command (0x01XX)

: The Laser diode is automatically turned On. To detect disc presence, the Focus Actuator searches at a designated speed (FSSPD(0x20), FSDELTA (0x21)). After this command, information such as Fepk (S-curve/2)data and SBpk (SBAD/2) are stored in the buffer so that SYSCON can read it.

Code	1'st byte							
01	D7	D6	D5	D4	D3	D2	D1	D0
	RPT	DTM1,0		0	FPKU	0	0	0

RPT : Repeat of Focus Search movement.
0 : Execute only once.
1 : Continue (maintain sense = "L") until receiving DDTcmd (RPT = 0).

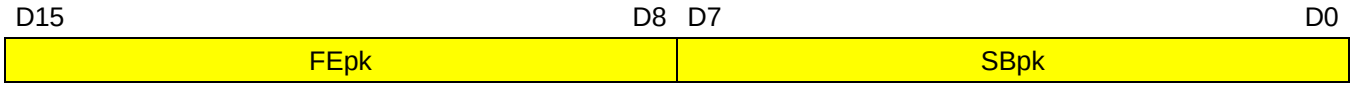
DTM1 — DTM0 :
00 : Execute Focus Search once (AUTO).
01 : Move Focus Actuator to Vref location.
10 : Raise Focus Actuator.
11 : Lower Focus Actuator.

FPKU : S-curve detect location (use during AUTO search).
0 : Detect when Down.
1 : Detect when Up.

→ Search Speed is adjusted using RAM's FSSPD (0x20) FSDELTA (0x21).
Search Speed = 10mv/(128fs * FSSPD/FSDELTA)

→ After SEARCH has been executed once, FE PEAK can be read through the MICOM Interface.

→ Data that MICOM can refer to after DDTcmd.



— FEpk : FE peak data (S-curve/2).

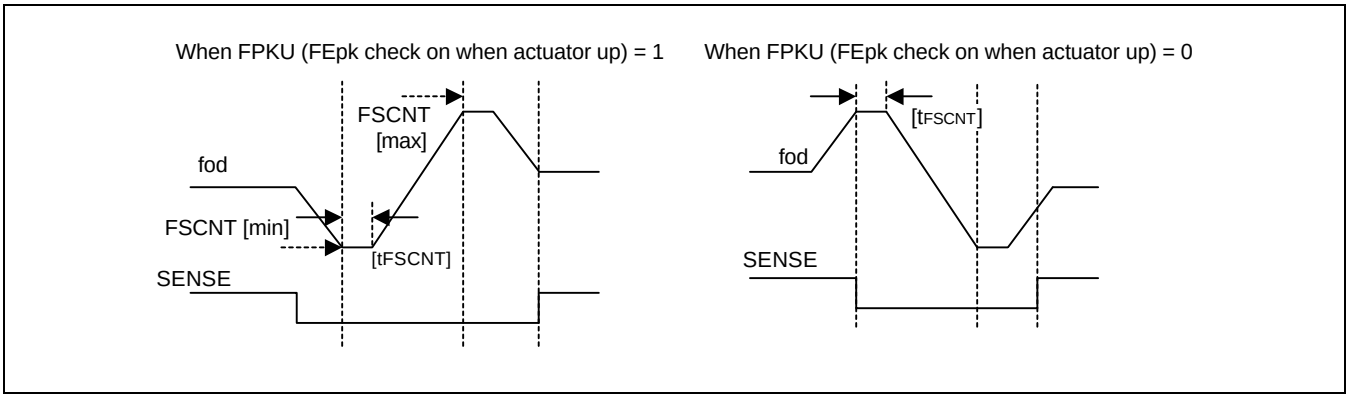
— SBpk : SBAD peak data (SBAD/2).

Related Memory

Name	Address	Function	Data	Value
DDTbuf	001A	DDT command buffer		
FSSPD	0020	Focus Search speed	0 × 0001	
FSDELTA	0021	Focus Search delta	0 × 0008	
FSCNT	0022	Focus Search counter		
FEMAX	0023	FE max data		
FEMAXp	0024	FECNT when FEmax		
FEMIN	0025	FE min data		
FEMINp	0026	FECNT when FEmin		
FEPK	0027	FEpp/2		
FSCNTmax	0028	Focus Search output max	0 × 1800	
FSCNTmin	0029	Focus Search output min	0 × E800	
SBADMAX	002A	SBAD max data		
SBADMIN	002B	SBAD min data		
SBADPK	002C	SBADpp/2		
tFSCNT	002D	Focus Search Wait Time	0 × 2000	
FE	0062	Focus error		

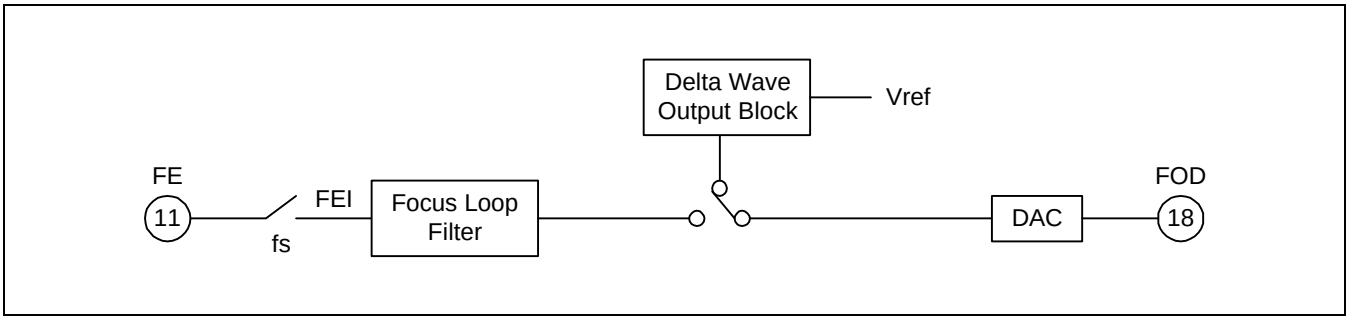
OPERATION DESCRIPTION

When the Disc Detect command is input, the output signal FOD starts from the Vref voltage to output a delta waveform as shown in the figure below. At this time, Up/Down Detect is decided by Auto Search Mode. Search Speed or slope is decided by FSSPD and FSDELTA, and the upper and lower limit duration is determined by tFSCNT.



— Disc Detection
Disc presence and type are detected by the Focus Search command. After command, MICOM reads FEpk and SBADpk.

Disc Detection Block Diagram



FOCUS PULL-IN

Summary

Delta waves are output from FOD to move the ACTUATOR up and down. FOCUS PULL-IN is executed near the FE(S_CURVE) signal's ZERO CROSS area.

- Input signal : FE, SBAD
- Output signal : FOD, FOKB

Command (0x02hhhh)

: This is a Focus Pull-in enabling command. The Laser diode is automatically turned on. If focus is already on when this command is received, no further actions are taken.

Code	1'st byte							
02	D7	D6	D5	D4	D3	D2	D1	D0
	0	FONU	0	0	PIM	0	0	0

FONU: Focus Pull-in location.
0 : Pull-in at Down after Actuator Up.
1 : Pulll-in at Up after Actuator Down.

PIM : Pull In Method.
0 : FE recognized. Absolute value of pull-in level used.
1 : FE recognized. Pull-in level's FEPK's percentage used (Can be freely set using RAM's buffer).

→ Search Speed is adjusted using RAM's FSSPD(0x20) FSDELTA (0x21).
Search Speed = 10mv/(128fs * FSSPD/FSDELTA)

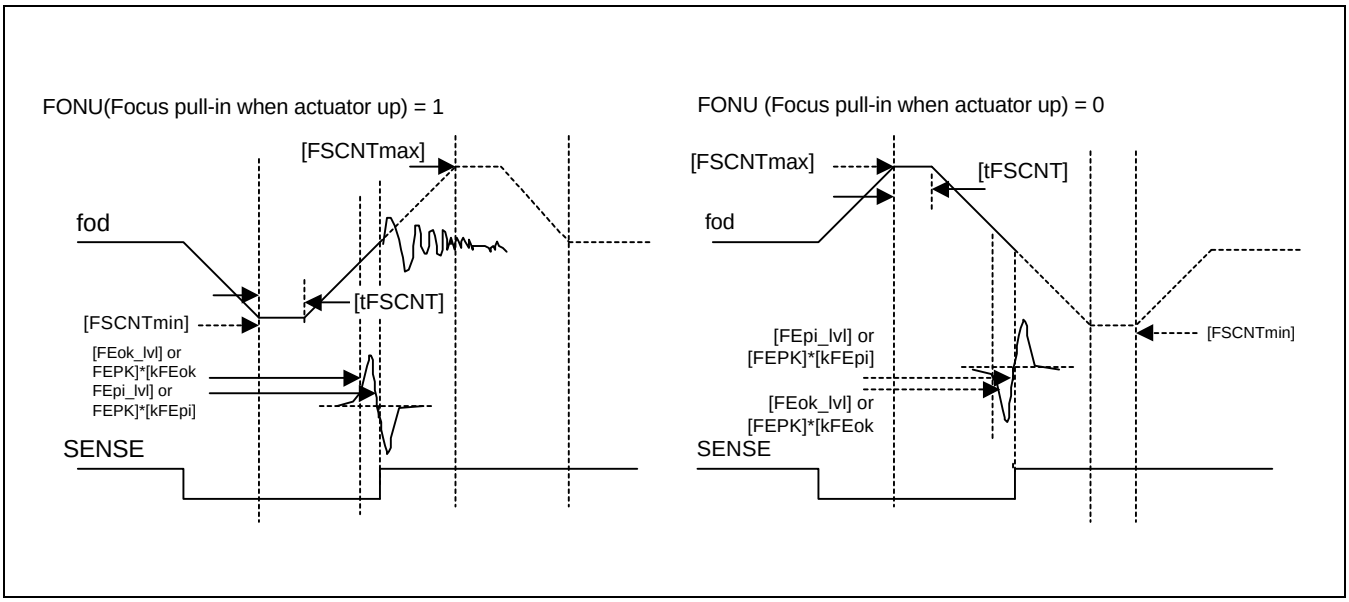
→ If FONcmd is received again during Play, Tracking/Sled is turned off.

Related Memory

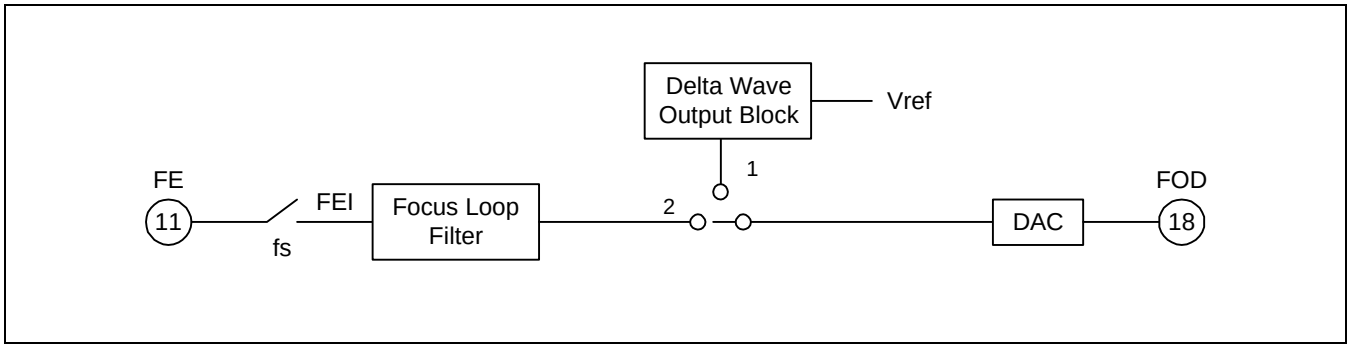
Name	Address	Function	Data	Value
FONbuf	001B	Focus ON command buffer		
FSSPD	0020	Focus Search speed		
FSDELTA	0021	Focus Search delta		
FSCNT	0022	Focus Search counter		
FSCNTmax	0028	Focus Search output max	0 × 1800	
FSCNTmin	0029	Focus Search output min	0 × E800	
tFSCNT	002D	search wait time	0 × 2000	
FEfs	002E	|FE| for focus pull-in		
FEok_lvl	002F	FE ok level for Focus search	0 × 1000	
FEpi_lvl	0030	FE pull-in level	0 × 0400	
FE	0062	Focus error		

Operation Description

When the Focus On command is input, Delta waves are output from FOD as shown in the figure below. When to execute (UP/DOWN) Pull-in is decided according to the FON at this time. Search Speed or the slope is decided by the FSSPD and FSDELTA value, and the upper and lower limit duration is determined by tFSCNT. Also, PIM decides whether to have the FE recognition, pull-in level at the absolute value or the FEPK percentage.



Focus Pull-in Block Diagram



TRACKING BALANCE

Summary

The purpose of this adjustment is for the average of the MAX and MIN values of each TE zero cross component's cycle, caused by eccentricity in the Off Track state, to be the same as Tofst. For CDs, TBAL signal is output and the E,F AMP gain within the RF AMP is modulated to repeat adjust the Balance.

Command

TBAcmd (0X0F00)
: The command averages the MAX and MIN values of TE when Focus is on and Tracking is off, by using eccentricity. It must always be executed before going into Play (Tracking on).

Code	1'st byte							
0F	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	PIM	0	0	TTBA

TIGAB: (D7 Reserved). Tracking input gain adjustment selection bit.
0 : Adjusted by MICOM.
1 : Tracking input gain changed by Servo according to TE level.

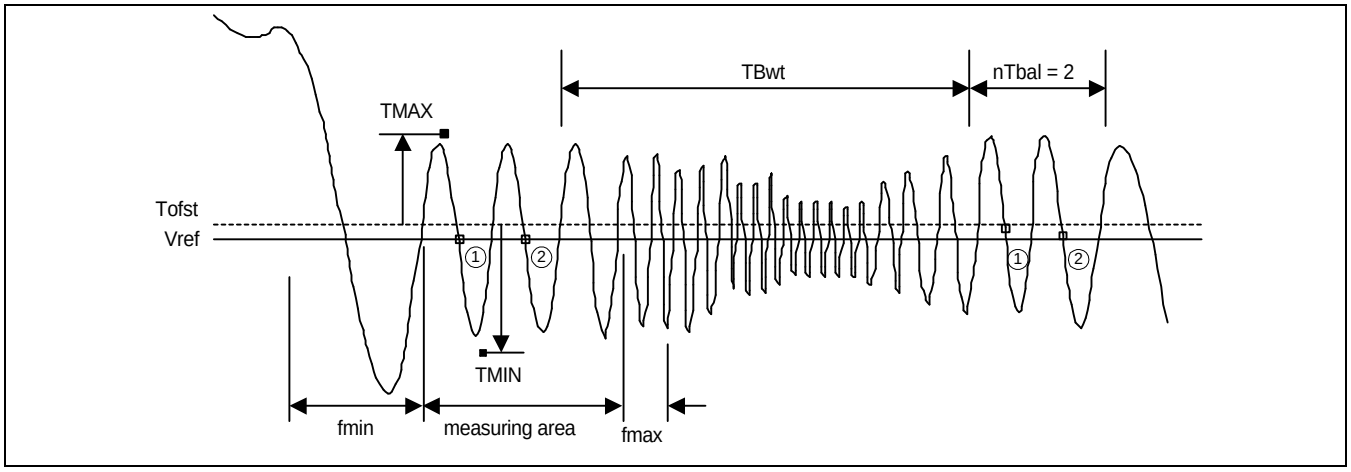
TTBA: Test mode for TBA
0 : Normal TBA
1 : Tracking Balance is changed once, then reverted to previous mode, regardless of Tracking Balance OK.

Related Memory

Name	Address	Function	Data	Value
TBALnoise	00C6	zero cross noise level	0400	
Tengh	00C7	TEpeak enough level	2000	
fmin	00CA	MINIMUM FREQUNCY for TZC detection	00F6	725Hz
fmax	00CB	MAXIMUM FREQUNCY for TZC detection	0020	5580Hz
TBok	00CC	T_BAL OK LEVEL (deviance allowed)	0100	19.5mV
tTBALmax	00CD	No zero cross max time	2000	
nTbal	00CE	Period of one measurement	0008	8 periods
TBwt	00CF	Wait time after TBAL change, until the beginning of the re-measurement	0200	5.734ms
TBk	FE6F	T_BAL adjustment sensitivity coefficient	9000	-0.875

Detailed Operation Description

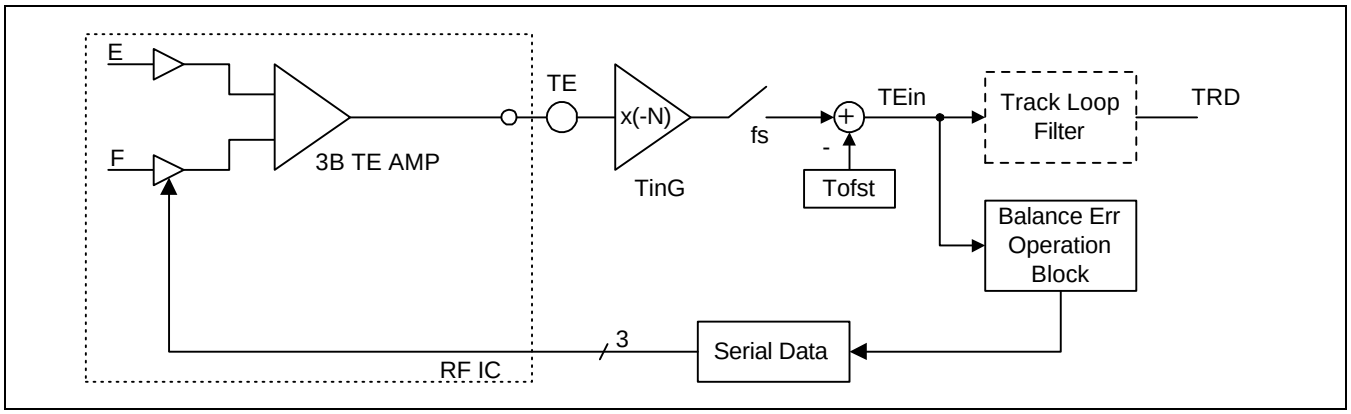
Out of the periods of TE(tzc) signals passing through Vref and satisfying the conditions of fmin and fmax, TEmin, TEmax, and the median of the two values is determined. When these periods have continued nTbal times, the difference between the median value and the average adjustment level (=Tofst) is found to be the balance error. If the error is smaller than TBok, the adjustment is terminated, and if larger, multiply TBk to Tbal's previous value for output.
So when the Tbal value has been output once, the Gain or Delay within the RF's TE AMP is varied, and the TE signal's balance error is varied as well. Because of this characteristic, you need a wait time (TBwt) longer than the settling time. When the system is stabilized, the above steps are repeated to get more balance error data.



Monitor Memory

Name	Addr.	Function
TEmax	00C9	TOP PEAK REG.
TEmin	00C8	BOTTOM PEAK REG.
WORK0	008B	Σ [TEmin+TEmax]/nTbal calculation results register
Tbal	00C5	Tbal output

Tracking Balance Block Diagram



FOCUS BIAS

Summary

The purpose of adjusting the Focus Bias is to insure optimum RF signal quality during PLAY. Although it is the Jitter amount that shows RF signal quality, it is very difficult to actually measure the jitter on the IC and create an algorithm to find the point of minimum jitter. The alternative is to adjust the Focus Bias so that the envelope size is at its maximum. The RF signal has the characteristic of having the least jitter near the point of Focus Bias when the RF envelope size is at its maximum.

- Input signal : FE, RFENV
- Output signal : FOD

Command

FBAcmd (0x11 00)
: When the RF signal is at its maximum, end Focus Balance Adjust using the RF Envelope signal.
Always use after Focus pull-in.

Code	1'st byte							
11	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	TFBA

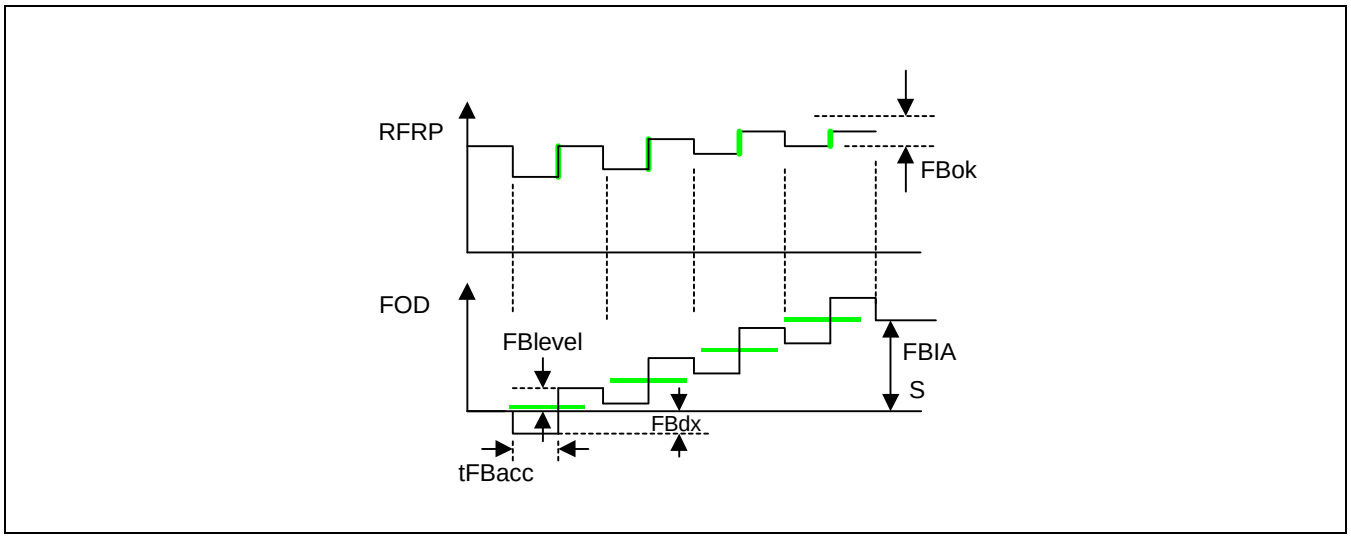
TFBA : Test mode for FBA.
0 : Normal FBA.
1 : Execute Focus Balance once then revert to previous mode, without regard to Focus Balance OK.

Related Memory

Name	Address	Function	Data	Value
tFBacc	00D0	Disturbance Width	05EA	8.58ms
FBdx	00D1	BIAS increase/decrease amount Buffer	0080	9.8mV
FBlevel	00D2	Disturbance Level	1000	312.5mV
FBok	00D3	Bias OK Level	0100	19.5mV
FBIAS	0097	fbias data save		

Detailed Operation Description

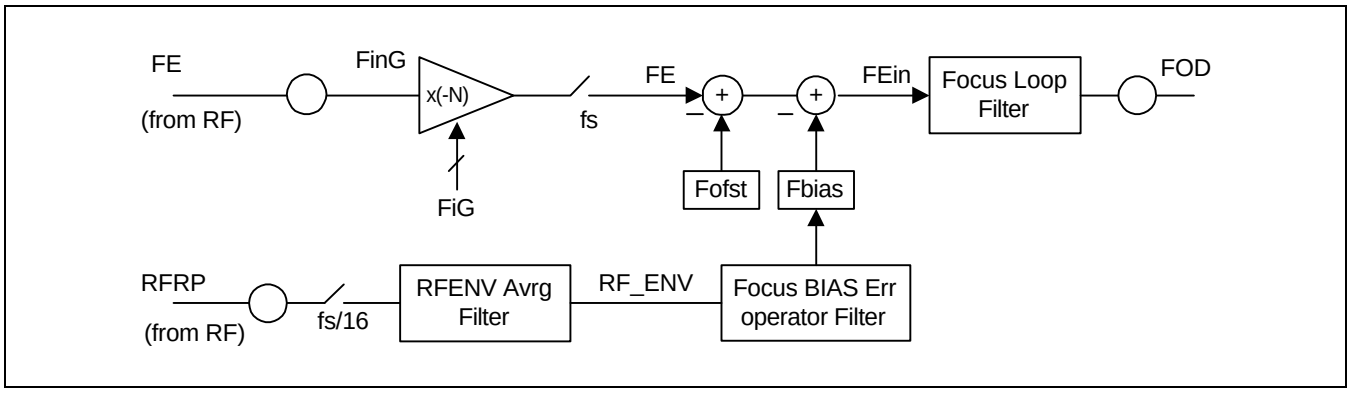
The difference between the RFENV must be minimized by adding DISTURBANCE to the FE signal. This DISTURBANCE uses FE as standard and sets a LEVEL for its use. The DISTURBANCE Level value is set to the initial - direction, RFenv(-) value is stored, and put on HOLD for the WIDTH. The value is then given to the + direction, the RFenv(+) value is stored, the difference between the two values is found, and checked to see if it is in the FBok Level. Depending on whether the difference is (+) or (-), the dxbuf amount is subtracted from the Fbias amount to make the final Fbias value.



Monitor Memory

Name	Address	Function
Work0	0089	Minus Rfrp Reg.
Work1	008a	Plus Rfrp Reg.
Work2	008b	Work1-Work0 Calculation results register

Focus Bias Block Diagram



TRACKING PULL-IN

Summary

Tracking Loop is turned On using TZC Frequency when the Tracking On Command(0X03) is received in Off Track status.

— Input signal : TE

— Output signal : TRD

Command

: Tracking Pull-in command.
If tracking is already on when this command is received, no further actions are taken.

Code	1'st byte							
03	D7	D6	D5	D4	D3	D2	D1	D0
	0	TON	SLDX	TFSB	TOLB1 — 0		0	KICK

TON : Track On/Off.
0 : Off.
1 : On.

SLDX : Sled Servo On/Off.
0 : SLED off.
1 : Sled servo on after a set time period since Tracking on.

TFSB : Eccentricity compensation pull-in control bit during Track pull-in.
0 : Normal pull-in.
1 : Eccentricity Compensation pull-in (between the edges of TZC are counted and pull-in is executed where the frequency is low).

TOLB1 - 0 : Lens Brake during Track Pull-in. T/F Gain control enable/disable.
Used when executing pull-in after a jump using the Stepping motor.
0X : OFF.
10 : ON (lens kick value used for lens brake time during Normal Pull-in).
11 : ON (Pull-in after Stepping motor feed kick).

KICK : KICKsignal control (for stepping motor sled move).
0 : Set KICKsignal to "L".
1 : Set KICKsignal to"H".

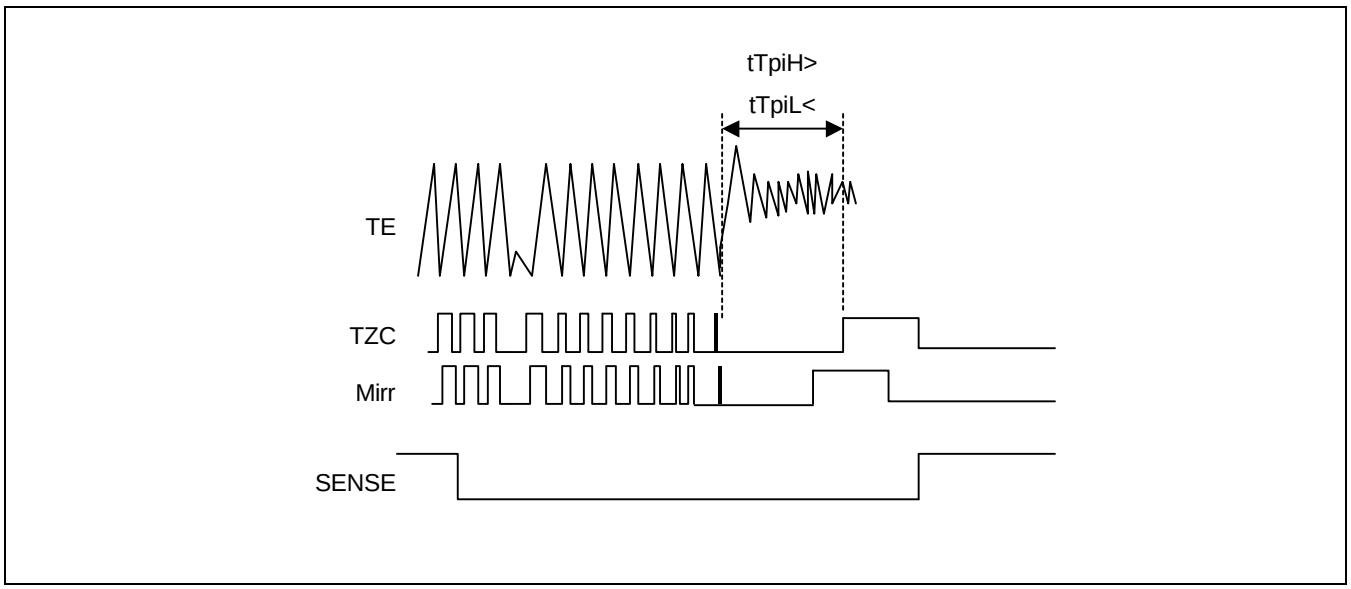
Related Memory

Name	Address	Function	Data	Value
tTpiH	004A	minimum TZC time when Tpi	0800	2048*0.1 us
tTpiL	004B	maximum TZC time when Tpi	2000	8192*0.1 us

Operation Description

1) TFSB = 0
When the Tracking On command is input, the MIRR and TZCsignal are checked. When a TZC edge is generated while the MIRR signal is "L", tracking is assumed to be on, and sense is output as "H".

2) TFSB = 1
When TZC period is less than tTpiH but larger than tTpiL, and a TZC edge is generated when MIRR signal is "L", tracking is assumed to be on, and sense is output as "H".



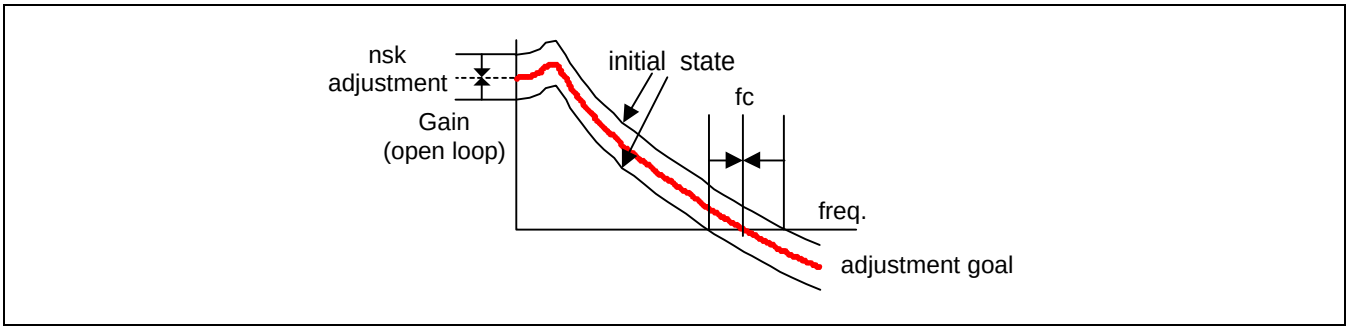
LOOP GAIN

Summary

The Loop Filter's Gain is automatically adjusted so that the Open Loop Bandwith for Focus/Tracking is at the specified frequency needed in the system.

— Input signal : FE, TE

— Output signal : FOD, TRD



Command

Focusing Gain Adjustment command (FGAcmd (0X0C00))
: This command adjusts the Auto Focus Gain. Use when the Focus servo is on, and the tracking servo is either on or off.

Code	1'st byte							
0C	D7	D6	D5	D4	D3	D2	D1	D0
	FGud	0	0	0	0	0	0	TFGA

FGud : Auto Focus Gain Update.
0 : No update.
1 : When changing Kfo, Kfuo after automatic adjustment, update according to the rate of change during the automatic adjustment.

TFGA : Test mode for FGA.
0 : Normal FGA.
1 : Change Focus Gain once then revert to previous mode, regardless of Focus Gain OK.

Tracking Gain Adjustment command (TGAcmd (0X0D00))
: This command adjusts the Auto Tracking Gain. Use when Focus servo and tracking servo are on.

Code	1'st byte							
0D	D7	D6	D5	D4	D3	D2	D1	D0
	TGud	0	0	0	0	0	0	TFGA

TGud : Auto Tracking Gain Update.
0 : No update.
1 : When changing Kto, Ktuo after automatic adjustment, update according to the rate of change during the automatic adjustment.

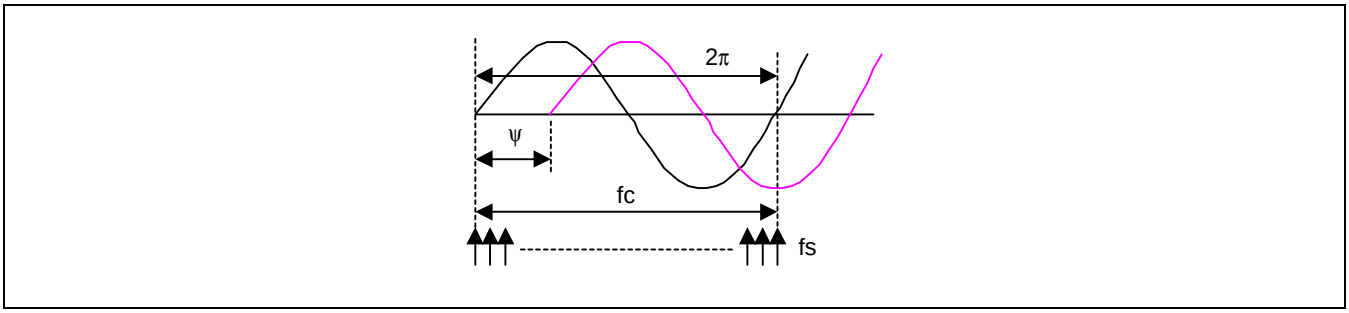
TTGA : Test mode for TGA.
0 : Normal TGA.
1 : Change tracking gain once then revert to previous mode, without regard to Tracking Gain OK.

Related Memory

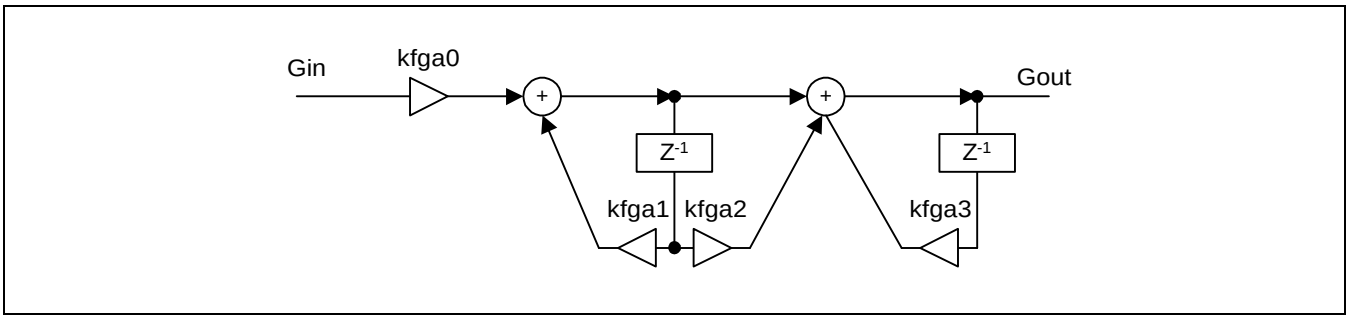
Name	Address	Function	Data	Value
Gin	0050	input for gain adjust		
GDF1	0051	BPF data for Gain adjust		
Gout	0052	BPF out		
Ydata	0053	Ydata=X+2Z		
zYdata	0054	Ydata(n-1)		
SINdata	0055	sin data		
sTsz	00E0	total sindata size		
sHsz	00E1	sTsz/2		
Xwave	00E2	current sin data pointer		
xGwait	00E3	Wait Time	0008	8 periods
xGcnt	00E4	measurement period	0010	16 periods
Xdisturb	00E5	disturb data		
Xphase	00E6	phase error		
Ffrq/Tfrq	00EC/00E9	Focusing/Tracking Bandwidth	0009/000C	1.8K/2.4K
FGok/TGok	00EA/00E7	Focusing/Tracking Gain Ok Level	0005/0005	0.38 §Æ
Kf/Kt	FE8C/FE84	Focusing/Tracking Disturbance Level	0500/0400	71.7/78.1mV
Kcf/Kct	FE8D/FE85	Focusing/Tracking adjustment sensitivity coefficient	E000/0800	-0.25/0.063
FGmax/TGmax	0058/0056	Focus/Track Gain Maximum Value	E000/1000	-0.25/0.125
FGmin/TGmin	0059/0057	Focus/Track Gain Minimum Value	F500/0400	-0.086/0.032

Detailed Operation Description

The adjustment consists of outputting a sine wave to the FOD output, comparing the original sine wave and the signal that has passed through MECHs such as P/U to make the phase difference into 90°. The LOOP EQ FILTER's final output gain is automatically adjusted. The adjustment is repeated many times to reach the optimum state. To eliminate NOISE components in the input signal, the signal goes through BPF handling.

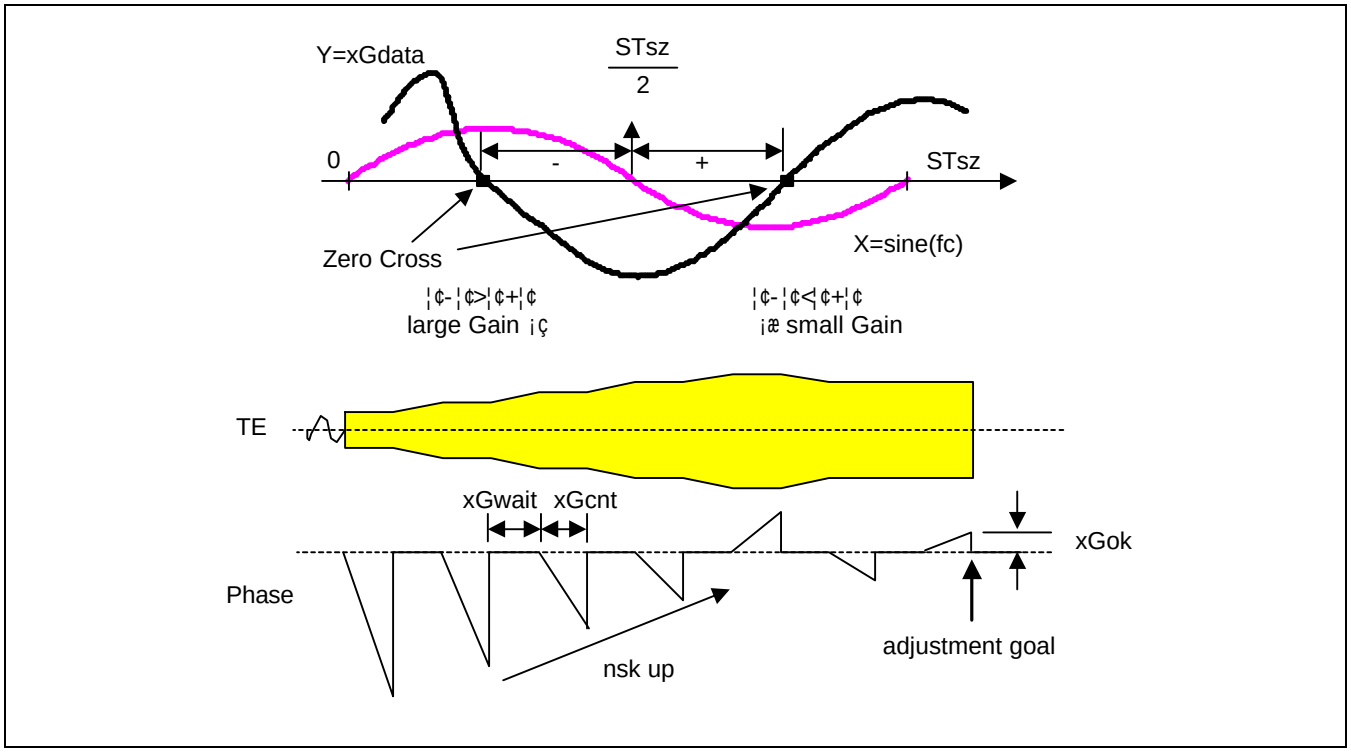


BPF Configuration and Filter Coefficient

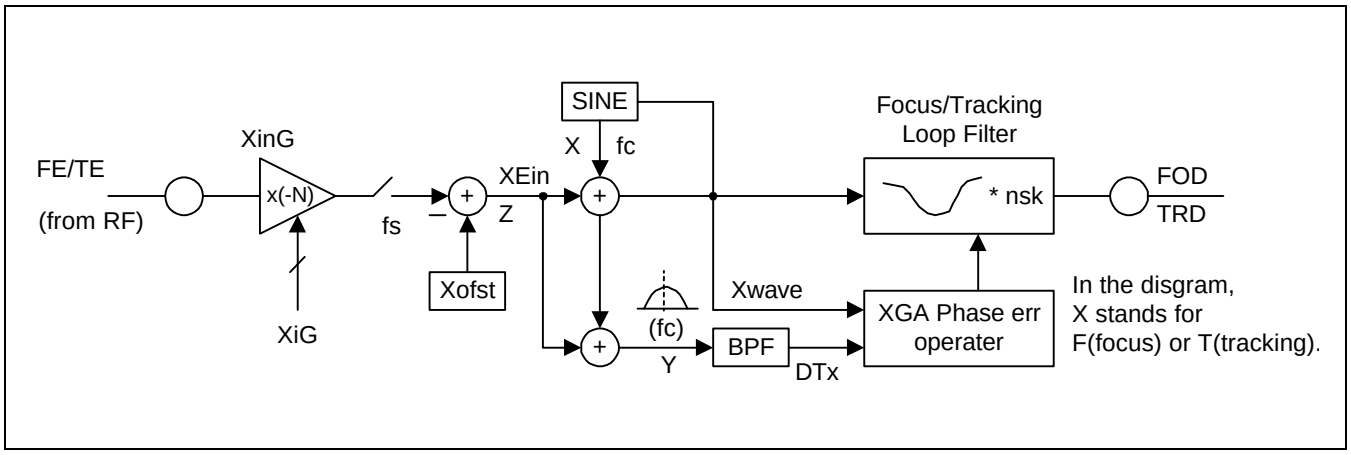


Name	Address	Function	Data
Kfga0/Ktga0	FF88/FF80	Coefficient for adjusting GAIN	0FAC/16A3
Kfga1/Ktga1	FF89/FF81	POLE FILTER 1 coefficient	7829/74AE
Kfga2/Ktga2	FF8A/FF82	ZERO FILTER coefficient	8000/8000
Kfga3/Ktga3	FF8B/FF83	POLE FILTER 2 coefficient	7829/74AE

Phase Difference Detection Waveform



Loop Gain Block Diagram



SAMSUNG ELECTRONICS

VELOCITY CONTROL TRACK JUMP

Summary

Velocity control Track jump uses the MIRR signal generated from the TRACK ERROR signal (TZC) read from the disc during jump and the RFRP signal to detect the P/U's velocity and direction. It uses the difference between the previously designated velocity profile and the actual velocity to output kick/brake to TRD, controlling track jump.

— Input signal : TE(TZC), MIRR

— Output signal : TRD, SLED0, SLED1, SENSE

Command (0x05XX)

TRack Jump command (TRJcmd)
: TRJcmd is a Track jump command that is used for track kick/brake jump and track velocity control jump.

Code	1'st byte							
05	D7	D6	D5	D4	D3	D2	D1	D0
	DIR	NUMS						

DIR : Direction you wish to move in using the Track Counter (TC).
0 : Outward movement.
1 : Inward movement.

NUMS : Number of upper tracks you want to move (0x00 - 0x7F).

→ Lower Jump track number is designated by CJNCcmd(0B).

Cd Jump Number Common command (CJNCcmd)
:This command designates the track number of TRJcmd and RPTcmd(Reserved), and the lower track number of SMVcmd, PSJcmd(Reserved), and STEPcmd(Reserved).

Code	2nd byte							
0B	D7	D6	D5	D4	D3	D2	D1	D0
	NUMS							

NUMS : The number of lower tracks you want to move (0x01 - 0xFF).

Jump MoDe1 select command (JMD1cmd)
: JMD1cmd is a Jump-related initial value selection command.

Code	1'st byte							
18	D7	D6	D5	D4	D3	D2	D1	D0
	JCKS1-0		0	0	0	0	0	0

— JCKS1-0 : H/W counter clock selection bit during Jump.
00 : MIRR
01 : TZC
1X : Latched MIRR (initial value).

Jump MoDe4 select command (JMD4cmd)
: JMD4cmd is a Jump-related initial value selection command.

Code	1'st byte							
1B	D15	D14	D13	D12	D11	D10	D9	D8
	RVSB	VCMP	VEDG		VPRDR		VCLKS	

RVSB : Reverse check control during Jump.
0 : If there is less tracks than RVSnum(0xbe) during reverse, jump stop.
1 : Do not execute Reverse check.

VCMP : 1 Counter compensation (when Cout is "H").
0 : Do not Compensate.
1 : Compensate.

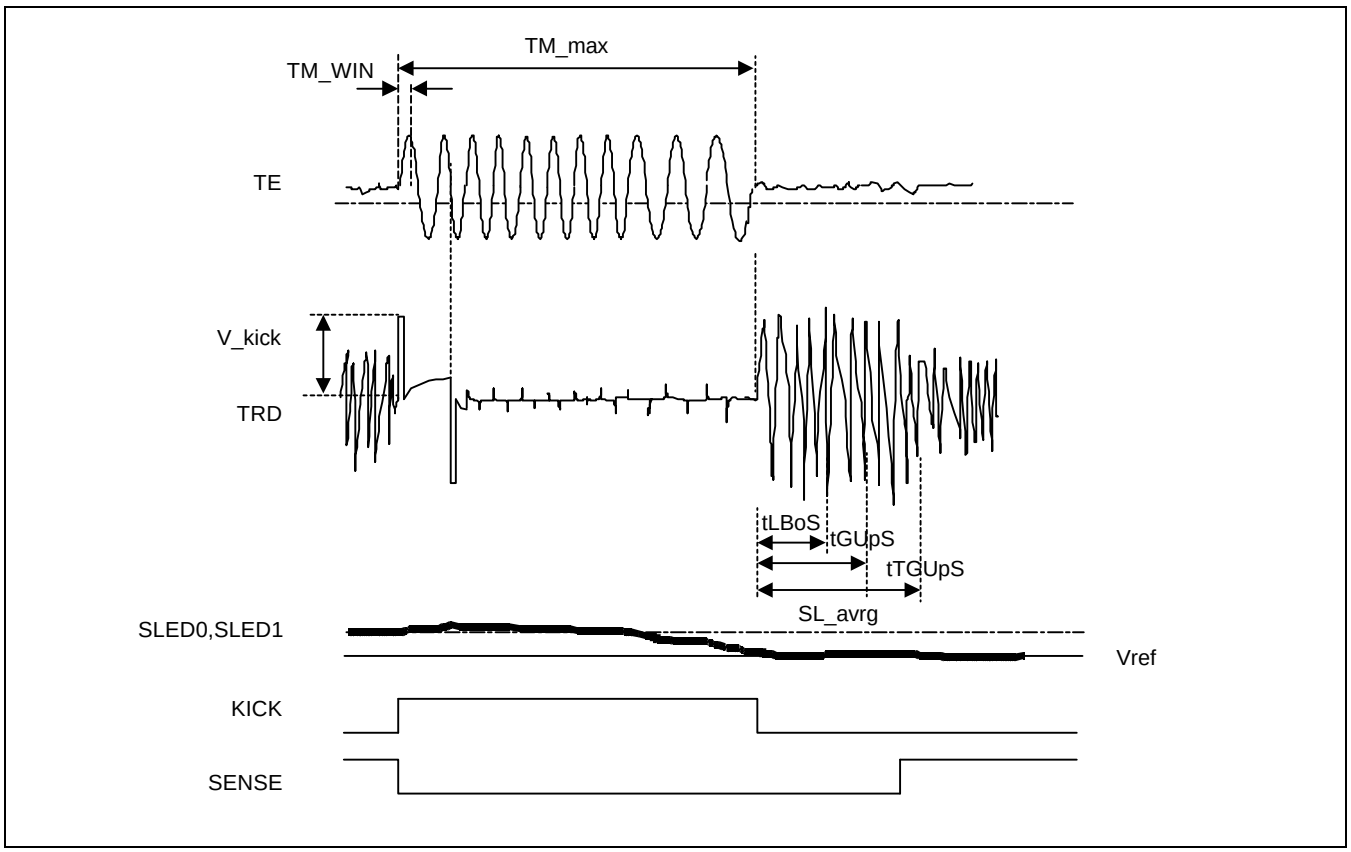
VEDG : Velocity jump period counter standard edge selection.
00 : Falling & Rising
01 : Falling
10 : Rising
11 : Falling & Rising

VPRDR : Velocity jump period standard signal (H/W counter and Kick/Brake standard clk changes together as well).
00 : TZC
01 : MIRR
10 : L_TZC (L_MIRR is selected for H/W counter and Kick/Brake standard clk).
11 : L_MIRR

VCLKS : Velocity Clock Select
00 : CK32 (1.25MHz = 800ns)
01 : CK16(2.5MHz = 400ns)
10 : CK08(5MHz = 200ns)
11 : CK04(10MHz = 100ns)

Related Memory

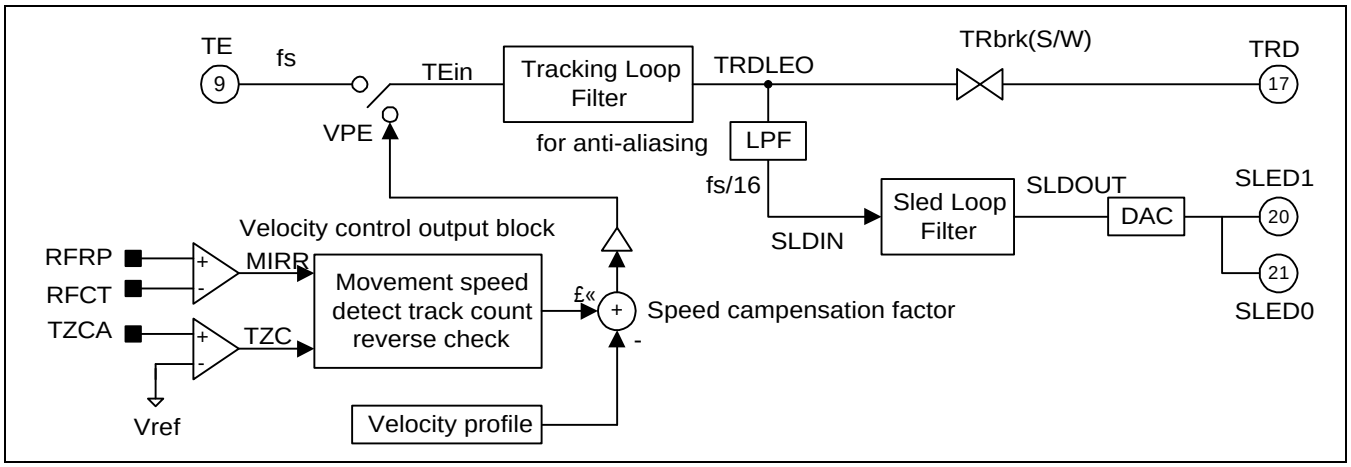
Name	Address	Function	Data	Value
tBRK1	00B0	brake time for 1 track jump	18	
tBRK	00B1	brake time for upper 1 track jump	C	
Tstbl	00B2	stable time after jump	0	
Twin	00B3	Track Jump TZC blind Time	0x10	90µs
NUMS	00B4	jump track number		
Vkick	00B5	initial kick level for velocity jump	-	
Rtrk	00B6	residual track number([vNUMS]-H/W counter-Vcmp)		
Vtmp	00B7	center calculation value memory		
Vctl	00B8	accumulation value of difference between current and profile velocity		
King	00B9	Velocity error		
VTKp	00BA	plus kick for velocity control jump	2000	
VTKm	00BB	minus kick for velocity control jump	E000	
TMedge	00BC	edge counter		
KICKedge	00BD	velocity control start edge	2	
RVSnum	00BE	Reverse jump check minimum track number		
Jnum	00BF	Number of tracks jumped (for stepping motor sled move)		
tJnoise	00C0	te zero cross noise cancel		
JMPCMDbuf	004C	Jump command save buffer		
JMPDATAbuf	004D	Jump data save buffer		
Jcomp	00F3	compensation for jump		
tLBoS	00DA	lens brake time	500	
tGUpS	00DB	F gain up time	300	
tTGUpS	00DC	T gain up time	3A9	



— BPROf0 - e : velocity profile

— REVCF0 - e : velocity profile error compensation factor
The error compensation factor is different according to the velocity.
(5kHz : You must multiply the error compensation factor that is appropriate for 10kHz.
→ If the error compensation factor of 5kHz is 0.5, the error compensation value of 10kHz is considered to be 1.)

Velocity Control Related Block Diagram



Operation Description

Jump-related values are adjusted before executing velocity jump. For example, the window time ([TM_WIN]) is selected in order to eliminate errors caused by MiRR or TZC noise early in the jump. Also, values such as lens brake time ([tLBOS]), focus gain up time ([tTGUS]), and tracking gain up time ([tTGUDS]) are selected after the jump. If needed, the initial kick values ([VKP],[VKM]) must be set as well.

Values such as clock and kick/brake period, which are used as standards during jump, are first set by 1Bcmd. The number of tracks you want to jump are input through the velocity jump command (0x5, 0x0B).

Also, the velocity profile that fits the clock is input into BProf0 - BProfe before the jump. The default value is the velocity profile data that executes kick/brake for each period.

When initialization is over, the jump is executed. The value that is output as trd is the result from the velocity profile [Prof0¡-e] and the L_MIRR positive edge's counter value difference signal that has been sent through the loop filter.

Name	Address	Function	Data	Value
RVECF0 RVECFe	FEC0 - FECE	Error's comparative velocity compensation value	4000,4000,4000,4000,4000,5000,6000,7FFF	
BProf0 - BProfe	FED0 - FEDE	Basic velocity profile data	00FA,00FA,00FA,00FA, 00FA,00D2,009A,0070	* One period of VCLKS
Prof0 - Profe	1E0 - 1EE	Velocity profile data used in the actual jump (variable according to command)		
kVHL	FECF	Last brake Level in upper 1 track jump	2000	3.125 V
IVBL1	FEDF	Initial Velocity Brake Level in 1 track		
IVBL	FEEF	Initial Velocity Brake Level in upper 1 track		
Jperiod	172	Jump period for RPTcmd		
kVf	FEF3	% for velocity controlled track jump	4000	50%

VELOCITY CONTROL FEED MOVE

Summary

Velocity control feed move detects moving speed and direction of P/U by using the TRACK ERROR signal (TZC) read from the disc and the MIRR signal generated from the RFRP signal (deferent of RF signal′s peak to peak level). It executes track jump use by the difference between the previously designated velocity profile and the actual velocity to output kick/brake to TRD.

— Input signal : TE(TZC), MIRR

— Output signal : TRD, SLED0, SLED1, SENSE

Command : transmit 3 command

JMD2cmd (0x19hh) : Set jump-related mode

Code	1'st byte							
19	D7	D6	D5	D4	D3	D2	D1	D0
	LFKS	FKMOD	FSEQ	FNEQ	HYS	TGS	FDC	-

LFKS: Lens kick / Feed move select bit.
0: Lens kick.
1: Feed move.

FKMOD: When LFKS is 'H', feed move type select.
0: Speed feedback type feed move.
1: Open control type feed move.

FSEQ: Usage feed search EQ in feed move.
0: Do not use
1: Use feed search EQ

FNEQ: Usage feed normal EQ in feed move.
0: Do not use
1: Use feed normal EQ

HYS: Usage hysterisis in the end of search.
0: Do not use
1: Use hysterisis

TGS: Usage tracking gain up in the end of search .
0: Do not use
1: Use tracking gain up

FDC: Add initial kick value(offset) to feed output in feed move .
0: Do not add
1: Add

VCFcmd (0x06hh): Select Velocity control feedkick jump direction and upper track number.

Code	1st byte							
06	D7	D6	D5	D4	D3	D2	D1	D0
	B/F	Upper byte of jump track						

B/F: Select move direction in kick.
0: Backward
1: Forward

CJNCcmd (0x0Bhh): Set jump-related mode.

Code	1st byte							
0B	D7	D6	D5	D4	D3	D2	D1	D0
	Lower byte of jump track							

NUMS : The range of tracks number you want to move is $1\text{-}2^{15}$(32767).

JMD3cmd (0x1Ahh): Select lower track number

Code	1'st byte							
1A	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	HCRE	HCRC		HCRS

HCRE: Hardware counter reference edge.
0: Raising
1: Falling

HCRC: Hardware counter reference clock.
00: CK32(1.25MHz = 800ns)
01: CK16(2.5MHz = 400ns)
10: CK08(5MHz = 200ns)
11: CK04(10MHz = 100ns)

HCRS: Hardware counter reference signal.
0: TZC.
1: Mirr.

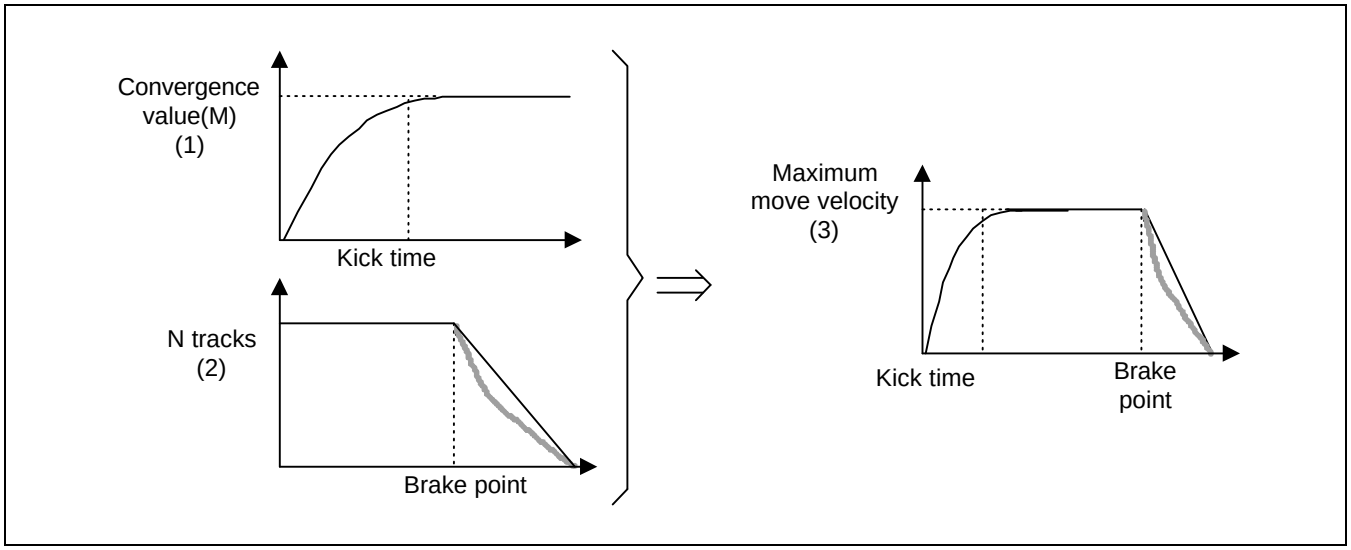
Related Memory

Name	Address	Function	Data	Value
FLAGbuf	0014	Flag mode(use only lower 4 bits)		
FLABsav	0015	Save FLAGbuf		
FLAGextral	0016			
Cstrd	008D	Current strd store		
Zstrd	008E	Previous strd store		
JUMCMDbuf	0035	Save jump command		
JUMDATbuf	0036	Save jump track number		
JMD23buf	001D	Save JMP2, JMP3 command(JMP2: upper, JMD3: lowder		
FKWt	0100	Kick initail window time	0x10	
FKPt	0101	Kick calculation period time	0xF	
FVGI	0102			
FVGO	0103			
Ctmp	0104			
MAXV	0105			
Vgab	0106			
Vgen	0107			
FINP	0108			
Fgab	0109			
Pre_cnt	010A			
R_trk	010B			
Cspd	010C	Jump track number		
FEQ1	010D			
FEQ2	010E			
FEQ3	010F			
FEQ4	0110			
FEQ5	0111			
Fkpok	0112			

Name	Address	Function	Data	Value
Kv10	FF00	Velocity generator filter coefficient	00A0	
Kv11	FF01		7B90	
Kv12	FF02		07D0	
Kv13	FF03		0000	
Kt1a	FF04			
Kv20	FF05	Feedback search EQ	0570	
Kv21	FF06	Save jump track number	7F90	
Kv22	FF07	Save JMP2, JMP3 command(JMP2: upper, JMD3: lower	0250	
Kv23	FF08	Kick initail window time	7FA0	
Kv24	FF09	Kick calculation period time	B370	
Kv25	FF0A		4EB0	
Maxspd	FF0B	200KHz	0147	
Prdspd	FF0C	11KHz	0012	
Ttov	FF0D			
Ht_tov	FF0E	3-HCRC		
Bpset	FF0F	4096 track	1000	
INV_BP	FF10	1/4096 shift	0003	
Mgraph	FF11			
Minspd	FF12	5KHz	8	
Kvg1	FF20		6000	
Kvg2	FF21	Jump track number	5800	
Kvg3	FF22		5000	
Kvg4	FF23		4800	
Kvg5	FF24		4000	
Kvg6	FF25		3800	
Kvg7	FF26		3000	
Kvg8	FF27		2800	
Kvg9	FF28		2000	
Flim	FF30	Fc value decision constant	0050	
Kv2a	FF31		E000	
BC_val	FF32	10MHz(100nS)	4000	

Velocity Profile

Velocity profile can decide kick time, maximum move velocity, break point.



— Kick Time
In graph(1), convergence track number is decide according to jump track, the time arrived around M is kick time.
This is decided by LFS's fc

— Maximum Move Velocity
Maximum Move velocity is decided by relation of convergence value(M) in graph(1) and N track in graph(2)

— Break Point
Break point is decided by mixing of graph(1) and graph(2). Break point is the time changed the sign in comparison
between value of graph(1) and value of graph(2).

Relation Of Track Number And Velocity

When maximum move velocity is Max, processing period is P, convergence value in graph(1) is M,

— Maximum move velocity is Max

— Maximum track number in processing P is Max/P

— When convergence value is N, maximum move velocity is (M*Max)/N, maximum track number is (M*Max)/(N*P)

— Change of convergence value per 1 track is P*M/Max

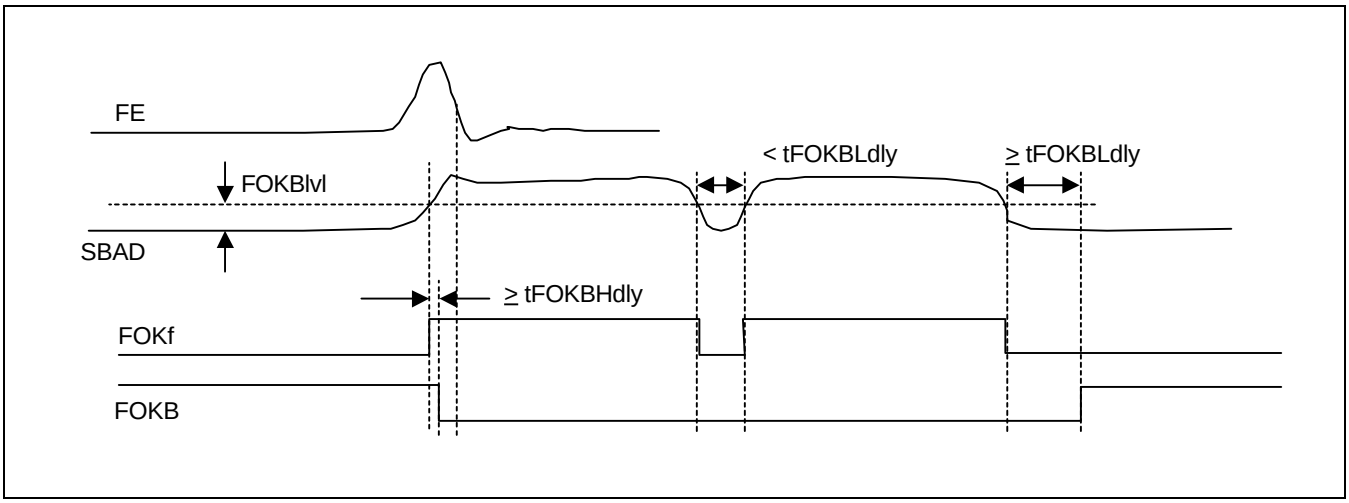
FOKB GENERATION

Summary

The FOCUS OK signal is generated from the E+Fsignal (SBAD) input from the RF IC.

— Input signal : SBAD

— Output signal : FOKB



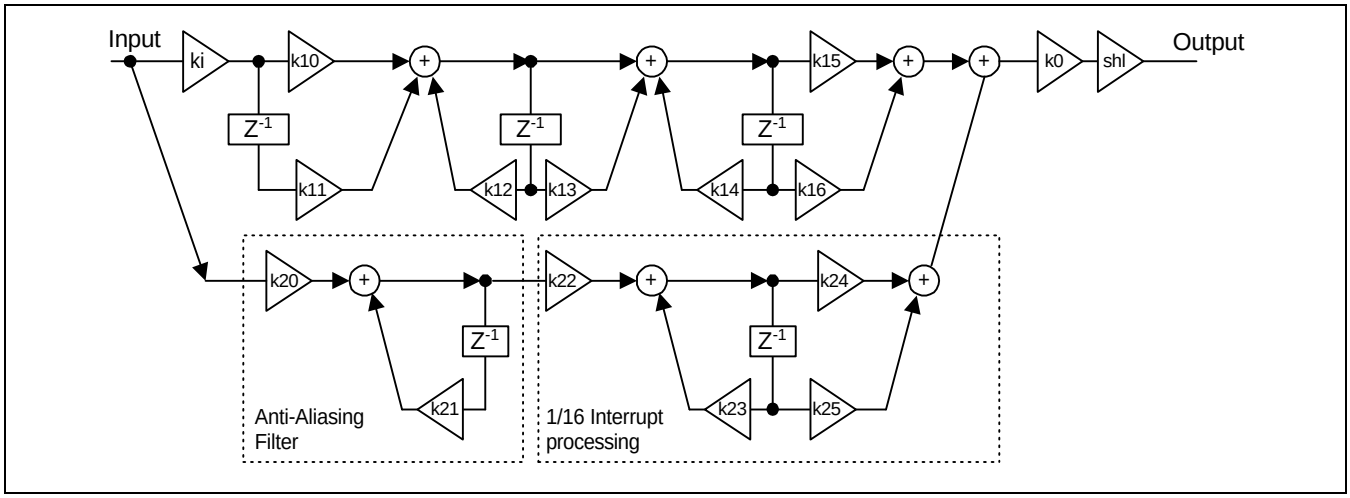
Command

The operation is handled in units of fs/16 without a separate execution command.

Related Registers

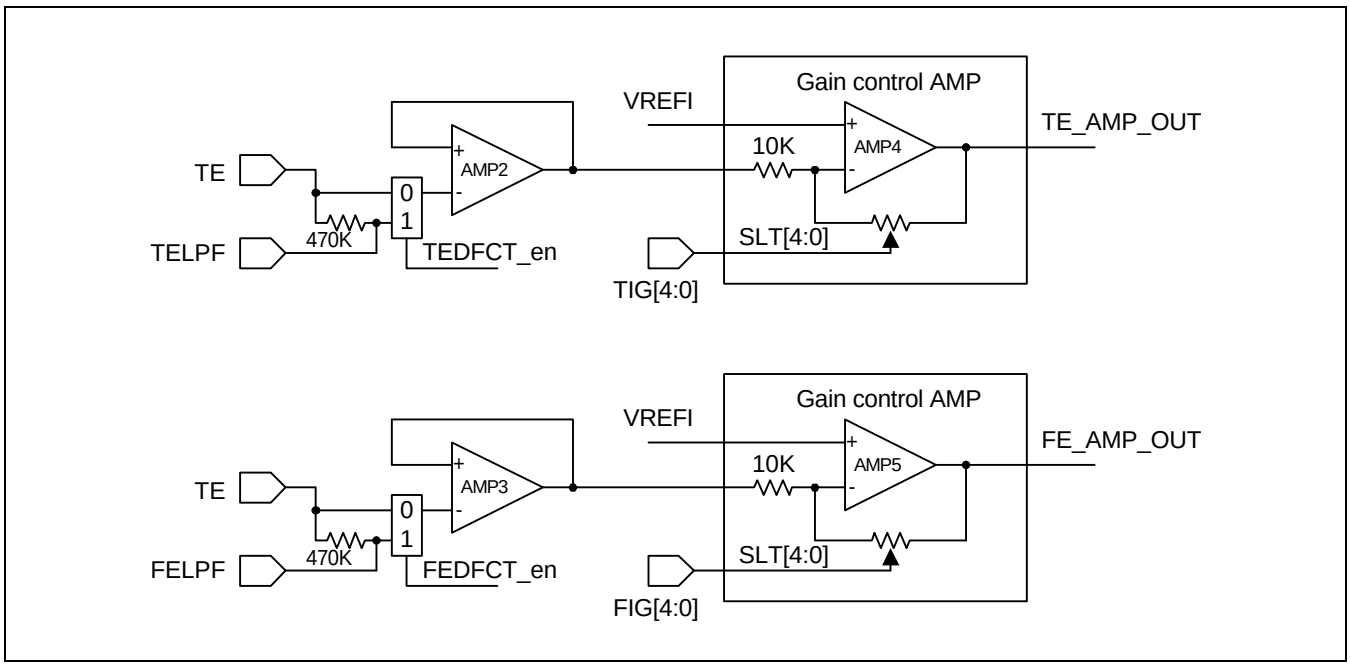
Register	Address	Function
FOKBlvl	0098	SBAD's FOCUS ON/OFF deciding LEVEL -> changes FOKf
tFOKBHdly	009A	FOK High Delay Time
tFOKBLdly	009B	FOK Low Delay Time

Focus/Tracking Loop Filter Configuration

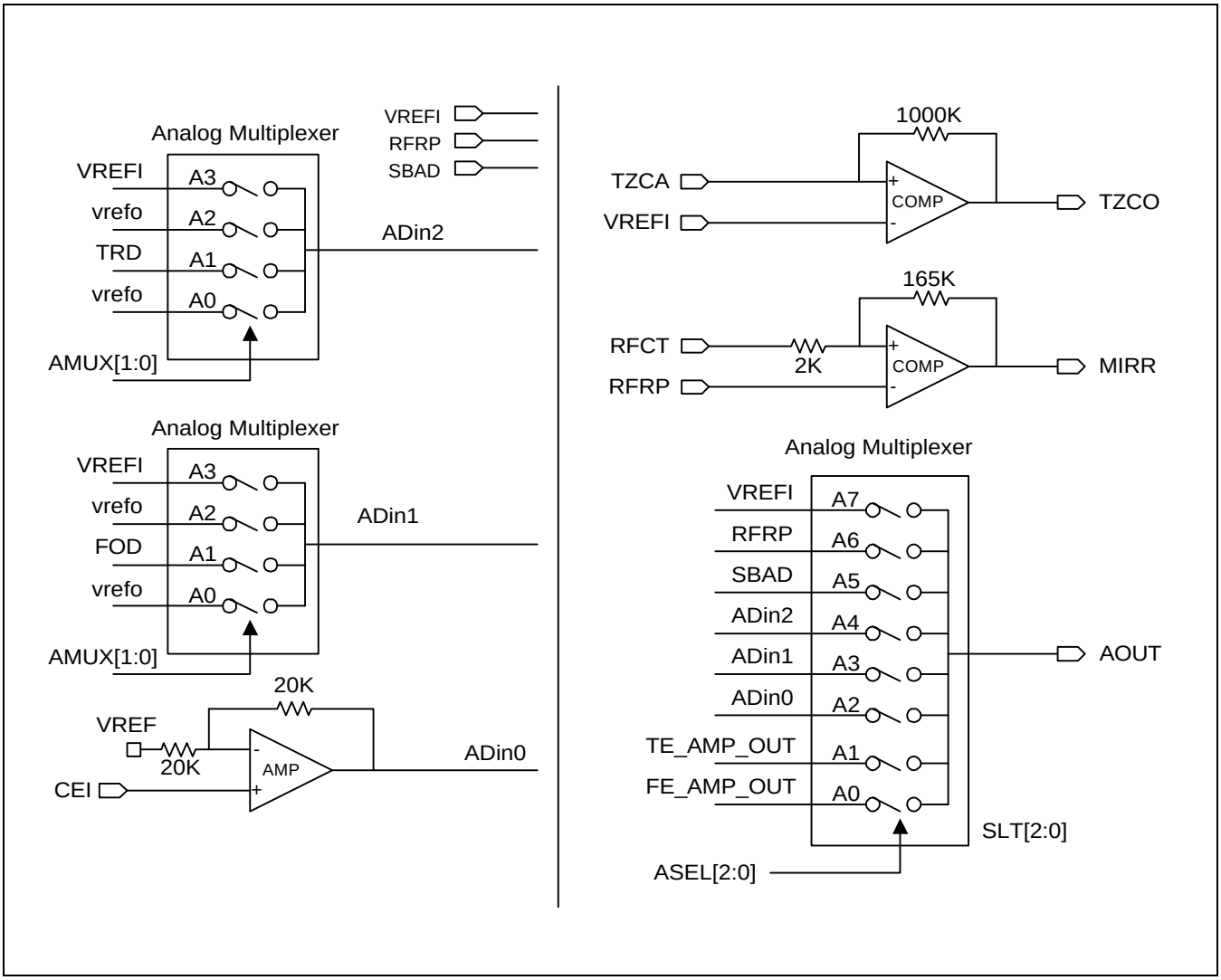


Coeff / Input	Ki	K10	K11	K12	K13	K14	K15	K16	K20	K21	K22	K23	K24	K25	Ko	shl
FE	Kfi	Kf10	Kf11	Kf12	Kf13	Kf14	Kf15	Kf16	Kf20	Kf21	Kf22	Kf23	Kf24	Kf25	Kfo	Kfshl
TE	Kti	Kt10	Kt11	Kt12	Kt13	Kt14	Kt15	Kt16	Kt20	Kt21	Kt22	Kt23	Kt24	Kt25	Kto	Ktshl

Analog Block



Analog Block



CD-DSP

Characteristics

— Wide capture range Analog PLL.

— Data Slicer that uses Duty Feedback method.

— EFM demodulation.

— Sync detection, protection, insertion.

— CLV, CAV DISC Spindle Motor control.

— C1/C2 ECC

— Built-in 16 K SRAM for ECC.

— Subcode P to W processing feature.

— CD-DA Audio processing feature.

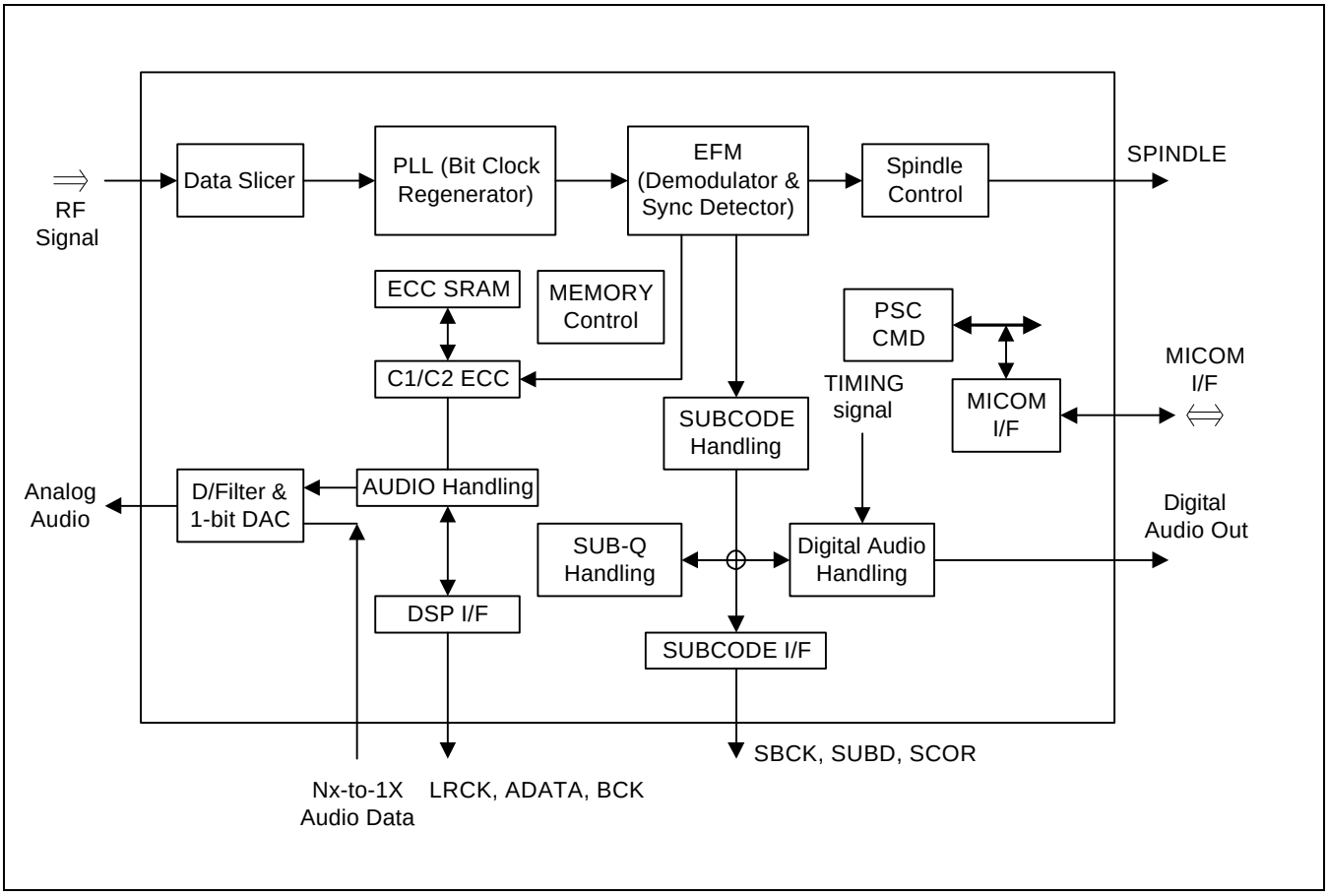
— SUB-Q De-interleaving & CRC Check

— 4X or 8X CD-DA DATA transmission support to CD-ROM Decoder Block for Audio Buffering (subcode sync and CD-DA DATA's synchronous output).

— Subcode Buffering.

— Subcode Sync. Insertion, Protection

Block Diagram



Register Map

1) Write Register

NAME	Addr.	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
INTCTL	40h	SBQIEN	REVIEN	ROVIEN	JITIEN	-	-	-	-
SYSCONT	41h	CLKSEL	-	MUTE	CDROM	-	S16T24B	ZCMT	-
SYSINIT	42h	-	MRESET	-	-	-	-	-	RAMCLR
MONCON	43h	SLORL[1:0]		EFMORP[1:0]		-	-	EFML_EN	PLCK_EN
HDDLYCTL	44h	VHD_DLY[3:0]				EHD_DLY[3:0]			
EQVSET	45h	-	EQV_SET[6:0]						
JITCTL	46h	PHOLD_EX	DLY_SEL[1:0]		KICKEN	AUDRST_EN	MPVCO	MPEQ	-
SERCTL	47h	-	EMSEL	-	EQ_SPD[3:0]				CLK_SV
AUDCTL	48h	DEEM_EN	SCSELP	SCSEL	PLCK_WINS	SUBDENSEL	SYNCSEL	-	AUDRST
ECCCTRL0	49h	ERAMOD	C1FLG	C2FLG	-	-	-	OFC2	C2ECC
ECCCTRL1	4Ah	JUMPEN	MRESYNEN	JITTEREN	C2PSEL	C2-FGTYPE[3:0]			
DFCTCTL	4Bh	DSHD	EQHD	SLON	-	-			
SBSY	4C	SS0WSEL	SS1WSEL	SS0WNDRST	SS1WNDRST	SS0ISEL[1:0]		SS1ISEL[1:0]	
DAOSUB	4D	M2DSUBCODE[7:0]							
PLLCTRL0	51h		PLOCKSET[1:0]		-	-	-	UPDN[1:0]	
PLLCTRL1	52h	TMX1	TMX0	PDHD	SLPD1	SLPD0	-	TALGC	-
PLLCTRL2	53h	iDACp[5:0]						VCOFIX	VCOHD
PLLCTRL3	54h	iDACn[5:0]						-	SLEFM
PLLCTRL4	55h	FDGAIN[7:0]							
PLLCTRL5	56h	PWM[7:0]							
SLICTRL0	57h	-	SLFIX[6:0]						
SLICTRL1	58h	LPFS	RES[2:0]			SLEN	INLG[2:0]		
SLICTRL2	59h	TSLCS	EQFIX	PKEN	PKCTL	DFRL[2:0]			-
EFMCTRL1	5Ah	SUBCON	SBFLUSHEN	SSEL	-	WSEL1	WSEL0	GSEL[1:0]	
EFMCTRL2	5Bh	-	CK33MSEL	-	-	-	-	GFSDET	WNDRST
MTRCTRL	5Ch	LJUMP	LOCKEX	MON_EX	DCTL	SPD[3:0]			
FCSEL	5Dh	FPLUS	ULHD	FAGD	RCAV	FNCW[1:0]		FCW[1:0]	

NAME	Addr.	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PCSEL	5Eh	FGSEL[1:0]		FGWDT	MOTSEL	PCEN	PCR	PCW[1:0]	
PCOFFS	5Fh	POFFS[7:0]							
EMOSEL	60h	CLVHD	SMON1	SMON0	SPOLAR	KICK	BRAKE	PWMCA[1:0]	
CAVSEL1	61h	CAVCK2	CAVCK1	CAVCK0	-	-	-	CAVR[9:8]	
CAVSEL2	62h	CAVR[7:0]							
DAOCTRL	63h	DAOEN	-	-	MEMPHIN	MDAOUIN	COPYEN	EMPHEN	ACMODE
CAVCTRL1	64h	ROTSEL	ROVS[2:0]			RIS[1:0]		FAL[1:0]	
DACCTRL	66h	DN	SDACCK	PWRSAVE	-	-	MUTEL	PDL	DEEM
DATTN	67h	-	-	ATTL[5:0]					

2) Read Register

NAME	Addr.	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
INTSTAT	70h	SUQINT	REVINT	ROVINT	JITINT	-	-	-	-
FRAME	71h	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8
COUNTER	72h	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
	73h	CTL3	CTL2	CTL1	CTL0	ADR3	ADR2	ADR1	ADR0
	74h	TNO7	TNO6	TNO5	TNO4	TNO3	TNO2	TNO1	TNO0
	75h	INDEX7	INDEX6	INDEX5	INDEX4	INDEX3	INDEX2	INDEX1	INDEX0
SUBQ	76h	MIN7	MIN6	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
DATA	77h	SEC7	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
	78h	FRM7	FRM6	FRM5	FRM4	FRM3	FRM2	FRM1	FRM0
	79h	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO
	7Ah	AMIN7	AMIN6	AMIN5	AMIN4	AMIN3	AMIN2	AMIN1	AMIN0
	7Bh	ASEC7	ASEC6	ASEC5	ASEC4	ASEC3	ASEC2	ASEC1	ASEC0
	7Ch	AFRM7	AFRM6	AFRM5	AFRM4	AFRM3	AFRM2	AFRM1	AFRM0
C1EBYTE	7Dh	C1EBYTE8	C1EBYTE7	C1EBYTE6	C1EBYTE5	C1EBYTE4	C1EBYTE3	C1EBYTE2	C1EBYTE1
C1ECODE	7Eh	C1EBYTE0	C1ECODE6	C1ECODE5	C1ECODE4	C1ECODE3	C1ECODE2	C1ECODE1	C1ECODE0
DPSTAT	7Fh	SBQERR	-	-	-	-	-	-	-
C2EBYTE	80h	C2EBYTE8	C2EBYTE7	C2EBYTE6	C2EBYTE5	C2EBYTE4	C2EBYTE3	C2EBYTE2	C2EBYTE1
C2ECODE	81h	C2EBYTE0	C2ECODE6	C2ECODE5	C2ECODE4	C2ECODE3	C2ECODE2	C2ECODE1	C2ECODE0
RBC	82h	-	-	-	-	RBC11	RBC10	RBC9	RBC8
RBC	83h	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
WBC	84h	-	-	-	-	WBC11	WBC10	WBC9	WBC8
WBC	85h	WBC7	WBC6	WBC5	WBC4	WBC3	WBC2	WBC1	WBC0

I/O DEFINITION

CLV-related signal (MOTOR I/F)

Symbol	I/O	Description	
SPINDLE	O	AFC/APC output, PWM (H, L, Hi-z)	

PLL-related signal

Symbol	I/O	Description	comment for one-chip
VCTRL	I	VCO Control Voltage	
RVCO	B	VCO V/I Converting Resistor	
RDAC	B	Biasing Resistor for iDAC at Charge Pump	
VALGC	I	ALGC PWM LPF OUTPUT	
RISS	O	VCO BIAS Resistance	
PWMO	O	ALGC Carrier Frequency controlling output	
PWMI	I	ALGC Carrier Frequency controlling input	

Slicer & EQ-related signal

Symbol	I/O	Description	comment for one-chip
RFI	I	Eye Pattern from RF	
EFMCOMP	O	Duty Feedback Slicer output	
EFMSL	O	Duty Feedback Slicer, slicer output	
LPF0	I	LPF input (CD 1X, 4X, 8X,16X)	
LPF1	I	LPF input (CD X24, 24X,32X, 40X, 48X)	
EQCTL	O	EQ output current	

EFM Demodulation-related signal

Symbol	I/O	Description	comment for one-chip
GFS	O	"H" when detected Frame Sync and inserted Frame Sync coincide	

Subcode I/F-related signal

Symbol	I/O	Description	comment for one-chip
EXCK	I	Subcode Data Readout Clock	
SBSO	O	Subcode P to W serial output	
WFCKO	O	Delayed WFCK (Write Frame Clock)	
SCORO	O	When either S0 or S1 is detected, SCORO is high	

1-Bit DAC and Audio Handling-related signal

Symbol	I/O	Description	comment for one-chip
LRCKI	I	Sample Rate Clock Input	From interpolation or ATAPI controller (or external input PAD)
BCKI	I	Bit Clock Input	
SDATAI	I	Serial Digital Input Data	
Vref	I/O	Reference Voltage Output for Bypass	PAD
AoutR	O	Analog Output for R-CH	PAD
AoutL	O	Analog Output for L-CH	PAD
VSSA	G	Analog Ground	Analog Power PAD for post analog-filter
VDDA	P	Analog Power Supply	
C2PO	O	C2 error pointer	for external interface output PAD
LRCKO	O	Sample Rate Clock Output	
BCKO	O	Bit Clock Output	
SDATAO	O	Serial Digital Output Data	

General MICOM Register

1) Write Register

40h	B7	B6	B5	B4	B3	B2	B1	B0
INCTL	SBQIEN	REVIEN	ROVIEN	JITIEN	-	-	-	-
Reset value	0	0	0	0	-	-	-	-

The INCTL Register controls the Data Processor Part's Interrupt generation. In other words, it has the ability to control the SINTB (PIN56)'s Interrupt output signal regardless of whether an Interrupt has been generated within the chip. If you enable this register's bits, the appropriate interrupts are output through Pin 56. If you disable the bits, the output of the interrupt signal is prevented. The interrupt that is received and handled from Firmware is the SUB-Q Interrupt controlled by SBQIEN (Bit 7). Firmware is aware of the chip's current condition by reading SUB-Q DATA 10 Bytes (73h - 7Ch).

Bit7 - SBQIEN : CD Subcode-sync Interrupt Request Enable
Enable/Disable bit of the Subcode-sync Interrupt generated every 98 frames at the CD DASP (13.3 ms at 1x).
1 : Enable 0 : Disable

Bit6 - REVIEN : Enable/Disable bit of the REVINT Interrupt generated at each disc rotation during reverse motion.
1 : Enable 0 : Disable

Bit5 - ROVIEN : Enable/Disable bit of the ROVINT Interrupt generated at each disc rotation when the motor's rotation speed exceeds that designated by MICOM Register CAVCTL2.ROVS[2:0](64h.6-4)
1 : Enable 0 : Disable

Bit4 - JITIEN : Enable/Disable bit of the Jitter Interrupt generated when there is jitter in the Memory Control Block.
1 : Enable 0 : Disable

40h	B7	B6	B5	B4	B3	B2	B1	B0
SYSCONT	CLKSEL	-	MUTE	CDROM	-	S16T24B	ZCMT	-
Reset value	1	-	1	1	-	1	0	-

The SYSCONT Register carries out the general control of the Data Processor.

Bit7 : CLKSEL : Clock Selection Bit
1 : Use PLCK Clock (4.3218 MHz * n speed ratio) when transmitting and handling CD-DA, V/CD, and CD-ROM's ECC.
0 : Use X'tal Clock when transmitting and handling CD-DA and V/CD's ECC (MAX 8x). Use PLCK Clock when exceeding 8x.

Bit5 : MUTE : Mute Control Bit. After Reset, the initial state is Mute ON. Firmware must release the Mute after system is stabilized.
1 : Mute ON.
0 : Mute OFF (normal status).

Bit4 - CDROM : Disc Selection Bit. This bit controls Interpolation. Interpolation can only be carried out in "L" status
in CD-DA Mode .
1 : CD-ROM or Video-CD Mode (INTERPOLATION OFF).
0 : CD-DA Mode (INTERPOLATION ON).

Bit2 - S16T24B : CD-DASP output Format Control Bit.
1 : 32-Bit Slot Out (Toshiba 16-Bit Mode).
0 : 48-Bit Slot Out (Sony 24-Bit Mode).

Bit1 - ZCMT : ZERO-CROSS Mute Control Bit.
1 : Zero Cross Mute ON.
0 : Zero Cross Mute OFF.

42h	B7	B6	B5	B4	B3	B2	B1	B0
SYSINIT	-	MRESET	-	-	-	-	-	RAMCLR
Reset value	-	1	-	-	-	-	-	1

The SYSINIT Register initializes the Data Processor's system.

Bit6 : MRESET : MICOM Master Reset.
Only the Chip is reset by MICOM. A period of time after Reset ON (more than 10 us), the chip automatically turns off the Reset.
1 : Reset OFF. Normal operation mode.
0 : Reset ON.

Bit0 - RAMCLR : SRAM Clear bit for use of ECC.
The RAMCLR bit is "H" after Power-on Reset, and writes initial value "FF" on the ECC SRAM. S5L9250B clears
all ECC SRAMs, makes the RAMCLR Bit into "L", and starts the Main operation.
1 : Enable ECC SRAM Clear.
0 : Disable ECC SRAM Clear.

MONCON : Monitor Output Control Register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
43 H	SLORL1	SLORL0	EFMORP1	EFMORP0	-	-	EFML_EN	PLCK_EN
Reset value	0	0	0	0	-	-	0	0

Bit7 to 6 - SLORL[1:0] : P81 Monitoring Output Selection signal

EFMORP1	EFMORP0	PAD 81 Output
0	0	PEAK (Slicer detected Defect)
0	1	EFMSL (Slicer)
1	0	EFML (PLL)
1	1	WFCK

Bit5 to 4 - EFMORP[1:0] : P78 Monitoring Output Selection signal

EFMORP1	EFMORP0	PAD 78 Output
0	0	0
0	1	0
1	0	PLCK
1	1	RFCK

***** For using Pin78 to output pin, DAOCTRL.MEMPHIN(63h.3) is have to set "L"

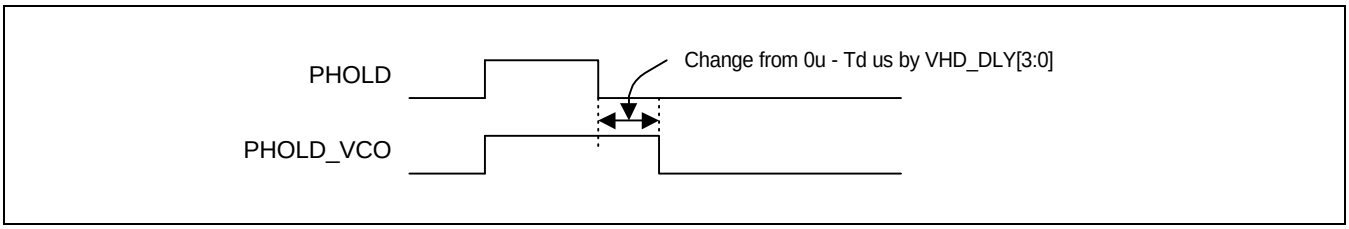
Bit1 - EFML_EN : PLL Block EFML Monitor signal output ENABLE Bit (H Active).

Bit0 - PLCK_EN : PLL BLOCK PLCK Monitor signal output ENABLE Bit (H Active).

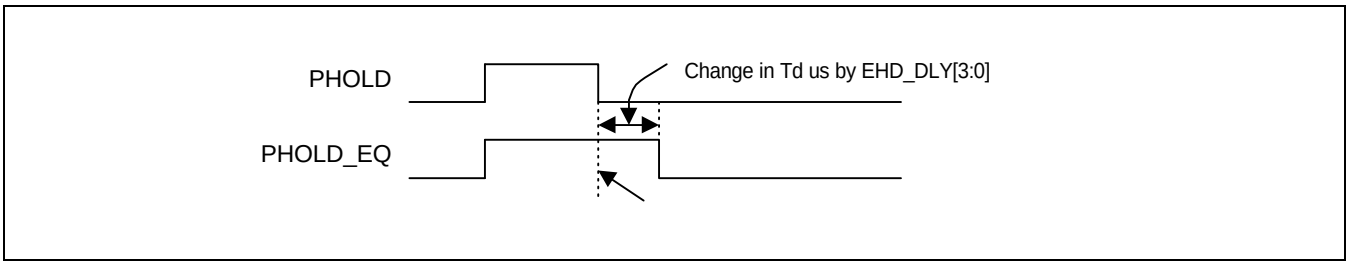
HDDLYCTL : HOLD TIME DELAY Control Register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
44 H	VHD_DLY3	VHD_DLY2	VHD_DLY1	VHD_DLY0	EHD_DLY3	EHD_DLY2	EHD_DLY1	EHD_DLY0
Reset value	0	0	0	0	0	0	0	1

Bit7 to 4 - VHD_DLY[3:0] : After JUMP signal is generated, the VCO HOLD TIME is delayed in 16 stages in units of 30 us from 0 — 420 us according to the VHD_DLY[3:0] value. (JUMP = ATSC + KICK + DFCT from Servo)
¡Ø Refer to 46h Register Description for Td us-related descriptions .



Bit3 to 0 - EHD_DLY[3:0] : After JUMP signal is generated, PLL is LOCKED when SLICTRL2.EQNORDL Bit(59h.1) is "H", then the EQ_HOLD signal is delayed in 16 stages in units of 30 us from 0 ~ 420 us according to the VHD_DLY[3:0] value. (JUMP = ATSC + KICK + DFCT from Servo)



EQVSET : EQ Control Voltage Register (R/W for TEST)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
45 H	-	EQVSET6	EQVSET5	EQVSET4	EQVSET3	EQVSET2	EQVSET1	EQVSET0
Reset value	-	1	0	0	0	0	0	0

Bit6 to 0 - EQVSET[6:0] : When a Long Jump is executed in CAV Mode from an inner disc circumference to an outer circumference, the PLL and EQ blocks can quickly react by MICOM writing the Equalizer control voltage value in EQVSET[6:0] after the jump. MICOM must write the EQVSET value before the Long Jump and set the MTRCTRL.LJUMP(5Ch.7) Bit to "H". The EQ Controller outputs the EQVSET[6:0] value as EQCTL(Pin 128) only while the EQ_HOLD (refer to 4Bh) is being generated while the LJUMP Bit is "H". At all other times, the EQ voltage controller's voltage is output.

JITCTL : Jitter Control Mask Register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
46 H	PHOLD_EX	DLY_SEL[1:0]		KICKEN	AUDRST_EN	MPVCO	MPEQ	-
Reset value	0	00		0	0	0	0	-

Bit7 - PHOLD_EX : This bit decides whether the PHOLD signal should be input as DASP in the Servo Block or into P30.
0 : Servo Part's PHOLD signal input as DASP's PHOLD signal (Normal operation).
1 : Pin 30's input used as DASP Part's PHOLD signal (TEST Mode).

Bit6 to 5 - DLY_SEL[1:0] : This bit decides the delay time after the HDDLYCTL(44h) Register's Falling Edge by designating the Delay Counter's standard Counter Clock.

DLY_SEL[1:0]	Clock Frequency	Standard Delay Time (Td)
00	33.8688 MHz	1.86 us
01	16.9344 MHz	3.72 us
10	8.4672 MHz	7.43 us
11	4.2336 MHz	14.86 us

Bit4 - KICKEN :This bit decides whether or not to use the Servo's Kick signal as the DASP's Jitter Controller control bit.
0 : Do not use Servo Part's KICK signal as DASP's Jitter control signal.
1 : Use the Servo Part's KICK signal as DASP's Jitter control signal for internal SRAM CLEAR.

Bit3 - AUDRST_EN : This bit decides whether or not to use the AUDRST(48h.0) input from MICOM in Audio Buffering Mode after Jump as the Memory Controller's jitter control signal.
0 : Do not use AUDRST Bit as DASP's Jitter control signal.
1 : Use AUDRST Bit as DASP's Jitter control signal.

Bit2 - MPVCO : This bit decides whether or not to use (Phold section + VHD_DLY[3:0]) within the Jitter Control conditions during Phold.
0 : Do not use (Phold section + VHD_DLY[3:0]) Time as a jitter control condition.
1 : Use (Phold section + VHD_DLY[3:0]) Time as a jitter control condition.

Bit1 - MPEQ : This bit decides whether or not to use (Phold section + Time to PLL LOCK generation) + VHD_DLY[3:0])(= PHOLD_EQ) as a jitter control condition during Phold.
0 : Do not use PHOLD_EQ Time as a jitter control condition
1 : Use PHOLD_EQ Time as a jitter control condition.

¡Ø When you use the signal above as the jitter control signal, the ECC SRAM's memory Pointer is initialized, and the data is damaged.

MISC : Miscellaneous Register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
47 H	-	EMSEL	-	EQ_SPD[3:0]				CLK_SV
Reset value	-	0	-	0	0	0	1	0

Bit6 - EMSEL : This bit selects the U bit during DAO output.
1 : Use the P78 input as the DAO Block's Emphasis Bit.
0 : Use the DACCTRL.DEEM(66h.0) Bit input from MICOM as the DAO Block's Emphasis Bit.

Bit4 to 0 - EQ_SPD[3:0] : This bit is for selecting the speed of the RF EQ control voltage generator.

SPD3	SPD2	SPD1	SPD0	Speed	Control Mode	Notes
0	0	0	0	1X	CLV	
0	0	0	1	4X	CLV	
0	0	1	0	8X	CLV, CAV MAX 12X	
0	0	1	1	16X	CAV MAX	
0	1	0	0	20X	CAV MAX	
0	1	0	1	24X	CAV MAX	
0	1	1	0	28X	CAV MAX	
0	1	1	1	32X	CAV MAX	
1	0	0	0	36X	CAV MAX	
1	0	0	1	40X	-	
1	0	1	0	48X	CAV MAX	
1	0	1	1	54X	CAV MAX	
1	1	0	0	60X	CAV MAX	

Bit0 - CLK_SV : This bit selects the Servo Part's System Clock.
1 : Use 33.8688 MHz as the Servo Part's System Clock.
0 : Use 40 MHz, the frequency generated using the Servo Part's built-in PLL, as the Servo Part's System Clock.

AUDCTL : AUDIO Buffering Control Register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
48 H	DEEM_EN	SCSELP	SCSEL	PLCK_WINS	SUBDENSEL	SYNCSEL	-	AUDRST
Reset value	0	0	0	0	1	1	-	0

Bit7 - DEEM_EN : 1-Bit DAC De-Emphasis feature's MASK Bit (66h.DEEM & DEEM_EN).
1 : De-Emphasis Masking ON.
0 : De-Emphasis Masking OFF.

Bit6 - SCSELP : This bit decides whether to use scand or scor as the subcode sync output to the CDROM decoder.
0 : scor.
1 : scand.

Bit5 - SCSEL : This bit decides whether to use scand or scor in the subcode data handling block as the subcode sync signal after the subcode sync det/prot/ins.
0 : scor.
1 : scand.

Bit4 - PLCK_WINS : This bit compares the phase of the detected subcode sync and subcode enable signal to detect the presence of subcode sync.
0 : Do not compare phase.
1 : Compare phase.

Bit3 - SUBDENSEL : Subcode sync. pattern detection enable.(When Subcode sync. Insertion, protection mode) Default value is 'H'.

Bit2 - SYNCSEL : This bit decides whether to execute subcode sync protection / insertion.
0 : Do not execute subcode sync prot / ins.
1 : Execute subcode sync prot / ins**.**

Bit0 - AUDRST : MICOM sets this bit to "H" at the end of a jump when one is being executed in Audio Buffering Mode. It is used in the Memory Controller's jitter control to clear the jitter between the Write and Read parts, minimizing the jitter between the Subcode Part and Main Data in Audio Buffering Mode. MICOM must write "L" before carrying out the following action.
1 : Clear the jitter of the Memory Controller.
0 : Do not use in the Memory Controller's jitter control.

This bit must be used with the JITCTL.AUDRST_EN(46h.3) bit set to "H".

49h	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ECCCTRL0	ERAMOD	C1FLG	C2FLG	-	-	-	OFC2	C2ECC
Reset value	0	0	0	-	-	-	1	1

Bit7 : ERAMOD : C2 Max Erasure correction mode
0 : Carry out Erasure correction when "Number of Erasure = 4".
1 : Carry out Error Correction when "Number of Erasure = 4".

Bit6 : C1FLG : Flag generating conditions during C1 correction.
0 : Generate flag even during MAX correction.
1 : Generate flag only when correction is impossible.

Bit5 : C2FLG : Flag generating conditions during C2 correction.
0 : Generate flag even during MAX correction.
1 : Generate flag only when correction is impossible.

Bit1 : OFC2 : C2 correction mode during overflow.
1 : Correct Error.
0 : Do not correct Error.

Bit0 : C2ECC : C2 correction mode selection (when overflowc2 is 1).
0 : Execute 2 Error correction when an overflag is generated during C2 correction.
1 : Execute 1 Error correction when an overflag is generated during C2 correction.
(When 2 errors are generated, do not carry out correction, but handle it as impossible to correct.)

4Ah	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ECCCTRL1	JUMPEN	MRESYNEN	JITTEREN	C2PSEL	C2FGTYPE3	C2FGTYPE2	C2FGTYPE1	C2FGTYPE0
Reset value	0	0	0	0	1	1	1	1

Bit7 : JUMPEN :
0 : Do not use Servo Part's JUMP signal in ECC PART's C2 correction.
1 : Use Servo Part's JUMP signal in ECC PART's C2 correction.
This bit prevents the incorrect correction within CD-DA Mode's Jump or Defect situations.

Bit6 : MRESYNEN :
0 : Do not execute syndrome recalculation during max erasure correction.
1 : Execute syndrome recalculation during max erasure correction.

Bit5 : JITTEREN : Noise prevention signal when jitter is generated.
0 : When there is jitter, carry out Interpolation according to the ECC results, then output data.
1 : When there is jitter, hold the Interpolation Part's data for 108 Frames before output.

Bit4 : C2PSEL :
0 : Separately C2PO's High byte and Low Byte for final data output in CD-ROM Mode.
1 : Do not separate C2PO's High byte and Low byte flag for final data output in CD-ROM Mode, but carry out ORRING before output.

Bit3 to 0 : C2FGTYPE[3:0] : C1 Flag Copy Conditions during C2 correction.
[3] : C1 Flag Copy conditions for Max Erasure correction.
[2] : Flag C1 Copy conditions for Max correction.
[1] : Flag C1 Copy conditions during Overflow.
[0] : Flag C1 Copy conditions when correction is impossible.

1 : C1 Flag Copy
0 : C2 Flag Generation

4Bh	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MIXAMPCTL	DSHD	EQHD	SLON	-	-	-	-	-
Reset value	0	0	1	-	-	-	-	-

Bit7 - DSHD : SLICER HOLD signal selection
0 : HOLD OFF
1 : HOLD ON

Bit6 - EQHD : EQ CONTROL HOLD signal selection
0 : HOLD OFF
1 : HOLD ON

Bit5 - SLON : Output control for EFMI NOISE elimination (EFMSL is masked in the Slicer Block).
0: Do not output EFMSL.
1: Output EFMSL(Initial value).

¡Ø EQ_HOLD = ((ATSC+KICK+DFCT) + EHD_DLY[3:0])(=PHOLD_EQ) & EQHD)
¡Ø DS_HOLD = (DSHD & (ATSC+KICK+DFCT))
¡Ø EFMSL_PAD = (SLON & EFMSL)

4Ch	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SBSY	SS0WSEL	SS1WSEL	SS0WNDRST	SS1WNDRST	SS0ISEL[1:0]		SS1ISEL[1:0]	
Reset value	0	0	0	0	0	0	0	0

Bit7 - SS0WSEL : This bit sets the subcode sync(s0) detection window range.
0 : 1 frame
1 : 2 frames

Bit6 - SS1WSEL : This bit sets the subcode sync(s1) detection window range.
0 : 1 frame
1 : 2 frames

Bit5 - SS0WNDRST : This bit opens the subcode sync(s0)'s protection window so that the detected sync can be read as subcode sync.
0 : Do not open.
1 : Open.

Bit4 - SS1WNDRST : This bit opens the subcode sync(s1)'s protection window so that the detected sync can be read as subcode sync.
0 : Do not open.
1 : Open.

Bit3 to 2 SS0ISEL[1:0] : Number of subcode sync(ds0) insertion blocks.
00 : 1 block
01 : 2 blocks
10 : 3 blocks
11 : 4 blocks

Bit1 to 0 SS1ISEL[1:0] : Number of subcode sync(ds1) insertion blocks.
00 : 1 block
01 : 2 blocks
10 : 3 blocks
11 : 4 blocks

4Dh	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DAOSUB	M2DSUBCODE[7:0]							
Reset value	00							

Bit7 to 0 - M2DSUBCODE : MICOM inputs subcode into this bit for DIGITAL AUDIO OUT output. The Default is "00", and usually ties the DAO Format's U Bit to "L" for output.

51h	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PLLCTRL0	-	PLCKSET[1:0]		-	-	-	UPDN[1:0	
Reset value	-	11		-	-	-	0	0

Bit7 to 5 - PLOCKSET[1:0] : This block selects the Frequency Detector Hold range after the PLL Lock falls.

00 : 4 Frames
01 : 6 Frames
10 : 8 Frames
11 : 10 Frames

Bit1 UPDN[1:0] : UP/DOWN current measurement selection (TEST MODE)

00 : Hi-Z for VCO Measurment
01 : Up for UP current measurement
10 : Down for DN current measurement
11 : Reserved

52h	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PLLCTRL1	TMX1	TMX0	-	SLPD1	SLPD0	-	TALGC	-
Initial Value	0	1	-	1	1	-	0	-

Bit7 to 6 - TMX[1:0] : TMAX Detection period selection in the Frequency Detector; Selected according to the number of EFM Transitions.

TMX1	TMX0	Content	Notes
0	0	32 Transitions	
0	1	64 Transitions	
1	0	128 Transitions	Recommended
1	1	256 Transitions	Test

Bit4 to 3 - SLPD[1:0] : PD (Phase Detector) selection
"00" : UP/DN Phase Detector outputs every ± EFM/2 edges
"01" : Increases UP/DN width to 1 PLCK at "00".
"10" : UP/DN Phase Detector outputs every ± EFM edges
"11" : Increases UP/DN width to 1 PLCK at "10".

Bit1 - TALGC : CLV/CAV selection signal.
0 : CLV (recommended for all modes)
1 : CAV

53h	B7	B6	B5	B4	B3	B2	B1	B0
PLLCTRL2	iDACp5	iDACp4	iDACp3	iDACp2	iDACp1	iDACp0	VCOFIX	VCOHD
Initial Value	1	0	0	0	0	0	0	0

Bit7 to 2 - iDACp [5:0]:Charge Pump UP current gain adjustment (Only applicable to PD. Selected by speed).
Charge Pump UP current = N * Iref
Here, N is the decimal value shown by iDACp [5:0], and
Iref = 95μA (RDAC = 22kΩ)

Bit1 - VCOFIX : Prevents PLL errors during DISC STOP.

0	Normal VCO Operation
1	Fix VCO voltage to 1.65 V

Bit0 - VCOHD : VCO Defect Hold selection (PHOLD_VCO & VCOHD).
0 : Hold OFF
1 : Hold ON

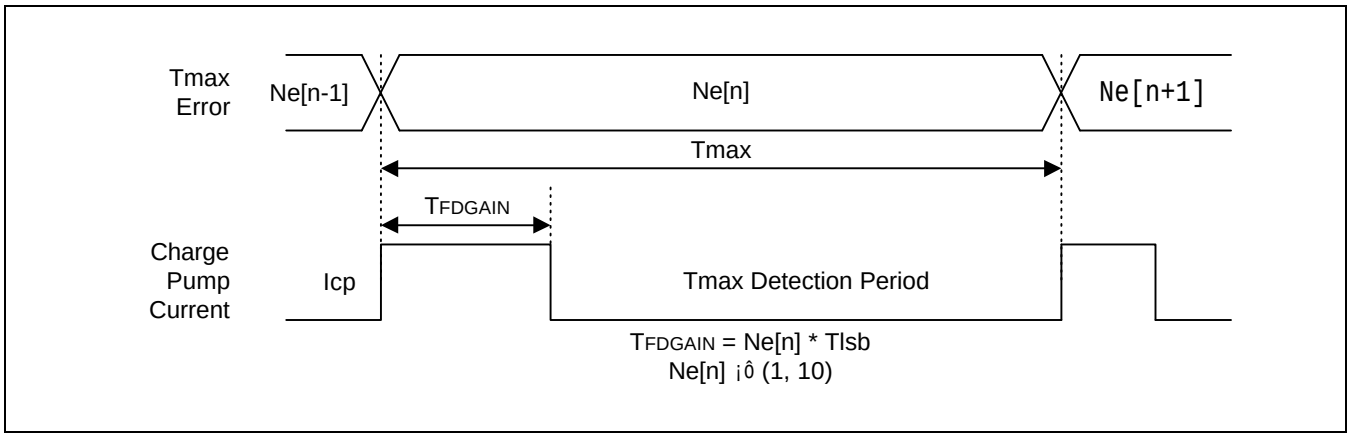
54h	B7	B6	B5	B4	B3	B2	B1	B0
PLLCTRL3	iDACn5	iDACn4	iDACn3	iDACn2	iDACn1	iDACn0	-	SLEFM
Initial Value	1	0	0	0	0	0	-	0

Bit7 to 2 : iDACn[5:0] : Charge Pump Down current gain adjustment (Only applicable to PD. Selected by speed).
Charge Pump Down current = N * Iref
Here, N is the decimal value shown by iDACn[5:0], and
Iref = 95μA (RDAC = 22kΩ)

Bit1 to 0 - SLEFM : Extracts PLL PD input signal and Channel Clock, and chooses the signal that latches the Channel Data.
1 : TEST EFMSL signal input (P95).
0 : Slicer's EFMSL input.

55h	B7	B6	B5	B4	B3	B2	B1	B0
PLLCTRL4	FDGAIN[7:0]							
Initial Value	0	1	0	0	0	0	0	0

Bit7 to 0 - FDGAIN[7:0] : The minimum pulse width data of the current output to the FDO by the Charge Pump.
The minimum pulse width, Tlsb, is found by the following formula:
Tlsb = 2 *(NFDGAIN+1)/fsys
Here, fsys ; System (33.8688 MHz)
NFDGAIN ; Decimal Value shown by FDGAIN[7:0].



56h	B7	B6	B5	B4	B3	B2	B1	B0
PLLCTRL5	PWM[7:0]							
Initial Value								

Bit7 to 0 - PWM[7:0] : Same timing generated as 55h for ALGC PWM use.

57h	B7	B6	B5	B4	B3	B2	B1	B0
SLICTRL0	-	SLFIX[6:0]						
Initial Value	-	0	0	0	0	0	0	0

Bit6 to 0 : - SLFIX[6:0] : Slicer level fix voltage (25.7 mV/ LSB, VDD = 3.3 V).
0 1 1 _ 1 1 1 1 : VDD
//
0 0 0 _0 0 0 0 0 : Vref (1.65 V)
//
1 0 0 _0 0 00 0 : GND

58h	B7	B6	B5	B4	B3	B2	B1	B0
SLICTRL1	LPFS	RES2	RES1	RES0	SLEN	INLG2	INLG1	INLG0
Reset value	0	0	0	0	0	0	0	0

Bit7 - LPFS:
1 : LPF1 Select For CD 24X, 32X, 40X, 48X.
0 : LPF0 Select For CD 1X, 4X, 8X, 16X.

Bit6 to 4 - RES2 to 0 : RFI block Input impedance , Rin.
"000": 1.5kΩ "010": 2.5 kΩ "100" : 5kΩ "110" : 10kΩ
"001": 2kΩ "011": 3kΩ "101" : 6.5kΩ "111" : 40kΩ

Bit3 - SLEN : Slice HOLD use.
1 : Use HOLD.
0 : Do not use HOLD.

Bit2 to 0 - INLG2 to 0 : Data Slicer AMP Gain Selection

1) AMP Gain (Ka = 1 + Ra2 / Ra1 , Ra1=10 Kohm)

INLG2	INLG1	INLG0	Ka [times]	Ra2 [Kohm]
0	0	0	1.0	0
0	0	1	1.5	5
0	1	0	2.0	10
0	1	1	5.0	40
1	0	0	10	90
1	0	1	20	190
1	1	0	30	290
1	1	1	50	490

59h	B7	B6	B5	B4	B3	B2	B1	B0
SLICTRL2	TSLCS	EQFIX	PKEN	PKCTL	DFRL[2:0]			-
Reset value	0	0	-	-	0	0	0	-

Bit7 : TSLCS:
1 : Slicer Level Fix Voltage Monitor
0 : Duty Feedback Data Slicing Level Voltage Monitor

Bi6 : EQFIX:
1 : EQ control voltage output by EQVSET[6:0]
0 : Normal Operation

Bit5 : PKEN : RFsignal PEAKING prevention after DEFECT.
1 : Apply PEAKING prevention.
0 : Do not apply PEAKING prevention.

Bit4 : PKCTL : Use PHOLD signal for SLICE as the SLICER HOLD signal.
(Used together with DSHD, and only applicable when SLICTRL1.SLEN (58h.3) is 'H'.)

DSHD	PKCTL	Function
0	0	No HOLD signal
0	1	Use DEFECT signal generated in SLICE
1	0	Use RF's DEFECT signal
1	1	Use RF DEFECT + SLICE DEFECT signal

Bit3 to 1 : DFRL[2:0] : DEFECT detection signal period for SLICE.
000 : PLCK*28T 001 : 42T 010 : 56T 011 : 70T
100 : 84T 101 : 98T 110 : 112T 111 : 126T

5Ah	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
EFMCTRL1	SUBCON	SBFLUSHEN	-	-	WSEL1	WSEL0	GSEL1	GSEL0
Reset value	0	0	-	-	0	0	0	0

Bit 7 : **SUBCON** : Sync protection WINDOW section selection.
1 : Output after synchronizing MAIN DATA and SUBCODE.
0 : Output without regard to MAIN DATA and SUBCODE sync.

Bit 6 : **SBFLUSHEN** : SUBCODE Buffer Flush MASK Bit.
1 : Flush SUBCODE Buffer when Jitter is generated.
0 : Prohibit SUBCODE Buffer Flush when Jitter is generated.

Bit 5 - SSEL ; SPINDLE PWM output Source selection signal. (Test bit)
1 : Pre D-EQ signal output.
0 : Post D-EQ signal output.

Bit 3 to 2 : **WSEL[1:0]** : Sync Protection WINDOW Section Selection

WSEL1	WSEL0	Frame Sync Protection Window
0	0	± 3 clocks
0	1	± 7 clocks
1	0	± 13 clocks
1	1	± 20 clocks

Bit 1 to 0 : **GSEL[1:0]**: Number of frames for Frame Sync insertion.

GSEL1	GSEL0	Number of Frames for Frame Sync Insertion
0	0	2 Frames
0	1	4 Frames
1	0	8 Frames
1	1	13 Frames

5Bh	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
EFMCTRL2	-	CK33MSEL	-	-	-	-	GFSDET	WNDRST
Reset value	-	0	-	-	-	-	0	0

Bit 6 : CK33MSEL : 33.8688 MHz System Clock output selection bit (PAD 40).
1 : 33.8688 MHz System Clock output Enable.
0 : 33.8688 MHz System Clock output Disable.

Bit 1 : GFSDET : Good Frame Sync detection condition.
1 : Accept as GFS even if there is a 1-bit difference with detected Sync.
0 : Perfect synchronization between detected and inserted Sync.

Bit 0 : WNDRST : Window Reset.
Open window if this bit is "High". It is used when you want to lock the window quickly by detecting new sync during track jump.

5Ch	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
MTRCTRL	LJUMP	LOCKEX	MON_EX	DCTL	SPD3	SPD2	SPD1	SPD0
Reset value	0	0	0	0	0	0	0	1

Bit7 - LJUMP : If MICOM sets this bit to "H" during a Long Jump or 2/3 Stroke, you must write "L" first, then "H" before the next operation. Before setting the LONG JUMP Bit to "H", first write the EQ control voltage applicable to EQVSET[6:0](45h).

0	Normal Operation
1	Long Jump

Bit6 - LOCKEX : Chooses and inputs the Servo Part's CLV LOCK signal (for TEST).

0	Receive CLV LOCK signal from interior (DASP), and output CLV LOCK signal from PAD 79.
1	Receive CLV LOCK signal from exterior (PAD29), and output CLV LOCK signal from PAD 79.

Bit5 - MON_EX : This bit decides whether the Servo Part should accept the Spindle Motor ON/OFF signal from the exterior, or the DASP output signal. The SMONsignal is output to PAD27.

0	Input DASP's SMON signal from the interior to the SERVO.
1	Input the SMON signal to P29 (TEST MODE).

Bit4 - DCTL : Disc Motor Control Mode.

0	CLV
1	CAV

Bit3 to 0 - SPD[3:0] : Speed Mode.

SPD3	SPD2	SPD1	SPD0	Speed	PLL Division Rate	Control MODE
0	0	0	0	1X	32	CLV
0	0	0	1	4X	8	CLV
0	0	1	0	8X	4	CLV, CAV MAX 12X
0	0	1	1	16X	3	CAV MAX
0	1	0	0	20X	3	CAV MAX
0	1	0	1	24X	2	CAV MAX
0	1	1	0	28X		CAV MAX
0	1	1	1	32X	1.5	CAV MAX
1	0	0	0	36X	1.5	CAV MAX
1	0	0	1	40X	1.5	-
1	0	1	0	48X	1	CAV MAX
1	0	1	1	54X	1	CAV MAX
1	1	0	0	60X	1	CAV MAX

VCO band 1

VCO band 2

VCO band 3

Incompatible

5Dh	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
FCSEL	FPLUS	ULHD	FAGD	RCAV	FNCW1	FNCW0	FCW1	FCW0
Reset value	0	0	1	0	0	0	1	0

Bit7 - FPLUS : PLUS ONLY MODE.
Carries out acceleration control when LOCK is HIGH. Deceleration control prohibited.
1 : Execute 0 : Do not execute

Bit6 - ULHD : Maintain previous value when CLV is unlocked.
1 : Use previous value 0 : Do not use previous value

Bit5 - FAGD : FREQUENCY CONTROL AUTO GAIN DOWN
1 : -12dB GAIN DOWN when unlocked.
0 : No Gain Down even when unlocked.

Bit4 - RCAV : ROUGH CAV MODE.
1 : When unlocked, limit the number of Disc Motor rotation to between the MIN and MAX. If a Lock Flag is generated, revert to CLV Mode. .
0 : AFC output when unlocked.

Bit3 to 2 - FNCW1 to 0 : AFC UNCONTROL RANGE (Dead Zone) SETTING.

FNCW1	FNCW0	Content
0	0	Do not use uncontrolled area.
0	1	Uncontrolled area ± 6.25%
1	0	Uncontrolled area ± 12.5%
1	1	Uncontrolled area ± 25%

Bit1 to 0 - FCW1 to 0 : AFC LINEAR CONTROL RANGE SETTING.

FCW1	FCW0	Initial Value	Division Rate (N)	Linear Control Range
0	0	200H	1	± 10%
0	1	480H	2	± 20%
1	0	5C0H	4	± 40%
1	1	RESERVED		

5Eh	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
PCSEL	FGSEL[1:0]		FGWDT	MOTSEL	PCEN	PCR	PCW1	PCW0
Reset value	00		0	0	1	0	1	1

Bit7 to 6 - FGSEL[1:0] : This bit selects the FG Counter to react to the 6/12 pole MOTOR's various FG.

FGSEL[1:0]	Division Rate
00	1
01	2
10	3
11	6

Bit5 - FGWDT ; FG signal ONESHOT PULSE WIDTH (Standard signal is generated at each disc rotation).
1 : 75 us width.
0 : 150 us width.

Bit4 - MOTSEL ; SPINDLE MOTOR selection signal.
1 : 12 pole Motor.
0 : 6 pole Motor.

Bit3 - PCEN ; PHASE CONTROL ENABLE
1 : Enable 0 : Disable

Bit2 - PCR : PHASE CONTROL RANGE
1 : Execute within AFC 25%.
0 : Execute within AFC 50%.

Bit1 to 0 - PCW1 to 0 : Phase Control period selection.

PCW1	PCW0	Control Period
0	0	24 Frames
0	1	48 Frames
1	0	96 Frames
1	1	192 Frames

5Fh	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
PCOFFS	POFFS7	POFFS6	POFFS5	POFFS4	POFFS3	POFFS2	POFFS1	POFFS0
Reset value	0	0	0	0	0	0	0	0

Bit7 to 0 : POFFS7 to 0 : Adds a set Offset value to the final output value according to motor type, in order to minimize the direct current residual deviation.

60h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
EMOSEL	CLVHD	SMON1	SMON0	SPOLAR	KICK	BRAKE	PWMCA1	PWMCA0
Reset value	0	0	0	0	0	0	1	0

Bit7 : CLVHD : Mask signal that holds the Spindle Motor Control if a disc defect or an external shock is detected in the set during Seek in the Servo IC.
"L" : Do not hold Spindle Motor control (Normal operation).
"H" : Hold Spindle Motor control.

Bit6 to 5 : SMON1 to 0 : Disc Motor On Mode

SMON1	SMON0	Operation
0	-	Disc Motor OFF , Fix ERROR handling OP AMP output to VDD/2
1	0	Disc Motor ON , Fix SMOF / SMOP output to Hi-Z
1	1	Disc Motor ON , Normal control operation

Bit4 : SPOLAR : Disc Motor Rotation Direction.
0 : Clockwise Direction.
1 : Counter clockwise Direction.

Bit3 : KICK : Disc Motor MAX Acceleration.
0 : Normal Control operation.
1 : Fix SMOF / SMOP output to VDD.

Bit2 : BRAKE : Disc Motor MAX deceleration.
0 : Normal Control operation.
1 : Fix SMOF / SMOP output to GND.

Bit1 to 0 : PWMCA1 to 0 : PWM Carrier Frequency Selection.

PWMCA1	PWMCA0	PWM Carrier Frequency
0	0	7.35 * 2 kHz
0	1	7.35 * 4 kHz
1	0	7.35 * 12 kHz
1	1	7.35 * 36 kHz

61h, 62h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
CAVSEL1	CAVCK[2:0]			-	-	-	CAVR[9:8]	
Reset value	0	0	0	-	-	-	0	0
CAVSEL2	CAVR[7:0]							
Reset value	0	0	0	0	0	0	0	0

In CAV Mode, Disc rotation velocity can be found using the following formula:
DISC RPM = (fsys * Nck * 10) / (1024 * (1793 - Ncavr))
Here, fsys ; System Clock (33.8688 MHz)
Ncavr ; Decimal Value shown by CAVR[9:0]
Ncavr = Σ CAVR[i] * 2^i (1 $\leq$ CAVR $\leq$ 381H)
Nck ; Clock division value selected by CAVCK[2:0]

CAVCK[2]	CAVCK[1]	CAVCK[0]	Nck	Disc RPM Range (MIN RPM at CAVR==1, MAX RPM at 381H)
0	0	0	1	184.6 to 369.1
0	0	1	2	369.1 to 738.3
0	1	0	4	738.3 to 1476.6
0	1	1	8	1476.6 to 2953.1
1	0	0	16	2953.1 to 5906.3
1	0	1	32	5906.3 to 11812.5
1	1	0	64	11812.5 to 23625.0

— MICOM Selection Method.
(1) Select the number of rotations that you want.
(2) Select Nck value according to the number of rotations. <- CAVCK[2:0] selection
(3) Calculate initial value Ncavr using the formula given above (Binary).
(4) CAVCK[2:0], CAVR[9:0] Data transmission.

— The AFC/APC control range can change according to the Ncavr variance.
; AFC control range increase (7.14 - 14.28%).
APC control range decrease (100 - 50%).

63h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
DAOCTRL	DAOEN	-	-	-	MEMPHIN	copyen	emphen	acmode
Reset value	0	-	-	-	1	0	0	0

Bit 7 - DAOEN : DIGITAL AUDIO OUT Enable/Disable Bit.
1 : Output DIGITAL AUDIO OUT from S5L9250B.
0 : Do not output DIGITAL AUDIO OUT from S5L9250B.

Bit 3 - MEMPHIN : DIGITAL AUDIO OUT Block's CONTROL signal input Bit.
1 : Use EMPH signal as the DAO Block input in P78.
0 : Use DEEM(66h.0) & DEEM_EN(48h.7) signal as DAO BLOCK input.

Bit 2 to 0 decides whether to allow COPY during DAO output, execute pre-emphasis, and to have 2 or 4 audio channels. Its value is decided by MICOM.

Bit 2 - COPYEN : This bit decides whether to allow Digital Audio Out Block Copy.
1 : Allow Digital Copy.
0 : Prohibit Digital Copy.

Bit 1 - EMPHEN : This bit tells you if there is pre-emphasis on the Digital Audio Out block's output.
1 : Pre-Emphasis ON
0 : Pre-Emphasis OFF.

Bit 0 - ACMODE : This bit tells you if the DAO output Audio is 2-Channel or 4-Channel.
1 : 4-Channel Audio
0 : 2-Channel Audio.

64h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
CAVCTRL	ROTSEL	ROVS2	ROVS1	ROVS0	RIS1	RIS0	FAL1	FAL0
Reset value	0	0	1	1	1	1	0	1

Bit7 : ROTSEL : Motor Rotation Direction Polarity Switching (Initial Value = `0`)
0 : Direction when the DIRROT signal input from the Drive IC is "H".
1 : Direction when the DIRROT signal input from the Drive IC is "L".

Bit6 to 4 : ROVS2 to 0 : Motor runaway discrimination standard selection

ROVS2	ROVS1	ROVS0	Content
0	0	0	Above 3000 RPM
0	0	1	Above 4000 RPM
0	1	0	Above 5000 RPM
0	1	1	Above 6000 RPM
1	0	0	Above 7000 RPM
1	0	1	Above 8000 RPM
1	1	0	Above 10000 RPM
1	1	1	Above 12000 RPM

Bit3 to 2 : RIS1 to 0 : Delay adjustment after GFS is "H" and before CLV LOCK becomes "H"
(Initial Value = '11').
00 : CLV LOCK is "H" when GFS's "H" continues for more than 2 WFCK (or FRAME SYNC).
01 : CLV LOCK is "H" when GFS's "H" continues for more than 4 WFCK (or FRAME SYNC).
10 : CLV LOCK is "H" when GFS's "H" continues for more than 8 WFCK (or FRAME SYNC).
11 : CLV LOCK is "H" when GFS's "H" continues for more than 16 WFCK (or FRAME SYNC).

Bit1 to 0 : FAL1 to 0 : Delay adjustment after GFS is "L" and before CLV LOCK becomes "L"
(Initial Value = '01').
00 : CLV LOCK is "L" when GFS's "L" continues for more than 256 WFCK (or FRAME SYNC).
01 : CLV LOCK is "L" when GFS's "L" continues for more than 128 WFCK (or FRAME SYNC).
10 : CLV LOCK is "L" when GFS's "L" continues for more than 64 WFCK (or FRAME SYNC).
11 : CLV LOCK is "L" when GFS's "L" continues for more than 32 WFCK (or FRAME SYNC).

66h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
DACCTRL	DN	SDACCK	PWRSAVE	H2L3	-	MUTEL	PDL	DEEM
Reset value	0	0	0	0	-	0	1	0

Bit7 : DN : 1-bit DAC speed mode.
0 : Normal speed.
1 : Double speed.

Bit6 : Built-in 1-Bit DAC System Clock Source selection signal.
0 : Input 17MHz system clock to 1-bit DAT within the IC.
1 : Input system clock output from an external IC supplying CD-AUDIO DATA to 1-Bit DAC.

Bit5 : PWRSAVE : POWER SAVE mode.
0 : Normal Operation.
1 : Power Saving Mode ON.

Bit4 : H2L3 : Built-in 1-Bit DAC System clock division rate => 16.9344MHz.
0 : Divide PAD 95 input CLOCK by 3 for use (50.8MHz / 3).
1 : Divide PAD 95 input CLOCK by 3 for use (33.8MHz / 2).

Bit2: MUTEL : 1-Bit DAC Mute Control Bit (Initial state is ON).
0 : 1-Bit DAC Mute ON.
1 : 1-Bit DAC Mute OFF (Normal Operation).

Bit1: PDL : 1-Bit DAC POWER SAVING Control Bit.
0 : 1-Bit DAC Power Saving Mode ON.
1 : 1-Bit DAC Power Saving Mode Off (Normal Operation).

Bit0 : DEEM : De-Emphasis Enable (48h.7 DEEM_EN Bit and AND Operation).
0 : De-Emphasis OFF
1 : De-Emphasis ON

67h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
DATTN	-	-	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
Reset value	-	-	0	0	0	0	0	0

Bit5 to 0 : ATTL5 - ATTL0 : Digital Attenuation Level (both L/R). Controls 1-Bit DAC output.

ATTL5 to ATTL0	Attenuation Level (dB)	ATTL5 to ATTL0	Attenuation Level (dB)
0 0 0 0 0 0	0	1 0 0 0 0 0	-6.30
0 0 0 0 0 1	-0.28	1 0 0 0 0 1	-6.58
0 0 0 0 1 0	-0.42	1 0 0 0 1 0	-6.88
0 0 0 0 1 1	-0.56	1 0 0 0 1 1	-7.18
0 0 0 1 0 0	-0.71	1 0 0 1 0 0	-7.50
0 0 0 1 0 1	-0.86	1 0 0 1 0 1	-7.82
0 0 0 1 1 0	-1.01	1 0 0 1 1 0	-8.16
0 0 0 1 1 1	-1.16	1 0 0 1 1 1	-8.52
0 0 1 0 0 0	-1.32	1 0 1 0 0 0	-8.89
0 0 1 0 0 1	-1.48	1 0 1 0 0 1	-9.28
0 0 1 0 1 0	-1.64	1 0 1 0 1 0	-9.68
0 0 1 0 1 1	-1.80	1 0 1 0 1 1	-10.10
0 0 1 1 0 0	-1.97	1 0 1 1 0 0	-10.55
0 0 1 1 0 1	-2.14	1 0 1 1 0 1	-11.02
0 0 1 1 1 0	-2.32	1 0 1 1 1 0	-11.51
0 0 1 1 1 1	-2.50	1 0 1 1 1 1	-12.04
0 1 0 0 0 0	-2.68	1 1 0 0 0 0	-12.60
0 1 0 0 0 1	-2.87	1 1 0 0 0 1	-13.20
0 1 0 0 1 0	-3.06	1 1 0 0 1 0	-13.84
0 1 0 0 1 1	-3.25	1 1 0 0 1 1	-14.54
0 1 0 1 0 0	-3.45	1 1 0 1 0 0	-15.30
0 1 0 1 0 1	-3.66	1 1 0 1 0 1	-16.12
0 1 0 1 1 0	-3.87	1 1 0 1 1 0	-17.04
0 1 0 1 1 1	-4.08	1 1 0 1 1 1	-18.06
0 1 1 0 0 0	-4.30	1 1 1 0 0 0	-19.22
0 1 1 0 0 1	-4.53	1 1 1 0 0 1	-20.56
0 1 1 0 1 0	-4.76	1 1 1 0 1 0	-22.14
0 1 1 0 1 1	-5.00	1 1 1 0 1 1	-24.08
0 1 1 1 0 0	-5.24	1 1 1 1 0 0	-26.58
0 1 1 1 0 1	-5.49	1 1 1 1 0 1	-30.10
0 1 1 1 1 0	-5.75	1 1 1 1 1 0	-36.12
0 1 1 1 1 1	-6.02	1 1 1 1 1 1	-¡Ä

2) Read Register

70h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
INTSTAT	SUQINT	REVINT	ROVINT	JITINT	-	-	-	-
Reset value	0	0	0	0	-	-	-	-

Bit7 : SUQINT : Subcode Q Sync Interrupt.

Bit6 : REVINT : When Disc is in reverse rotation, an Interrupt is generated at each disc rotation (FG/6).

Bit5 : ROVINT : If the MOTOR's rotation velocity exceeds that set by MICOM (ROVS[2:0]), an Interrupt is generated at each disc rotation (FG/6).

Bit4 : JITINT : "H" when there is jitter in the DASP PART's MEMORY Controller.

FRAME Counter Value Read Register

Address	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
71h	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8
72h	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0

Bit15 to 0 : FC[15:0]

— Carries out UP-COUNT for each frame and notifies MICOM.

— If actual data is written on a different linear speed because of differences in the disc manufacturing process, this bit is used for correcting the linear speed difference by allowing MICOM to calculate it.

SUBQ DATA Read Register

Address	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
73h	CTL3	CTL2	CTL1	CTL0	ADR3	ADR2	ADR1	ADR0
74h	TNO7	TNO6	TNO5	TNO4	TNO3	TNO2	TNO1	TNO0
75h	INDEX7	INDEX6	INDEX5	INDEX4	INDEX3	INDEX2	INDEX1	INDEX0
76h	MIN7	MIN6	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
77h	SEC7	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
78h	FRM7	FRM6	FRM5	FRM4	FRM3	FRM2	FRM1	FRM0
79h	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO
7Ah	AMIN7	AMIN6	AMIN5	AMIN4	AMIN3	AMIN2	AMIN1	AMIN0
7Bh	ASEC7	ASEC6	ASEC5	ASEC4	ASEC3	ASEC2	ASEC1	ASEC0
7Ch	AFRM7	AFRM6	AFRM5	AFRM4	AFRM3	AFRM2	AFRM1	AFRM0

2) Read Register

7Dh	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
C1EBYTE	C1EBYTE[8:1]							
Reset value	0	0	0	0	0	0	0	0

— C1EBYTE[8:0] : Number of Error bytes generated during C1 correction calculated according to SUBCODE Sync.

7Eh	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
C1ECODE	C1EBYTE[0], C1ECODE[6:0]							
Reset value	0	0	0	0	0	0	0	0

— C1ECODE[6:0] : Number of uncorrectable error codewords generated during C1 correction. Updated at each SUBCODE Sync.

7Fh	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
DPSTAT	SBQERR	-	-	-	-	-	-	-
Reset value	0	-	-	-	-	-	-	-

Bit7 : SBQERR : Shows the presence of errors in SUBCODE 80byte at each SUQINT.
1 : Errors present after SUB-Q CRC Check.
0 : No errors present after SUB-Q CRC Check.

80h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
C2EBYTE	C2EBYTE[8:1]							
Reset value	0	0	0	0	0	0	0	0

— C2EBYTE[8:0] : The Number of Error bytes generated during C2 correction calculated according to the SUBCODE Sync.

81h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
C2ECODE	C2EBYTE[0], C2ECODE[6:0]							
Reset value	0	0	0	0	0	0	0	0

— C2ECODE[6:0] : The number of uncorrectable error codewords during C2 correction calculated according to SUBCODE Sync.

82h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
RBCH	-				RBC[11:8]			
Reset value	-				0	0	0	0

83h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
RBCL	RBC[7:0]							
Reset value	0	0	0	0	0	0	0	0

— RBC[11:0] : Read Frame Counter value during JITTER Interrupt generation.

84h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
WBCH	-				WBC[11:8]			
Reset value	-				0	0	0	0

85h	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
WBCL	WBC[7:0]							
Reset value	0	0	0	0	0	0	0	0

— WBC[11:0] : Write Frame Counter value during JITTER Interrupt generation.

CLOCK GENERATION

The CLKEGN block generates all the clocks used within the CD-DSP part and the signals related to the reset of each block. All clocks used in the CD-DSP are made from the 33.8688 MHz frequency generated from a crystal. These clocks go through muxing according to the speed and audio output format mode operation demanded by MICOM, and are then output. During scan test, all clocks operate at the clock speed input into the sysclk (33.8688 MHz function operation).

1) I/O Description

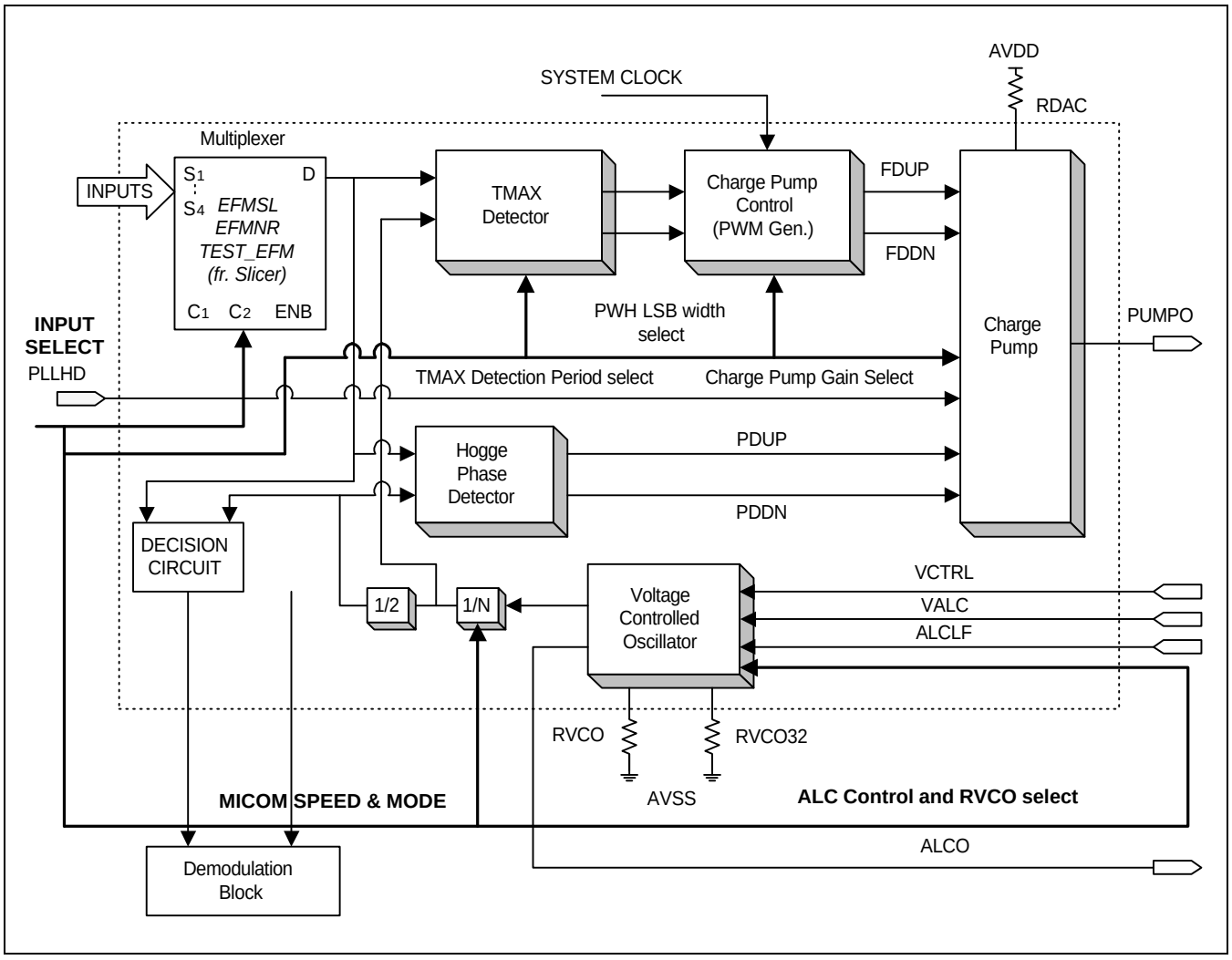
Pin Name	I/O	To/From	Descriptions
i_rstb	I	External	System Reset From Outside
sysclk	I	External	33.8688MHz clock
wfck	I	EFM	7.35kHz clock from EFM
dctl	I	MICOM	Disc mode signal from MICOM
spd_mode	I	MICOM	Playing speed mode
out_mode	I	MICOM	Audio output mode (0: 24-bit mode, 1:32-bit mode)
i_test_en	I	External	Scan test enable (1: test mode)
o_rstb	O	Internal Block	reset signal to each block. Negative logic
rfck	O	Clock Gen	7.35kHz clock at x'tal
o_RFCntENb	O	Clock Gen	Read frame counter enable.
o_WFCntEnb	O	Clock Gen	Write frame counter enable.
o_JitterCntEnb	O	Clock Gen	Jitter counter enable.
o_rstECUb	O	Clock Gen	ECU block reset signal. Low active.
o_ReqAddrRst	O	Clock Gen	Interpolator Data address request signal reset. High active

CHANNEL CLOCK RECOVERY PLL

Features

— Single LPF (Loop Filter) regardless of speed
— ± 50% wide capture range
— Loop gain automatic adjustment feature for CAV control
— Disc Defect and Shock handling
— Servo track jump handling
— Sync. frame noise reduction
— Programmable charge pump current setting (two 6-bit iDAC)

Block Diagram



Block Description

PLL receives a signal called EFMI as its input, which zero crosses the signal input from the RF block into in the slicer, handles it in digital signal level, and outputs it. The PLL synchronizes this standard input signal (EFMI) with its built-in VCO clock frequency and phase. The VCO clock in sync with the EFMI signal is appropriately divided according to speed. Jitter is eliminated by latching the input signal once with this clock. This is to reduce the errors when demodulating back to the original signal in the DSP block. The PLL is often called the decision circuit.

I/O Definition

Symbol	I/O	Description	comment for one-chip
EFMSL	I	Simple Slicer Output	From Data Slicer
EFMNR	I	Slicer Output with Noise Rejection	
EFMGN	I	EFM Pattern Generation by DSP (for Test)	From DSP
iDACO	O	Charge Pump Output	
VCTRL	I	VCO Control Voltage	
RVCO	B	VCO V/I Converting Resistor	
RDAC	B	Biasing Resistor for iDAC at Charge Pump	
VALC	I	Reference Voltage for Automatic Loop Gain Control (ALC)	
ALGCO	O	ALGC PWM Output (Digital Level)	
ALCLF	I	ALC PWM LPF Output (DC Voltage, Analog Level)	
PLLHD	I	Set High when DFCT, SHOCK, Track Jump	From DSP
CLVLOCK	I	CLV LOCK indicator	From CLV/CAV
PLCK	O	VCO Clock Divided by N	To DSP
EFML	O	Retimed EFM by PLCK	To DSP
PLOCK	O	PLL LOCK indicator with Hysterisis	
PLOCK1	O	PLL LOCK indicator without Hysterisis	To Data Slicer
CK33	I	SYSTEM CLOCK 33 MHz	
Other MICOM Registers	I	MICOM Interface	From MICOM I/F

MICOM Registers

Please refer to the MICOM Register Descriptions.

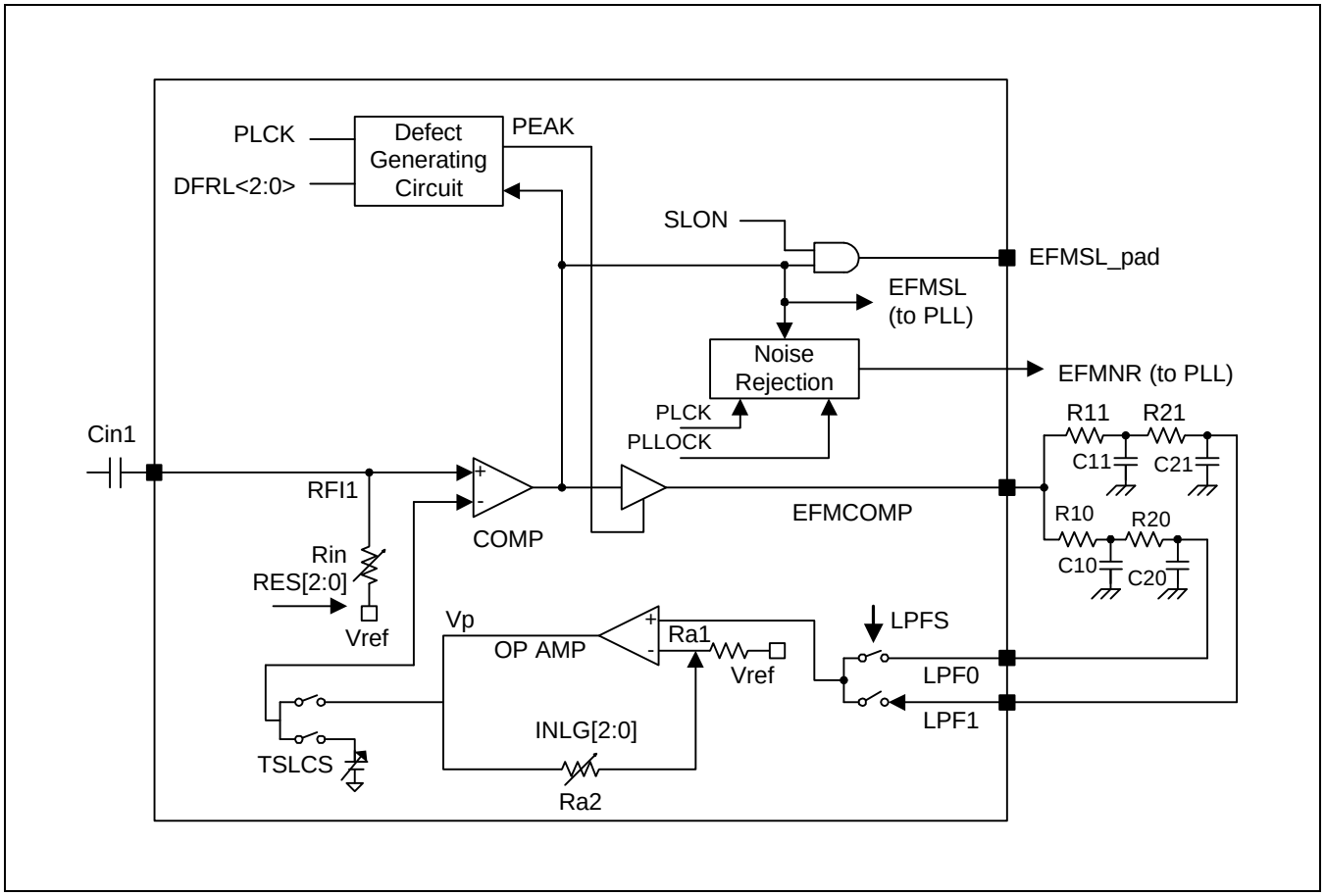
DATA SLICER & EQ REMOVAL

Data Slicer

Data Slicer Characteristics

- 2 STEP integration area selection conversion
- RF input size: min = 0.5 Vpp , Max = 1.5 Vpp
- 8 STEP RF input Impedance select
- 8 STEP AMP Gain select
- Hold feature
- Noise Rejection circuit

Block Diagram



SAMSUNG ELECTRONICS

Block Description

— This block uses the EFM signal's DSV characteristics to integrate the comparator output's duty and track the slicing level to use the Duty Feedback method.

— The Noise Rejection has a pulse width of less than 1.5T for Data Slicing output.

I/O Definition

Symbol	I/O	Description	Comment for one-chip
RFI	I	Eye Pattern from RF	PAD
EFMCOMP	O	Duty Feedback Slicer output	PAD
EFMSL	O	Duty Feedback Slicer, Current control method Slicer output	MONITOR
LPF0	I	LPF input (CD X1,X4,X8)	PAD
LPF1	I	LPF input (CD X16, X24)	PAD
LPFS	I	'L' : LPF0 'H' : LPF1	MICOM (Reset : L)
TSLCS	I	'H' : Slice Level Fix voltage 'L' : Slicer Level voltage	MICOM (Reset : L)
DSLCS	I	'L' : Duty Feedback Slicer 'H' : DIGITAL Method Slicer	MICOM (Reset : L)
RES[2:0]	I	8Step's input Impedance select	MICOM (Reset : LLL)
INLG[2:0]	I	Input Gain select	MICOM (Reset : LLL)
HOLD	I	Hold signal in case of Defect	Internal (Defect : H)
EFMNR	O	Slice signal after Noise Rejection	Internal
PLCK	I	Channel Bit Clock	Internal
PLLOCK	I	PLL Lock signal	Internal (Lock : H)
PEAK	O	Defect detection signal	

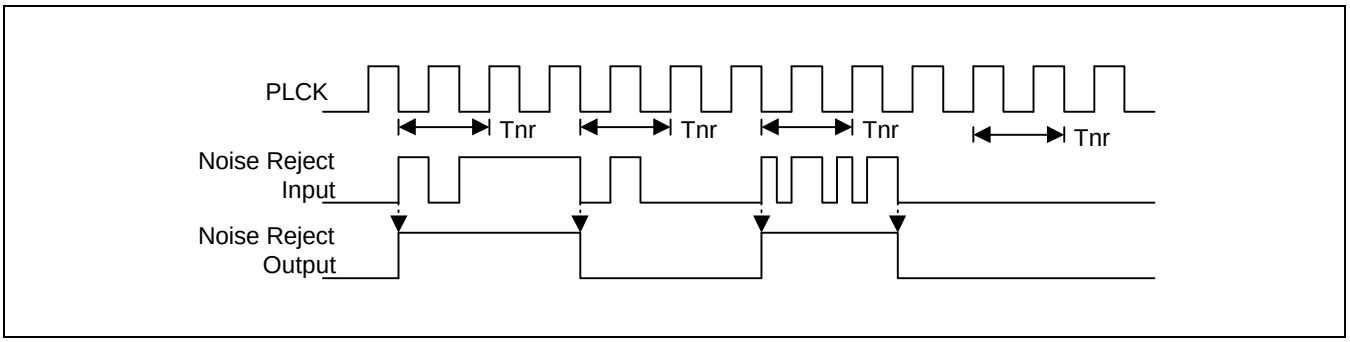
Related Register

SLICTRL1	B7	B6	B5	B4	B3	B2	B1	B0
58H	LPFS	RES2	RES1	RES0	SLEN	INLG2	INLG1	INLG0
Reset value	0	0	0	0	0	0	0	0

SLICTRL2	B7	B6	B5	B4	B3	B2	B1	B0
59H	TSLCS	EQFIX	PKEN	PKCTL	DFRL2	DFRL1	DFRL0	-
Reset value	0	0	0	0	0	0	0	

Timing Diagram

- After the NR input signal transition is generated, the block operates only for reverse transitions larger than the Noise Rejection width.
- The block operates only when PLL is in Lock state.



— Noise Rejection width: Tnr = 1.5 * Tch
Time to the second Rising Edge from the point after input signal Transition (in Lock status, sync with PLCK's Falling Edge).

Control

Characteristics

— Bit Clock Frequency-voltage conversion output for Analog Equalizer control; Center frequency selection change and output fix mode

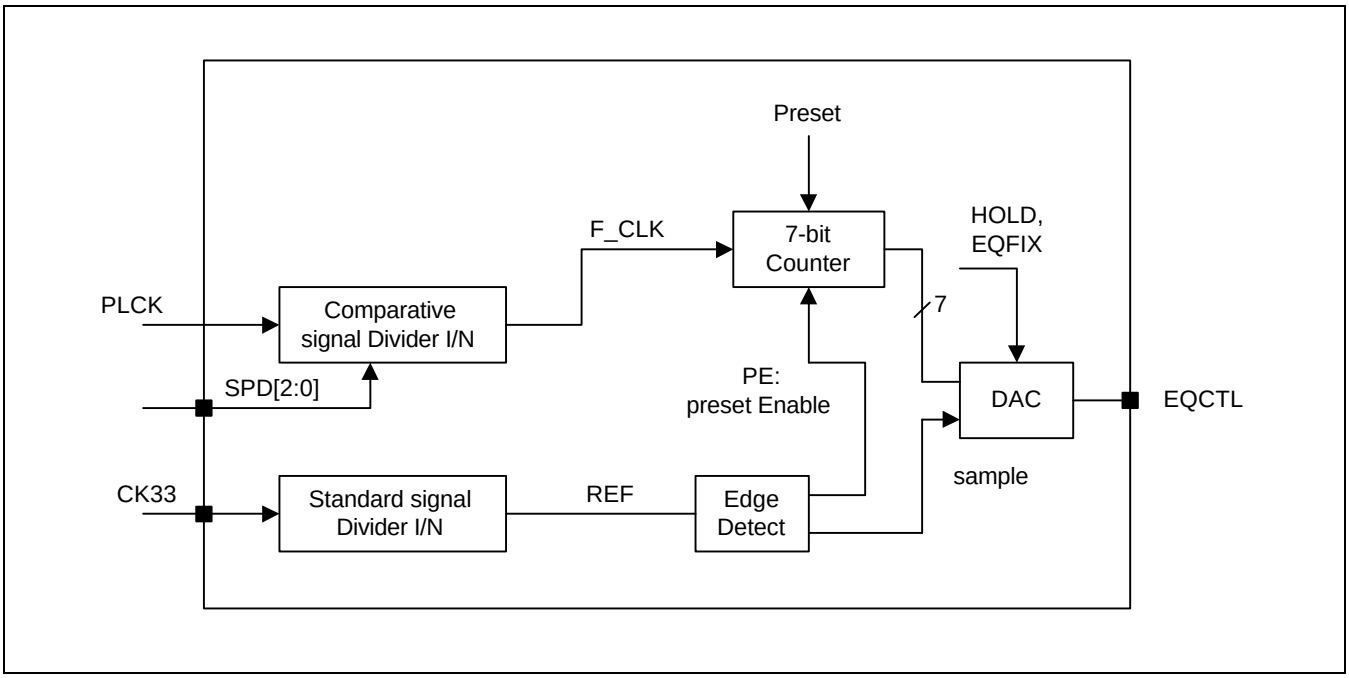
— Input frequency range: 0.5 * fc to 1.5 * fc (fc: F/V Center Freq.)

— F/V Slope : + 1.65 / fc [Volt/Hz] (fc's ± 10% change ± 0.165V output change)

— Linearity: < ± 7% (Ideal output characteristic standard)

— Hold feature

Block Diagram



Block Diagram Description

— CK33-divided REF signal and the PLCK-divided comparative signal are countered, and that counter value is output to the 7-bit DAC for use in the RF Equalizer's control voltage.

— In case of a defect, a Hold signal is received to hold to the previous control voltage, and a MICOM Register (EQFIX) controls the control voltage to eqvset[6:0].

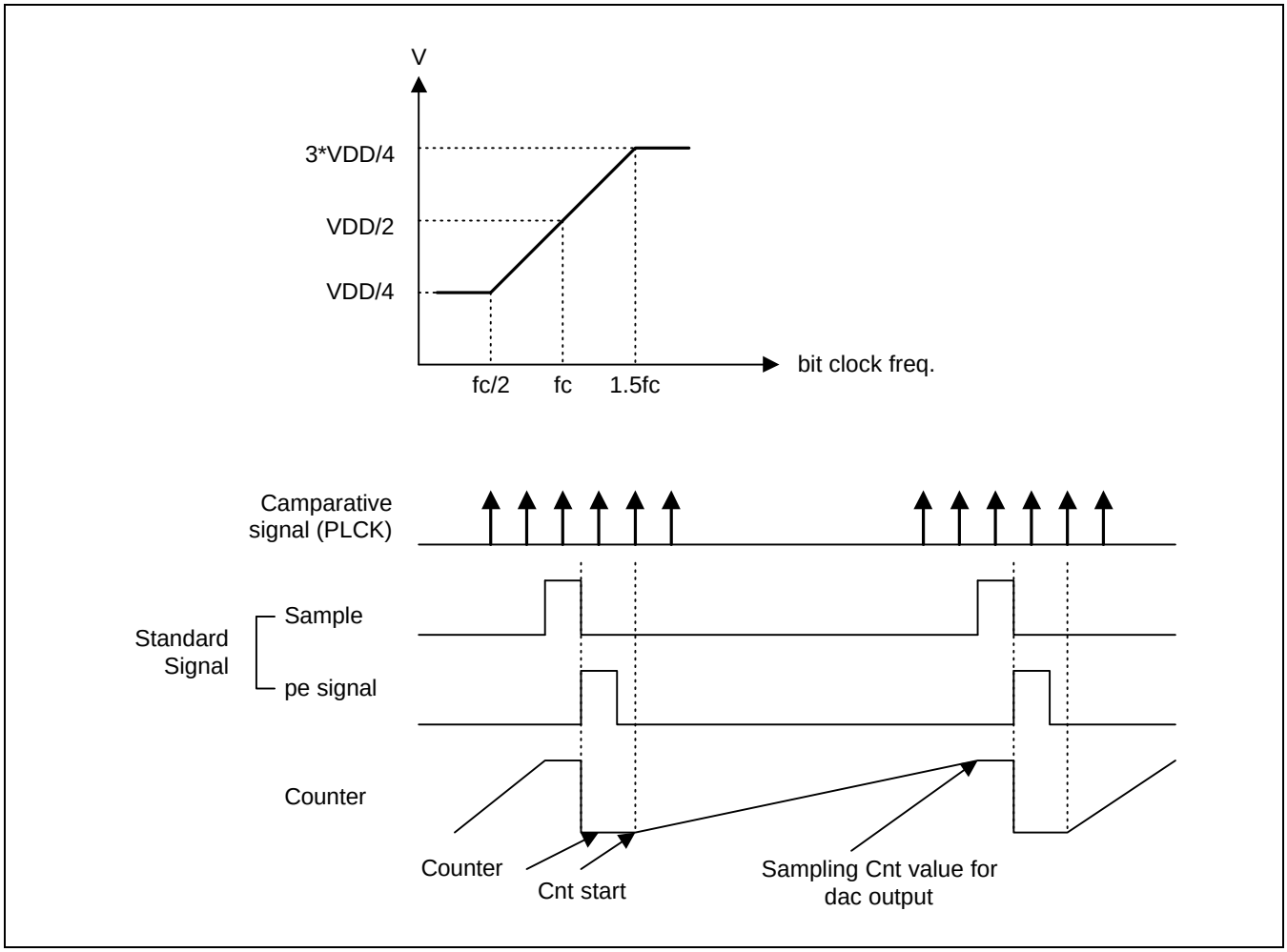
I/O Definition

Symbol	I/O	Description	comment for one-chip
PLCK	I	Channel Bit Clock	Internal
EQFIX	I	EQ output voltage controlled to Eqvset [6:0]	MICOM Register
HOLD	I	Hold EQ output to previous value in case of Defect	Internal
EQCTL	O	EQ output voltage	PAD
CK33	I	SYSTEM CLOCK	PAD
EQ_SPD[3:0]	I	SPEED MODE	MICOM Register

Related Register and Bit Description

; Please refer to 5.2.5.3.1.5.

Timing Diagram

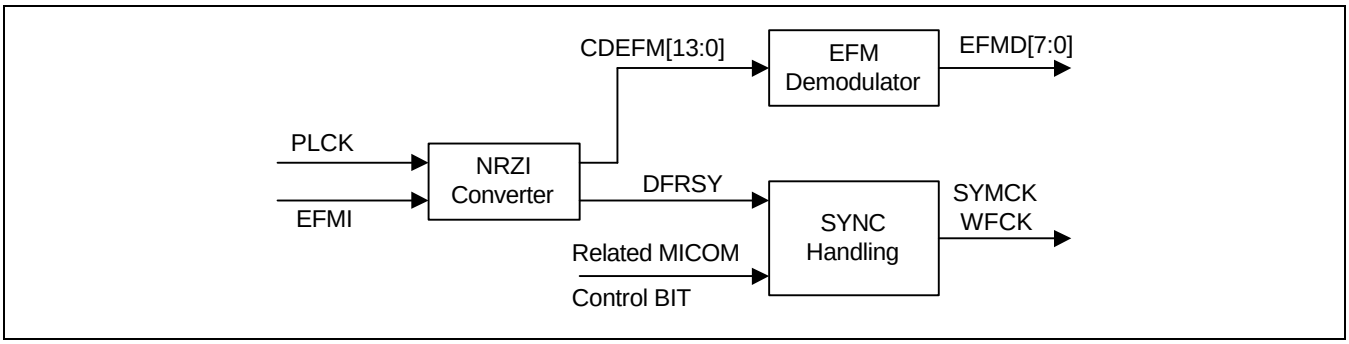


EFM DEMODULATION AND SYNC PROTECTION

Characteristics

- EFM Demodulator
— Converts NRZI Pattern's input signal to NRZ.
— Converts 14-Channel Bit → 8-data bit.
— Subcode Sync detection.
- Sync Detection/Protection/Insertion.
— EFM Sync Protection Window Selection.
— Frame Sync Insertion Frame number selection.
— Frame Sync Detection/Protection/Insertion.

Block Diagram

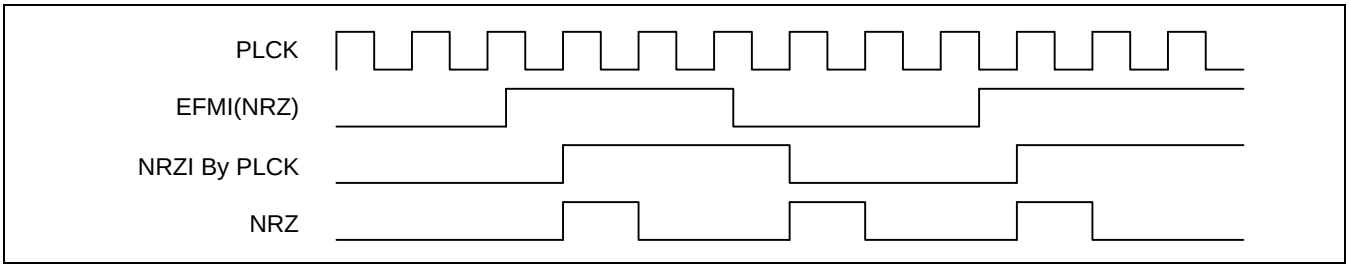


EFM Demodulator's Block Diagram

Block Description

The Bitstream read from the Disc goes through waveform remodelling in the RF and Data Slicer, and is input as NRZI Pattern to the EFM block (EFMI). The EFMI signal phase is synchronized with PLCK (1X : 4.3218 MHz, NX : N * 4.3218 MHz), the PLL output signal locked to the Channel Bit frequency, and then converted into NRZ Pattern. Figure 1 shows the NRZI Conversion's Timing Diagram.

EFM signal uses the internal Shift Register to input the 14 bits of the EFM demodulation signal (3 Merge Bits removed from the 17-bit EFM demodulation signal) as the EFM demodulator's CDEFM[13:0] signal. The 8 Data bit is converted to 14 channel bit according to the conversion table, and demodulation output EFMD[7:0] is output.



NRZI Conversion Timing Diagram

The NRZI-converted EFM signal uses the internal Shift Register to input the 14 bits of the EFM demodulation signal (3 Merge Bits removed from the 17-bit EFM demodulation signal) as the EFM demodulator's CDEFM[13:0] signal. The 8 Data bit is converted to 14 channel bit according to the conversion table, and demodulation output EFMD[7:0] is output.

Frame Sync (24 Channel Bit Length) detection also uses internal Shift Register to prevent the detection of mistaken sync by setting Window sections. It outputs Frame period's WFCK signal, and the EFM Symbol Data period, SYMCK. If the Frame sync and inserted Frame sync coincide when detecting sync signals, the GFS (Good Frame Sync) is output to the Pin.

I/O Definition

Symbol	I/O	Description	comment for one-chip
PLCK	I	Channel Bit Clock	from PLL
EFMI	I	EFM NRZ INPUT	from PLL
EFMD[7:0]	O	EFM Demodulation output	to internal SRAM
DFRSY	-	Detected Frame Sync	Internal signal
CDEFM¡¸13:0¡¹	-	Out of CD DATA 17 bits, 14 bits of CD Data excluding the 3 Merge bits	Internal signal
Related MICOM Control BIT	I/O	EFM control-related MICOM BIT	FROM/TO MICIF
SYMCK	O	33 SYMCLK generated in FRAME SYNC section	to CD-DSP
WFCK	O	VCO CLOCK for CLV use, 7.35 kHz	to CD-DSP
GFS	O	"H" when detected Frame Sync and inserted Frame Sync coincide	**PAD**, to CLV Part

Related Register

5Ah(W)	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
EFMCTRL1	SUBCON	SBFLUSHEN	-	-	WSEL1	WSEL0	GSEL1	GSEL0
Reset value	0	0	-	-	0	0	0	0

5Bh(W)	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
EFMCTRL2	-	CK33MSEL	-	-	-	WLOCK	GFSDET	WNDRST
Reset value	-	0	-	-	-	0	0	0

SPINDLE MOTOR CONTROL

Characteristics

— CD AUDIO/ROM CLV (4X, 8X), CAV(12X, 16X, 24X, 32X, 40X, 48X)

— Wide PLL compatible

— MICOM Setting CAV

— 256-step High Resolution

— Control Range Selection Mode

— Frequency, Phase Error Gain setting Mode

— Output Offset Increase/Decrease feature (compatible with various different motors)

— Low Power Deceleration Prohibition Mode

— Rough CAV Mode

— Emergency Monitor (Detects Reverse Rotation, Speeding)

— Carries out Digital EQ according to speed

— Independent Disc Motor Control
; Direct output to Motor Driver using AFC, APC, and Loop Compensator configuration

Block Description

1) Characteristics

(1) CLV (Constant Linear Velocity)
; Controlled using the Frame Sync separated from Channel Bit Data as the comparative signal.
2 types (CD: 4X / 8X) of different speed modes.

(2) CAV (Constant Angular Velocity)
; Controlled using the FG signal as the comparative signal.
Selects number of disc rotation by MICOM Data (Rotation / standard Clock Data selection).
Number of rotation control range : 245 - 15697 RPM

(3) Rough CAV
; When executing track jump in CLV Mode, automatic conversion to CAV Mode is carried out so that MICOM can directly set the number of disc motor revolutions. Lock Down is usually generated during Track Jump, and when controlled to near the number of tracks being jumped, PLL can easily go to Lock without sudden changes in the Data Rate.

— AFC / APC Gain Selection
; . AFC Auto Gain Down Selection
. By OAK DSP Core
. 3 STEP PWM Carrier frequency change

— 4 STEP AFC linear form control range selection

— 4 STEP AFC Control Dead Zone selection

— 2 STEP APC Control range selection

— Forced output Mode: Forced APC output OFF, output Hold

— 4 STEP Phase Error Sampling frequency selection

— Phase Offset adjustment

— Number of MOTOR Poles: 6 Poles (Standard 3 pulse /revolution)
12 Poles (6 pulse /revolution)

— FG Division Ratio Selection Possible : Division by factors of 1/2/3/6

Block Diagram

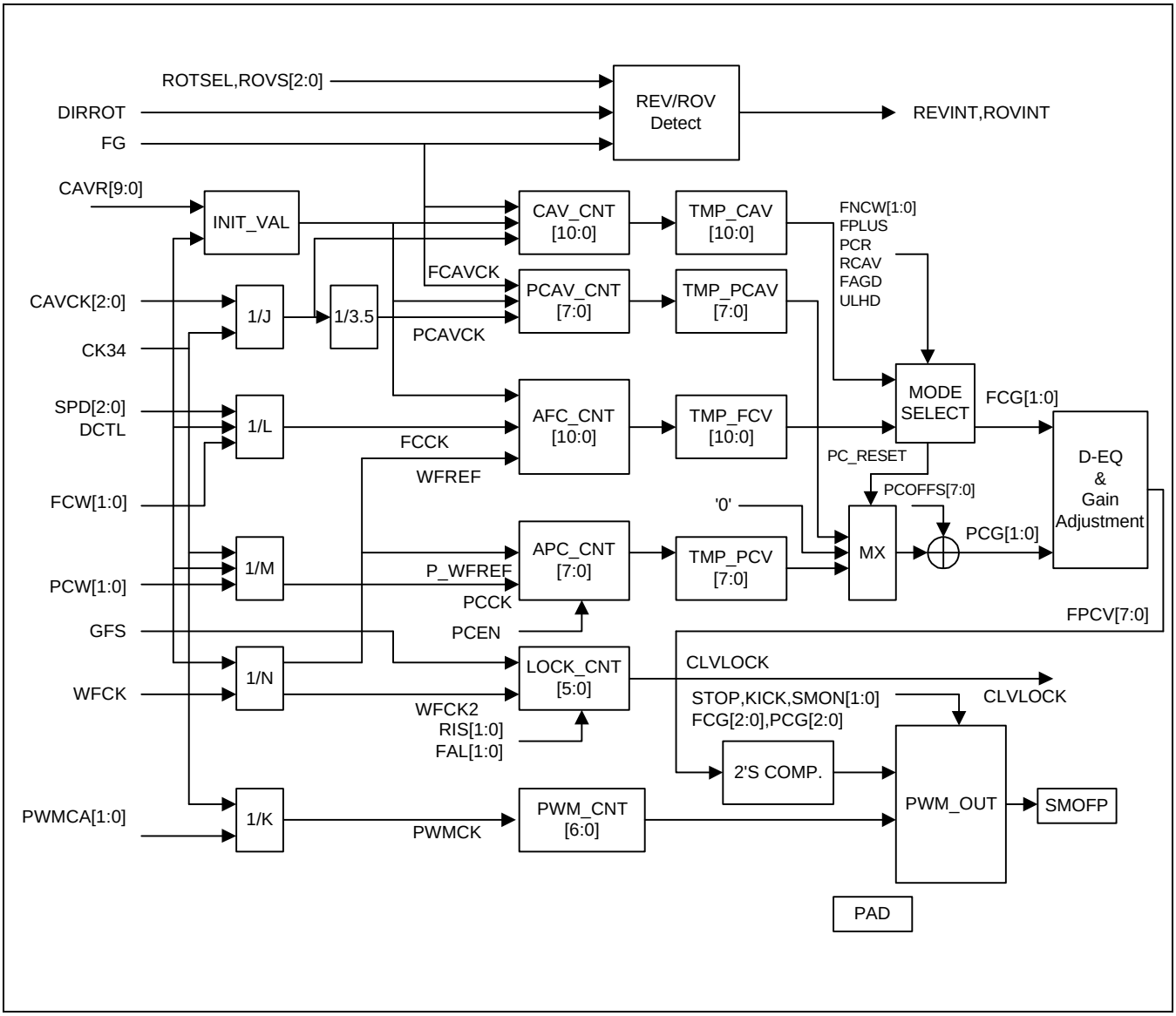


Figure 3. Block Diagram of the Spindle Motor Control Block

I/O Definition

Symbol	I/O	Description	comment for one-chip
CK34	I	XTAL Clock Input for CD (33.8688 MHz)	EXTERNAL
RSTB	I	Reset (Low Active)	EXTERNAL
DIRROT	I	Motor Rotate Direction	EXTERNAL(MOTOR)
FG	I	Frequency Generator (for CAV)	RF
WFCK	I	EFM Dem. Frame Sync	EFM DEM.
GFS	I	Good Frame Sync	EFM DEM.
FPLUS	I	Plus Only Mode	CTR REG
FAGD	I	Frequency Auto Gain Down	CTL REG
RCAV	I	Auto Gain Down	CTL REG
FCW1 - 0	I	FC Control Width	CTL REG
FNCW1 - 0	I	FC No Control Width	CTL REG
SPD2 - 0	I	Spindle Control Speed Select	CTL REG
DCTL	I	Motor Control Method Select	CTL REG
SMON1 - 0	I	Motor Control On	CTL REG
SPOLAR	I	Motor Control Output Polarity	CTL REG
POFFS7 - 0	I	Phase Control Offset	CTL REG
PWMCA1 - 0	I	PWM Carrier Frequency Select	CTL REG
PCEN	I	Phase Control Enable	CTL REG
PCR	I	Phase Control Range Setting	CTL REG
PCW1 - 0	I	Phase Control Period	CTL REG
START	I	Motor Kick	CTL REG
BRAKE	I	Motor Brake	CTL REG
ROTSEL	I	Disc Rotation Direction Select	CTL REG
ROVS2 - 0	I	Overrun Detect Condition Setting	CTL REG
RIS1 - 0	I	CLV Lock Condition	CTL REG
FAL1 - 0	I	CLV Unlock Condition	CTL REG
CLVLOCK	O	CLV Lock	MONITOR
REVINT	O	Reverse Rotate Interrupt	MICOM I/F
ROVINT	O	Overrun Interrupt	MICOM I/F
SPINDLE	O	PWM (Frequency + Phase) Output	PAD

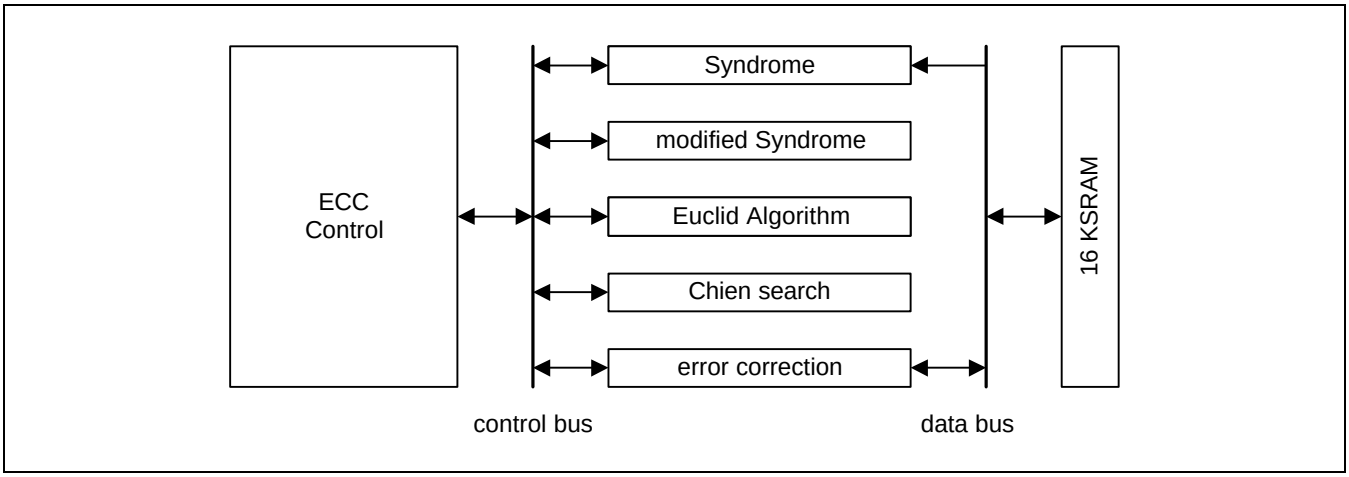
C1/C2 ERROR CORRECTION

Block Description

— Double correction for C1 & quadruple correction for C2,

— using an internal 16 K bit SRAM.

Block Diagram



Detailed Function Description

— C1 pointer (flag) for prevention of C2 miscorrection, according to the C1 error status (c1flg).

— C2 pointer (flag) for Interpolation (CD-Audio) or continuous ECC (CD-ROM), according to the C2 error status (c2flg).

— C2 error corrector executes 3 symbol erasure, 4 symbol erasure or 2 symbol error correction according to the MICOM register (eramod, c2ecc).

— Monitoring of correction status using the MICOM register (c1ebyte, c1ecode, c2ebyte, c2ecode).

I/O Pins

— No external pins (PAD)

MICOM Registers

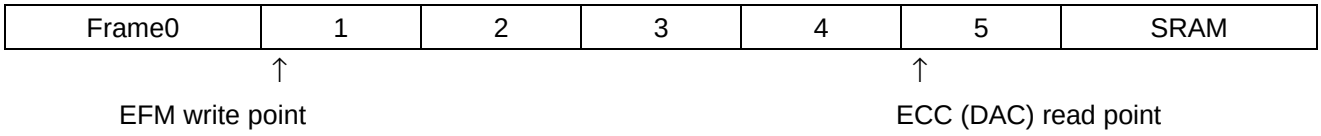
— MICOM write register
. eramod, c1flg, c2flg, c2ecc

— MICOM read register
. c1ebyte, c1ecode, c2ebyte, c2ecode

MMU (MEMORY MANAGEMENT UNIT)

SRAM Resource

Since frame sync period is 7.35 kHz (=4.3218 MHz/588 bits) and the amount of ECC data within 1 frame is 32 bytes, the speed in which data is input into the disc is 235.2 k bytes per second. However, of the ECC data, 8 bytes are parity data, which means that the actual amount of audio data input into the disc is 176.4 k bytes. Also, the data output to DAC is 44.1 kHz, stereosignal is output in units of word (=16 bits), and the output data is 176.4 k bytes per second. Therefore, the ratio of the input and output signal matches at 1:1 on average, but the EFM input data may show a slight difference according to the disc revolution, so you must take this difference into consideration when decoding. Usually, the input data is decoded with a jitter margin of 4 frames. Jitter is the change in EFM input due to various reasons such as disc rotation speed. The change in EFM input amount may overwrite the data being executed, so to prevent this, there is a jitter margin of ± 4 frames. This means that since you need more than 108 frames of data to carry out ECC, the difference between the ECC read point and ECC write point is maintained at within ± 4 frames so that this area is not damaged through EFM write (refer to the figure below).



Of the resources that access internal memory, there are EFM input and ECC that corrects errors, and the Interpolator that interpolates the error.

- **EFM Write**

Within 1 Frame sync period, 32 bytes out of 588 bits are stored in the internal memory. The remaining data are merge bits, sync patterns, and subcode bytes.

- **ECC R/W**

— Address

1) Normal Read Address : Interleaved Data + Parity Data
2) Read/Write Address for Error Data
3) Read/Write Address for C1/C2 data

— Memory Access Occurrence

C1 decoding

- — Data Read : 32 bytes
- — C1 Correction Read/Write : MAX 2/2 bytes
- — C1 Flag write : 1 byte

C2 decoding

— Data Read : 28 bytes
— C1 flag Read : 28 bytes
— C2 correction Read/Write : MAX 4/4 bytes
— C2 flag Write : 12 bytes
— C1 flag Read : 24 bytes

- **Interpolation Read Address - Data + C2PO**

To carry out Interpolation, you need 4 bytes of data read and 2 bytes of C2 erasure read per 44.1 kHz.

Memory Access Timing Analysis

	1 x		N x	
	Number of Data Access	Frequency	Number of Data Access	Frequency
EFM	32 bytes per 7.35 kHz	235.2 kByte/sec	32 bytes per 7.35 * N kHz	235.2 * N kByte/sec
ECC	137 bytes per 7.35 kHz	1006.95 kByte/sec	137 bytes per 7.35 * N kHz	1006.95 * N kByte/sec
Interpolation	6 bytes per 44.1 kHz (36 bytes per 7.35 kHz)	264.6 kByte/sec	6 bytes per 44.1 * N kHz (36 bytes per 7.35 * N kHz)	264.6 * N kByte/sec
Total	181 bytes per 7.35 kHz	1.507 MByte/sec	362 bytes per 7.35 kHz	3.014 MByte/sec

Memory Size & Map

The reason why Memory size is 16K bits (2048 bytes) is because you need 108 frames of data for error correction. The memory is needed as the error correction decoding buffer, audio out buffer, and EFM write's jitter margin. The memory use of each part is shown in the table below.

	Content	Size	Sub-Total	Total
ECC	Data	1560 bytes	1670 bytes	1849 bytes
	C1 Erasure	109 bytes		
	C2 Erasure	1 bytes		
Interpolation	Audio Data	48 bytes	51 bytes	
	C2 Erasure	3 bytes		
EFM	Data	128 bytes	128 bytes	

As shown in the table above, you need a minimum of 1849 bytes, and there is a reserve of 199 bytes (approximately 6 frames) in case of a change in EFM input rate. MICOM sends a speed control command to the spindle servo to carry out the memory overflow/underflow check, in case jitter exceeds the margin of ±4 frames.

Memory must be used efficiently to carry out decoding within 16 k bits. This is not possible using the address generation method by ALU operation, so you need to store the memory map in ROM for optimization.

Address Generation

EFM Write Address

ECC R/W Address

1) Normal Read Address : Interleaved Data + Parity Date

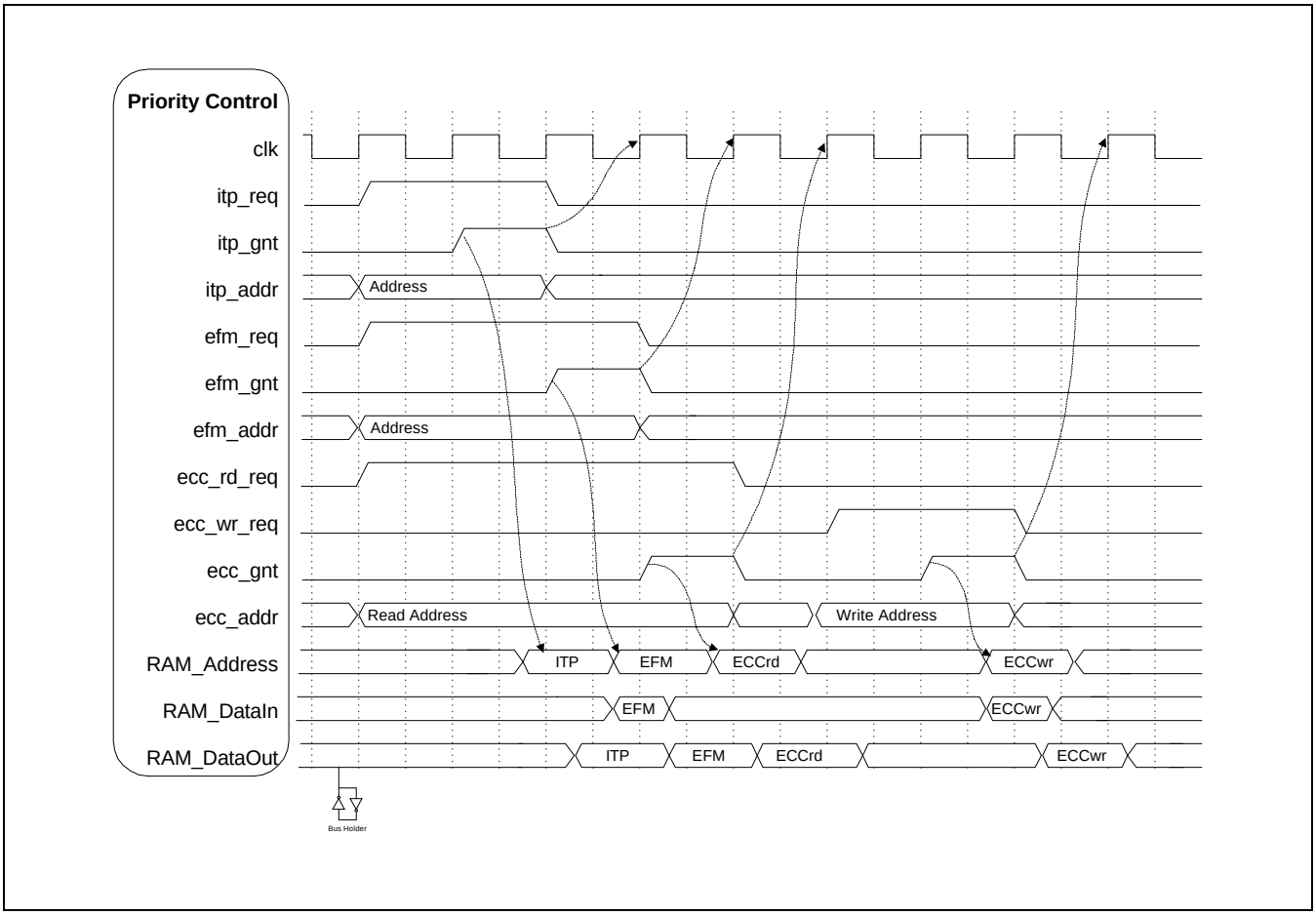
2) Read/Write Address for Error Data

3) Read/Write Address for C1/C2 data

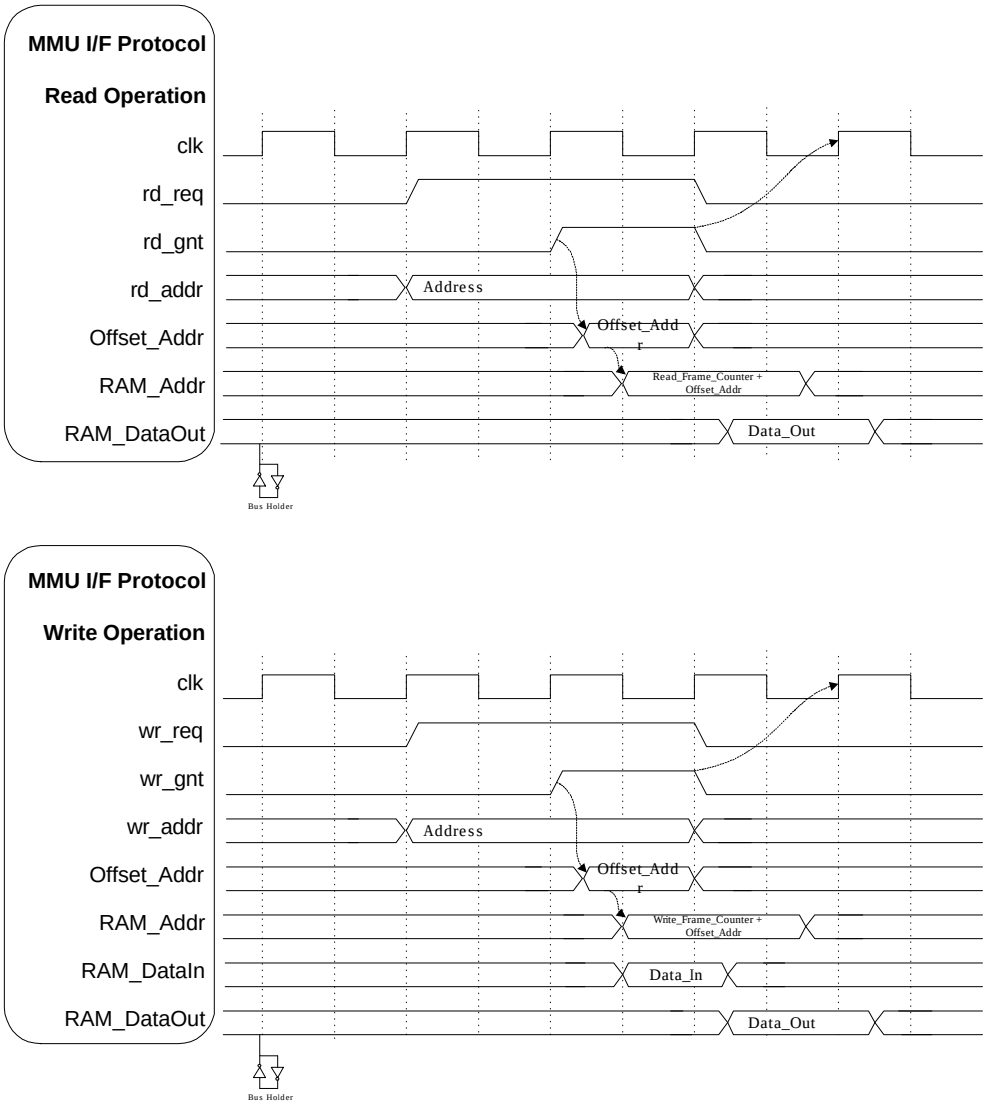
Interpolation Read Address - Data + C2PO

Priority Control

As we saw above, the blocks that access the memory are EFM, ECC, and the Interpolator. There is a priority between these blocks, and the MMU block allows them memory use according to this priority. First priority is given to the Interpolator since there is no way to restore the music once it stops. The EFM that accepts data from the optical disc has second priority, and the ECC that reads data from the buffer and corrects errors has the lowest priority. Also, for active memory access, the other blocks excepting the ECC cannot demand continuous access to data, and is not able to demand data again within 6 clocks of the movement frequency after receiving data. The flowchart given below shows the priority control.



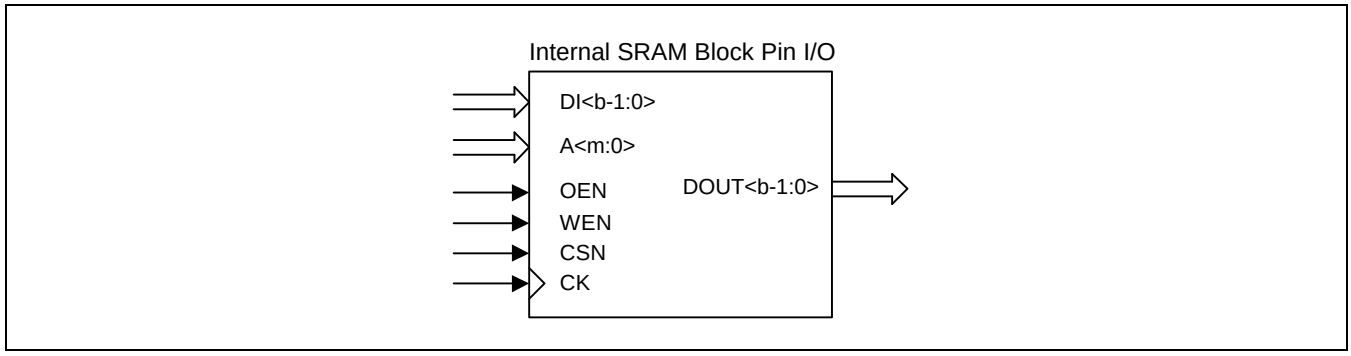
The protocol between the MMU block and each request blocks during read/write are shown in the figure below. Although the number of clocks needed for 1 data access is 3, data access is possible at each clock because of pipeline action.

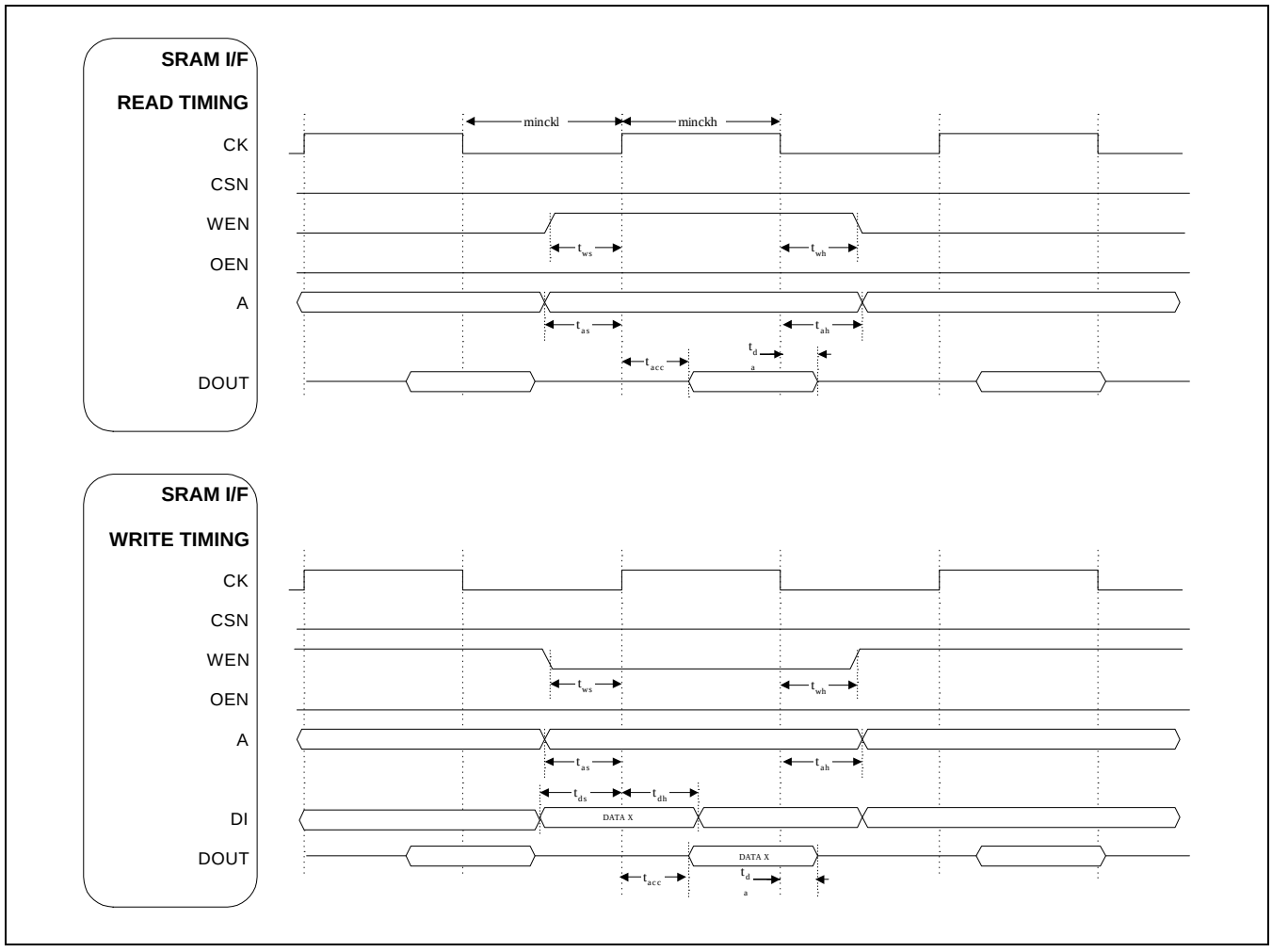


* RAM_DataOut is 8 bits.

Internal SRAM

The I/O and Block Diagram of the SRAM made using the ASIC Design kit is shown below, together with the timing diagram. The SRAM output is valid only for 1 clock period. The output block has a busholder attatched to maintain previous data because of high impedance output.





MMU Block I/O

Port	I/O	To/From	Comment
clk4M	I	CLKGEN	MMU clock (CAV : plck/2, CLV : x'tal/16)
i_rstb	I	CLKGEN	MMU Reset signal
i_EfmReq	I	EFM	EFM write Request
i_EfmAddr	I	EFM	EFM Offset Address
i_EccRdReq	I	ECU	ECC Read Request
i_EccWrReq	I	ECU	ECC Write Request
i_EccAddr	I	ECU	ECC Offset Address
i_ItpReq	I	ITP	Interpolation Read Request
i_ItpAddr	I	ITP	Interpolation Offset Address
i_EfmWrData	I	EFM	EFM Write Data
i_EccWrData	I	ECU	ECU Write Data
I_EccCnt	I	ECU	EccCnt latch Enable Signal
i_AcptEccCnt	I	ECU	EccCnt latch Enable Signal
i_RFCntEnb	I	CLKGEN	Read Frame Counter Count Enable Signal
i_WFCntEnb	I	CLKGEN	Write Frame Counter Count Enable Signal
i_JitterCntEnb	I	CLKGEN	Jitter Calculation Enable Signal
i_MUTE	I	MICOM	Audio mute signal
i_RAMCLR	I	MICOM	ECC SRAM Clear signal
i_KICK_SERVO	I	SERVO	Kick, Lens Kick input signal
i_KICKEN	I	MICOM	Signal that decides whether to use the Servo's Kick signal when controlling DASP jitter.
i_AUDRSTEN	I	MICOM	Signal that decides to use AUDRST input from MICOM after jump in the Audio Buffering Mode as the memory controller's jitter control signal.
i_AUDST	I	MICOM	Signal that selects "H" at the end of a jump from MICOM when executing a jump in Audio Buffering Mode.
i_MPEQ	I	MICOM	Signal that decides whether or not to use the PHOLD_EQ signal in the jitter control conditions.
i_PHOLD_EQ	I	CLKGEN	PHOLD + Time to PLL LOCK + EHD_DLY[3:0]
i_MPVCO	I	MICOM	Signal that decides whether to use the PHOLD_VCO signal in the jitter control conditions
i_PHOLD_VCO	I	CLKGEN	PHOLD + VHD_DLY[3:0]
o_Jitter	O	MICOM	Jitter Monitoring Signal (active High)
o_EfmGntMask	O	EFM	EFM Grant Signal
o_EccGntMask	O	ECU	ECU Grant Signal

Port	I/O	To/From	Comment
o_ItpGntMask	O	ITP	Interpolation Grant Signal
o_EndOfTrx	O	ECU	Indicate signal that is end of tranfer
o_RAMCLRReset	O	MICOM	SRAM Clear complete signal
o_WBC	O	PS	Write Frame Counter output signal
o_RBC	O	PS	Read Frame Counter output signal
o_CSNMask	O	SRAM	memory CSN signal
o_RamWENMask	O	SRAM	memory WEN signal
o_RamAddrMask	O	SRAM	memory address
o_RamDataInMask	O	SRAM	write date to memory

SUBCODE INTERFACE (INCLUDING SUB-Q)

Block Description

— extracts 'control & display data' that called Subcode from EFM data stream.

— Subcode Q 98 bits : 2 bits for S0 and S1, 80 data bits, 16 CRC bits

Block Diagram

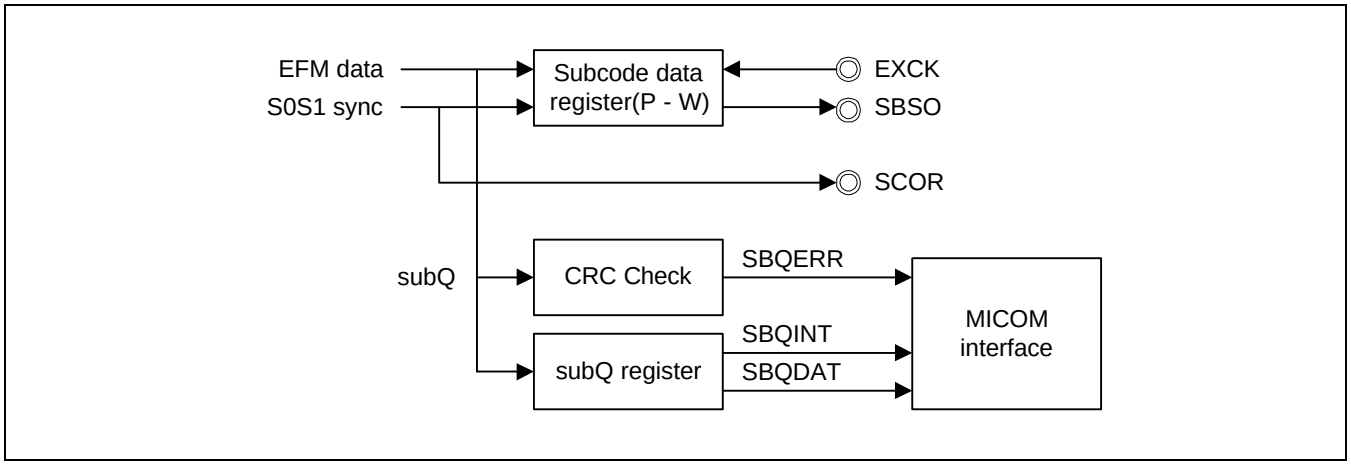


Figure 4. Subcode Handling Block Diagram

Detailed Function Description

— The 8-bit subcodes P - W can be read from SBSO by inputting EXCK.

— subQ 80 bits and CRC check output can be read from MICOM register.

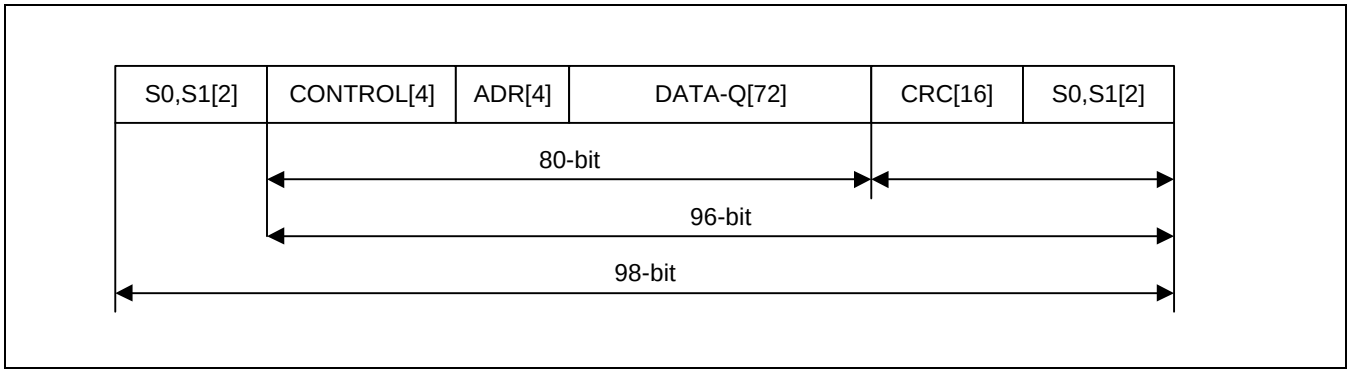


Figure 5. SUB-Q Channel Format

I/O Pin

Symbol	I/O	Description	comment for one-chip
SCAND	I	Subcode Sync (S0 × S1)	from EFM
SCOR	I	Subcode Sync (S0+S1)	from EFM
SBCD[7:0]	I	EFM decoded Subcode Data	from EFM
WFCK	I	Write Frame Sync	from EFM
EXCK	I	Subcode Data Readout Clock	from external PAD
SBSO	O	Subcode P to W serial output	to external PAD
WFCKO	O	Delayed WFCK(Write Frame Clock)	to external PAD
SCORO	O	when either S0 or S1 is detected, SCORO is high	to external PAD
SBQERR	O	CRC check output	to MICOM
SBQDAT[7:0]	O	MICOM read data bus for subQ (10 Byte)	UCOMIF
SBQINT	O	subcode sync interrupt	

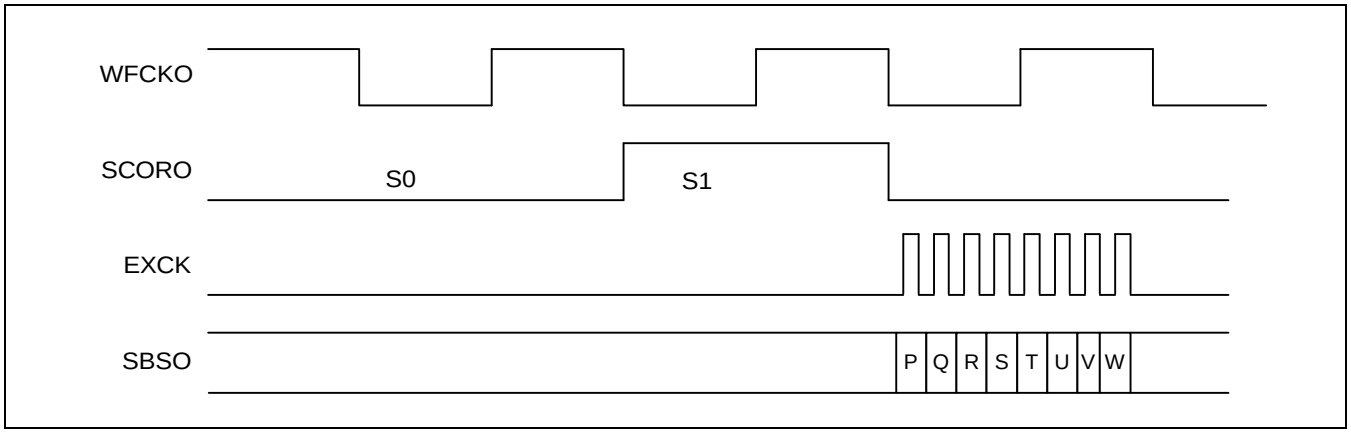
MICOM Register

— MICOM write register
. SBQIEN : subcode sync interrupt request enable

— Micom read register
. SUBINT : subcode sync interrupt
. SBQD[79:0] : SBQ data register

Address	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
73h(r)	CTL3	CTL2	CTL1	CTL0	ADR3	ADR2	ADR1	ADR0
74h(r)	TNO7	TNO6	TNO5	TNO4	TNO3	TNO2	TNO1	TNO0
75h(r)	INDEX7	INDEX6	INDEX5	INDEX4	INDEX3	INDEX2	INDEX1	INDEX0
76h(r)	MIN7	MIN6	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
77h(r)	SEC7	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
78h(r)	FRM7	FRM6	FRM5	FRM4	FRM3	FRM2	FRM1	FRM0
79h(r)	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO
7Ah(r)	AMIN7	AMIN6	AMIN5	AMIN4	AMIN3	AMIN2	AMIN1	AMIN0
7Bh(r)	ASEC7	ASEC6	ASEC5	ASEC4	ASEC3	ASEC2	ASEC1	ASEC0
7Ch(r)	AFRM7	AFRM6	AFRM5	AFRM4	AFRM3	AFRM2	AFRM1	AFRM0

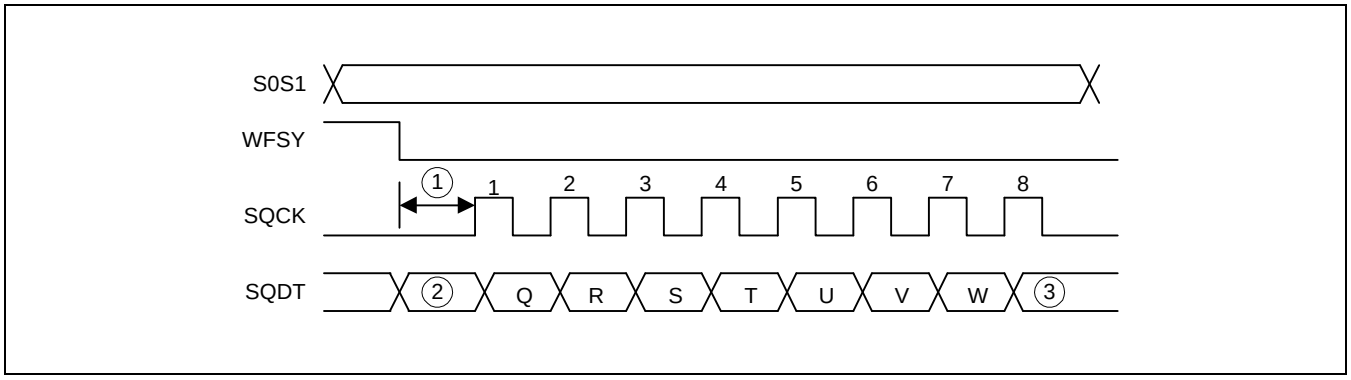
SUBCODE Output I/F (for CD-G)



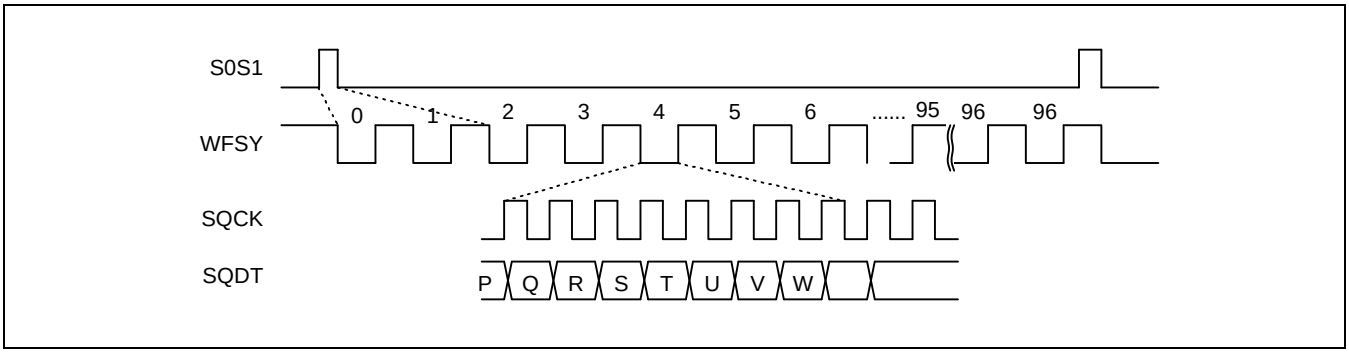
MICOM Register

— MICOM write register
. SBQIEN : subcode sync interrupt request enable

— Micom read register
. SUBINT : subcode sync interrupt
. SBQD[79:0] : SBQ data register



¨ç : After WFSY becomes falling edge, SQCK becomes 'L' for about 10µsec.
¨è : Subcode P is output if S0S1 is 'L', and subcode sync S0 and S1 are output if 'H'.
¨é : If pulses are input into the SQCK terminal over seven, subcode data (P,Q,R,S,T,U,V, W) are repeated.



- 1 SUBCODE SYNC = 98 EFM FRAMEs (1 EFM FRAME = 7.35 kHz, 1 SUBCODE SYNC = 75 Hz)
- 98 EFM FRAMEs = 2 Bytes for SUBCODE SYNC(S0, S1) + 96 Bytes for SUBCODE DATA
- 96 Bytes SUBCODE DATA = 1(P) Bit × 96 + 1(Q) Bit × 80 + 16 Bits(CRC for EDC) for CDP + 6 (R - W) Bits × 96 for CDG

CD AUDIO PROCESSOR (INTERPOLATION + 1-BIT DAC)

Block Description

— Interpolation : previous data hold + average

— Digital attenuation

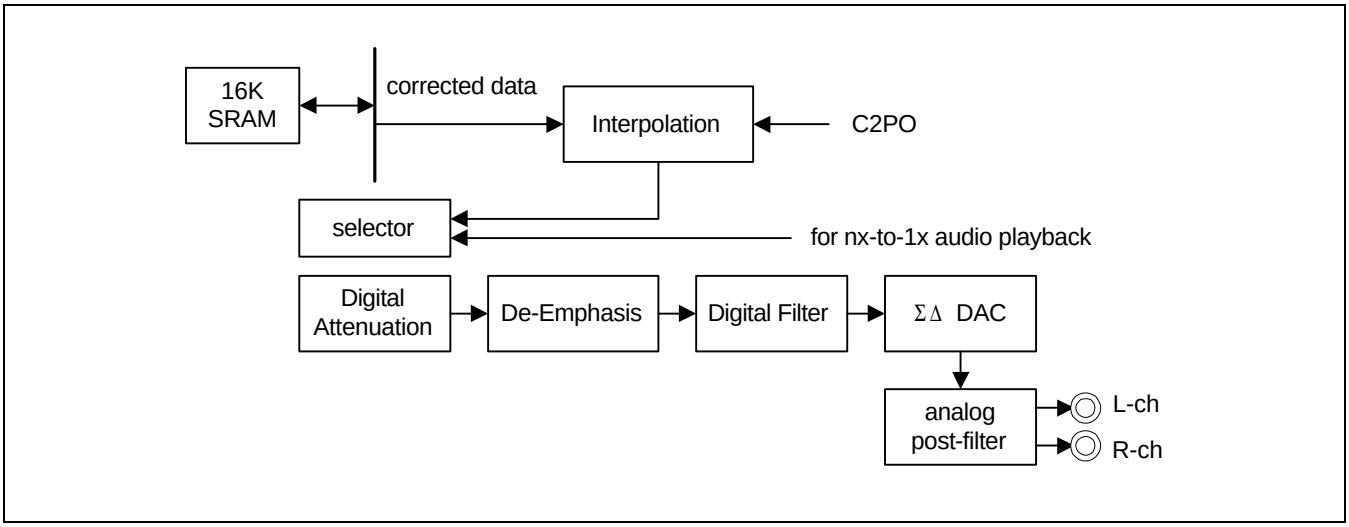
— De-emphasis

— 4Fs over sampling digital filter

— 16-bit Σ Δ digital-to-analog converter

— Analog post filter

Block Diagram



Detailed Function Description

— Double speed operation of internal DAC output

— Digital attenuation is a volume control of 64 levels with mute.

— Digital filter performs 4X interpolation. Its output data rate is 4Fs for normal speed mode and 8Fs for double speed operation.

— Digital sigma-delta modulator of bit-stream type has the MF (Multiple Feedback) topology, and it performs a noise-shaping function. The modulator shapes the quantization noise by suppressing its in-band component and pushes the noise energy outside of the band-of-interest without deteriorating the audio input signal.

— The analog postfilter is comprised of the SC-postfilter and anti-imaging filter. The SC-postfilter removes the quantization noise shaped to out-of-band by the digital Σ Δ modulator. This Analog filter has good clock jitter characteristics and a very linear characteristic.

I/O pins

1-bit DAC block (from digital attenuator - analog audio)

Symbol	I/O	Description	comment for one-chip
MSCK	I	Master Clock Input (384Fs for 1X/2X playback)	from clock generation
MCK	I	MICOM Command Clock Input	MICOM interface for digital attenuation
MDATA	I	MICOM Command Data Input	
MLD	I	MICOM Command Load Input (When Low, load)	
DN	I	High is Double (2Fs) Mode, Low is Normal(1Fs) Mode.	from MICOM reg.
DEEM	I	De-Emphasis On/Off. "H" is enabled. "L" is disabled.	from subcode or MICOM reg. (or external input PAD)
LRCK	I	Sample Rate Clock Input	from interpolation or ATAPI controller (or external input PAD)
BCK	I	Bit Clock Input	
SDATA	I	Serial Digital Input Data	
BIST_MODE	I	Bist On/Off Select. "H" is Bist On, "L" is DF Test On	test mode selection
Tsel	I	I/O direct selection for Test Pins (1bitIOL, 1bitIOR) "H" is Input, "L" is Output	test mode selection
1bitIOL	I/O	1-bit Input for Analog Postfilter of L-CH (Tsel = H) 1-bit Output for Digital Sigma-Delta Modulator (Tsel = L)	PAD for test
1bitIOR	I/O	1-bit Input for Analog Postfilter of R-CH (Tsel = H) 1-bit Output for Digital sigma-delta Modulator (Tsel = L)	PAD for test
FS64	I/O	64×Sampling Clock Input for test, Enabled if Tsel = H. 64Fs Clock Output if Tsel=L	PAD for test
Vref	I/O	Reference Voltage Output for Bypass	required PAD
Iref	I/O	Test Pin for Analog Supply Current	PAD for test
AoutR	O	Analog Output for R-CH	required PAD
AoutL	O	Analog Output for L-CH	required PAD
ERROR	O	Test Pin for Embeded memory BIST(BIST_MODE="H") or DF test(BIST_MODE="L") Ouput pin	PAD for test
DONE	O	Test pin for embeded memory BIST(BIST_MODE="H") or DF test(BIST_MODE="L") output pin	PAD for test
VBB	G	Analog Ground	Analog Power PAD for post analog-filter
VSSA	G	Analog Ground	
VDDA	P	Analog Power Supply	

Audio Interface

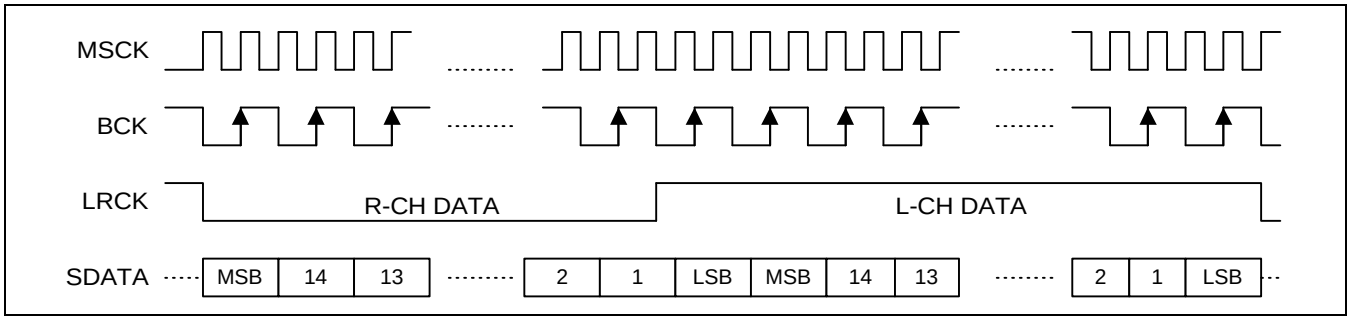
Symbol	I/O	Description	comment for one-chip
C2PO	O	C2 error pointer	for externel interface output PAD
LRCKO	O	Sample Rate Clock Input	from interpolation or ATAPI controller (or external PAD)
BCKO	O	Bit Clock Input	
SDATAO	O	Serial Digital Input Data	

MICOM Register

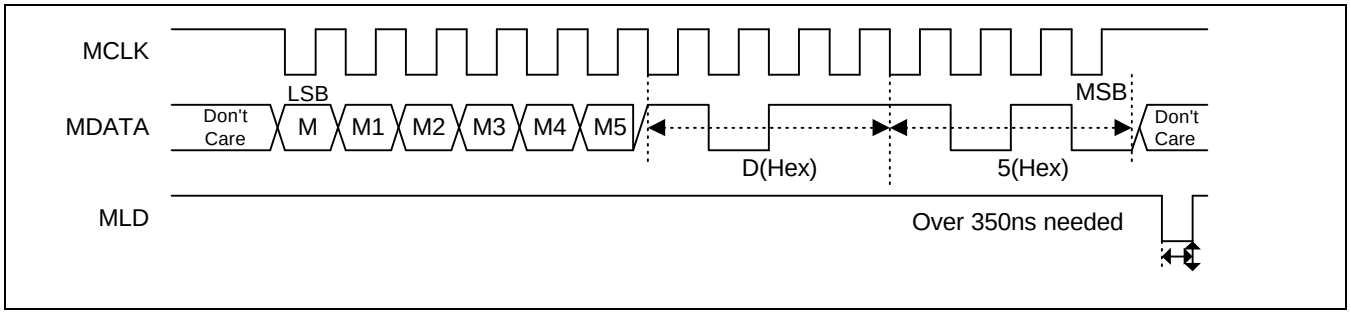
— MICOM Write Register
. DN : normal/double speed mode for 1-bit DAC
. DEEM : De-Emphasis enable
. Digital attenuation level : specific MICOM interface timing format

Timing Chart

— Audio data input
. for normal speed : MSCK = 384Fs, BCK = 32Fs, LRCK = 1Fs
. for double speed : MSCK = 384Fs, BCK = 64Fs, LRCK = 2Fs



— MICOM Interface



— The Interface shown above is that of the DAC core. Design configuration outside the DAC core must take this format into consideration.

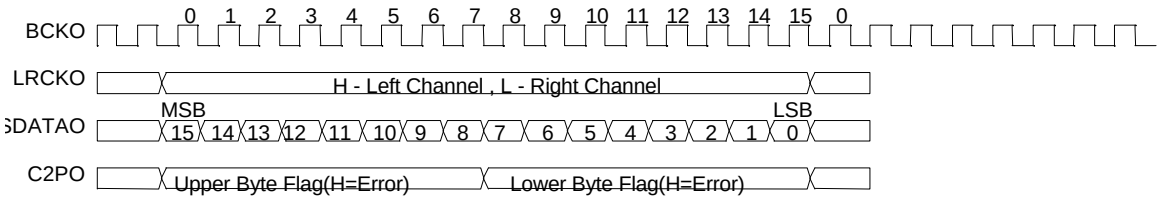
Out of the interface formats shown below, the CD-DSP output timing supports the "Toshiba DSP Interface format" and"Sony-24-Clock DSP interface format-1" , andthe S5L9250B's built-in DAC input timing for nx-to-1x supports the"EIAJ (16-bit) Audio Data Interface format"and "Philips 12S (16-bit) audio data interface format" .

CD-ROM, V-CD OUTPUT INTERFACE FORMAT (TO CD-ROM DECODER)

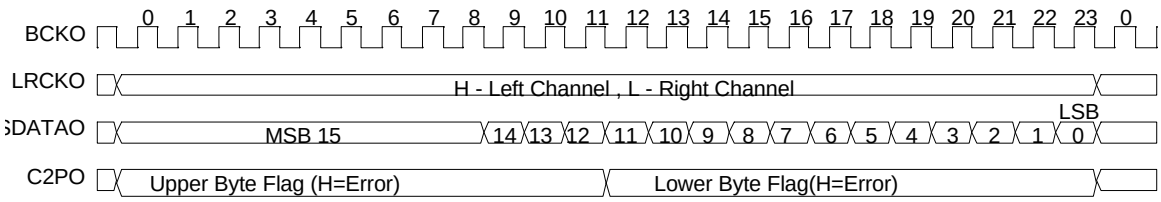
¾ Toshiba 16-Clock DSP Interface Format

1) CD-ROM, V-CD OUTPUT Interface Format (to CD-ROM DECODER)

- Toshiba 16-Clock DSP Interface Format

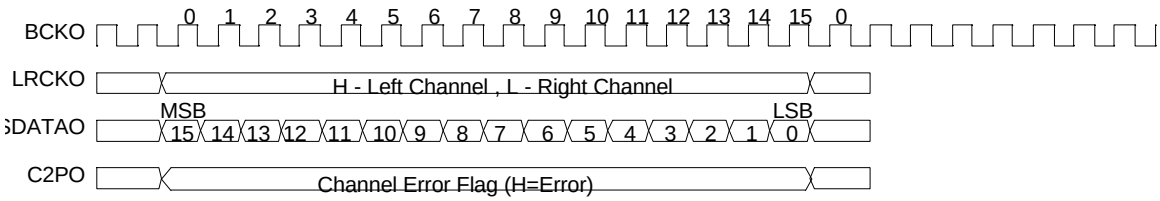


- Sony 24-Clock DSP Interface Format-1

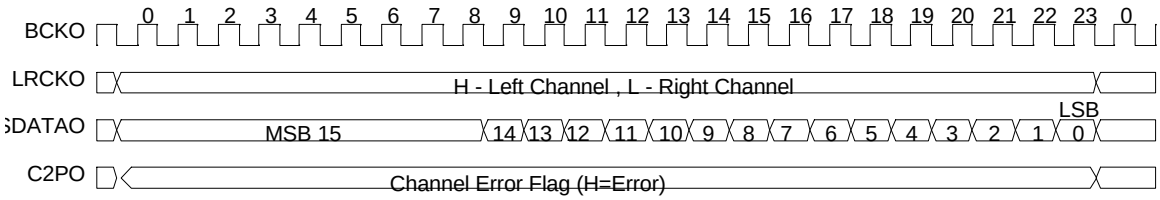


2) CD-AUDIO OUTPUT Interface Format (to CD-ROM DECODER)

- Toshiba 16-Clock DSP Interface Format



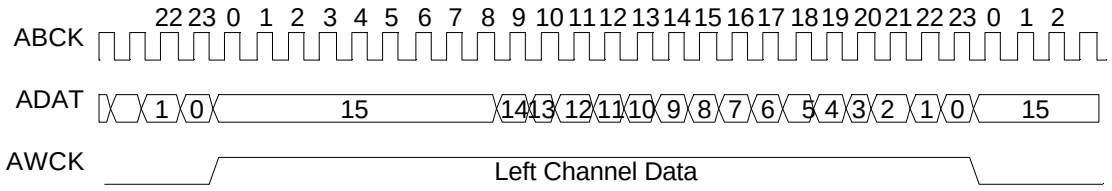
- Sony 24-Clock DSP Interface Format-1



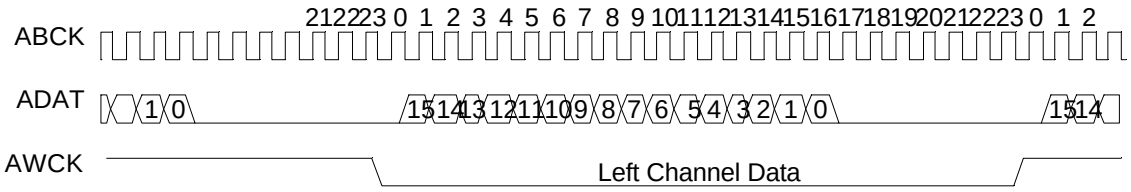
SAMSUNG ELECTRONICS

3) CD Audio Interface Format for 1-bit DAC (from CD-ROM DECODER)

- EIAJ (16-bit) Audio Data Interface Format

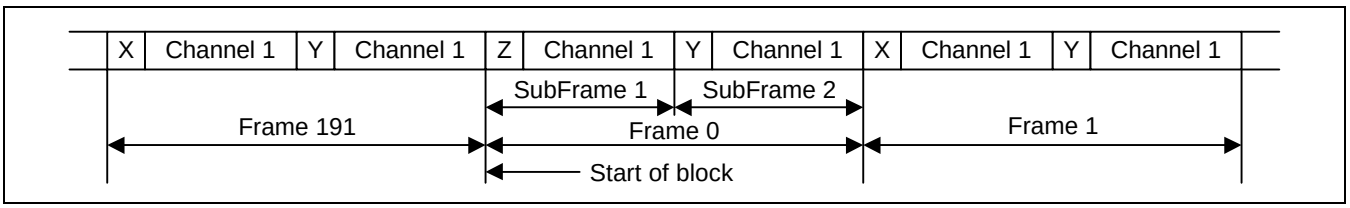


- Philips I2S (16-bit) Audio Data Interface Format



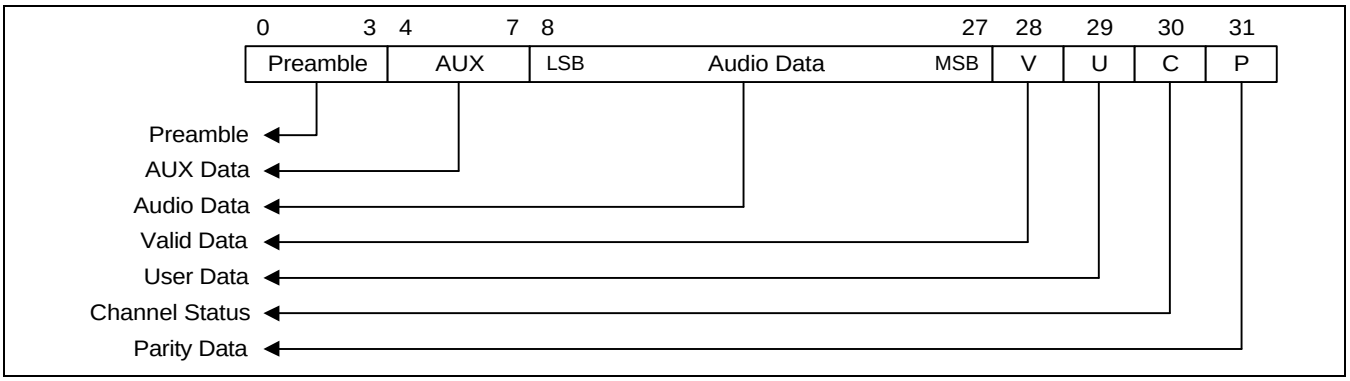
Block Description

The goal of the Digital audio interface block is to transmit the data in the CD disc serially into the surrounding systems. This interface method has the advantage of needing only one pin for transmission. In other words, there are no additional pins needed such as separate clocks. Because of this advantage, it is utilized not only in audio systems for home use, but also for professional use.



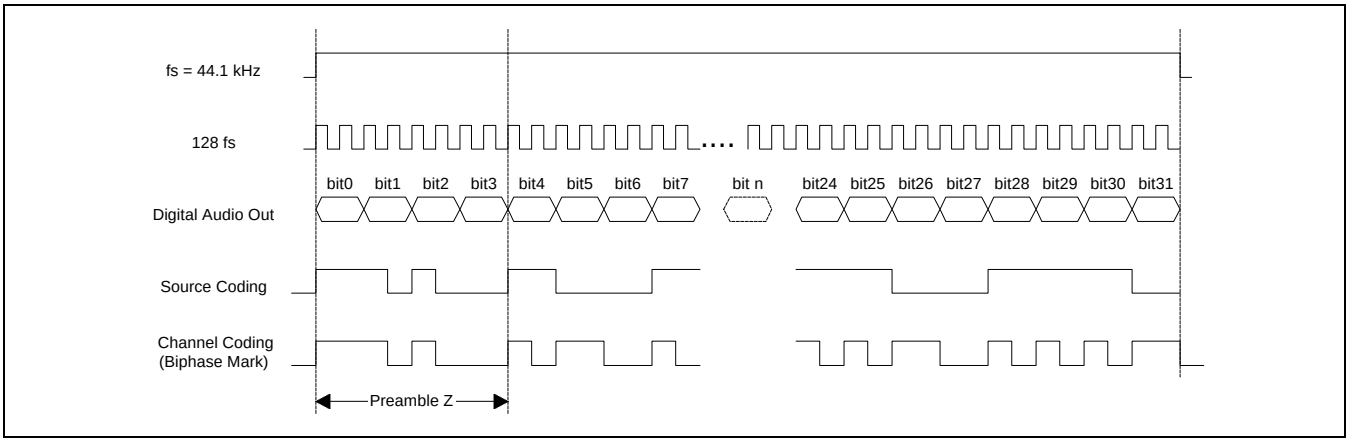
SPDIF (Sony-Philiiips Digital audio Interface)

This interface is called SPDIF because Sony and Philips came up with the Digital audio interface method for CDs, and its regulations are registered in the AES (Audio Engineering Society). SPDIF serially transmits data and is sensitive to background noise. To overcome this disadvantage, the digital out data is transmitted after being demodulated into biphase form. Phase0 is given a different value from the previous data's phase1 value. If the source data is '0', phase1 is given the same value as phase0, and if it is '1', phase1 is given a different value from phase0.



Structure of Format

Each subframe is configured of 32 time slots, and a subframe includes audio data. 2 subframes make 1 frame, which as Left, Right stereo signal components. 192 frames make 1 block, which is the control bit information unit.



Subframe Format

Preamble (4 bit) : The Preamble has the sync data of each subframe and block, and preamble data is not converted into biphase signal to maintain the sync data's uniqueness. However, it starts with the opposite value of the previous symbol's phase1 value. The Preamble needs three patterns to tell apart left, right, and the beginning of a block, which are shown below.

Preceding state	0	1	
	Channel Coding		
"X"	11100010	00011101	Subframe 1
"Y"	11100100	00011011	Subframe 2
"Z"	11101000	00010111	Subframe 1 and block start

Preamble 'X' is channel 1's sync., and preamble 'Y' is channel 2's sync. Preamble 'Z' is used to show the block's start sync. The reason why there are two sync patterns for each preamble is because the value is reversed according to the phase of the previous data.
2) AUX (4 bits) : auxiliary data area.
3) Audio Data (20 bits) : Although the resolution of the audio data transmitted to Digital out for CDs is 16 bits, it can be 20 or 24 bits by augmenting the audio data area to the AUX area. This are is LSB first.
4) Validity Bit (1 bit) : If Studio sample word can be converted into analog audio signal, validity bit is set to '1'. If not, it is set to'0'. In the case of CDs, it is set to'0'.
5) User data (1 bit) : CDs use this area to transmit subcode data.
6) Control Status Data (1 bit) : Data is input by each subframe, and 192 subframes make one Control status data. There are the consumer mode and professional mode in this area, and the 4th generation CDP supports consumer mode. For CDs, control status data has the following meaning.

Bit	Description
0	0 : Consumer use, 1 : Professional use
1	0 : Normal Audio, 1 : Nonaudio Mode
2	0 : Copy Prohibit, 1 : Copy Permit
3	0 : No Preemphasis, 1 : Preemphasis
4	Reserved (= 0)
5	0 : 2 channel, 1 : 4 channel
6 - 7	00 : mode 0, reserved
8 - 15	10000000 : 2 channel CD player User bit channel = CD Subcode bit optional
16 - 19	Source number (= 0000)
20 - 23	Channel number (= 0000)
24 - 27	Sampling frequency : 44.1kHz = 0000
28 - 29	Clock accuracy 00 : Normal accuracy, 10 : High accuracy, 01 : Variable speed
30 - 191	Don't care (all zero)

BLOCK I/O

Name	I/O	To/From	Contents
i_rstb	I	CLKGEN	SPDIF Block Reset Signal
i_LRClk	I	CLKGEN	LR Channel Clock = fs
clk128fs	I	CLKGEN	Data Transfer Clock = 128 fs
i_DIGOUTEN	I	MICOM	Digital audio out block enable signal
i_EMPH	I	SUBCODE	emphasis on/off
i_CpyRgt	I	SUBCODE	1 : Copy Permit, 0 : Copy Protect
i_AudData	I	ITP	16 bits Audio Data
i_SubData	I	SUBCODE	8 bits Subcode Data
o_DigAudOut	O	PAD	Digital Audio serial output

— This block can be used in both Nx Audio Buffering Mode (CAV Mode) and KS9245's AUDIO Bypass Mode.
: However, in KS9245's AUDIO Bypass Mode, D/Audio Out signal must be input from outside the CD-ROM Decoder. (So if you don't use Audio Buffering Mode, you must use the D/audio Out Block of the CD-DSP. In that case, features such as stereo, mono, and swap provided by the D/AUD block are not provided, and is output in stereo only mode.) :CAV Mode.

MICOM I/F

CHARACTERISTICS

- MICOM I/F Mode

  1) Intel Mode (8051) : Direct Access Register Mode support.

  2) Motorola Mode (68HC11) : Direct Access Register Mode support.

  → Address is latched at ALE's falling edge.

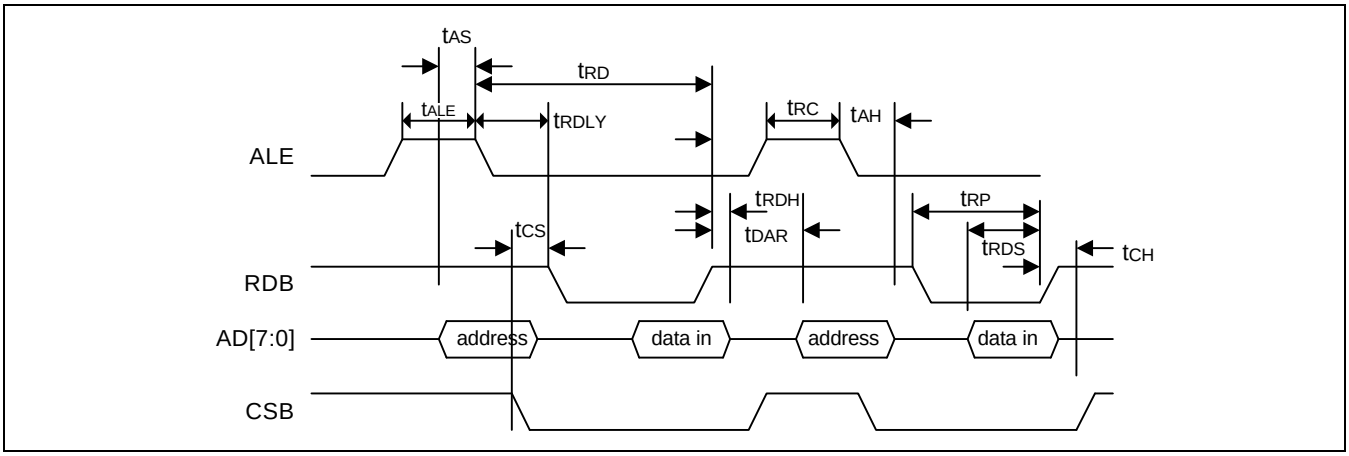
  → Apart from the basic MICOM I/F signal, you can set the Intel, Motorola, and indirect Mode by setting TEST1, TEST2, TEST3 and TEST4 PIN
  : Please refer to P163.

  3) Indirect Access Register Mode support.

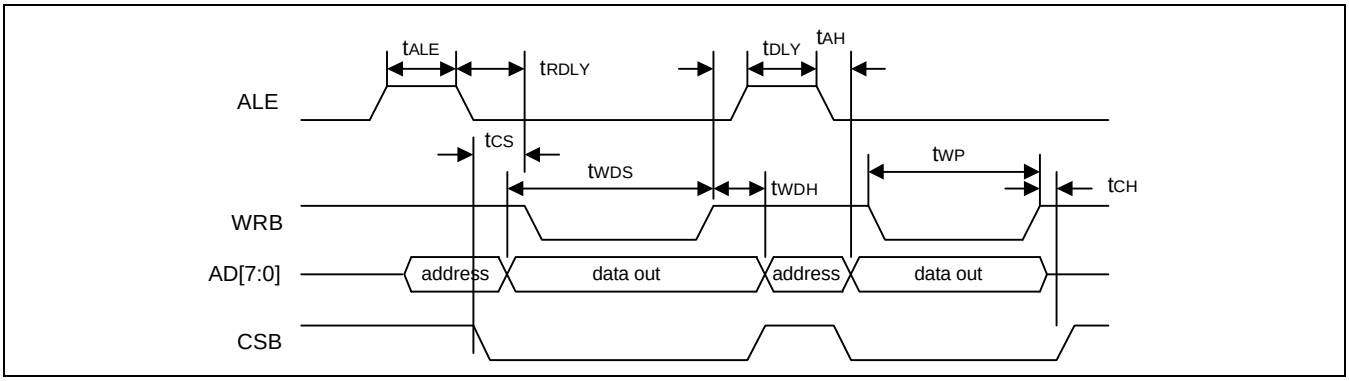
MICROPROCESSOR INTERFACE

Multiplexed Intel Mode Register Read/Write Timing

Microcontroller Read Cycle

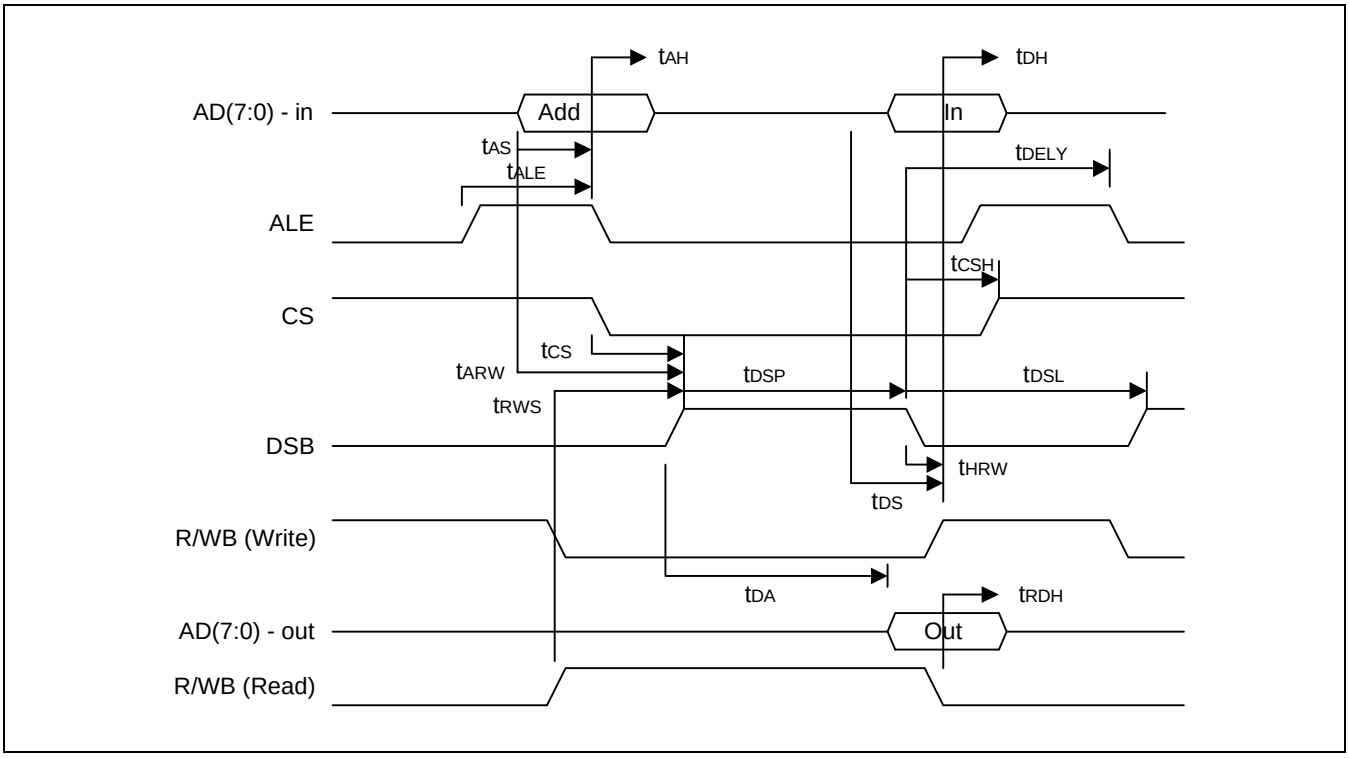


Microcontroller Write Cycle



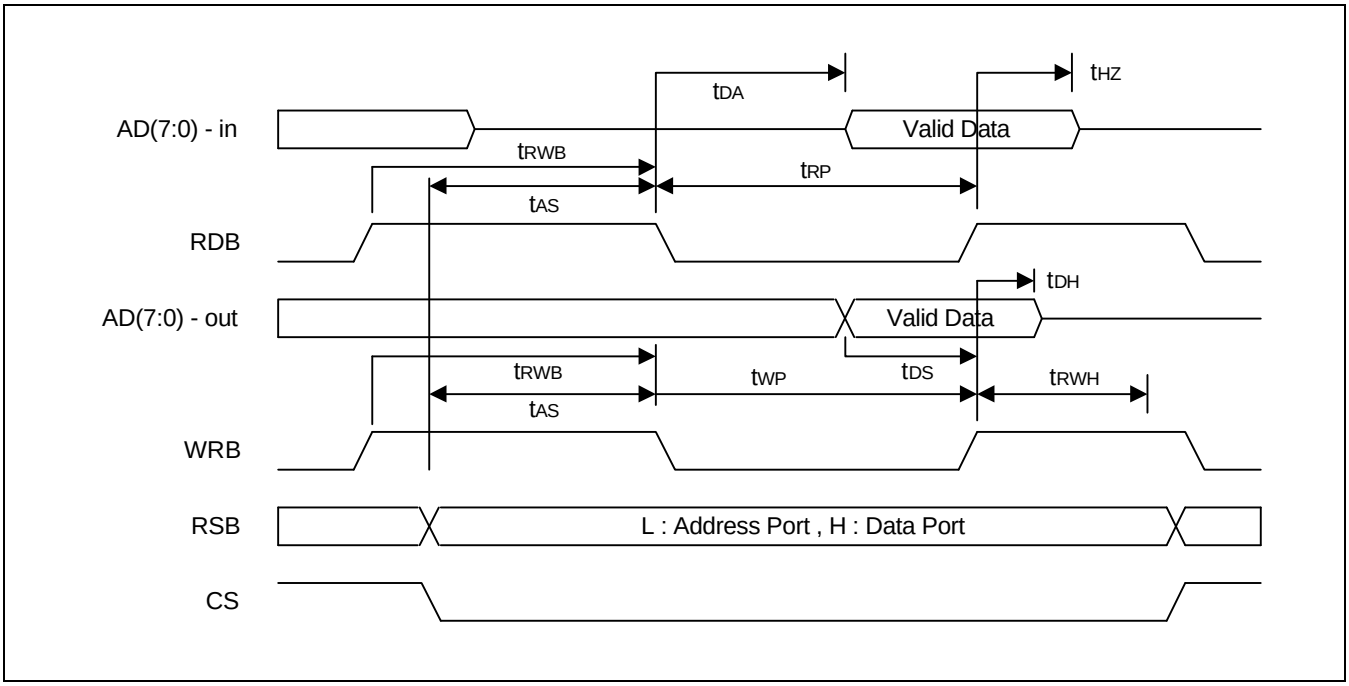
Parameter	Symbol	Min.	Max.	Unit
ALE Pulse Width	tALE	1 Sysclk		ns
Address Setup Time	tAS	10		
Address Hold Time	tAH	5		ns
Chip Select Setup for Read/Write Command	tCS	10		ns
Chip Select Hold for Read/Write Command	tCH	0		ns
ALE Active from Read/Write Rising Edge Delay	tDLY	0		ns
Write Pulse Width	tWP	2 Sysclk		ns
Read Pulse Width	tRP	3 Sysclk		ns
Data Pulse to next Address Valid	tDAR	10		ns
Data setup Time for Write	tWDS	10		ns
Data Hold Time for Write	tWDH	10		ns
ALE Falling to RDB/WRB Falling	tRDLY	15		ns
Read Data Setup Time	tRDS	1 Sysclk		ns
Read Data Hold Time	tRDH	0		ns

Multiplexed Motorola Mode Register Read/Write Timing



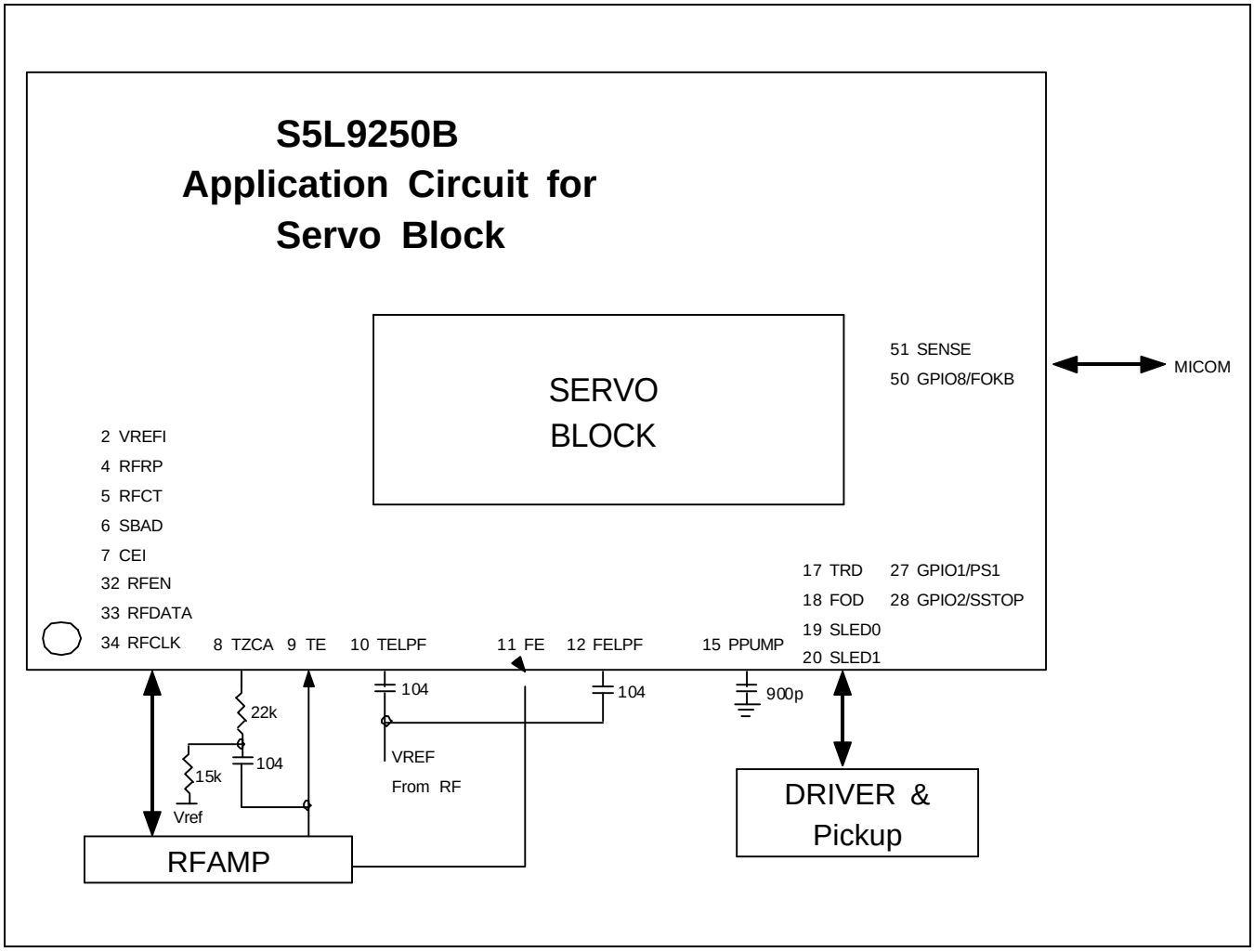
Parameter	Symbol	Min.	Max.	Unit
ALE Pulse Width	tALE	1 Sysclk		ns
Address Setup Time	tAS	10		ns
Address Hold Time	tAH	10		ns
Address Valid Before Read/Write Command	tARW	15		ns
Chip Select setup for Read/Write	tCS	10		ns
Chip Select Hold for Read/Write	tCH	0		ns
R/WB Setup Width DS	tRWS	5		ns
R/WB Hold Width DS	tHRW	5		ns
DSB Pulse Width	tDSP	3 Sysclk		ns
DSB Recover Time	tDSL	1 Sysclk		ns
Data Setup Time for Write	tDS	10		ns
Data Hold Time for Write	tDH	10		ns
Read Access Time	tDA	1 Sysclk	2 Sysclk	ns
DSB to ALE Falling Edge Delay	tDELY	1.5 Sysclk		ns
Read Data Hold Time	tRDH	0		

Indirect Access Register Mode Read/Write Timing

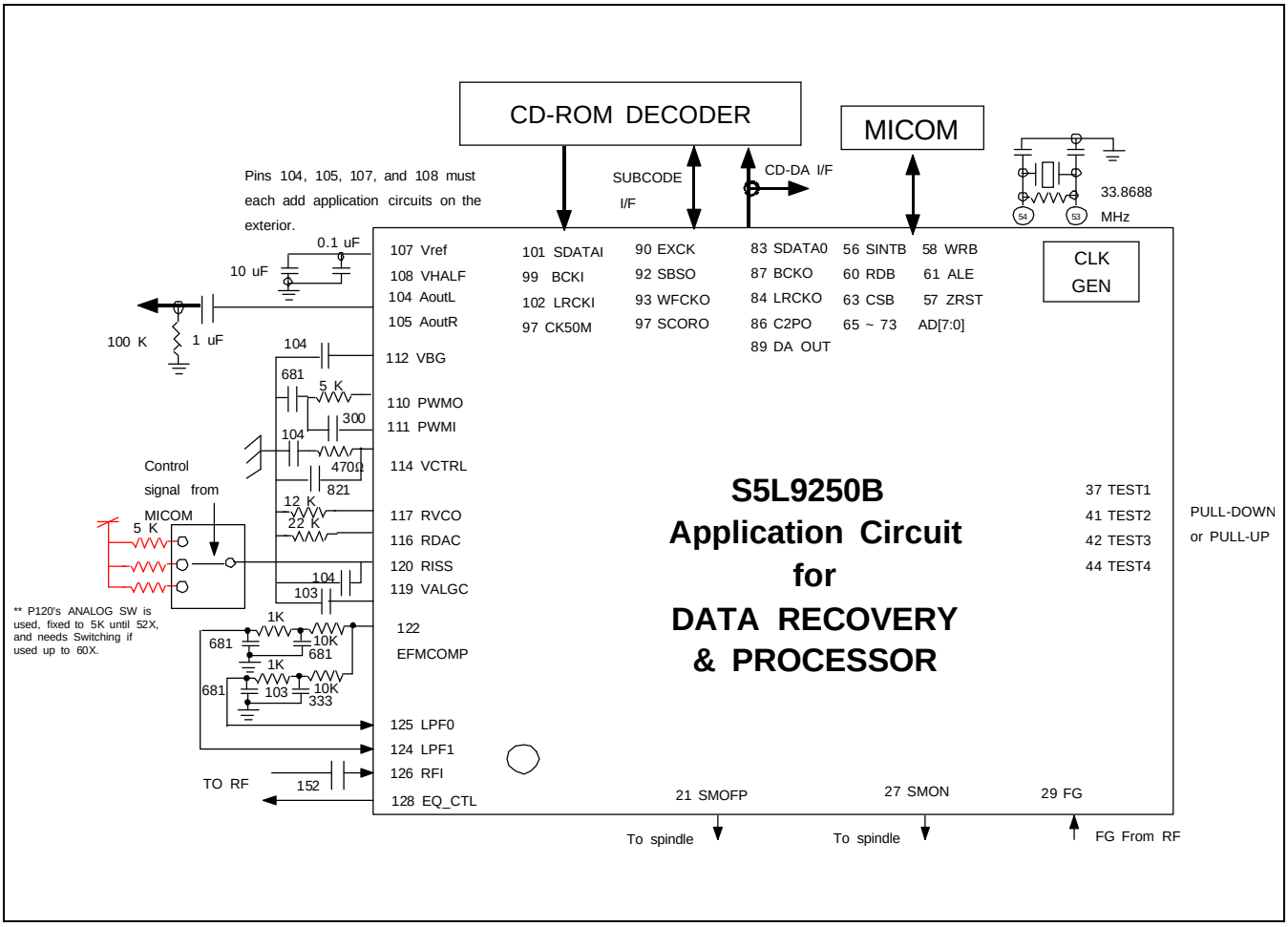


Parameter	Symbol	Min.	Max.	Unit
WRB Recover Time to next RDB or WRB	tRWB	2 Sysclk		ns
CS or RSB Setup for Read/Write	tAS	10		ns
WRB Pulse Width	tWP	40		ns
RDB Pulse Width	tRP	40		ns
CS or RSB Hold Time	tRWH	6		ns
Data Setup Time for Write	tDS	10		ns
Data Hold Time for Write	tDH	10		ns
Read Access Time	tDA	10	20	ns
Read Data Hold Time	tHZ	0		ns

APPLICATION CIRCUIT (1)



APPLICATION CIRCUIT (2)



¥¹¥°. MONITER MODE

S5L9250B Monitor Mode Setting Conditions (Normal Operation)

* Mmode : Monitor Mode Selection Register

Address	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
4Eh	MDSP3	MDSP2	-	-	MSERVO3	-	-	-
Reset value	0	0	-	-	0	-	-	-

* Please refer to ¥¹¥±. TEST MODE for normal operation conditions.

(Normal Operation Conditions) & (4Eh MICOM Data Setting Value)

PAD NAME	MDSP[3:0]= "1000"	MDSP[3:0]= "0100"	MDSP1 ="0010"	MDSP0 ="0001"	MSERVO3 = "1000"	MSERVO2 ="0100"	MSERVO1 = "0010"	MSERVO0 = "0001"
TZCO	EccGnt	frsy						
MIRR	EfmGnt	p_wfref	-	-		-	-	-
PHOLD	EccWrReq	p_xfref						
COUT	ItpGnt	Jitter						
LOCK	EccRdReq	WfCntEnb						
GFS	EfmReq	RfCntEnb						
C2PO	EndOfTrx	dfrsy			KICK			
PLCK	ItpReq	JitterCntEnb			DFCTO			

¥¹¥±. TEST MODE

1.1 BI9250X Test Mode Setting Conditions : Scan Enable Signal(PAD75)

Pin No.	Pin Name	Normal Intel	Normal Motorola	Normal Indir	Nand _Tree	soak_test	glue _intel	glue_ motorola	glue_indir	BIST MODE	SCAN_ MODE	block_intel	block_motorola	block_indir	srom_test	sdac_test
P37	TEST1	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H
P41	TEST2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H
P42	TEST3	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H
P44	TEST4	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L

1.2 S5L9250B Block Test Mode Setting Characteristics

BI9250X can be operated in various modes b adjusting the values of P37, P41, P42, P44, theTEST1, TEST2, TEST3, TEST4. NORMAL INTEL, NORMAL MOTOROLA, and NORMAL INDIRECT MODE are modes used in normal operation, which makes the MICOM I/F operate in INTEL MODE, MOTOROLA MODE, or INDIRECT MODE. The remaining 6 modes are TEST modes, including NAND TREE TEST, OAK CORE TEST, SERVO ROM TEST, ECC SRAM TEST (BIST), SCAN TEST MODE, BLOCK TEST MODE. You need to set the 4 test pins according to the mode you want. Of the test modes above, Glue Test and block_test adjust TEST1, 2, 3, and 4 for respective use as Intel, Motorola, and Indirect mode.