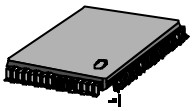
INTRODUCTION

64-LQFP-1010



S5L9276 is a single chip ISO/IEC 11172-3 Layer III audio decoder, capable of decoding compressed elementary bit stream as specified in ISO/IEC standard. As a decoder for the DISC-MAN, it can provide you more small and cheaper solution for MP3 player application.
S5L9276 is low voltage IC that can read MP3 and CD-ROM format discs and can be applied to various products.

FEATURES

- Includes CD-ROM decoder with ECC and EDC
- ISO/IEC 11172-3 L1/L2/L3 Decoding.
- ISO/IEC 13818-3 L1/L2/L3 Decoding
- Supports All MPEG Bit Rates including free format for ISO/IEC 11172-3.
- Supports All MPEG Bit Rates except 8kbps and free format for ISO/IEC 13818-3.
- Supports 32/44.1/48kHz Spl for ISO/IEC 11172-3. (For variable bit rate, support only 44.1kHz sampling rate.)
- Supports 32/44.1/48kHz and 16/22.05/24 kHz for ISO/IEC 13818-3.
  (For variable bit rate, support only 44.1KHz & 22.05kHz sampling rate.)
- Single/ Dual/ Stereo// Joint Stereo
- Supports Any Combination of Intensity Stereo & MS Stereo
- Serial Host Interface
- Supports Off-chip DAC
- Anti Shock Memory Controller
- Supports 16Mbit EDO/FP DRAM
- Use of Standard Crystal 16.9344MHz
- 16.9344MHz Clock Output Port
- Power Save Mode : POWER-DOWN, SLEEP, POWER_SAVE
- Pause and Replay
- Fast Forward
- Fast Backward (Rewind)
- Back Skip
- Forward Skip
- CDFS(CD-ROM File System) Decoding (ISO9660, Joliet, and Romeo Format)
- Low Power Dissipation : 65mA @3.0 volts

ORDERING INFORMATION

Device	Package	Supply Voltage	Operating Temperature
S5L9276X01	64-LQFP-1010	2.7V — 3.3V	-20°C — +75°C

FUNCTIONAL BLOCK DIAGRAM

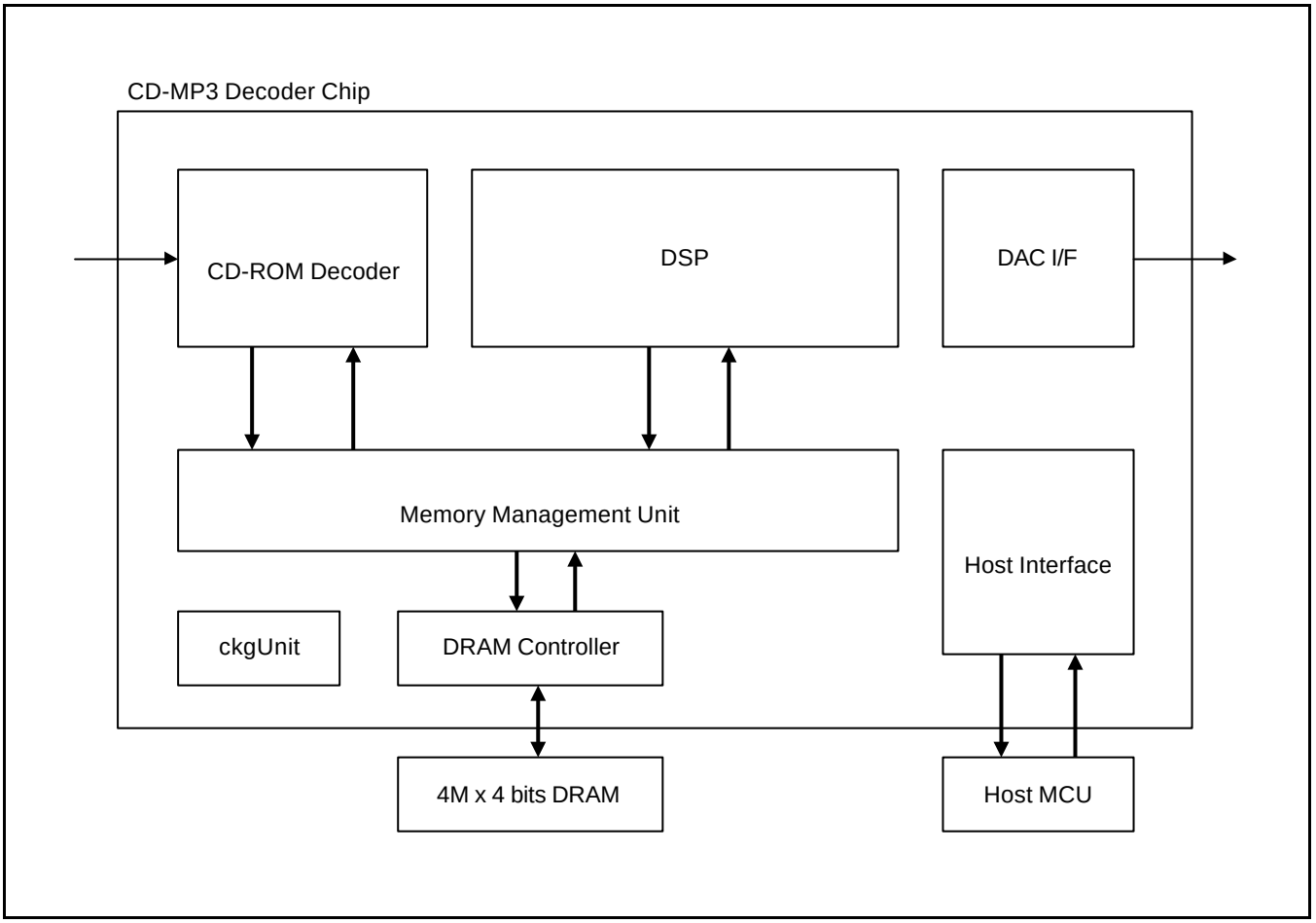
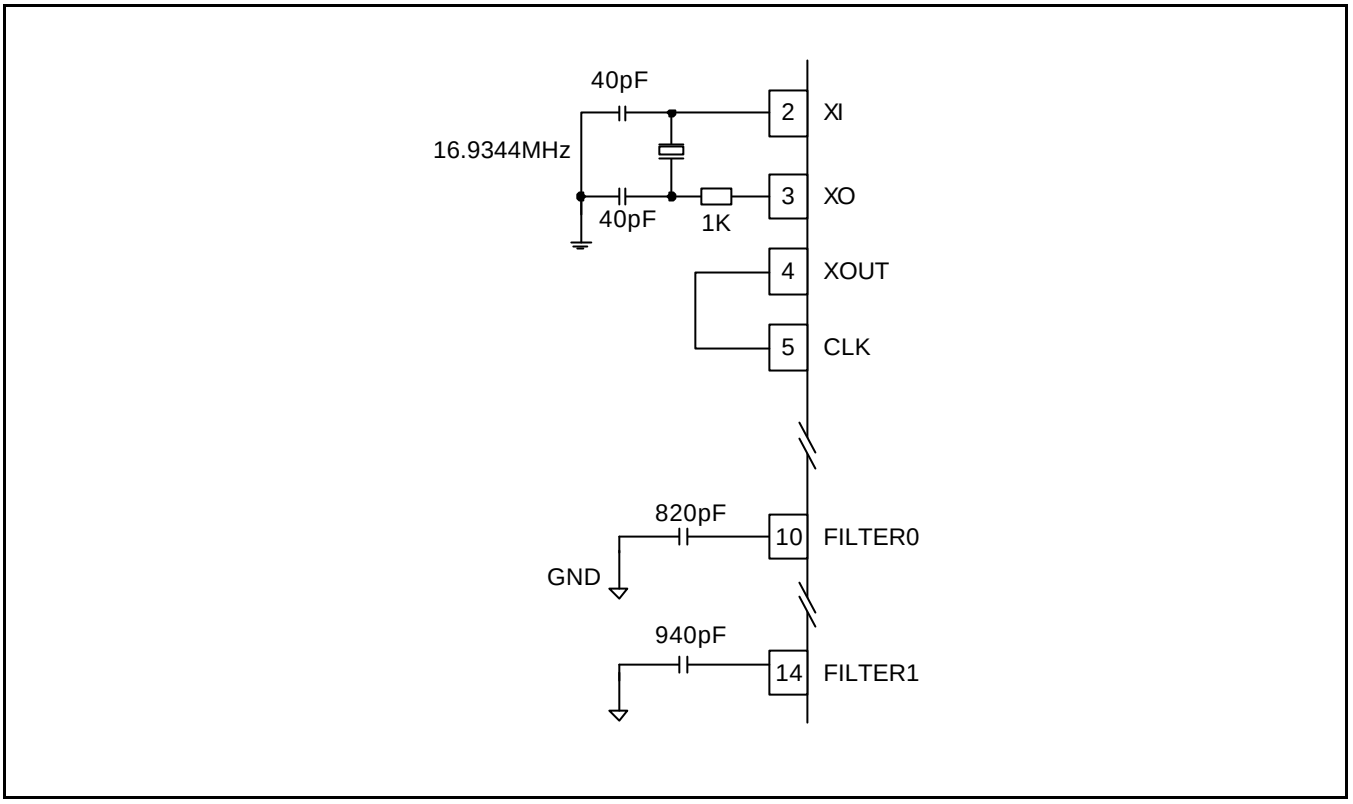
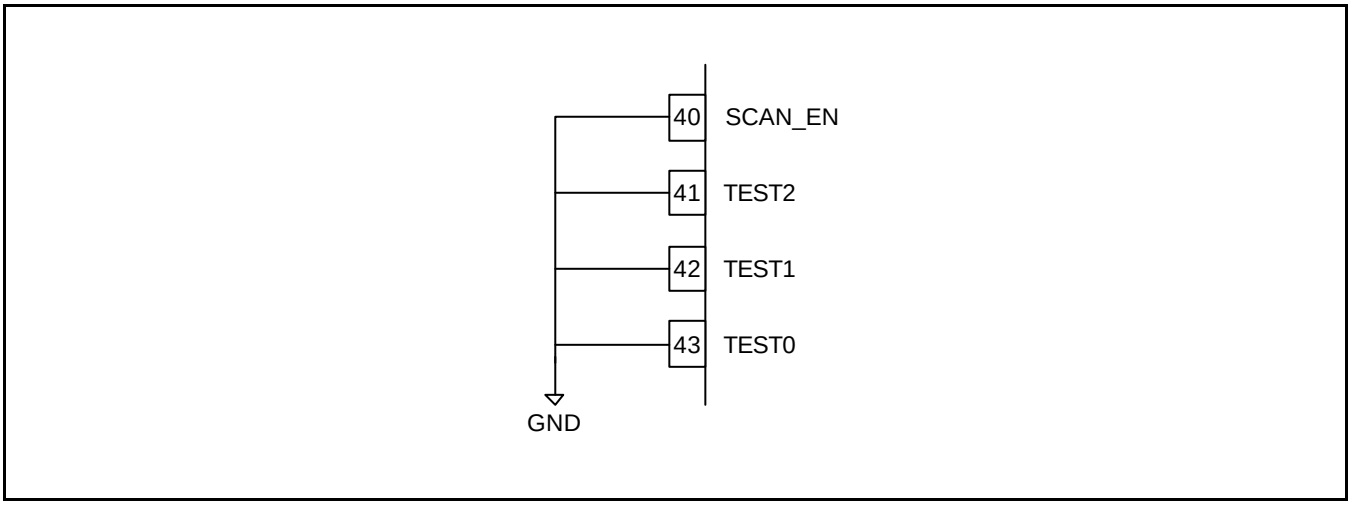


Figure 1. Functional Block Diagram of S5L9276

APPLICATION DIAGRAM



Test Pin Connection



DRAM Connection

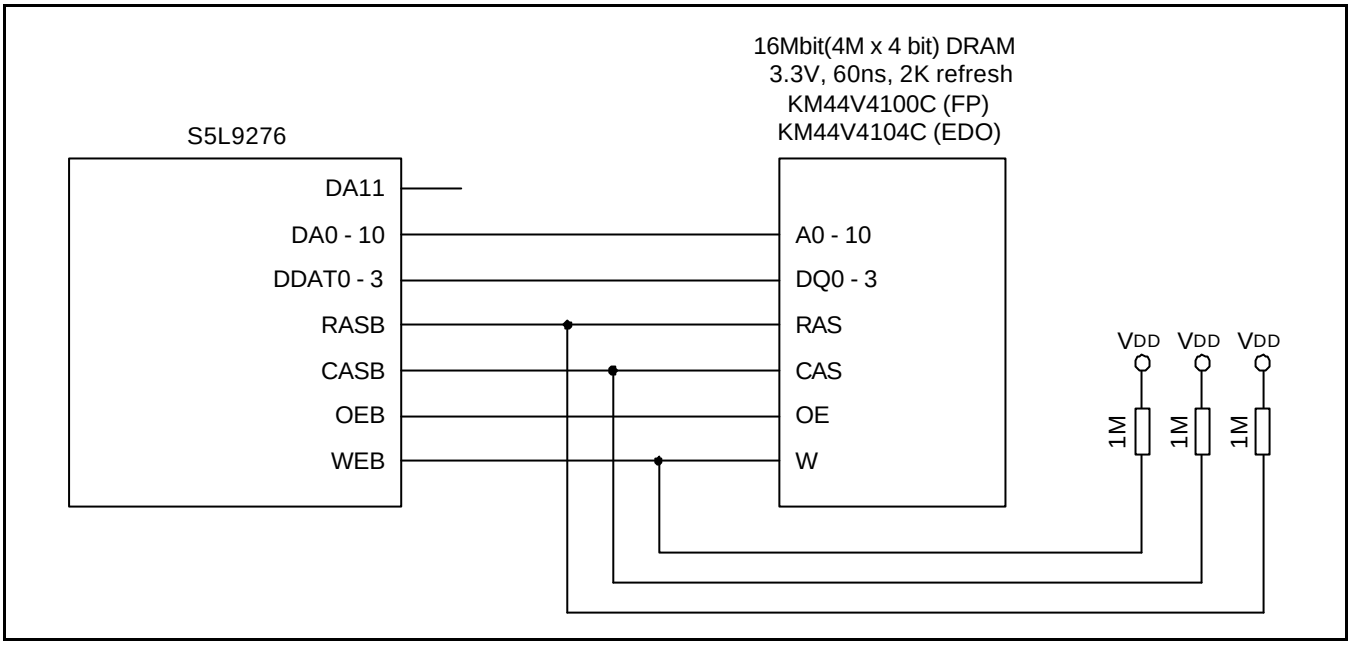


Figure 2. Interface with 4Mx4bit DRAM Type A (2K ref. Product)

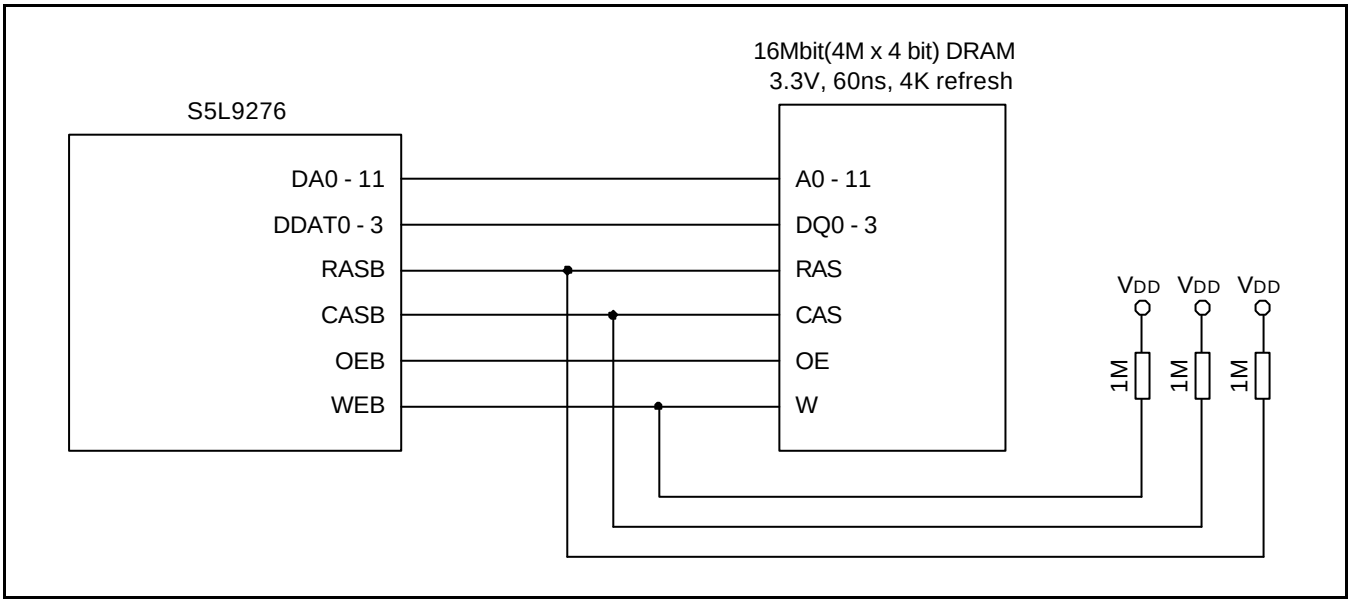


Figure 3. Interface with 4Mx4bit DRAM Type B (4K ref. Product)

ETC

SP_SEL (pin15) = GND
AD1(pin34) = OPEN
AD2(pin29) = OPEN
AD3(pin28) = OPEN
DAII(pin30) = GND

PIN CONFIGURATION

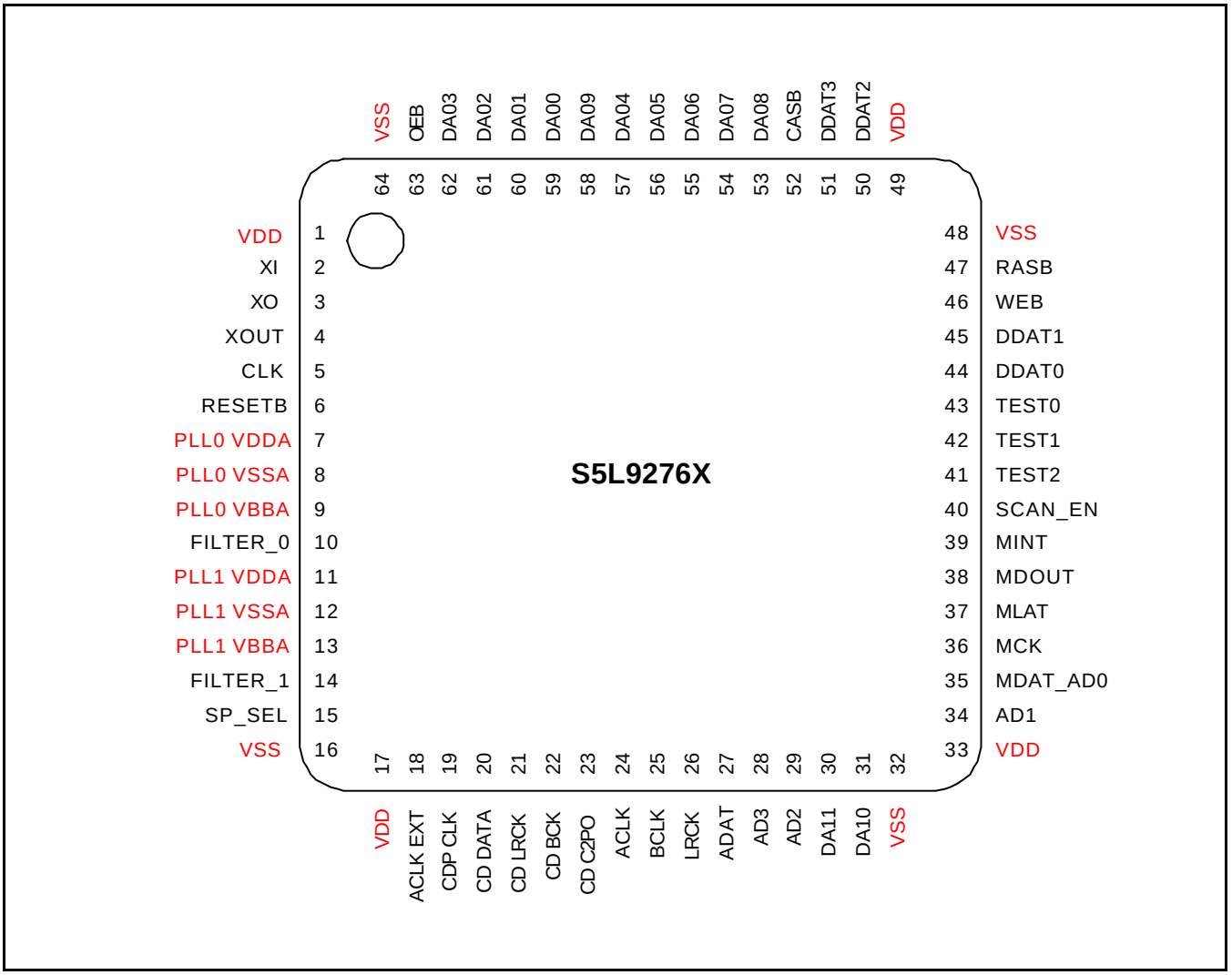


Figure 4. 64 pin Low profile Quad Flat Package (LQFP)

PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	VDD	P	Digital Power
2	XI	I	X'tal Oscillator input(16.9344MHz)
3	XO	O	X'tal Oscillator output
4	XOUT	O	Buffered Output of XO
5	CLK	I	System Clock input
6	RESETB	I	System Reset Active LOW
7	PLL0 VDDA	P	Analog Power for PLL0
8	PLL0 VSSA	G	Analog Ground for PLL0
9	PLL0 VBBA	G	Analog Ground for PLL0
10	FILTER_0	O	External Capacitor port for PLL0
11	PLL1 VDDA	P	Analog Power for PLL1
12	PLL1 VSSA	G	Analog Ground for PLL1
13	PLL1 VBBA	G	Analog Ground for PLL1
14	FILTER_1	O	External Capacitor port for PLL0
15	SP_SEL	I	Tied to GROUND.
16	VSS	G	Digital Ground
17	VDD	P	Digital Power
18	ACLK EXT	I	External Audio Clock source
19	CD CLK	O	Clock Output for CD DSP IC
20	CD DATA	I	Data from CD DSP IC
21	CD LRCK	I	LRCK from CD DSP IC
22	CD BCK	I	BCK from CD DSP IC
23	CD C2PO	I	C2PO from CD DSP IC
24	ACLK	O	Audio clock to DAC clock input
25	BCLK	O	BCLK to DAC
26	LRCK	O	LRCK to DAC
27	ADAT	O	Data to DAC
28	AD3	I/O	Open (Not Used)
29	AD2	I/O	Open (Not Used)
30	DA11	O	Address Output 11 for DRAM
31	DA10	O	Address Output 10 for DRAM
32	VSS	G	Digital Ground

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
33	VDD	P	Digital Power
34	AD1	I/O	Open (Not Used)
35	MDAT_AD0	I	Data input pin
36	MCK	I	Micom Clock pin
37	MLAT	I	Data Latch input pin
38	MDOUT	O	Data from CD-MP3 to MCU
39	MINT	O	Interrupt output to MCU
40	SCAN_EN	I	Scan Test enable
41	TEST2	I	Tied to GROUND.
42	TEST1	I	Tied to GROUND.
43	TEST0	I	Tied to GROUND.
44	DDAT0	B	Data0 BUS for External DRAM
45	DDAT1	B	Data1 BUS for External DRAM
46	WEB	O	Write Enable for External DRAM
47	RASB	O	Row Address for External DRAM
48	VSS	G	Digital Ground
49	VDD	P	Digital Power
50	DDAT2	B	Data2 BUS for External DRAM
51	DDAT3	B	Data3 BUS for External DRAM
52	CASB	O	Column Address for External DRAM
53	DA08	O	Address Output8 for DRAM
54	DA07	O	Address Output7 for DRAM
55	DA06	O	Address Output6 for DRAM
56	DA05	O	Address Output5 for DRAM
57	DA04	O	Address Output4 for DRAM
58	DA09	O	Address Output9 for DRAM
59	DA00	O	Address Output0 for DRAM
60	DA01	O	Address Output1 for DRAM
61	DA02	O	Address Output2 for DRAM
62	DA03	O	Address Output3 for DRAM
63	OEB	O	Output to make data output to " Hi-Z" at DRAM
64	VSS	G	Digital Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
power supply voltage	VDD	-0.3 — + 3.8		V
Input supply voltage	VI	3.3V I/O	-0.3 — VDD + 0.3	V
		5V-tolerant	-0.3 — 5.5	
Operating temperature	TOPR	-20 — 70		°C
Storage temperature	TSTG	-40 — 125		°C

ELECTRICAL CHARACTERISTICS

Pin Number	Function Description
Pin 10, Pin14	Analog Normal Output Pad with Resistor 50ohm and Separate Bulk Bias (poar50_bb)
Pin2:Pin3	Oscillator Cell with Enable and 1Mohm Resistor (psoscm26)
Pin4,Pin19,Pin39,Pin28,Pin29	LVCMOS Normal Output Buffer (pob2)
Pin6,Pin20,Pin21,Pin22,Pin23,Pin36,Pin37	5V-tolerant LVCMOS Level Input Buffer (ptic)
Pin5,Pin18,Pin40,in41,Pin42,Pin43	LVCMOS Schmitt Trigger Level Input Buffer (pic)
Pin28,Pin29,Pin34,Pin35,Pin44,Pin45,Pin50,Pin51	LVCMOS Tri-State Bi-Directional buffer with Pull-Up (pbcut1)
Pin24,Pin25,Pin26,Pin27,Pin30,Pin31,Pin38,Pin39,Pin 46,Pin47,Pin52,Pin53,Pin54,Pin55,Pin56,Pin57,Pin58, Pin59,Pin60,Pin61,Pin62,Pin63	Tri-State Output Buffer (pot2)

V_{DD}= 3.3 ± 0.3V, T_A = 0 to 70°C (In case of normal IO)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage (LVCMOS interface)		2.0			V
V_{IL}	Low level input voltage (LVCMOS interface)				0.6	V
VT	Switching threshold	LVCMOS		1.4		V
VT+	Schmitt trigger, positive-going threshold	LVCMOS			2.0	
VT-	Schmitt trigger, negative-going threshold	LVCMOS	0.8			
I_{IH}	High level input current					
	Input buffer	$V_{IN} = V_{DD}$	-10		10	uA
	Input buffer with pull-up		10	30	60	
I_{IL}	Low level input current					
	input buffer		-10		10	uA
	Input buffer with pull-up	$V_{IN} = V_{SS}$	-60	-30	-10	
V_{OH}	High level output voltage					
	Type B1 to B24 Note2	I_{OH} = -1uA	V_{DD}-0.05			V
	Type B1	I_{OH} = -1mA	2.4			
	Type B2	I_{OH} = -2mA				
V_{OL}	Low level output voltage					
	Type B1 to B24Note2	I_{OH} = 1uA			0.05	V
	Type B1	I_{OH} = 1mA			0.4	
	Type B2	I_{OH} = 2mA				
I_{OZ}	Tri-state output leakage current	V_{OUT}= V_{SS} or V_{DD}	-10		10	uA
I_{OS}	Output short circuit current	V_{DD}= 3.6V, V_O = V_{DD}			210	mA
		V_{DD}= 3.6V, V_O = V_{SS}	-170			
I_{DD}	Quiescent supply current	V_{IN} = V_{SS} or V_{DD}			100note3	uA
C_{IN}	Input capacitanceNote4	Any Input and Bidirectional Buffers			4	pF
C_{OUT}	Output capacitanceNote4	Any Output Buffer			4	pF

V_{DD}= 3.3 ± 0.3V, V_{EXT}= 5+ 0.25V, TA = 0 to 70°C (In case of 5V-tolerant IO)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH} Note1	High level input voltage (LVCMOS interface)		2.0			V
V_{IL} Note1	Low level input voltage (LVCMOS interface)				0.6	V
VT	Switching threshold	LVCMOS		1.4		V
VT+	Schmitt trigger, positive-going threshold	LVCMOS			2.0	
VT-	Schmitt trigger, negative-going threshold	LVCMOS	0.8			
I_{IH}	High level input current					
	Input buffer	V_{IN} = V_{DD}	-10		10	uA
	Input buffer with pull-up		10	30	60	
I_{IL}	Low level input current					
	input buffer		-10		10	uA
	Input buffer with pull-up	V_{IN} = V_{SS}	-60	-30	-10	
I_{OZ}	Tri-state output leakage current	V_{OUT}= V_{SS} or V_{EXT}	-10		10	uA
I_{OS}	Output short circuit current	V_{DD}=3.6V, V_O=V_{DD}			55	mA
		V_{DD}=3.6V, V_O=V_{SS}	-55			
I_{DD}	Quiescent supply current	V_{IN}= V_{SS} or V_{DD}			100 Note3	uA
C_{IN}	Input capacitance	Any Input and Bidirectional Buffers			4	pF
C_{OUT}	Output capacitance	Any Output Buffer			4	pF

NOTES:

1. All 5V-tolerant input have less than 0.2V hysterisis.
2. Type B1 means 1mA output driver cells, and Type B6/24 means 6mA/24mA output driver cells.
3. This value depends on the customer design.
4. This value exclude package parasitic.

OPERATION DESCRIPTION

IO TIMING SPECIFICATION

MCU Interface

a. Serial interface mode

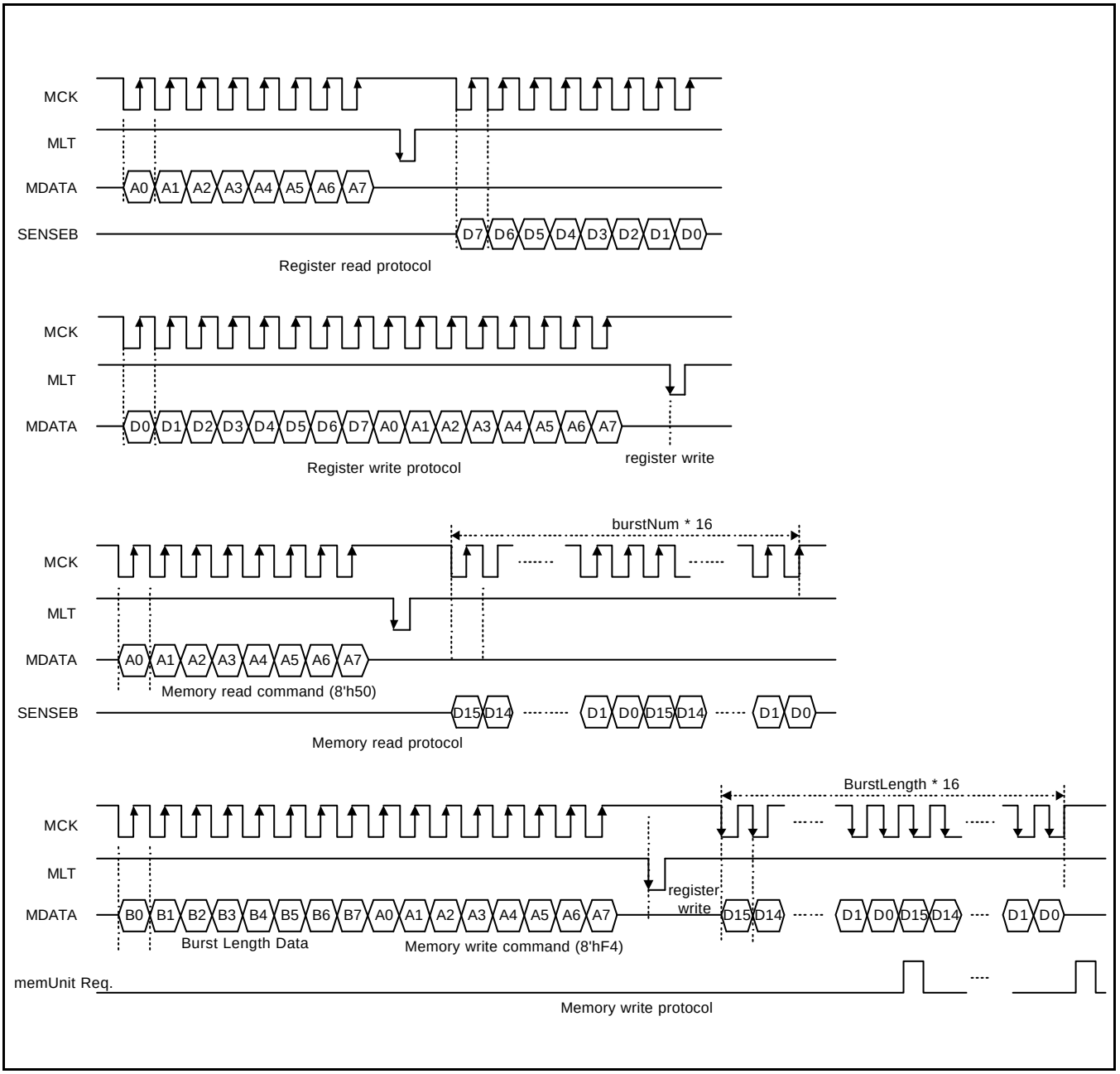


Figure 5. Serial interface mode

b. Parallel interface mode

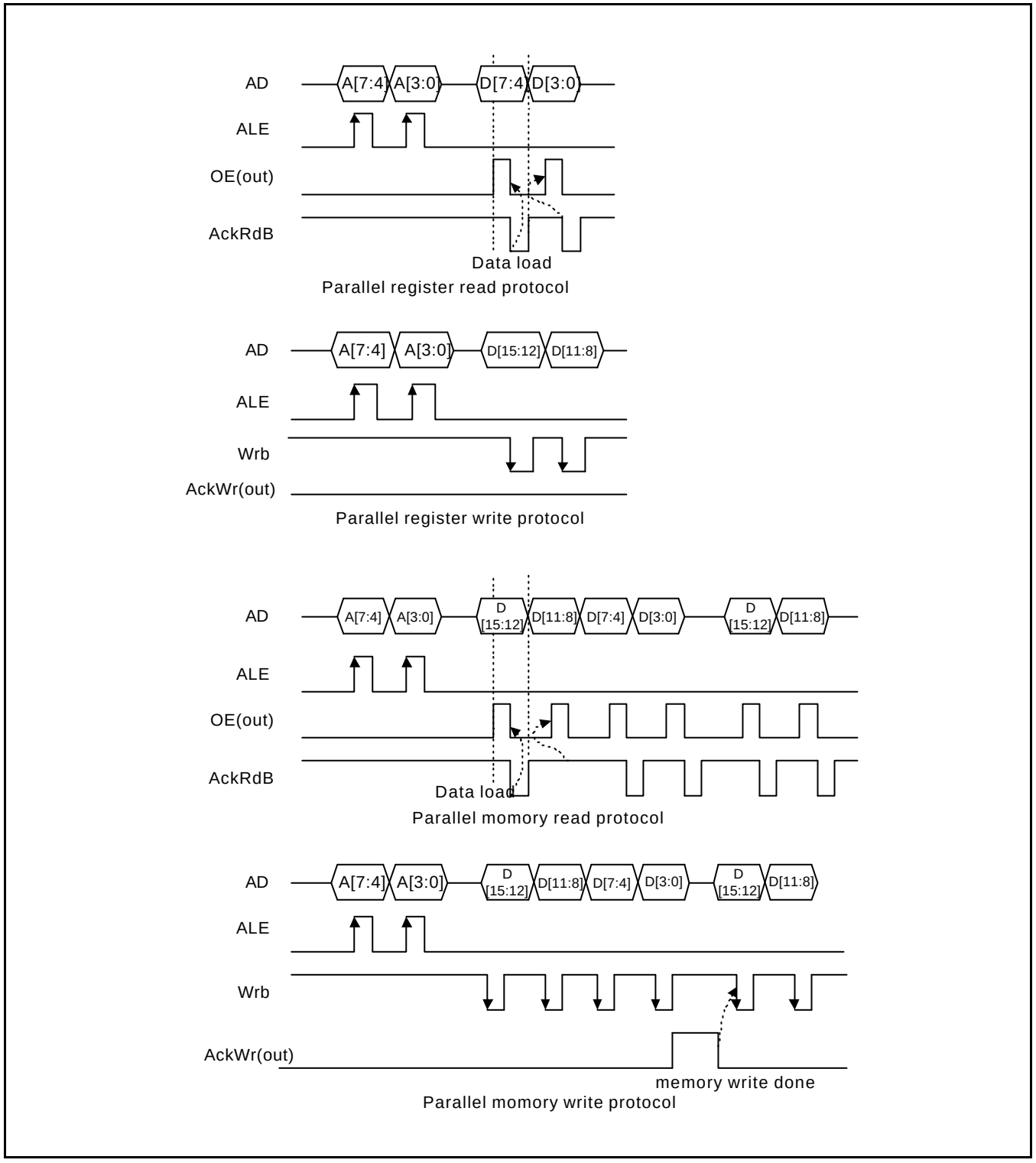


Figure 6. Parallel interface mode

Description for the memory read protocol

1. Write Start Address to H_MEM_ADDR_HIGH (8'hf0), H_MEM_ADDR_MID (8'hf1), and H_MEM_ADDR_LOW (8'hf2).
2. Write BL(Burst Length) to H_MEM_ADDR_BL (8'hf3). The BL is programmable between 1 and 63. The default value of the H_MEM_ADDR_BL when reset is 1.
3. Send command 8'h50 (i.e. Transfer address of the H_MEM_READ).
4. Read MDOUT as many bits as the " BL*16 ". (16bits per 1 burst, each burst is MSB first.)

Description for the memory write protocol

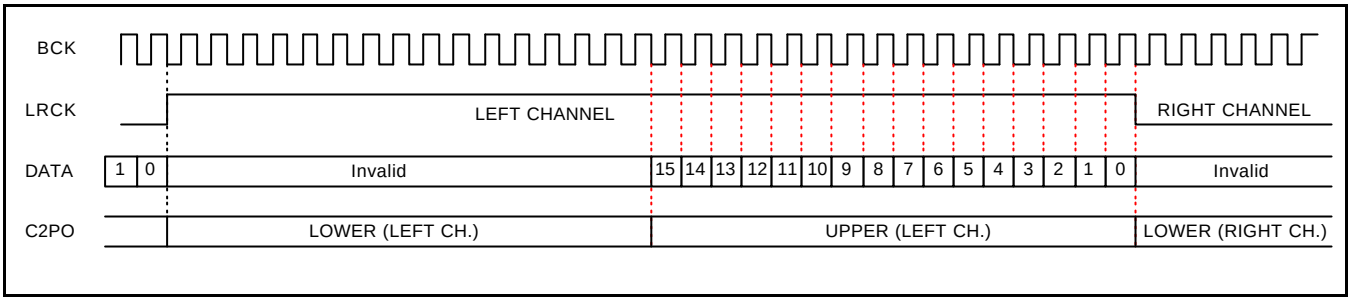
1. Write Start Address to H_MEM_ADDR_HIGH (8'hf0), H_MEM_ADDR_MID (8'hf1), and H_MEM_ADDR_LOW (8'hf2).
2. Write BL(Burst Length)and memory write command to H_MEM_WRITE (8'hf4). The BL is programmable between 1 and 63.
3. Write MDAT as many bits as the " BL*16 ". (16bits per 1 burst, each burst is MSB first.)

Description for the input buffer write protocol

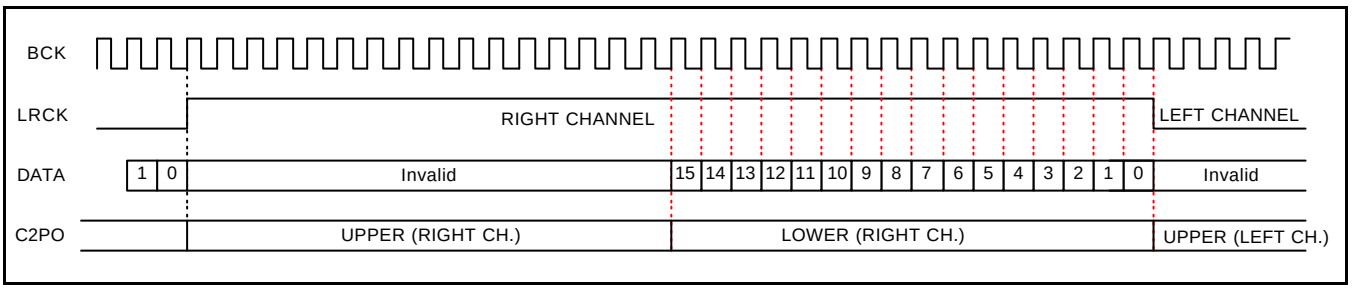
1. Write BL(Burst Length)and input buffer write command to H_MEM_WRITE_IB (8'hf5). The BL is programmable between 1 and 63.
2. Write MDAT as many bits as the " BL*16 ". (16bits per 1 burst, each burst is MSB first.)

CD-DSP Interface

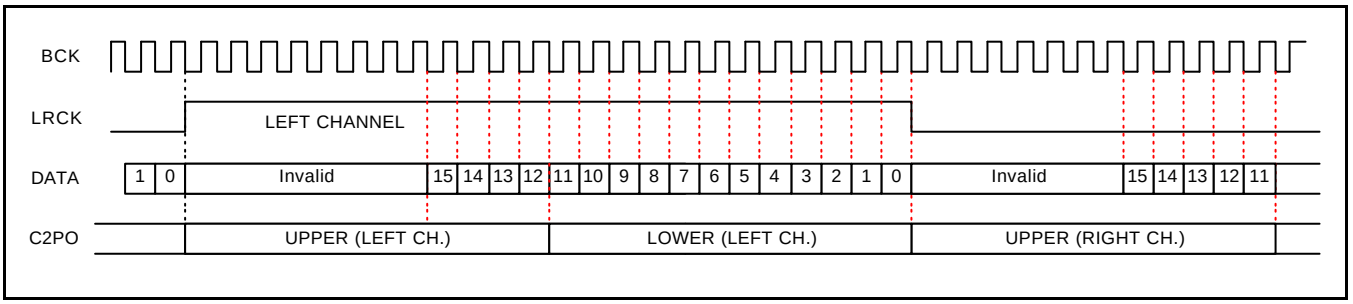
(a) 32-bit BCK, MSB First, Right Channel Low, C2PO LSB First, Data Latch Timing High:



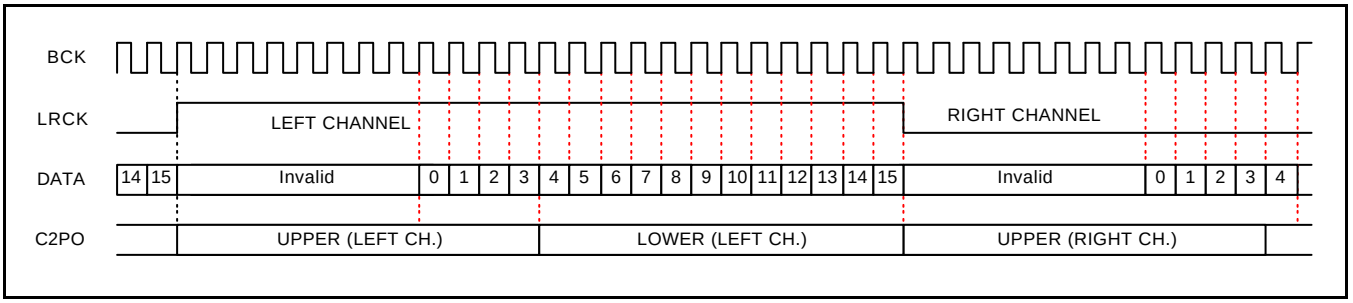
(b) 32-bit BCK, MSB First, Left Channel Low, C2PO MSB First, Data Latch Timing Low:



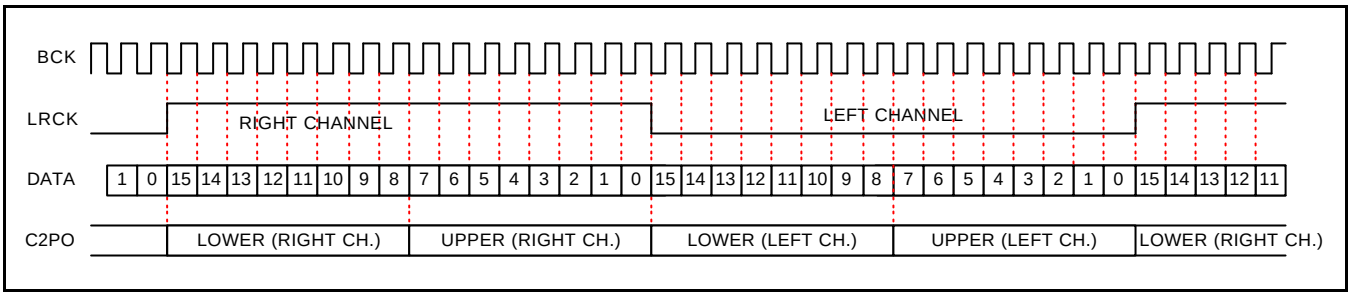
(c) 24-bit BCK, MSB First, Right Channel Low, C2PO MSB First, Data Latch Timing High:



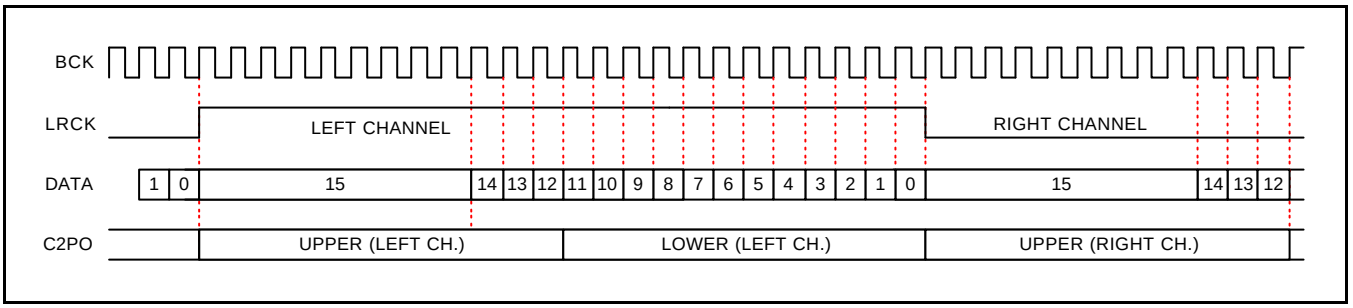
(d) 24-bit BCK, LSB First, right Channel Low, C2PO MSB First, Data Latch Timing Low:



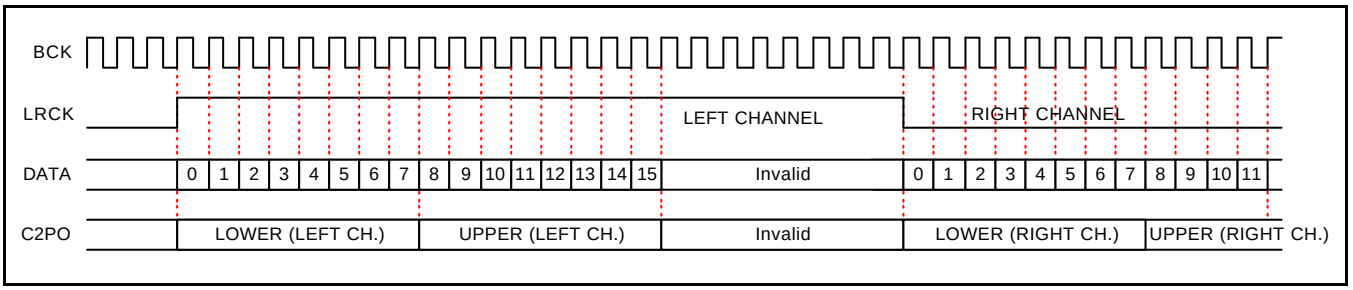
(e) 16-bit BCK, MSB First, Left Channel Low, C2PO LSB First, Data Latch Timing High:



(f) 24-bit BCK, MSB First, Right Channel Low, C2PO MSB First, Data Latch Timing Low:



(g) 24-bit BCK, LSB First, Right Channel Low, C2PO LSB First, Data Latch Timing Low:



Even on the format of description it changes a H_INPIF_W register value and the CD DSP which is various and the interface is possible.

DRAM Interface

Read Cycle

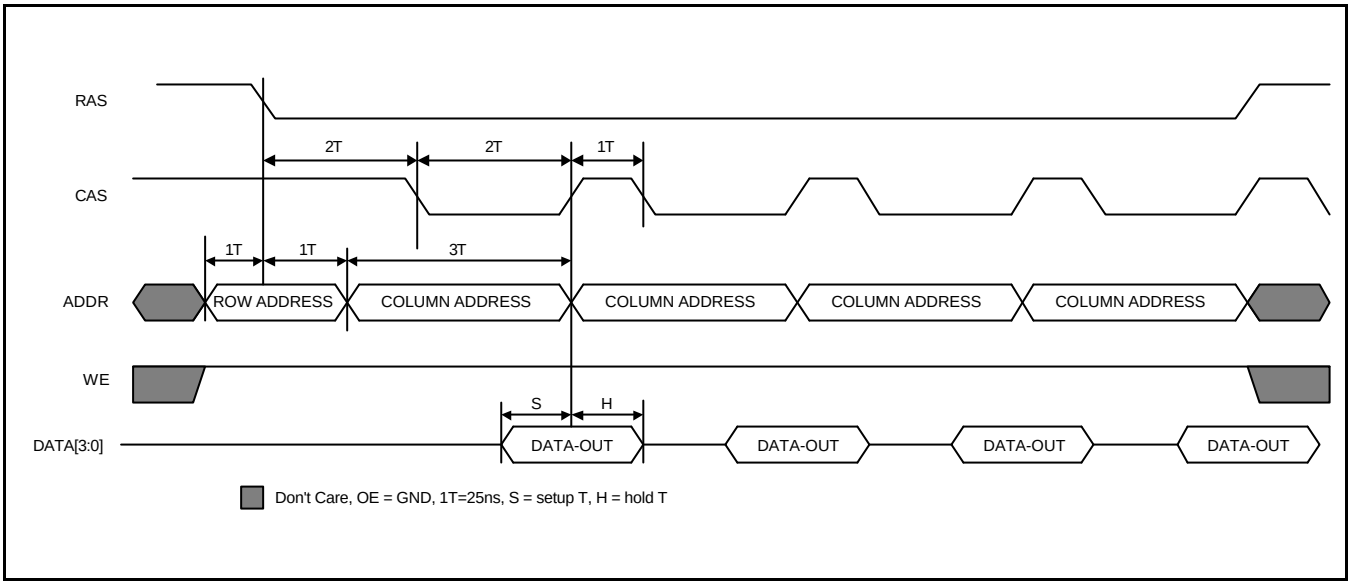


Figure 7. Read Cycle

Write Cycle

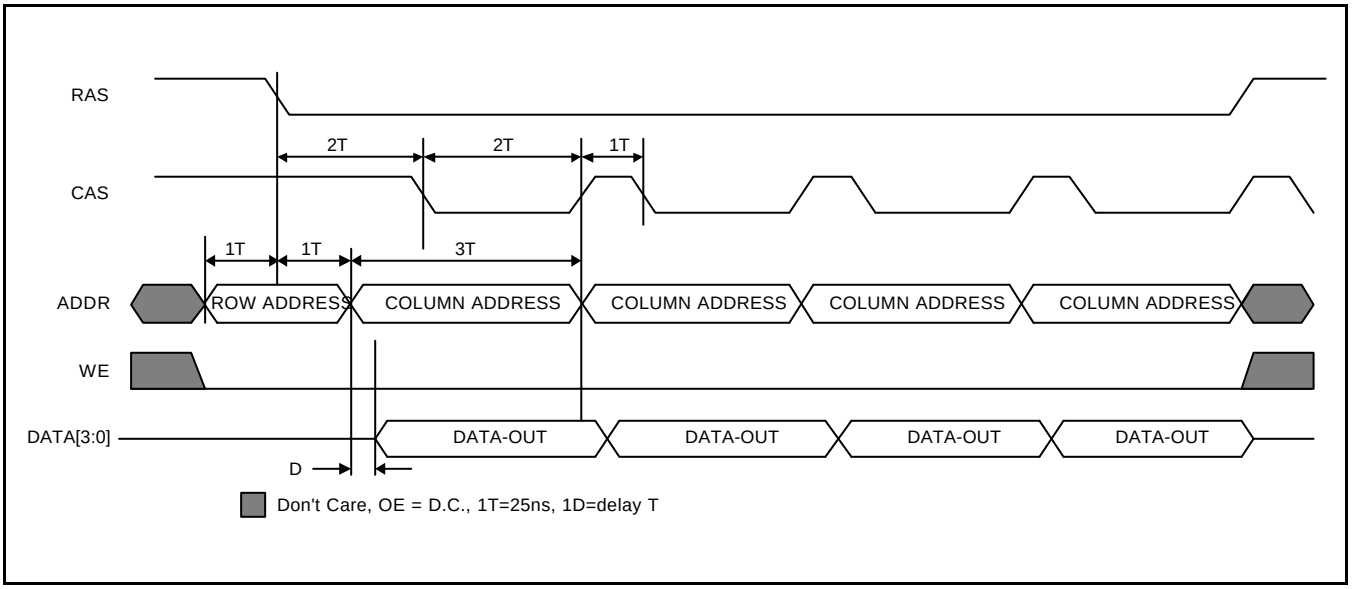


Figure 8. Write Cycle

RAS Before CAS Refresh

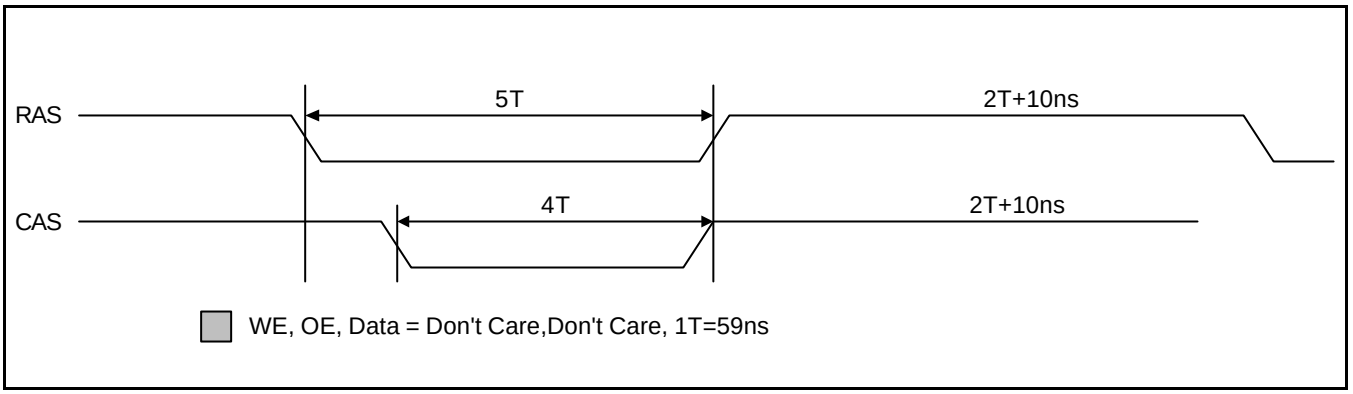
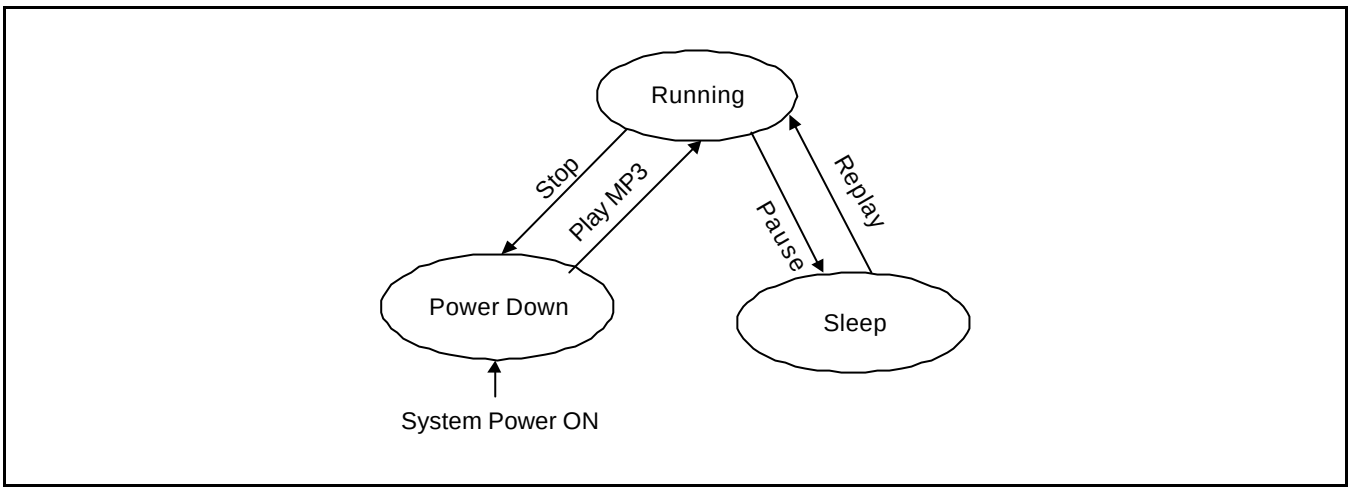


Figure 9. RAS Before CAS Refresh

POWER MANAGEMENT

Power Save Modes

Down : Master Clock Disabled. Whole chip is in reset state and clocking is disabled.
Sleep Mode : All units suspended except hitUnit and DRAM Controller Block to refresh DRAM.



Power down mode

Power down mode is implemented using MLAT, MCK, and MDAT. When the MLAT is low the MDAT is goes to low, the CD-MP3 goes to "power down reset" mode. It means power ON state. When the MLAT is low and the MCK goes to LOW, the CD-MP3 toggles the "power down mode". The default value of MLAT, MCK, and MDAT is HIGH. When the system power becomes ON and the master reset comes, Micom should set the value of MLAT, MCK, and MDAT to HIGH. And should reset the power down mode of CD-MP3 using MLAT and MDAT LOW. Finally should send the S/W reset to CD-MP3 H_SOFT_RST (8'hE0) register.

Sleep mode

In sleep mode, the minimal power is supplied which is needed just for DRAM refresh, receiving host command, and etc. There is a register H_SLEEP_CR to control Sleep mode. To enter sleep mode write "1xxxxxxx" into the H_SLEEP_CR. To wake up from sleep mode write "0xxxxxxx" into the H_SLEEP_CR.

H_SLEEP_CR 8'hdf

Power Save mode

In power save mode, hardware units in the S5L9276X can be dynamically enabled or disabled during it's operation to reduce the power consumption. This feature is enabled by writing xxxxxxx1 to H_PSV_ENABLE and disabled by writing xxxxxx0 to H_PSV_ENABLE.
Make sure that Power Save mode should be disabled for Micom to access all other S5L9276 registers.

H_PSV_ENABLE 8'hde

HOST MCU CONTROL SPACE

Registers to control CD-ROM sector decoding

// Read only registers (8'h20 — 8'h2F reserved for cdrUnit - Read)

H_MIN_R	8'h24	"minute" in the header of the sector being currently decoded.
H_SEC_R	8'h25	"second" in the header of the sector being currently decoded.
H_FRM_R	8'h26	"frame" in the header of the sector being currently decoded.
H_MODB_R	8'h27	CD-ROM Mode information in the header of the sector being currently decoded.
H_FN_R	8'h28	The file number information in the sub header of the current frame. This is valid for Mode-2 format.
H_CN_R	8'h29	The channel number information in the sub header of the current frame. This is valid for Mode-2 format.
H_SM_R	8'h2a	The sub-mode information in the sub header of the current frame. This is valid for Mode-2 format.
H_CI_R	8'h2b	The coding information in the sub header of the current frame. This is valid for Mode-2 format.
H_ERR_R	8'h2c	The Header Error flags in the sub header of the current frame.
		bit7 M_EMIN (Error in MIN)
		bit6 M_ESEC (Error in SEC)
		bit5 M_EFRM (Error in FRM)
		bit4 M_EMOD (Error in MODB)
		bit3 M_EFN (Error in FN)
		bit2 M_ECN (Error in CN)
		bit1 M_ESM (Error in SM)
		bit0 M_ECI (Error in CI)
H_BLKST_R	8'h2d	Indicates that unexpected Sync has been detected.
		bit7 Long Block 0 : Normal case. 1 : The CD-ROM decoder detects the Internal Synchronization pattern but does not detect the External Synchronization pattern. The previous frame has longer bytes of data than expect.
		bit6 Short Block 0 : Normal case. 1 : The CD-ROM decoder detects the External Synchronization pattern but does not detect the Internal Synchronization pattern. The previous frame has shorter bytes of data than expect.
		bit5 Invalid Block 0 : Normal case. 1 : The CD-ROM decoder does not detect either External or Internal Synchronization pattern when Internal or External Synchronization pattern is detected. Current frame data is invalid.
		bit4:0 not used

// Write only registers (8'hB0 — 8'hBF reserved for cdrUnit - Write)

H_INPIF_W 8'hB1

bit7	M_BCKS1
bit6	M_BCKS0
bit7:6	Indicate the number of BCKs per 16-bit word 00 = 16 BCKs, Data valid at every BCK 01 = 24 BCKs. Data valid for the last 16 BCKs 10 = 24 BCKs. Data valid for the first 16 BCKs 11 = 32 BCKs. Data valid for the last 16 BCKs
bit5	M_DATMF Must be set equal to '1' for the input data with MSB first
bit4	M_C2PMF Must be set equal to '1' for the input C2PO with MSB first
bit3	M_LRB. Must be set equal to '1' if HIGH of LRCK indicates the left channel.
bit2	M_LATCH(not enable) 1 : Input data is latched on the rising edge of BCK, 0 : Input data is latched on the falling edge of BCK.
bit1	M_C2PEN 1 : C2PO data is input with other data, 0 : No C2PO data is input with other data.
bit0	M_PHILIPS. When the CD-DSP data format is as PHILIPS', this bit should be a logical '1' 1: Supports PHILIPS' IIS DSP interface format. 0 : Do not supports PHILIPS' IIS DSP interface format. default value : 0x00

H_HEAD_W 8'hB2 MODE1, MODE2-Form1, MODE2-Form2

bit7	Mode2/Mode1 1 : Mode2 0 : Mode1
bit6	Form2/Form1 1 : Form2 0 : Form1
bit5	AC. Auto correction 1 : CD-ROM decoder acts as according to the value of mode/form bits in the header/sub header 0 : CD-ROM decoder acts as according to the value of bit7:6 of this register
bit4	DSCR .Descrambling Enable/Disable 1 : Descrambling Enable 0 : Descrambling Disable
bit3:0	not used

H_OPSR_W	8'hB3	0x00: Set CDROM decoding mode to IDLE mode. CDROM decoder discards all input bit stream and does no decoding. All registers containing decoded header information is not valid in this mode. 0x90: Set CDROM decoding mode to MONITORING mode. Decodes Header only. 0x91: Set CDROM decoding mode to DECODING mode. This causes S5L9276 starts to decode the following sector and store to DRAM.
H_START_M	8'hB4	Not Used
H_START_S	8'hB5	Not Used
H_START_F	8'hB6	Not Used
H_ECC_EN	8'hB7	Control register for ECC enable/disable. bit7:1 not used bit0 H : Ecc Enable default value : 0x00

Registers to communicate with embedded DSP core

// Read only registers (8'h00 — 8'h0F reserved for dspUnit - Read)		
H_OUT1_LOW	8'h01	Low byte of OUT1 register.
H_OUT1_HIGH	8'h02	High byte of OUT1 register.
H_OUT2_LOW	8'h03	Low byte of OUT2 register.
H_OUT2_HIGH	8'h04	High byte of OUT2 register.
H_OUT_XTRA	8'h05	Extra byte of OUT register.
H_EMPH	8'h06	Indicate Emphasis ON/OFF and Emphasis Type. bit[7:2] : not used. bit[1] : If "1", Emphasis ON. If "0", emphasis OFF. bit[0] : Emphasis Type
// Write only registers (8'h80 — 8'h8F reserved for dspUnit - Write)		
H_SSPINT	8'h80	Micom command register. Micom writes a command to this register.
H_IN_LOW	8'h81	Low byte of in register
H_IN_HIGH	8'h82	High byte of in register
H_IN_XTRA	8'h83	Extra byte of in register

Registers for configuration and status of DRAM

// Read only registers (8'h10 — 8'h1F reserved for memUnit - Read)

H_DUMP_CNT	8'h11	Total number of CD frames currently has been dumped to DRAM since 0x91 was written to OPSR register. Once all frames as many as specified in the H_FRAME_NO register are dumped into DRAM, OPSR value will be changed to 90 automatically after completion of dump. At every time after 0x91 was written to OPSR and 1 frame has been dumped, the H_DUMP_CNT reset to "1".
H_IB_STATE	8'h12	Input Buffer Occupancy bit0 : Empty bit1 : Low bit2 : High
H_IB_DATA_COUNT_H	8'h13	The high positive byte of the data count value which is to the input buffer
H_IB_DATA_COUNT_M	8'h14	The middle position byte of the data count value which is to the input buffer
H_IB_DATA_COUNT_L	8'h15	The low position byte of the data count value which is to the input buffer
H_OBL_DATA_COUNT_H	8'h16	The high positive byte of the data count value which is to the OBL buffer
H_OBL_DATA_COUNT_M	8'h17	The middle positive byte of the data count value which is to the OBL buffer
H_OBL_DATA_COUNT_L	8'h18	The low positive byte of the data count value which is to the OBL buffer
H_OBR_DATA_COUNT_H	8'h19	The high positive byte of the data count value which is to the OBR
H_OBR_DATA_COUNT_M	8'h1a	The middle positive byte of the data count value which is to the OBR buffer
H_OBR_DATA_COUNT_L	8'h1b	The low positive byte of the data count value which is to the OBR buffer

// Write only registers (8'h90 — 8'hAF reserved for memUnit - Write)

H_CD_START_H	8'h90
H_CD_START_L	8'h91
H_CD_END_H	8'h92
H_CD_END_L	8'h93
H_IB_START_H	8'h94
H_IB_START_M	8'h95
H_IB_START_L	8'h96
H_IB_END_H	8'h97
H_IB_END_M	8'h98
H_IB_END_L	8'h99
H_OBL_START_H	8'h9a
H_OBL_START_M	8'h9b
H_OBL_START_L	8'h9c
H_OBL_END_H	8'h9d
H_OBL_END_M	8'h9e
H_OBL_END_L	8'h9f
H_OBR_START_H	8'ha0
H_OBR_START_M	8'ha1
H_OBR_START_L	8'ha2
H_OBR_END_H	8'ha3
H_OBR_END_M	8'ha4
H_OBR_END_L	8'ha5
H_REFRESH_INTERVAL	8'ha6

DRAM refresh interval rate

bit1:0	00:	624 cycles
	01:	608 cycles
	10:	576 cycles
	11:	480 cycles

H_DRAMIF_NOE	8'ha7	DRAM Interface Output Enable Control Register bit7 : DRAM Interface Outputs Enable (Active Low.) bit6 — 0 : don't care
H_FRAME_NO	8'ha8	The frame as many as specified in this H_FRAME_NO register are dumped into DRAM after every 0x91 is written in the OPSR. OPSR value will be changed to 90 automatically after completion of dump. The maximum value allowed for the H_FRAME_NO is IB size/1024.
H_SHOCK	8'ha9	When detect shock from Micom, it sets this register with the value of "xxxxxxx1". This causes to stop dump operation and deletes frames as many as specified in the H_RETURN_SECTOR register from the Input Buffer. When there's no shock, Micom sets H_SHOCK register with the value of "xxxxxxx0".
H_IB_WR_OFFSET	8'haa	Input Buffer is in LOW state when the condition below is met :" Input Buffer Vacancy is equal to or less than (Size of Input Buffer - the value in the H_IB_WR_OFFSET) "
H_RETURN_SECTOR	8'hab	When occurred the shock, before recognizing with the shock, the case shock where the data which breaks has become the dump in the dram the set it does as a favor the thing authorization which will erase the data of the some frame in standard. If set register clear the H_DUMP_CNT.
H_DRAM_TYPE	8'hac	Define the DRAM type. bit1:0 00: 4Mbit dram 10: 16Mbit dram 2K ref. 11: 16Mbit dram 4K ref.

Registers to control DAC interface

// Read only registers (8'h30 — 8'h3F reserved for difUnit - Read)

// Write only register (8`hB0)
H_DAC_TYPE 8'hB0 To control Type of 1bit DAC.

Register	Name	Value	Operation
H_DAC_TYPE[7]	bck phase	0	rising edge output data strobe
		1	falling edge output data strobe
H_DAC_TYPE[6]	lrck phase	0	If lrck is 'L', data is R-channel.
		1	If lrck is 'H', data is R-channel.
H_DAC_TYPE[5:4]	num of bck per lrck	00	32 Fs
		01	48 Fs
		10	64 Fs
		11	Don't use
H_DAC_TYPE[3:2]	num of real data	00	16
		01	18
		10	20
		11	24
H_DAC_TYPE[1:0]	real data position(justify)	00	I2S justify
		01	right justify
		10	left justify
		11	Don't use

// Write only registers (8'hC0 — 8'hCF reserved for difUnit - Write)
H_DACIF_nOE 8'hC0 To control Tri-State Output of difUnit.
bit7 : If "1", DAC Interface outputs goes high impedance state.
If "0", DAC Interface outputs enabled.
bit6 — 0 : don't care
To control type of DAC data array
bit6 : If "1", the type of DAC is LSB first.
If "0", that is MSB first.
bit5 — 0 : don't care

Registers for configuration of clock

// Read only registers (8'h40 — 8'h4F reserved for ckgUnit - Read)

// Write only registers (8'hD0 — 8'hDF reserved for ckgUnit)

H_PLL0_P0	8'hd0	P register for PLL0 (See chapter 7.)
H_PLL0_M0	8'hd1	M register for PLL0 (See chapter 7.))
H_PLL0_S0	8'hd2	S register for PLL0 (See chapter 7.))
H_PLL1_P1	8'hd3	P register for PLL1 (See chapter 7.))
H_PLL1_M1	8'hd4	M register for PLL1 (See chapter 7.))
H_PLL1_S1	8'hd5	S register for PLL1 (See chapter 7.))
H_CKG_DIV_XY	8'hd6	(See chapter 7.))
H_CKG_CMD_0	8'hd7	(See chapter 7.))
H_SLEEP_CR	8'hdf	SLEEP control register bit7 — 1 : don't care bit0 : If "1", Set S5L9276 to SLEEP mode. If "0", set S5L9276 to RUNNING mode.

Registers for reset control

// Write only registers (8'hE0 — 8'hEF reserved for rstUnit - Write)

H_SOFT_RST	8'hE0	Master reset by software control

Registers for DRAM access and Interrupt Source Register

// Read only registers (8'h50 — 8'h5F reserved for hifUnit - Read)

H_MEM_READ	8'h50	Buffer Register for DRAM burst read
H_INT_READ	8'h51	Interrupt Source Register

// Write only registers (8'hF0 — 8'hFF reserved for hifUnit - Write)

H_MEM_ADDR_HIGH	8'hf0	High byte of start address for DRAM burst read
H_MEM_ADDR_MID	8'hf1	Middle byte of start address for DRAM burst read
H_MEM_ADDR_LOW	8'hf2	High byte of start address for DRAM burst read
H_MEM_ADDR_BL	8'hf3	Burst Length for DRAM burst read (1 — 63, default is 1.)
H_MEM_WRITE	8'hf4	Buffer Register for DRAM burst write
H_MEM_WRITE_IB	8'hf5	Buffer Register for Input Buffer in DRAM burst write

SETTING SYSTEM CLOCK FREQUENCY

PLL configuration should be changed in the SLEEP mode only. To change PLL configuration,

1. enter to SLEEP mode.
2. change PLL configuration.
3. wait 250ms.
4. exit from SLEEP mode.

NOTE :

ACLK : audio clock of S5L9276X internal.
CLK : system clock of S5L9276X internal.

MODE 1 - Dual PLL Mode A (H_CKG_CMD0[2:1] = 01 or 00 , PLL_BYPASS = LOW)

		aclk = 12.288MHz clk = 38.7MHz	**aclk = 16.9344MHz clk =38.7MHz**	**aclk = 18.432MHz clk = 38.7MHz**
Host Control	H_PLL0_P0	19 (D)	19 (D)	19 (D)
	H_PLL0_M0	40 (D)	40 (D)	40 (D)
	H_PLL0_S0	0 (D)	0 (D)	0 (D)
	H_PLL0_P1	5 (D)	xxxx xxxx (B)	5 (D)
	H_PLL0_M1	12 (D)	xxxx xxxx (B)	22 (D)
	H_PLL0_S1	0 (D)	xxxx xxxx (B)	0 (D)
	H_CKG_DIV_XY	xx11 xx00 (B)	xxxx xxxx (B)	xx11 xx00 (B)
	H_CKG_CMD0	0000 0010 (B)	0000 0000 (B)	0000 0010 (B)
PIN SETTING	CLK (I)	CONNECTED TO XOUT		
	ACLK_EXT (I)	TIED TO GND		
	XI	16.9344MHz X-tal		
	XO	16.9344MHz X-tal		

MODE 2 - Dual PLL Mode B (H_CKG_CMD0[2:1] = 01 or 00 , PLL_BYPASS = LOW)

		aclk = 12.2919MHz clk = 32.33MHz	**aclk = 16.9344MHz clk = 32.33MHz**	**aclk = 18.4378MHz clk = 32.33MHz**
Host Control	H_PLL0_P0	20 (D)	20 (D)	20 (D)
	H_PLL0_M0	34 (D)	34 (D)	34 (D)
	H_PLL0_S0	0 (D)	0 (D)	0 (D)
	H_PLL0_P1	10 (D)	xxxx xxxx (B)	14 (D)
	H_PLL0_M1	65 (D)	xxxx xxxx (B)	65 (D)
	H_PLL0_S1	3 (D)	xxxx xxxx (B)	2 (D)
	H_CKG_DIV_XY	xx01 xx00 (B)	xxxx xxxx (B)	xx01 xx00 (B)
	H_CKG_CMD0	0000 0010 (B)	0000 0000 (B)	0000 0010 (B)
PIN SETTING	CLK (I)	CONNECTED TO XOUT		
	ACLK_EXT (I)	TIED TO GND		
	XI	16.9344MHz X-tal		
	XO	16.9344MHz X-tal		

MODE 3 - Single PLL Mode (H_CKG_CMD0[2:1] = 10 or 00 , PLL_BYPASS = LOW)

		aclk = 12.3159MHz clk = 36.9MHz	aclk = 16.9344MHz clk =38.7MHz	aclk = 18.407MHz clk = 36.8MHz
Host Control	H_PLL0_P0	20 (D)	19 (D)	21 (D)
	H_PLL0_M0	40 (D)	40 (D)	42 (D)
	H_PLL0_S0	0 (D)	0 (D)	0 (D)
	H_PLL0_P1	xxxx xxxx (B)	xxxx xxxx (B)	xxxx xxxx (B)
	H_PLL0_M1	xxxx xxxx (B)	xxxx xxxx (B)	xxxx xxxx (B)
	H_PLL0_S1	xxxx xxxx (B)	xxxx xxxx (B)	xxxx xxxx (B)
	H_CKG_DIV_XY	xx10 xxxx (B)	xxxx xxxx (B)	xx01 xxxx (B)
	H_CKG_CMD0	0000 0100 (B)	0000 0000 (B)	0000 0100 (B)
PIN SETTING	CLK (I)	CONNECTED TO XOUT		
	ACLK_EXT (I)	TIED TO GND		
	XI	16.9344MHz X-tal		
	XO	16.9344MHz X-tal		

MODE 4 - PLL BYPASS Mode (PLL_BYPASS = HIGH)

		aclk = External Source (ACLK_EXT) clk = External Source (CLK)
Host Control	H_PLL0_P0	xxxx xxxx (B)
	H_PLL0_M0	xxxx xxxx (B)
	H_PLL0_S0	xxxx xxxx (B)
	H_PLL0_P1	xxxx xxxx (B)
	H_PLL0_M1	xxxx xxxx (B)
	H_PLL0_S1	xxxx xxxx (B)
	H_CKG_DIV_XY	xxxx xxxx (B)
	H_CKG_CMD0	xxxx xxxx (B)
PIN SETTING	CLK (I)	System Clock Frequency
	ACLK_EXT (I)	Audio Clock Frequency (384Fs)
	XI	TIED TO GND
	XO	OPEN

MICOM PROGRAMMING GUIDELINE

Transferring Input Bit stream to S5L9276

Micom is allowed to initiate the transfer when the Input Buffer is in LOW state which is by the "Input Buffer State" Interrupt (See section skip function) from CD-MP3 IC.

Burst Transfer with the number of sectors being transferred.

— Verify the Input Buffer is in LOW state. The register H_IB_STATE tells Input Buffer (Empty, Low, or High). When there is any change in the H_IB_STATE, "Input Buffer " Interrupt arises, and External MCU can read the H_IB_STATE to know the Input State. When Input Buffer is in lower than the "Input Buffer Low Threshold" we say is in LOW state. Input Buffer Low Threshold is determined by the value of the register _IB_WR_OFFSET. It has the following relationship.

  Low Threshold = (Input Buffer Size in number of words) - (H_IB_WR_OFFSET)*1024

— Micom decides the start sector address from which the CD-ROM sectors are transferred S5L9276.

— Write number of sectors being transferred into H_FRAME_NO register.

— Micom initiate to transfer CD-ROM sectors from CDP subsystem to S5L9276 starting the address (MSF) which is several sectors ahead the start sector address.

— Micom gets sector address information (MSF) from CDP subsystem while CDP transfers CD-ROM sectors to S5L9276.

— Micom checks continuously if the MSF received from CDP subsystem is reached at the MSF from which Micom wants to put the corresponding sector in S5L9276.

— If the MSF received from CDP subsystem is reached at (the start MSF - 1), Micom "0x91" to H_OPSR_W in S5L9276 to allow for S5L9276 to start decode sectors when sector boundary is reached.

— When "Dump-End" interrupt encountered during sector transfer, read the H_DUMP_CNT and check if the content of the H_DUMP_CNT is equal to the content of _FRAME_NO. If they are equal, it indicates all sectors have been transferred successfully if they are not, it indicates that Input Buffer High condition were met in the middle of transfer and the remaining transfer has been discarded after that condition. If that n has occurred, Micom should transfer again from the sector which was cancelled. new start sector address can be calculated with the previous start sector address and content of the H_DUMP_CNT register.

* S5L9276 set the "Dump-End" interrupt when the content of the H_DUMP_CNT is equal to content of H_FRAME_NO and also when Input Buffer High condition were met during transfer.

Burst Transfer without the number of sectors being transferred.

— Verify the Input Buffer is in LOW state. The register H_IB_STATE tells Input Buffer (Empty, Low, or High). When there is any change in the H_IB_STATE, "Input Buffer " Interrupt arises, and External MCU can read the H_IB_STATE to know the Input State. When Input Buffer is in lower than the "Input Buffer Low Threshold" we say is in LOW state. Input Buffer Low Threshold is determined by the value of the register _IB_WR_OFFSET. It has the following relationship.

Low Threshold = (Input Buffer Size in number of words) - (H_IB_WR_OFFSET)*1024

— Micom decides the start sector address from which the CD-ROM sectors are transferred S5L9276.

— Write 0 to the H_FRAME_NO. (The default value after reset this is 0 therefore, this would not be necessary.)

— Micom initiate to transfer CD-ROM sectors from CDP subsystem to S5L9276 starting the address (MSF) which is several sectors ahead the start sector address.

— Micom gets sector address information (MSF) from CDP subsystem while CDP transfers CD-ROM sectors to S5L9276.

— Micom checks continuously if the MSF received from CDP subsystem is reached at the MSF from which Micom wants to put the corresponding sector in S5L9276.

— If the MSF received from CDP subsystem is reached at (the start MSF - 1), Micom "0x91" to H_OPSR_W in S5L9276 to allow for S5L9276 to start decode sectors when sector boundary is reached.

— When "Dump-End" interrupt encountered during sector transfer, it indicates the input is in BUFFER-HIGH state and any more transfer is discarded to avoid input buffer .

— Read the H_DUMP_CNT register which represents the number of sectors that have successfully transferred.

— Micom calculate new start sector address which is the one for the next to the last which has been transferred before.

— Repeat the whole process.

CDFS Table Read

S5L9276X decodes File Allocation Table of CD-ROM and stores it to DRAM. Micom can access DRAM to read the CDFS Table using register read protocol.

Setting DRAM Refresh Rate

Micom can change DRAM refresh rate by change a code in the H_REFRESH_INTERVAL register as following :

H_REFRESH_INTERVAL(8'ha2) VALUE	Maximum Refresh Interval
8'bxxxxxx00	624 cycles
8'bxxxxxx01	608 cycles
8'bxxxxxx10	576 cycles
8'bxxxxxx11	480 cycles

Configuration of DRAM Memory Map

When S5L9276 is reset the DRAM is configured to the default memory map as shown below.

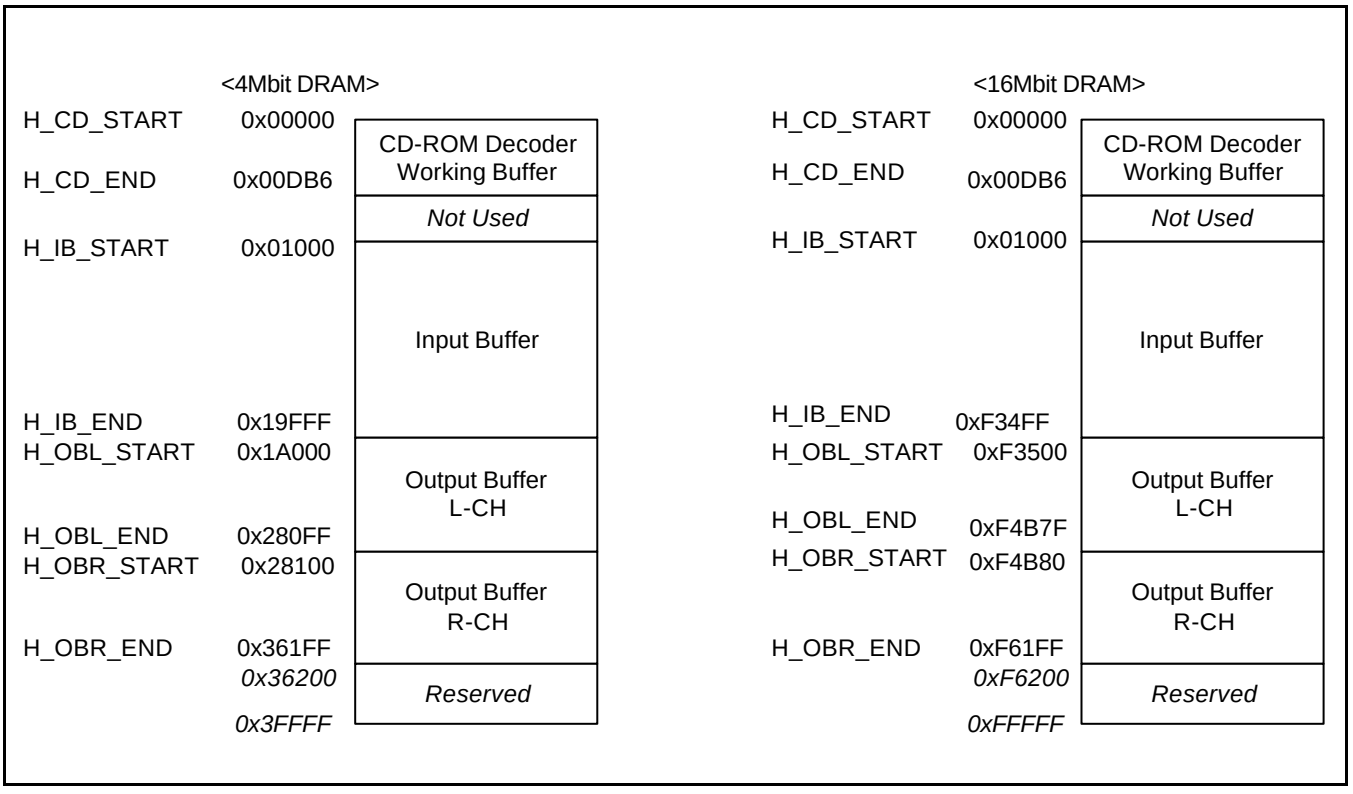


Figure 10.

REGISTER	ADDRESS (HEX)	ADDRESS (DEC)	SIZE
H_CD_START	0x00000	0	Size = 3511
H_CD_END	0x00DB6	3510	
	0x00DB7	3511	585 words
	0x00FFF	4095	*Not Used*
H_IB_START	0x01000	4096	IB_Size = 100K
H_IB_END	0x19FFF	106495	
H_OBL_START	0x1A000	106496	OBL_Size = 57600
H_OBL_END	0x280FF	164095	
H_OBR_START	0x28100	164096	OBR_Size = 57600
H_OBR_END	0x361FF	221695	
	0x36200	221696	40448 Words
	0x3FFFF	262143	*Reserved*

A storage for CDFS Table which is decoded by S5L9276 is needed for Micom to access. CDFS Table also stored in OBR(Output Buffer Right Channel) and OBL(Output Buffer Channel). S5L9276 provides memory map switching mechanism which enables of the OBR(Output Buffer Right Channel) Map between CDFS decoding and decoding modes. In CDFS decoding mode OBR and OBL are allocated outside of location of them in MP3 decoding mode to keep the CDFS table does not overlap the audio output buffer. Micom can access CDFS Table any time if necessary.

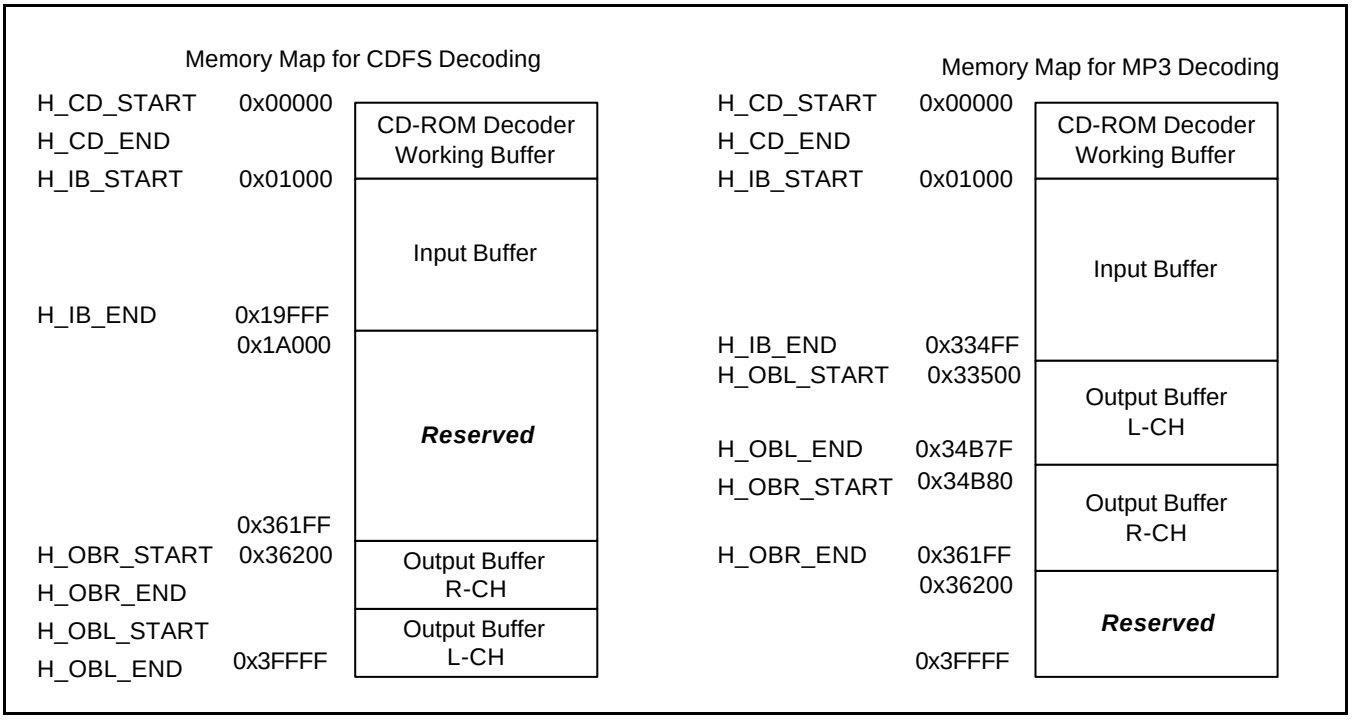


Figure 11. Memory Map Configuration for 4Mbit DRAM

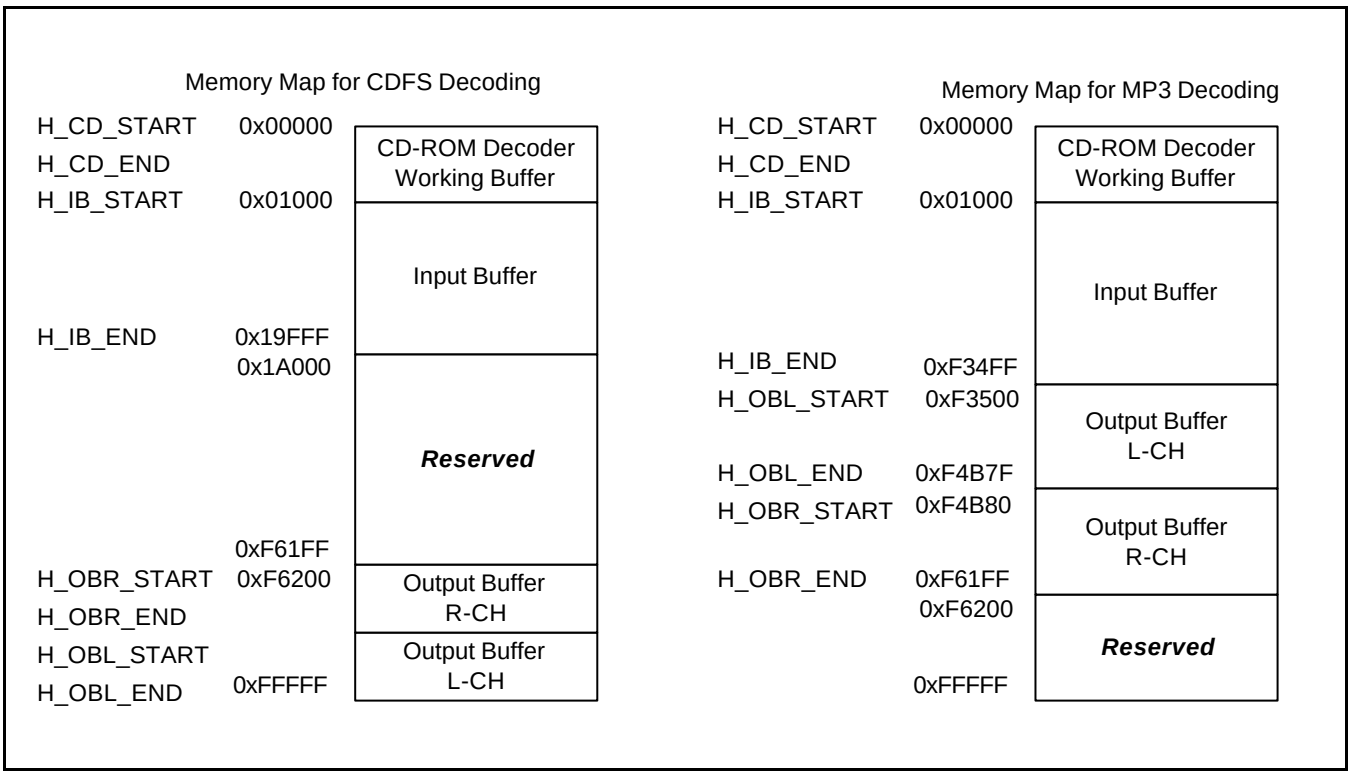
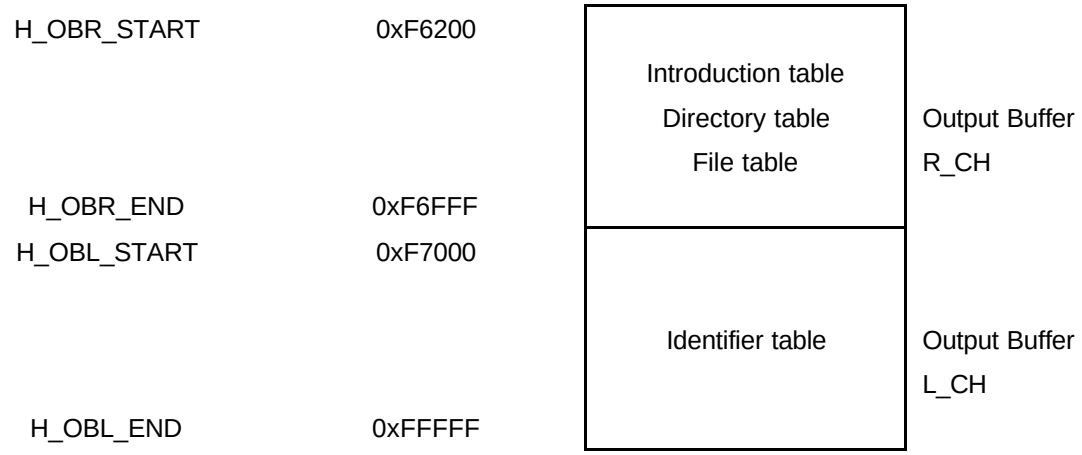


Figure 12. Memory Map Configuration for 16Mbit DRAM

Data Structure of CDFS Table in DRAM

Data Structure of CDFS Table divided into four area : The Introduction Table Area, Table Area, File Table Area and Identifier Table Area. According to Figure , is a typical configuration of DRAM, Output Buffer R-CH and Output Buffer L-CH are to store all CDFS Tables when S5L9276 is in the CDFS decoding mode. The Area, Directory Table Area and File Table Area are located in the Output R-CH. The Identifier Table Area is located in the Output Buffer L-CH.



Introduction Table

Table consists of 4 words (1 word = 16bits). This Table is located in the top the Output Buffer R-CH.

Address	Contents (16 bits)
36200	Total number of directories in a CD
36201	Total number of MP3 files in a CD
36202	Total number of directories which contains any MP3 file in a CD
36203	The directory number which contains the 1'st MP3 file in the whole directory path. The directory number is assigned for each directory in the order of sequence in the file system structure.

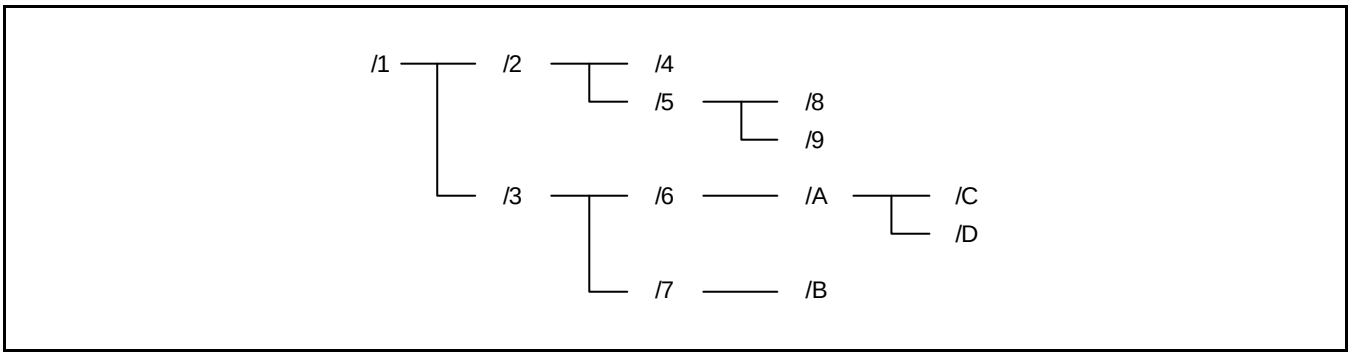
Directory Table

Directory Table follows the Introduction Table and comprises of consecutive directory records. There are as many directory records as the total number of directories in a table. Each directory record consists of 6 words as following.

Address	Contents (16 bits)
36204+6i	The 1'st MP3 file number in this directory. ***(if there is no MP3 files in this directory, this represents the 1'st MP3 file number in next directory)***
36205+6i	The total number of MP3 files in this directory ***(Zero if there is no MP3 files in this directory.)***
36206+6i	Directory identifier length
36207+6i	Parent directory number
36208+6i	Sub directory number
36209+6i	Next directory number

i : 0 — (total number of directories-1)

All directories in a CD are given directory number which is a series of number from 1 to number of the total directory count. Directories has no MP3 files also given number and included in the directory table. Therefore root directory is always directory number 1. An explanation is given below about the relationship between directory, sub directory and next directory with example :



directory number	1	2	3	4	5	6	7	8	9	A	B	C	D
parent directory	1	1	1	2	2	3	3	5	5	6	6	A	A
sub directory	**1**	4	6	4	8	A	7	8	9	C	B	C	D
next directory	1	3	2	5	4	7	6	9	8	B	A	D	C

File Table

File Table follows the Directory Table and comprises of consecutive file records. In the table, there are as many file records as the total number of MP3 file. Each file record of 6 words as following.

Address	Contents			
36204 + Nd*6 +6j	M		S	
36204 + Nd*6 +6j +1	0x00		F	
36204 + Nd*6 +6j +2	L8	L7	L6	L5
36204 + Nd*6 +6j +3	L4	L3	L2	L1
36204 + Nd*6 +6j +4	MP3 file identifier length			
36204 + Nd*6 +6j +5	MP3 file type			

Nd : total number of directories
j: 0 — (Nf-1) , **Nf** = total number of MP3 files

There is no file record for a non-MP3 file.

M, S, and F are the values indicating 1 sector before to the actual sector address beginning of a file. A file length is described as 8 hex digits (L8 — L1). The length represented is FFFFFFFF.

The value of M, S, and F which are all 0xAA or 0xBB indicates End of File Table data.

Identifier Table

Table is stored in the Output Buffer CH-L. Because the maximum length of or file identifier is 128 bytes both of the identifiers occupy 64(40h) words in DRAM . The directory identifiers comes first and file identifiers follow the directory . The first directory identifier occupies address 37000h — 3703Fh in DRAM. The addresses of each directory identifier (=X) are calculated as following :

X = F7000h + i * 40h , i : 0 — (Nd - 1)

The start addresses of each file identifiers (=Y) are calculated as following :

Y = F7000h + (nd * 40h) + j * 40h , j = 0 — (Nf - 1)

Boot Process Programming

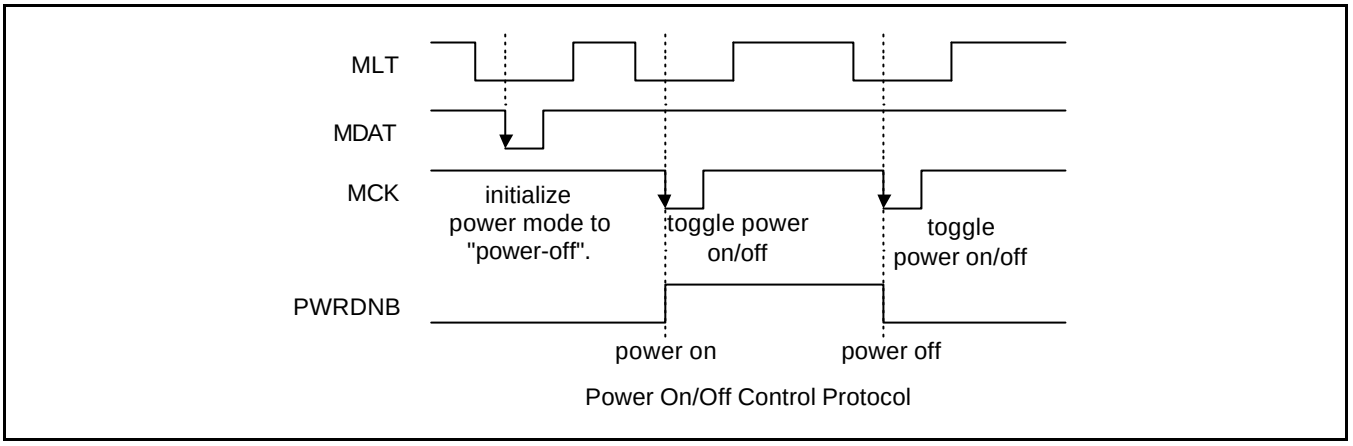
1. Power on CD-MP3 IC

#initial i_MLT=i_MDAT=i_MCK=HIGH
#25ns(min) i_MLT <= LOW
#25ns(min) i_MDAT <= LOW
#25ns(min) i_MDAT <= HIGH
#25ns(min) i_MLT <= HIGH

When the system is powered-on and the "power-on reset" comes, Micom should set the of MLT, MCK, and MDAT to 1'b1. When the MLT is low and the MDAT goes to low, the S5L9276 enters to "power-off" mode. Make sure to initialize the power mode to "power-off" mode at first.
And then the power-on process shown below is the next process required for S5L9276 to be powered on.

#initial	i_MLT=i_MDAT=i_MCK=HIGH
#25ns(min)	i_MLT <= LOW
#25ns(min)	i_MCK <= LOW
#25ns(min)	i_MCK <= HIGH
#25ns(min)	i_MLT <= HIGH

At every supply of MCK pulse (active LOW) the mode is toggled between power-on and -off.



Power On/Off Control Protocol

2. S/W reset

Send Software Reset to CD-MP3 by writing to H_SOFT_RST(8'hE0) with 8'bxxxxxx01. After several system cycles Software Reset automatically cleared. **Make sure that S/W reset should be asserted twice with the time interval of 250ms.** (PLL is reset in the first S/W reset, and wait for 250ms to settle the PLL frequency and after that, assert second S/W reset to accomplish the S5L9276 reset.)

3. enable DRAM interface output drivers

H_DRAMIF_NOE	(8'hA7)	* 8'b0xxxxxxx

4. configuration of ckgUnit

To configure ckgUnit to Mode1 44.1kHz, for example,

1. Enter to SLEEP mode
2. Configure PLL

H_PLL0_P0	(8'hD0)	* 8d'19
H_PLL0_M0	(8'hD1)	* 8d'40
H_PLL0_S0	(8'hD2)	* 8d'0
H_PLL0_P1	(8'hD3)	* don't care
H_PLL0_M1	(8'hD4)	* don't care
H_PLL0_S1	(8'hD5)	* don't care
H_CKG_DIV_XY	(8'hD6)	* don't care
H_CKG_CMD_0	(8'hD7)	* 8d'0

3. Wait longer than 250ms.
4. Exit from SLEEP mode

5. Set DAC Type

H_DAC_TYPE	(8'hB0)	*8'h91 for DAC in S5L9288

6. Set CDP Type

H_INPIF_W	(8'hB1)	* 8'h72	// for SAMSUNG CD-DSP chip
H_HEAD_W	(8'hB2)	* 8'h18	// for MODE1 FORM1
H_ECC_EN	(8'hB7)	* 8'bxxxxxxx1	// Enable ecc

7. enable DAC interface output drivers and set type of DAC data array to MSB-first

H_DACIF_nOES	(8'hC0)	* 8'b00xxxxxx

8. set DRAM refresh interval

H_REFRESH_INTERVAL	(8'hA6)	* 8'bxxxxxx00

We can select one of the four preset refresh interval value.

9 Set DRAM Type (8'hAC) *8'b00000000

0x00 : 4Mbit DRAM
0x02 : 16Mbit 2Kref DRAM
0x03 : 16Mbit 4Kref DRAM

CDFS Decode Process Programming

1. Boot Process
2. Set Memory Map Address for File Table

(Set map for output buffers as following, as an example for 16M DRAM:)

H_OBL_START_L	(8'h9C)	*8'h00
H_OBL_START_M	(8'h9B)	*8'h70
H_OBL_START_H	(8'h9A)	*8'hXf
H_OBL_END_L	(8'h9F)	*8'hFF
H_OBL_END_M	(8'h9E)	*8'hFF
H_OBL_END_H	(8'h9D)	*8'hXf
H_OBR_START_L	(8'hA2)	*8'h00
H_OBR_START_M	(8'hA1)	*8'h62
H_OBR_START_H	(8'hA0)	*8'hxf
H_OBR_END_L	(8'hA5)	*8'hff
H_OBR_END_M	(8'hA4)	*8'hff
H_OBR_END_H	(8'hA3)	*8'hff

We must note that upper 4 bits of H_OBR_END_H should be 1111 to indicate end of memory map transmission.

3. Wait for Interrupt

When interrupted read H_INT_READ register to identify interrupt type.

H_INT_READ	(8'h51)	* 8'bxxx010xx that indicates re-map done successfully.

4. Check CD-ROM format and if it is mode2-form2 send a command "8'h0D" .

H_SSPINT	(8'h80)	* 8'h0D Mode2Form2

S5L9276 regards files with extension of ".mp2" or ".mp3" as MP3 audio files by default and generates File System Table which includes information of files with those file extensions only. But files with the extension of ".mpg" may also be regarded as MP3 audio files by sending a command "8'h0F".

H_SSPINT	(8'h80)	* 8'h0F FATmpAllOK

5. Send a Command DECODE_CDFS.

H_SSPINT	(8'h80)	* 8'h02 is DECODE_CDFS

This cause interrupting ssp1611 for ssp1611 to know CD-ROM sectors with CDFS Table will be put into the input buffer.

6. Transfer CD-ROM sectors to S5L9276 in the way described in Section transferring input bit stream.
7. During the sector transfer in step 5, check if *"Sending MSF"* Interrupt has been received.

H_INT_READ	(8'h51)	*8'bxxx001xx : **Sending MSF Interrupt** (See section skip function)

After receiving interrupt, Micom should get next sector address by reading the registers below :

H_OUT1_LOW	(8'h01)	* S
H_OUT1_HIGH	(8'h02)	* M
H_OUT2_LOW	(8'h03)	* F

If M, S and F read are all AAh or BBh, it indicates CDFS decoding has been completed. If they are all AAh it indicates that this CD is not in a juliet format. If they are all BBh it indicates that CD is in joliet format CD. If M, S and F are not all AAh or BBh go to step 8.

8. Transfer CD-ROM sectors to S5L9276 in the way described in Section transferring input bit stream with the start sector address MSF.
9. Repeat 6,7,8.
10. During step 9, When there is an error in the sector received i.g. if the file system is not in accordance with ISO9660, S5L9276 asks the sector again to the Micom. if this happens repeatedly, this means that there is a non-recoverable error in the . In this case micom sends FATnextDIR command for S5L9276 to give up decoding the file system information for the current search path and it's sub-tree. Receiving this command, S5L9276 asks Micom new sector for the next search path of the file system.

H_SSPINT	(8'h80)	* 8'h0E FATnextDIR

When CDFS decoding is completed successfully, decoded CDFS tables are stored in such a way described in **Section. Data Structure of CDFS Table in DRAM** . Micom can read the tables any time. In the Identifier Table, 64 words are allocated to directory or file identifiers. Because 2 bytes are required to represent 1 character Joliet format, maximum 64 characters can be stored in each 64 words of an identifier. in DOS format, because 1 character is represented by 1 byte code, maximum 128 can be stored in each 64 words of identifier. Micom should know if a CD is Joliet format or not to recognize the identifier correctly.

TAG DECODE PROCESS

ID3 TAG Version 1.xx

1. Boot Process
2. **Re-map : Configure Memory Map**
3. **Transfer the last sector of an MP3 file to S5L9276.**
4. **Write a sector size to registers IN1.**
5. Issue the command DECODE_TAG.
6. Waits interrupt 8'bxxx001xx

   H_INT_READ (8'h51) *8'bxxx001xx : DECODE_TAG Acknowledge
7. Read OUT1. If the content of OUT1 is 0xDD01, it indicates there is no TAG in the sector. If the TAG information is found, the content of OUT1 is DRAM of the start of TAG information.
8. If TAG is found, Micom reads DRAM to decode the TAG ins formation.

ID3 TAG Version 2.xx

1. Boot Process
2. **Remap : Configure Memory Map**
3. **Transfer the first sector of an MP3 file to S5L9276.**
4. TAG Information follows ID3 characters therefore Micom can read 3 bytes of the first to decide if there is TAG information in the MP3 file.
5. Micom reads DRAM to decode TAG information.

MP3 decode process

1. Boot Process
2. **Re-map : set memory map address for output buffer (returns memory map to MP3** mode from CDFS decode mode by writing back the default value for output buffer channel.)

H_OBR_START_L	(8'hA2)	*8'h00
H_OBR_START_M	(8'hA1)	*8'h81
H_OBR_START_H	(8'hA0)	*8'hx2
H_OBR_END_L	(8'hA5)	*8'hff
H_OBR_END_M	(8'hA4)	*8'h61
H_OBR_END_H	(8'hA3)	*8'hf3

We must note that upper 4 bits of H_OBR_END_H should be 1111 to indicate end of map transmition.

3. Wait for Interrupt

   H_INT_READ (8'h51) * 8'bxxx010xx that indicates remap done successfully.

wait for interrupt from ssp1611 that indicates CD-MP3 chip has successfully the remap sequence. When Micom reads H_INT_READ register the interrupt be cleared automatically.

4. Send Command DECODE_MP3.

H_SSPINT	(8'h80)	* 8'h03 is DECODE_MP3

5. Micom reads CDFS Table and select a music to be play.
6. Micom set Total_Sector_Number as follows. Total_Sector_Number is a value with 20bit range.

H_IN_XTRA	(8'h83)	: XYZW XXXX Y : if FF(Fast Forward) state when going to next song, set Y=1 Z : if FB(Fast Backrward) state when going to next song, set Z=1 W: if CD-ROM format is Form2, W=1 XXXX: Total_Sector_Number[19:16]
H_IN_HIGH	(8'h82)	: Total_Sector_Number[15:8]
H_IN_LOW	(8'h81)	: Total_Sector_Number[7:0]

7. Transfer CD-ROM sectors to S5L9276 in the way described in Section transferring input bitstream.
8. S5L9276 starts decoding of input bitstream. When audio sampling frequency information the bitstream header S5L9276 writes it to the register H_OUT1_LOW and interrupt . And then S5L9276 stops it's decoding. S5L9276 will resume it's decoding after configures audio clock frequency. When interrupted from S5L9276 for audio frequency information transfer, Micom reads the sampling frequency information in H_OUT1_LOW (8'h01) and set audio clock in S5L9276.

H_INT_READ	(8'h51)	* 8'bxxx011xx that indicates sending audio sampling frequency code
H_OUT1_LOW	(8'h01)	* frequency code

Sampling Frequency Information
000 : 44.1 kHz
001 : 48 kHz
010 : 32 kHz
011 : Not Used
100 : 22.05 kHz
101 : 24 kHz
110 : 16 kHz

After setting audio clock frequency Micom send a command (0x23) to S5L9276 to indicate clock frequency setting completed successfully.

H_SSPINT	(8'h80)	* 8'h23 is completion of frequency setting

9. When both of input buffer and output buffer are empty it means that end-of-song S5L9276 is in IDLE state. Micom can see when input buffer becomes empty S5L9276 interrupts Micom when input buffer state has been changed. Micom can a certain time until output buffer becomes empty when Micom can conclude that -of-song reached. Therefore Micom should keep in mind the last sector has been sent S5L9276 and from that time it checks input buffer state at each interrupts.

Skip Function

1. Micom controls servo system to stop feeding CD data to S5L9276.
2. Micom send a command "Pause". (This is for the purpose of audio fade-out.)

   H_SSPINT (8'h80) * 8'h07 (Pause)
3. Follow the sequence from step2 (Re-map) of the "MP3 decode process".

Fast Forward Function

1. Micom writes "number of frame to be skipped" to H_IN_LOW , and "number of frames be decoded" to H_IN_HIGH.
2. Micom send a command FAST FORWARD.
3. Micom send a command REPLAY to return to normal play.

Fast Backward Function

At starting Fast Backward, Input Buffer could contain less than 10 sec of input bitstream. Input Buffer should be empty to reverse without delay caused by this input bitstream.

1. Micom send a command "Input Buffer Clear"

   H_SSPINT (8'h80) * 8'h06 is Input Buffer Clear

2. Micom determine Skip_Sector_Number and Dump_Sector_Number.
   Micom writes ratio of Skip_Sector_Number and Dump_Sector_Number to H_IN_LOW
   (that is Skip_Sector_Number/Dump_Sector_Number) and writes 0 to H_IN_HIGH.
3. Micom send a command "FAST BACKWARD".

   H_SSPINT (8'h80) * 8'h0A is FAST BACKWARD.
4. Micom waits for interrupt

   H_INT_READ (8'h51) * 8'bxxx110xx that indicates input buffer cleared.
   After receiving interrupt, Micom should get Rewinded_Sector_Number by reading the shown below :

   H_OUT1_LOW (8'h01) *
   H_OUT1_HIGH (8'h02) *
5. Micom convert Rewind_Sector_Num to Rewind_MSF
6. Micom update Dump_Start_MSF by subtracting Dump_Curr_MSF with Rewind_MSF
7. Micom start to dump at Dump_Start_MSF repeating dump and skip. dump as much as Dump_Sector_Number and skip as much as Skip_Sector_Number.
8. Micom send a command REPLAY to return to normal play.

Get Decoding Time for Display

Wait interrupt continuously during decoding process for time display.

H_INT_READ	(8'h51)	*8'bxxx111xx that indicates S5L9276 send Current_Decoding_Sec

S5L9276 send this interrupt about twice or three times per second. The exact period is determined by sampling frequency. but Micom doesn't need to know the period becase send Current_Decoding_Sec (in second) when interrupt. Micom only have to Current_Decoding_Sec. After receiving interrupt, Micom should get Current_Decoding_Sec (hexa value) by reading the registers shown below :

H_OUT1_LOW	(8'h01)	*
H_OUT1_HIGH	(8'h02)	*

Micom would better display Current_Decoding_Sec in the format of minute: second than second.

Set Current Decoding Time with Current Sector Number

During Fast Forward or Fast Backward, S5L9276 cannot send correct decoding time of skipped frames. But Micom can update decoding time correctly by sending number currently being decoded.

1. Micom writes lower byte of "sector number currently decoded" to H_IN_LOW and higher byte of "sector number currently decoded" to H_IN_HIGH.
2. Micom send a command "Set Current Decoding Time with Sector Number".

H_SSPINT	(8'h80)	* 8'h11 is "Set Current Decoding Time with Sector Number".

Form that time, S5L9276 send new Current_Decoding_Sec converted from "the sector currently decoded" set by Micom.

Compute Total Time

Total_Sector_Number was set in the way, Micom can call "Compute Time" to get total play time.

1. Micom send command "Compute Total Time".

H_SSPINT	(8'h80)	* 8'h10 (Compute Total Time)

2. Micom wait interrupt.

H_INT_READ	(8'h51)	*8'bxxx110xx that indicates S5L9276 send total time in second

After receiving interrupt, Micom should get Total_Sec (hexa value) by reading the shown below :

H_OUT1_LOW	(8'h01)	*
H_OUT1_HIGH	(8'h02)	*

Micom would better display Total_Sec in the format of minute: second than second.

Display CDFS decoding state

Micom can display how much directories and mp3 files is decoded.
In CDFS decoding process, after receiving **Sending MSF** interrupt, Micom should get next sector address by reading the registers shown below

H_OUT1_LOW	(8'h01)	* S
H_OUT1_HIGH	(8'h02)	* M
H_OUT2_LOW	(8'h03)	* F

And then,
1. Micom send command "FAT decode State" after saving MSF record.

H_SSPINT	(8'h80)	* 8'h19 (FAT decode State)

2. Micom read decoding states

H_OUT1_LOW	(8'h01)	* No. of song low
H_OUT1_HIGH	(8'h02)	* No. of song high
H_OUT2_LOW	(8'h03)	* No. of directory

Interrupt handling

There is one signal line for interrupt from S5L9276 to Micom (MINT). When Micom is interrupted by S5L9276, it should read the interrupt source register in CD-MP3 (H_INT_READ 8'h51) which indicates the interrupt type to identify which interrupt service should be done.

H_INT_READ

b7	b6	b5	b4	b3	b2	b1	b0

b7 : Not Used. (always LOW.)
b6 - b5 : cdrUnit Interrupt Source
b4 - b2 : dspUnit Interrupt Source
b1 - b0 : memUnit Interrupt Source

cdrUnit Interrupt Source Description :
xx1 : Header Error (When S5L9276 detects error in header of a CD-ROM sector this interrupt is set.)
x1x : Sector Address Decoded Out of Range (Discard this in current version of S5L9276.)
1xx : EDC Error

dspUnit Interrupt Source Description :
001 : Sending M.F.S
This interrupt bits are set when S5L9276 expects to get CD-ROM sectors which is in jumped address from the current sector address during the CDFS decoding. (End Of CDFS Decoding is indicated by M.F.S = all zero.)
010 : End of REMAP
011 : Sending Audio Sampling Frequency Code
100 : reserved
101 : Sending Output Buffer Left Channel Empty Signal
110 : End of Input Buffer Clear / Sending Total Time in second
111 : Sending Decoding Time for Display

memUnit Interrupt Source Description :
01 : Dump-End
10 : Input Buffer State
11 : reserved for future use.

Command Set Description

Micom can send a command to S5L9276 by writing a command ID to H_SSPINT register.

H_SSPINT (8'h80)

b7	b6	b5	b4	b3	b2	b1	b0

b7 — b0 : Host Command ID

Host Command IDs

0x01 : DECODE_TAG
0x02 : DECODE_CDFS
0x03 : DECODE_MP3
0x04 : End of Input, indicates last data of MP3 bitstream for current music has been supplied.
0x05 : An Interrupt indicating that Micom completed audio clock frequency setting in response of audio sampling frequency information which is sent to Micom by ssp1611. ssp1611 should wait this interrupt to continue decoding after audio sampling frequency has been changed. In addition to this interrupt, ssp1611 should also wait until the output buffer becomes empty to ensure audio DAC responds correctly at the boundary of different sampling frequency boundary.
0x06 : Clear Input Buffer (This command should be issued before Fast Backward command.)
0x07 : Pause (ssp1611 stop reading by setting Flag for difUnit interrupt service routine not to read OBrChannel and send MUTE data to difUnit. When Paused ssp1611 need to fade out the audio.)
0x08 : Replay (ssp1611 clears the Flag for difUnit interrupt service routine resume to read the OBrChannel. ssp1611 need to fade in the audio.)
0x09 : Fast Forward
0x0A : Fast Backward
0x0B : Soft Mute (ssp1611 keeps enabling OBrChannel read but discard the data. Send MUTE data to difUnit. Needs to fade out.)
0x0C : Soft Mute Off
0x0D : FAT Mode2Form2
0x0E : FAT next Dir
0x0F : FAT mp AllOK
0x10 : Compute Total Time
0x11 : Set current decoding time with sector number
0x12 : Repeat start
0x13 : Repeat end
0x14 : Repeat reset
0x15 : Don't use
0x16 : Don't use
0x17 : Don't use
0x18 : FAT joliet NO(read only ISO9660 format)
0x19 : Display decoding state(No. of song , No. of directory)
0x1A : Display decoding state(CD format , Total directory)
0x1B : FAT micom Error
0x1C : FAT micom Exit
0x1d : Don't use
0x1e : Don't use
0x1f : Don't use
0x20 : Don't use
0x21 : Send Header Inform
0x22 : MPEG2 Interpolation On
0x23 : MPEG2 Interpolation Off
0x24 : FAT Check Easy
0x25 : Quick FAT
0x26 : Quick FAT next directory DRAM Interface

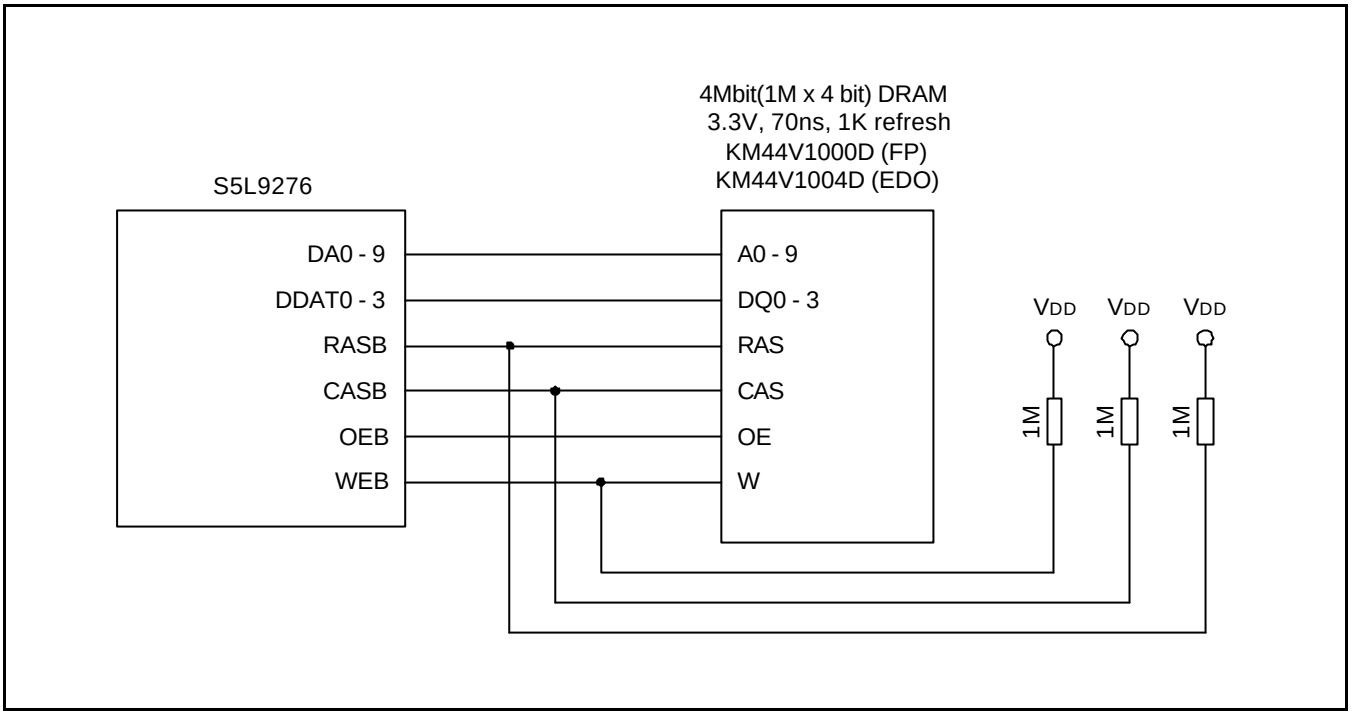


Figure 13. Interface with 1Mx4bit DRAM

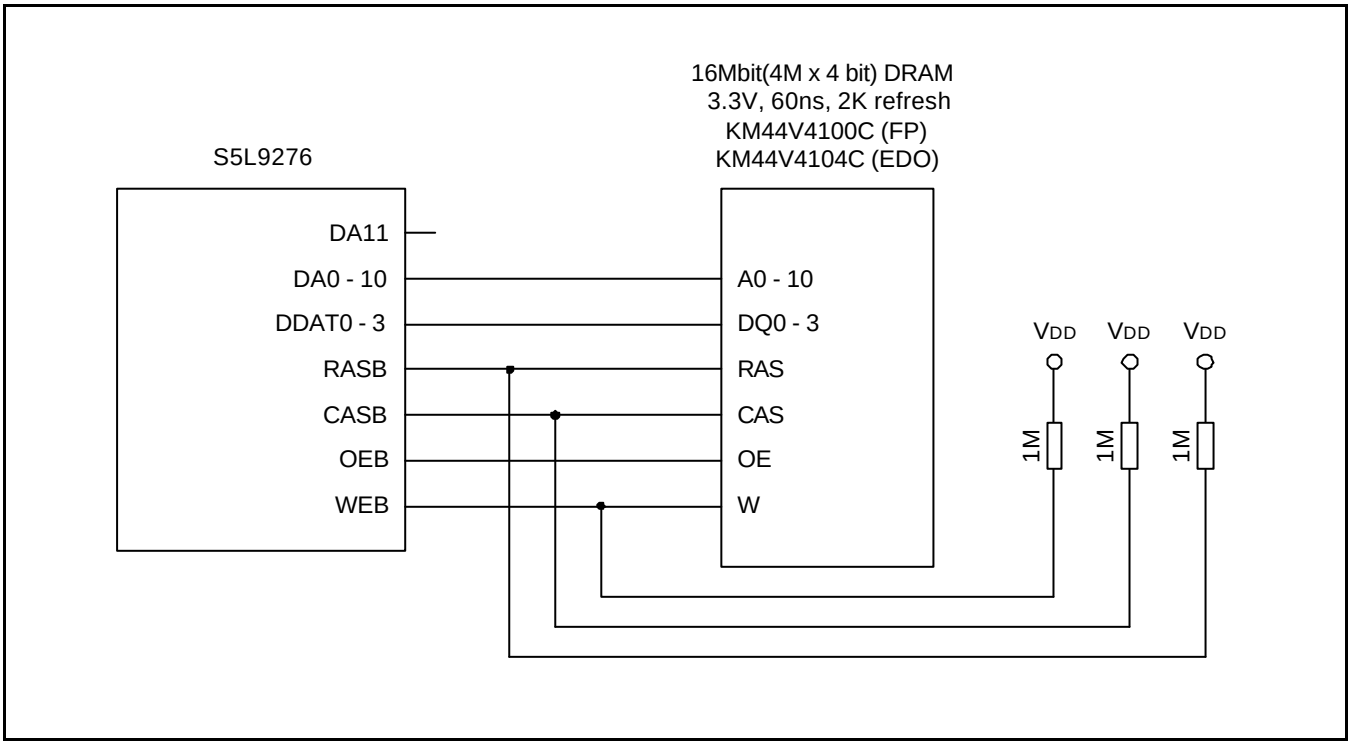


Figure 14. Interface with 4Mx4bit DRAM Type (2K ref. product)

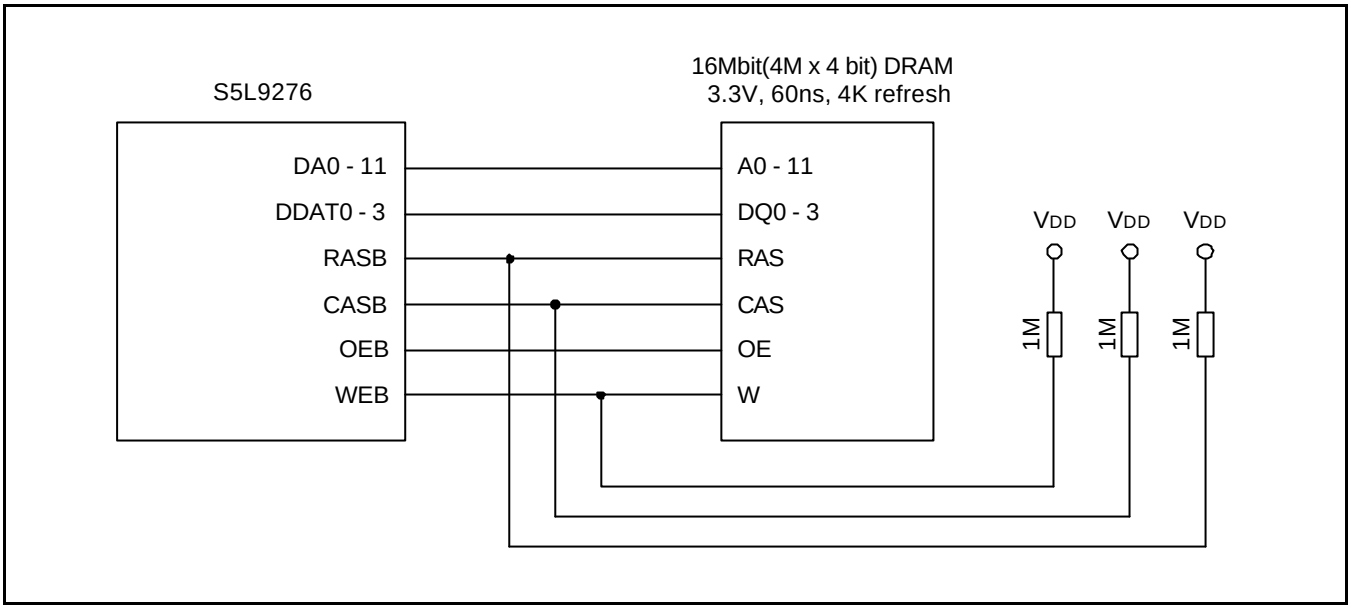


Figure 15. Interface with 4Mx4bit DRAM Type B (4K ref. Product)

NOTES