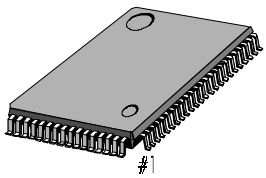
INTRODUCTION

The S5L9284D is a CMOS integrated circuit designed for the digital audio signal processor.
It is a monolithic IC with built-in 16K SRAM and DPLL.
It is similar to S5L9283 IC but has advanced error correction ability.

80–QFP–1420C



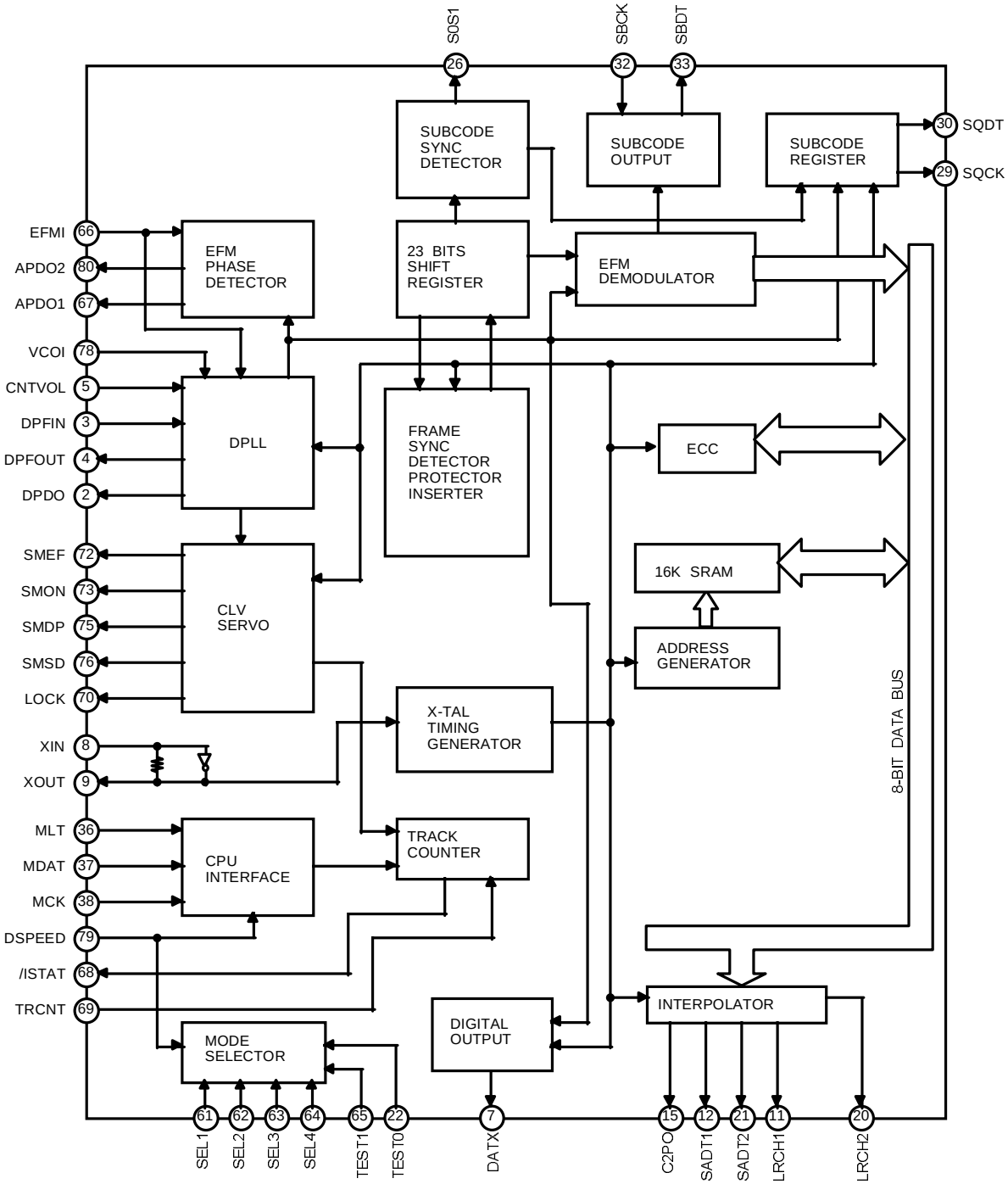
FEATURES

- EFM data demodulation
- Built-in frame sync detection, protection and insertion circuit
- C1: 2 error correction; C2: 4 erasure correction
- Interpolation
- Subcode data serial output
- CLV servo controller
- Tracking counter
- MICOM interface
- Built-in 16K SRAM
- Digital audio output (TX)
- Built-in digital PLL and analog PLL
- Double speed function
- Single power supply: +5V

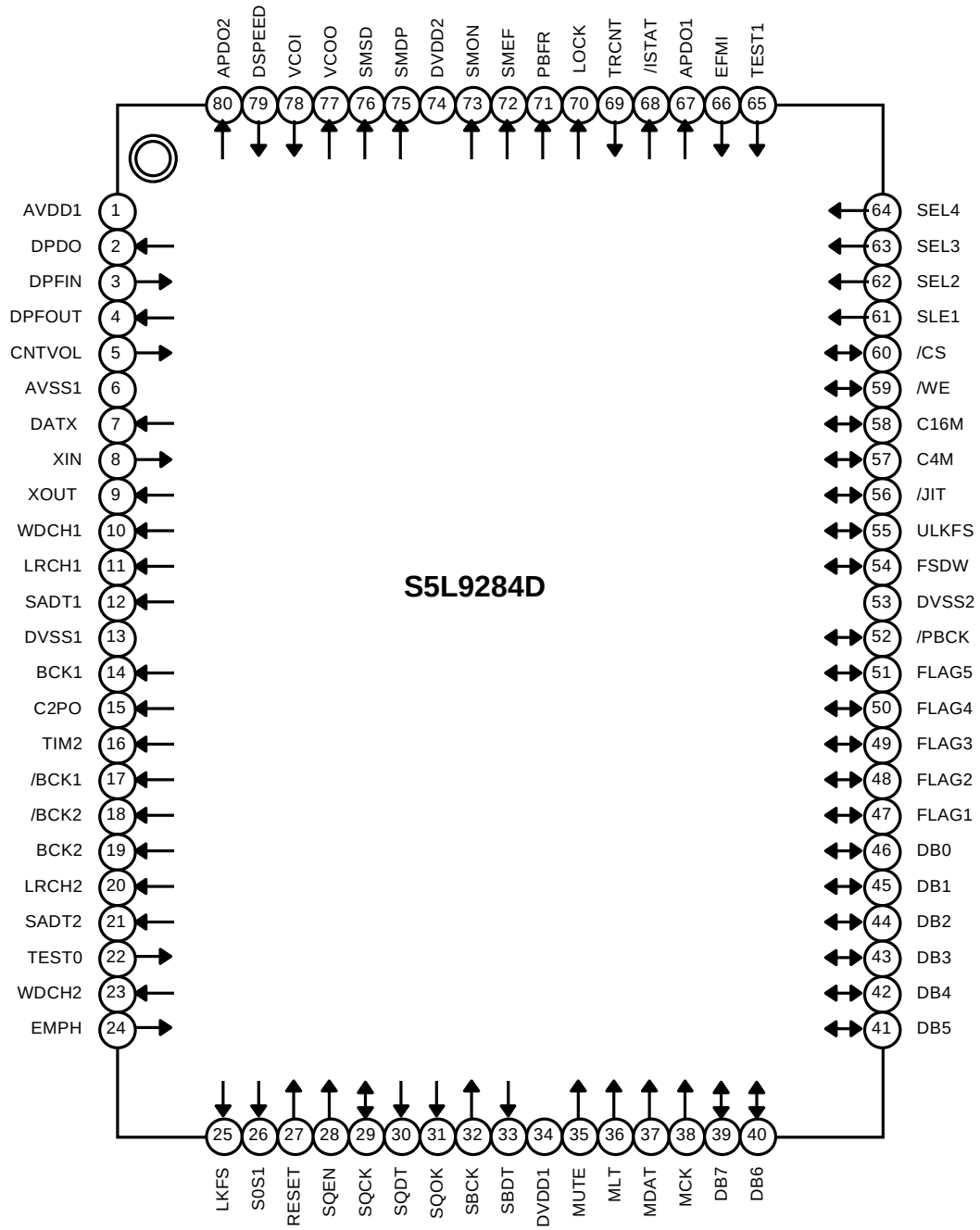
ORDERING INFORMATION

Device	Package	Operating Temperature
S5L9284D01-Q0R0	80-QFP-1420C	–20°C to +75°C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	AV_{DD1}	–	Analog supply voltage 1
2	DPDO	O	Charge pump output for master PLL
3	DPFIN	I	Filter input for master PLL
4	DPFOUT	O	Filter output for master PLL
5	CNTVOL	I	VCO control voltage for master PLL
6	AV_{SS1}	–	Analog ground 1
7	DATX	O	Digital audio output
8	XIN	I	X-tal oscillator input (16.9344MHz / 33.8688MHz)
9	XOUT	O	X-tal oscillator output
10	WDCH1	O	Word clock of 48 bits/slot
11	LRCH1	O	Channel clock of 48 bits/slot
12	SADT1	O	Serial audio data output with 48 bits/slot
13	DV_{SS1}	–	Digital ground 1
14	BCK1	O	Serial audio data bit clock for 48 bits/slot
15	C2PO	O	C2 pointer for serial audio data
16	TIM2	O	Normal or double speed control output pin
17	/BCK1	O	Inverted clock of BCK1
18	/BCK2	O	Inverted clock of BCK2
19	BCK2	O	Serial audio data bit clock for 64 bits/slot
20	LRCH2	O	Channel clock for 64 bits/slot
21	SADT2	O	Serial audio data output with 64 bits/slot
22	TEST0	I	Test input pin (“L”: normal, “H”: test)
23	WDCH2	O	Word clock of 64 bit/slot
24	EMPH	O	Emphasis/Non-emphasis output (“H”: Emphasis)
25	LKFS	O	The lock status output of frame sync
26	S0S1	O	Output of subcode sync signal (S0 + S1)
27	RESET	I	System reset at Low
28	SQEN	I	SQCK control input (“L”: internal clock, “H”: external clock)
29	SQCK	I/O	Subcode-Q data bit clock
30	SQDT	O	Subcode-Q data serial output
31	SQOK	O	The CRC check result signal output of subcode-Q

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
32	SBCK	I	Subcode data bit clock
33	SBDT	O	Subcode serial data output
34	DV_{DD1}	–	Digital supply voltage 1
35	MUTE	I	Mute control input (“H”: Mute ON)
36	MLT	I	Latch signal input from micom
37	MDAT	I	Serial data input from micom
38	MCK	I	Serial data transferring clock input from micom
39	DB7	I/O	Data port 7 for external SRAM (MSB)
40	DB6	I/O	Data port 6 for external SRAM
41	DB5	I/O	Data port 5 for external SRAM
42	DB4	I/O	Data port 4 for external SRAM
43	DB3	I/O	Data port 3 for external SRAM
44	DB2	I/O	Data port 2 for external SRAM
45	DB1	I/O	Data port 1 for external SRAM
46	DB0	I/O	Data port 0 for external SRAM (LSB)
47	FLAG1	I/O	Monitoring output for C1 error correction (RA0)
48	FLAG2	I/O	Monitoring output for C1 error correction (RA1)
49	FLAG3	I/O	Monitoring output for C2 error correction (RA2)
50	FLAG4	I/O	Monitoring output for C2 error correction (RA3)
51	FLAG5	I/O	C2 decoder flag (“H”: when the processing C2 code is in impossible correction status /RA4)
52	/PBCK	I/O	VCOI/2 clock (4.3218/8.6436 MHz), when locked in with EFMI (RA5)
53	DV_{SS2}	–	Digital ground 2
54	FSDW	I/O	Unprotected frame sync (RA6)
55	ULKFS	I/O	Frame sync protection status (RA7)
56	/JIT	I/O	RAM overflow and underflow status (RA8)
57	C4M	I/O	4.2336 MHz clock output (RA9)
58	C16M	I/O	16.9344 MHz clock output (RA10)
59	/WE	I/O	Write enable output to external SRAM
60	/ CS	I/O	Chip select output to external SRAM
61	SEL1	I	X-tal selection terminal (“L”:16.9344 MHz, “H”: 33.8688 MHz)
62	SEL2	I	DPLL selection terminal (“L”: DPLL, “H”: APLL)

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
63	SEL3	I	CD-ROM selection terminal (“L”: CDP, “H”: CD-ROM)
64	SEL4	I	SRAM selection terminal (“L”: internal SRAM, “H”: external SRAM)
65	TEST1	I	Test terminal (“L”: normal, “H”: test)
66	EFMI	I	EFM data input
67	APDO1	O	Charge pump output for analog PLL
68	/ISTAT	O	The internal status output
69	TRCNT	I	Tracking clock input signal
70	LOCK	O	Output signal of LKFS conditions sampled PBFR/16 (If LKFS is High, lock is High. If the LKFS is sampled Low at least 8 times by PBFR/16, lock is Low)
71	PBFR	O	Write frame clock (Lock : 7.35kHz)
72	SMEF	O	LPF time constant control of the spindle servo error signal
73	SMON	O	ON/OFF control signal for spindle servo
74	DV_{DD2}	–	Digital supply voltage 2
75	SMDP	O	Spindle motor driving output (rough control in the speed mode, phase control in the phase mode
76	SMSD	O	Spindle motor (Velocity control in the phase mode)
77	VCOO	O	VCO output
78	VCOI	I	VCO inut (when in locked status by means of PBFR, it is 8.6436MHz)
79	DSPEED	I	Double speed mode control (“H”: normal speed, “L”: 2-times speed)
80	APDO2	O	Analog PLL charge pump output for double speed mode

NOTES:

1. PBFR: 7.35 kHz Write frame clock produced by data which is being reproduced.
2. /PBCK : Channel bit clock of data which being reproduced.
3. /JIT : Display signal of either RAM overflow or underflow for ± 4 frame jitter margin.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 — + 7.0	V
Input Voltage	V_I	-0.3 — + 7.0	V
Output Voltage	V_O	-0.3 — + 7.0	V
Operating Temperature	T_{OPR}	-20 — + 75	°C
Storage Temperature	T_{STG}	-40 — + 125	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5 V, V_{SS} = 0 V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
High Input Voltage1	$V_{IH\ (1)}$	(Note 1)	$0.7V_{DD}$	–	–	V
Low Input Voltage1	$V_{IL(1)}$	(Note 1)	–	–	$0.3V_{DD}$	V
High Input Voltage2	$V_{IH\ (2)}$	(Note 2)	$0.8V_{DD}$	–	–	V
Low Input Voltage2	$V_{IL\ (2)}$	(Note 2)	–	–	$0.2V_{DD}$	V
High Outut Voltage1	$V_{OH\ (1)}$	I_{OH} = –1mA(Note 3)	V_{DD} – 0.5	–	V_{DD}	V
Low Output Voltage1	$V_{OL\ (1)}$	I_{OL} = 1mA (Note 3)	0	–	0.4	V
High Outut Voltage2	$V_{OH\ (2)}$	I_{OH} = –1mA (Note 4)	V_{DD} – 0.5	–	V_{DD}	V
Low Output Voltage2	$V_{OL\ (2)}$	I_{OL} = 1mA (Note 4)	0	–	0.4	V
High Outut Voltage3	$V_{OH\ (3)}$	I_{OH} = –1mA (Note 5)	V_{DD} – 0.5	–	V_{DD}	V
Low Output Voltage3	$V_{OL\ (3)}$	I_{OL} = 1mA (Note 5)	0	–	0.4	V
Input Leak Current1	I_{LKG1}	V_I = 0 to V_{DD} (Note 6)	–5	–	+ 5	mA
Input Leak Current2	I_{LKG2}	V_O = 0 to V_{DD} (Note 7)	–10	–	+10	mA
Tri-State Output Leak Current	$I_{O\ (LKG)}$	V_I = 0 to V_{DD} (Note 8)	–5	–	+ 5	mA

NOTES:

1. Input Voltage1: All input pins
2. Input Voltage2: All BIDIR pins
3. Output Voltage1: All output pins
4. Output Voltage2: All BIDIR pins
5. Output Voltage 3: All Tri - state output pins
6. Input Leak Current 1: All input pins except for XIN, VCOI
7. Input Leak Current 2: XIN, VCOI
8. Output Leak Current : SMEF, SMDP, SMSD, APDO1, APDO2, DPDO

AC CHARACTERISTICS

A. XIN, VCOI (When the pulse is input to)

(V_{DD} = 5 V, V_{SS} = 0 V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
High Level Pulse Width	$t_{w\,H}$	13	–	–	ns
Low Level Pulse Width	$t_{w\,L}$	13	–	–	ns
Pulse Frequency	t_{CK}	26	–	–	ns
Input High Level	V_{IH}	V_{DD} – 1.0	–	–	V
Input Low Level	V_{IL}	–	–	0.8	V
Rising & Falling Time	t_R, t_F	–	–	8	ns

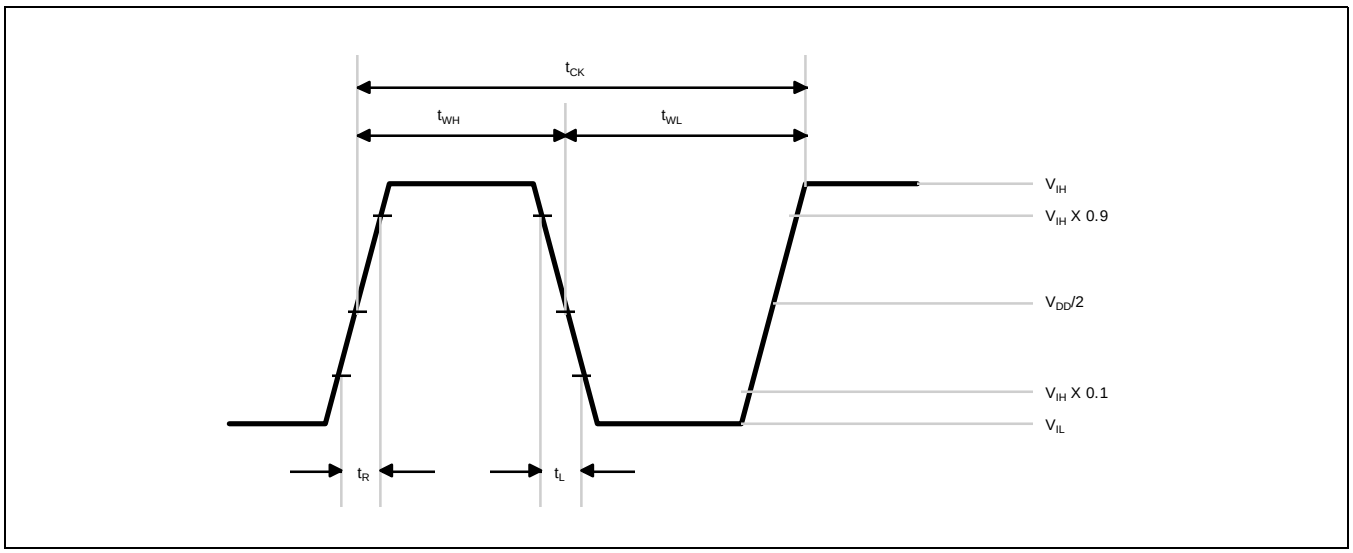


Figure 1.

B. MCK, MDAT, MLT, TRCNT

(V_{DD} = 5 V, V_{SS} = 0 V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	$f_{CK\ 1}$	-	–	1	MHz
Clock Pulse Width	t_W	300	–	–	ns
Setup Time	t_{SU}	300	–	–	ns
Hold Time	t_H	300	–	–	ns
Delay Time	t_D	300	–	–	ns
Latch Pulse Width	t_{WCK1}	300	–	–	ns
TRCNT, SQCK Frequency	$f_{CK\ 2}$	–	–	1	MHz
TRCNT, SQCK Pulse Width	t_{WCK2}	300	–	–	ns

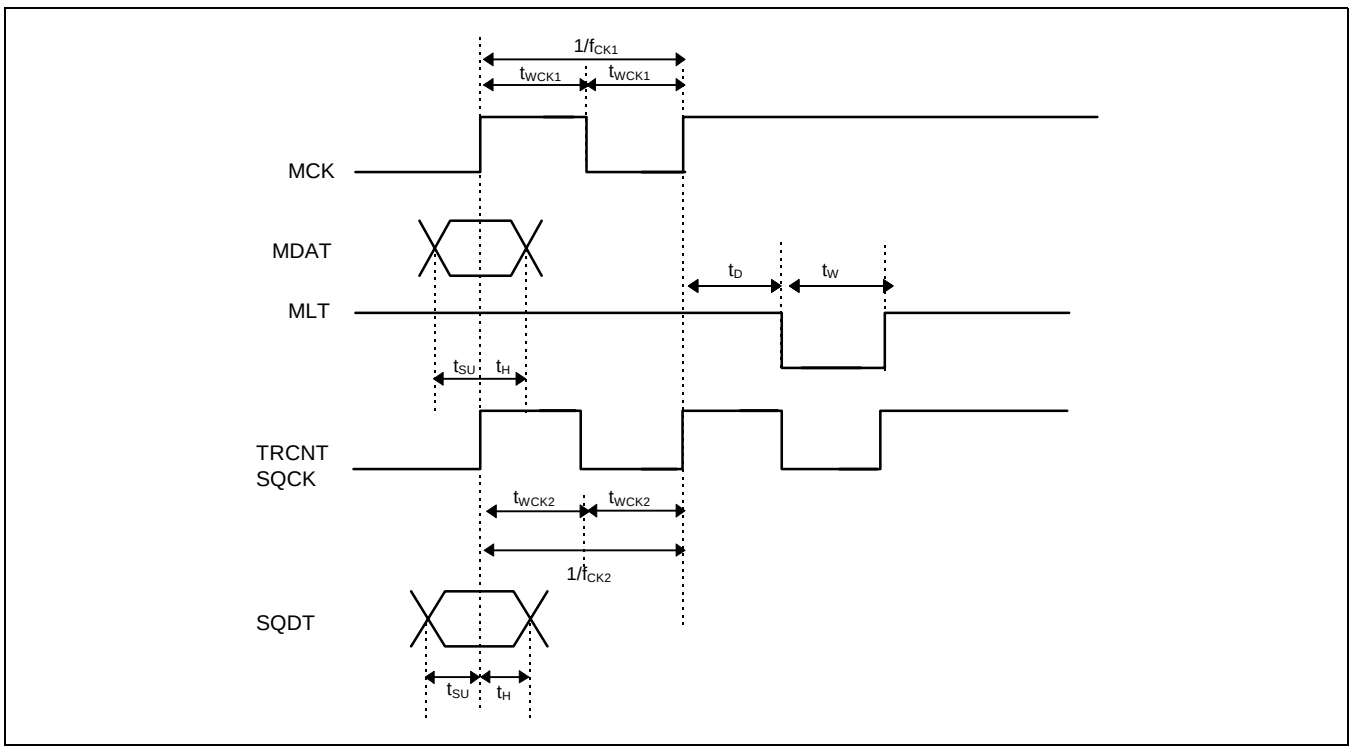


Figure 2.

FUNCTION DESCRIPTION

MICOM INTERFACE

The data input from MICOM is input to MDAT and transported by MCK.
The input signal is loaded to the control register by means of MLT.
The timing chart is as follows.

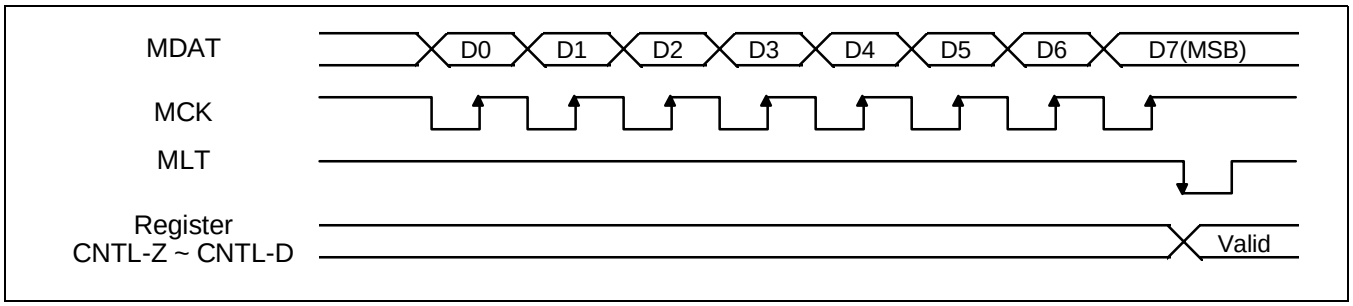


Figure 3. MICOM Data Input Timing Chart

Control Register	Comment	Address D7 — D4	Data				/ISTAT
			D3	D2	D1	D0	Terminal
CNTL-Z	Data Control	1001	ZCMT	HIPD	NCLV	CRCQ	HI-Z
CNTL-S	Frame Sync Protection Attenuation Control	1010	FSEM	FSEL	WSEL	ATTM	HI-Z
CNTL-L	Tracking Counter Lower 4 Bits	1011	TRC3	TRC2	TRC1	TRC0	/Complete
CNTL-U	Tracking Counter Upper 4 Bits	1100	TRC7	TRC6	TRC5	TRC4	/Count
CNTL-W	CLV Control	1101	COM	WB	WP	GAIN	HI-Z
CNTL-C	CLV Mode	1110	CLV Mode				/(Pw ≥ 64)
CNTL-D	Double Speed	1111	–	–	DS1	DS2	HI-Z

CNTL-Z Register

It is a register to control the zero cross mute of audio data, the phase terminal control, the phase servo and having CRCF data in SQDT or not.

	DATA	DATA = 0	DATA = 1
ZCMT	D3	Zero cross mute is OFF	Zero cross mute is ON
HIPD	D2	It operates phase normally	The phase becomes “L” to “Hi-Z”
NCLV	D1	Phase servo is acted by frame sync	Phase servo is controlled by base counter
CRCQ	D0	SQDT output except for SQOK	SQDT = CRCF when S0S1 = “H”

CNTL-S Register

It is a register to control frame sync protection and attenuation.

FSEM	FSEL	FRAME
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	CLOCK
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	– ∞
1	0	– 12
1	1	– 12

CNTL-L, U Register

After the number of tracks that must be counted is input from micom , the data is loaded to the tracking counter by the CNTL-L, U register.

CNTL-W Register

It is a register to control CLV-servo.

	DATA	DATA = 0	DATA = 1	Comment
COM	D3	XTFR/4 and PBFR/4		Phase comparison frequency control during Phase - mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period control during speed or HSpeed-mode
WP	D1	XTFR/4	XTFR/2	Peak hold period control during Speed-mode
GAIN	D0	–12dB	0dB	SMDP gain control during Speed or HSpeed-Mode

CNTL-C Register

Mode	D7-D4	D3-D0	SMDP	SMSD	SMEF	SMON
Forward	1110	1000	H	Hi-Z	L	H
Reverse		1010	L	Hi-Z	L	H
Speed		1110	Speed-mode	Hi-Z	L	H
Hspeed		1100	Hspeed-mode	Hi-Z	L	H
Phase		1111	Phase-mode	Phase-mode	Hi-Z	H
XPHSP		0110	Speed, phase-mode	Hi-Z, Phse-mode	L, Hi-Z	H
VPHSP		0101	Speed, Phase-mode	Hi-Z, Phase-mode	L, Hi-Z	H
Stop		0000	L	Hi-Z	L	L

CNTL-D Register

It is a register to control normal speed mode and double speed mode.

Mode	D7-D4	D3-D0	Comment
Normal	1111	XX00	Normal Speed
Double		XX11	Double Speed

TRACKING COUNTER

This block is used to improve track-jump characteristics. The number of tracks, which must be jumped, is input from micom, and the operating of the count is performed by the TRCNT pulse at the positive edge of MLT. If the number of
tracks is loaded into the register and the CNTL-L is selected, the /COMPLETE signal is output to the /ISTAT terminal,
and if the CNTL-U is selected, the /COUNT signal is output. The following is the timing chart of the tracking counter block.

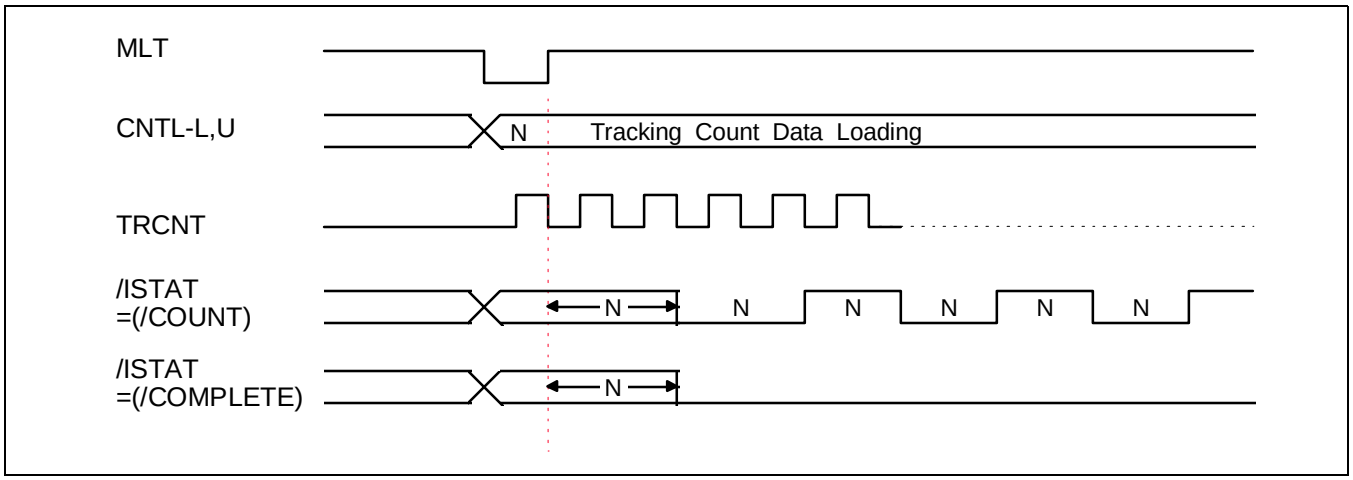


Figure 4. Tracking Counter Timing Chart

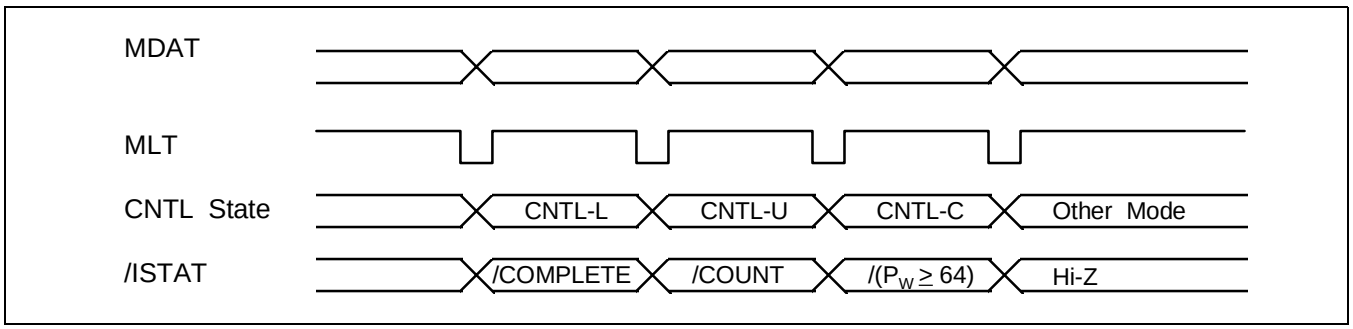


Figure 5. /ISTAT Output Signal According to CNTRL Register

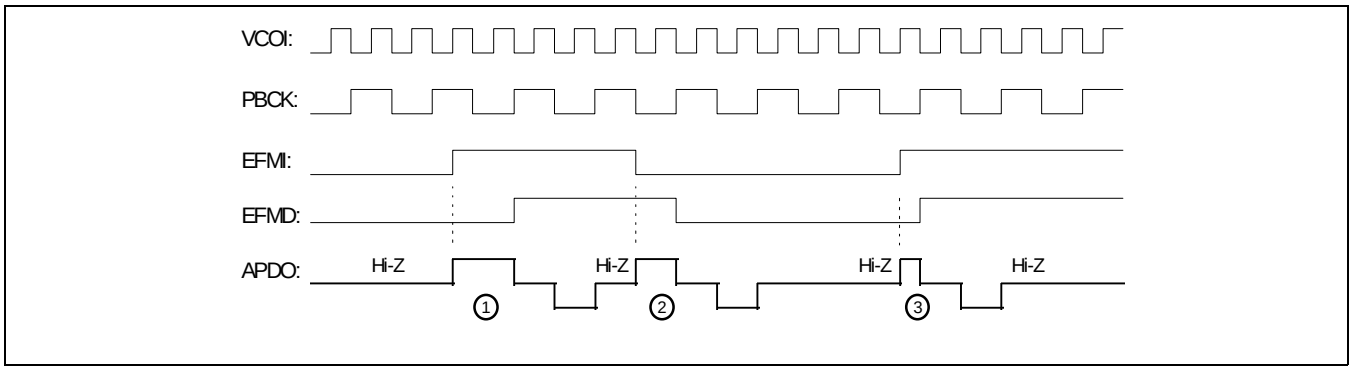
EFM DEMODULATION BLOCK

This block consists of an EFM demodulator which demodulates EFM data obtained from a disc, an EFM phasedetector and a controller, etc.

EFM PHASE DETECTOR

As the EFM signal input from a disc includes the components of 2.1609 MHz, the EFM phase detector uses the bit clock (/PBCK) of 4.3218 MHz, to detect the phase of this signal.
This PBCK detects the phase at the edge of the EFM signal and the result is output to the APDO1 or APDO2 terminals.

A. At Normal Operating



In case of (1) : When the EFM signal is slower than VCO
In case of (2) : When the EFM signal is locked with VCO
In case of (3) : When the EFM signal is faster than VCO

Figure 6. Timing Chart of the EFM Phase Detector

B. At Abnormal Operating

If the HIPD of CNTL-Z is “H” and “L” of the LKFS is shorter than 3.5T (a period PBFR is T), the Hi-Z is output to the APDO terminal as many as “L” , and if it is over 3.5T, the Hi-Z is output as many as 3.5T.

EFM DEMODULATOR

The 14-bit data is channeled through the circuit, and is de modulated to 8-bit data.
Demodulated data has two kinds of signals, One is subcode data and the other is audio data. They are respectively input into the subcode block written in the internal 16K SRAM to perform error correction.

FRAME SYNC DETECTOR, PROTECTOR AND INSERTER

A. Frame Sync Detector

The data consists of frame units, which include frame sync, subcode data, PCM data, redundancy data, etc. The frame sync is detected in order to maintain the sync.

B. Frame Sync Protector/Inserter

Occasionally, the frame sync is omitted or detected in a place where it doesn't exist by the effect of error or jitter on a disc.

In these cases, we need to protect or insert the signal. A window is made to protect the frame sync by using the WSEL. If the frame sync is input to the window, it is true data, and if isn't input, it is ignored. The width of the window is determined by WSEL of the CNTL-S register. If the frame sync is not detected in the frame sync protection window, one sync which is made by the internal counter block, is inserted in sequence. When the appointed number of frames is achieved by FSEM, FSEL of the CNTL-S register, the ULKFS becomes "L" and the frame sync protection window is ignored. The frame sync is received absolutely at that time. When the frame sync is received, the ULKFS signal becomes "H" and the frame sync window is received.

LKFS	ULKFS	Comment
1	1	Corresponding with playback frame sync and generated frame sync
0	1	1. Out of correspondence with playback frame sync generated frame sync, but PBFR sync is detected in the window selected by WSEL. 2. Out of correspondence with PBFR sync and XTFR sync, and sync is inserted because it isn't detected in the window selected by WSEL.
0	0	1. After inserting as many frames as decided by FSEM and FSEL of the CNTL-S register, and the window is ignored. 2. In case that the PBFR sync is not detected continually after (1).

SUBCODE BLOCK

The subcode sync signal (that is S0, S1) is detected in the subcode sync block. When S0 is detected, S1 is detected after one frame. At that time, the S0 + S1 signal is output to the S0S1 terminal, and the S0S1 signal is output to the SBDT terminal when the S0S1 signal is "H". The subcode data among the data input to the EFM terminal, is demodulated to 8-bit subcode data (P, Q, R, S,T, U, V, W). It is synchronized with the PBFR signal and is output to SBDT by the SBCK clock. Among the eight subcode data, only Q data is selected and loaded to the eighty shift register by the PBFR signal. The result of the CRC (Cycle Redundancy Check) of loading data, is synchronized with the S0S1 positive edge and output to the SQOK terminal.
If the result is error, "L" is output to the SQOK terminal, and if it is true, "H" is output instead.
If the CRCD of CNTL-Z mode is "H", the result of CRC checking is output to the SQDT terminal from the S0S1 section "H" to the period of the SQCK negative edge.

The following is the timing chart of the subcode block

At SQEN = “L”: SBDT, SQDT, S0S1, SQOK, VCOI Timing Chart.

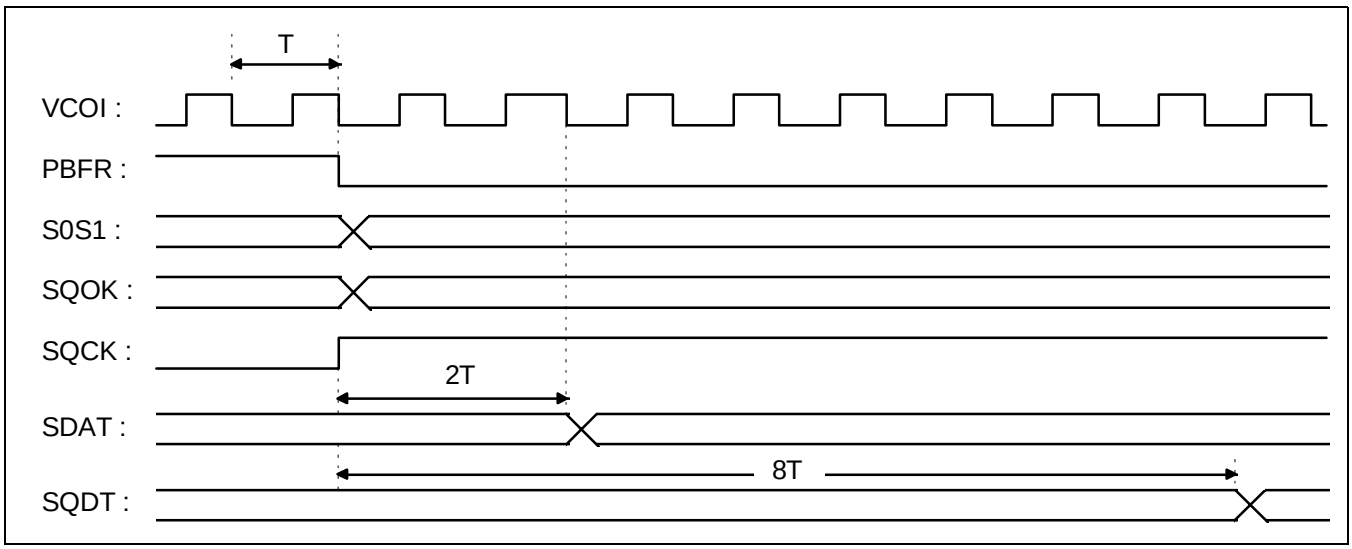


Figure 7. Subcode-Q Timing Chart 1

At SQEN = “L”: SQOK, SQDT, S0S1 Timing Chart

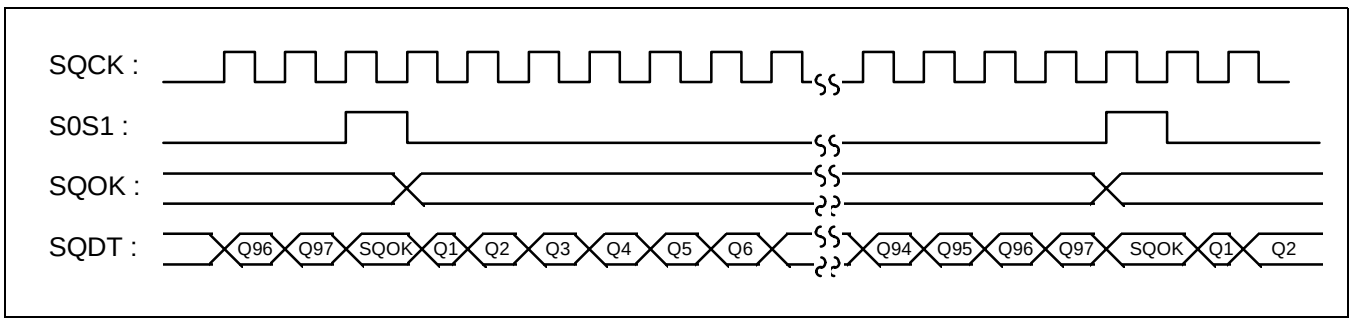


Figure 8. Subcode-Q Timing Chart 2

At SQEN = “H”: SQOK, SQDT, S0S1, Timing Chart

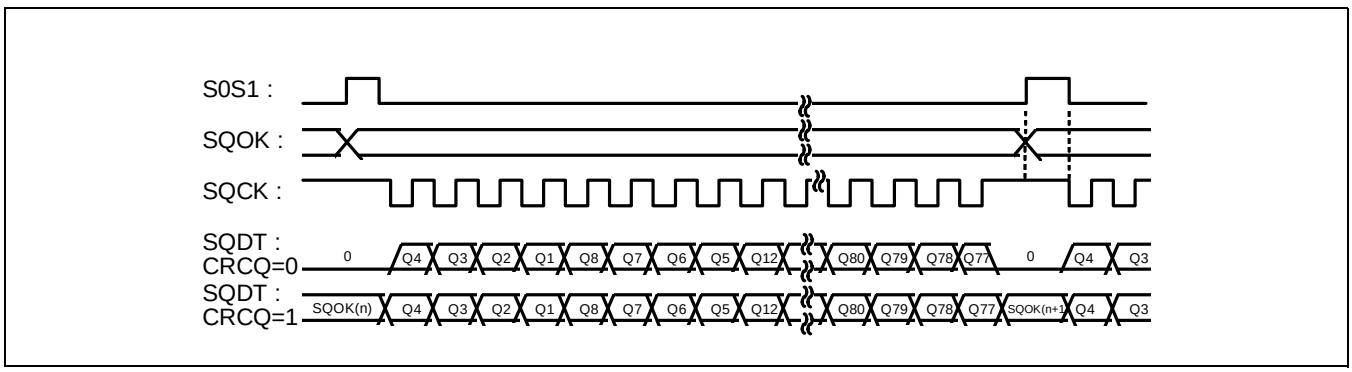


Figure 9. Subcode-Q Timing Chart 3

(Comment) : If the SQOK of the subcode Q data is “H”, the subcode data is output to SQDT according to the SQCK signal.
If the SQOK is “L”, it is output to SQDT with “L”.

VCOI, SBDT, SBCK Timing Chart.

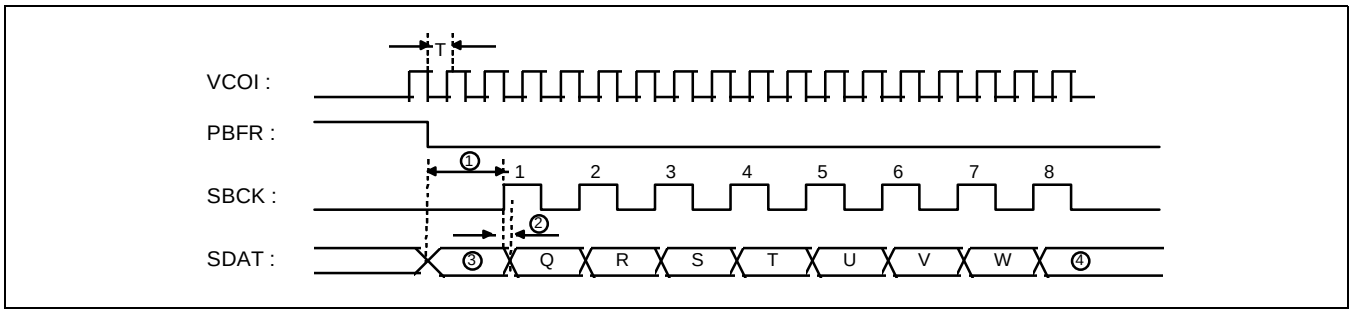


Figure 10. Timing Chart of Subcode Data Output

(1) : After PBFR becomes negative edge, SBCK becomes “L” for about 10 msec.
(2) : If S0S1 is “L”, subcode P is output, and if “H”, S0S1 is output.
(3) : If a period of VCOI is “T”, the width of (3) is 4T.
(4) : If the pulse input to the SBCK terminal is over seven, subcode data(P, Q, R, S, T, U, V, W) is repeated.

ECC (ERROR CORRECTION CODE) BLOCK

The function of the ECC block is to recover damaged data to some extent when data on a disc is damaged. By using the CIRC (Cross Interleaved Reed-Solomon Code), 2-Error correction is performed for C1 (32, 28) and 4-erasure correction is performed for C2 (28, 24).
ECC is performed by the unit of one symbol of eight bits. In correcting C1, a C1 pointer is generated, and in correcting C2, the C2 pointer is generated. C1, C2 pointers send error information to the data which ECC is given. After correcting C2, against uncorrectable data, error data is sent to display by outputting a C2 FLAG.
This information data is input to the interpolator block in order to handle error data.
The monitoring flow for error correction is available through FLAG1 ~ FLAG5 terminals.

The monitoring flow for error correction

MODE	FLAG5	FLAG4	FLAG3	FLAG2	FLAG1	REMARK
C1 0,1 error	0	1	1	1	0	–
C1 2 error	0	1	1	1	1	–
C1 irretrievable error	0	1	1	1	1	–
C1 0,1,2 error	0	1	1	1	1	Attenuation
C2 0,1,2,3,4 error	1	1	1	0	1	–
C2 irretrievable error 1	1	1	1	1	0	–
C2 irretrievable error 2	1	1	1	1	1	C1 point copy 1

INTERPOLATION / MUTE BLOCK

Interpolator

When a burst error occurs on a disc, sometimes the data can't be corrected even if an ECC process is performed. The interpolator block revises data by using a C2 pointer output through the ECC block.The data input to a data bus is input to the left and right channel, respectively, in the order of the lower 8-bit and the upper 8-bit.
A pre-hold method is taken when a C2 pointer is "H" continuously. In case of a single error, an everage interpolation method is carried out with the range of the data before and after an error happens.
When LRCH signal during one LRCH cycle is "L", R-CH data is output, L-CH data is output when the check is "H".

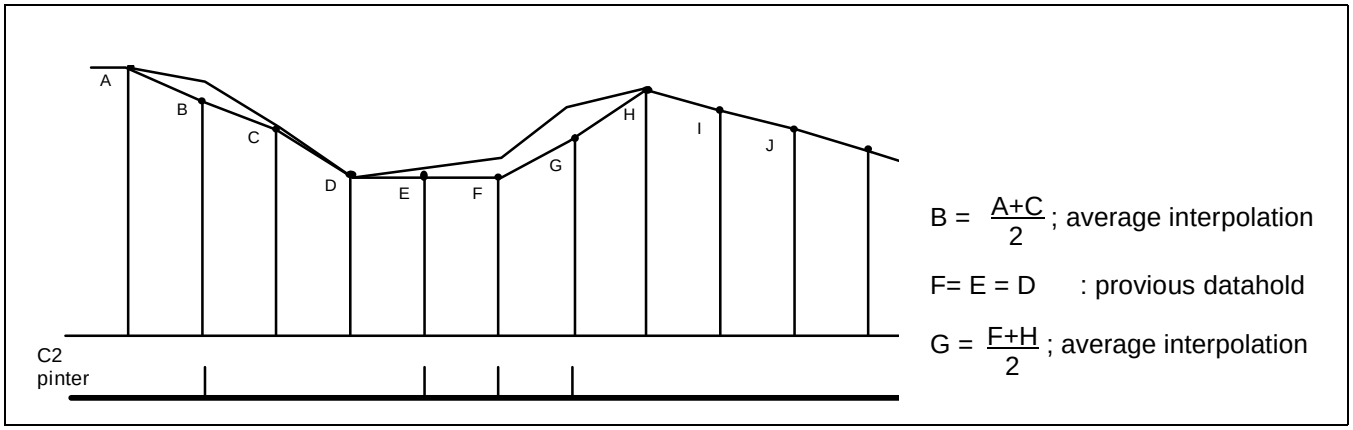


Figure 11. Interpolation.

Mute and Attenuation

By using a mute terminal and the ATTM signal of the CNTL-S register, audio data is muted or attenuated.There are two kinds of mute: zero-cross muting and muting

A. Zero-Cross Muting

The audio data is muted, after ZCMT of CNTL-Z register goes to "H". In that case the mute is "H" and the upper 6-bit of audio data became all "L" or "H".

B. Muting

The audio data is muted when ZCMT of the CNTL-Z register is "L" and the mute terminal is "H".

C. Attenuation

The signal attenuation occurs by the means of the ATTM of the CNTL-Z register, and the mute signal as shown the following,.

Attm	Mute	Degree of Attenuation
0	0	0 dB
0	1	– ∞ dB
1	0	–12 dB
1	1	–12 dB

DIGITAL AUDIO OUT BLOCK

The 2 channel, 16-bit data is connected and output serially to other digital systems by the digital audio interface format.

<Digital audio interface format for CD>

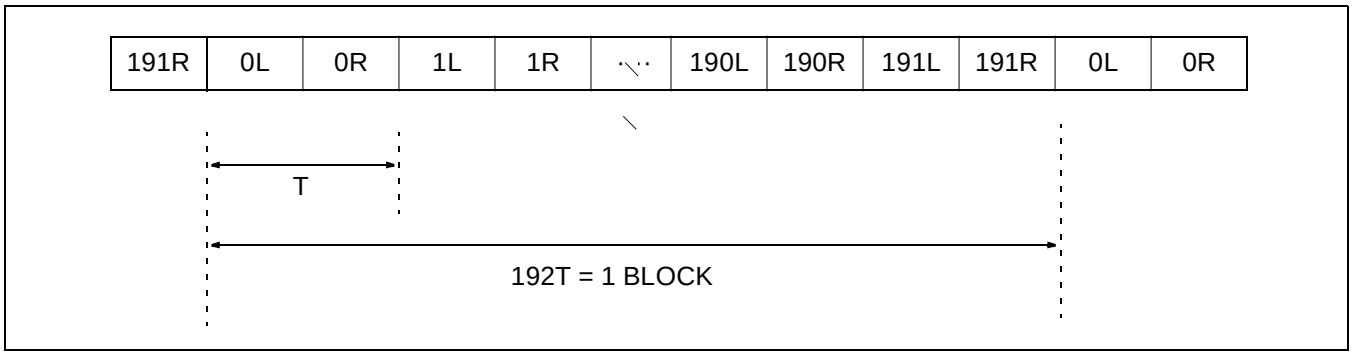


Figure 12.

0L: L-CH format includs block sync preamble.
1L ~ 191L: L-CH format includs L-CH sync preamble.
0R ~ 191R: R-CH format includs R-CH sync preamble.

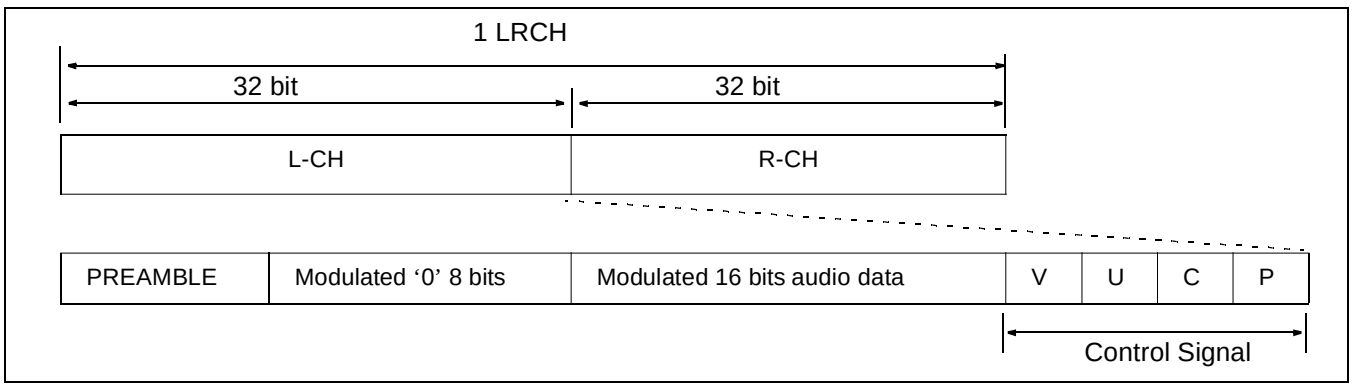


Figure 13. Digital Audio Out Format

A. Preamble

It is used to discriminate between the block sync of data and L/R-channel of data.

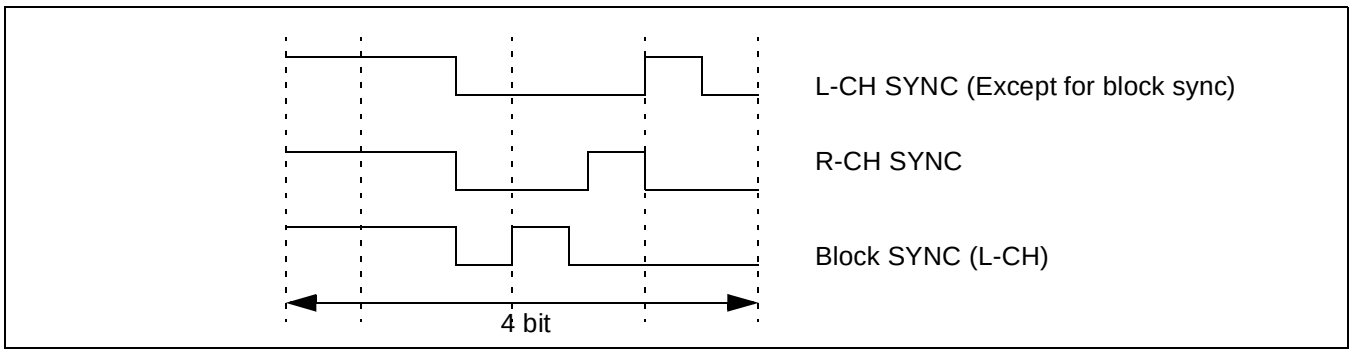


Figure 14. Preamble Signal

B. Control signal

(1) Validity bit: It indicate that the error of 16-bit audio data exists, or doesn't ("H" : error, "L": valid data)
(2) User definable bit: Subcode data input.

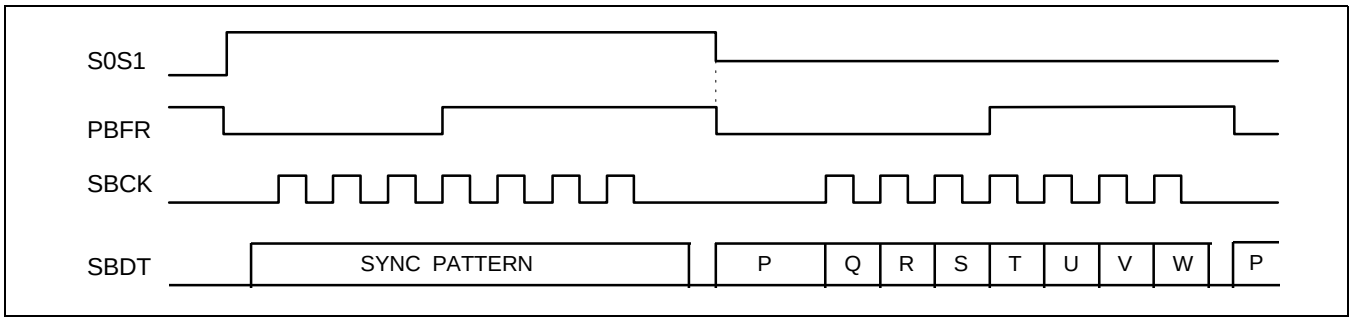


Figure 15. Timing Chart of Digital Audio Out

(3) Channel status bit: The upper 4-bit of subcodes Q indicate the number of channels, pre-emphasis copy and CDP category, etc.

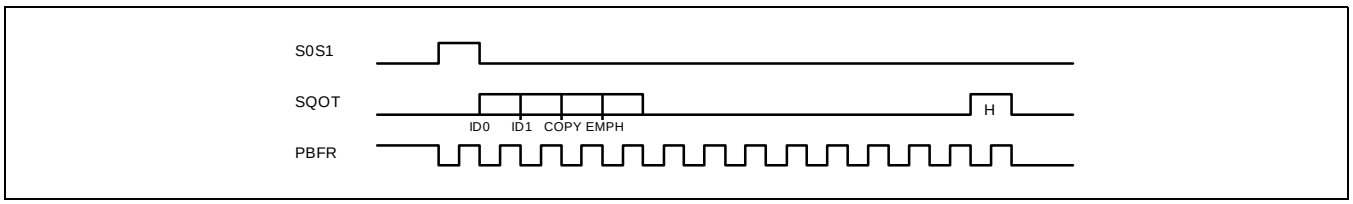


Figure 16. Timing Chart of Channel Status Data Output

(4) Parity bit: Making even parity

CLV SERVO BLOCK

The CNTL-C register is selected to control the CLV (Constant Linear Velocity) servo by the data input from micom. In the CNTL-C register, the CLV servo action mode is appointed by the data input from micom to control the spindle motor. In case of a double-speed setting, the CNTL-C register has to be selected after the CNTL-D register sets, so that it is able to detect / (Pw ≥ 64) signal from the /ISTAT terminal.

Forward Mode

The status of the related output terminals are as follows.

SMDP	SMSD	SMEF	SMON
H	Hi-Z	L	H

Reverse Mode

The status of the related output terminals are as follows.

SMDP	SMSD	SMEF	SMON
L	Hi-Z	L	H

Speed-Mode

The speed-mode is the mode for the rough control of a spindle motor when a track is jumping or when an EFM phase is unlocked. If a period of VCO is “T”, the pulse width of frame sync is “22T”. In case that the signal detected from an EFM signal exceeds “22T” by noise on the disc.... etc., it must be removed. If not, the right frame sync can’t be detected. In this case, the pulse width of the EFM signal is detected by peak and bottom hold clock. The peak hold clock is XTFR/2 or XTR/4, and the bottom hold clock is XTFR/16 or XTFR/32. The detected value is used for the synchronized frame signal. If a synchronized frame signal is less than 21T, the SMDP terminal outputs “L”. When it is equal to 22T, it outputs “HiZ”, and when it is more than 23T, it outputs “H”. If the gain signal of the CNTL-W register is “L”, the output of SMDP terminal is reduced up to - 12 dB. If it is “H”, there is no reduction.

Hi-Speed-Mode

The rough servo mode, which moves 20,000 tracks in high speed, acts between the inner and outer peripheries of the CD. The track’s mirror domain (where there are no pits) is duplicated with 20 kHz signals to the EFM. In this case, the servo action is unstable, because, the peak value of the mirror signal is longer than the original frame signal, which is detected. In Hspeed mode, by using the 8.4672/256 MHz signal against peak hold, and the XTFR/16 or XTFR/32 signal against bottom hold, the mirror is removed , and the Hspeed action becomes stable . The output conditions in Hspeed mode are: SMSD is “Hi-Z”, “SMEF” is “L”, and SMON is “H”.

SMDP	SMSD	SMEF	SMON
–	Hi-Z	L	H

Phase-Mode

The phase-mode is the mode to control the EFM phase. Phase difference between PBFR/4 and XTFR/4 is detected when NCLV of CNTL-Z is “L” and the difference is output to the SMDP terminal. If a cycle of VCO/2 signal is put as “T” and it is put as “/WP” during an “H” period of PBFR, it outputs “H” to the SMSD terminal from the falling edge of PBFR to the (/WP-278T) X 32, and then, outputs “L” to the falling edge of the next.

XPHSP-Mode

The XPHSP mode is the mode used in normal operation. It samples a LKFS signal made in the frame sync block at a cycle of PBFR/16. If the sampling is “H”, the phase mode is performed, and if “L” is sampled 8 times consecutively, the speed mode is performed automatically. The selection of peak hold period of speed mode, and bottom hold period and gain of speed / Hspeed mode is determined by the CNTL-W register.

VPHSP-Mode

The VPHSP-mode is the mode used for rough servo control. It uses VCO instead of X-tal in the EFM pattern test. When the range of VCO center changes, VCO is easily locked because the rotation of a spindle motor changes in the same direction.

STOP

Stop is the mode used to stop the spindle motor.

SMDP	SMSD	SMEF	SMON
L	Hi-Z	L	L

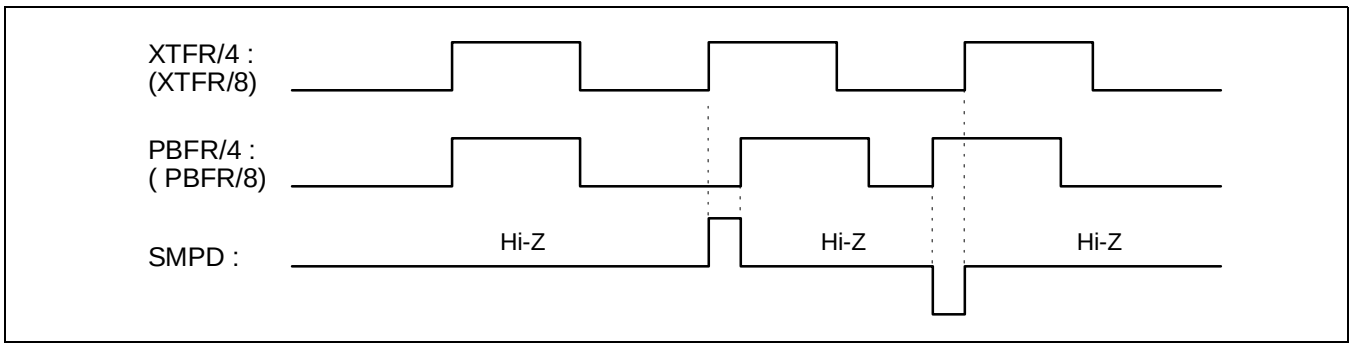


Figure 17. Timing Chart SMDP Output

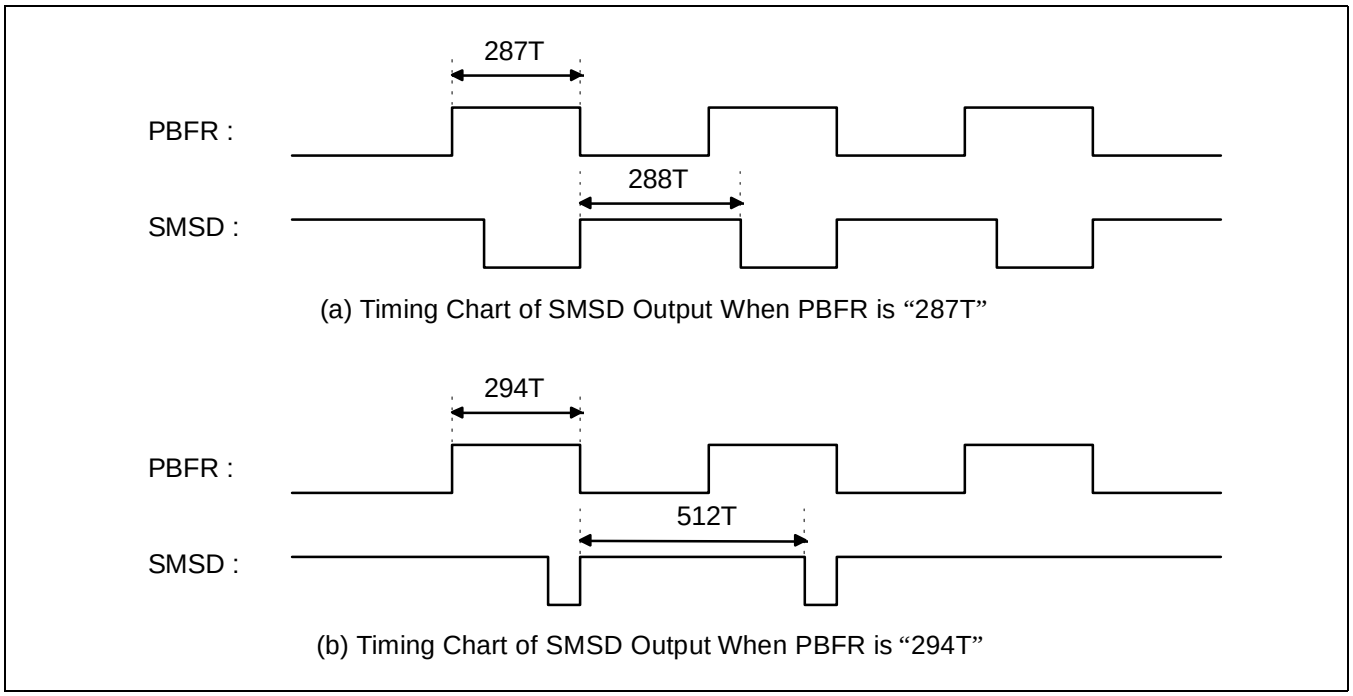


Figure 18. Timing Chart of SMSD Output at Phase Mode.

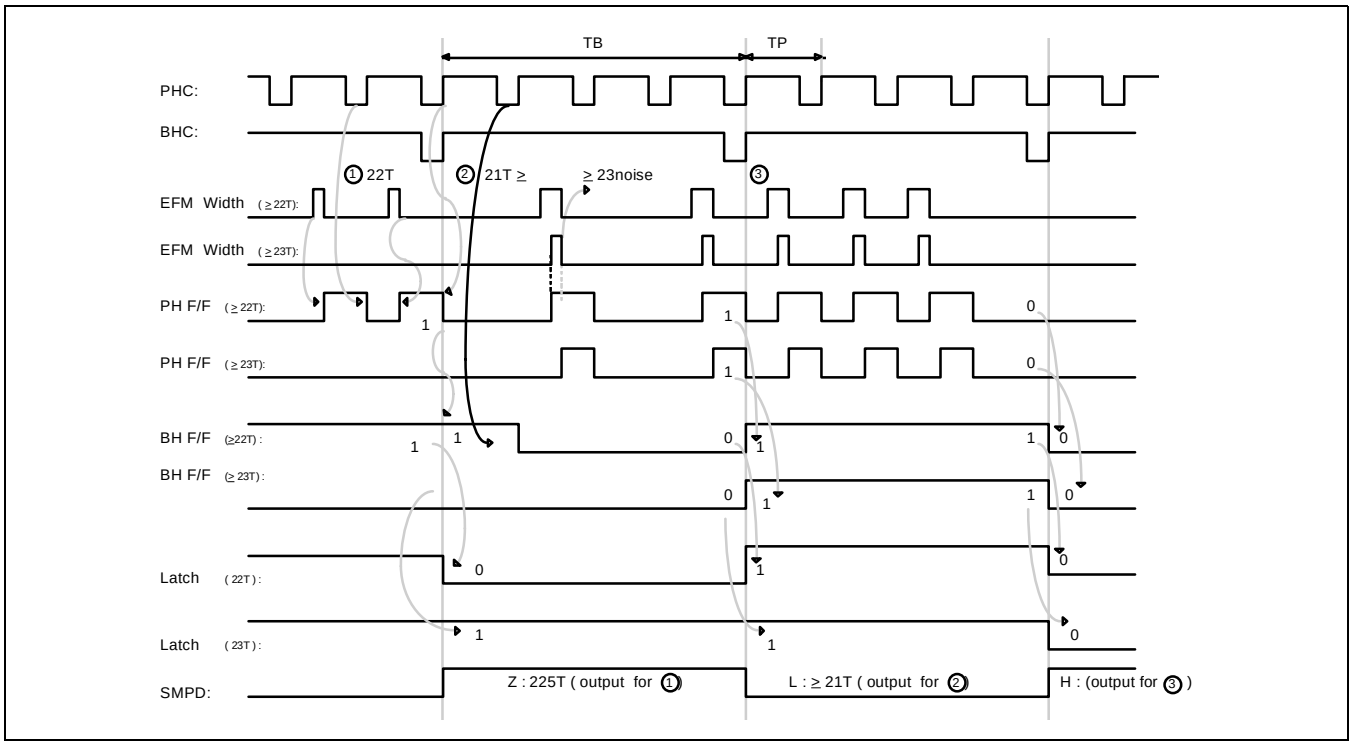


Figure 19. Timing Chart of SMPD Output When the Gain is “H” in the Speed Mode

DIGITAL PLL BLOCK

This device contains analog PLL and digital PLL together, in order to obtain the stable channel clock for demodulating the EFM signal.
The block diagram of digital PLL is as follows.

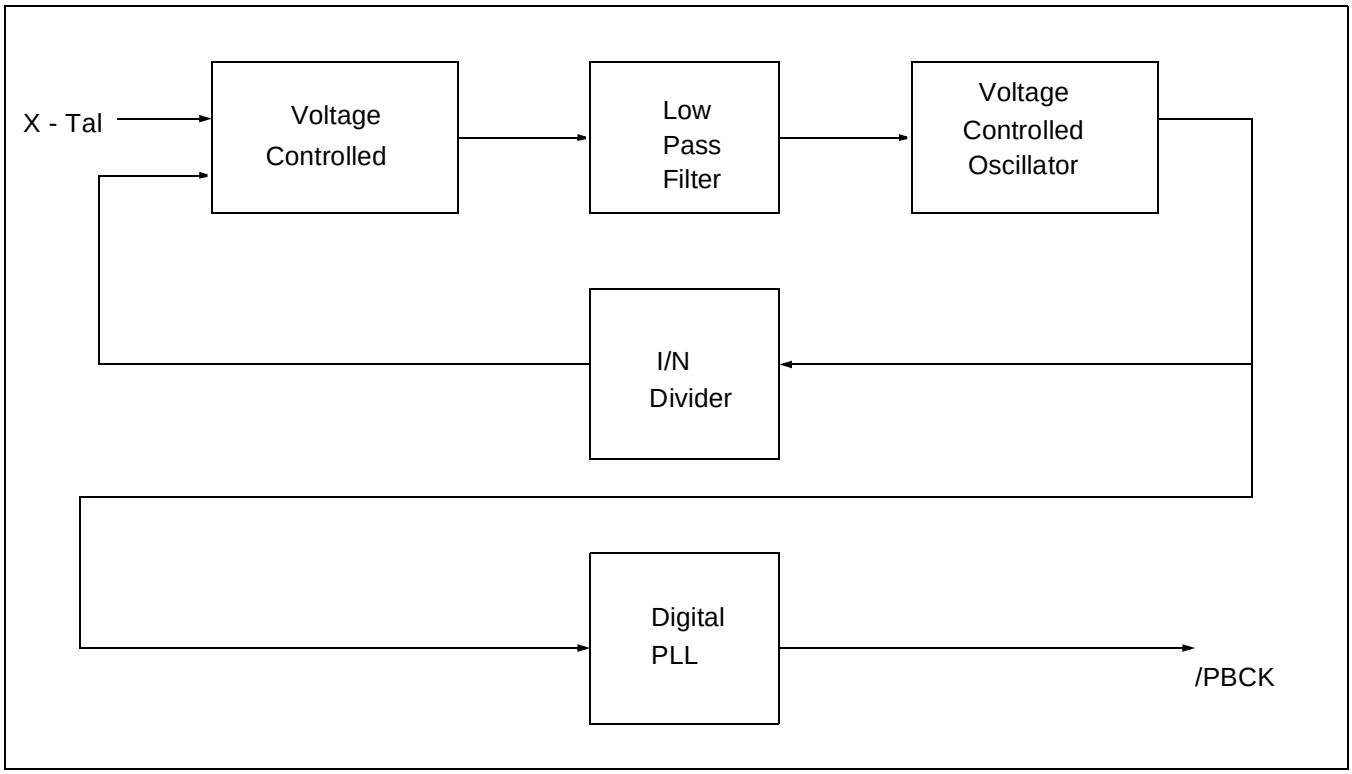


Figure 20. The Application Diagram of Digital PLL