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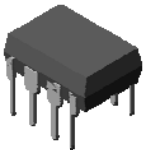
Low Power Audio Amplifier S6419/P

SOP-8



DIP-8

ORDERING INFORMATION

Product	Marking	Package
S6419	S6419	SOP-8
S6419P	S6419	DIP-8

▲ Marking Information

① Device Code

② YWW : Year & Week Code

□ : Assembly Plant Code

Description

The S6419/P is a low power audio amplifier integrated circuit, intended for the communication applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages.

Coupling capacitor to the speaker is not required. Open loop gain is around 80dB, and the closed loop gain is set with two external resistors [Rf and Ri : refer to page 2].

A chips disable pin permits powering down and/or muting the input signal.

Application

◈ Telephone

◈ Speakerphone

◈ Fax machine & Combination Printer

Features and Benefits

◈ Wide range of operating supply voltage (2~16V) for telephone line powered applications.

◈ Low quiescent supply current (typ.)2.0mA for battery powered applications.

◈ Added disable input for saving power
Low muting mode supply current (Typ.)65uA.

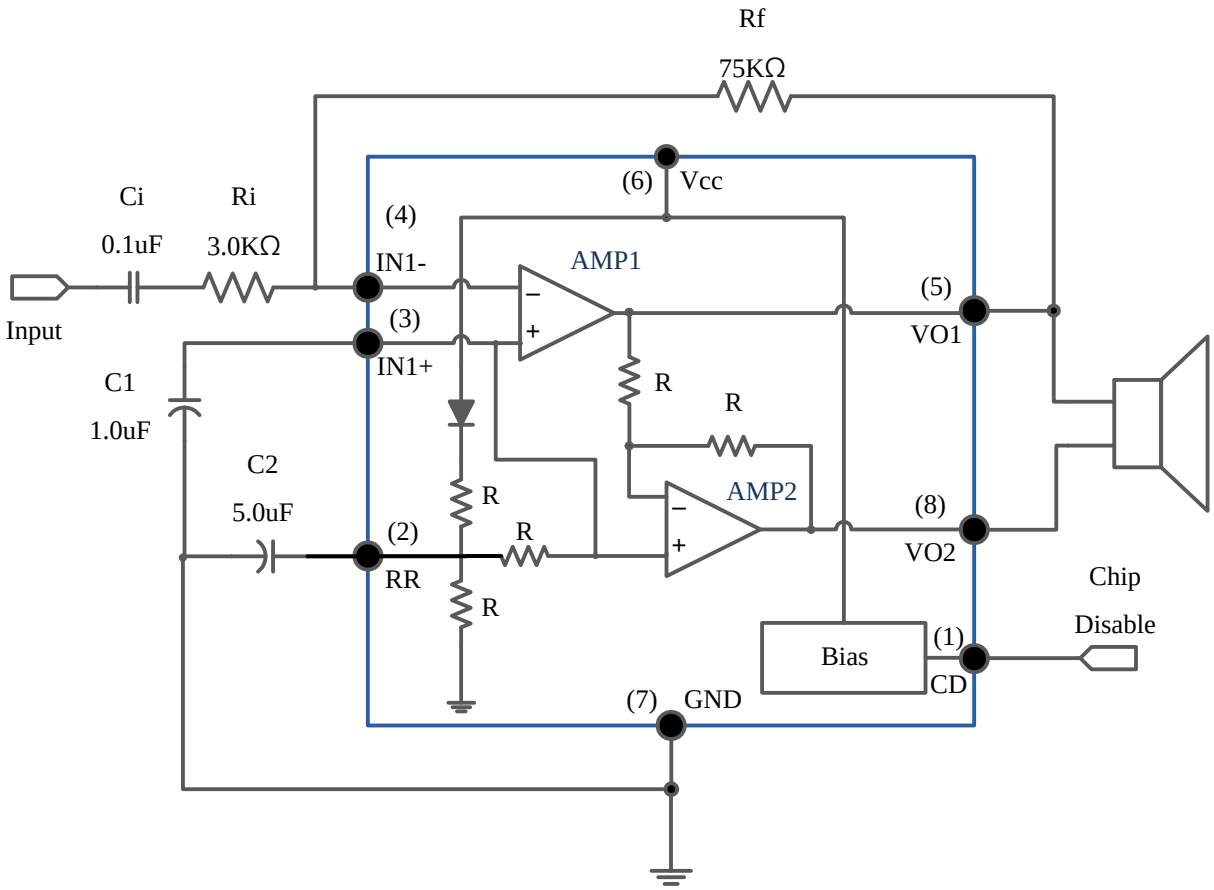
◈ Available to drives a wide range of load (8Ω to 100Ω)

◈ Output power exceeds 250mW with 32Ω Speaker.

◈ Low total harmonic distortion (Typ.) 0.5%

◈ Few external components are required.

◈ Internal Block Diagram & Typical Application Circuit



C2 : Optional external Cap.

Differential Gain : 2*(Rf/Ri)

◈ Pin Description

No	Symbol	I/O	Description
1	Chip Disable	I	This pin can be used to power down the IC to converse power, or for muting. Enable(Open or less than 0.8V), Disable (2.0V to Vcc)
2	RR	I	A capacitor at this pin increase PSRR and affects turn-on time. This pin can be left open if the capacitor at pin 1 is sufficient.
3	IN1(+)	I	OP-Amp1's Non-inverting Input
4	IN1(-)	I	OP-Amp1's Inverting Input
5	VO1	O	Differential Output1 [DC Level: (V_{CC}-0.7V)/2]
6	V_{CC}	PWR	V_{CC} for Audio Amplifier
7	GND	GND	GND
8	VO2	O	Differential Output2 [DC Level : (V_{CC}-0.7V)/2]

Absolute maximum ratings (Ta=25℃)

Characteristic	Symbol		Ratings	Unit
Supply voltage	V_{CC}		-1 to +18	V
Output current	I_{OUT}		±250	mA
Input voltage at RR, CD, IN(+), IN(-)	V_{IN}		-1 to V_{CC}+1	V
Applied output voltage to VO1, VO2 (disable)	V_O		-1 to V_{CC}+1	V
Power Dissipation	P_D	SOP-8	600	mW
		DIP-8	1000	mW
Operating temperature	T_{opr}		-20 ~ +70	℃
Storage temperature	T_{stg}		-55 ~ 150	℃

Recommended Operation Conditions (Ta=25℃)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.0	-	16.0	V
Load Impedance	R_L	8.0	-	100	Ω
Peak Load Current	I_L	-	-	±200	mA
Differential Gain (5.0KHz Bandwidth)	AVD	0	-	46	dB
Voltage at chip disable	VCD	0	-	V_{CC}	V
Ambient Temperature	Ta	-20	-	70	℃

Electrical Characteristics

(Unless otherwise specified. V_{CC} = 6V, Ta = +25 °C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Amplifiers (DC Characteristics)						
Output DC Level @ VO1,VO2	VO(3V)	V_{CC} =3.0V, R_L=16Ω, Rf=75KΩ	1.0	1.15	1.25	V
	VO(6V)	V_{CC} =6.0V, R_L=16Ω, Rf=75KΩ	-	2.65	-	
	VO(12V)	V_{CC} =12.0V, R_L=16Ω, Rf=75KΩ	-	5.65	-	
Output High Level	V_{OH}	2.0V≤V_{CC}≤16V, I_{OUT}=-75mA	-	$V_{CC-1.0}$	-	V
Output Low Level	V_{OL}	2.0V≤V_{CC}≤16V, I_{OUT}=75mA	-	0.16	-	V
Output DC Offset Voltage (VO1-VO2)	ΔVO	V_{CC} =6.0V, R_L=32Ω, Rf=75KΩ	-30	0	+30	mV
Input Bias Current	I_{IB}	V_{CC} =6.0V	-	-100	-200	nA
Equivalent Resistance @ IN1+	R_{EQ}	V_{CC} =6.0V	100	150	220	KΩ
Equivalent Resistance @ RR		V_{CC} =6.0V	18	25	40	KΩ
Chip Disable (Pin 1)						
Input Voltage (Low)	V_{IL}	-	-	-	0.8	V
Input Voltage (High)	V_{IH}	-	2.0	-	-	V
Input Resistance	R_{CD}	V_{CC}=V_{CD}=16V	50	90	175	KΩ
Power Supply						
Power Supply Current	$I_{CC(3V)}$	V_{CC} =3.0V, R_L=∞, CD=0.8V	-	2.0	3.0	mA
	$I_{CC(16V)}$	V_{CC} =16.0V, R_L=∞, CD=0.8V	-	3.0	4.0	mA
	$I_{CC(Disable)}$	V_{CC} =3.0V, R_L=∞, CD=2.0V	-	65	100	uA
Amplifiers (AC Characteristics)						
Open Loop Gain (AMP.1)	G_V1	-	80	-	-	dB
Open Loop Gain (AMP.2)	G_V2	V_{CC} =3.0V, R_L=16Ω, f=1.0KHz	-0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	-	-	1.5	-	MHZ
Output Power	P_{OUT}(3V)	V_{CC} =3.0V,R_L=16Ω,THD≤10%	55	-	-	mW
	P_{OUT}(6V)	V_{CC} =6.0V,R_L=32Ω,THD≤10%	250	-	-	
	P_{OUT}(12V)	V_{CC} =12.0V,R_L=100Ω,THD≤10%	400	-	-	
Total Harmonic Distortion (f=1.0KHz)	THD	V_{CC} =6.0V, R_L=32Ω, P_{OUT}=125mW	-	0.5	1.0	%
		V_{CC}≥3.0V, R_L=8Ω, P_{OUT}=20mW	-	0.5	-	
		V_{CC}≥12V, R_L=32Ω, P_{OUT}=200mW	-	0.6	-	
Power Supply Rejection (V_{CC}=6.0V, ΔV$_{CC}$=3.0V)	PSRR	**C1=∞, C2=0.01uF	50	-	-	dB
		**C1=0.1uF, C2=0, f=1.0KHz	-	12	-	
		**C1=1.0uF, C2=5.0uF, f=1.0KHz	-	52	-	
Muting	$G_{V(mute)}$	Mute=2V, 1KHz<f<20KHz	-	>70	-	dB

** External Capacitance C1, C2 : Refer to the Page 2 (Typical application circuit.)

Fig.1 Supply Current vs. V_{CC}

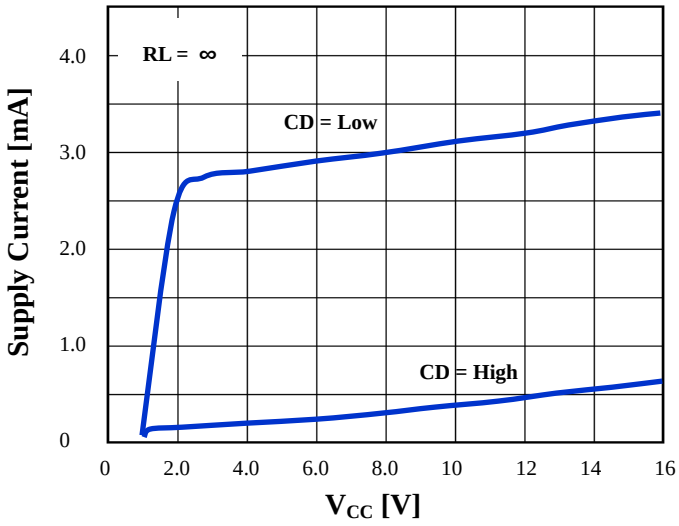


Fig.2 Supply Current vs. Ambient Temp.

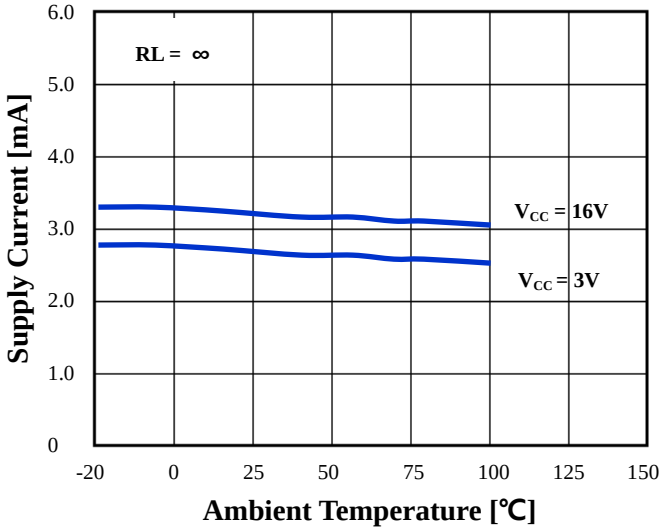


Fig.3 Small Signal Response

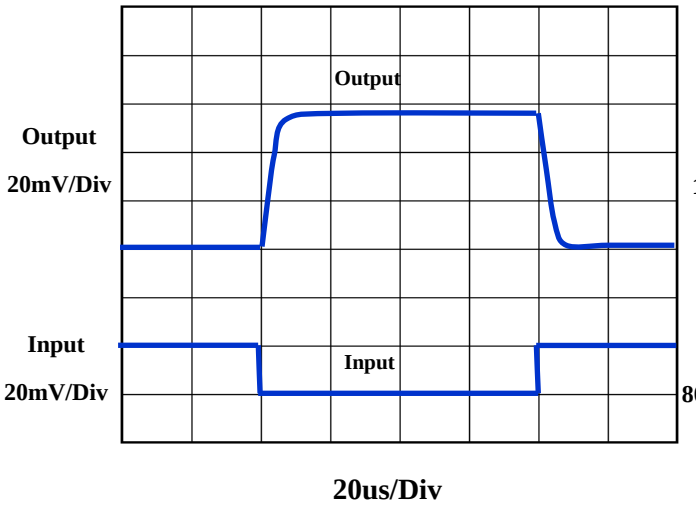


Fig.4 Large Signal Response

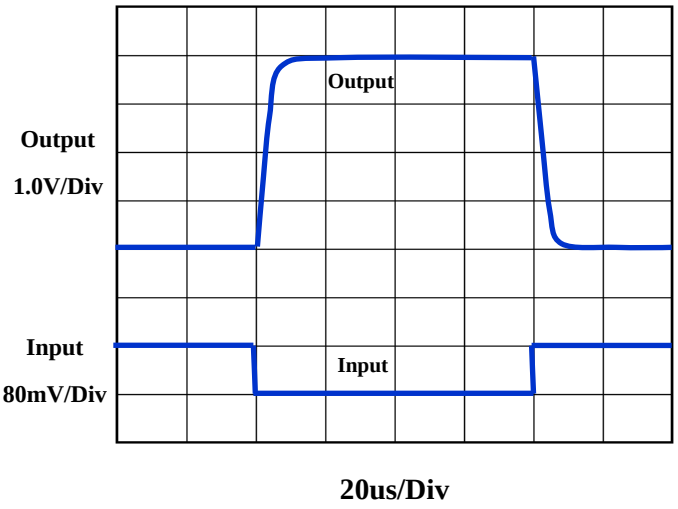


Fig.5 V_{CC}-V_{OH} vs. Load Current

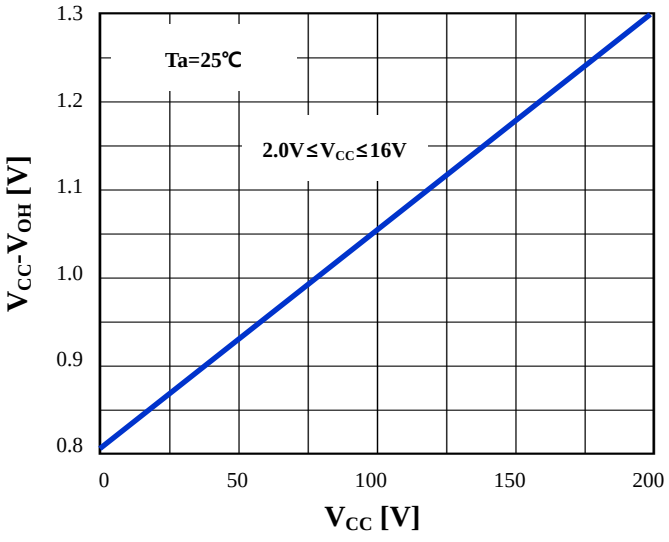


Fig.6 V_{OL} vs. Load Current

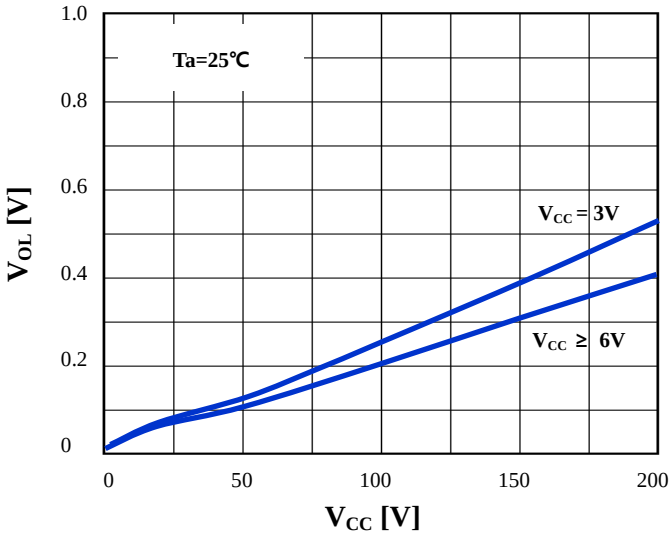


Fig.7 Device Dissipation [8.0Ω Load]

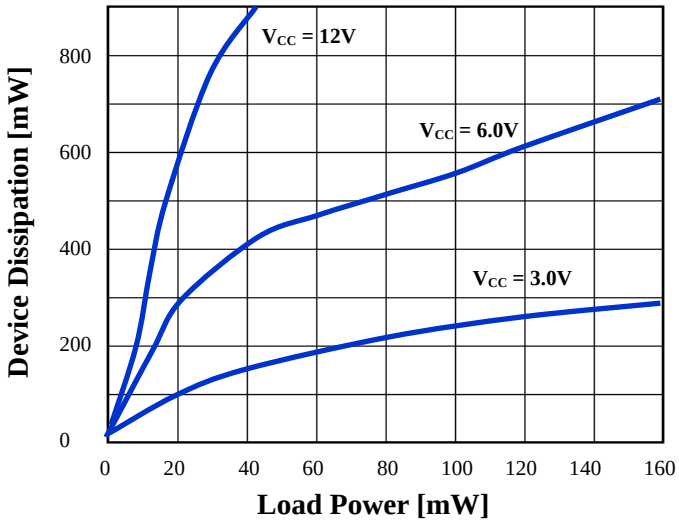


Fig.8 Device Dissipation [16Ω Load]

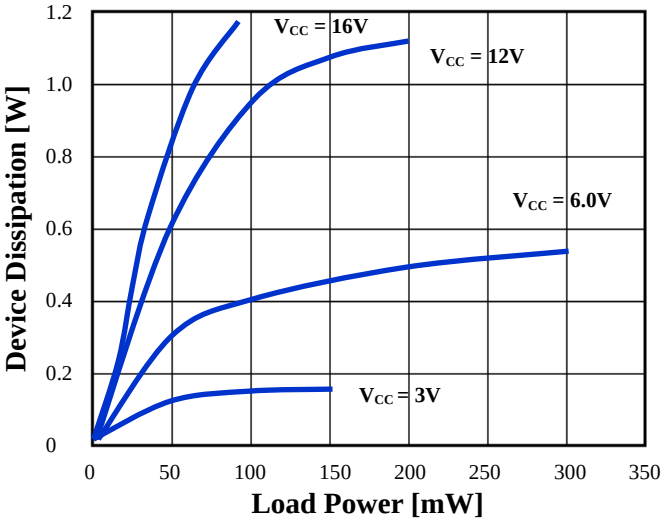


Fig.9 Device Dissipation [32Ω Load]

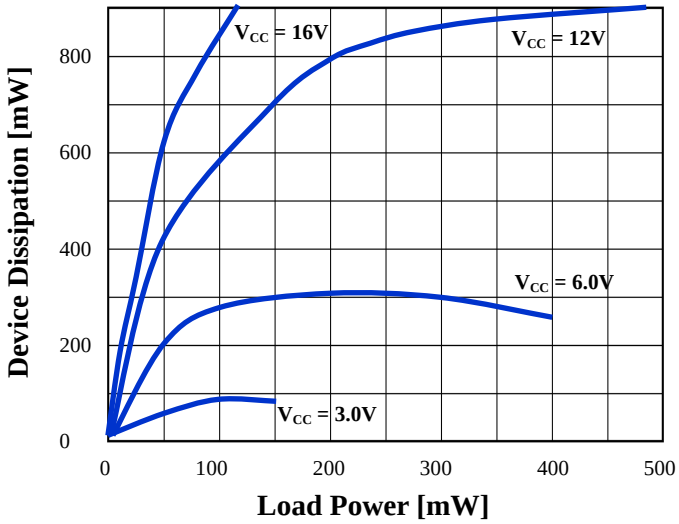


Fig.10 THD vs. Output Power

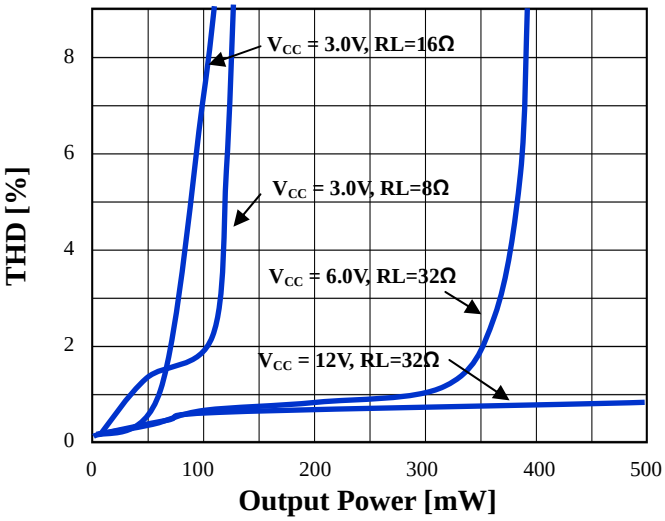


Fig.11 Differential Gain vs. Frequency

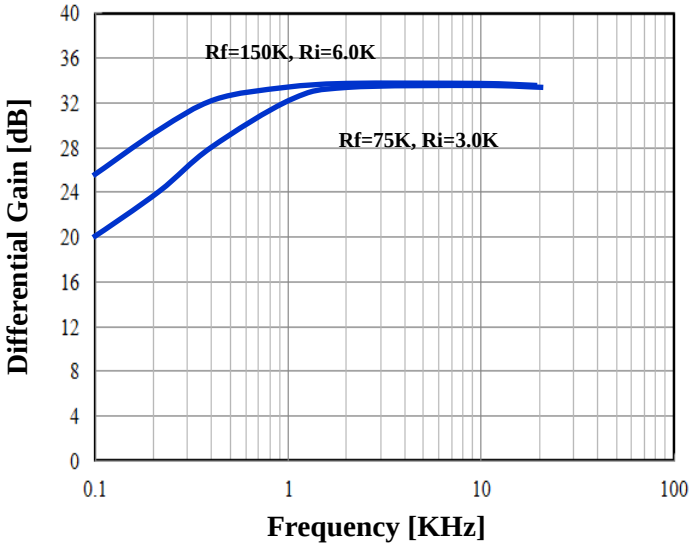
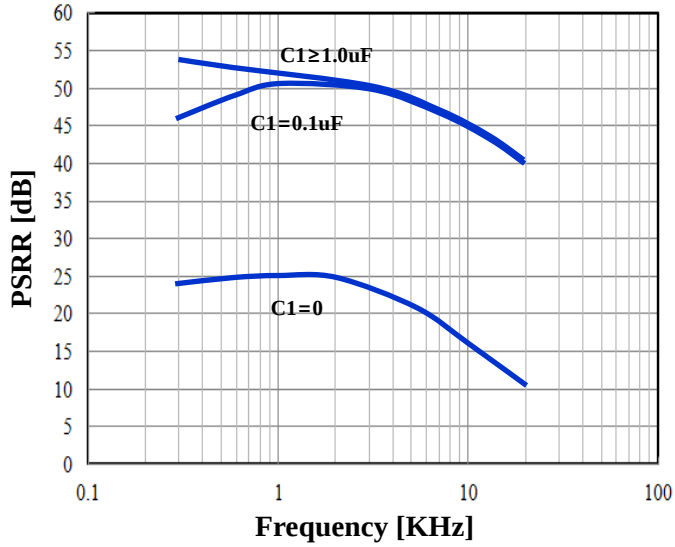
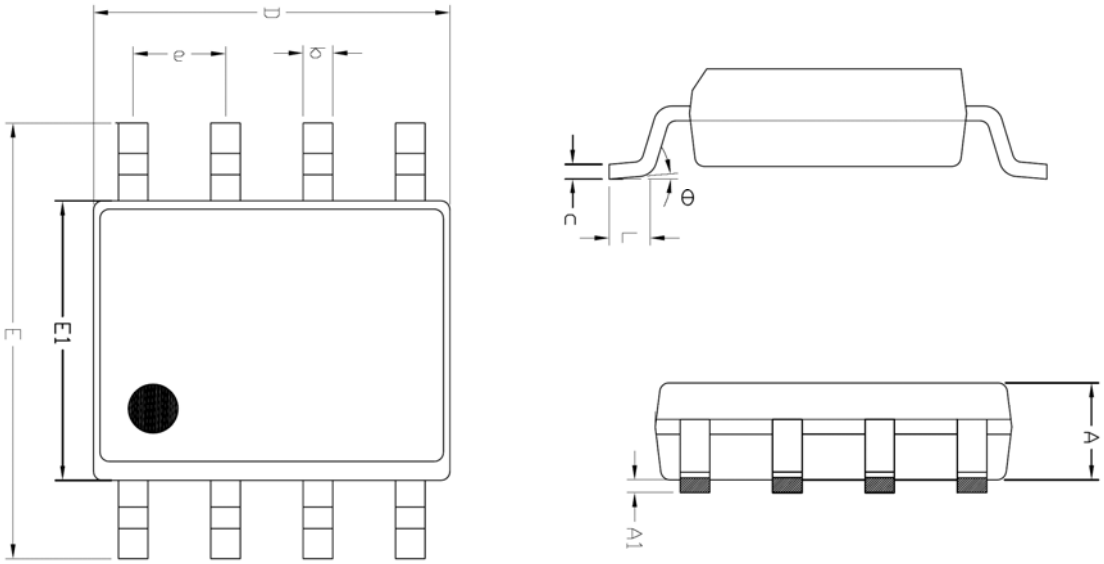


Fig.12 PSRR vs. Frequency @ C2=5.0uF

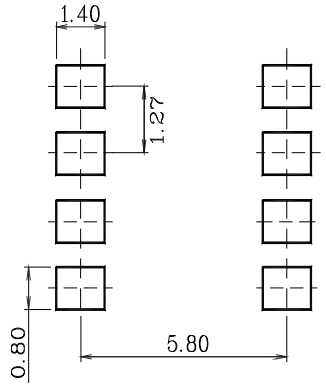


Outline Dimension (Unit : mm)

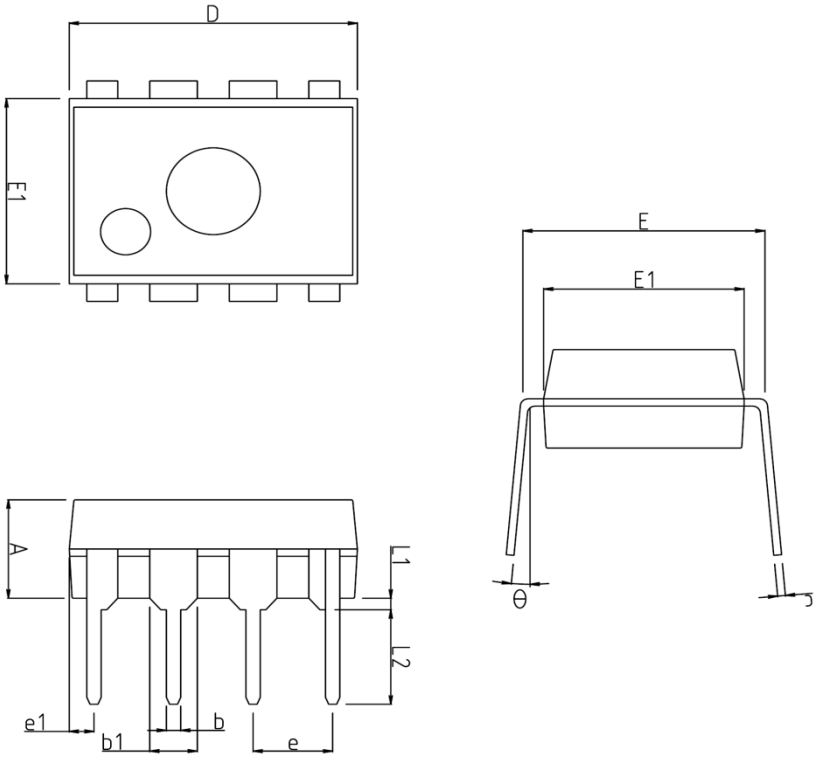


SYMBOL	MILLIMETER(mm)			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	1.245	—	1.445	
A1	0.125	0.175	0.275	
b	0.320	0.420	0.520	
c	0.170	0.220	0.270	
D	4.802	4.902	5.002	
E	5.870	6.020	6.170	
E1	3.761	3.861	3.961	
e	1.270 BSC			
L	0.462	0.562	0.662	
θ	0 °	—	8 °	

※ Recommend PCB solder land (Unit : mm)



Outline Dimension (Unit : mm)



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	3.20	3.40	3.60	
b	0.36	0.46	0.56	
b1	1.42	1.52	1.62	
c	0.20	0.25	0.35	
D	9.00	9.20	9.40	
E	7.37	7.62	7.87	
E1	6.20	6.40	6.60	
e	2.54 TYP			
e1	0.79 TYP			
L1	0.33	–	–	
L2	3.00	3.30	3.60	
θ	0°	–	15°	

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