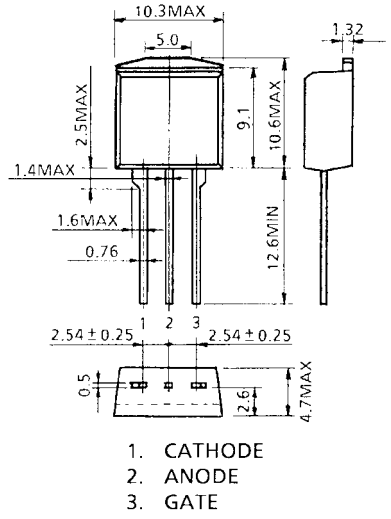
TOSHIBA THYRISTOR SILICON PLANAR TYPE

S6744

MEDIUM POWER CONTROL APPLICATIONS

- Repetitive Peak Off−State Voltage : V_{DRM} = 400V
  Repetitive Peak Reverse Voltage : V_{RRM} = 400V
- Average On−State Current : $I_{T\ (AV)}$ = 8A
- A Large Current Pulse Capability

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	13−10J1B

Weight: 1.7 g

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Repetitive Peak Off−State Voltage and Repetitive Peak Reverse Voltage	V_{DRM} V_{RRM}	400	V
Non−Repetitive Peak Reverse Voltage (Non−Repetitive<5ms, T_j = 0~125°C)	V_{RSM}	500	V
Average On−State Current (Half Sine Waveform Tc = 72°C)	$I_{T\ (AV)}$	8	A
R.M.S On−State Current	$I_{T\ (RMS)}$	12.6	A
Peak One Cycle Surge On−State Current (Non−Repetitive)	I_{TSM}	200 (50Hz)	A
		220 (60Hz)	
I^2t Limit Value	I^2t	200	A^2s
Repetitive Peak Surge On−State Current (Note 1)	I_{TRM}	1300	A
Critical Rate of Rise of On−State Current (Note 2)	di / dt	100	A / μs
Peak Gate Power Dissipation	P_{GM}	5	W
Average Gate Power Dissipation	$P_{G\ (AV)}$	0.5	W
Peak Forward Gate Voltage	V_{FGM}	10	V
Peak Reverse Gate Voltage	V_{RGM}	−5	V
Peak Forward Gate Current	I_{GM}	2	A
Junction Temperature	T_j	−40~125	°C
Storage Temperature Range	T_{stg}	−40~125	°C

Note 1: $C_M \leq 500\mu F$, $t_w \leq 300\mu s$, $V_D \leq 350V$

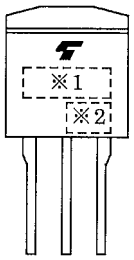
Note 2: di / dt Test condition

V_{DRM} = 0.5 × Rated, $I_{TM} \leq 25A$, $t_{gw} \geq 10\mu s$, $t_{gr} \leq 250ns$, $i_{gp} = I_{GT} \times 2.0$

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

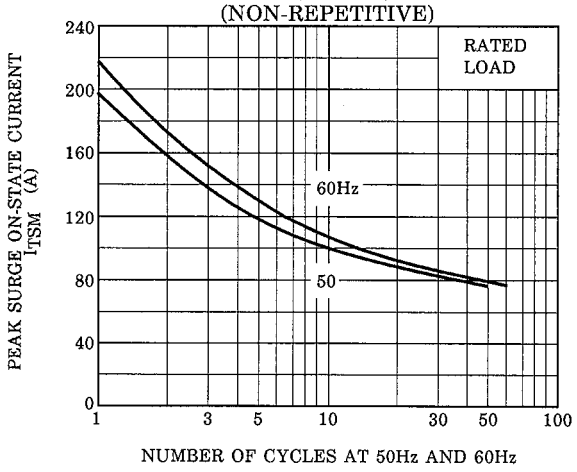
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Repetitive Peak Off−State Current and Repetitive Peak Reverse Current	I_{DRM} I_{RRM}	V_{DRM} = V_{RRM} = Rated	—	—	10	μA
Peak On−State Voltage	V_{TM}	I_{TM} = 25A	—	—	1.5	V
Gate Trigger Voltage	V_{GT}	V_D = 6V, R_L = 10Ω	—	—	1.0	V
Gate Trigger Current	I_{GT}		—	—	20	mA
Gate Non−Trigger Voltage	V_{GD}	V_D = Rated × 2 / 3, Tc = 125°C	0.2	—	—	V
Critical Rate of Rise of Off−State Voltage	dv / dt	V_{DRM} = Rated,Tc = 125°C, Exponential Rise	—	50	—	V / μs
Holding Current	I_H	V_D = 6V, I_{TM} = 1A	—	—	40	mA
Latching Current	I_L	V_D = 6V, f = 50Hz, t_{gw} = 100μs, i_G = 40mA	—	—	60	mA
Thermal Resistance	$R_{th\ (j-a)}$	Junction to Ambient	—	—	70	°C / W

MARKING

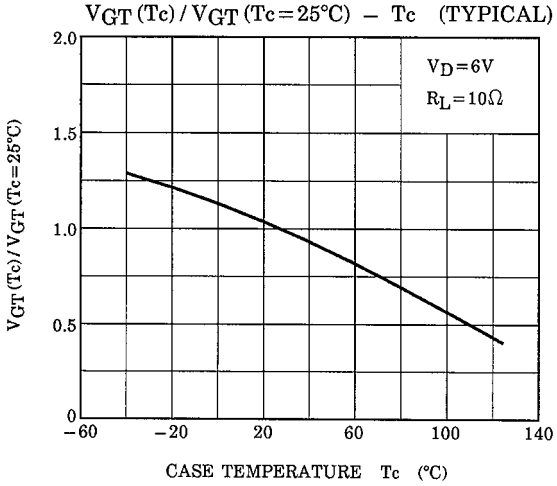


*1	TYPE NAME	S6744	MARK	S6744
*2	Lot Number Month (Starting from Alphabet A) Year (Last Decimal Digit of the Current Year)		Example 8A : January 1998 8B : February 1998 8L : December 1998	

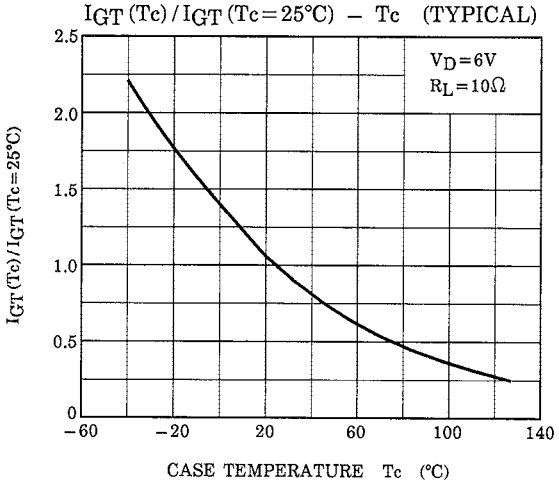
SURGE ON-STATE CURRENT
(NON-REPETITIVE)



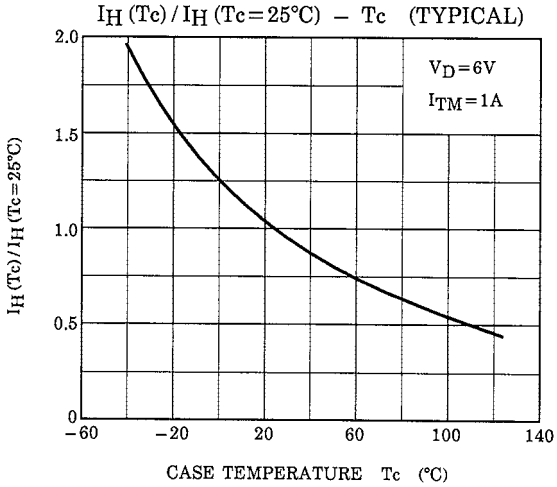
V_{GT} (Tc) / V_{GT} (Tc = 25°C) – Tc (TYPICAL)



I_{GT} (Tc) / I_{GT} (Tc = 25°C) – Tc (TYPICAL)



I_H (Tc) / I_H (Tc = 25°C) – Tc (TYPICAL)



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