Rev.0.11

Data Sheet

S6D04H0

-X01

-X02

MOBILE DISPLAY DRIVER IC

TRADEMARK & COPYRIGHT INFORMATION

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REVISION HISTORY

Rev.#	Date	History	Author
0.11	May `09	Modify Table8 – add power condition in sleep-in current Modify Table8 – change power condition in LCD source driver output on Resistance Modify Table8 – Operating current1: memory access speed Mhz → fps	
0.10	Apr `09	Copyright © 2008 to 2009 update Modify Table8 - AVDD, GVDD add Modify Table4 - DB[17:0] Pin usage comment add Add Minimum NHW[7:0](F2h command) Modify Table110 - HBLK_SRC[2:0]=001, 010 set disable Modify Figure53 - Note added Modify Figure54 - Note added Serial Read at 1para command - Comment added(no dummy read) Add Description - RDCABCMB is valid in case that BCTRL(WRCTRLD 53h)=1 Add Note at Table140 - Maximum Rating Voltage should not be exceed 25volt Add restriction at BRMIN command(5Eh command) Modify Table92 - D[1:0] Control at VGL Delete Note - RGB_MODE=0 removed Add Test Key Comment(F0h, F1h command) Modify SEQ1,2,3,4,5 default value(F4h command) Modify MTP Sequence Add Initial sequence - Figure59 Modify Timing Diagram – Figure114 Add note – Table140 D1 part Modify Table8 – Output voltage deviation GVDD → AVDD	
0.00	Oct `08	1. Initial Release	

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Preface

About This Data Sheet

This document is to provide a complete data sheet of S6D04H0 IC design.
It also provides useful information to those who works on a panel module or a set

IMPORTANT NOTICE

Precautions against Light

The conductivity of a semiconductor is strongly influenced by electro-magnetic radiation such as visible light, infrared light, ultraviolet light, or gamma radiation. When light is absorbed, electron-hole pairs are generated raising the conductivity of the material, eventually altering the electrical characteristics of the IC. Therefore, if the packages that expose IC's to external light sources, such as COB, COG, TCP, and COF, are used, effective means to shield the IC from the light coming in all directions – top, bottom, and the sides – must be devised. Full observation of the following precautions is strongly recommended.

1. Make sure that the IC and substrate (board or glass) are protected from a stray light.
2. Always test and inspect products under the environment with no light penetration.

CHAPTER 1

OVERVIEW

1. OVERVIEW

1.1. INTRODUCTION

S6D04H0 is a single-chip display driver IC for a TFT-LCD panel. S6D04H0 has source drivers with built-in memory, gate drivers and power sources. S6D04H0 can support a TFT-LCD panel up to a resolution of 240-RGB x 320-dot graphics with 262k color.

1.2. PRODUCT OPTIONS

S6D04H0 may offer more than one option in order to meet customer-specific functions from the customers. Table 1 describes its functions.

Table 1. List of S6D04H0 Options.

Options	Remarks
-X01,X02	Reference Design of S6D04H0

1.3. FEATURES

S6D04H0 offers the following key features:

- Single chip TFT-LCD controller and driver with Display RAM.
- Display resolution: 240*RGB(H) *320(V)
- Display data RAM (frame memory): 240 x 320 x 18-bit = 1,382,400 bits
- Output:
  - Source output
  - Common electrode output
  - Gate output
- Display mode (Color mode)
  - Full color mode (Idle mode off): 262k-color
  - 65k-color
  - Reduce color mode (Idle mode on): 8-color
- MPU Interface:
  - 3-wire 9–bit data serial interface
  - 4-wire 8–bit data serial interface
  - 8 / 9 / 16 / 18bit parallel interface with 80-series MPU
  - 8 / 9 / 16 / 18bit parallel interface with 68-series MPU
  - 6 / 18bit RGB interface
- VSYNC Interface with 80-series MPU
- Display features
  - CABC (MIE2.5G) for saving current consumption
  - Partial display mode
  - Line inversion for low cross talk
- MIPI DCS support
- MIE (Mobile Image Enhancement) function
  - Adaptive luminance/contrast enhancement function
  - Reduce the power consumption of backlight
- On chip
  - DC/DC converter
  - Adjusted VCOM generation
  - Oscillator for display clock generation
  - Timing generation

- Non-Volatile Memory (NVM)
  - 7bits for VCOM adjustment
- Driving Algorithm
  - Line inversion, frame inversion
- Supply voltage range
  - Analog supply voltage range for VCI to VSSA: 2.4V ~ 3.3V
  - I/O supply voltage range for VDD3 to VSS: 1.65V ~ 3.3V
- Output voltage levels
  - Source output voltage range for GVDD to VSSA: 2.46V to 5V
  - Power supply for driver circuit range for AVDD to VSSA: 4.2V to 6.0V
  - Max 6.0V Common electrode output voltage range for VCOM
  - Positive Gate output voltage range for VGH to VSSA: 8.4V to 16.5V (Note 3)
  - Negative Gate output voltage range for VGL to VSSA: –15V to –6.3V (Note 3)
- Lower power consumption, suitable for battery operated systems
- Optimized layout for COG assembly
- Operate temperature range: –40℃ to +85℃

Note.

1. Blank display means: Normal White Display = White, Normal Black Display = Black.
2. AVDD Min: When VCI1 = 2.1V, AVDD Max: When VCI1=3.0V
3. |VGH| & |VGL| Min: When VCI1 = 2.1V, |VGL| Max: When VCI1=3.0V, |VGH - VGL| Max: 30.0V
4. |VGH| Max should be lower than or equal to 16.5V in normal operating condition,
5. NVM and EEPROM mean MTP (Multi Time Programmable) in this data sheet.

1.4. BLOCK DIAGRAM

1.4.1. MODULE LEVEL

Figure 1 shows the block diagram of a mobile display panel module and related interface signals required by set makers and module makers. Level I interface signals are usually required by a set maker who would then request the display module such a function, and Level II interface signals are required by a display module maker for its own purpose.

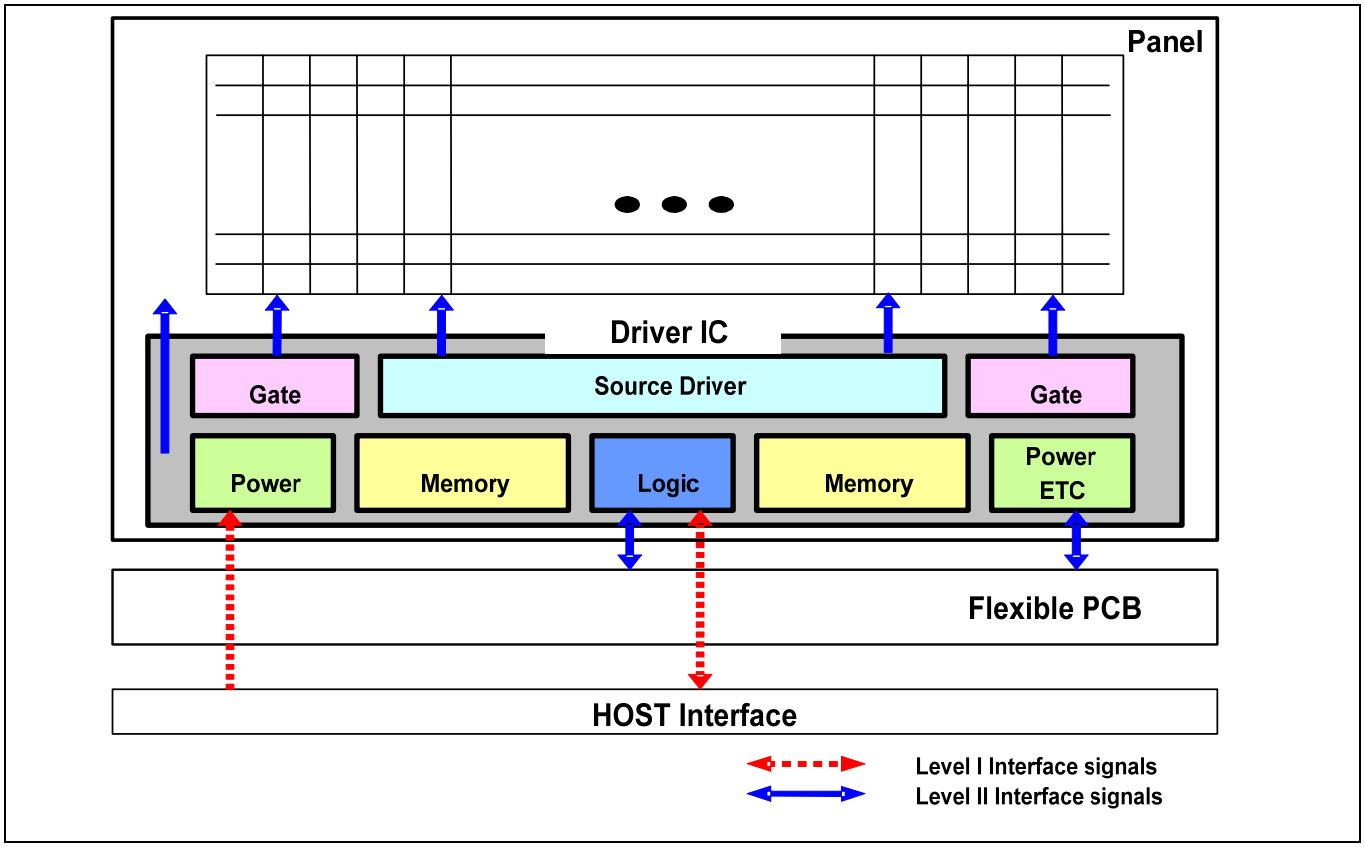


Figure1. Interface Signal Flow of a Mobile Display Panel Module.

There are also Level III signals which is for the internal use only for the driver IC itself. These signals may not necessarily be released to the customer since it is designed for a specific manufacturing purpose and are supposed to be hidden to customers.

This data sheet only provide a guideline to Level I and II interface signals since some of specifications related to Level I and II need a margin on IC side and would not be necessarily the same as the one in Level I and II specification even though both uses the same interface signals. This is mainly due to the parasitic and design requirements within the flexible PCB used by a display module maker. IC specification will offer related information among Level I/II on how each interface signals interact each other.

1.4.2. FUNCTIONAL BLOCK DIAGRAM OF THE IC

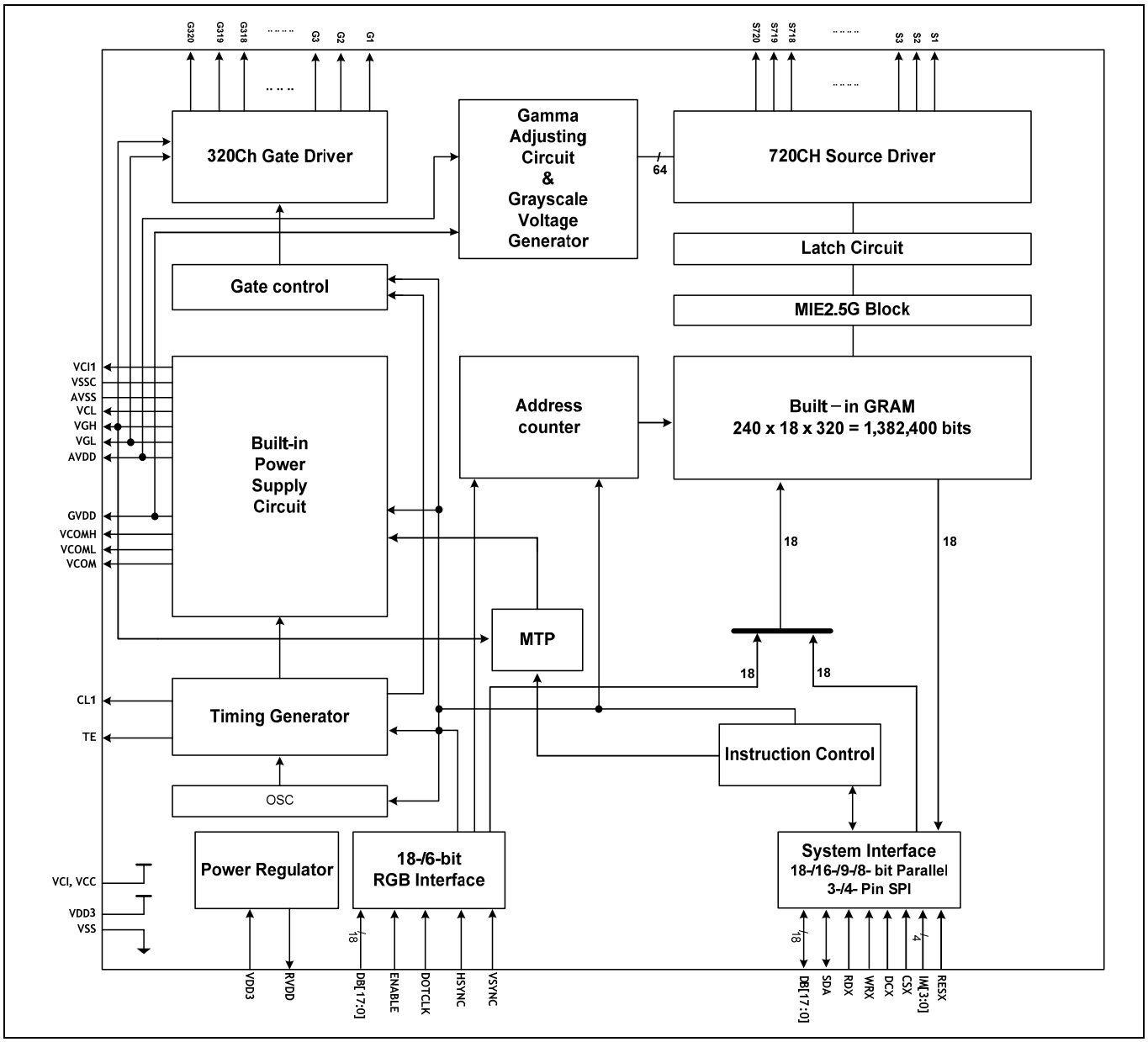


Figure2. S6D04H0 Block Diagram

1.5. PAD INFORMATION

1.5.1. CONFIGURATION OF SIGNAL PADS

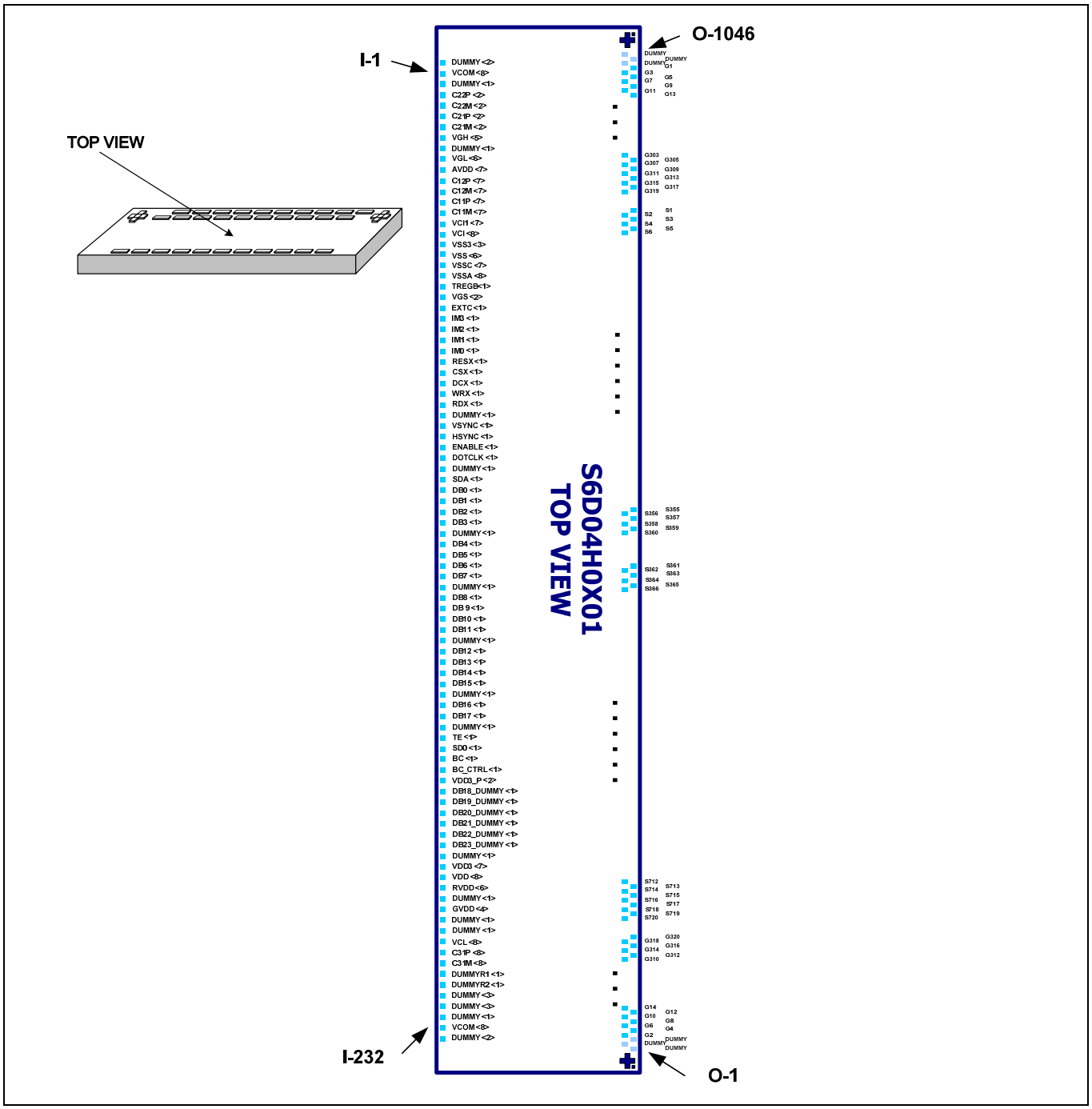


Figure3. S6D04H0 PAD Configuration

Note.

Pattern Surface

1.5.2. BUMP INFORMATION

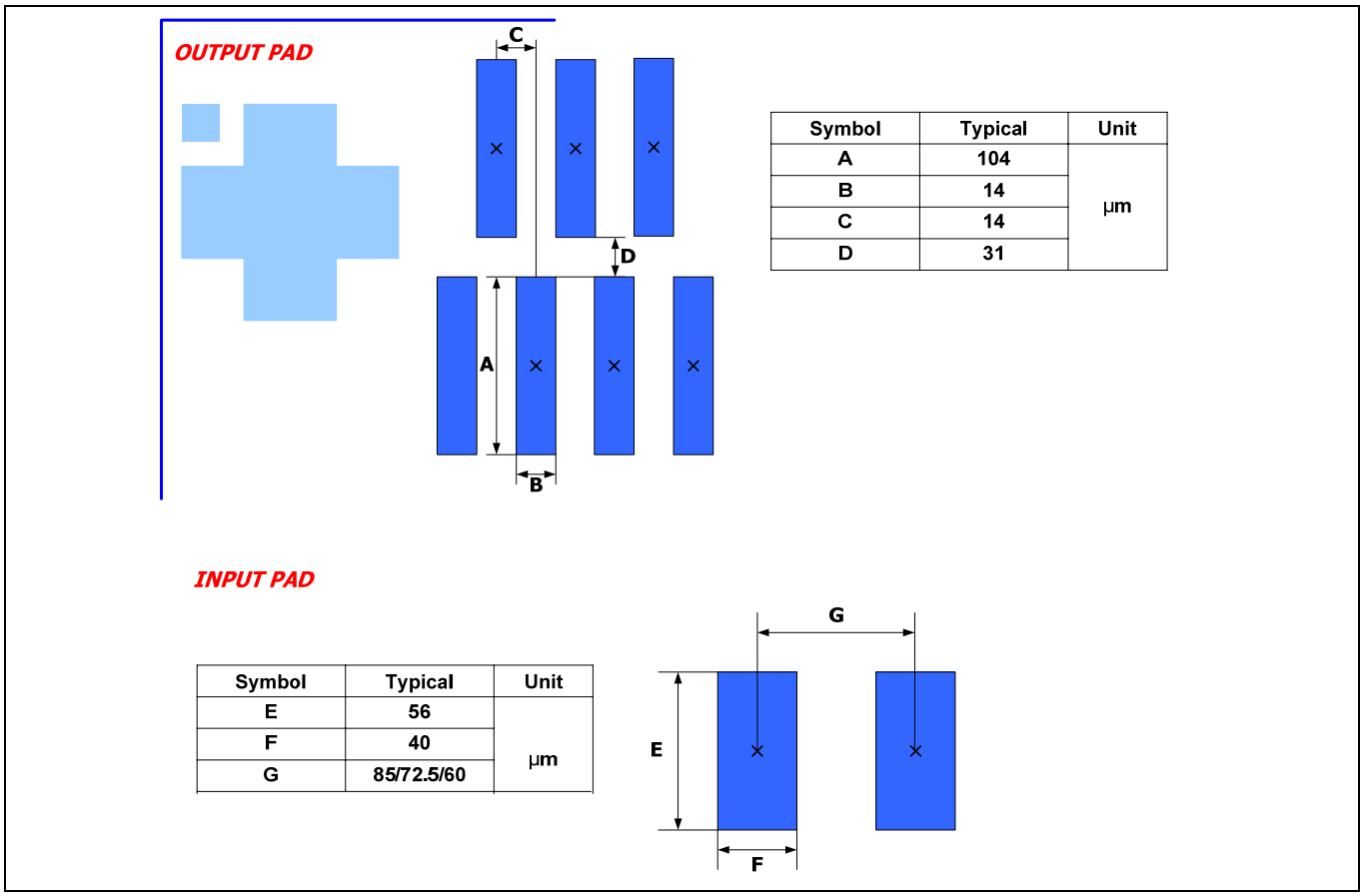
Table 2. Bump Information

Item	Pad No.	Size		Unit
		X	Y	
Chip Size	-	15260	720	μm
Pad Pitch	Input Side	85 / 72.5 / 60		
	Output Side	14		
Bumped Pad Top Size	Input Side	40±2	56±2	
	Output Side	14±2	104±2	
Bumped Pad Height	Height In Wafer	15±3		
	Tolerance In Chip	Under 2		
	Dimple Height	Under 2		
Chip Thickness	-	300±10		

Note.

1. Scribe lane 80um included in this die size
2. Wafer thickness can be varied with the customer's needs.

1.5.3. BUMP DIMENSION



Symbol	Typical	Unit
A	104	µm
B	14	
C	14	
D	31	

Symbol	Typical	Unit
E	56	µm
F	40	
G	85/72.5/60	

Figure4. Bump Dimension

1.5.4. ALIGN KEY

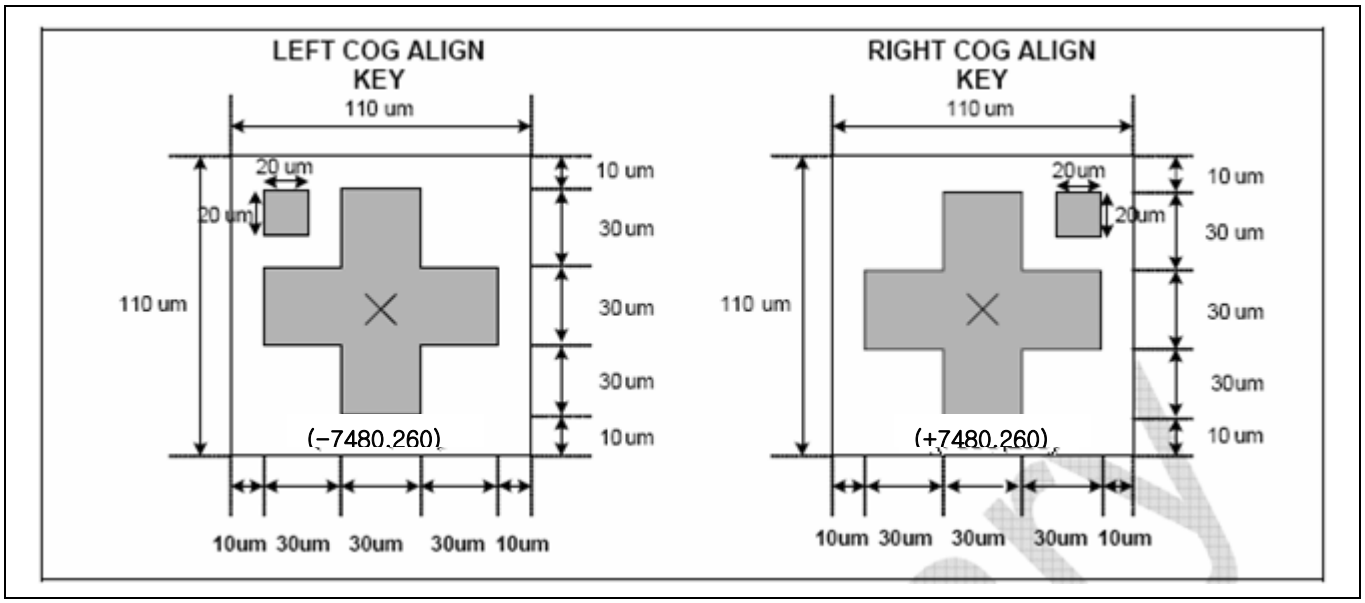


Figure5. COG Align Key Configuration and Coordinate

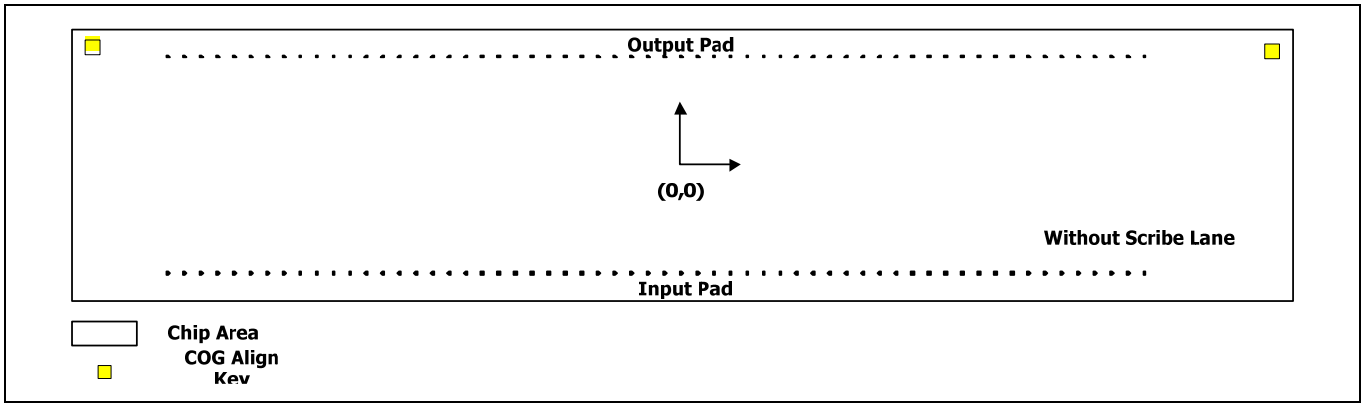


Figure6. COG Align Key Arrangement Layout

1.6. DESCRIPTION OF SIGNAL PADS

1.6.1. POWER SUPPLY PINS

Table 3. Power Supply Pins

Symbol	Name	Description
VDD3	I/O voltage	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)
VDD3_P	LED driver Power	Power supply for LED driver interface. (1.65 ~ 3.3 V) If LED driver is not used, fix this pin at VSS.
VCI	Analog Power	High voltage power supply for analog circuit blocks (2.4 ~ 3.3 V)
VDD	Regulated Voltage	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad
VSS3	I/O Ground	System ground level for I/O circuits.
VSS	Logic Ground	System ground level for logic blocks
VSSA	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.
VSSC	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise

1.6.2. INTERFACE LOGIC PINS

Table 4. Interface Logic Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>Selects the MPU interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface mode</th><th>Data pad</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit Parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 16-bit Parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 9-bit Parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit Parallel I/F</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data Serial interface I</td><td>SDA : In/Out</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data Serial interface I</td><td>SDA : In/Out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>68 MCU 8-bit Parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>68 MCU 16-bit Parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>68 MCU 9-bit Parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>68 MCU 18-bit Parallel I/F</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data Serial interface II</td><td>SDI : In /
SDO : Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data Serial interface II</td><td>SDI : In /
SDO : Out</td></tr>
</table>
MPU Parallel interface bus and serial interface select
* : Fix this pin at VDD3 or VSS.</td></tr>
<tr><td>RESX</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>EXTC</td><td>I</td><td>Select to access Level2 command (“Low” : Leve1 only, “High” : Level1 and Level2”)</td></tr>
<tr><td>CSX</td><td>I</td><td>Chip select input pin (“Low” enable).
This pin can be permanently fixed “Low” in MPU interface mode only.
* note1,2</td></tr>
<tr><td>DCX (SCL)</td><td>I</td><td>This pin is used to select “Data or Command” in the parallel interface or 4-wire 8-bit serial data interface.
When DCX = ’1’, data is selected.
When DCX = ’0’, command is selected.
This pin is used serial interface clock in 3-wire 9-bit serial data interface.
If not used, this pin should be connected to VDD3 or VSS.</td></tr>
</table>

Symbol	I/O	Description
RDX (E)	I	This pin is used to “Read Clock” in 80-series parallel interface. This pin is used to “Read / Write Clock” in 68-series parallel interface. If not used, this pin should be connected to VDD3 or VSS.
WRX (RWX)	I	This pin is used to “Write Clock” in 80-series parallel interface. This pin is used to select “Read / Write Operation” in 68-series parallel interface. This pin is used serial interface clock in 4-wire 8-bit serial data interface. If not used, this pin should be connected to VDD3 or VSS.
DB[17:0]	I/O	When RGB I/F, DB[17:0] are used to RGB interface data bus. When MPU I/F, DB[17:0] are used to MPU parallel interface data bus. If not used, fix this pin at VDD3 or VSS.
SDI / SDA	I/O	When IM[3] : Low, Serial in/out signal. When IM[3] : High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDD3 or VSS.
SDO	O	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	Pixel clock signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
VSYNC	I	Vertical sync. Signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
HSYNC	I	Horizontal sync. Signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
ENABLE	I	Data enable signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.

Note.

1. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.
2. When CSX=’1’, there is no influence to the parallel and serial interface.

1.6.3. DRIVER INPUT / OUTPUT PINS

Table 5. Driver Input / Output Pins

Symbol	I/O	Description
S1 to S720	O	Source driver output pads.
G1 to G320	O	Gate driver output pads
VCI1	O	An internal reference voltage generated between VCI and VSSA. Reference input voltage for 1st and 3rd step up circuit.
AVDD	O	Output voltage of 1st step up circuit (2 x VCI1). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.
VGH	O	Positive power output of the 2nd step up circuit. Connect a capacitor for stabilization. Gate “ON” level voltage.
VGL	O	Negative power output of the 2nd step up circuit. Connect a capacitor for stabilization. To protect IC against Latch up, connect the cathode of the schottky diode to the VSS pad. And the anode of the schottky diode to the VGL pad. Refer to application circuit.
VCL	O	Power supply for generating VCOM low level. 3rd step up circuit output voltage. Connect a capacitor for stabilization.
C11P, C11M C12P, C12M	–	Connect the charge-pumping capacitor for generating AVDD level.
C21P, C21M C22P, C22M	–	Connect the charge-pumping capacitor for generating VGH, VGL level.
C31P, C31M	–	Connect the charge-pumping capacitor for generating VCL level.
GVDD	O	High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VGS	I	Low reference voltage for grayscale voltage generator. Connect an external resistor or to system ground.
VCOM	O	Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.
BC	O	Output pin for PWM(Pulse Width Modulation) signal of LED driving. If not used, open this pad.
BC_CTRL	O	Output pin for enabling LED driving. If not used, open this pad.

1.6.4. TEST PINS

Table 6. Test Pins

Symbol	I/O	Description
TREGB	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
DUMMYR1 DUMMYR2	I	Contact resistance measurement pad. In normal operation, leave this unconnected. These pads are at VSS level. When measuring an ohmic resistance of the contact, do not apply any power.
TMODE[3:0]	–	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
TMUX[2:0]	–	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
EXCLK	–	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
DB18_DUMMY ~ DB23_DUMMY	–	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
VCIR_EXIN	–	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
VGH_DUMMY	–	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
VGL_DUMMY	–	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
DUMMY	–	Dummy pin. Leave these pads open.

CHAPTER 2

ELECTRICAL SPECIFICATION

2. ELECTRICAL SPECIFICATIONS

2.1. ABSOLUTE MAXIMUM RATINGS

Table 7. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage for logic block	VDD – VSS	–0.3 to +3.3	V
Supply voltage for I/O block	VDD3 – VSS	–0.3 to +5.0	V
Supply voltage for step-up circuit	VCI – VSS	–0.3 to +5.0	V
LCD Supply Voltage range	AVDD – VSS	–0.3 to +6.5	V
	VGH – VSS	–0.3 to +22.0	V
	VSS – VGL	–0.3 to +22.0	V
	VSS – VCL	–0.3 to +5.0	V
	| VGH – VGL |	–0.3 to +33	V
Input Voltage range	Vin	–0.3 to VDD3+0.5	V
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–55 to +110	°C

Note.

1. The absolute maximum rating is the limit value. When the IC is exposed to the operating environment beyond this range, the IC does not assure normal operations and may be damaged permanently, not be able to be recovered.
2. The operating temperature is the range of device-operating temperature. They do not guarantee chip performance.

CAUTION

Stresses above these absolute maximum ratings may cause permanent damage. These are stress ratings only and functional operation at these conditions is not implied. Exposure to maximum rating conditions for extended periods may reduce device reliability.

2.2. DC ELECTRICAL CHARACTERISTICS

Table 8. DC Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Pin
Power voltage(1)	VDD3		1.65	1.8	3.3	V	VDD3
Power voltage(2)	VCI		2.4	–	3.3	V	VCI
LCD driving voltage	AVDD		4.2	5.0	6.0	V	AVDD
	VGH		8.4		16.5	V	VGH
	VGL		–15		–6.3	V	VGL
	VGH-VGL				30.0	V	VGH, VGL
	VCL		–3		–2.1	V	VCL
	VCI–VCL				6.0	V	VCI, VCL
	GVDD		2.46	4.5	5.0	V	GVDD
High Level Input Voltage	VIH		0.7V DD3		VDD3	V	All input pins
Low Level Input Voltage	VIL		0.0		0.3V DD3	V	All input pins
High Level Output Voltage	VOH	IOH = –0.5mA	0.8V DD3		VDD3	V	DB[17:0], TE
Low Level Output Voltage	VOL	IOH = +0.5mA	0.0		0.2V DD3	V	DB[17:0], TE
Input Current	ILI1	GND ≤ VIN ≤ VDD3	-1.0		1.0	uA	CSX,RDX,WRX, DB[17:0],& RESX
Output voltage deviation (Mean value) AVDD=5.0V,GVDD=4.5V	ΔVo	AVDD–0.8 ≤ Vso	–	–	±55	mV	S[1:720]
		VSS+0.8 < Vso < AVDD–0.8	–	–	±25		
		Vso ≤ VSS + 0.8	–	–	±55		
Sleep In Current	IDD_{SI}_VDD3	VCI=2.8V VDD3=1.8V Ta=25℃	–	–	25	uA	VSS
	IDD_{SI}_VCI		–	–	5	uA	VSS
Operating Current 1	IDD_{OP1}_ VDD3	30fps memory access (VCI=2.8v,VDD3=1.8v Load=100pf. Ta=25℃)	–		*1.8	mA	
	IDD_{OP1}_VCI	30fps memory access	–		8.8	mA	

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Pin
		(VCI=2.8v,VDD3=1.8v Load=100pf. Ta=25℃)					
Operating Current 2	IDD_{OP2}_ VDD3	Memory Not Access (VCI=2.8v,VDD3=1.8v Load=100pf. Ta=25℃)	–		*500	uA	
	IDD_{OP2}_VCI	Memory Not Access (VCI=2.8v,VDD3=1.8v Load=100pf. Ta=25℃)	–		8.8	mA	
Internal Oscillator frequency	Fosc1	Frame freq. = 60 Hz Display line = 320 Ta = 25℃	8.55 (8.1)	9	9.45 (9.9)	MHz	*(Ta= All Temp)
Step-up output efficiency	AVDD	ILOAD = 4 mA	90	95	–	%	
	VGH	ILOAD = 0.1 mA	90	95	–	%	
	VGL	ILOAD = 0.1 mA	90	95	–	%	
	VCL	ILOAD = 0.3 mA	90	95	–	%	
LCD Gate driver output On resistance	Ronvgh	VGH = 8.4V VGL = ~6.3V	–	–	7	kΩ	
	Ronvgl		–	–	7	kΩ	
LCD source driver output On resistance	Ronp	AVDD = 5.0V VSSA = 0V	–	–	30	kΩ	
	Ronn		–	–	30	kΩ	
LCD Binary driver Output On resistance	Ronpb	GVDD = 4.5V VSSA = 0V	–	–	300	kΩ	
	Ronnb		–	–	300	kΩ	

Note.

DC Electrical Characteristics(Total): -40℃ to +85℃

Fosc: 25℃

Ivdd: 25℃(no load), 25℃(EDS 100pF load)

∗ : Don't applied to MIE function

2.3. AC CHARACTERISTEICS

2.3.1. 80-SERIES 8/ 9/ 16/ 18 BIT PARALLEL INTERFACE

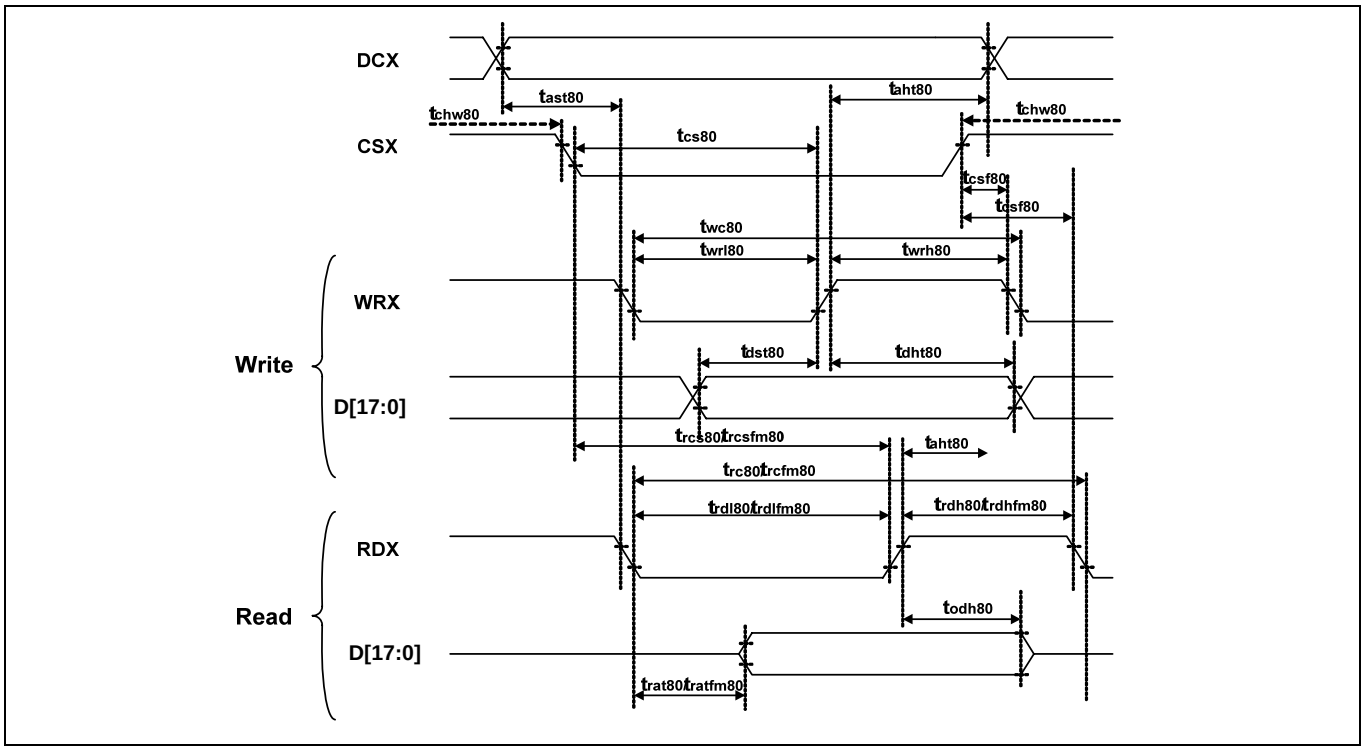


Figure7. 80-Series Parallel Interface

Table 9. AC Characteristics of 80-Series Parallel Interface

Signal	Parameter	Symbol	Min	Max	Unit	Description
DCX	DCX setup time	tast80	0	–	ns	
	DCX hold time	taht80	10	–	ns	
CSX	CSX “H” pulse width	tchw80	0	–	ns	
	Chip select setup time(write)	tcs80	15	–	ns	
	Chip select setup time (Read ID)	trcs80	45	–	ns	
	Chip select setup time (Read FM)	trcsfm80	355	–	ns	
	Chip select wait time(write/read)	tcsf80	10	–	ns	
WRX	Write cycle	twc80	66	–	ns	
	Control pulse H duration	twrh80	15	–	ns	
	Control pulse L duration	twrl80	15	–	ns	
RDX(ID)	Read cycle	trc80	160	–	ns	When read
	Control pulse H duration	trdh80	90	–	ns	ID data

Signal	Parameter	Symbol	Min	Max	Unit	Description
	Control pulse L duration	trdl80	45	–	ns	
RDX(FM)	Read cycle	trcfm80	450	–	ns	When read from frame memory
	Control pulse H duration	trdhfm80	90	–	ns	
	Control pulse L duration	trdlfm80	355	–	ns	
D[18:0]	Write data setup time	tdst80	10	–	ns	For maximum CL = 30 pF For minimum CL = 8 pF
	Write data hold time	tdht80	10	–	ns	
	Read access time	trat80	–	40	ns	
	Read access time (FM)	tratfm80	–	340	ns	
	Read output disable time	todh80	20	80	ns	

Note.

Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V, VSS=0V

2.3.2. 68-SERIES 8/ 9/ 16/ 18 BIT PARALLEL INTERFACE

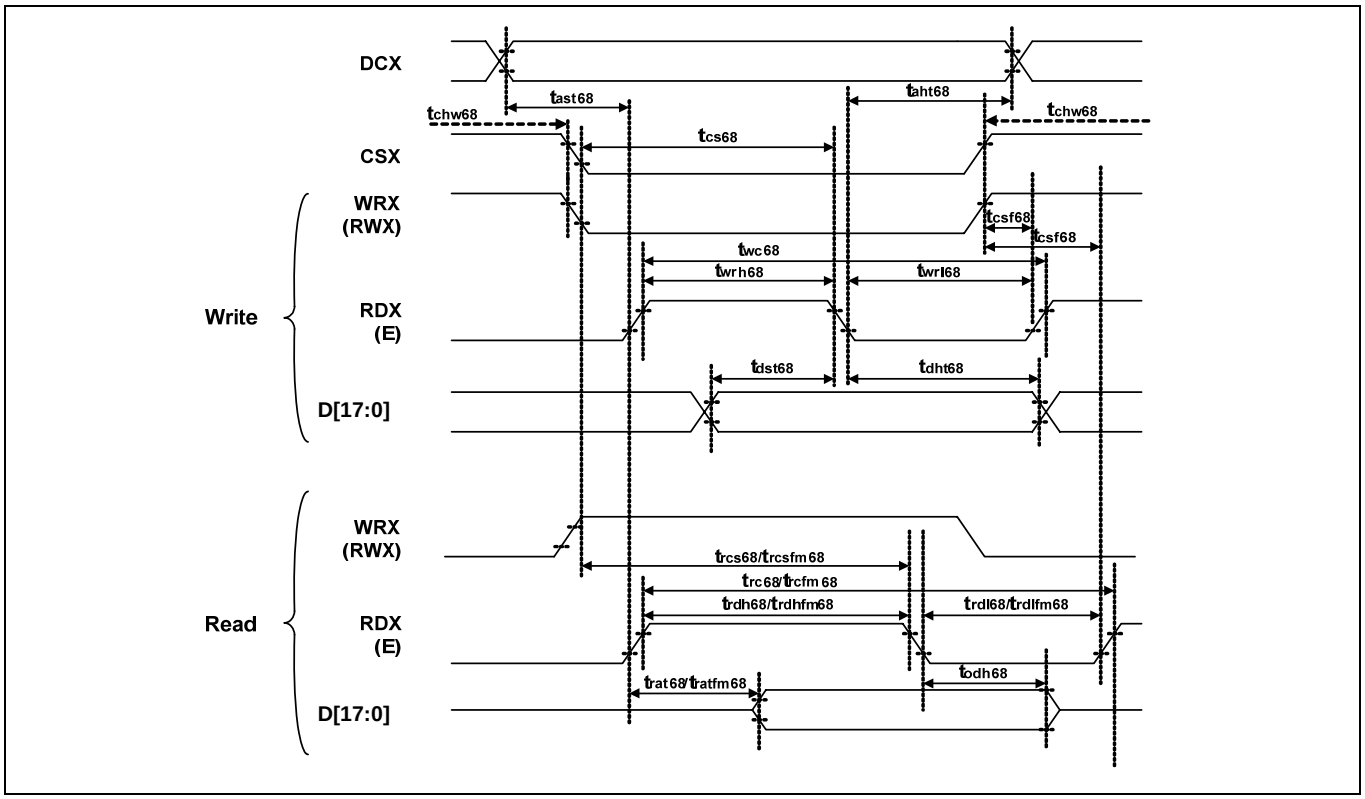


Figure8. 68-Series Parallel Interface

Table 10. AC Characteristics of 68-Series Parallel Interface

Signal	Parameter	Symbol	Min	Max	Unit	Description
DCX	DCX setup time	tast68	0	–	ns	
	DCX hold time	taht68	10	–	ns	
CSX	CSX “H” pulse width	tchw68	0	–	ns	
	Chip select setup time(write)	tcs68	15	–	ns	
	Chip select setup time (Read ID)	trcs68	45	–	ns	
	Chip select setup time (Read FM)	trcsfm68	355	–	ns	
	Chip select wait time(write/read)	tcsf68	10	–	ns	
WRX	Write cycle	twc68	66	–	ns	
	Control pulse H duration	twrh68	15	–	ns	
	Control pulse L duration	twrl68	15	–	ns	
RDX(ID)	Read cycle	trc68	160	–	ns	When read ID data
	Control pulse H duration	trdh68	90	–	ns	

Signal	Parameter	Symbol	Min	Max	Unit	Description
	Control pulse L duration	trdl68	45	–	ns	
RDX(FM)	Read cycle	trcfm68	450	–	ns	When read from frame memory
	Control pulse H duration	trdhfm68	355	–	ns	
	Control pulse L duration	trdlfm68	90	–	ns	
DB[23:0]	Write data setup time	tdst68	10	–	ns	For maximum CL = 30 pF For minimum CL = 8 pF
	Write data hold time	tdht68	10	–	ns	
	Read access time	trat68	–	40	ns	
	Read access time (FM)	tratfm68	–	340	ns	
	Read output disable time	todh68	20	80	ns	

Note.

Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V, VSS=0V

2.3.3. 3-WIRE 9-BIT SERIAL INTERFACE

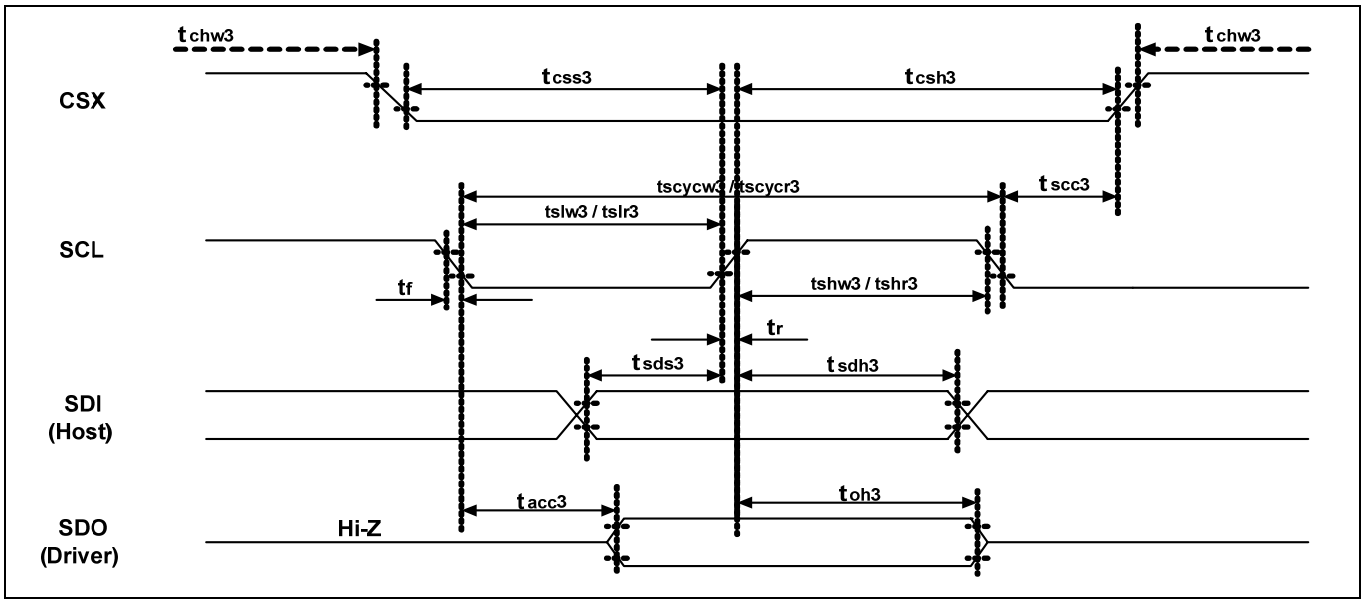


Figure9. 3-Wire 9-Bit Serial Interface

Table 11. AC Characteristics of 3-Wire 9-Bit Serial Interface

Parameter	Symbol	Conditions	Min	Max	Unit
Serial Clock Cycle(Write)	tscycw3	SCL	100	–	ns
SCL ”H” pulse width(Write)	tshw3	SCL	35	–	ns
SCL ”L” pulse width(Write)	tslw3	SCL	35	–	ns
Data setup time(Write)	tsds3	SDA	30	–	ns
Data hold time(Write)	tsdh3	SDA	30	–	ns
Serial Clock Cycle(Read)	tscycr3	SCL	150	–	ns
SCL ”H” pulse width(Read)	tshr3	SCL	60	–	ns
SCL ”L” pulse width(Read)	tslr3	SCL	60	–	ns
Access time	tacc3	SDO (Note2)	10	50	ns
Output disable time	toh3	SDO (Note2)	15	50	ns
CSX “H” pulse width	tchw3	CSX	40	–	ns
CSX–SCL time	tcssw3	CSX(Write)	60	–	ns
	tcshw3	CSX(Write)	65	–	ns

Note.

1. Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V, VSS=0V
2. For maximum CL = 30 pF, for minimum CL = 8 pF

2.3.4. 4-WIRE 8-BIT SERIAL INTERFACE

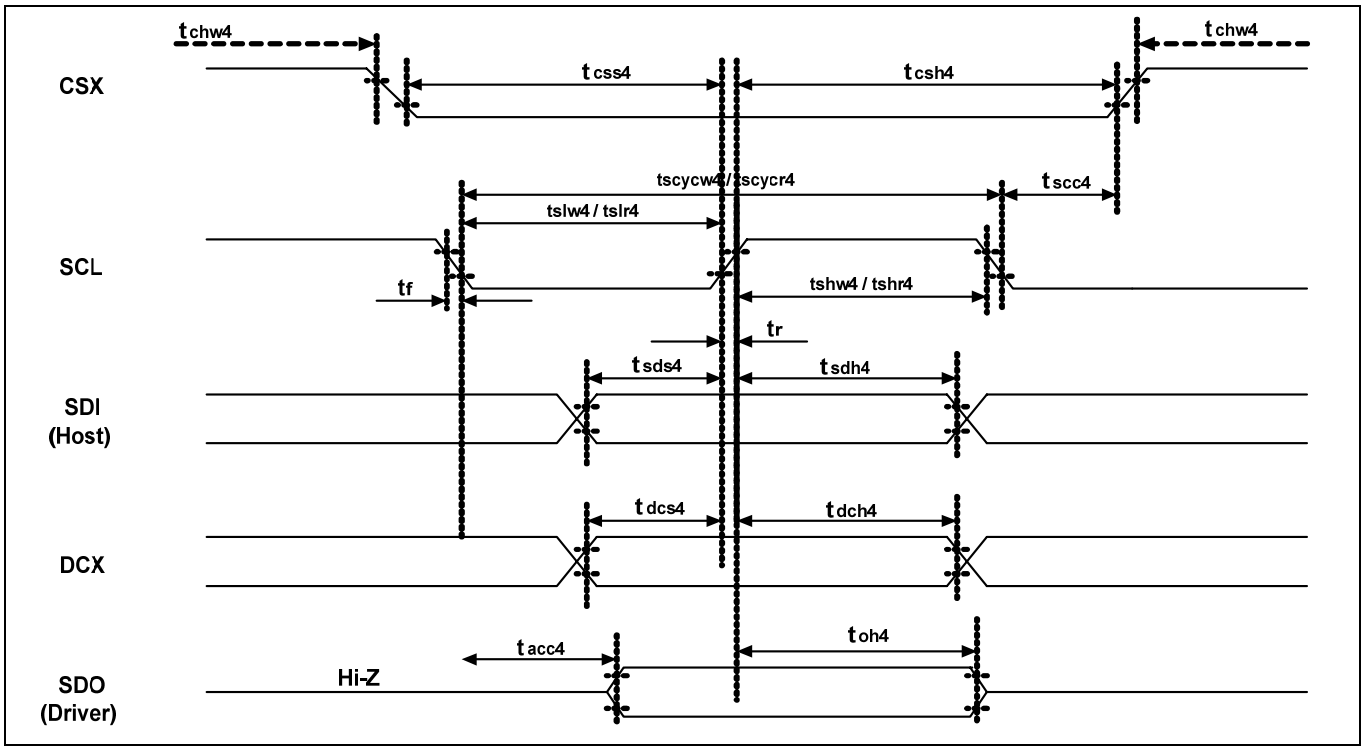


Figure10. 4-Wire 8-Bit Serial Interface

Table 12. AC Characteristics of 4-Wire 8-Bit Serial Interface

Parameter	Symbol	Conditions	Min	Max	Unit
Serial Clock Cycle(Write)	tscycw4	SCL	100	–	ns
SCL ”H” pulse width(Write)	tshw4	SCL	35	–	ns
SCL ”L” pulse width(Write)	tslw4	SCL	35	–	ns
Data setup time(Write)	tsds4	SDA	30	–	ns
Data hold time(Write)	tsdh4	SDA	30	–	ns
DCX setup time	tdcs4	DCX	30	–	ns
DCX hold time	tdch4	DCX	30	–	ns
Serial Clock Cycle(Read)	tscycr4	SCL	150	–	ns
SCL ”H” pulse width(Read)	tshr4	SCL	60	–	ns
SCL ”L” pulse width(Read)	tslr4	SCL	60	–	ns
Access time	tacc4	SDO (Note2)	10	50	ns
Output disable time	toh4	SDO (Note2)	15	50	ns
CSX “H” pulse width	tchw4	CSX	40	–	ns

Parameter	Symbol	Conditions	Min	Max	Unit
CSX–SCL time(Write)	tcssw4	CSX	60	–	ns
	tcshw4	CSX	65	–	ns

Note.

1. Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V, VSS=0V
2. Note2. For maximum CL = 30 pF, for minimum CL = 8 pF

2.3.5. RGB INTERFACE CHARACTERISTICS

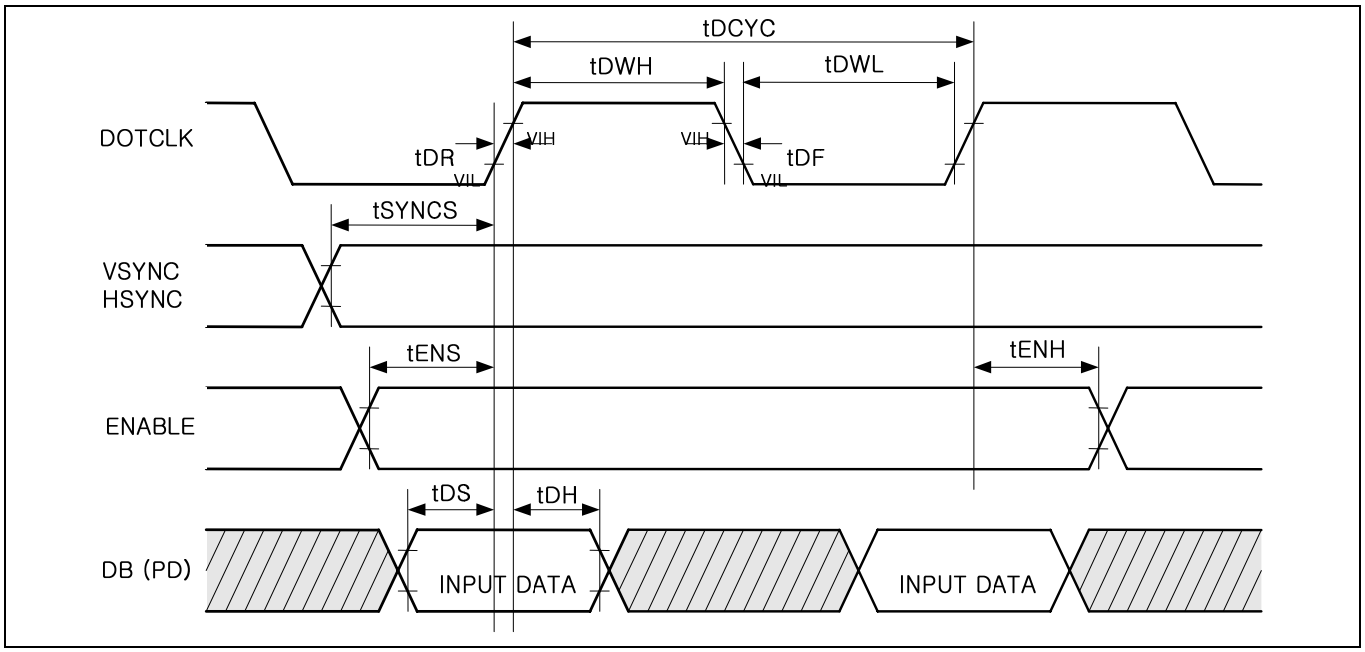


Figure11. RGB Interface

Table 13. RGB Interface AC Characteristics

(Ta = -40 ~+85 ℃, VDD3=1.65V~3.3V, VCI=2.4V~3.3V)

Parameter	Description	Min	Max	Unit
tDCYC	DOTCLK period	100	–	ns
tDWL	DOTCLK pulse width low	50	–	ns
tDWH	DOTCLK pulse width high	50	–	ns
tDR / tDF	DOTCLK rising / falling time	–	20	ns
tSYNCS	VSYNC, HSYNC setup	30	–	ns
tENS	ENABLE setup	50	–	ns
tENH	ENABLE hold	50	–	ns
tDS	Input Data setup	50	–	ns
tDH	Input Data hold	50	–	ns

Note.

1. VSYNC Low Pulse Width ≥1H
2. HSYNC Low Pulse Width ≥ 1 DOTCLK

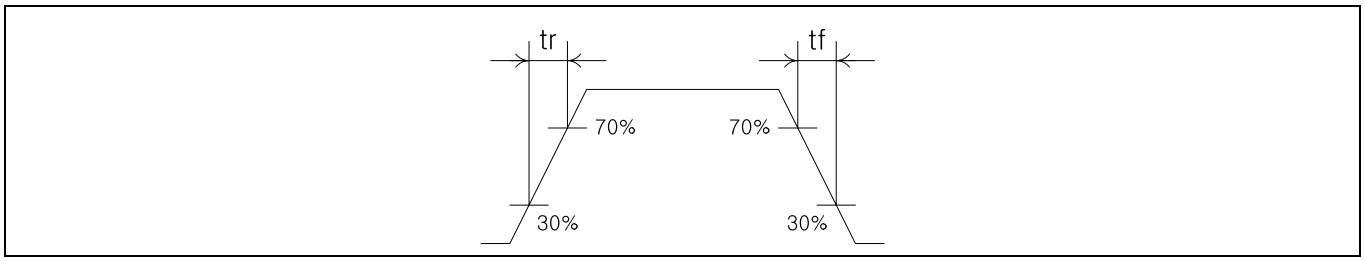


Figure12. Rising and Falling

Note.

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

2.3.6. TACC, TODH MEASUREMENT CONDITION

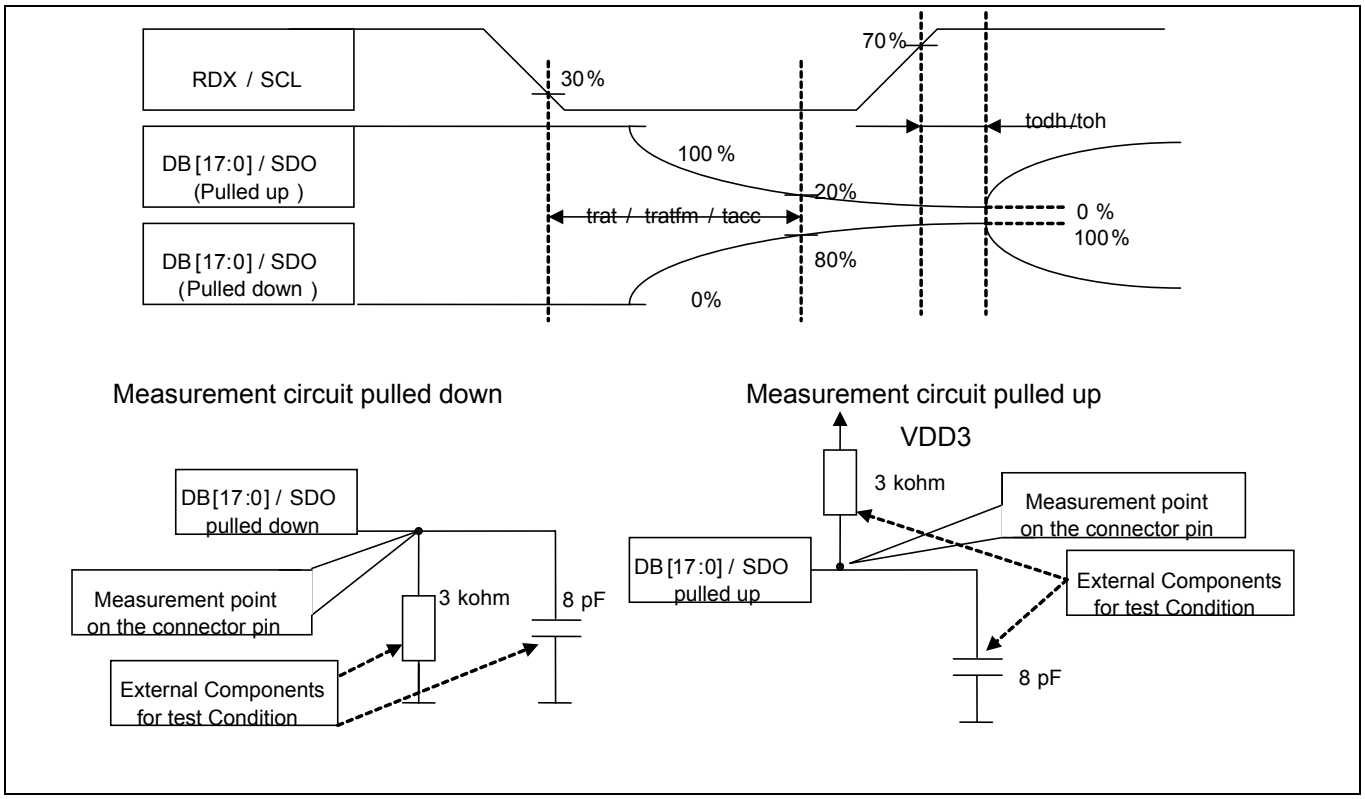


Figure13. Minimum Measurement Condition

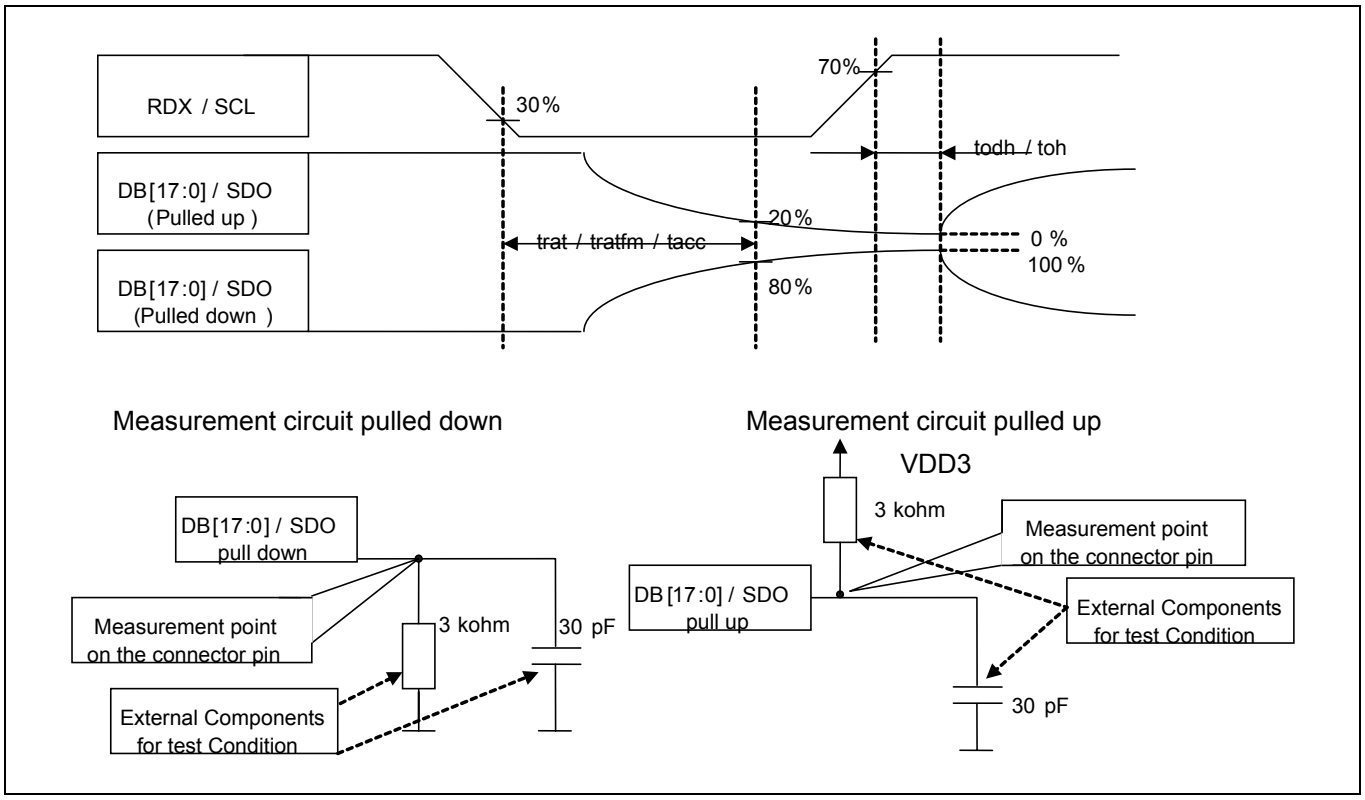


Figure14. Maximum Measurement Condition

2.3.7. RESET TIMING

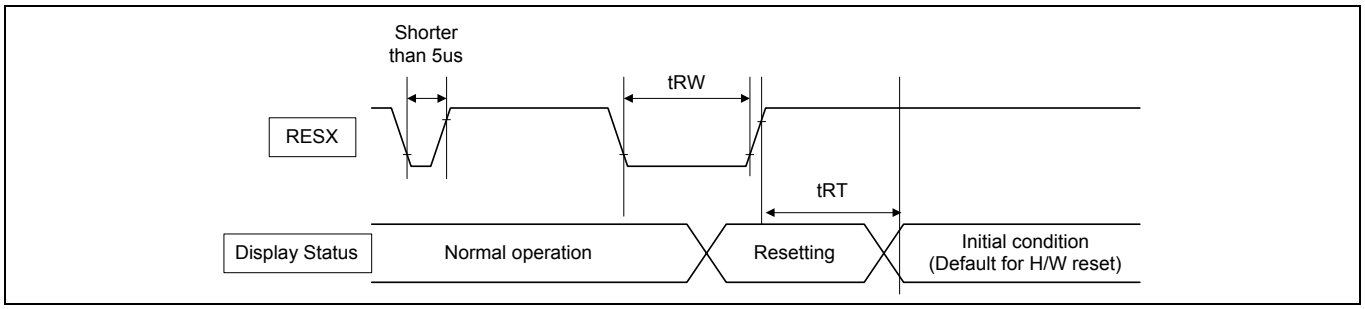


Figure15. Reset Timing

Table 14. Reset Input Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10	–	us
	tRT	Reset cancel	–	5 (note 5)	ms
			–	120 (note 6, 7)	ms

Note.

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

Table 15. Reset Operation According to Resx Pulse Width

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.

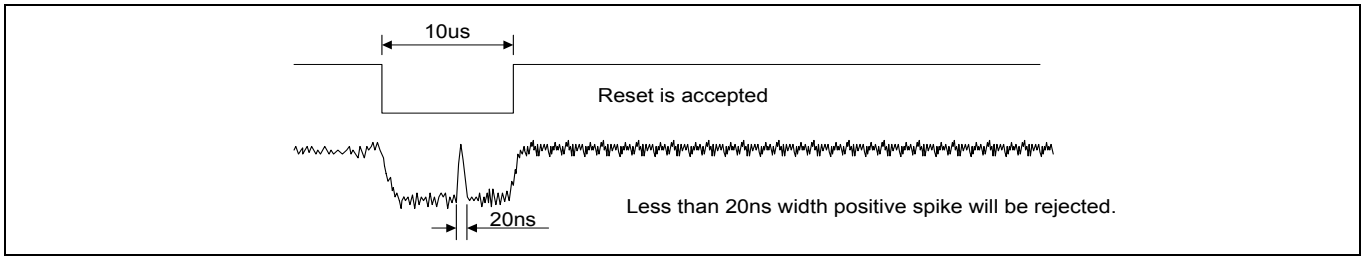


Figure16. Spike Rejection

4. Spike Rejection also applies during a valid reset pulse as shown below:
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also, Sleep Out command cannot be sent for 120msec.

CHAPTER 3

INTERFACE

3. INTERFACE

3.1. MPU INTERFACE

3.1.1. INTERFACE TYPE SELECTION

Selection of given interfaces are set by IM[3], IM[2], IM[1], and IM[0] pins as shown below.

Table 16. Interface Type Selection

IM[3]	IM[2]	IM[1]	IM[0]	Interface	Description
0	0	0	0	80-series 8bit parallel I/F	8bit read display data and 8bit read parameter
0	0	0	1	80-series 16bit parallel I/F	16bit read display data and 8bit read parameter
0	0	1	0	80-series 9bit parallel I/F	9bit read display data and 8bit read parameter
0	0	1	1	80-series 18bit parallel I/F	18bit read display data and 8bit read parameter
0	1	0	1	3-wire 9bit serial I/F I	8bit command and 8 / 24 / 32bit parameter
0	1	1	0	4-wire 8bit serial I/F I	8bit command and 8 / 24 / 32bit parameter
1	0	0	0	68-series 8bit parallel I/F	8bit read display data and 8bit read parameter
1	0	0	1	68-series 16bit parallel I/F	16bit read display data and 8bit read parameter
1	0	1	0	68-series 9bit parallel I/F	9bit read display data and 8bit read parameter
1	0	1	1	68-series 18bit parallel I/F	18bit read display data and 8bit read parameter
1	1	0	1	3-wire 9bit serial I/F II	8bit command and 8 / 24 / 32bit parameter
1	1	1	0	4-wire 8bit serial I/F II	8bit command and 8 / 24 / 32bit parameter

3.1.2. PIN DESCRIPTION

MPU interface is changed according to the bus width used. The pin assignment is listed in the table below.

3.1.2.1. 3-Wire 9-bit serial interface I

Pin Name	Description
CSX	Chip select signal
DCX (SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of DCX (SCL) signal.
SDA	Serial input/output data
DB[17:0]	Display Data of RGB Interface

3.1.2.2. 4-Wire 8-bit serial interface I

Pin Name	Description
CSX	Chip select signal
DCX	Data is regard as a command when DCX is low. Data is regard as a parameter or a display data when DCX is high.
WRX (SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of WRX signal.
SDA	Serial input/output data
DB[17:0]	Display Data of RGB Interface

3.1.2.3. 3-Wire 9-bit serial interface II

Pin Name	Description
CSX	Chip select signal
DCX (SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of DCX (SCL) signal.
SDA	Serial input data
SDO	Serial output data
DB[17:0]	Display Data of RGB Interface

3.1.2.4. 4-Wire 8-bit serial interface II

Pin Name	Description
CSX	Chip select signal
DCX	Data is regard as a command when DCX is low. Data is regard as a parameter or a display data when DCX is high.
WRX (SCL)	Clock for serial interface During write mode, the data is latched on the rising edge of WRX signal.
SDI / SDA	Serial input data
SDO	Serial output data
DB[17:0]	Display Data of RGB Interface

3.1.2.5. 80-Series parallel interface

Pin Name	Description
CSX	Chip select signal
DCX	Data bus is regard as a command when DCX is low. Data bus is regard as a parameter or a display data when DCX is high.
RDX (E)	Clock for read operation. When RDX is low, the data bus held on output state.
WRX (RWX)	Clock for write operation. The data is latched on the rising edge of WRX.
DB[17:0]	Data bus **Interface** / **DB Pins** 8-bit Parallel Interface : DB17-DB8 : unused, DB7-DB0 : 8-bit data 16-bit Parallel Interface : DB17-DB16 : unused, DB15-DB0 : 16-bit data 9-bit Parallel Interface : DB17-DB9 : unused, DB8-DB0 : 9-bit data 18-bit Parallel Interface : DB17-DB0 : 18-bit data If not used, fix this pin to VSS.

3.1.2.6. 68-Series parallel interface

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>CSX</td><td>Chip select signal</td></tr>
<tr><td>DCX</td><td>Data bus is regard as a command when DCX is low.
Data bus is regard as a parameter or a display data when DCX is high.</td></tr>
<tr><td>RDX (E)</td><td>Clock for read / write operation</td></tr>
<tr><td>WRX (RWX)</td><td>Read / write selection signal (Read: High / Write: Low)</td></tr>
<tr><td>DB[17:0]</td><td>Data bus
<table>
<tr><th>Interface</th><th>DB Pins</th></tr>
<tr><td>8-bit Parallel Interface</td><td>DB17-DB8: unused, DB7-DB0 : 8-bit data</td></tr>
<tr><td>16-bit Parallel Interface</td><td>DB17-DB16: unused, DB15-DB0 : 16-bit data</td></tr>
<tr><td>9-bit Parallel Interface</td><td>DB17-DB9: unused, DB8-DB0 : 9-bit data</td></tr>
<tr><td>18-bit Parallel Interface</td><td>DB17-DB0: 18-bit data</td></tr>
</table>
If not used, fix this pin to VSS.</td></tr>
</table>

3.1.3. INPUT / OUTPUT PIN ASSIGNMENT

The block diagrams for MPU interface are illustrated below.

3.1.3.1. 3-Wire 9-bit serial interface I

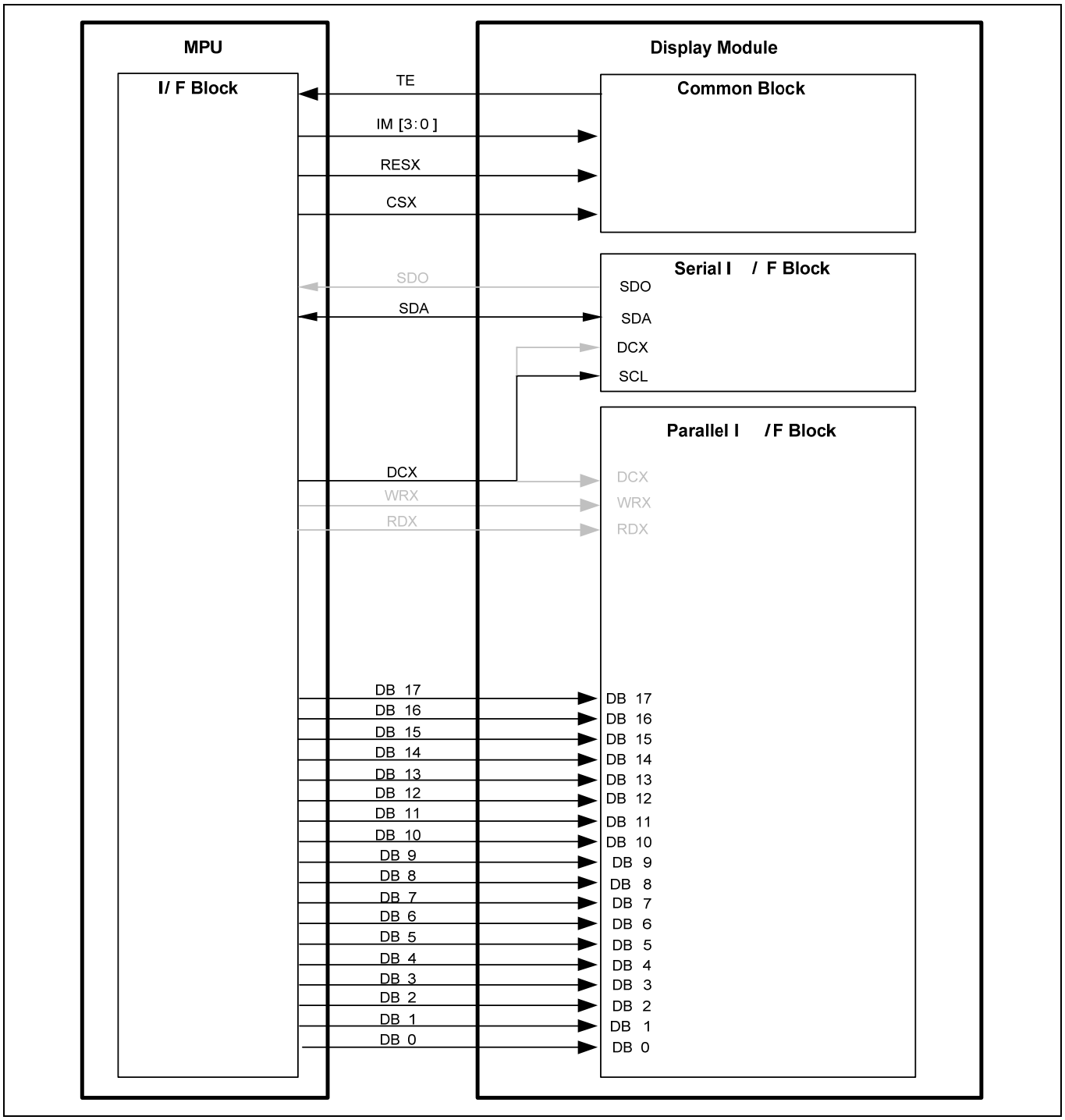


Figure17. 3-Wire 9-Bit Serial Interface I (RGB 18-Bit I/F)

3.1.3.2. 4-Wire 8-bit serial interface I

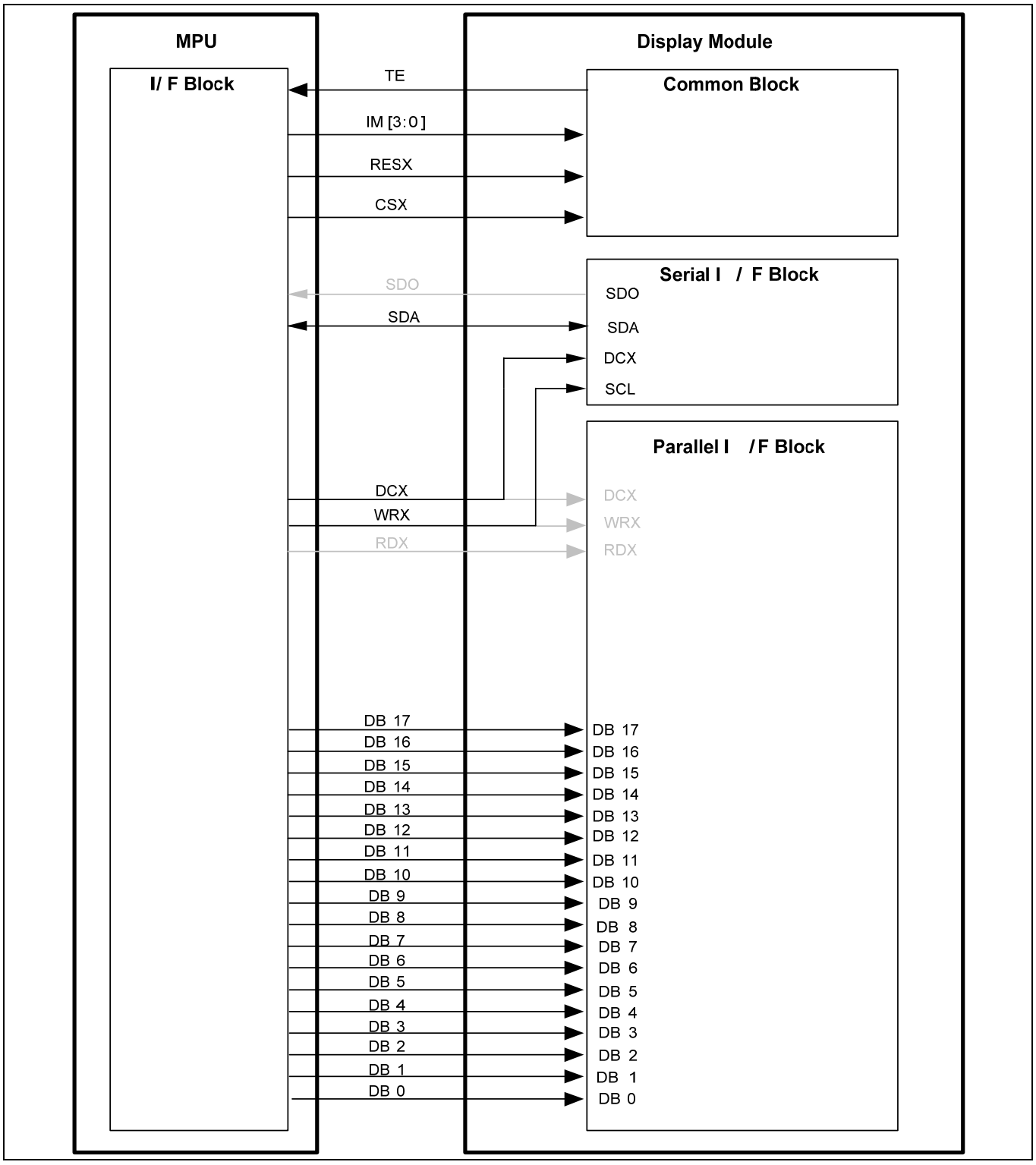


Figure18. 4-Wire 8-Bit Serial Interface I (RGB 18-Bit I/F)

3.1.3.3. 3-Wire 9-bit serial interface II

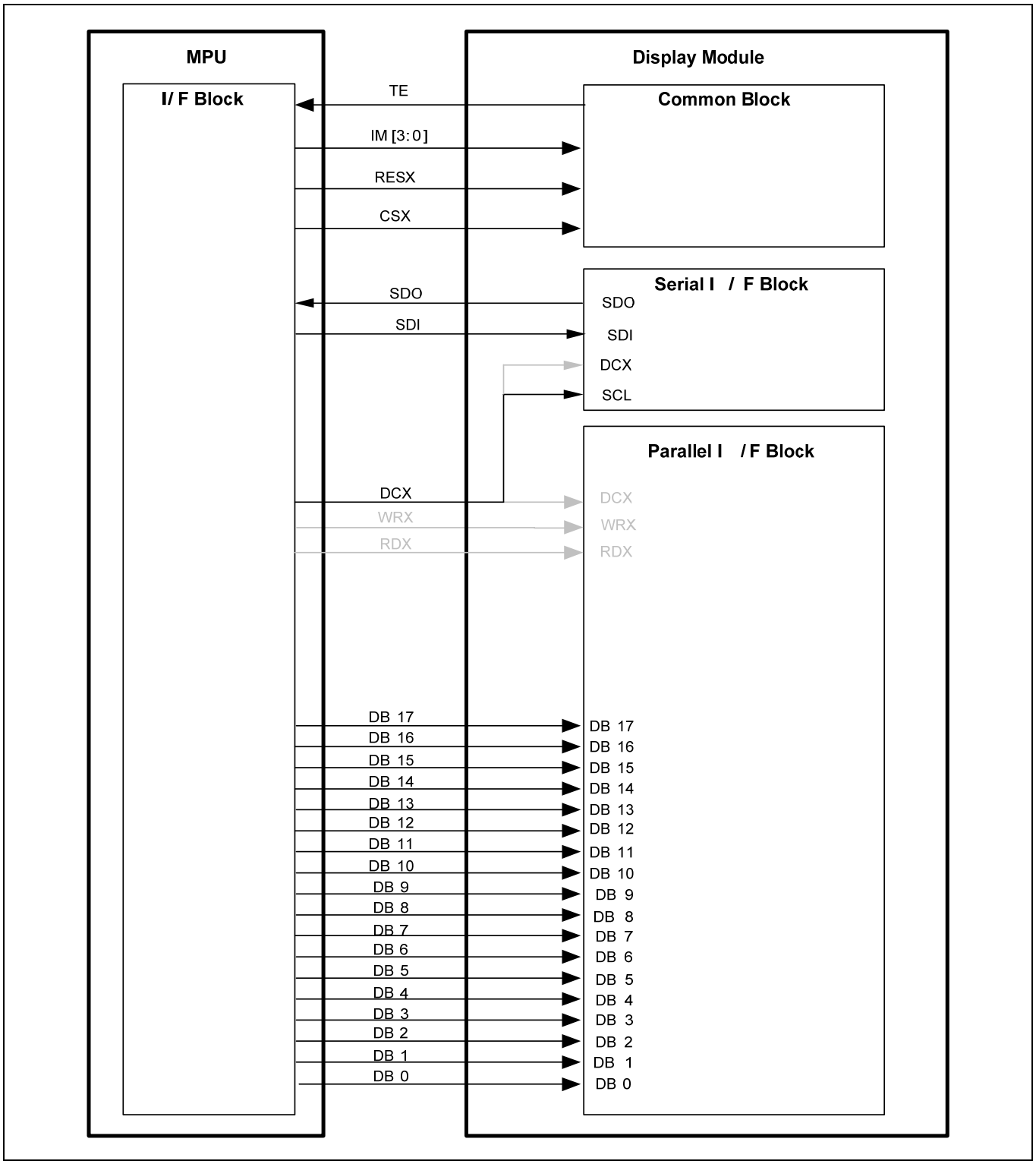


Figure19. 3-Wire 9-Bit Serial Interface II (RGB 18-Bit I/F)

3.1.3.4. 4-Wire 8-bit serial interface II

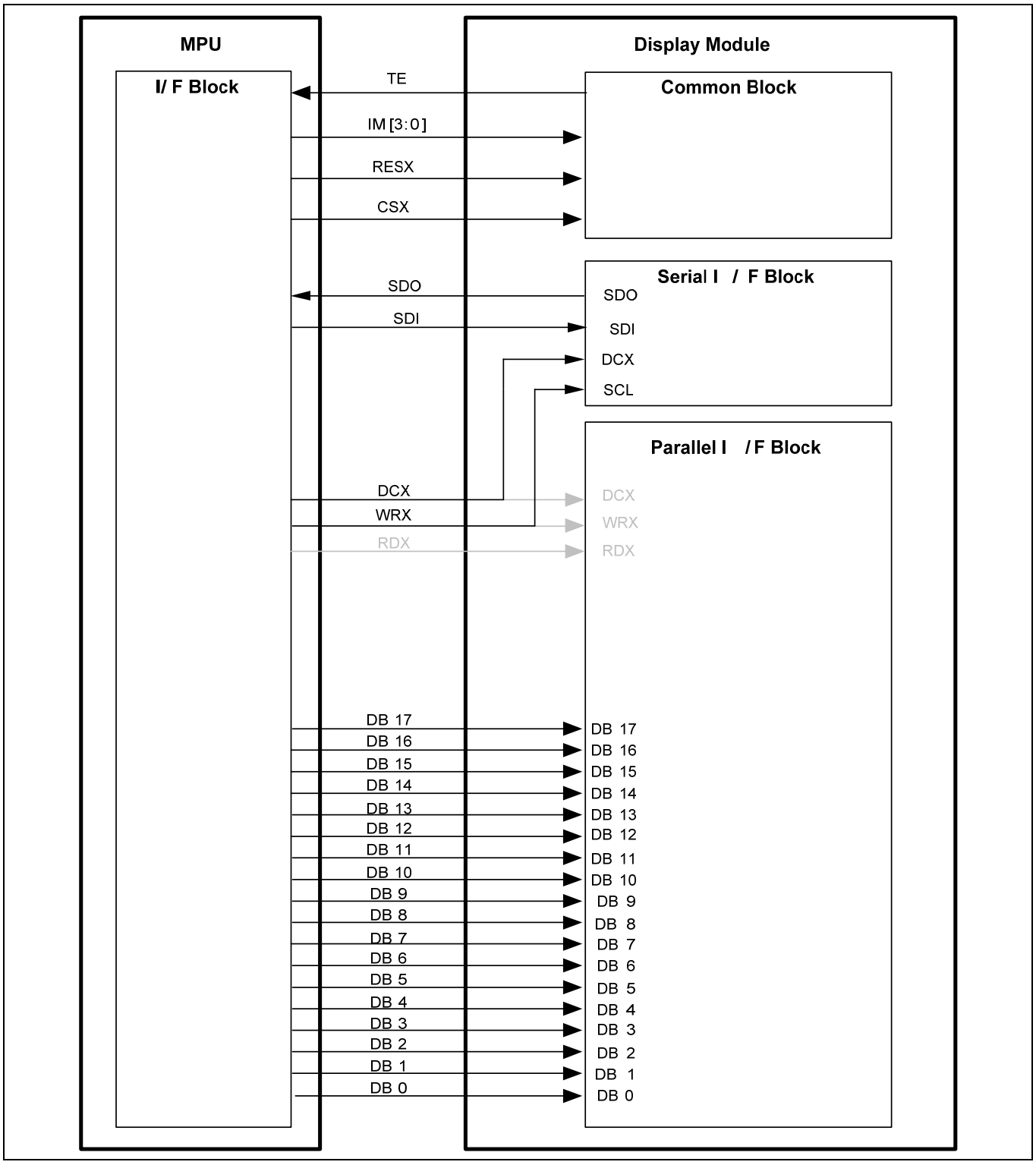


Figure20. 4-Wire 8-Bit Serial Interface II (RGB 18-Bit I/F)

3.1.3.5. 80-Series parallel interface

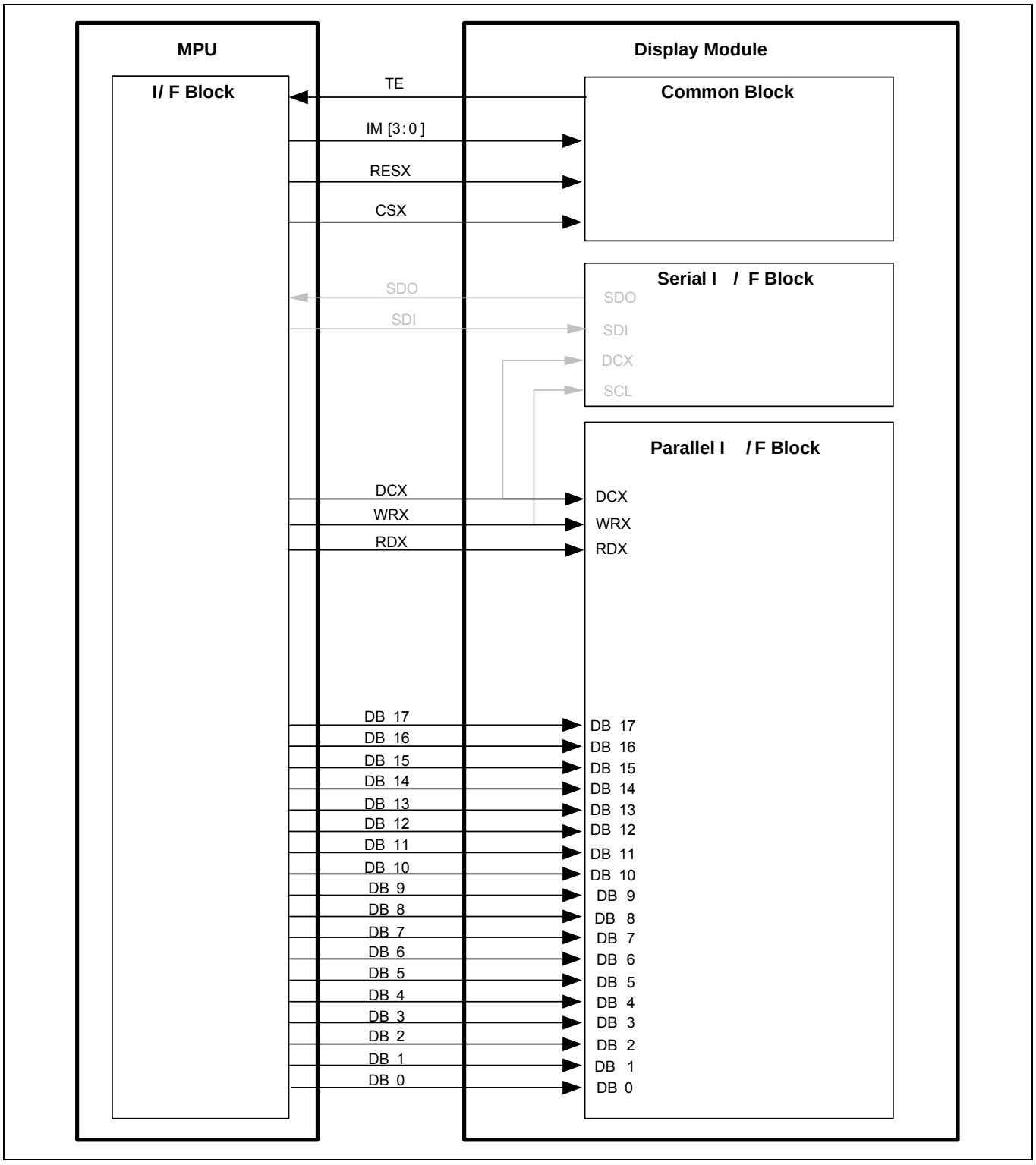


Figure21. 80-Series Parallel Interface

3.1.3.6. 68-Series parallel interface

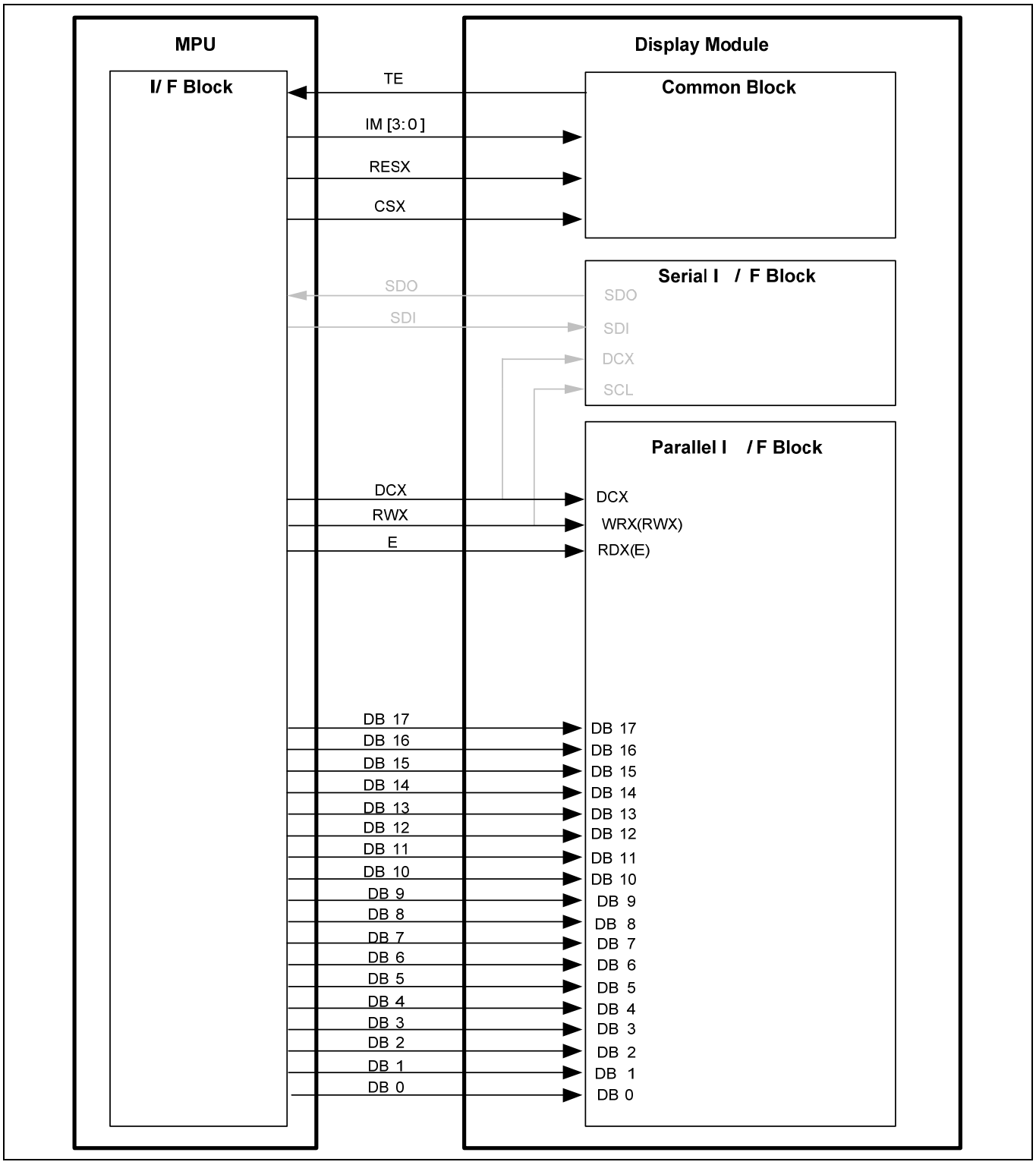


Figure22. 68-Series Parallel Interface

3.1.4. 3-WIRE 9-BIT SERIAL INTERFACE

This serial interface is 3-wire 9-bit bi-directional interface for communication between the micro controller and the LCD driver IC. CSX, SCL (DCX), SDA and SDO are used for interface with MPU only, so it can be stopped when no communication is necessary.

3.1.4.1. 3-Wire 9-bit data serial interface write mode

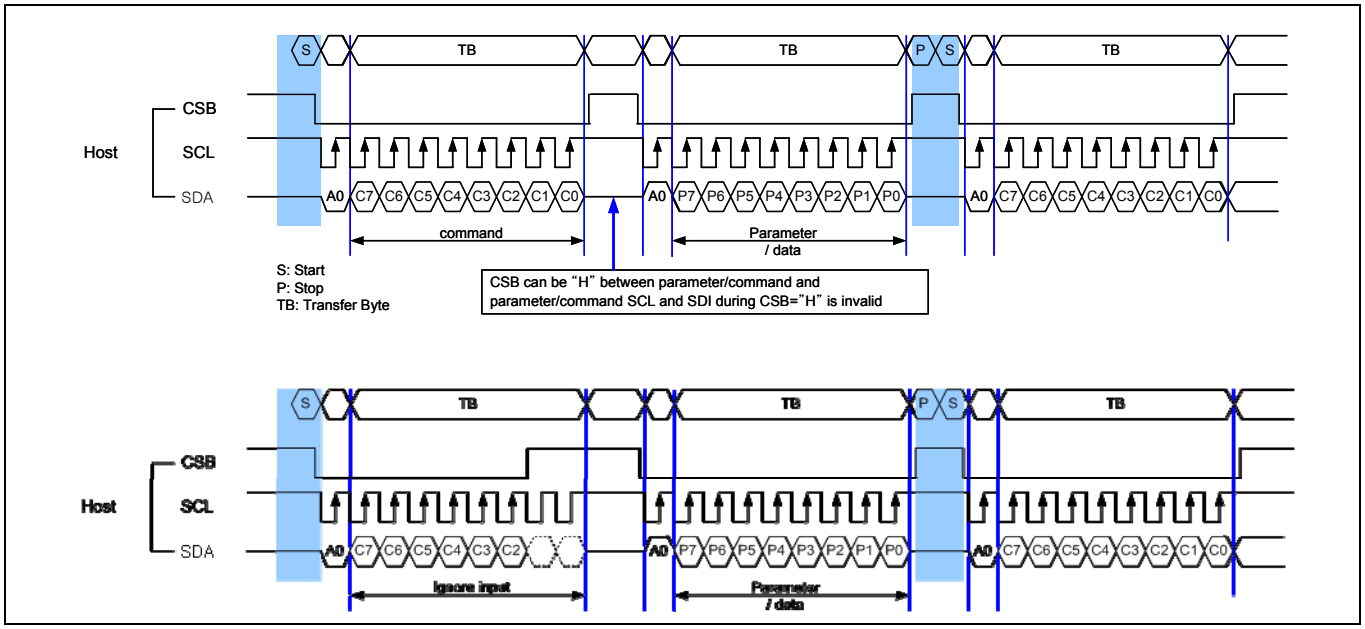


Figure23. 3-Wire 9-Bit Serial Interface I Bus Protocol, Write to Register or Display RAM

3.1.4.2. 3-Wire 9-bit data serial interface read 1-byte mode

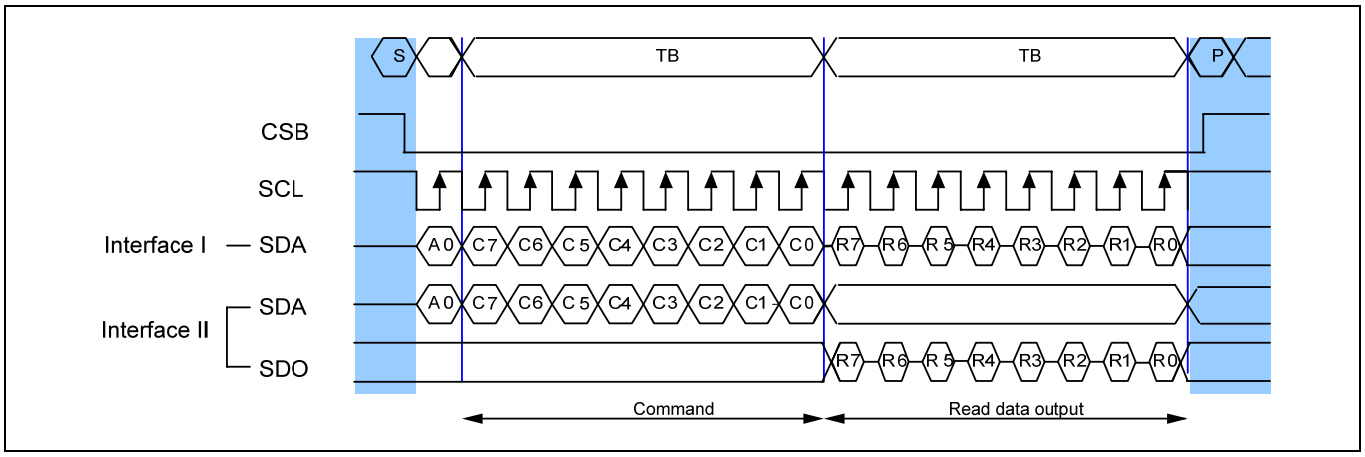


Figure24. 3-Wire 9-Bit Serial Interface I/II Bus Protocol, Read 1-Byte From Register

3.1.4.3. 3-Wire 9-bit data serial interface read multi-byte mode

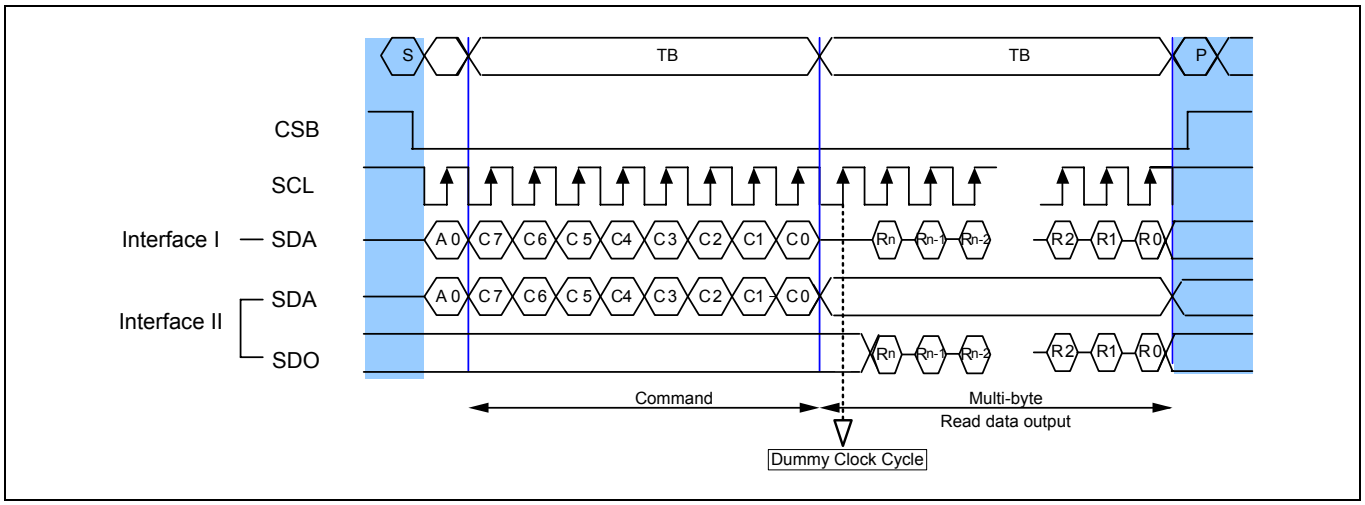


Figure25. 3-Wire 9-Bit Serial Interface I/II Bus Protocol, Read Multi-Byte From Register

3.1.5. 4-WIRE 8-BIT SERIAL INTERFACE

This serial interface is 4-wire 8-bit bi-directional interface for communication between the micro controller and the LCD driver IC. CSX, DCX, SCL, SDA and SDO are used for interface with MPU only, so it can be stopped when no communication is necessary.

3.1.5.1. 4-Wire 8-bit data serial interface write mode

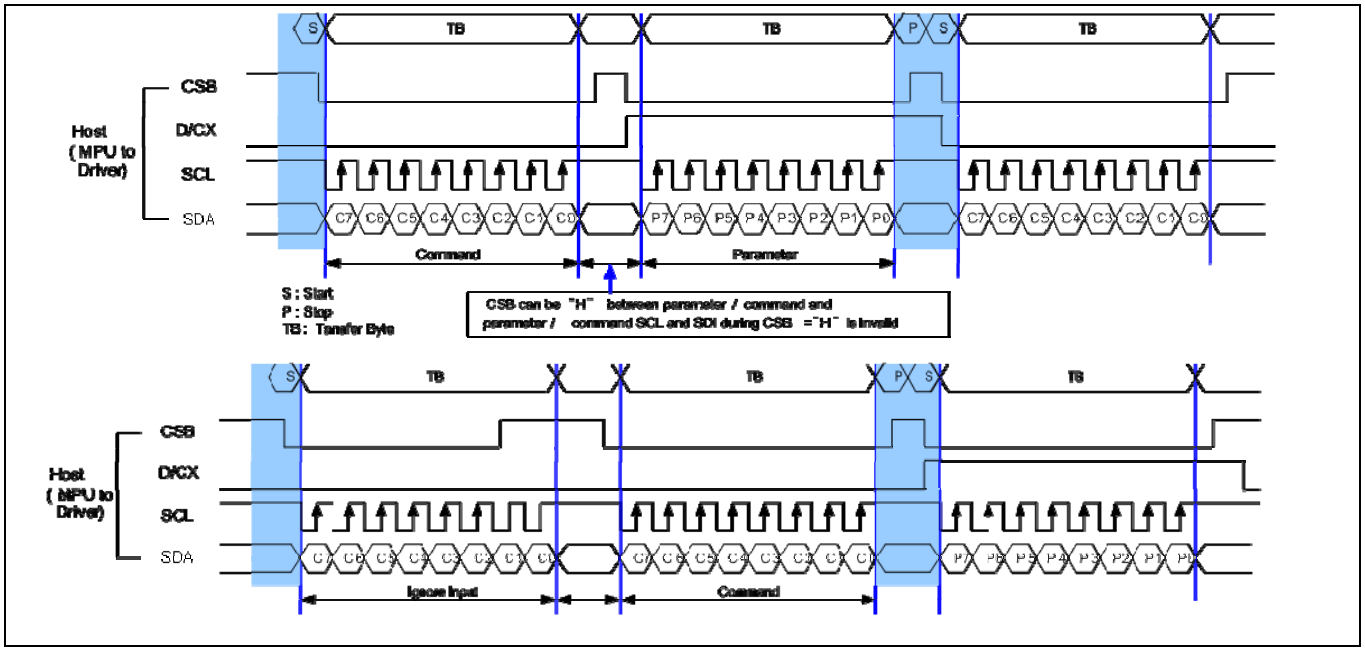


Figure26. 4-Wire 8-Bit Serial Interface I Bus Protocol, Write to Register or Display RAM

3.1.5.2. 4-Wire 8-bit data serial interface read 1-byte mode

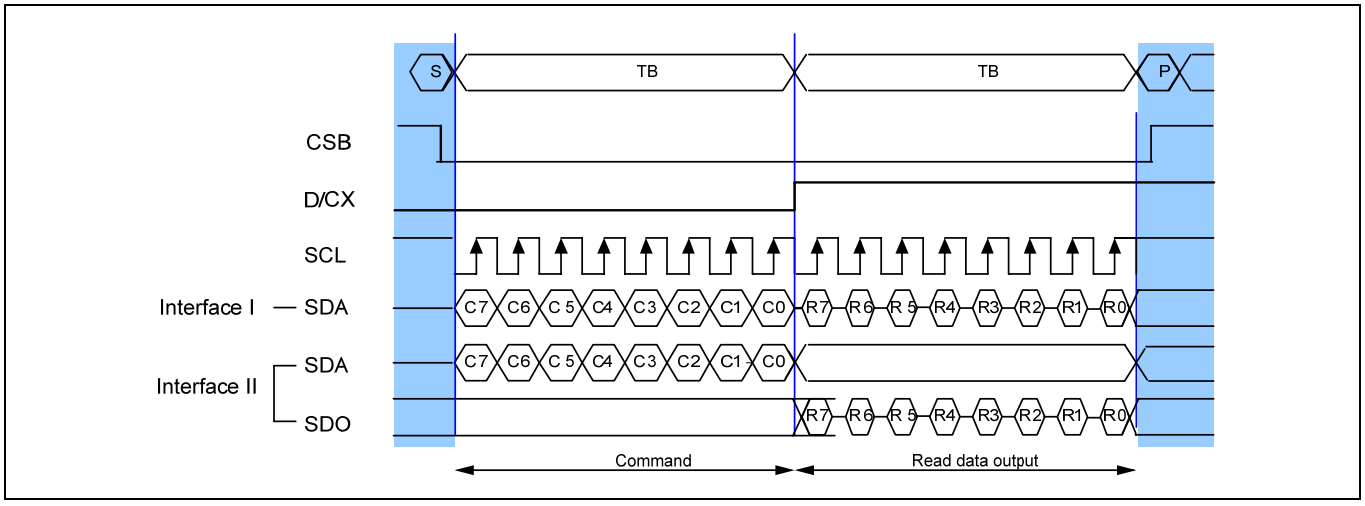


Figure27. 4-Wire 8-Bit Serial Interface I/II Bus Protocol, Read 1-Byte From Register

3.1.5.3. 4–Wire 8-bit data serial interface read multi-byte mode

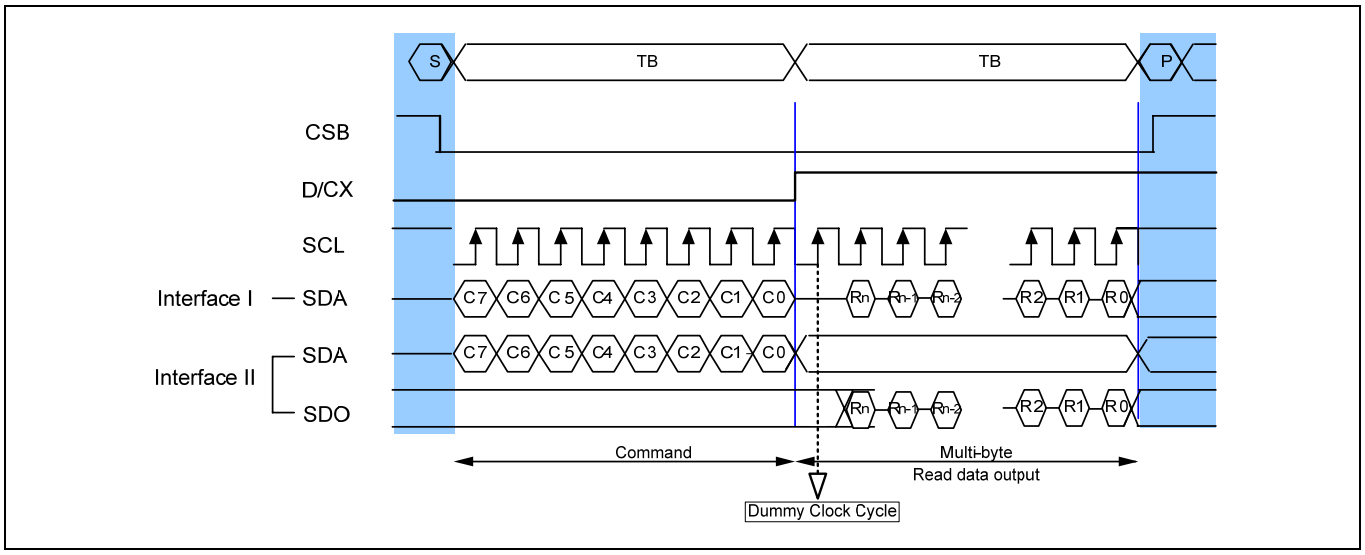


Figure28. 4-Wire 8-Bit Serial Interface I/II Bus Protocol, Read Multi-Byte From Register

3.1.6. 80-SERIES PARALLEL INTERFACE

3.1.6.1. 80-series MPU Parallel Interface Write Mode

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, WRX) and data signals (DB[17:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=’0’) and vice versa it is data (=’1’).

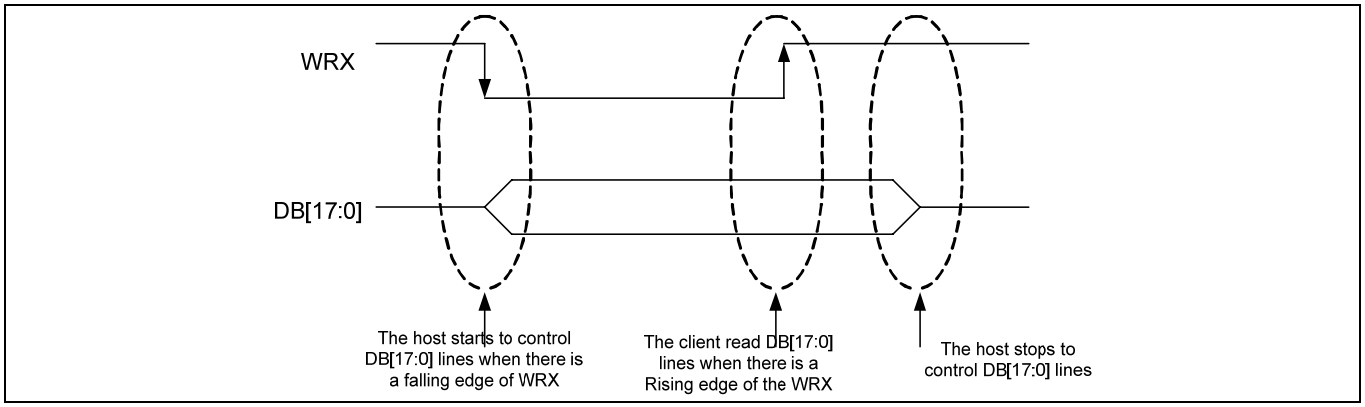


Figure29. 80-Series WRX Protocol

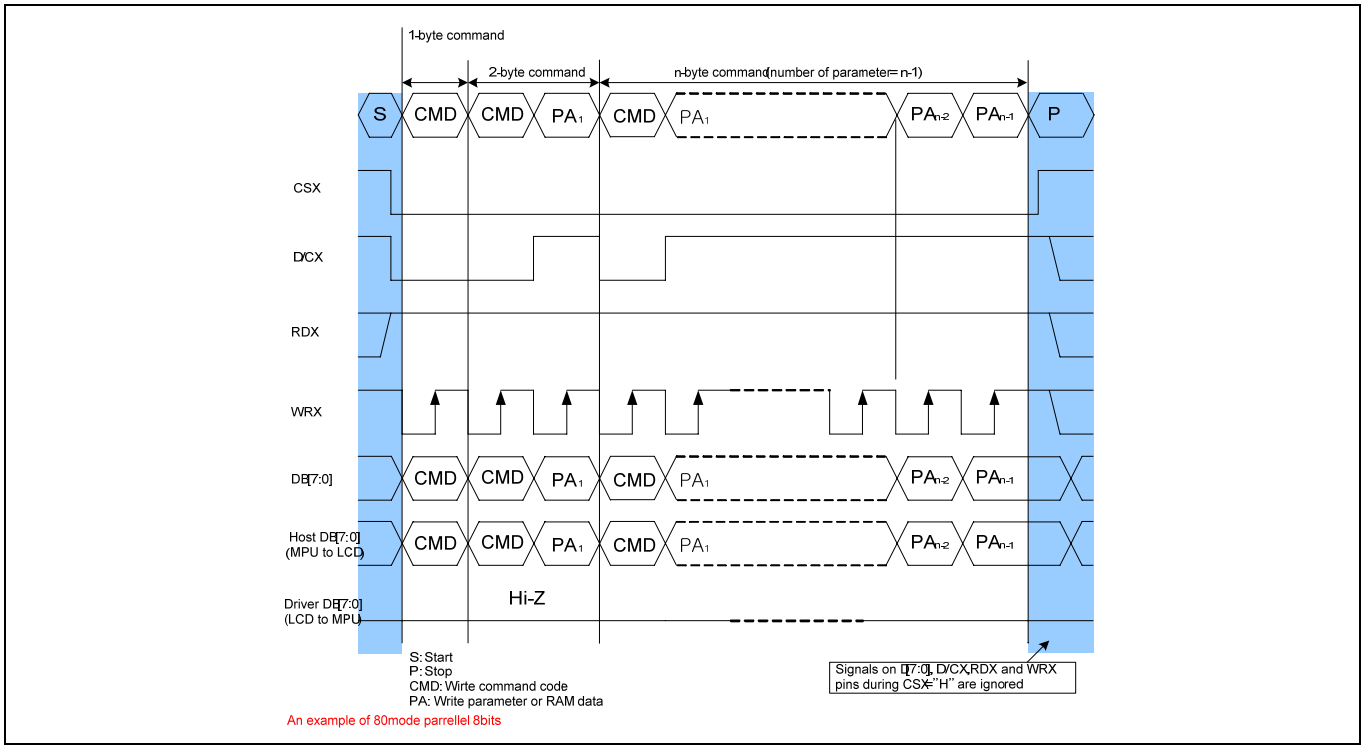


Figure30. 80-Series Parallel Bus Protocol, Write to Register or Display RAM

3.1.6.2. 80-Series mpu parallel interface read mode

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (DB[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

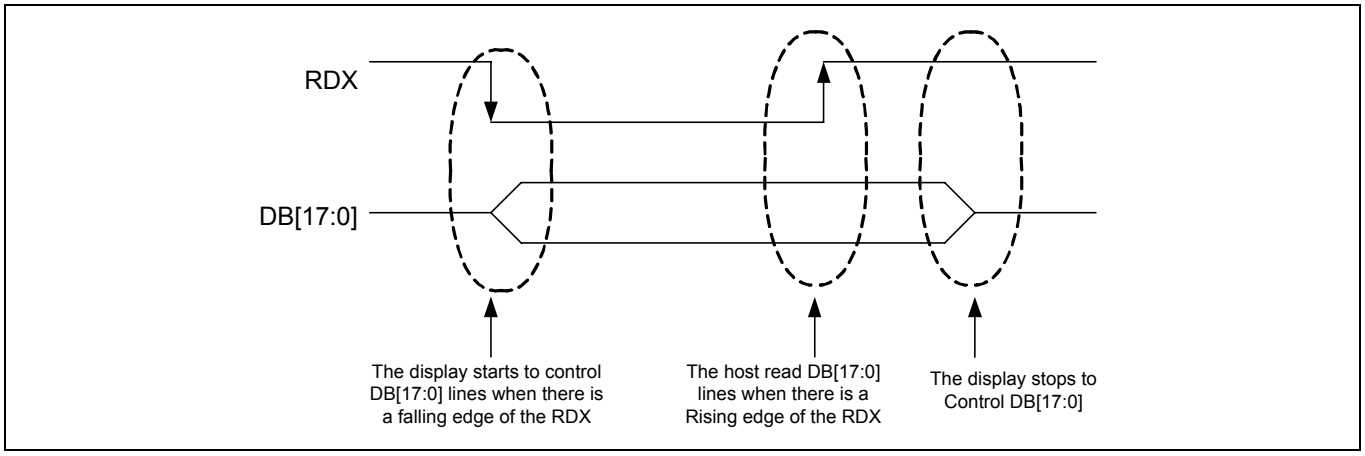


Figure31. 80-Series RDX Protocol

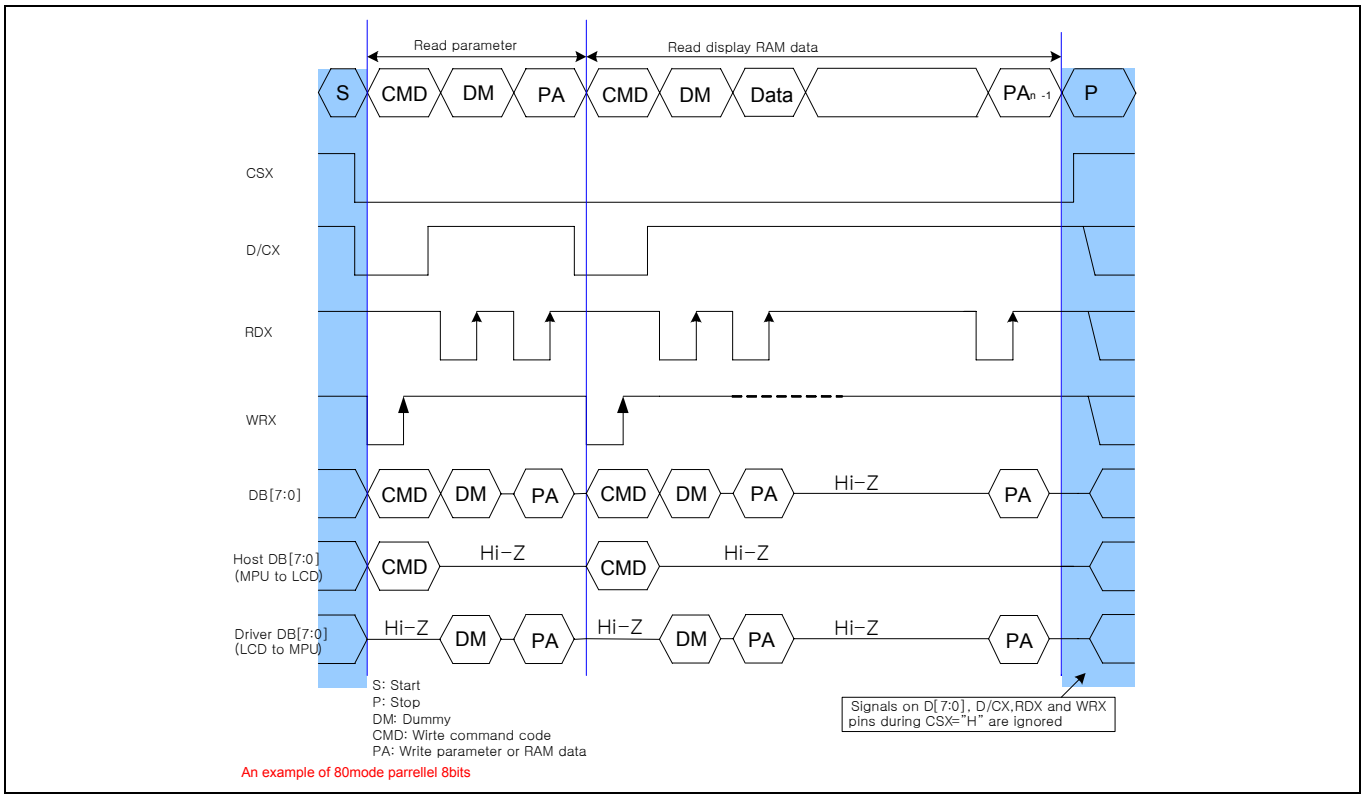


Figure32. 80-Series Parallel Bus Protocol, Read From Register

3.2. INTERFACE DESCRIPTION

The parallel interface of S6D04H0 can communicate with the MPU using max.18 bit bidirectional data bus (DB17 to DB0) to transfer command, parameter and display data. The serial interface uses SDI, SDO for transferring data.

3.2.1. BIDIRECTIONAL DATA BUS

The purpose of MPU interface in S6D04H0 is to communicate with the MPU in a direct connection. If the driver IC is not selected as CSX = Low, the data bus (data line) is placed in the high-impedance state to prevent the other driver ICs from adverse effects. When the driver IC is not selected, inputs through the MPU interface (DCX, RDX and WRX) have no effect.

Table 17. Description OF Data Bus for 80-Series

DCX	WRX	RDX	Description
L	↑	H	Command write Commands are input to DB7 to DB0.
H	↑	H	Parameter and display data write Parameters and display data are respectively input to DB7 to DB0 and DB17 to DB0.
L	H	↑	Parameter and display data read Parameters and display data are respectively output to DB7 to DB0 and DB17 to DB0.
L	H	↑	Dummy data is output

Table 18. Description of Data Bus for 68-Series

DCX	WRX (RWX)	RDX (E)	Description
L	L	↓	Command write Commands are input to DB7 to DB0.
H	L	↓	Parameter and display data write Parameters and display data are respectively input to DB7 to DB0 and DB17 to DB0.
L	H	↓	Parameter and display data read Parameters and display data are respectively output to DB7 to DB0 and DB17 to DB0.
L	H	↓	Dummy data is output

While using the parallel interface, the bus width which is used changes depending on the display data format. When a display data format which uses DB17 to DB8 is selected, it is necessary that DB17 to DB8 are set either HIGH or LOW as input on the MPU side although DB17 to DB8 are ignored when command and parameters are input.

3.2.2. DISPLAY MODULE DATA TRANSFER RECOVERY

If there is a break in data transmission while transferring a Command, Frame Memory or Multiple Parameter command data, before Bit D0 of the byte has been completed, then the Display Module will reject the previous bits and have reset the interface such that it will be ready to receive the same byte retransmitted when the chip select line (CSX) is next activated. See the following example;

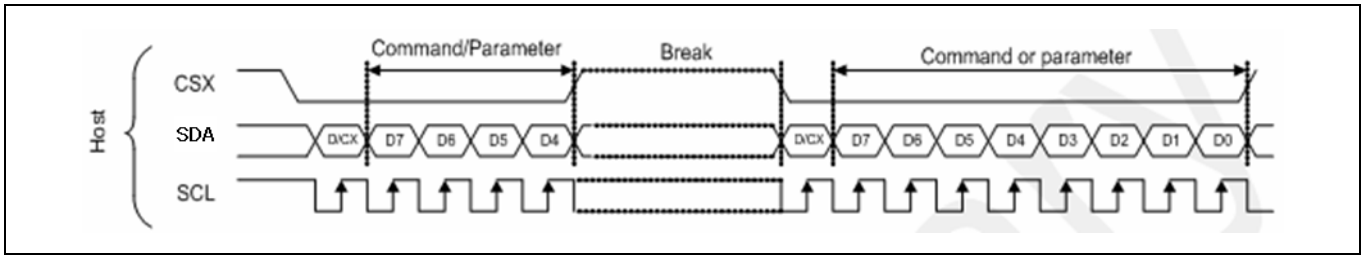


Figure33. Break During Data Transmission

If a 1 or more parameter command is being sent and a break occurs sending before the last parameter of the command and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown.

3.2.2.1. Break during middle of frame

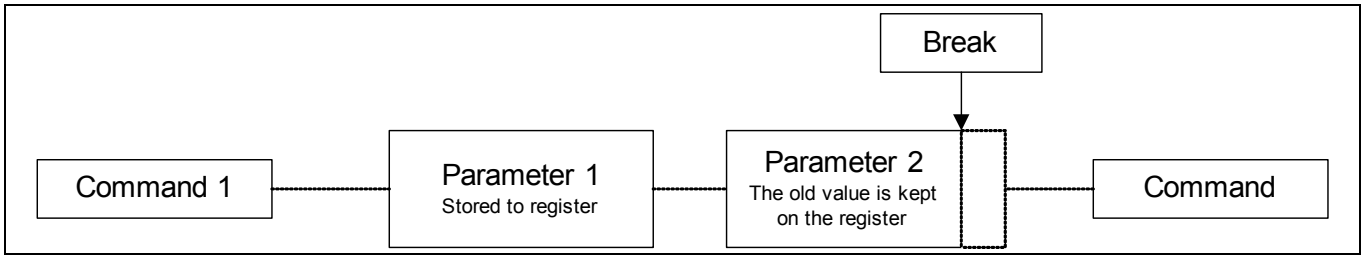


Figure34. Break During Middle of Frame

3.2.2.2. Break between frames

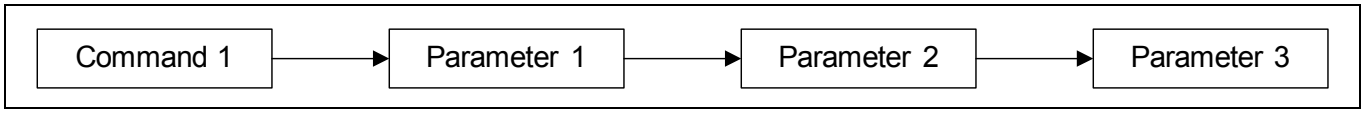


Figure35. Without Break

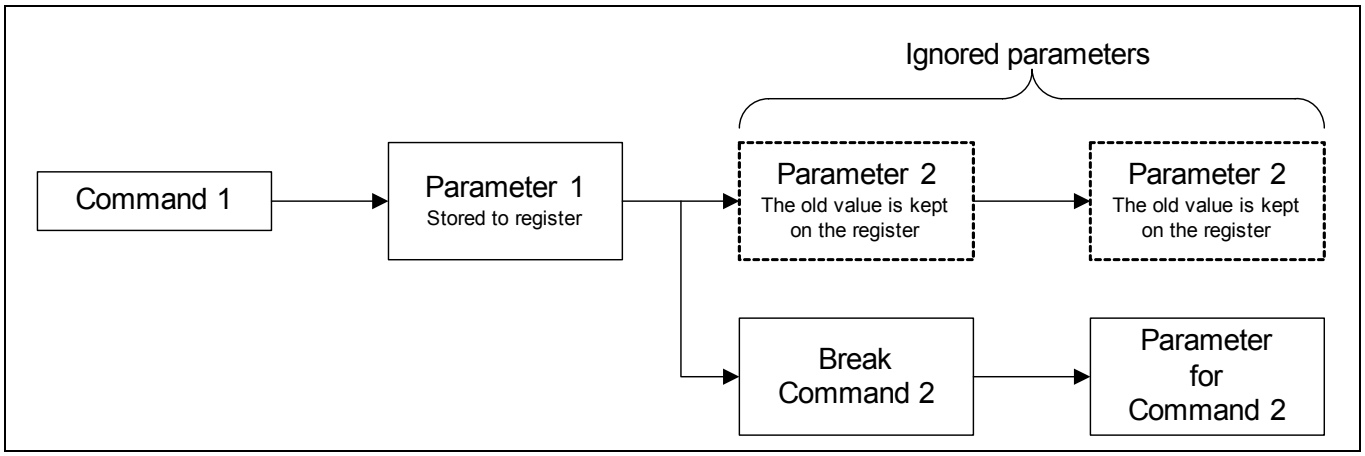


Figure36. With Break

Note.

Break can be e.g. another command or noise pulse.

3.2.3. DISPLAY MODULE DATA TRANSFER PAUSE

It will be possible when transferring a Command, Frame Memory Data or Multiple Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

3.2.3.1. Serial interface pause

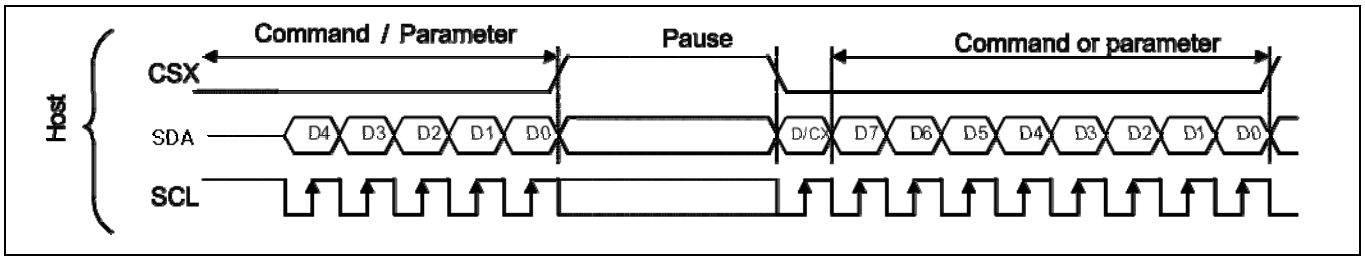


Figure37. Serial Interface Pause

This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

3.2.3.2. Parallel interface pause

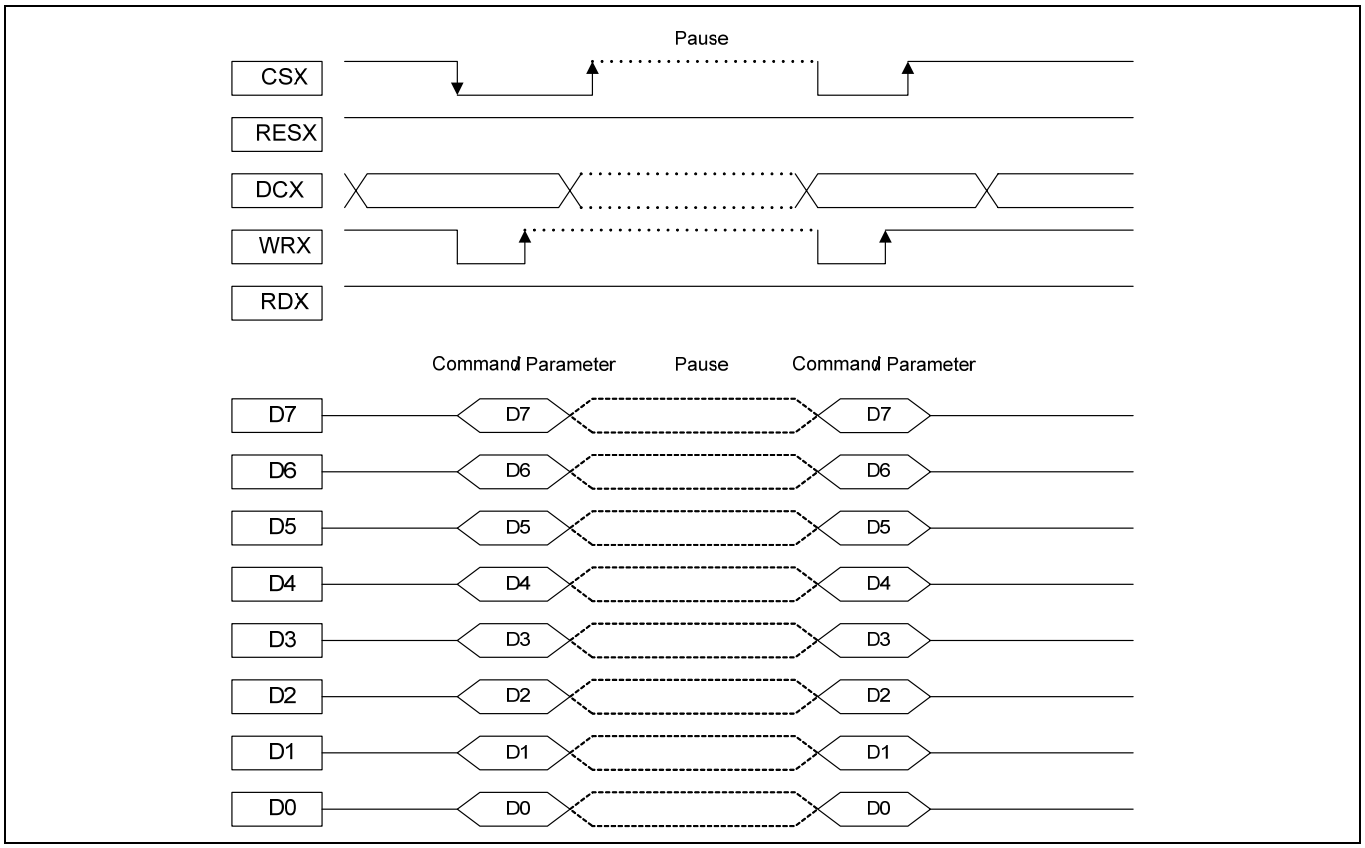


Figure38. Parallel Interface Pause

This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

3.2.4. DISPLAY MODULE DATA TRANSFER MODES

The module has various color modes for transferring data to the display data RAM. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

3.2.4.1. Method I

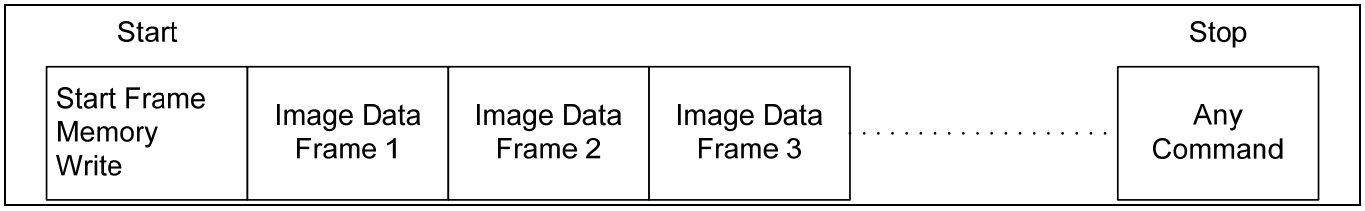


Figure39. Method I of Data Transfer Mode

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start pint and the next Frame is written.

3.2.4.2. Method II

The Image data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame downloaded.

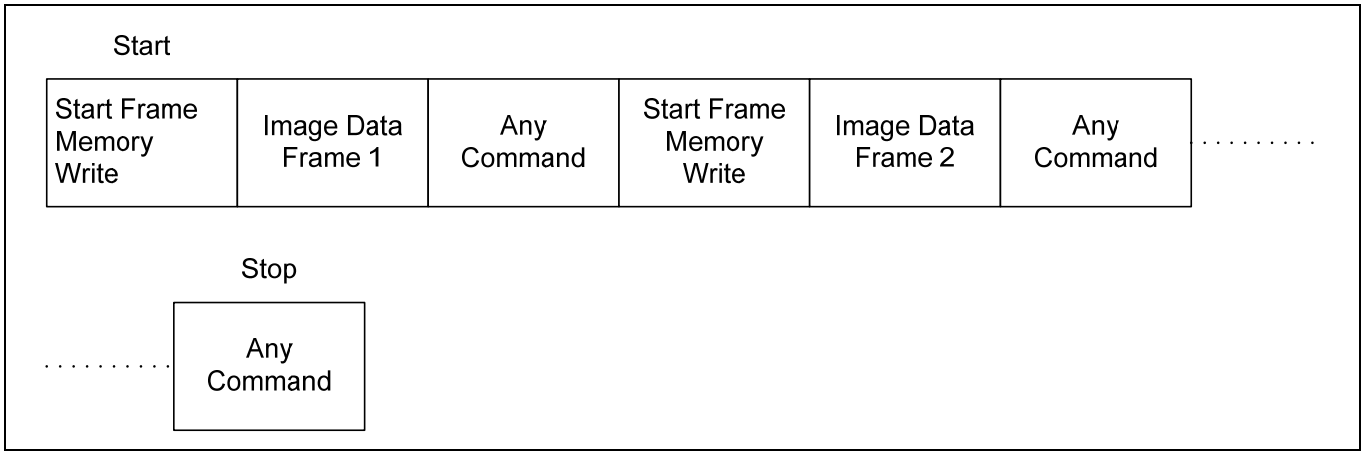


Figure40. Method 2 of Data Transfer Mode

Note.

1. These apply to all data transfer color modes on both Serial and Parallel interfaces.
2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored to the Frame Memory.

3.3. DISPLAY DATA FORMAT

Various data formats are available in which display data can be written to the display data RAM. It is possible to choose a format suitable for the purpose of use. The data format is determined by a combination of COLMOD and MDT commands.

3.3.1. DISPLAY DATA FORMAT FOR WRITE

Table 19. Display Data Format for Write

Color Mode	Interface(IM[2:0])				
	18Bit	9Bit	16Bit	8Bit	
	011	010	001	000	
262k Color (COLMOD[2:0] = 110)	18bit 666 1/1 (MDT=00)	9bit 666 1/2 (MDT=00)	16bit 666 2/3 (MDT=00)	6bit 666 1/3 (MDT=00)	Expand by IPM Note1
		6bit 666 1/3 (MDT=01)	12bit 666 1/2 (MDT=01) 16bit 666 1/2 (MDT=10) 16bit 666 1/2 (MDT=11)		
65k Color (COLMOD[2:0] = 101)	16bit 565 1/1 (MDT=00)	8bit 565 1/2 (MDT=00)	16bit 565 1/1 (MDT=00)	8bit 565 1/2 (MDT=00)	Expand by IPM Note1

Note.

1. Display data expand (565 → 666) method is decided by IPM command. In default condition (IPM = “00”), MSB data are copied to LSB data for expanding. See Figure. 41 and Figure. 42.
2. Registers set related to data format (IPM, MDT) are on the F7H command (Level 2)

Table 20. MDT Description

MDT[1:0](Value)	Description
00	1pixel by 1cycle format
01	2pixel by 3cycle format
10	1pixel by 2cycle format
11	1pixel by 3cycle format

In 65k color mode (16-bit data) data bit should be expanded to 18-bit like below. It will be used “IPM=00”

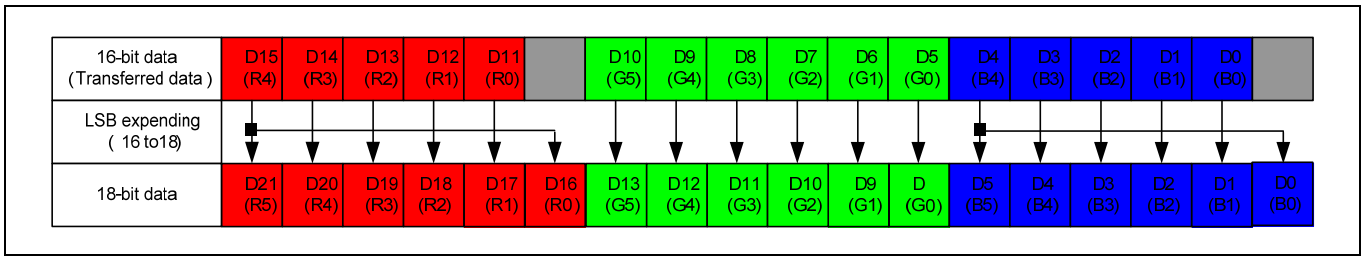


Figure41. Data Expand Method(65K Color Mode)

3.3.2. DISPLAY MODULE DATA COLOR CODING(262K COLOR MODE)

For the display data to be accessed in 262k color mode, it is necessary that 262k color mode be selected (B2 to B0: 110) using COLMOD command before writing or reading to or from the display data RAM. In this mode, the display data per pixel comprised of 6 bits for R, 6 bits for G and 6 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MPU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed, and the display data is read out to the MPU bus according to the format selected.

3.3.2.1. 8Bit parallel interface for 666 1/3 formats

Table 21. 8Bit Parallel Interface for 666 1/3 Formats

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

3.3.2.2. 16Bit parallel interface for 666 2/3 formats(MDT=00)

Table 22. 16Bit Parallel Interface for 666 2/3 Formats(MDT="00")

Count	0	1	2	3	…	358	359	360
DCX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9					…			
D8					…			
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5

Count	0	1	2	3	…	358	359	360
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1				…			
D0	C0				…			

3.3.2.3. 16Bit parallel interface for 666 1/2 formats(MDT = “01”)

Table 23. 16Bit Parallel Interface For 666 1/2 Formats(MDT = “01”)

Count	0	1	2	3	4	…	479	480
DCX	0	1	1	1	1	…	1	1
D15		0R5	0B5	1R5	1B5	…	239R5	239B5
D14		0R4	0B4	1R4	1B4	…	239R4	239B4
D13		0R3	0B3	1R3	1B3	…	239R3	239B3
D12		0R2	0B2	1R2	1B2	…	239R2	239B2
D11		0R1	0B1	1R1	1B1	…	239R1	239B1
D10		0R0	0B0	1R0	1B0	…	239R0	239B0
D9						…		
D8						…		
D7	C7	0G5		1G5		…	239G5	
D6	C6	0G4		1G4		…	239G4	
D5	C5	0G3		1G3		…	239G3	
D4	C4	0G2		1G2		…	239G2	
D3	C3	0G1		1G1		…	239G1	
D2	C2	0G0		1G0		…	239G0	
D1	C1					…		
D0	C0					…		

3.3.2.4. 16Bit parallel interface for 666 1/2 formats(MDT = “10”)

Table 24. 16Bit Parallel Interface for 666 1/2 Formats(MDT = “10”)

Count	0	1	2	3	4	…	479	480
DCX	0	1	1	1	1	…	1	1
D15		0R5	0B1	1R5	1B1	…	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	239R4	239B0
D13		0R3		1R3		…	239R3	
D12		0R2		1R2		…	239R2	
D11		0R1		1R1		…	239R1	
D10		0R0		1R0		…	239R0	
D9		0G5		1G5		…	239G5	
D8		0G4		1G4		…	239G4	
D7	C7	0G3		1G3		…	239G3	
D6	C6	0G2		1G2		…	239G2	
D5	C5	0G1		1G1		…	239G1	
D4	C4	0G0		1G0		…	239G0	
D3	C3	0B5		1B5		…	239B5	
D2	C2	0B4		1B4		…	239B4	
D1	C1	0B3		1B3		…	239B3	
D0	C0	0B2		1B2		…	239B2	

3.3.2.5. 16Bit parallel interface for 666 1/2 formats(MDT = “11”)

Table 25. 16Bit Parallel Interface for 666 1/2 Formats(MDT = “11”)

Count	0	1	2	3	4	…	479	480
DCX	0	1	1	1	1	…	1	1
D15			0R3		1R3	…		239R3
D14			0R2		1R2	…		239R2
D13			0R1		1R1	…		239R1
D12			0R0		1R0	…		239R0
D11			0G5		1G5	…		239G5
D10			0G4		1G4	…		239G4
D9			0G3		1G3	…		239G3
D8			0G2		1G2	…		239G2

Count	0	1	2	3	4	…	479	480
D7	C7		0G1		1G1	…		239G1
D6	C6		0G0		1G0	…		239G0
D5	C5		0B5		1B5	…		239B5
D4	C4		0B4		1B4	…		239B4
D3	C3		0B3		1B3	…		239B3
D2	C2		0B2		1B2	…		239B2
D1	C1	0R5	0B1	1R5	1B1	…	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	239R4	239B0

3.3.2.6. 9Bit parallel interface for 666 1/2 formats

Table 26. 9Bit Parallel Interface for 666 1/2 Formats(MDT = 00)

Count	0	1	2	3	…	478	479	480
DCX	0	1	1	1	…	1	1	1
D8		0R5	0G2	1R5	…	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	…	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	…	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	…	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	…	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	…	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	…	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	…	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	…	238B0	239G3	239B0

Table 27. 9-Bit Parallel Interface for 666 1/3 Formats(MDT = 01)

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D8					…			
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G5	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G4	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0

Count	0	1	2	3	…	718	719	720
D1	C1				…			
D0	C0				…			

3.3.2.7. 18Bit parallel interface for 666 1/1 formats

Table 28. 18Bit Parallel Interface for 666 1/1 Formats

Count	0	1	2	…	239	240
DCX	0	1	1	…	1	1
D17		0R5	1R5	…	238R5	239R5
D16		0R4	1R4	…	238R4	239R4
D15		0R3	1R3	…	238R3	239R3
D14		0R2	1R2	…	238R2	239R2
D13		0R1	1R1	…	238R1	239R1
D12		0R0	1R0	…	238R0	239R0
D11		0G5	1G5	…	238G5	239G5
D10		0G4	1G4	…	238G4	239G4
D9		0G3	1G3	…	238G3	239G3
D8		0G2	1G2	…	238G2	239G2
D7	C7	0G1	1G1	…	238G1	239G1
D6	C6	0G0	1G0	…	238G0	239G0
D5	C5	0B5	1B5	…	238B5	239B5
D4	C4	0B4	1B4		238B4	239B4
D3	C3	0B3	1B3		238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

3.3.2.8. 4-Wire 8-bit serial interface for 666 1/3 formats

Table 29. 4-Wire 8-Bit Serial Interface for 666 1/3 Formats

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3

Count	0	1	2	3	…	718	719	720
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

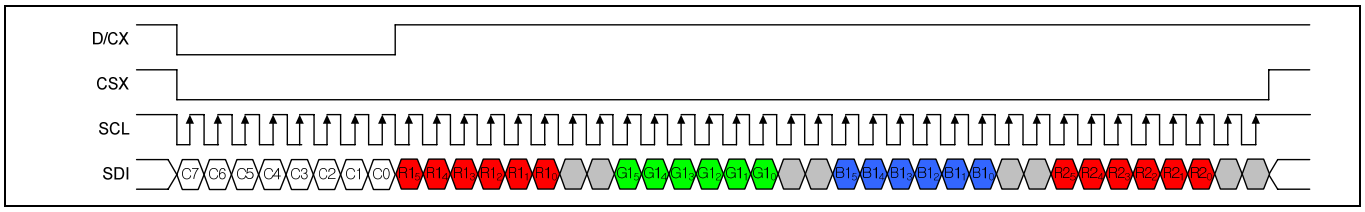


Figure42. 4-Wire 8-Bit Serial Interface for 666 1/3 Formats

3.3.2.9. 3-Wire 9-bit serial interface for 666 1/3 formats

Table 30. 3-Wire 9-Bit Serial Interface for 666 1/3 Formats

Count	0	1	2	3	…	718	719	720
DCX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

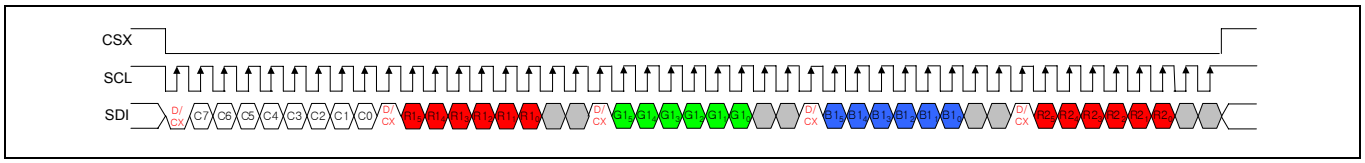


Figure43. 3-Wire 9-Bit Serial Interface for 666 1/3 Formats

3.3.3. DISPLAY MODULE DATA COLOR CODING (65K COLOR MODE)

For the display data to be accessed in 65k color mode, it is necessary that 65k color mode be selected (B2 to B0: 101) using COLMOD command before writing or reading to or from the display data RAM. In this mode, the display data per pixel comprised of 5 bits for R, 6 bits for G and 5 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MPU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed, and the display data is read out to the MPU bus according to the format selected.

3.3.3.1. 8Bit parallel interface for 565 1/2 formats

Table 31. 8Bit Parallel Interface for 565 1/2 Formats

Count	0	1	2	3	4	…	359	480
DCX	0	1	1	1	1	…	1	1
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G3	239B0

3.3.3.2. 16Bit parallel interface for 565 1/1 formats

Table 32. 16Bit Parallel Interface for 565 1/1 Formats

Count	0	1	2	…	239	240
DCX	0	1	1	…	1	1
D15		0R4	1R4	…	238R4	239R4
D14		0R3	1R3	…	238R3	239R3
D13		0R2	1R2	…	238R2	239R2
D12		0R1	1R1	…	238R1	239R1
D11		0R0	1R0	…	238R0	239R0
D10		0G5	1G5	…	238G5	239G5
D9		0G4	1G4	…	238G4	239G4
D8		0G3	1G3	…	238G3	239G3
D7	C7	0G2	1G2	…	238G2	239G2

Count	0	1	2	…	239	240
D6	C6	0G1	1G1	…	238G1	239G1
D5	C5	0G0	1G0	…	238G0	239G0
D4	C4	0B4	1B4	…	238B4	239B4
D3	C3	0B3	1B3	…	238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

3.3.3.3. 9Bit parallel interface for 565 1/2 formats

Table 33. 9Bit Parallel Interface for 565 1/2 Formats

Count	0	1	2	3	4	…	359	480
DCX	0	1	1	1	1	…	1	1
D8						…		
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G3	239B0

3.3.3.4. 18Bit parallel interface for 565 1/1 formats

Table 34. 18Bit Parallel Interface for 565 1/1 Formats

Count	0	1	2	…	239	240
DCX	0	1	1	…	1	1
D17						
D16						
D15		0R4	1R4	…	238R4	239R4
D14		0R3	1R3	…	238R3	239R3
D13		0R2	1R2	…	238R2	239R2
D12		0R1	1R1	…	238R1	239R1
D11		0R0	1R0	…	238R0	239R0

Count	0	1	2	…	239	240
D10		0G5	1G5	…	238G5	239G5
D9		0G4	1G4	…	238G4	239G4
D8		0G3	1G3	…	238G3	239G3
D7	C7	0G2	1G2	…	238G2	239G2
D6	C6	0G1	1G1	…	238G1	239G1
D5	C5	0G0	1G0	…	238G0	239G0
D4	C4	0B4	1B4	…	238B4	239B4
D3	C3	0B3	1B3	…	238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

3.3.3.5. 4-Wire 8-bit serial interface for 565 1/2 formats

Table 35. 4-Wire 8-Bit Serial Interface for 565 1/2 Formats

Count	0	1	2	3	4	…	359	480
DCX	0	1	1	1	1	…	1	1
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G3	239B0

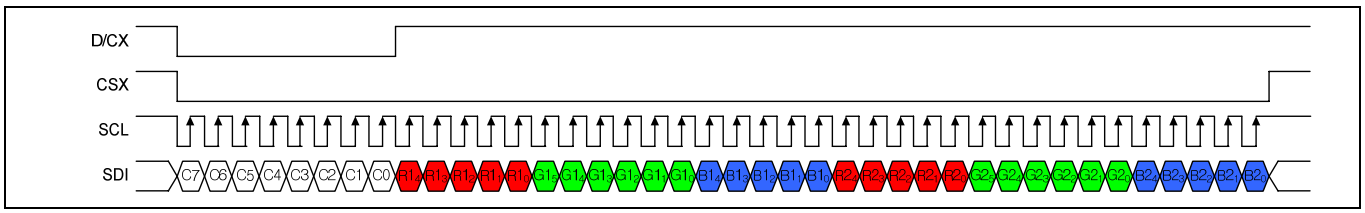


Figure44. 4-Wire 8-Bit Serial Interface for 565 1/2 Formats

3.3.3.6. 3-Wire 9-bit serial interface for 565 1/2 formats

Table 36. 3-Wire 9-Bit Serial Interface for 565 1/2 Formats

Count	0	1	2	3	4	…	359	480
DCX	0	1	1	1	1	…	1	1
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G3	239B0

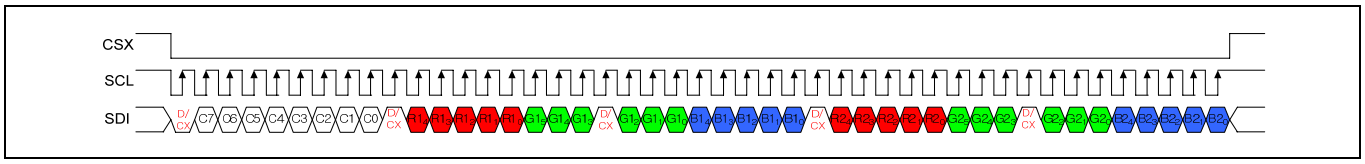


Figure45. 3-Wire 9-Bit Serial Interface for 565 1/2 Formats

3.4. RGB INTERFACE

3.4.1. DEFINITION

The module uses 6 or 18-bit parallel RGB interface which includes: VSYNC, HSYNC, ENABLE, DOTCLK, DB[17:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

Pixel clock (DOTCLK) is running all the time without stopping and it is used to entering VSYNC, HSYNC, ENABLE and DB[17:0] states when there is a rising edge of the DOTCLK. The DOTCLK can not be used as continues internal clock for other functions of the display module e.g. Sleep in mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of he DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is negative (‘0’, low) active and its state is read to the display module by a rising edge of the DOTCLK signal.

Data Enable (ENABLE) is used to tell when there is received a RGB information that should be transferred on the display. This is a positive (‘1’, high) active and its state is read to the display module by a rising edge of the DOTCLK signal.

DB[17:0] are used to tell what is the information of the image that is transferred on the display (When ENABLE= ’1’ and there is a rising edge of DOTCLK). DB[17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal.

The DOTCLK cycle is described in the following figure.

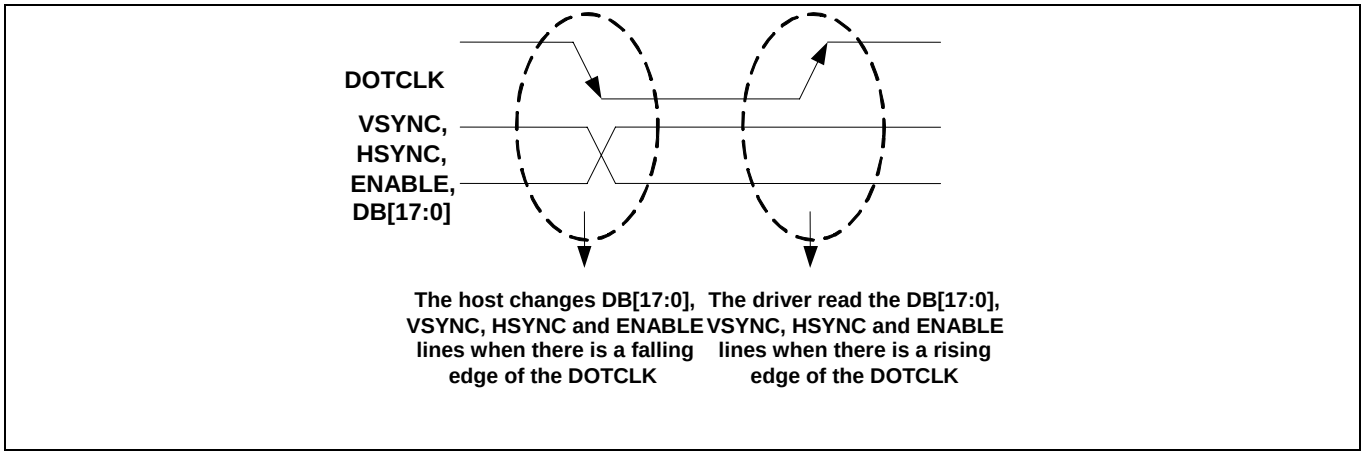


Figure46. DOTCLK Timing

Note.

DPL=0 of IFCTL (F7h) command.

3.4.2. MOTION PICTURE DISPLAY

S6D04H0 incorporates RGB interface to display motion pictures and GRAM to store data for display.
The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK.

In the period between the completion of displaying one frame data and the next VSYNC signal, the display status will remain in front porch period.

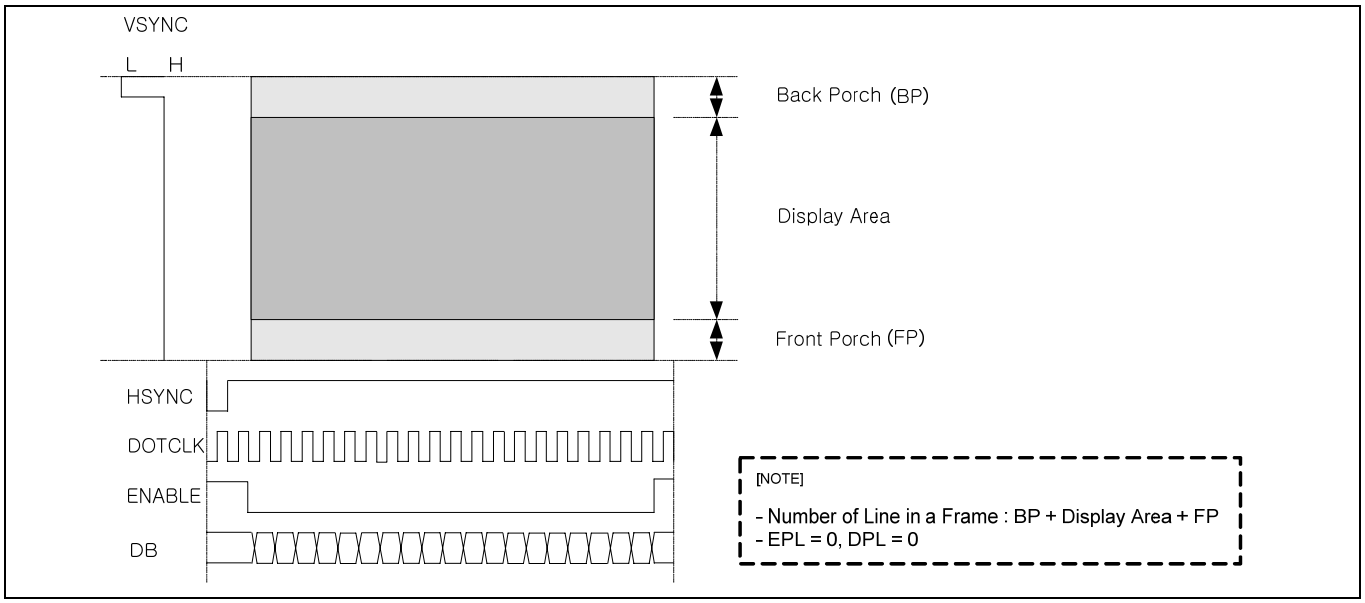


Figure47. RGB Interface

Note.

For RGB interface, VSYNC, HSYNC, DOTCLK should be supplied at much higher resolution than that of panel.

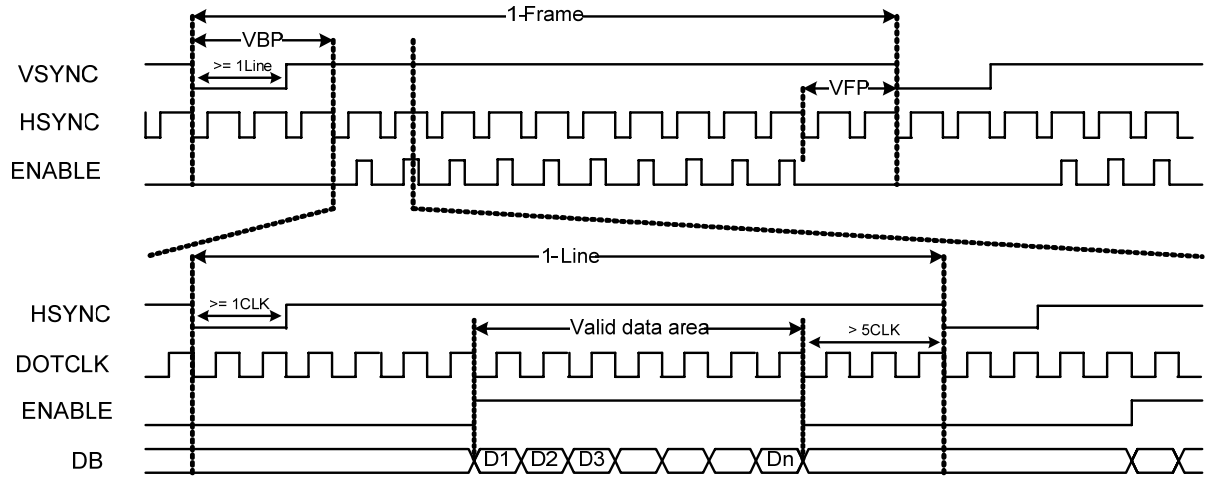
There are five timing conditions for RGB Interface that is determined according to RIM, COLMOD and each condition is described below.

Table 37. Rgb Interface Mode Selection

RIM	COLMOD[6:4]	Color Depth
0	110	262k-color (1 transfer/pixel)
	101	65k-color (1 transfer/pixel)
1	110	262k-color (3 transfer/pixel)
	101	65k-color (3 transfer/pixel)

3.4.3. RGB MODE

3.4.3.1. RGB Mode – 18-bit I/F

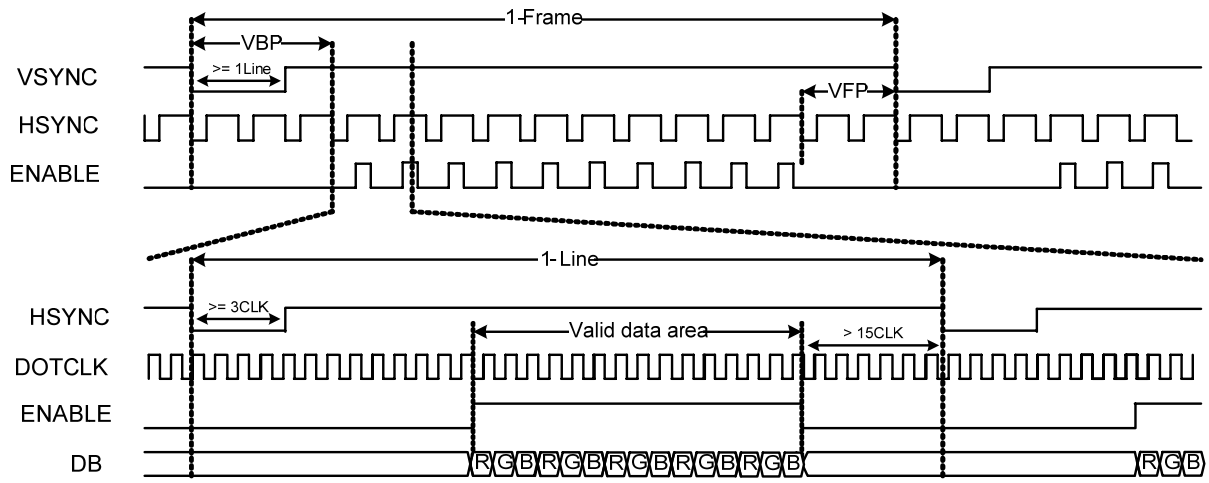


RGB mode 1 – 18-bit I/F timing diagram (RIM = 0)

Note.

DPL=0, EPL=1, HPL=0 and VPL=0 of IFCTL (F7h) command.

3.4.3.2. RGB Mode – 6-bit I/F



RGB mode 1 – 6-bit I/F timing diagram (RIM = 1)

Note.

DPL=0, EPL=1, HPL=0 and VPL=0 of IFCTL (F7h) command.

3.4.4. RGB DISPLAY DATA FORMAT

3.4.4.1. RGB 18-bit I/F – 262k-color

Table 38. 18-Bit Interface for 666 1/1 Formats

Count	1	2	…	239	240
DB17	0R5	1R5	…	238R5	239R5
DB16	0R4	1R4	…	238R4	239R4
DB15	0R3	1R3	…	238R3	239R3
DB14	0R2	1R2	…	238R2	239R2
DB13	0R1	1R1	…	238R1	239R1
DB12	0R0	1R0	…	238R0	239R0
DB11	0G5	1G5	…	238G5	239G5
DB10	0G4	1G4	…	238G4	239G4
DB9	0G3	1G3	…	238G3	239G3
DB8	0G2	1G2	…	238G2	239G2
DB7	0G1	1G1	…	238G1	239G1
DB6	0G0	1G0	…	238G0	239G0
DB5	0B5	1B5	…	238B5	239B5
DB4	0B4	1B4		238B4	239B4
DB3	0B3	1B3		238B3	239B3
DB2	0B2	1B2	…	238B2	239B2
DB1	0B1	1B1	…	238B1	239B1
DB0	0B0	1B0	…	238B0	239B0

3.4.4.2. RGB 18-Bit I/F – 65k-color

Table 39. 18-Bit Interface for 565 1/1 Formats

Count	1	2	…	239	240
DB17					
DB16					
DB15	0R4	1R4	…	238R4	239R4
DB14	0R3	1R3	…	238R3	239R3
DB13	0R2	1R2	…	238R2	239R2
DB12	0R1	1R1	…	238R1	239R1
DB11	0R0	1R0	…	238R0	239R0
DB10	0G5	1G5	…	238G5	239G5

Count	1	2	…	239	240
DB9	0G4	1G4	…	238G4	239G4
DB8	0G3	1G3	…	238G3	239G3
DB7	0G2	1G2	…	238G2	239G2
DB6	0G1	1G1	…	238G1	239G1
DB5	0G0	1G0	…	238G0	239G0
DB4	0B4	1B4	…	238B4	239B4
DB3	0B3	1B3		238B3	239B3
DB2	0B2	1B2		238B2	239B2
DB1	0B1	1B1	…	238B1	239B1
DB0	0B0	1B0	…	238B0	239B0

3.4.4.3. RGB 6-Bit I/F – 262k-color

Table 40. 6-Bit Interface Type Ⅰ for 666 1/3 Formats

Count	1	2	3	…	718	719	720
DB5	0R5	0G5	0B5	…	239R5	239G5	239B5
DB4	0R4	0G4	0B4	…	239R4	239G4	239B4
DB3	0R3	0G3	0B3	…	239R3	239G3	239B3
DB2	0R2	0G2	0B2	…	239R2	239G2	239B2
DB1	0R1	0G1	0B1	…	239R1	239G1	239B1
DB0	0R0	0G0	0B0	…	239R0	239G0	239B0

3.4.4.4. RGB 6Bit I/F – 65k-color

Table 41. 6-Bit Interface Type Ⅰ for 565 1/3 Formats

Count	1	2	3	…	718	719	720
DB5	0R4	0G5	0B4	…	239R4	239G5	239B4
DB4	0R3	0G4	0B3	…	239R3	239G4	239B3
DB3	0R2	0G3	0B2	…	239R2	239G3	239B2
DB2	0R1	0G2	0B1	…	239R1	239G2	239B1
DB1	0R0	0G1	0B0	…	239R0	239G1	239B0
DB0		0G0		…		239G0	

3.4.5. DISPLAY TIMING OF RGB INTERFACE

3.4.5.1. Display timing when rgb data is written at shift register

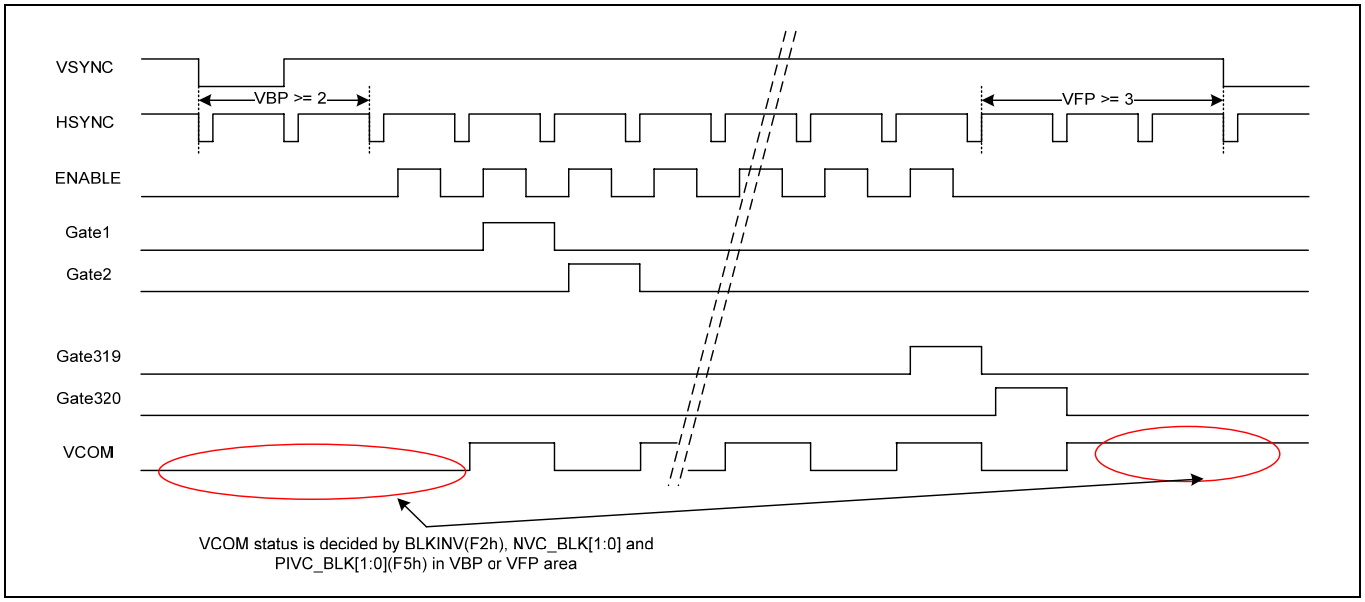


Figure48. Display Timing Diagram When RAM_ACCS = 0 (F7h)

Note.

When RAM_ACCS=0, real Vertical Back Porch is VBP + 1 and real Vertical Front Porch is VFP – 1 .

3.4.5.2. Display timing when rgb data is written at memory

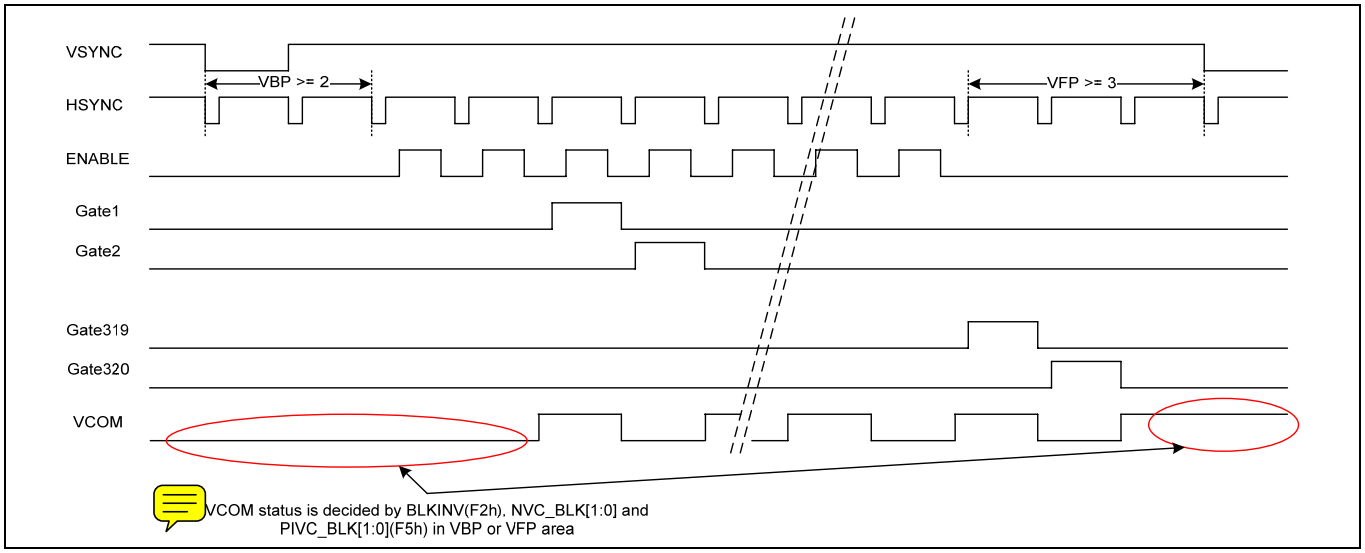


Figure49. Display Timing Diagram When RAM_ACCS = 1 (F7h)

Note.

When RAM_ACCS=1, real Vertical Back Porch is VBP + 2 and real Vertical Front Porch is VFP – 2 .

3.5. VSYNC INTERFACE

3.5.1. DEFINITION

The S6D04H0 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

When DM1-0=”10”, VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is writ

ten to RAM via the system interface with higher speed than for internal display operation. This method enables tearing-free display of motion pictures with the conventional interface.

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

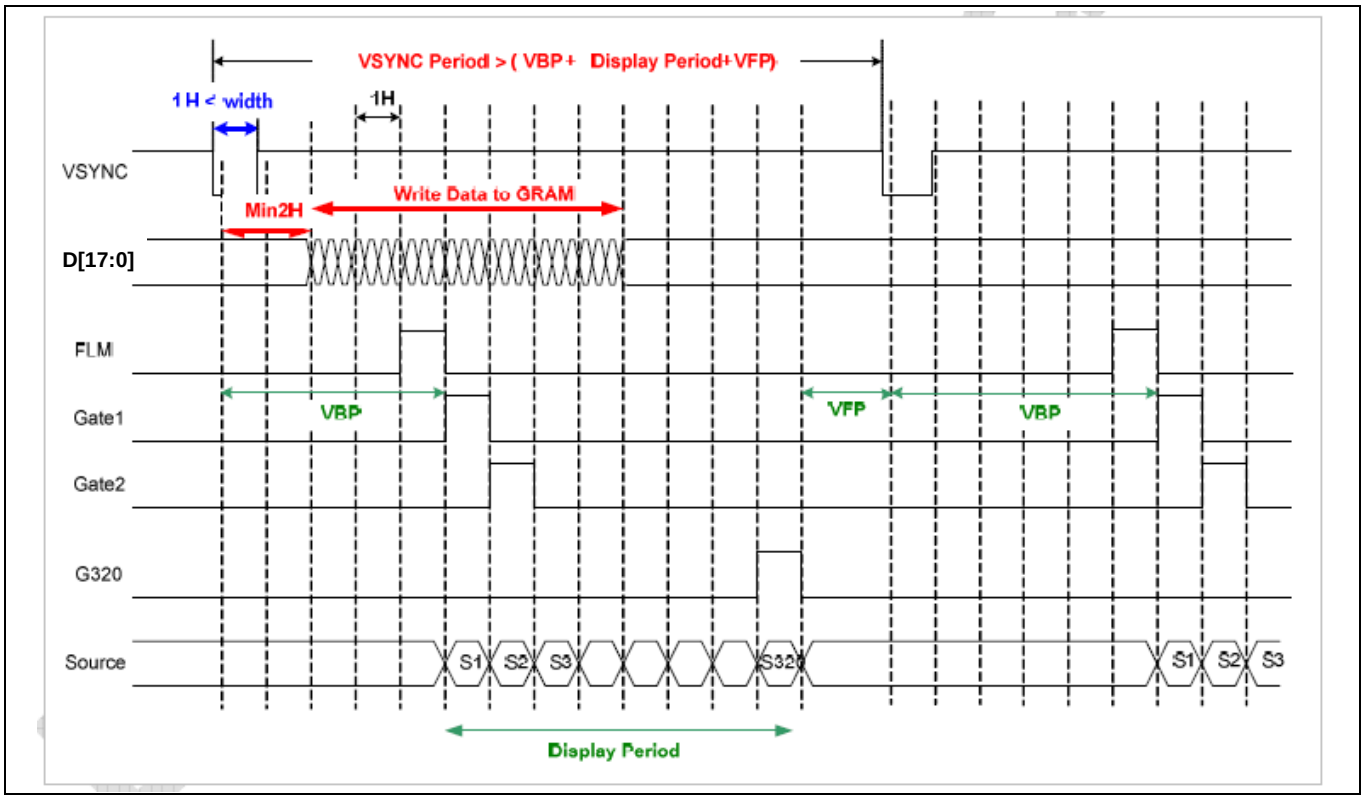


Figure50. Timing Diagram of VSYNC I/F

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result

obtained from the calculation shown below. The internal memory writing address counter is reset by VSYNC. So, insure interval time between VSYNC falling and GRAM data writing.

Note.

1. VSYNC period should always be constant. If not, some degradation of display such as flicker may occur in LCD system.
2. Display data don't need to be written for every VSYNC period. For example, any system is working under 60Hz frame rate and 30-fps motion picture condition. So being written display data for every other frame would be enough.

3.5.2. VSYNC INTERFACE MODE

3.5.2.1. Leading mode.

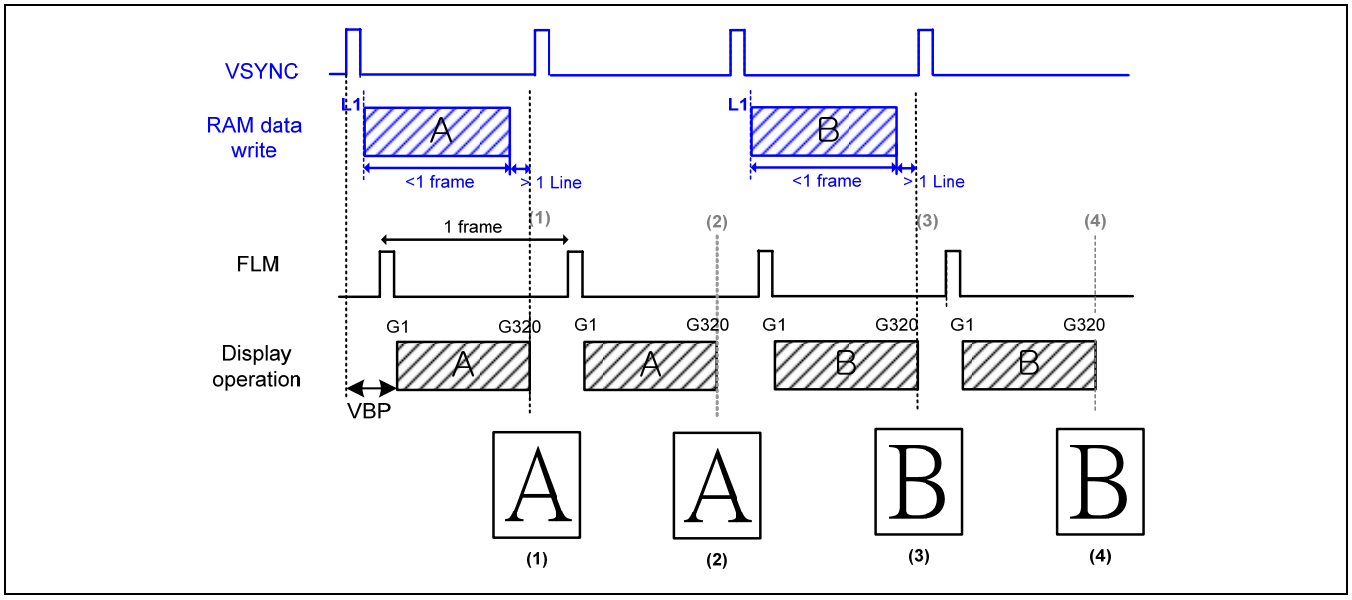


Figure51. Operation for Leading Mode of VSYNC Interface (VPL = 1)

3.5.2.2. Lagging mode.

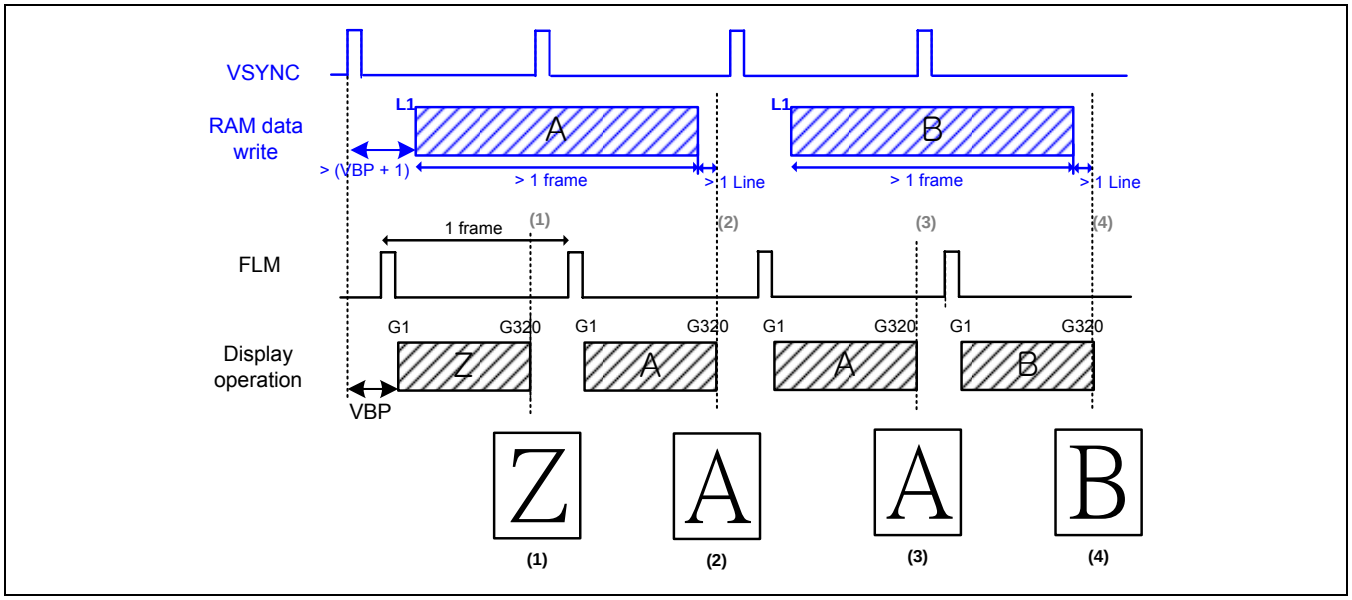


Figure52. Operation for Lagging Mode of VSYNC Interface (VPL = 1)

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*Internal clock frequency (fosc) [Hz] = Frame freq. × (Display line (NL) + Front porch (VFP) + Back porch (VBP)) × *37-Clock × Fluctuation*

Minimum speed for RAM writing [Hz] > 320 × Display line (NL) / {((Back porch (BP) + Display line (NL) – Margin) × 37 Clock) / fosc}

Note.

When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

An example is shown below.

3.5.3. EXAMPLE

Display size	240RGB × 320 lines
Display line number	320 lines
Back/Front porch	8 lines / 8 lines (VBP / VFP)
Frame Frequency	60Hz

Internal clock frequency (fosc) [Hz] = 60 Hz × (320 + 8 + 8) lines× *37 clock × 1.1 / 0.9 = 694.61 kHz

Note.

1. Calculating the internal clock frequency requires considering the fluctuation. In the above case a 10% Fluctuation within the VSYNC period is assumed.
2. The fluctuation includes LSI production variation and air temperature fluctuation. Other fluctuations, including those for the external resistors and the supplied power, are not included in this example. Please keep in mind that a margin for these factors is also needed.
   Minimum speed for RAM writing [Hz] > 240 × 320 / {((14 + 320 – 2) lines × *37 clock) / 694.61 kHz} = 4.38 MHz
3. In this case RAM writing starts immediately after the falling edge of VSYNC.
4. The margin for display line should be two lines or more at the completion of RAM writing for one frame.

* 1H clock (default) = 148 display clock

Note) display clock = oscillator clock /3

CHAPTER 4

FUNCTIONAL DESCRIPTION

4. FUNCTIONAL DESCRIPTION

4.1. POWER

4.1.1. POWER ON / OFF SEQUENCE

VDD3 and VCI can be applied in any order.

VDD3 and VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDD3 must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDD3 or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note.

1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before the reception of Sleep Out command. Same is the case between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 4.1.1.1, it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise, function is not guaranteed.

The power on/off sequence is illustrated in the next pages.

4.1.1.1. Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDD3 have been applied – otherwise, correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

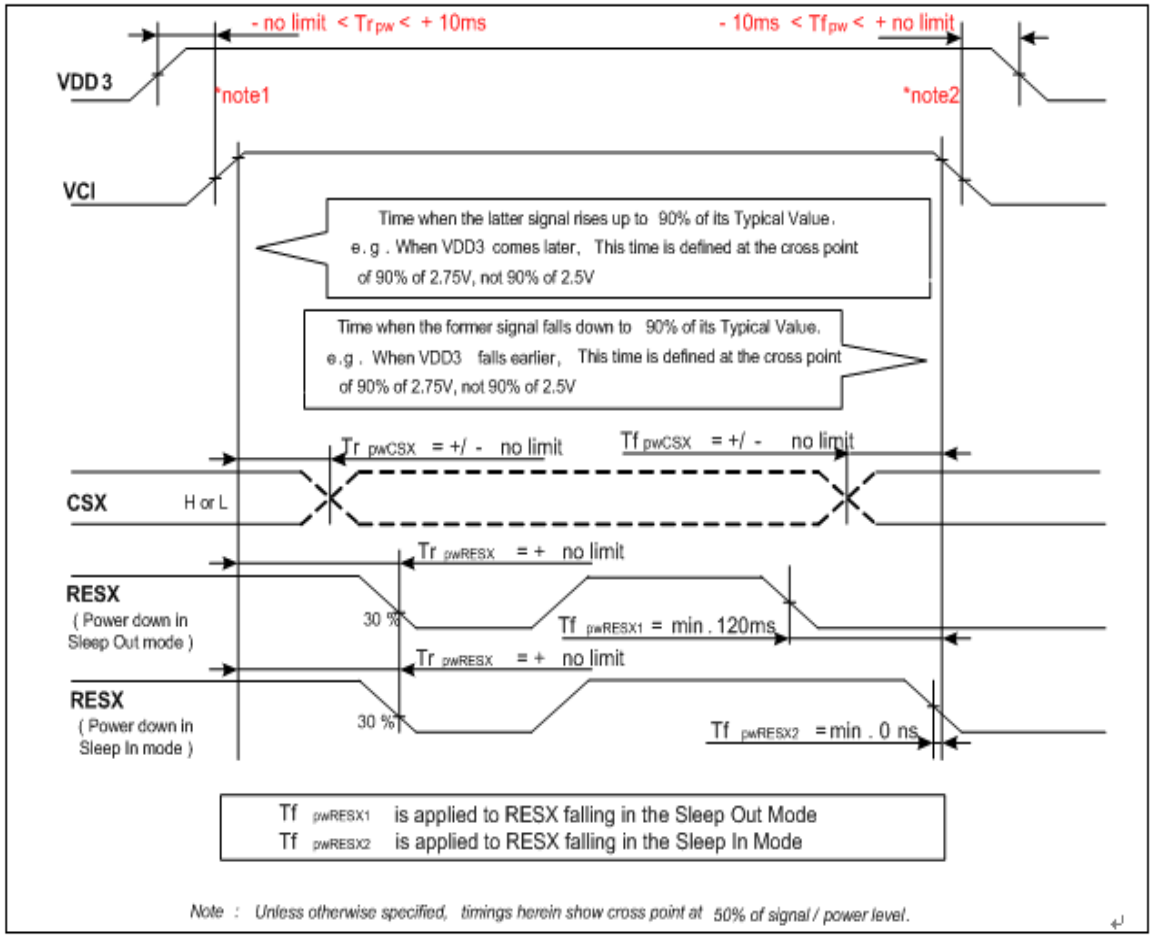


Figure 102 RESX line is held high or unstable by host at power on

Figure53. RESX Line is Held High or Unstable by Host At Power On

Note1. In case that VCI comes first, VDD3 should be applied & settled within 10ms after VCI is applied.

Note2. In case that VCI disappears first, VDD3 should also be turned off within 10ms after VCI is off.

Case 2 – RESX line is held low by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and VDD3 have been applied.

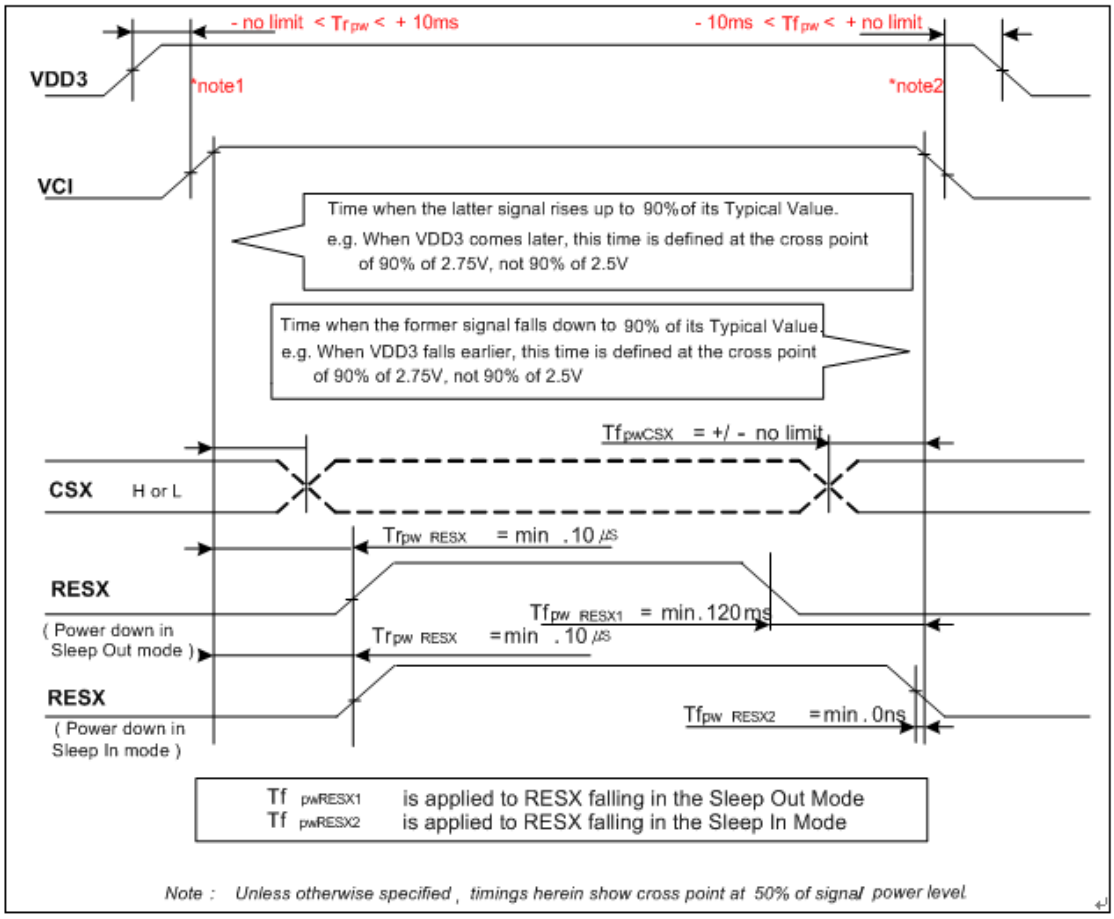


Figure 103 RESX line is held low by host at power on

Figure54. RESX Line is Held Low by Host At Power On

Note1. In case that VCI comes first, VDD3 should be applied & settled within 10ms after VCI is applied.

Note2. In case that VCI disappears first, VDD3 should also be turned off within 10ms after VCI is off.

4.1.2. ABRUPT POWER OFF

The abrupt power-off represents a situation where, for e.g, a battery is removed without the expected power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abrupt power-off, the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power-On Sequence” powers it up.

4.1.3. POWER LEVELS

6 level modes are defined they are in order of Maximum power consumption to Minimum power consumption.

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out
   In this mode, the full display area is used but with 8 colors,
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used but with 8 colors
5. Sleep In Mode
   In this mode, the step up circuit, Internal oscillator and panel driver circuit are stopped. Only the MPU interface and memory works with VDD3 power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and VDD3 are removed

Note.

Transition between modes 1-5 is controllable by MPU commands. Mode 6 is entered only when both Power supplies are removed.

4.1.4. POWER FLOW CHART FOR DIFFERENT POWER MODES

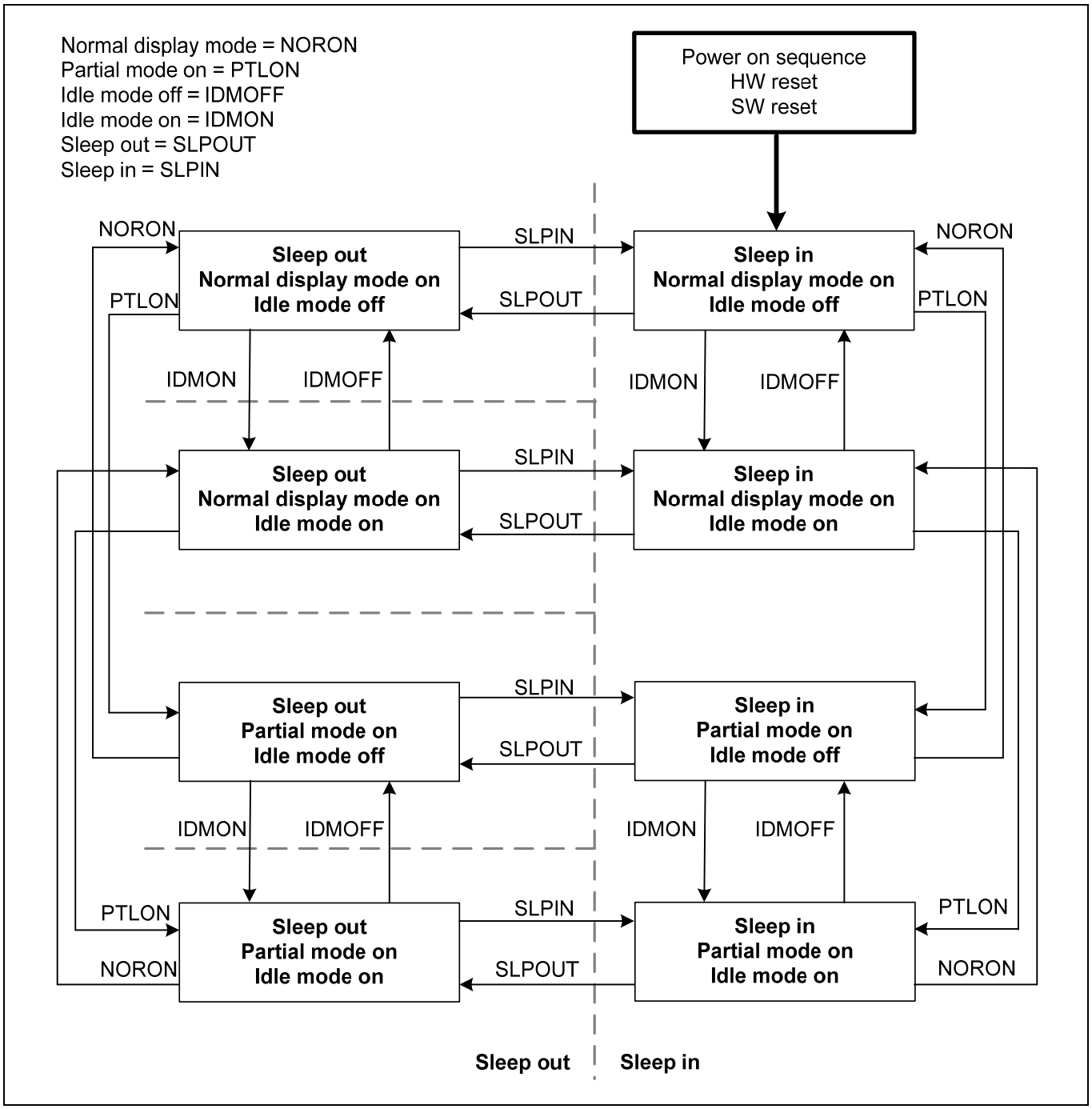


Figure55. Power Flow Chart

Note.

1. There is no abnormal visual effect when there is a change from one power mode to another power mode.
2. There is no limitation, which is not specified by this spec, when there is a change from one power mode to another power Mode

4.1.5. POWER SUPPLY

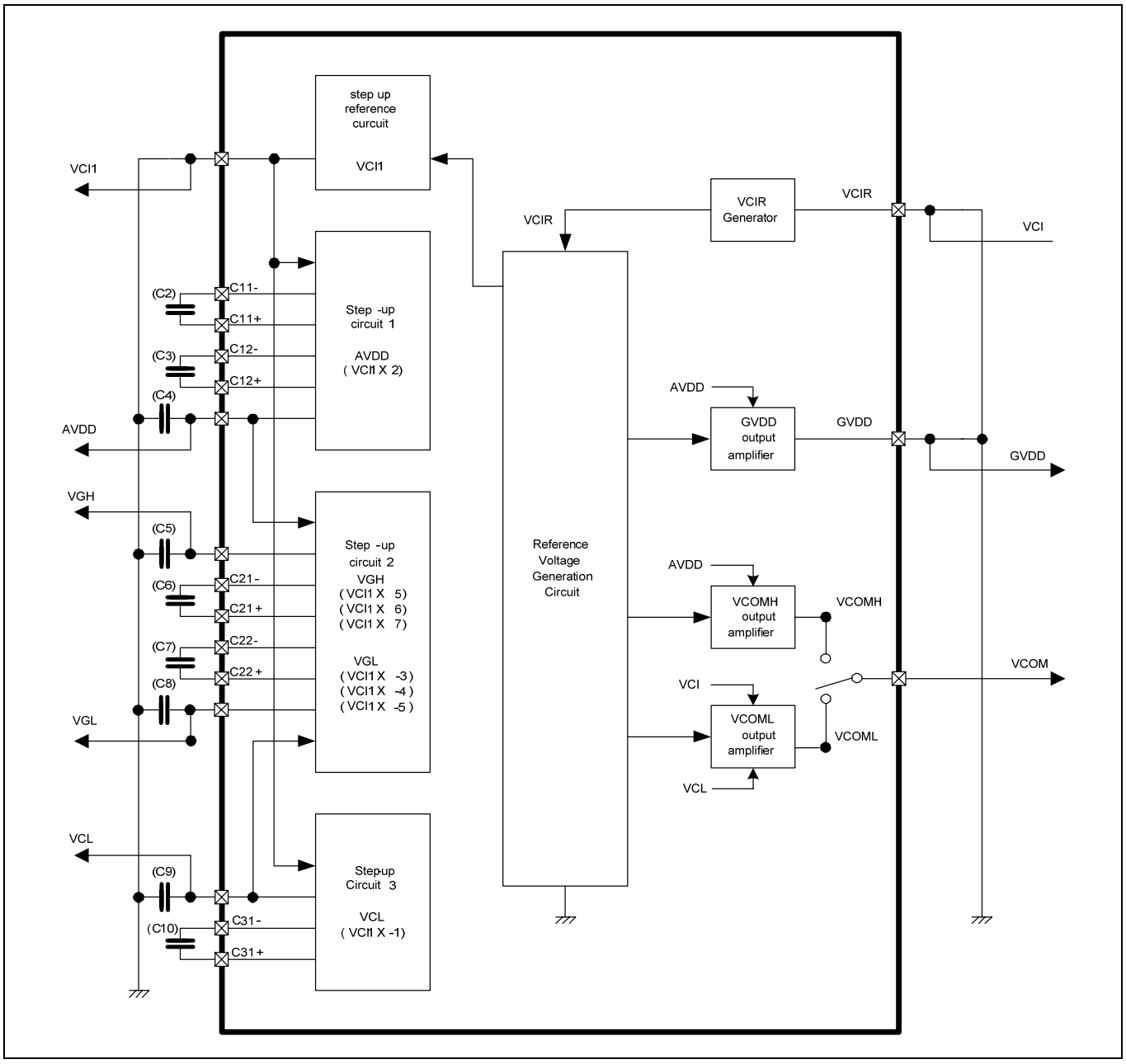


Figure56. Configuration of the Internal Power-Supply Circuit

The step-up circuits consist of step-up circuits 1 to 3. Step-up circuit 1 doubles the voltage which is supplied to VCI1 for AVDD level, and VCI1 is positively amplified by 5 or 6 or 7 times for VGH level and negatively amplified by 3 or 4 or 5 times for VGL level in step-up circuit 2. Step-up circuit 3 flips the VCI1 level and generates the VCL level. These step-up circuits generate the supply powers of AVDD, VGH, VGL and VCL in sequence after regulation. The regulated GVDD is for the grayscale voltage, another regulated VCOMH and the other regulated

VCOML are for VCOM which is connected to counter electrode of TFT LCD panel, and generate each level depending on that voltage. Connect VCOM to the TFT panel.

4.1.5.1. Pattern diagrams for voltage setting

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.

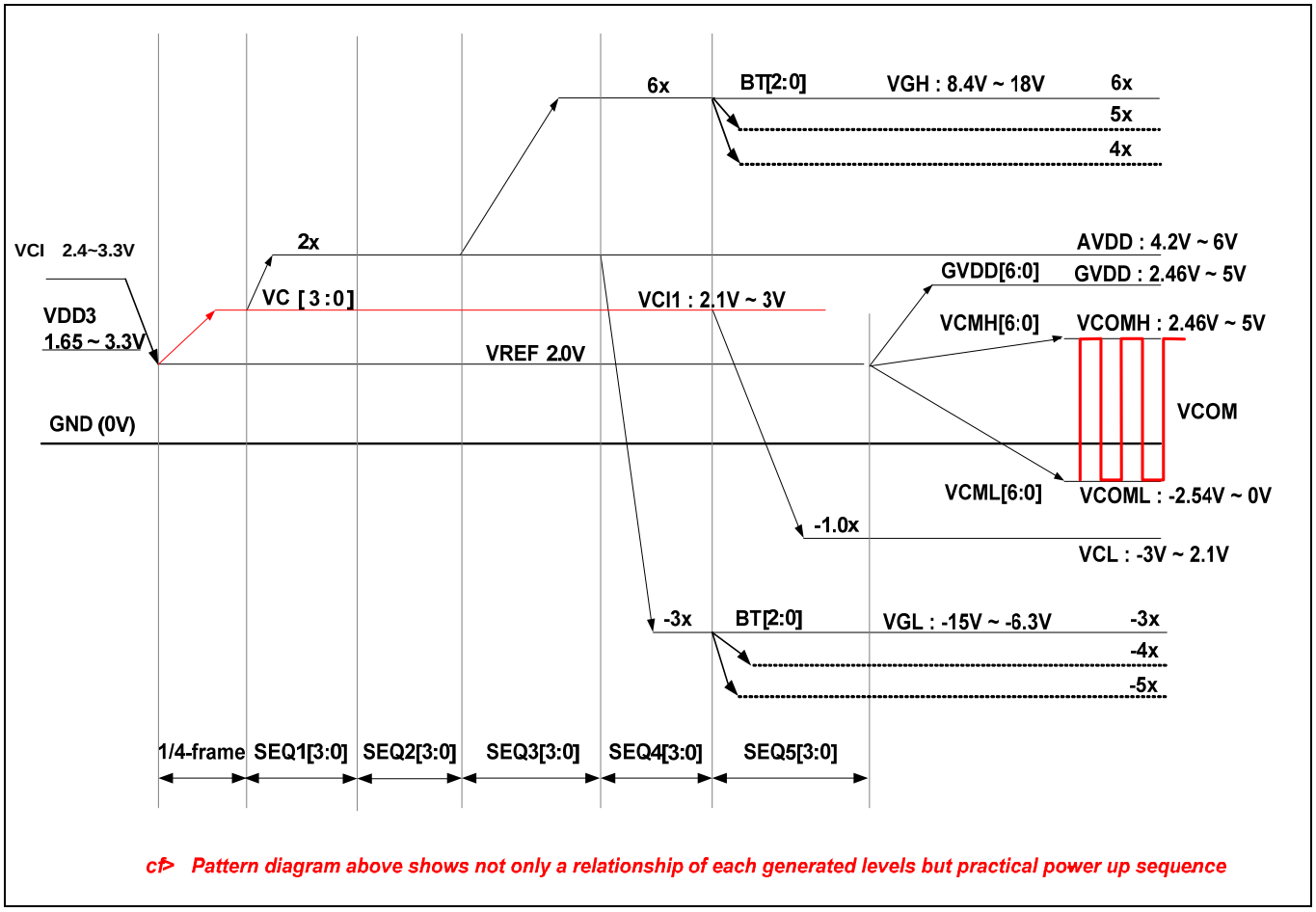


Figure57. Sequence of Power Boosting S6D04H0

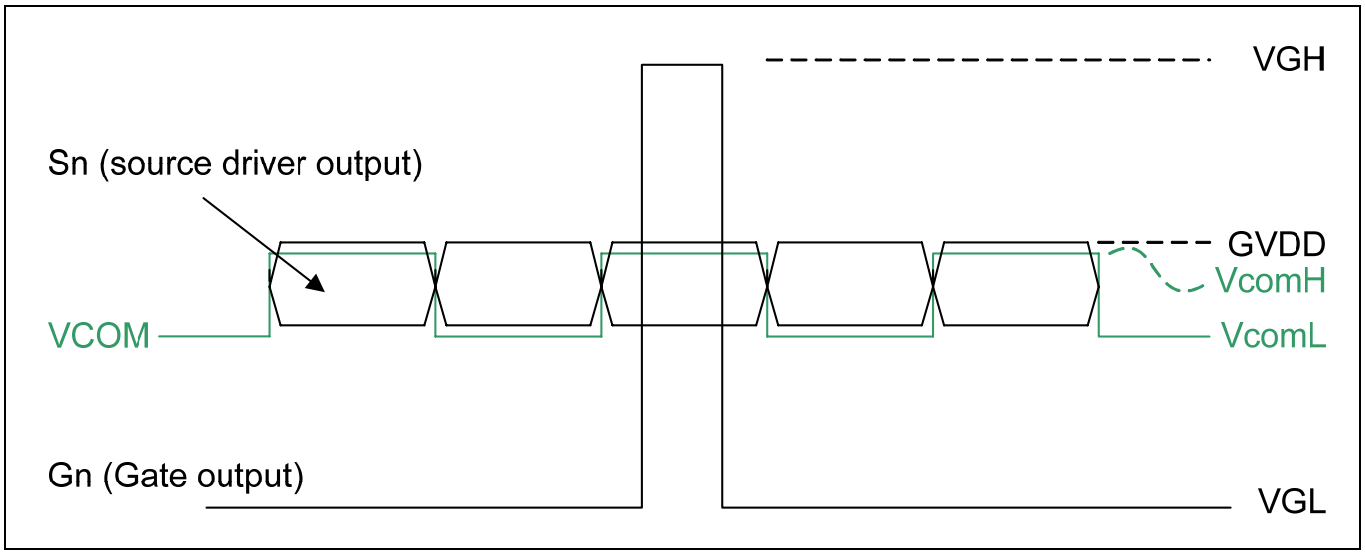


Figure58. Power-Up Pattern Diagram & An Example of Source/VCOM Waveforms

4.1.6. SETUP FLOW OF POWER

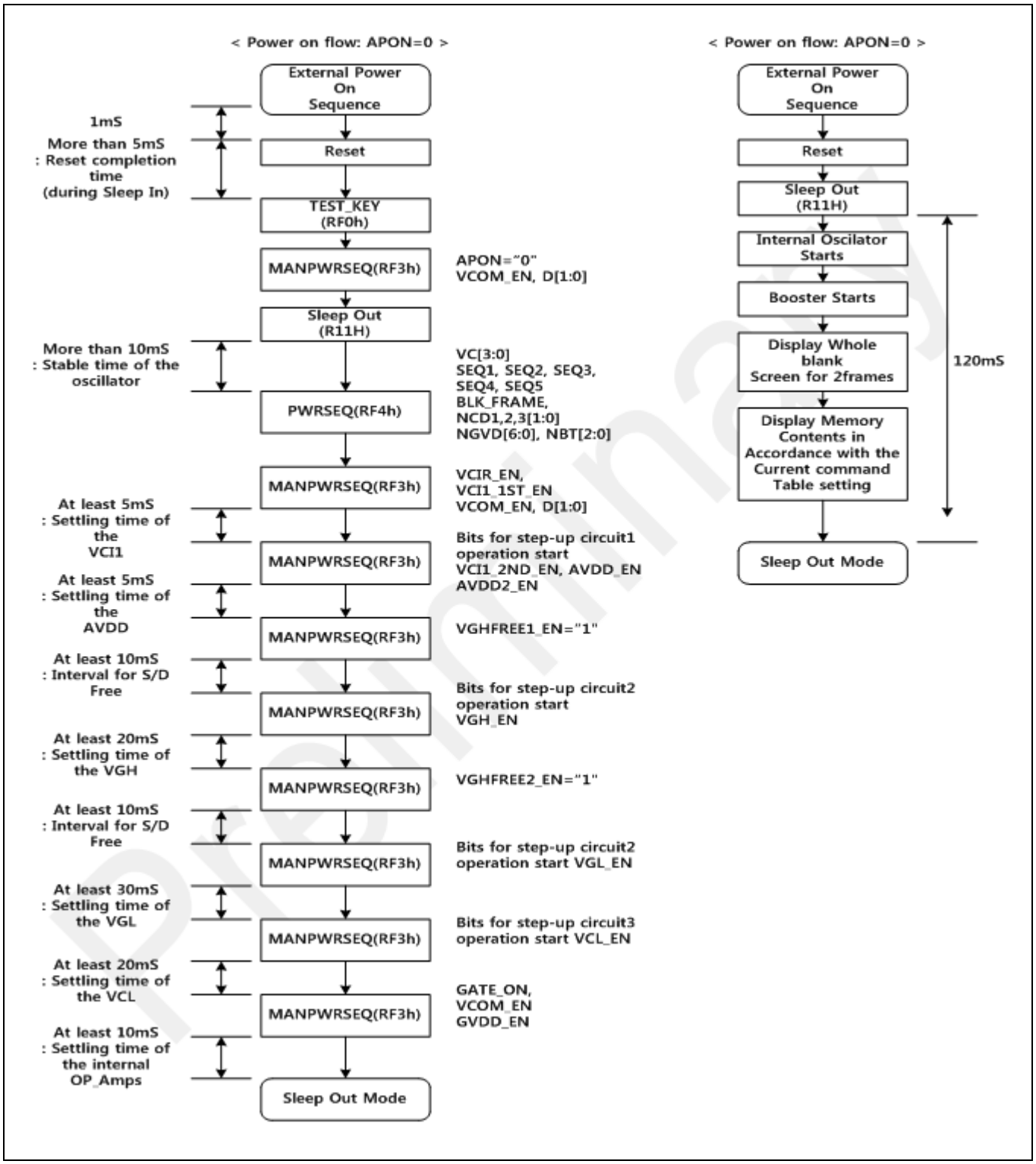


Figure59. Power-Up Pattern Diagram

4.2. SOURCE

4.2.1. GAMMA ADJUSTMENT FUNCTION

S6D04H0 provides the gamma adjustment function to display 262,144 colors simultaneously for each R/G/B color. The gamma adjustment executed by the high/ mid/ low level adjustment registers determines 11 grayscale reference levels. Furthermore, since the high-level adjustment register, mid-level adjustment register and the low-level adjustment register have the positive polarities and negative polarities, you can adjust them to match LCD panel and a gamma for each R/G/B color, respectively.

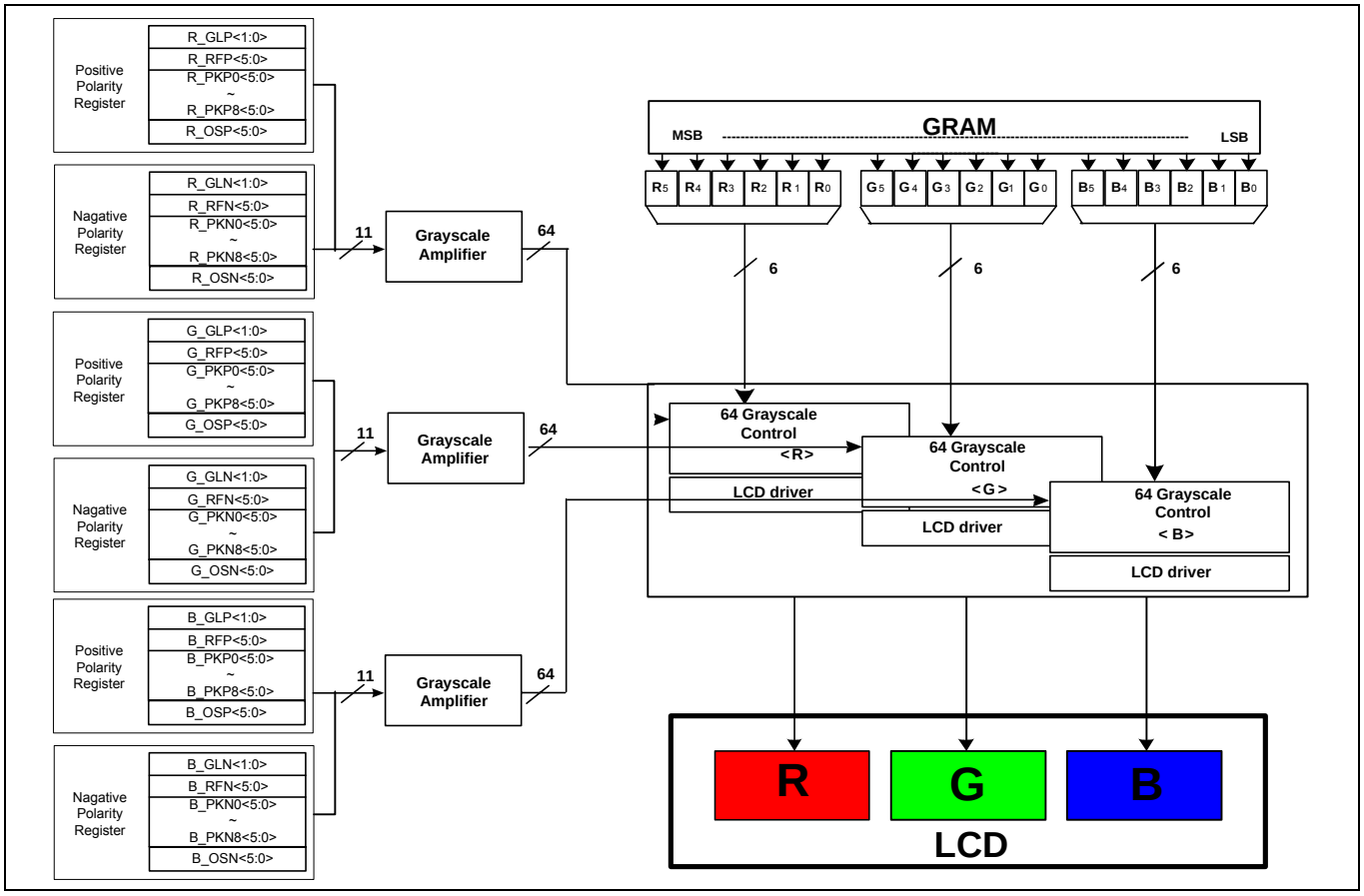


Figure60. Gamma Adjustment Block Diagram

4.2.2. GAMMA CURVE

4.2.2.1. Gamma curve 1 (GC0)

Gamma Curve 1 (GC0), applies the function. $y = x^{2.2}$

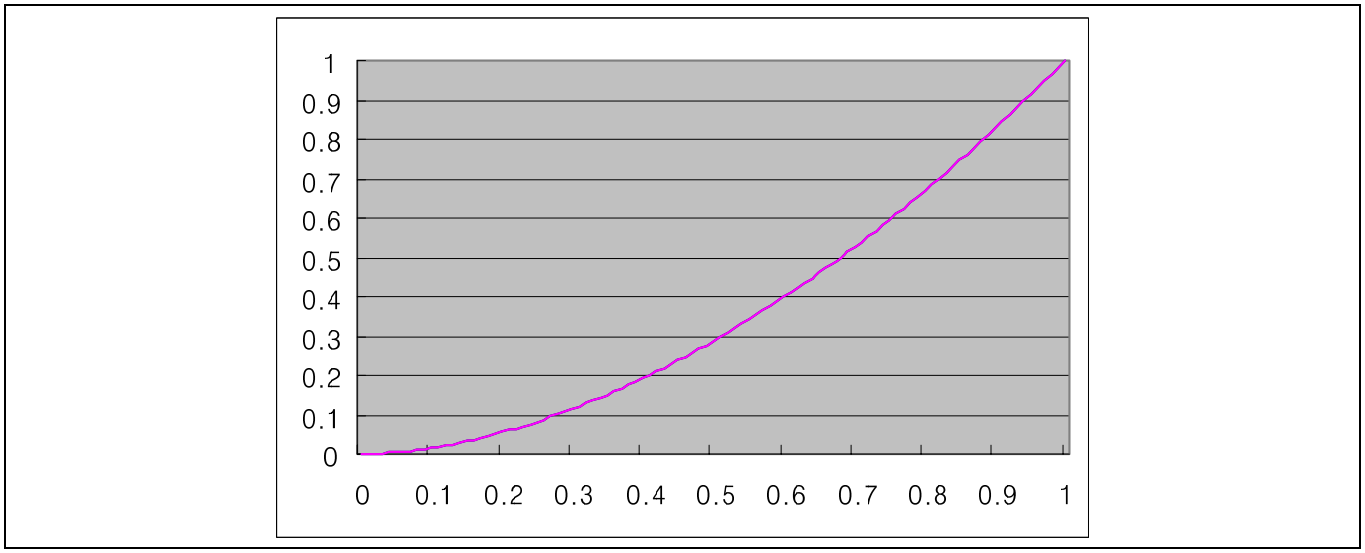


Figure61. Gamma $y = x^{2.2}$

4.2.2.2. Gamma curve 2 (GC1)

Gamma Curve 2 (GC1), applies the function. $y = x^{1.8}$

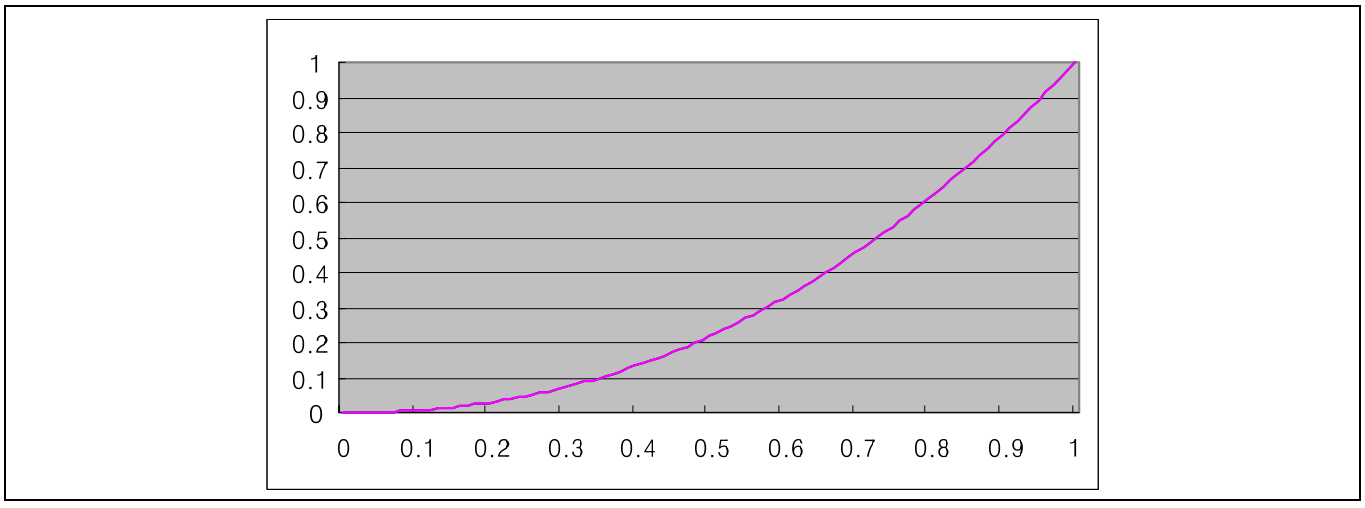


Figure62. Gamma $y = x^{1.8}$

4.2.2.3. Gamma curve 3(GC2)

Gamma Curve 3(GC2), applies the function. $y = x^{2.5}$

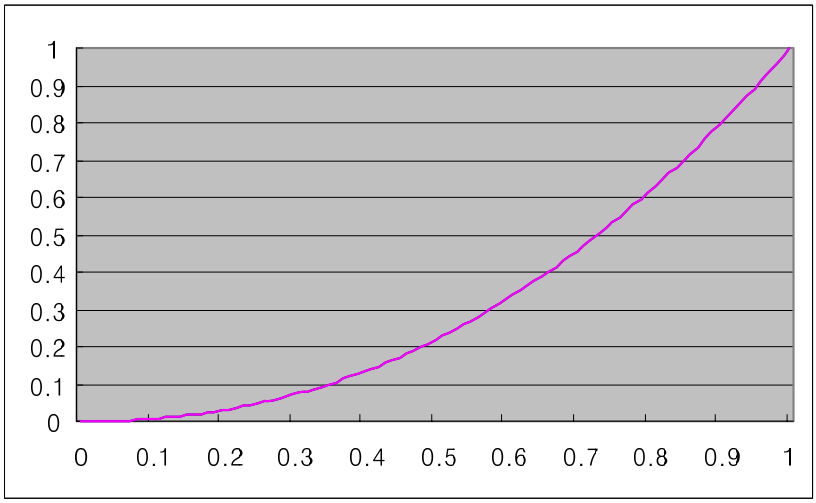


Figure63. Gamma $y = x^{2.5}$

4.2.2.4. Gamma curve 4 (GC3)

Gamma Curve 4 (GC3) is linear, i. e. $y = x^{1}$

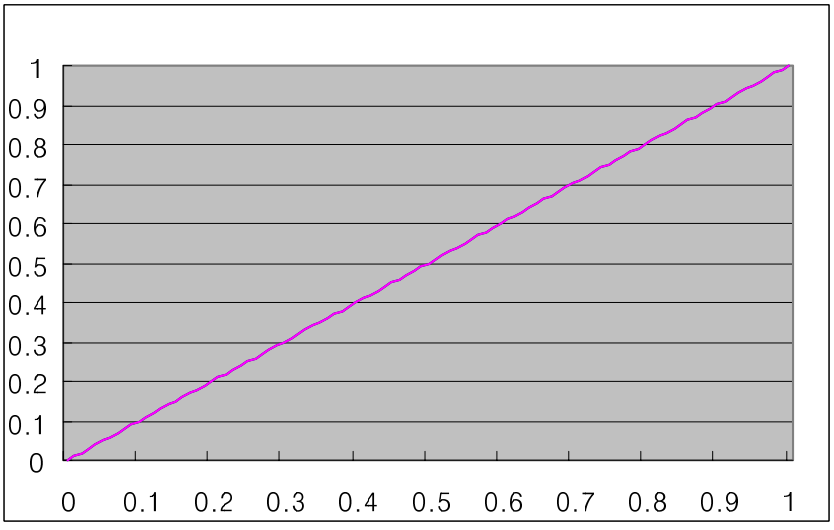


Figure64. Gamma $y = x^{1}$

4.2.3. STRUCTURE OF GRAYSCALE AMPLIFIER

S6D04H0 provides the gamma adjustment function to display 262,114 colors simultaneously for each R/G/B color. The gamma adjustment executed by the high/ mid/ low level adjustment registers determines 11 grayscale reference levels. Furthermore, since the high-level adjustment register, mid-level adjustment register and the low-level adjustment register have the positive polarities and negative polarities, you can adjust them to match LCD panel and a gamma for each R/G/B color, respectively.

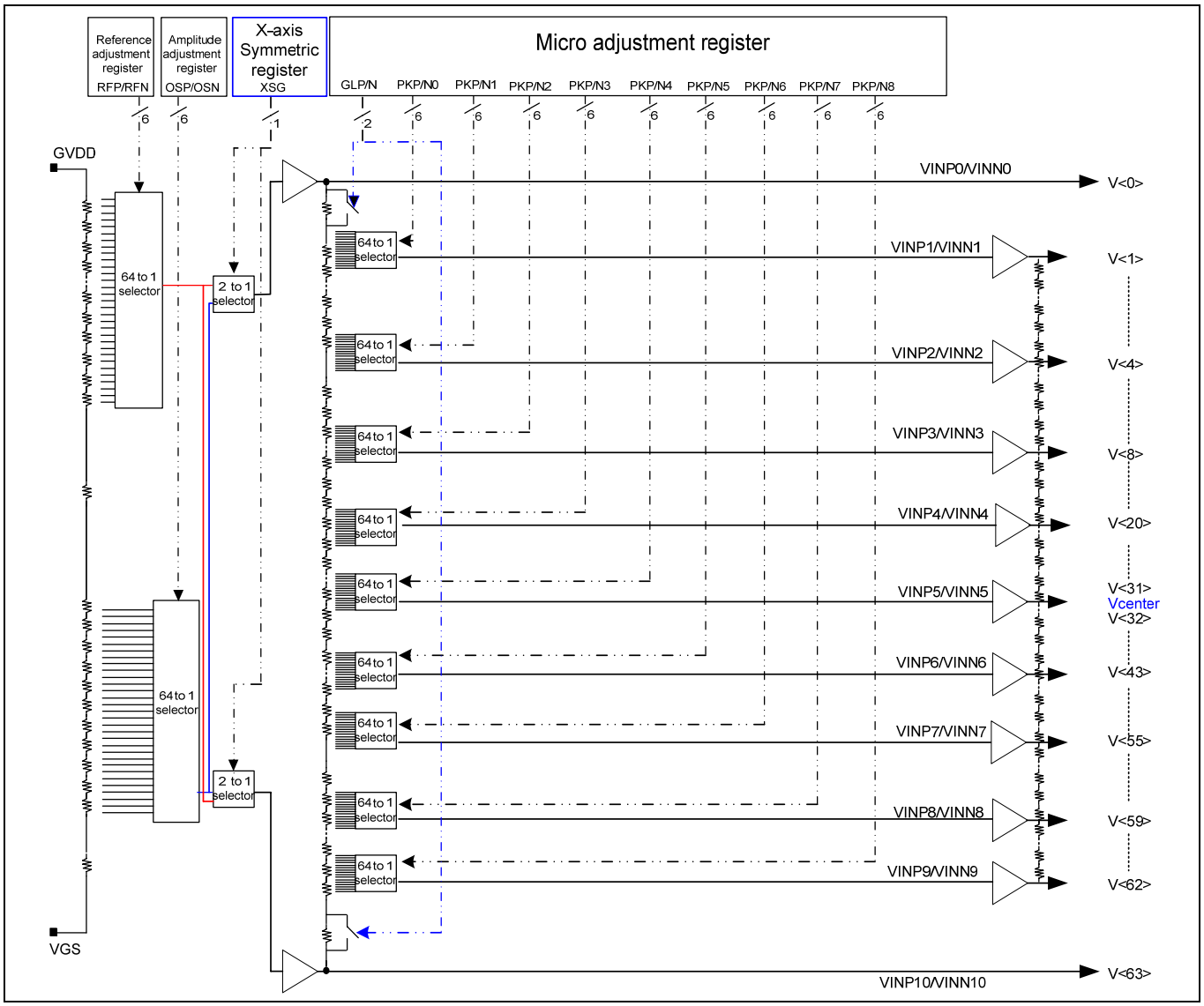


Figure65. Structure of Grayscale Amplifier

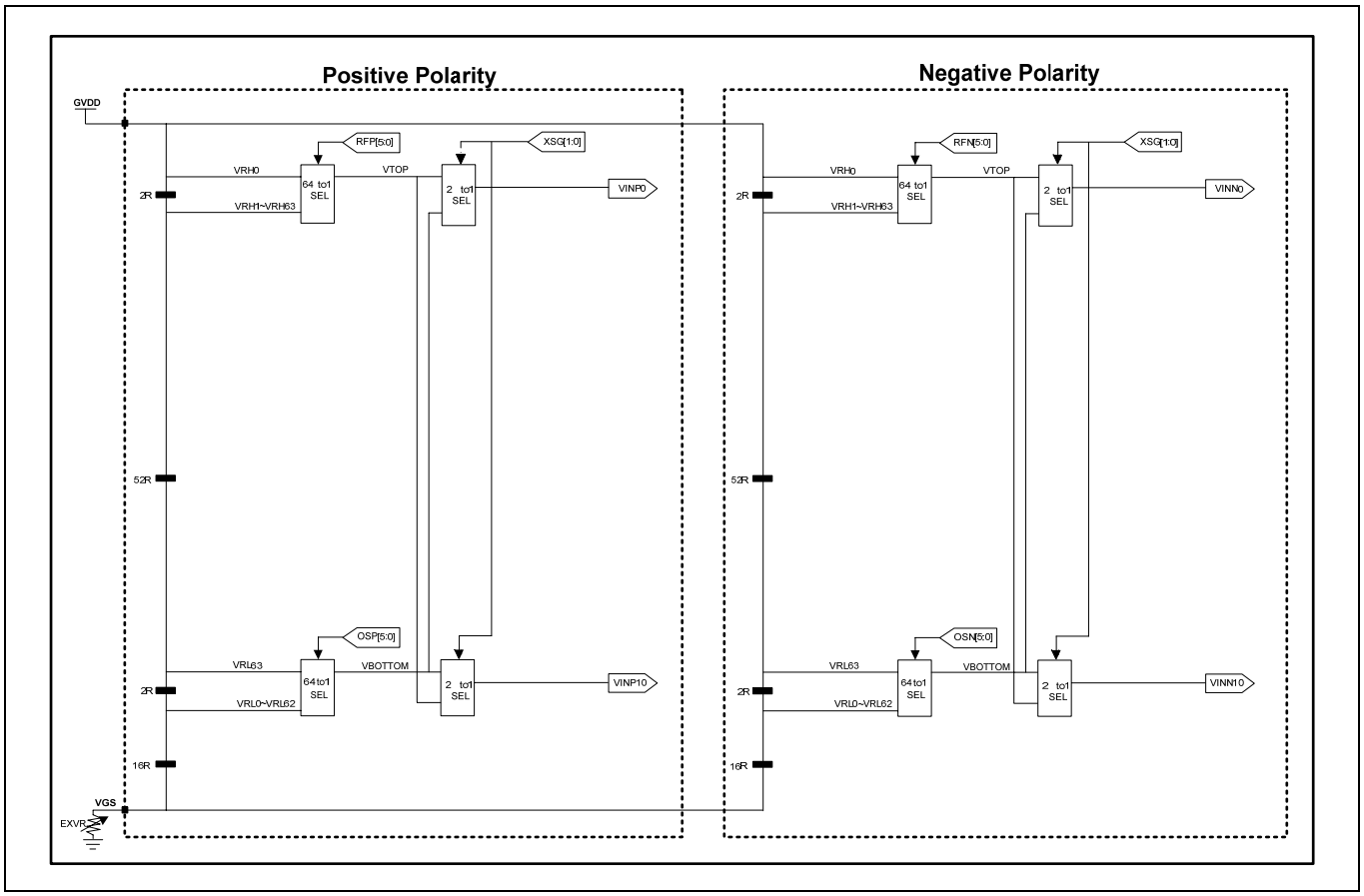


Figure66. Structure of Resistor Ladder Network I

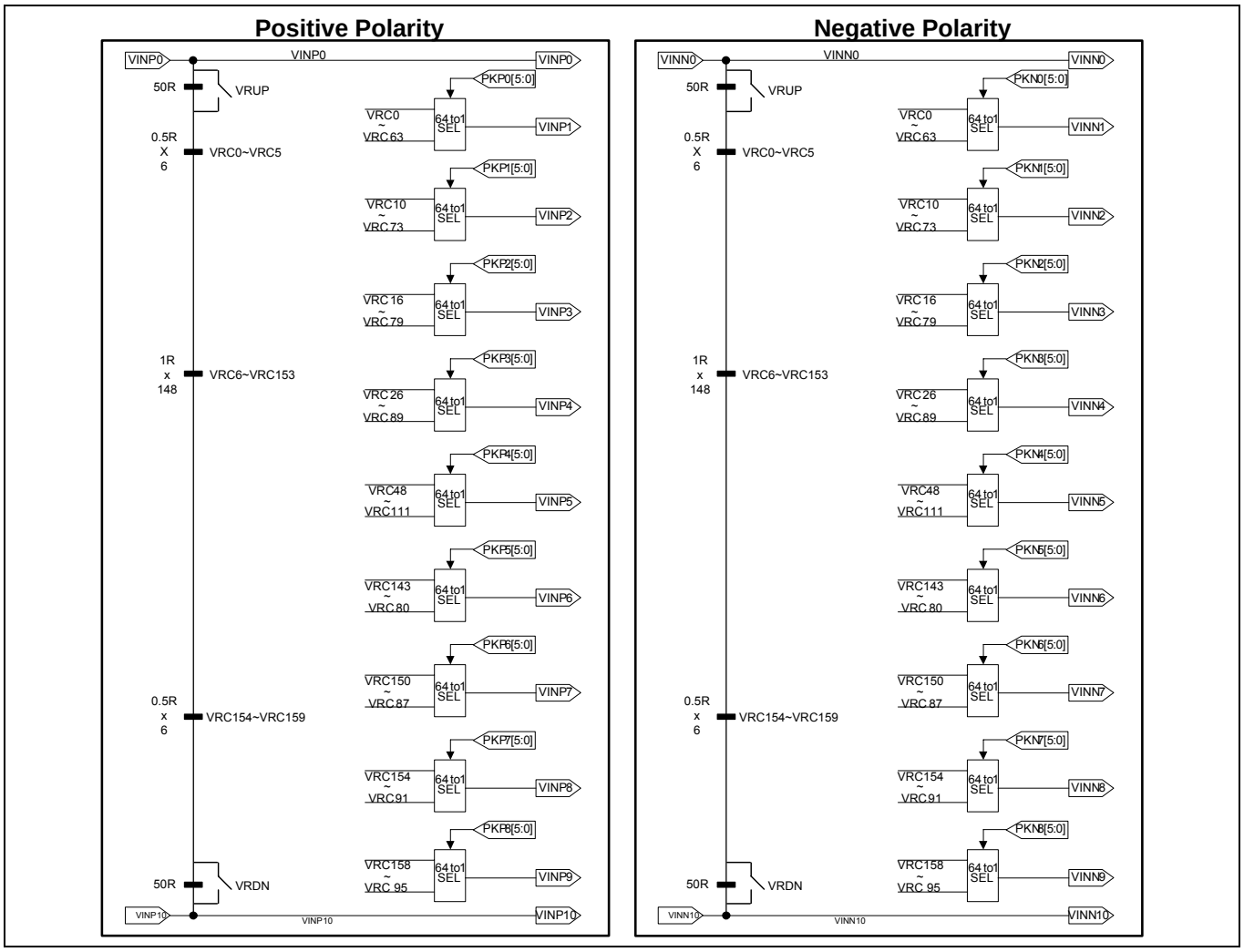


Figure67. Structure of Resistor Ladder Network Ⅱ

4.2.4. GAMMA ADJUSTMENT REGISTER

This block has registers to set up the grayscale voltage according to the gamma specification of the LCD panel. These registers can independently set up the positive/negative polarities. There are 4 types of register groups to adjust the amplitude on the grayscale characteristics of the grayscale voltage, and R/G/B gamma adjustment registers are separated. The following figures indicate the operation of each adjustment registers.

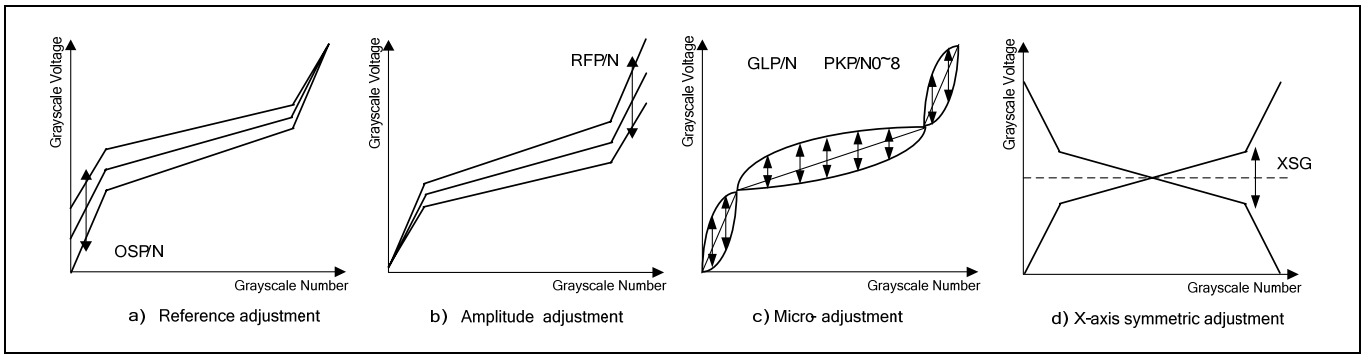


Figure68. The Operation of Adjusting Register

4.2.4.1. Reference adjustment register

The Reference adjustment register is used to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the VINP10/VINN10 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4.2.4.2. Amplitude adjustment register

The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the VINP0/VINN0 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4.2.4.3. Micro-adjustment register

The Micro adjustment register is employed to make subtle adjustment to the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

4.2.4.4. X-axis symmetric adjustment register

The X-axis symmetric adjustment register is to adjust X-axis symmetric of the grayscale voltage. This register can be detailedly explained with NGF register selection. 1st case; when XSG=0 and NGF=1, Vp<N>+Vn<N>=Vp<0>+Vn<0> and gamma symmetric axis is (Vp<0>+Vn<0>)/2. 2nd case; when XSG=0 and NGF=0, negative gamma voltage can be changed using negative gamma register value and symmetric axis will be changed according to negative gamma voltage. 3rd case; when XSG=1 and NGF=1, Vp<N>=Vn<|63-N|>. 4th

case; when XSG=1 and NGF=0, Vp<N>+Vn<N> ≠ Vp<0>+Vn<0> but can have similar value in some degree using both positive and negative gamma registers.

Table 42. Gamma Adjusting Register

Register	Positive Polarity	Negative Polarity	Set-up Contents
Reference adjustment Amplitude adjustment	OSP[5:0]	OSN[5:0]	The voltage of VBOTTOM is selected by the 64 to 1 selector
	RFP[5:0]	RFN[5:0]	The voltage of VTOP is selected by the 64 to 1 selector
X-axis symmetric adjustment	XSG		The voltage of VINP10/VINN10 is selected by the 2 to 1 selector
			The voltage of VINP0/VINN0 is selected by the 2 to 1 selector
Micro adjustment	GLP[1:0]	GLN[1:0]	The voltage of grayscale number from 1 to 62 is adjusted by the variable resistor
	PKP0[5:0]	PKN0[5:0]	The voltage of grayscale number 1 is selected by the 64 to 1 selector
	PKP1[5:0]	PKN1[5:0]	The voltage of grayscale number 4 is selected by the 64 to 1 selector
	PKP2[5:0]	PKN2[5:0]	The voltage of grayscale number 8 is selected by the 64 to 1 selector
	PKP3[5:0]	PKN3[5:0]	The voltage of grayscale number 20 is selected by the 64 to 1 selector
	PKP4[5:0]	PKN4[5:0]	The voltage of grayscale number VC (middle voltage between v<31> and V<32>) is selected by the 64 to 1 selector
	PKP5[5:0]	PKN5[5:0]	The voltage of grayscale number 43 is selected by the 64 to 1 selector
	PKP6[5:0]	PKN6[5:0]	The voltage of grayscale number 55 is selected by the 64 to 1 selector
	PKP7[5:0]	PKN7[5:0]	The voltage of grayscale number 59 is selected by the 64 to 1 selector
	PKP8[5:0]	PKN8[5:0]	The voltage of grayscale number 62 is selected by the 64 to 1 selector

4.2.5. RESISTOR LADDER NETWORK / SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are three ladder resistors including the 64 to 1 selector selecting voltage generated by the ladder resistance voltage. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel and another.

4.2.5.1. Resistor ladder network 1 / selector

There are 2 adjustments that are for the reference / amplitude adjustment (RFP(N)/ OSP(N)) and micro adjustment (PKP(N)). The voltage level is set by the reference / amplitude adjustment registers and micro adjustments as below.

Table 43. Amplitude Adjustment

Register Value RFP(N) [5:0]	Selected Voltage VTOP	Formula of VTOP
000000	VRH0	(320R/320R) * (GVDD-VGS) + VGS
000001	VRH1	(318R/320R) * (GVDD-VGS) + VGS
000010	VRH2	(316R/320R) * (GVDD-VGS) + VGS
000011	VRH3	(314R/320R) * (GVDD-VGS) + VGS
000100	VRH4	(312R/320R) * (GVDD-VGS) + VGS
000101	VRH5	(310R/320R) * (GVDD-VGS) + VGS
000110	VRH6	(308R/320R) * (GVDD-VGS) + VGS
000111	VRH7	(306R/320R) * (GVDD-VGS) + VGS
001000	VRH8	(304R/320R) * (GVDD-VGS) + VGS
001001	VRH9	(302R/320R) * (GVDD-VGS) + VGS
001010	VRH10	(300R/320R) * (GVDD-VGS) + VGS
001011	VRH11	(298R/320R) * (GVDD-VGS) + VGS
001100	VRH12	(296R/320R) * (GVDD-VGS) + VGS
001101	VRH13	(294R/320R) * (GVDD-VGS) + VGS
001110	VRH14	(292R/320R) * (GVDD-VGS) + VGS
001111	VRH15	(290R/320R) * (GVDD-VGS) + VGS
010000	VRH16	(288R/320R) * (GVDD-VGS) + VGS
010001	VRH17	(286R/320R) * (GVDD-VGS) + VGS
010010	VRH18	(284R/320R) * (GVDD-VGS) + VGS
010011	VRH19	(282R/320R) * (GVDD-VGS) + VGS
010100	VRH20	(280R/320R) * (GVDD-VGS) + VGS
010101	VRH21	(278R/320R) * (GVDD-VGS) + VGS

Register Value RFP(N) [5:0]	Selected Voltage VTOP	Formula of VTOP
010110	VRH22	(276R/320R) * (GVDD-VGS) + VGS
010111	VRH23	(274R/320R) * (GVDD-VGS) + VGS
011000	VRH24	(272R/320R) * (GVDD-VGS) + VGS
011001	VRH25	(270R/320R) * (GVDD-VGS) + VGS
011010	VRH26	(268R/320R) * (GVDD-VGS) + VGS
011011	VRH27	(266R/320R) * (GVDD-VGS) + VGS
011100	VRH28	(264R/320R) * (GVDD-VGS) + VGS
011101	VRH29	(262R/320R) * (GVDD-VGS) + VGS
011110	VRH30	(260R/320R) * (GVDD-VGS) + VGS
011111	VRH31	(258R/320R) * (GVDD-VGS) + VGS
100000	VRH32	(256R/320R) * (GVDD-VGS) + VGS
100001	VRH33	(254R/320R) * (GVDD-VGS) + VGS
100010	VRH34	(252R/320R) * (GVDD-VGS) + VGS
100011	VRH35	(250R/320R) * (GVDD-VGS) + VGS
100100	VRH36	(248R/320R) * (GVDD-VGS) + VGS
100101	VRH37	(246R/320R) * (GVDD-VGS) + VGS
100110	VRH38	(244R/320R) * (GVDD-VGS) + VGS
100111	VRH39	(242R/320R) * (GVDD-VGS) + VGS
101000	VRH40	(240R/320R) * (GVDD-VGS) + VGS
101001	VRH41	(238R/320R) * (GVDD-VGS) + VGS
101010	VRH42	(236R/320R) * (GVDD-VGS) + VGS
101011	VRH43	(234R/320R) * (GVDD-VGS) + VGS
101100	VRH44	(232R/320R) * (GVDD-VGS) + VGS
101101	VRH45	(230R/320R) * (GVDD-VGS) + VGS
101110	VRH46	(228R/320R) * (GVDD-VGS) + VGS
101111	VRH47	(226R/320R) * (GVDD-VGS) + VGS
110000	VRH48	(224R/320R) * (GVDD-VGS) + VGS
110001	VRH49	(222R/320R) * (GVDD-VGS) + VGS
110010	VRH50	(220R/320R) * (GVDD-VGS) + VGS
110011	VRH51	(218R/320R) * (GVDD-VGS) + VGS
110100	VRH52	(216R/320R) * (GVDD-VGS) + VGS
110101	VRH53	(214R/320R) * (GVDD-VGS) + VGS

Register Value RFP(N) [5:0]	Selected Voltage VTOP	Formula of VTOP
110110	VRH54	(212R/320R) * (GVDD-VGS) + VGS
110111	VRH55	(210R/320R) * (GVDD-VGS) + VGS
111000	VRH56	(208R/320R) * (GVDD-VGS) + VGS
111001	VRH57	(206R/320R) * (GVDD-VGS) + VGS
111010	VRH58	(204R/320R) * (GVDD-VGS) + VGS
111011	VRH59	(202R/320R) * (GVDD-VGS) + VGS
111100	VRH60	(200R/320R) * (GVDD-VGS) + VGS
111101	VRH61	(198R/320R) * (GVDD-VGS) + VGS
111110	VRH62	(196R/320R) * (GVDD-VGS) + VGS
111111	VRH63	(194R/320R) * (GVDD-VGS) + VGS

Table 44. Reference Adjustment

Register Value OSP(N) [5:0]	Selected Voltage VBOTTOM	Formula of VBOTTOM
000000	VRL0	(16R/320R) * (GVDD-VGS) + VGS
000001	VRL1	(18R/320R) * (GVDD-VGS) + VGS
000010	VRL2	(20R/320R) * (GVDD-VGS) + VGS
000011	VRL3	(22R/320R) * (GVDD-VGS) + VGS
000100	VRL4	(24R/320R) * (GVDD-VGS) + VGS
000101	VRL5	(26R/320R) * (GVDD-VGS) + VGS
000110	VRL6	(28R/320R) * (GVDD-VGS) + VGS
000111	VRL7	(30R/320R) * (GVDD-VGS) + VGS
001000	VRL8	(32R/320R) * (GVDD-VGS) + VGS
001001	VRL9	(34R/320R) * (GVDD-VGS) + VGS
001010	VRL10	(36R/320R) * (GVDD-VGS) + VGS
001011	VRL11	(38R/320R) * (GVDD-VGS) + VGS
001100	VRL12	(40R/320R) * (GVDD-VGS) + VGS
001101	VRL13	(42R/320R) * (GVDD-VGS) + VGS
001110	VRL14	(44R/320R) * (GVDD-VGS) + VGS
001111	VRL15	(46R/320R) * (GVDD-VGS) + VGS
010000	VRL16	(48R/320R) * (GVDD-VGS) + VGS
010001	VRL17	(50R/320R) * (GVDD-VGS) + VGS
010010	VRL18	(52R/320R) * (GVDD-VGS) + VGS
010011	VRL19	(54R/320R) * (GVDD-VGS) + VGS

Register Value OSP(N) [5:0]	Selected Voltage VBOTTOM	Formula of VBOTTOM
010100	VRL20	(56R/320R) * (GVDD-VGS) + VGS
010101	VRL21	(58R/320R) * (GVDD-VGS) + VGS
010110	VRL22	(60R/320R) * (GVDD-VGS) + VGS
010111	VRL23	(62R/320R) * (GVDD-VGS) + VGS
011000	VRL24	(64R/320R) * (GVDD-VGS) + VGS
011001	VRL25	(66R/320R) * (GVDD-VGS) + VGS
011010	VRL26	(68R/320R) * (GVDD-VGS) + VGS
011011	VRL27	(70R/320R) * (GVDD-VGS) + VGS
011100	VRL28	(72R/320R) * (GVDD-VGS) + VGS
011101	VRL29	(74R/320R) * (GVDD-VGS) + VGS
011110	VRL30	(76R/320R) * (GVDD-VGS) + VGS
011111	VRL31	(78R/320R) * (GVDD-VGS) + VGS
100000	VRL32	(80R/320R) * (GVDD-VGS) + VGS
100001	VRL33	(82R/320R) * (GVDD-VGS) + VGS
100010	VRL34	(84R/320R) * (GVDD-VGS) + VGS
100011	VRL35	(86R/320R) * (GVDD-VGS) + VGS
100100	VRL36	(88R/320R) * (GVDD-VGS) + VGS
100101	VRL37	(90R/320R) * (GVDD-VGS) + VGS
100110	VRL38	(92R/320R) * (GVDD-VGS) + VGS
100111	VRL39	(94R/320R) * (GVDD-VGS) + VGS
101000	VRL40	(96R/320R) * (GVDD-VGS) + VGS
101001	VRL41	(98R/320R) * (GVDD-VGS) + VGS
101010	VRL42	(100R/320R) * (GVDD-VGS) + VGS
101011	VRL43	(102R/320R) * (GVDD-VGS) + VGS
101100	VRL44	(104R/320R) * (GVDD-VGS) + VGS
101101	VRL45	(106R/320R) * (GVDD-VGS) + VGS
101110	VRL46	(108R/320R) * (GVDD-VGS) + VGS
101111	VRL47	(110R/320R) * (GVDD-VGS) + VGS
110000	VRL48	(112R/320R) * (GVDD-VGS) + VGS
110001	VRL49	(114R/320R) * (GVDD-VGS) + VGS
110010	VRL50	(116R/320R) * (GVDD-VGS) + VGS
110011	VRL51	(118R/320R) * (GVDD-VGS) + VGS

Register Value OSP(N) [5:0]	Selected Voltage VBOTTOM	Formula of VBOTTOM
110100	VRL52	(120R/320R) * (GVDD-VGS) + VGS
110101	VRL53	(122R/320R) * (GVDD-VGS) + VGS
110110	VRL54	(124R/320R) * (GVDD-VGS) + VGS
110111	VRL55	(126R/320R) * (GVDD-VGS) + VGS
111000	VRL56	(128R/320R) * (GVDD-VGS) + VGS
111001	VRL57	(130R/320R) * (GVDD-VGS) + VGS
111010	VRL58	(132R/320R) * (GVDD-VGS) + VGS
111011	VRL59	(134R/320R) * (GVDD-VGS) + VGS
111100	VRL60	(136R/320R) * (GVDD-VGS) + VGS
111101	VRL61	(138R/320R) * (GVDD-VGS) + VGS
111110	VRL62	(140R/320R) * (GVDD-VGS) + VGS
111111	VRL63	(142R/320R) * (GVDD-VGS) + VGS

4.2.5.2. Resistor ladder network 2 / selector

In the 64-to-1 selector, the voltage level must be selected by the given ladder resistance and the micro-adjustment register and output the nine types of the reference voltage, VIN1 to VIN9.

Following figure explains the relationship between the micro-adjustment register and the selected voltage

Table 45. Relationship Between Micro-Adjustment Register and Selected Voltage

Register Value	Selected Voltage								
PKP(N) [5:0]	VINP(N) 1	VINP(N) 2	VINP(N) 3	VINP(N) 4	VINP(N) 5	VINP(N) 6	VINP(N) 7	VINP(N) 8	VINP(N) 9
000000	VRC0	VRC10	VRC16	VRC26	VRC48	VRC143	VRC150	VRC154	VRC158
000001	VRC1	VRC11	VRC17	VRC27	VRC49	VRC142	VRC149	VRC153	VRC157
000010	VRC2	VRC12	VRC18	VRC28	VRC50	VRC141	VRC148	VRC152	VRC156
000011	VRC3	VRC13	VRC19	VRC29	VRC51	VRC140	VRC147	VRC151	VRC155
000100	VRC4	VRC14	VRC20	VRC30	VRC52	VRC139	VRC146	VRC150	VRC154
000101	VRC5	VRC15	VRC21	VRC31	VRC53	VRC138	VRC145	VRC149	VRC153
000110	VRC6	VRC16	VRC22	VRC32	VRC54	VRC137	VRC144	VRC148	VRC152
000111	VRC7	VRC17	VRC23	VRC33	VRC55	VRC136	VRC143	VRC147	VRC151
001000	VRC8	VRC18	VRC24	VRC34	VRC56	VRC135	VRC142	VRC146	VRC150
001001	VRC9	VRC19	VRC25	VRC35	VRC57	VRC134	VRC141	VRC145	VRC149
001010	VRC10	VRC20	VRC26	VRC36	VRC58	VRC133	VRC140	VRC144	VRC148

Register Value	Selected Voltage								
PKP(N) [5:0]	VINP(N) 1	VINP(N) 2	VINP(N) 3	VINP(N) 4	VINP(N) 5	VINP(N) 6	VINP(N) 7	VINP(N) 8	VINP(N) 9
001011	VRC11	VRC21	VRC27	VRC37	VRC59	VRC132	VRC139	VRC143	VRC147
001100	VRC12	VRC22	VRC28	VRC38	VRC60	VRC131	VRC138	VRC142	VRC146
001101	VRC13	VRC23	VRC29	VRC39	VRC61	VRC130	VRC137	VRC141	VRC145
001110	VRC14	VRC24	VRC30	VRC40	VRC62	VRC129	VRC136	VRC140	VRC144
001111	VRC15	VRC25	VRC31	VRC41	VRC63	VRC128	VRC135	VRC139	VRC143
010000	VRC16	VRC26	VRC32	VRC42	VRC64	VRC127	VRC134	VRC138	VRC142
010001	VRC17	VRC27	VRC33	VRC43	VRC65	VRC126	VRC133	VRC137	VRC141
010010	VRC18	VRC28	VRC34	VRC44	VRC66	VRC125	VRC132	VRC136	VRC140
010011	VRC19	VRC29	VRC35	VRC45	VRC67	VRC124	VRC131	VRC135	VRC139
010100	VRC20	VRC30	VRC36	VRC46	VRC68	VRC123	VRC130	VRC134	VRC138
010101	VRC21	VRC31	VRC37	VRC47	VRC69	VRC122	VRC129	VRC133	VRC137
010110	VRC22	VRC32	VRC38	VRC48	VRC70	VRC121	VRC128	VRC132	VRC136
010111	VRC23	VRC33	VRC39	VRC49	VRC71	VRC120	VRC127	VRC131	VRC135
011000	VRC24	VRC34	VRC40	VRC50	VRC72	VRC119	VRC126	VRC130	VRC134
011001	VRC25	VRC35	VRC41	VRC51	VRC73	VRC118	VRC125	VRC129	VRC133
011010	VRC26	VRC36	VRC42	VRC52	VRC74	VRC117	VRC124	VRC128	VRC132
011011	VRC27	VRC37	VRC43	VRC53	VRC75	VRC116	VRC123	VRC127	VRC131
011100	VRC28	VRC38	VRC44	VRC54	VRC76	VRC115	VRC122	VRC126	VRC130
011101	VRC29	VRC39	VRC45	VRC55	VRC77	VRC114	VRC121	VRC125	VRC129
011110	VRC30	VRC40	VRC46	VRC56	VRC78	VRC113	VRC120	VRC124	VRC128
011111	VRC31	VRC41	VRC47	VRC57	VRC79	VRC112	VRC119	VRC123	VRC127
100000	VRC32	VRC42	VRC48	VRC58	VRC80	VRC111	VRC118	VRC122	VRC126
100001	VRC33	VRC43	VRC49	VRC59	VRC81	VRC110	VRC117	VRC121	VRC125
100010	VRC34	VRC44	VRC50	VRC60	VRC82	VRC109	VRC116	VRC120	VRC124
100011	VRC35	VRC45	VRC51	VRC61	VRC83	VRC108	VRC115	VRC119	VRC123
100100	VRC36	VRC46	VRC52	VRC62	VRC84	VRC107	VRC114	VRC118	VRC122
100101	VRC37	VRC47	VRC53	VRC63	VRC85	VRC106	VRC113	VRC117	VRC121
100110	VRC38	VRC48	VRC54	VRC64	VRC86	VRC105	VRC112	VRC116	VRC120
100111	VRC39	VRC49	VRC55	VRC65	VRC87	VRC104	VRC111	VRC115	VRC119

Register Value	Selected Voltage								
PKP(N) [5:0]	VINP(N) 1	VINP(N) 2	VINP(N) 3	VINP(N) 4	VINP(N) 5	VINP(N) 6	VINP(N) 7	VINP(N) 8	VINP(N) 9
101000	VRC40	VRC50	VRC56	VRC66	VRC88	VRC103	VRC110	VRC114	VRC118
101001	VRC41	VRC51	VRC57	VRC67	VRC89	VRC102	VRC109	VRC113	VRC117
101010	VRC42	VRC52	VRC58	VRC68	VRC90	VRC101	VRC108	VRC112	VRC116
101011	VRC43	VRC53	VRC59	VRC69	VRC91	VRC100	VRC107	VRC111	VRC115
101100	VRC44	VRC54	VRC60	VRC70	VRC92	VRC99	VRC106	VRC110	VRC114
101101	VRC45	VRC55	VRC61	VRC71	VRC93	VRC98	VRC105	VRC109	VRC113
101110	VRC46	VRC56	VRC62	VRC72	VRC94	VRC97	VRC104	VRC108	VRC112
101111	VRC47	VRC57	VRC63	VRC73	VRC95	VRC96	VRC103	VRC107	VRC111
110000	VRC48	VRC58	VRC64	VRC74	VRC96	VRC95	VRC102	VRC106	VRC110
110001	VRC49	VRC59	VRC65	VRC75	VRC97	VRC94	VRC101	VRC105	VRC109
110010	VRC50	VRC60	VRC66	VRC76	VRC98	VRC93	VRC100	VRC104	VRC108
110011	VRC51	VRC61	VRC67	VRC77	VRC99	VRC92	VRC99	VRC103	VRC107
110100	VRC52	VRC62	VRC68	VRC78	VRC100	VRC91	VRC98	VRC102	VRC106
110101	VRC53	VRC63	VRC69	VRC79	VRC101	VRC90	VRC97	VRC101	VRC105
110110	VRC54	VRC64	VRC70	VRC80	VRC102	VRC89	VRC96	VRC100	VRC104
110111	VRC55	VRC65	VRC71	VRC81	VRC103	VRC88	VRC95	VRC99	VRC103
111000	VRC56	VRC66	VRC72	VRC82	VRC104	VRC87	VRC94	VRC98	VRC102
111001	VRC57	VRC67	VRC73	VRC83	VRC105	VRC86	VRC93	VRC97	VRC101
111010	VRC58	VRC68	VRC74	VRC84	VRC106	VRC85	VRC92	VRC96	VRC100

Table 46. Relationship Between Micro-Adjustment Register and Selected Voltage(Continued)

Register Value	Selected Voltage								
PKP(N) [5:0]	VINP(N) 1	VINP(N) 2	VINP(N) 3	VINP(N) 4	VINP(N) 5	VINP(N) 6	VINP(N) 7	VINP(N) 8	VINP(N) 9
111011	VRC59	VRC69	VRC75	VRC85	VRC107	VRC84	VRC91	VRC95	VRC99
111100	VRC60	VRC70	VRC76	VRC86	VRC108	VRC83	VRC90	VRC94	VRC98
111101	VRC61	VRC71	VRC77	VRC87	VRC109	VRC82	VRC89	VRC93	VRC97
111110	VRC62	VRC72	VRC78	VRC88	VRC110	VRC81	VRC88	VRC92	VRC96
111111	VRC63	VRC73	VRC79	VRC89	VRC111	VRC80	VRC87	VRC91	VRC95

The grayscale levels are determined by the following formulas listed in the following equations.
Negative gamma voltages are calculated with the same equation of positive gamma voltages, but the gray scale is symmetric, which means negative V<0> is equal to positive V<63>. Rt and Ra in the below equations are determined by GL[1:0] Registers as follows.

GLP/N[1:0]=00, Rt = 154R, Ra=R
GLP/N [1:0]=01, Rt = 204R, Ra=R+50R
GLP/N [1:0]=10, Rt = 204R, Ra=R
GLP/N [1:0]=11, Rt = 254R, Ra=R+50R

4.2.6. GRAYSCALE LEVELS

Table 47. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC0	(153.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000000”	VNP1
VRC1	(153Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000001”	
VRC2	(152.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000010”	
VRC3	(152Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000011”	
VRC4	(151.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000100”	
VRC5	(151Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000101”	
VRC6	(150Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000110”	
VRC7	(149Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “000111”	
VRC8	(148Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001000”	
VRC9	(147Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001001”	
VRC10	(146Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001010”	
VRC11	(145Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001011”	
VRC12	(144Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001100”	
VRC13	(143Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001101”	
VRC14	(142Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001110”	
VRC15	(141Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “001111”	
VRC16	(140Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010000”	
VRC17	(139Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010001”	
VRC18	(138Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010010”	
VRC19	(137Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010011”	
VRC20	(136Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010100”	
VRC21	(135Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010101”	
VRC22	(134Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010110”	
VRC23	(133Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “010111”	
VRC24	(132Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011000”	
VRC25	(131Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011001”	
VRC26	(130Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011010”	
VRC27	(129Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011011”	
VRC28	(128Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011100”	
VRC29	(127Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011101”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC30	(126Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011110”	
VRC31	(125Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “011111”	
VRC32	(124Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100000”	
VRC33	(123Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100001”	
VRC34	(122Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100010”	
VRC35	(121Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100011”	

Table 48. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC36	(120Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100100”	VINP1
VRC37	(119Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100101”	
VRC38	(118Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100110”	
VRC39	(117Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “100111”	
VRC40	(116Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101000”	
VRC41	(115Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101001”	
VRC42	(114Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101010”	
VRC43	(113Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101011”	
VRC44	(112Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101100”	
VRC45	(111Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101101”	
VRC46	(110Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101110”	
VRC47	(109Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “101111”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110000”	
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110001”	
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110010”	
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110011”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110100”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110101”	
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110110”	
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “110111”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111000”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111001”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111010”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111011”	
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111100”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111101”	
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111110”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP0[5:0] = “111111”	
VRC10	(146Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000000”	VINP2
VRC11	(145Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000001”	
VRC12	(144Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000010”	
VRC13	(143Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000011”	
VRC14	(142Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000100”	
VRC15	(141Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000101”	
VRC16	(140Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000110”	
VRC17	(139Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “000111”	

Table 49. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC18	(138Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001000”	VINP2
VRC19	(137Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001001”	
VRC20	(136Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001010”	
VRC21	(135Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001011”	
VRC22	(134Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001100”	
VRC23	(133Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001101”	
VRC24	(132Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001110”	
VRC25	(131Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “001111”	
VRC26	(130Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010000”	
VRC27	(129Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010001”	
VRC28	(128Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010010”	
VRC29	(127Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010011”	
VRC30	(126Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010100”	
VRC31	(125Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010101”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC32	(124Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010110”	
VRC33	(123Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “010111”	
VRC34	(122Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011000”	
VRC35	(121Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011001”	
VRC36	(120Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011010”	
VRC37	(119Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011011”	
VRC38	(118Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011100”	
VRC39	(117Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011101”	
VRC40	(116Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011110”	
VRC41	(115Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “011111”	
VRC42	(114Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100000”	
VRC43	(113Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100001”	
VRC44	(112Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100010”	
VRC45	(111Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100011”	
VRC46	(110Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100100”	
VRC47	(109Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100101”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100110”	
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “100111”	
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101000”	
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101001”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101010”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101011”	

Table 50. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101100”	VINP2
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101101”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101110”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “101111”	
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110000”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110001”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110010”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110011”	
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110100”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110101”	
VRC64	(92Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110110”	
VRC65	(91Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “110111”	
VRC66	(90Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111000”	
VRC67	(89Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111001”	
VRC68	(88Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111010”	
VRC69	(87Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111011”	
VRC70	(86Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111100”	
VRC71	(85Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111101”	
VRC72	(84Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111110”	
VRC73	(83Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP1[5:0] = “111111”	
VRC16	(140Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000000”	VINP3
VRC17	(139Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000001”	
VRC18	(138Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000010”	
VRC19	(137Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000011”	
VRC20	(136Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000100”	
VRC21	(135Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000101”	
VRC22	(134Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000110”	
VRC23	(133Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “000111”	
VRC24	(132Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001000”	
VRC25	(131Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001001”	
VRC26	(130Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001010”	
VRC27	(129Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001011”	
VRC28	(128Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001100”	
VRC29	(127Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001101”	
VRC30	(126Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001110”	
VRC31	(125Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “001111”	

Table 51. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC32	(124Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010000”	VINP3
VRC33	(123Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010001”	
VRC34	(122Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010010”	
VRC35	(121Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010011”	
VRC36	(120Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010100”	
VRC37	(119Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010101”	
VRC38	(118Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010110”	
VRC39	(117Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “010111”	
VRC40	(116Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011000”	
VRC41	(115Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011001”	
VRC42	(114Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011010”	
VRC43	(113Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011011”	
VRC44	(112Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011100”	
VRC45	(111Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011101”	
VRC46	(110Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011110”	
VRC47	(109Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “011111”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100000”	
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100001”	
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100010”	
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100011”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100100”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100101”	
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100110”	
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “100111”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101000”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101001”	
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101010”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101011”	
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101100”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101101”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101110”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “101111”	
VRC64	(92Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110000”	
VRC65	(91Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110001”	
VRC66	(90Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110010”	
VRC67	(89Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110011”	

Table 52. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC68	(88Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110100”	VINP3
VRC69	(87Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110101”	
VRC70	(86Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110110”	
VRC71	(85Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “110111”	
VRC72	(84Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111000”	
VRC73	(83Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111001”	
VRC74	(82Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111010”	
VRC75	(81Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111011”	
VRC76	(80Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111100”	
VRC77	(79Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111101”	
VRC78	(78Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111110”	
VRC79	(77Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP2[5:0] = “111111”	
VRC26	(130Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000000”	VINP4
VRC27	(129Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000001”	
VRC28	(128Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000010”	
VRC29	(127Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000011”	
VRC30	(126Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000100”	
VRC31	(125Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000101”	
VRC32	(124Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000110”	
VRC33	(123Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “000111”	
VRC34	(122Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001000”	
VRC35	(121Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001001”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC36	(120Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001010”	
VRC37	(119Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001011”	
VRC38	(118Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001100”	
VRC39	(117Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001101”	
VRC40	(116Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001110”	
VRC41	(115Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “001111”	
VRC42	(114Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010000”	
VRC43	(113Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010001”	
VRC44	(112Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010010”	
VRC45	(111Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010011”	
VRC46	(110Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010100”	
VRC47	(109Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010101”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010110”	
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “010111”	

Table 53. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011000”	VINP4
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011001”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011010”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011011”	
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011100”	
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011101”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011110”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “011111”	
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100000”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100001”	
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100010”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100011”	
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100100”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100101”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC64	(92Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100110”	
VRC65	(91Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “100111”	
VRC66	(90Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101000”	
VRC67	(89Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101001”	
VRC68	(88Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101010”	
VRC69	(87Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101011”	
VRC70	(86Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101100”	
VRC71	(85Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101101”	
VRC72	(84Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101110”	
VRC73	(83Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “101111”	
VRC74	(82Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110000”	
VRC75	(81Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110001”	
VRC76	(80Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110010”	
VRC77	(79Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110011”	
VRC78	(78Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110100”	
VRC79	(77Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110101”	
VRC80	(76Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110110”	
VRC81	(75Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “110111”	
VRC82	(74Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111000”	
VRC83	(73Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111001”	
VRC84	(72Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111010”	
VRC85	(71Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111011”	

Table 54. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference voltage
VRC86	(70Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111100”	VINP4
VRC87	(69Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111101”	
VRC88	(68Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111110”	
VRC89	(67Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP3[5:0] = “111111”	
VRC48	(108Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000000”	VINP5
VRC49	(107Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000001”	

Pads	Formula	Micro-Adjusting Register Value	Reference voltage
VRC50	(106Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000010”	
VRC51	(105Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000011”	
VRC52	(104Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000100”	
VRC53	(103Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000101”	
VRC54	(102Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000110”	
VRC55	(101Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “000111”	
VRC56	(100Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001000”	
VRC57	(99Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001001”	
VRC58	(98Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001010”	
VRC59	(97Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001011”	
VRC60	(96Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001100”	
VRC61	(95Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001101”	
VRC62	(94Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001110”	
VRC63	(93Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “001111”	
VRC64	(92Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010000”	
VRC65	(91Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010001”	
VRC66	(90Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010010”	
VRC67	(89Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010011”	
VRC68	(88Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010100”	
VRC69	(87Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010101”	
VRC70	(86Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010110”	
VRC71	(85Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “010111”	
VRC72	(84Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011000”	
VRC73	(83Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011001”	
VRC74	(82Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011010”	
VRC75	(81Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011011”	
VRC76	(80Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011100”	
VRC77	(79Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011101”	
VRC78	(78Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011110”	
VRC79	(77Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “011111”	

Table 55. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC80	(76Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100000”	VINP5
VRC81	(75Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100001”	
VRC82	(74Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100010”	
VRC83	(73Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100011”	
VRC84	(72Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100100”	
VRC85	(71Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100101”	
VRC86	(70Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100110”	
VRC87	(69Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “100111”	
VRC88	(68Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101000”	
VRC89	(67Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101001”	
VRC90	(66Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101010”	
VRC91	(65Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101011”	
VRC92	(64Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101100”	
VRC93	(63Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101101”	
VRC94	(62Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101110”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “101111”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110000”	
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110001”	
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110010”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110011”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110100”	
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110101”	
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110110”	
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “110111”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111000”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111001”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111010”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111011”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111100”	
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111101”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111110”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP4[5:0] = “111111”	
VRC143	(13Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000000”	VINP6
VRC142	(14Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000001”	
VRC141	(15Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000010”	
VRC140	(16Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000011”	

Table 56. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC139	(17Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000100”	VINP6
VRC138	(18Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000101”	
VRC137	(19Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000110”	
VRC136	(20Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “000111”	
VRC135	(21Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001000”	
VRC134	(22Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001001”	
VRC133	(23Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001010”	
VRC132	(24Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001011”	
VRC131	(25Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001100”	
VRC130	(26Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001101”	
VRC129	(27Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001110”	
VRC128	(28Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “001111”	
VRC127	(29Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010000”	
VRC126	(30Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010001”	
VRC125	(31Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010010”	
VRC124	(32Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010011”	
VRC123	(33Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010100”	
VRC122	(34Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010101”	
VRC121	(35Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010110”	
VRC120	(36Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “010111”	
VRC119	(37Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011000”	
VRC118	(38Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011001”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC117	(39Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011010”	
VRC116	(40Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011011”	
VRC115	(41Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011100”	
VRC114	(42Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011101”	
VRC113	(43Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011110”	
VRC112	(44Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “011111”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100000”	
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100001”	
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100010”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100011”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100100”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100101”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100110”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “100111”	

Table 57. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101000”	VINP6
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101001”	
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101010”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101011”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101100”	
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101101”	
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101110”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “101111”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110000”	
VRC94	(62Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110001”	
VRC93	(63Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110010”	
VRC92	(64Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110011”	
VRC91	(65Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110100”	
VRC90	(66Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110101”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC89	(67Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110110”	
VRC88	(68Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “110111”	
VRC87	(69Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111000”	
VRC86	(70Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111001”	
VRC85	(71Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111010”	
VRC84	(72Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111011”	
VRC83	(73Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111100”	
VRC82	(74Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111101”	
VRC81	(75Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111110”	
VRC80	(76Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP5[5:0] = “111111”	
VRC150	(6Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000000”	VINP7
VRC149	(7Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000001”	
VRC148	(8Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000010”	
VRC147	(9Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000011”	
VRC146	(10Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000100”	
VRC145	(11Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000101”	
VRC144	(12Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000110”	
VRC143	(13Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “000111”	
VRC142	(14Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001000”	
VRC141	(15Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001001”	
VRC140	(16Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001010”	
VRC139	(17Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001011”	

Table 58. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC138	(18Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001100”	VINP7
VRC137	(19Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001101”	
VRC136	(20Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001110”	
VRC135	(21Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “001111”	
VRC134	(22Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010000”	
VRC133	(23Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010001”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC132	(24Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010010”	
VRC131	(25Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010011”	
VRC130	(26Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010100”	
VRC129	(27Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010101”	
VRC128	(28Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010110”	
VRC127	(29Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “010111”	
VRC126	(30Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011000”	
VRC125	(31Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011001”	
VRC124	(32Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011010”	
VRC123	(33Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011011”	
VRC122	(34Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011100”	
VRC121	(35Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011101”	
VRC120	(36Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011110”	
VRC119	(37Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “011111”	
VRC118	(38Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100000”	
VRC117	(39Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100001”	
VRC116	(40Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100010”	
VRC115	(41Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100011”	
VRC114	(42Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100100”	
VRC113	(43Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100101”	
VRC112	(44Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100110”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “100111”	
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101000”	
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101001”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101010”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101011”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101100”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101101”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101110”	
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “101111”	

Table 59. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110000”	VINP7
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110001”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110010”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110011”	
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110100”	
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110101”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110110”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “110111”	
VRC94	(62Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111000”	
VRC93	(63Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111001”	
VRC92	(64Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111010”	
VRC91	(65Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111011”	
VRC90	(66Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111100”	
VRC89	(67Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111101”	
VRC88	(68Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111110”	
VRC87	(69Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP6[5:0] = “111111”	
VRC154	(2.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000000”	VINP8
VRC153	(3Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000001”	
VRC152	(4Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000010”	
VRC151	(5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000011”	
VRC150	(6Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000100”	
VRC149	(7Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000101”	
VRC148	(8Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000110”	
VRC147	(9Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “000111”	
VRC146	(10Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001000”	
VRC145	(11Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001001”	
VRC144	(12Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001010”	
VRC143	(13Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001011”	
VRC142	(14Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001100”	
VRC141	(15Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001101”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC140	(16Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001110”	
VRC139	(17Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “001111”	
VRC138	(18Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010000”	
VRC137	(19Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010001”	
VRC136	(20Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010010”	
VRC135	(21Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010011”	

Table 60. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC134	(22Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010100”	VINP8
VRC133	(23Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010101”	
VRC132	(24Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010110”	
VRC131	(25Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “010111”	
VRC130	(26Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011000”	
VRC129	(27Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011001”	
VRC128	(28Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011010”	
VRC127	(29Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011011”	
VRC126	(30Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011100”	
VRC125	(31Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011101”	
VRC124	(32Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011110”	
VRC123	(33Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “011111”	
VRC122	(34Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100000”	
VRC121	(35Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100001”	
VRC120	(36Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100010”	
VRC119	(37Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100011”	
VRC118	(38Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100100”	
VRC117	(39Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100101”	
VRC116	(40Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100110”	
VRC115	(41Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “100111”	
VRC114	(42Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101000”	
VRC113	(43Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101001”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC112	(44Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101010”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101011”	
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101100”	
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101101”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101110”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “101111”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110000”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110001”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110010”	
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110011”	
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110100”	
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110101”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110110”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “110111”	

Table 61. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111000”	VINP8
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111001”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111010”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111011”	
VRC94	(62Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111100”	
VRC93	(63Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111101”	
VRC92	(64Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111110”	
VRC91	(65Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP7[5:0] = “111111”	
VRC158	(0.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000000”	VINP9
VRC157	(1Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000001”	
VRC156	(1.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000010”	
VRC155	(2Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000011”	
VRC154	(2.5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000100”	
VRC153	(3Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000101”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC152	(4Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000110”	
VRC151	(5Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “000111”	
VRC150	(6Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001000”	
VRC149	(7Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001001”	
VRC148	(8Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001010”	
VRC147	(9Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001011”	
VRC146	(10Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001100”	
VRC145	(11Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001101”	
VRC144	(12Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001110”	
VRC143	(13Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “001111”	
VRC142	(14Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010000”	
VRC141	(15Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010001”	
VRC140	(16Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010010”	
VRC139	(17Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010011”	
VRC138	(18Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010100”	
VRC137	(19Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010101”	
VRC136	(20Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010110”	
VRC135	(21Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “010111”	
VRC134	(22Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011000”	
VRC133	(23Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011001”	
VRC132	(24Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011010”	
VRC131	(25Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011011”	

Table 62. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1 (Continued)

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC130	(26Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011100”	VINP9
VRC129	(27Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011101”	
VRC128	(28Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011110”	
VRC127	(29Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “011111”	
VRC126	(30Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100000”	
VRC125	(31Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100001”	

Pads	Formula	Micro-Adjusting Register Value	Reference Voltage
VRC124	(32Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100010”	
VRC123	(33Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100011”	
VRC122	(34Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100100”	
VRC121	(35Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100101”	
VRC120	(36Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100110”	
VRC119	(37Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “100111”	
VRC118	(38Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101000”	
VRC117	(39Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101001”	
VRC116	(40Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101010”	
VRC115	(41Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101011”	
VRC114	(42Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101100”	
VRC113	(43Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101101”	
VRC112	(44Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101110”	
VRC111	(45Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “101111”	
VRC110	(46Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110000”	
VRC109	(47Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110001”	
VRC108	(48Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110010”	
VRC107	(49Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110011”	
VRC106	(50Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110100”	
VRC105	(51Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110101”	
VRC104	(52Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110110”	
VRC103	(53Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “110111”	
VRC102	(54Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111000”	
VRC101	(55Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111001”	
VRC100	(56Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111010”	
VRC99	(57Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111011”	
VRC98	(58Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111100”	
VRC97	(59Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111101”	
VRC96	(60Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111110”	
VRC95	(61Ra/Rt) * (VINP0 – VINP10) + VINP10	PKP8[5:0] = “111111”	

Table 63. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 2

Grayscale Voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	VC-(VC-V43) * (0.5/11.5)
V1	VINP1	V33	VC-(VC-V43) * (1.25/11.5)
V2	V1-(V1-V4) * (6/12)	V34	VC-(VC-V43) * (2.25/11.5)
V3	V1-(V1-V4) * (10/12)	V35	VC-(VC-V43) * (3/11.5)
V4	VINP2	V36	VC-(VC-V43) * (4/11.5)
V5	V4-(V4-V8) * (2.5/7.5)	V37	VC-(VC-V43) * (5/11.5)
V6	V4-(V4-V8) * (4.5/7.5)	V38	VC-(VC-V43) * (6/11.5)
V7	V4-(V4-V8) * (6/7.5)	V39	VC-(VC-V43) * (7/11.5)
V8	VINP3	V40	VC-(VC-V43) * (8/11.5)
V9	V8-(V8-V20) * (1.5/13.25)	V41	VC-(VC-V43) * (9/11.5)
V10	V8-(V8-V20) * (3.5/13.25)	V42	VC-(VC-V43) * (10.5/11.5)
V11	V8-(V8-V20) * (4.5/13.25)	V43	VINP6
V12	V8-(V8-V20) * (5.5/13.25)	V44	V43-(V43-V55) * (1/17.5)
V13	V8-(V8-V20) * (6.75/13.25)	V45	V43-(V43-V55) * (2.5/17.5)
V14	V8-(V8-V20) * (7.75/13.25)	V46	V43-(V43-V55) * (3.75/17.5)
V15	V8-(V8-V20) * (8.75/13.25)	V47	V43-(V43-V55) * (4.75/17.5)
V16	V8-(V8-V20) * (9.75/13.25)	V48	V43-(V43-V55) * (6.5/17.5)
V17	V8-(V8-V20) * (10.75/13.25)	V49	V43-(V43-V55) * (7.5/17.5)
V18	V8-(V8-V20) * (11.75/13.25)	V50	V43-(V43-V55) * (9/17.5)
V19	V8-(V8-V20) * (12.75/13.25)	V51	V43-(V43-V55) * (10.5/17.5)
V20	VINP4	V52	V43-(V43-V55) * (12/17.5)
V21	V20-(V20-VC) * (1.5/12.25)	V53	V43-(V43-V55) * (13.5/17.5)
V22	V20-(V20-VC) * (2.5/12.25)	V54	V43-(V43-V55) * (15.5/17.5)
V23	V20-(V20-VC) * (3.75/12.25)	V55	VINP7
V24	V20-(V20-VC) * (4.75/12.25)	V56	V55-(V55-V59) * (2/9.5)
V25	V20-(V20-VC) * (5.75/12.25)	V57	V55-(V55-V59) * (4/9.5)
V26	V20-(V20-VC) * (6.75/12.25)	V58	V55-(V55-V59) * (6.5/9.5)
V27	V20-(V20-VC) * (7.75/12.25)	V59	VINP8
V28	V20-(V20-VC) * (8.75/12.25)	V60	V59-(V59-V62) * (3.5/11.5)
V29	V20-(V20-VC) * (9.75/12.25)	V61	V59-(V59-V62) * (6.5/11.5)

Grayscale Voltage	Formula	Grayscale voltage	Formula
V30	V20-(V20-VC) * (10.75/12.25)	V62	VINP9
V31	V20-(V20-VC) * (11.75/12.25)	V63	VINP10
VC	VINP5		

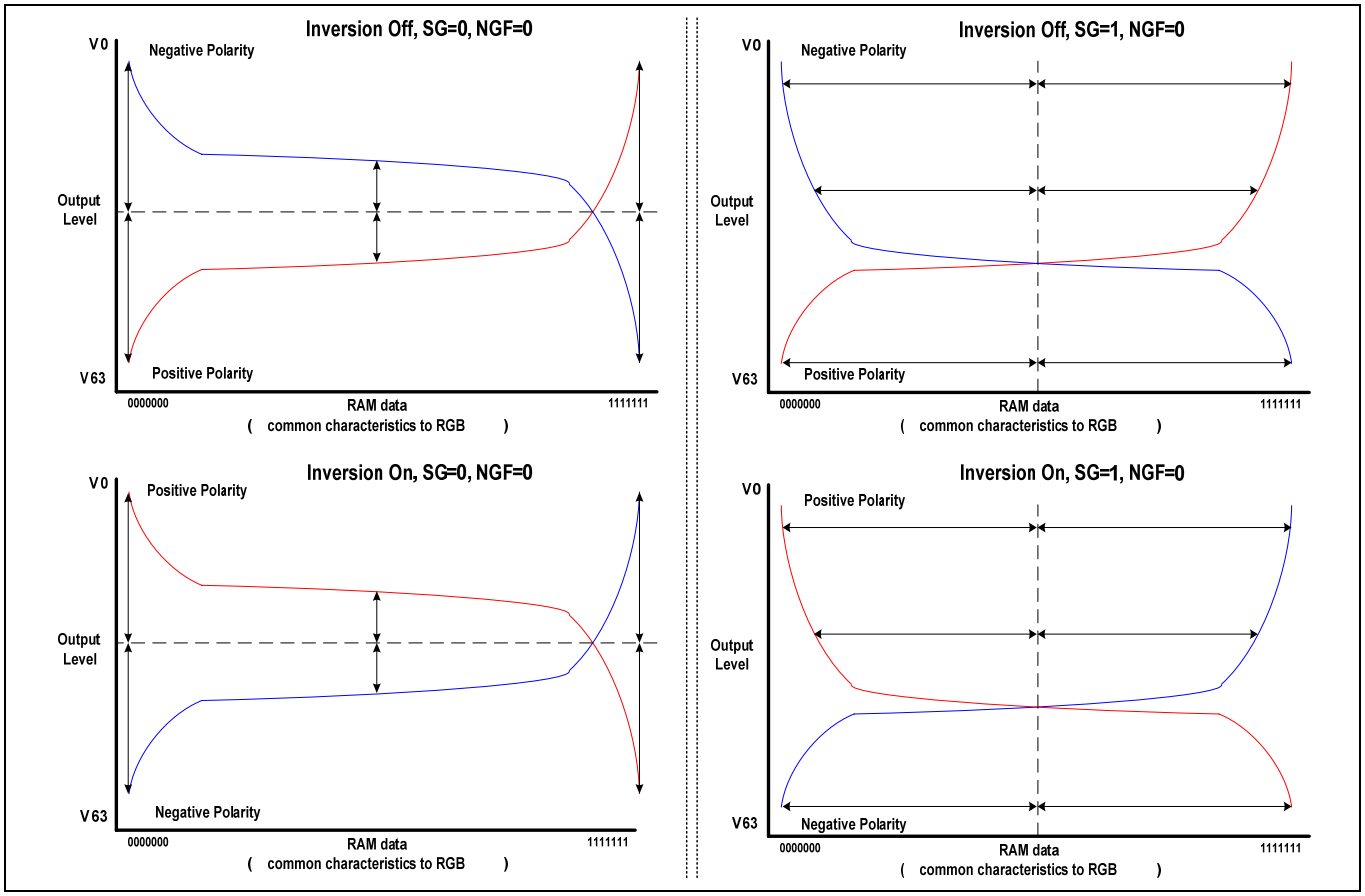
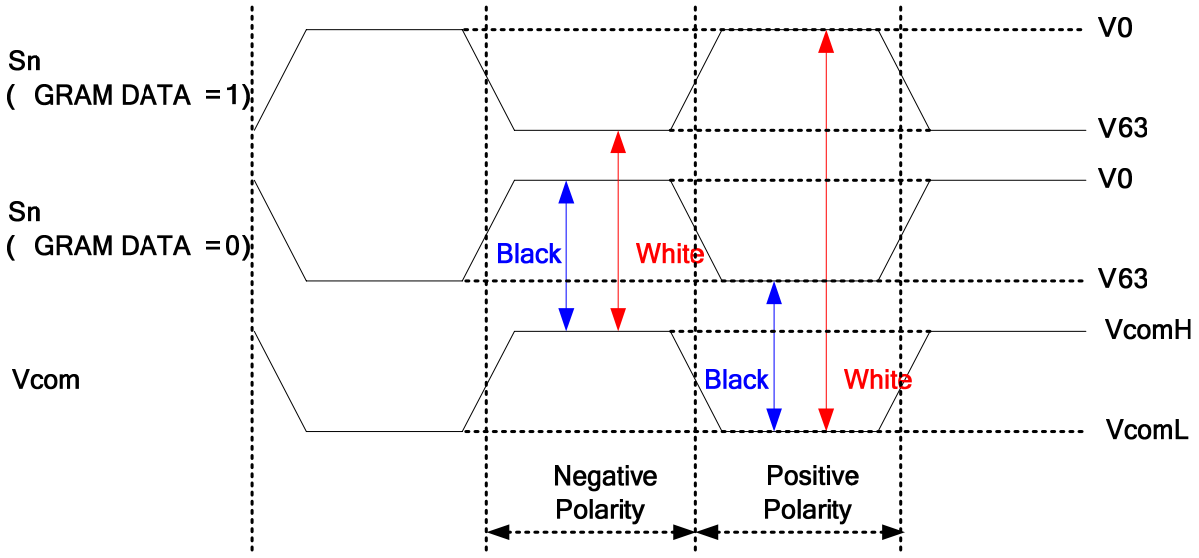
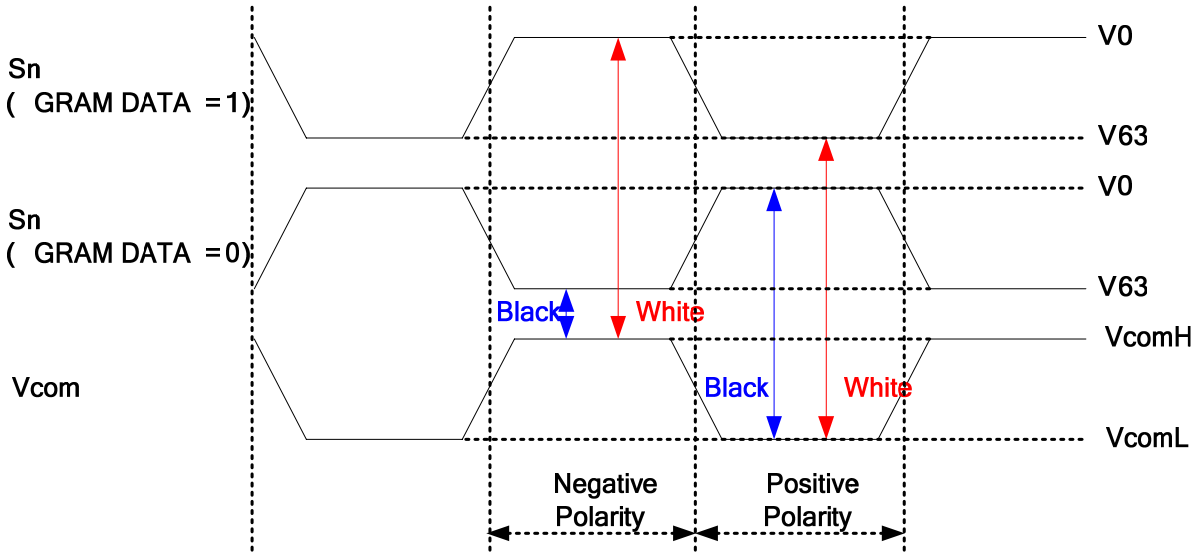


Figure69. Relationship Between RAM Data and Output Voltage



(a) For Normally Black Panel (Inversion Off)



(b) For Normally White Panel (Inversion On)

Figure70. Relationship Between Source Output and VCOM

4.3. DISPLAY DATA RAM

4.3.1. CONFIGURATION

S6D04H0 has an integrated 240x320x18-bit graphic type of static RAM. This memory allows storing on-chip a 240xRGBx320 image with 18-bit resolution. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.Memory to Display Address Mapping

4.3.1.1. When using 240RGB x 320 resolution

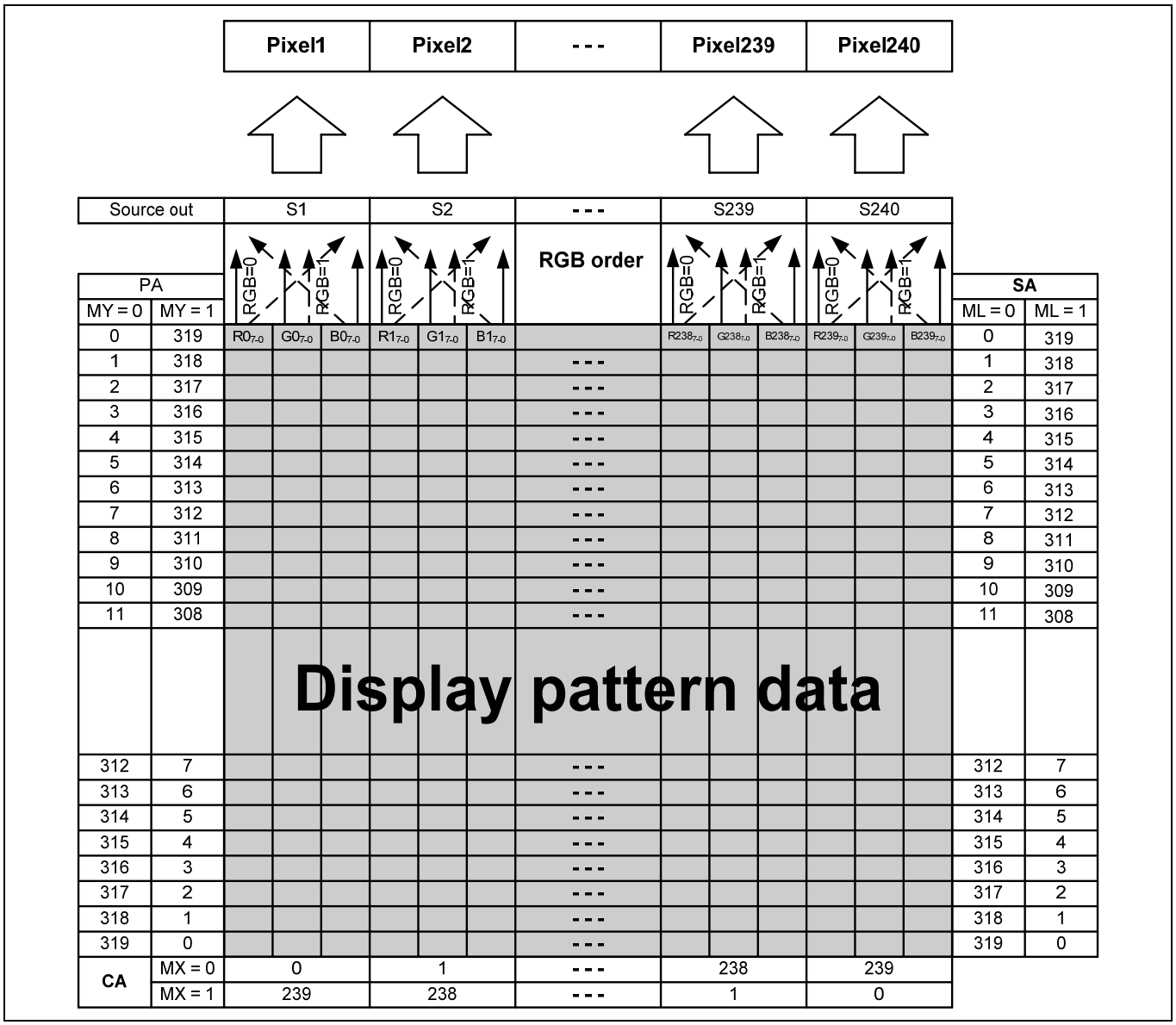


Figure71. When Using 240RGB x 320 Resolution

Note.

PA = Page Address,

CA = Column Address,

SA = Scan Address,

MX = Mirror X-axis (Column address direction parameter), B6 parameter of MADCTL command

MY = Mirror Y-axis (Page address direction parameter), B7 parameter of MADCTL command

ML = Scan direction parameter, B4 parameter of MADCTL command

RGB= Red, Green and Blue pixel position change, B3 parameter of MADCTL command

4.3.2. NORMAL DISPLAY ON OR PARTIAL MODE ON, VERTICAL SCROLL OFF

4.3.2.1. When using 240RGB x 320 resolution

In this mode, contents of the frame memory within an area where column pointer is 00h to EFh and page pointer is 000h to 13Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

1). Example for Normal Display On (B6 = B7 = B4 = '0' on MADCTL)

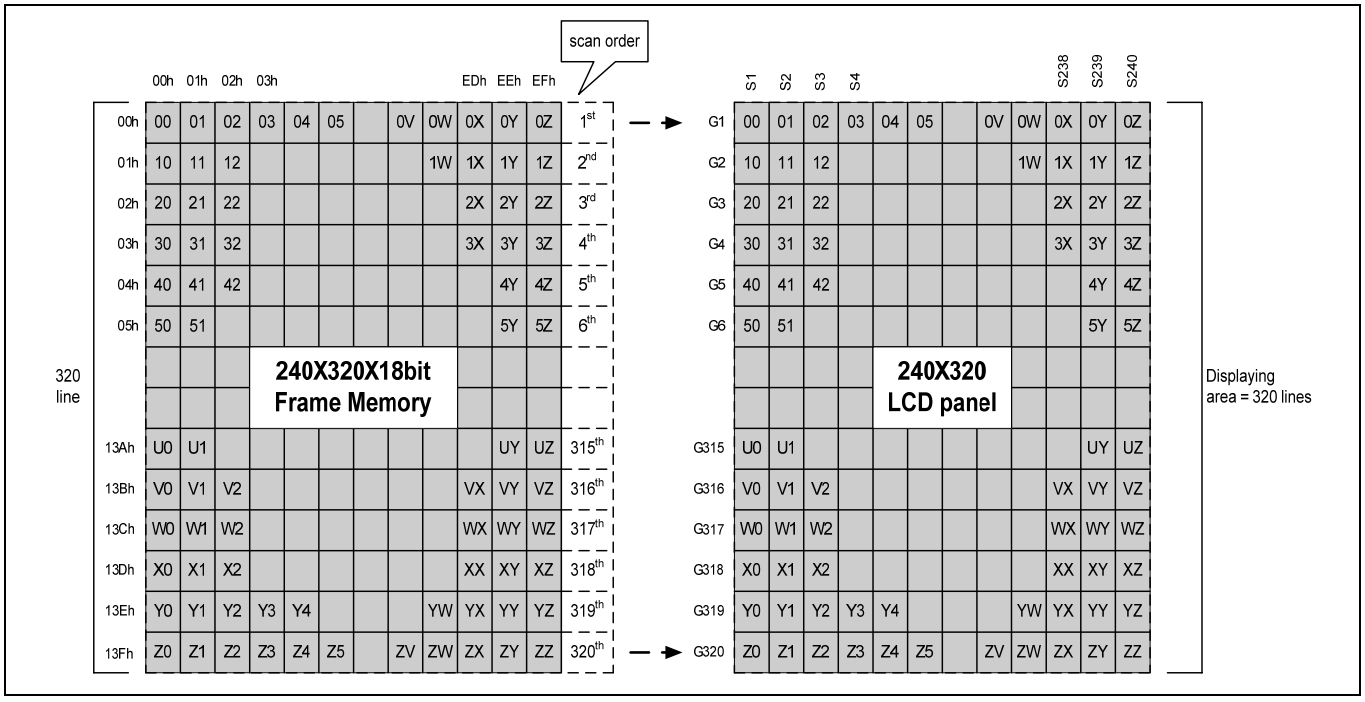


Figure72. Normal Display On (B6 = B7 = B4 = '0' On MADCTL)

2). Partial display on: SR [15:0] = 04h, ER [15:0] = 13Ch, madctl (B6 = B7 = B4 = '0')

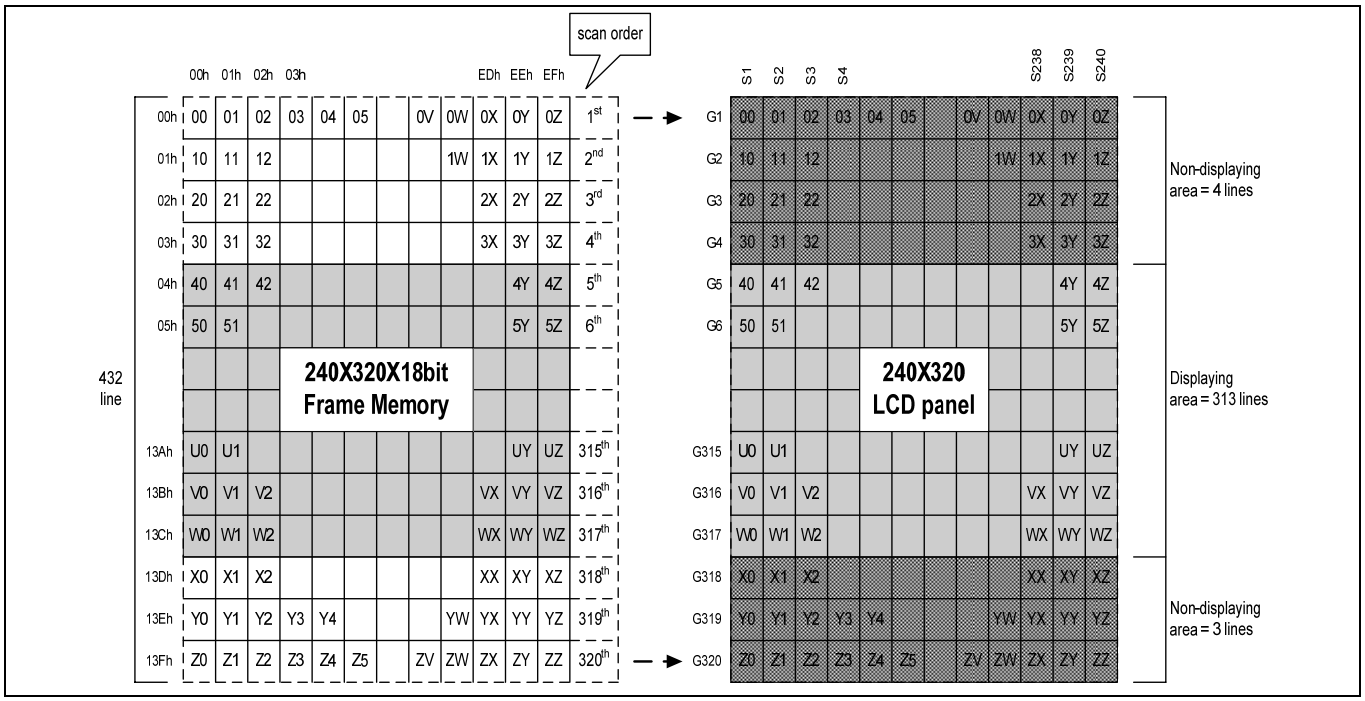
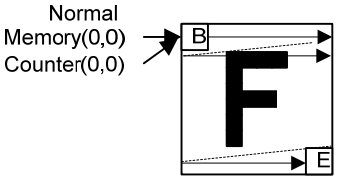
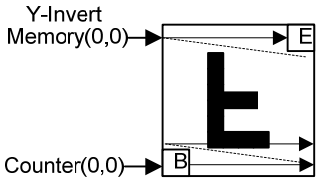
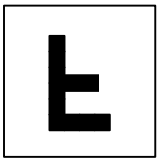
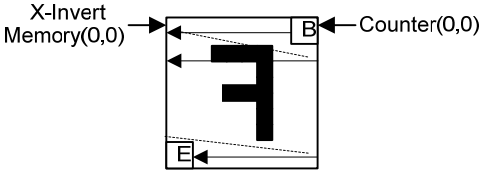
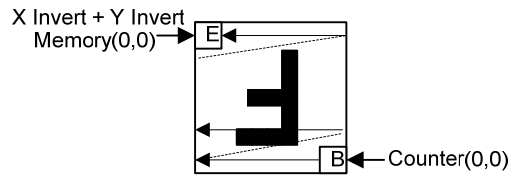
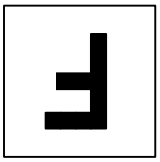
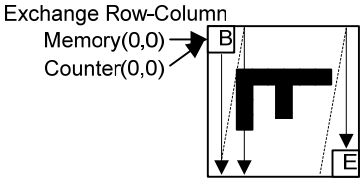
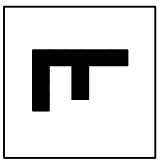
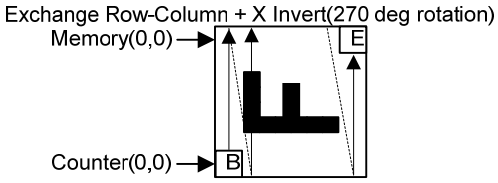
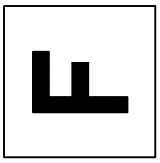
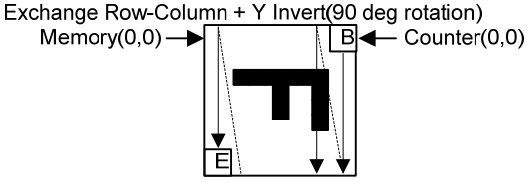
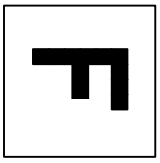
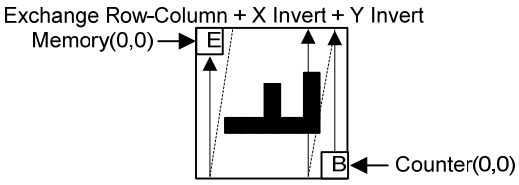
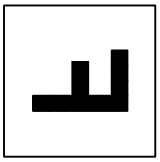


Figure73. Partial Display On: SR [15:0] = 04h, ER [15:0] = 13Ch, MADCTL (B6 = B7 = B4 = '0')

Table 64. MPU to Memory Write/Read Direction By Madctl

Note. There is not possible to avoid the tearing effect in normal display if B5=1.

B5 B6 B7 (Bits)	Image in the Memory ("→" Means "MPU to Memory Read/Write Direction")	IMAGE in the Display
0 0 0		
0 0 1		
0 1 0		

B5 B6 B7 (Bits)	Image in the Memory ("→" Means "MPU to Memory Read/Write Direction")	IMAGE in the Display
0 1 1		
1 0 0		
1 0 1		
1 1 0		
1 1 1		

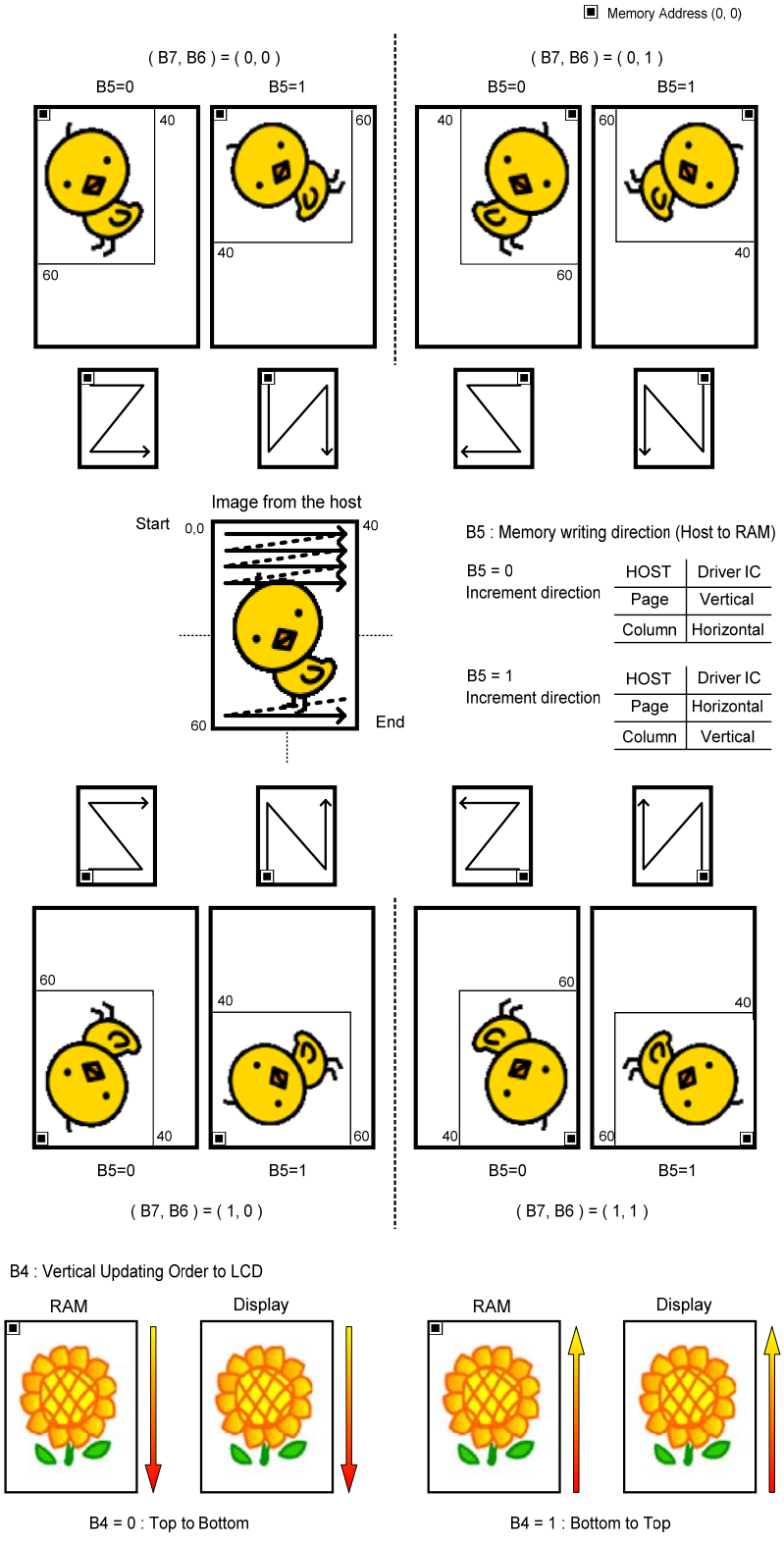


Figure74. Example for Rotation With B7, B6, B5 and B4

4.3.3. COMMAND DEFINITION WHICH INDEPENDENT OF THE IC MOUNT POSITION

Depending on how the MADCTL command is set, the top-bottom / left-right definitions are changed in the driver IC to adapt the mounted form.

4.3.3.1. Model of LCD module for the S6D04H0

The LCD module for the S6D04H0 is shown below. The top-bottom / left-right positions, RGB filter and white or black ground defined in this development specification are in accordance with the diagram shown below.

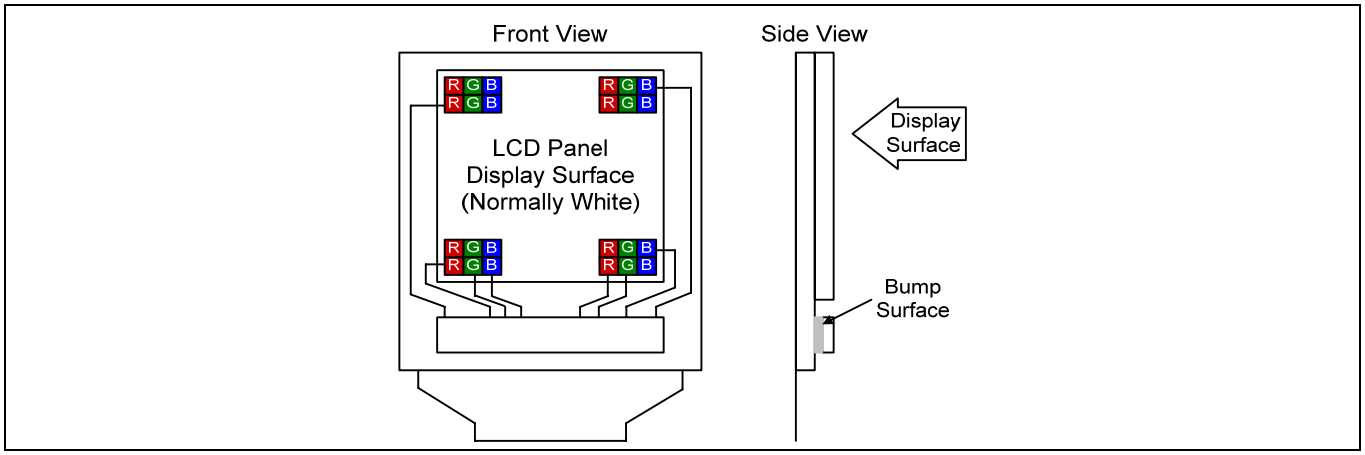


Figure75. Model of LCD Module for the S6D04H0

4.3.3.2. Position definition by IC mount

The set value of MADCTL actually used internally in the IC changes depending on how MADCTL is set. The arithmetic operation in the table below is performed on each bit.

Table 65. Position Definition by IC Mount

MADCTL(36h)	IFCTL(F7h)	IC Internal Setting Value
0	0	0
0	1	1
1	0	1
1	1	0

The set value of MADCTL in the case in which is set to “00h” make a result in the memory access control direction as onto below.

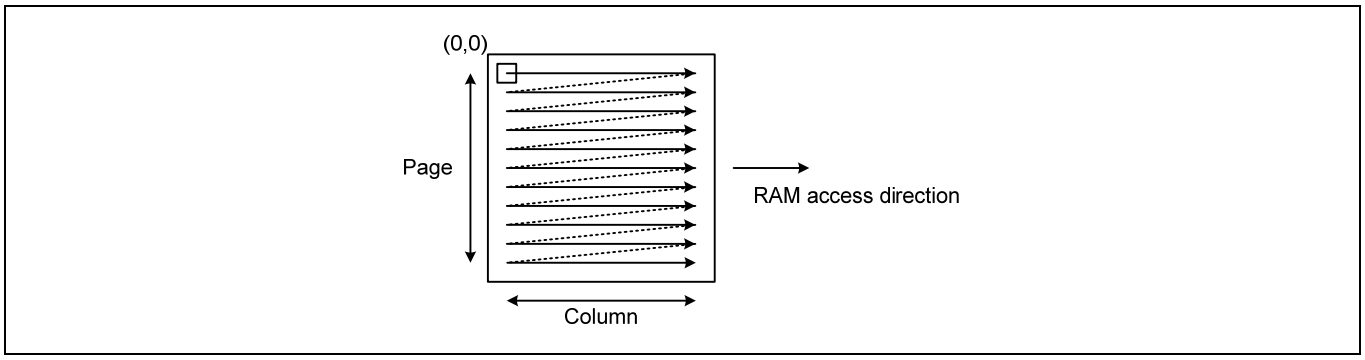
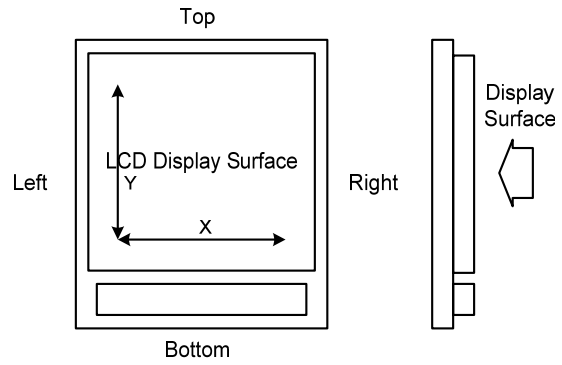


Figure76. Memory Access Control Direction

Refer to the top-bottom / left-right relationship. (The non-bump plane is the surface.)

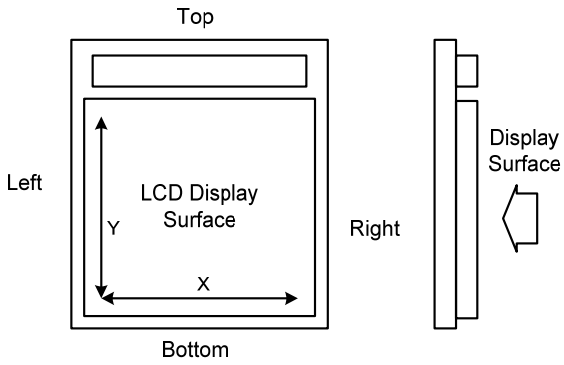
If the driver IC is left-mounted or right-mounted due to the device structure, the display data RAM to LCD display data readout and gate scan direction should be set left-right rather than top-bottom.

Case of Bottom-Mounted IC



(Example) MADCTL(00h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Top to Bottom
Gate line scan Direction	Top to Bottom

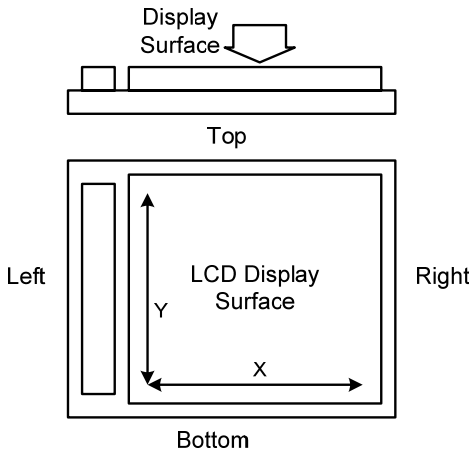
Case of Top-Mounted IC



(Example) MADCTL(D0h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Top to Bottom
Gate line scan Direction	Top to Bottom

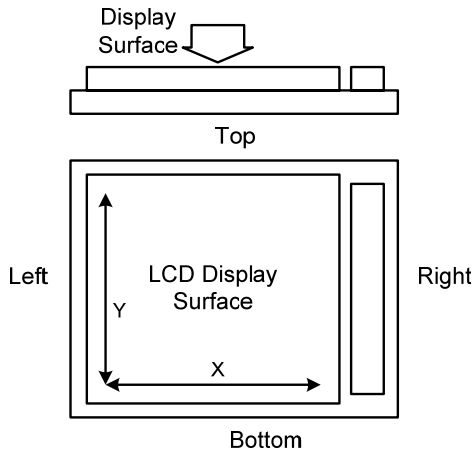
.

Case of Left-Mounted IC



(Example) MADCTL(A0h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Right to Left
Gate line scan Direction	Right to Left

Case of Right-Mounted IC



(Example) MADCTL(60h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Left to Right
Gate line scan Direction	Left to Right

Figure77. Relationship of Each Direction

4.3.4. 0-ADDRESS POSITION AND RAM ACCESS SCAN DIRECTION

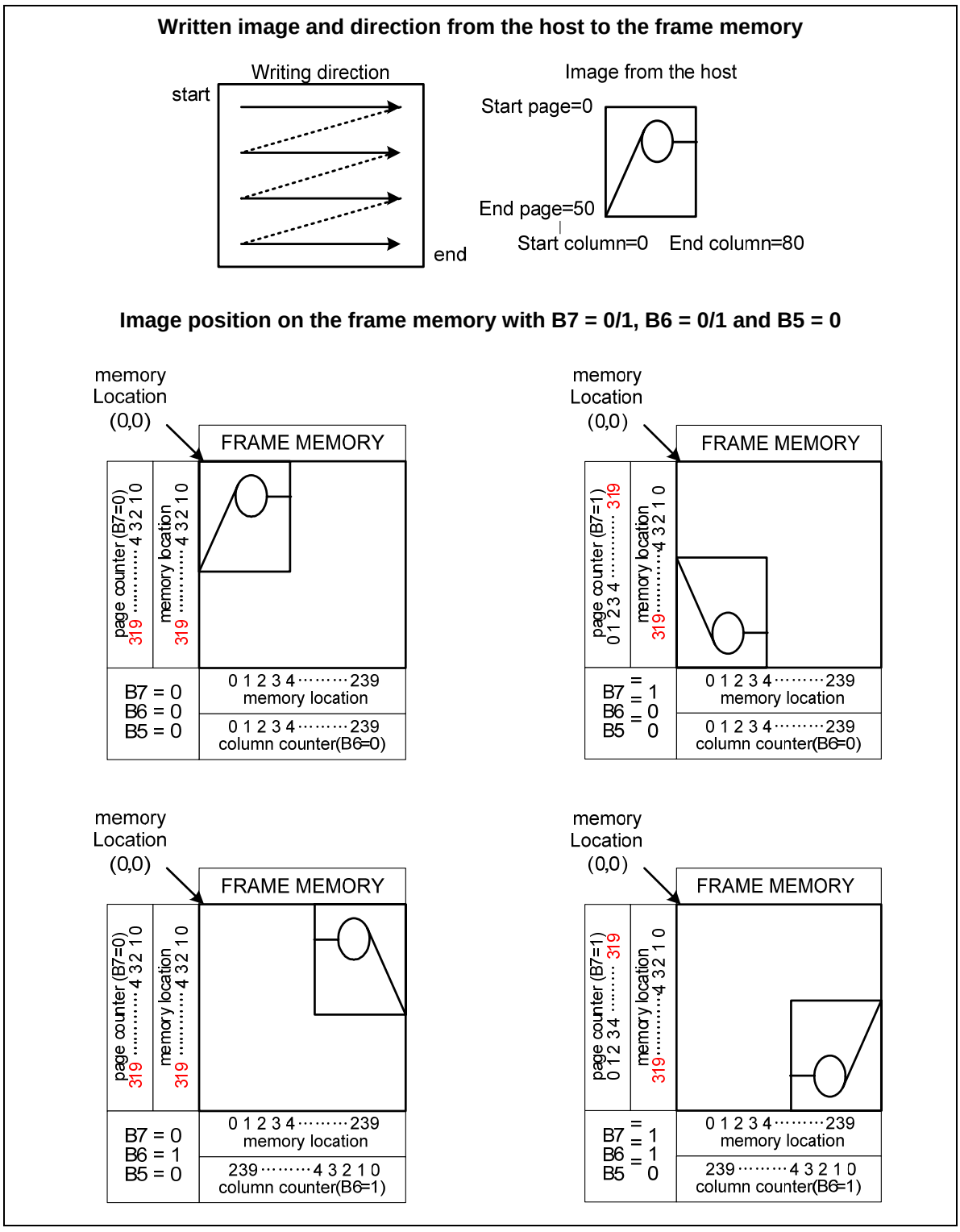


Figure78. Refer to MADCTL (MADCTL=00h)

Written image and direction from the host to the frame memory

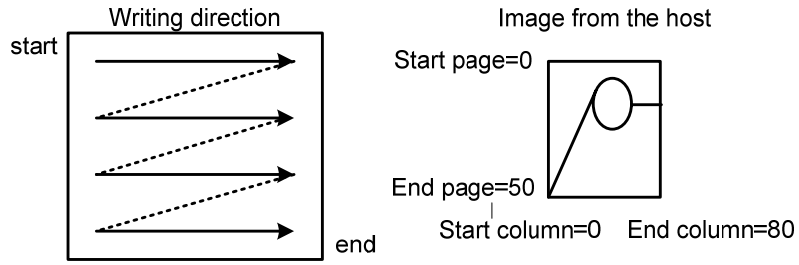


Image position on the frame memory with B7 = 0/1, B6 = 0/1 and B5 = 1

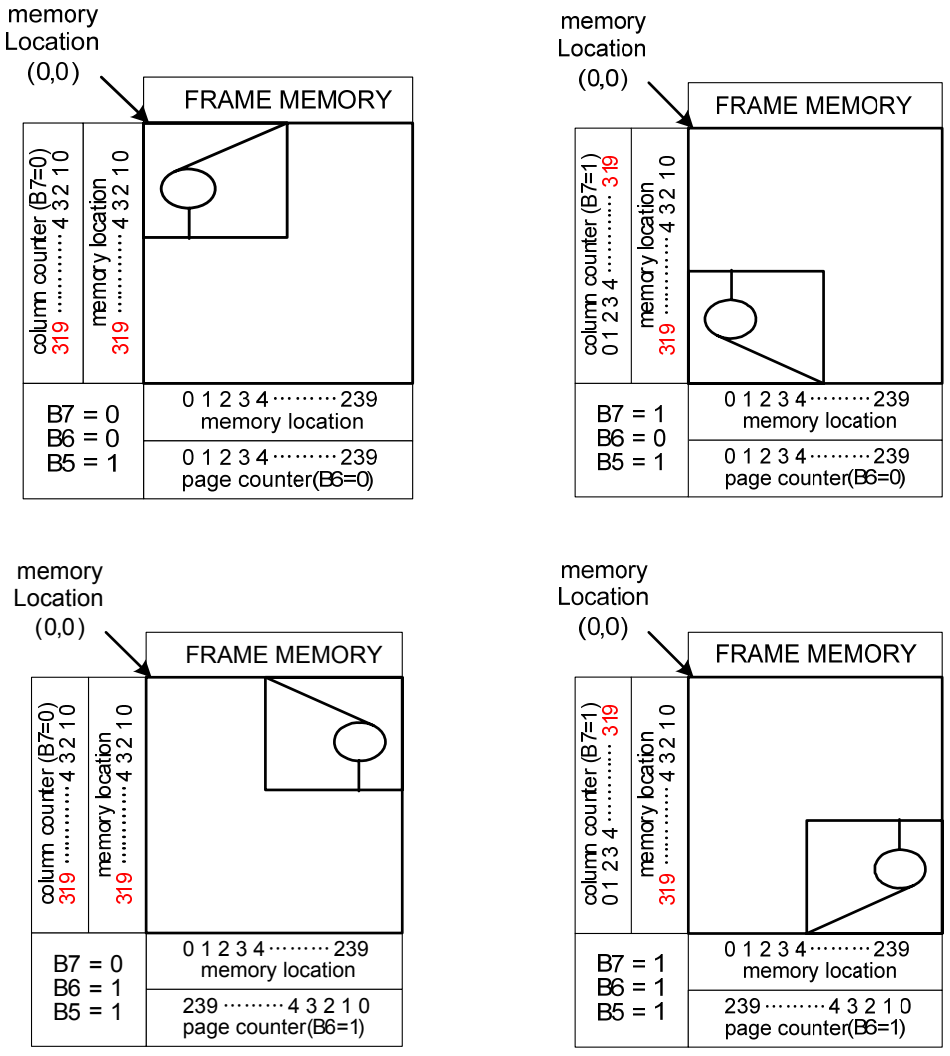


Figure79. Refer to MADCTL (MADCTL=00h)

4.4. MTP CONTROL

4.4.1. MTP CONTROL IN INTERNAL MODE

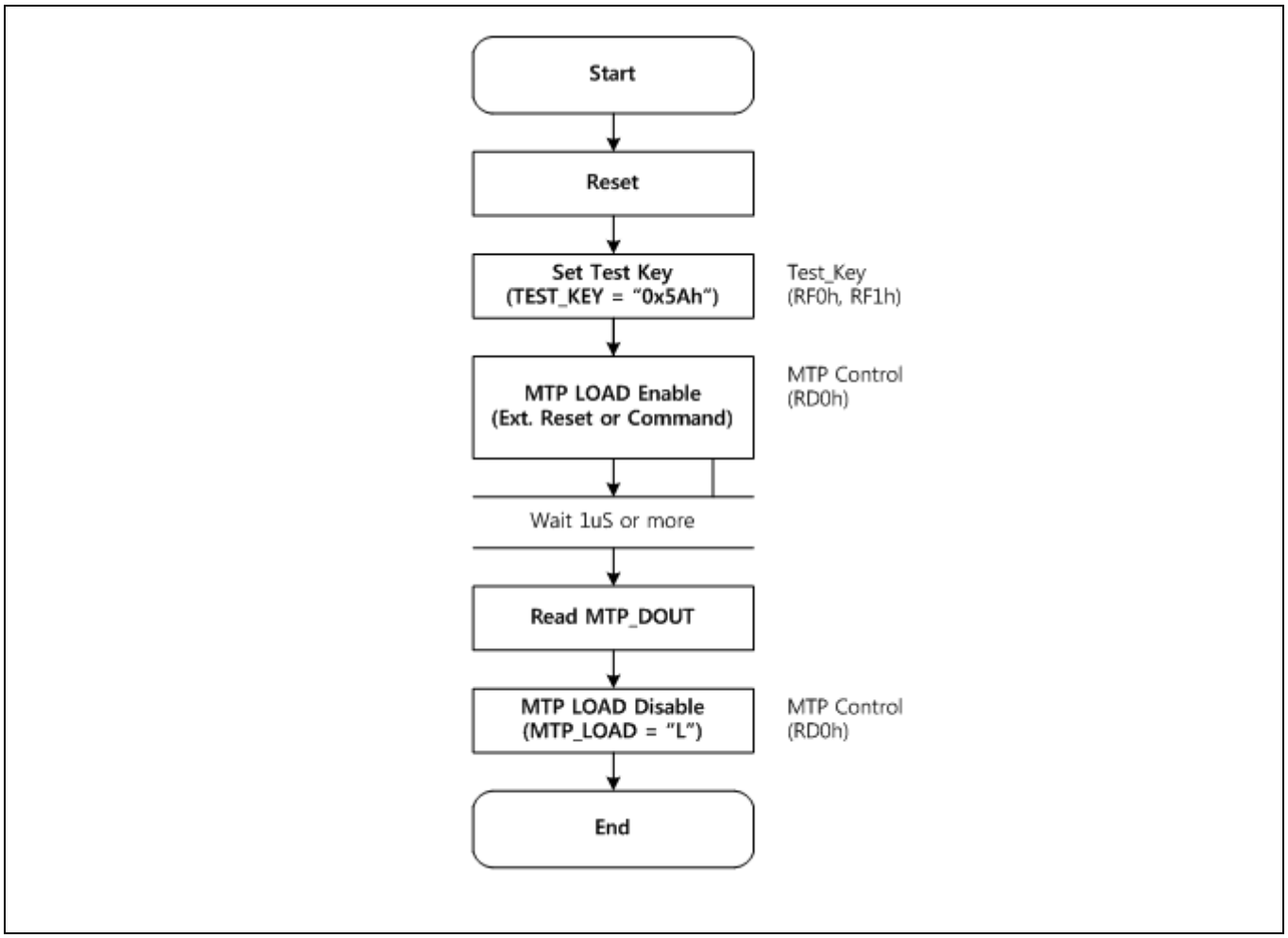


Figure80. Flow of MTP Load / Read

4.4.1.1. Using VCI1 for MTP at Internal Power Mode

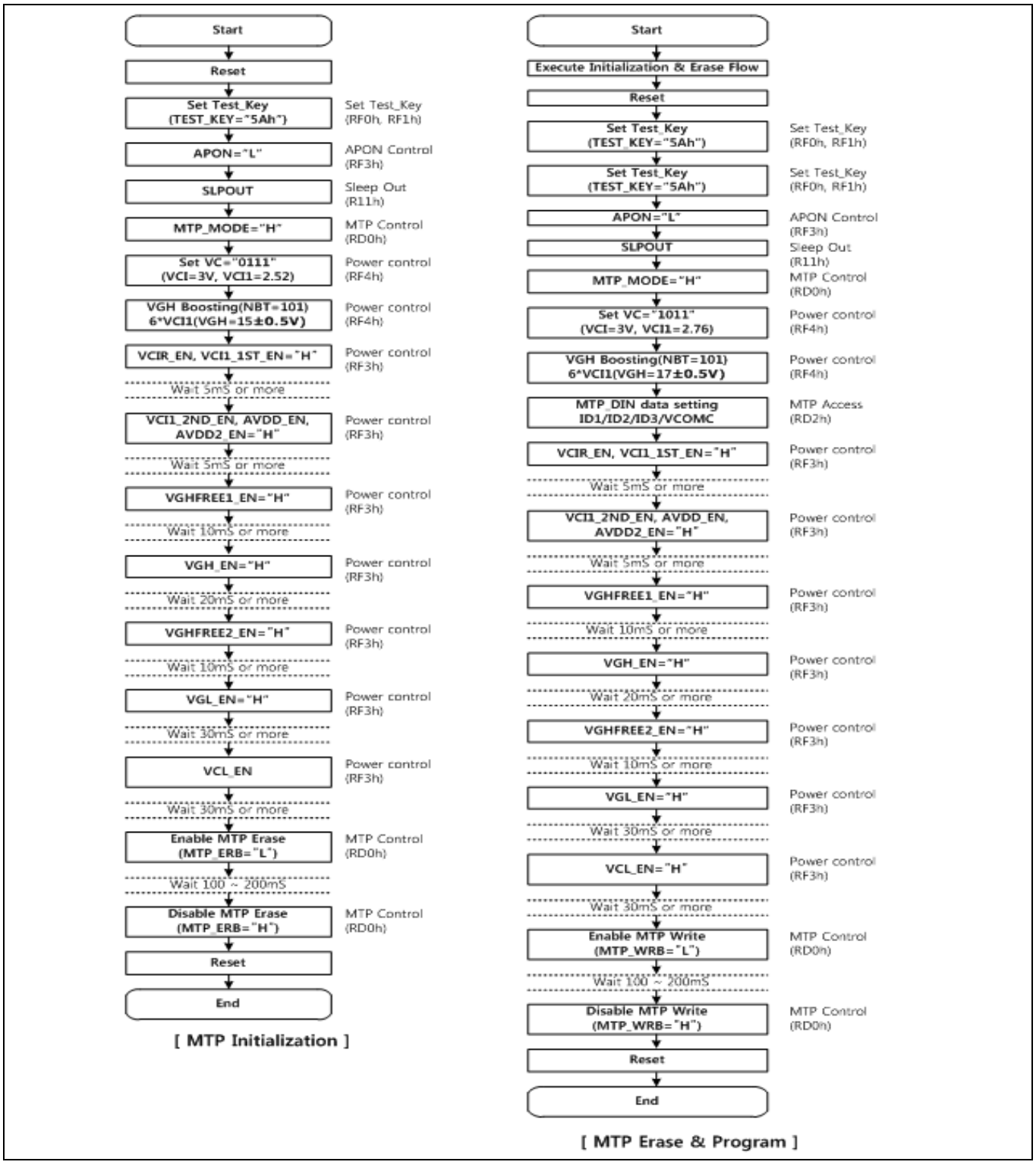


Figure81. MTP Initialization, Erase and Program Internal Power Mode(VCI1)

4.4.1.2. Using VCI for MTP at Internal Power Mode

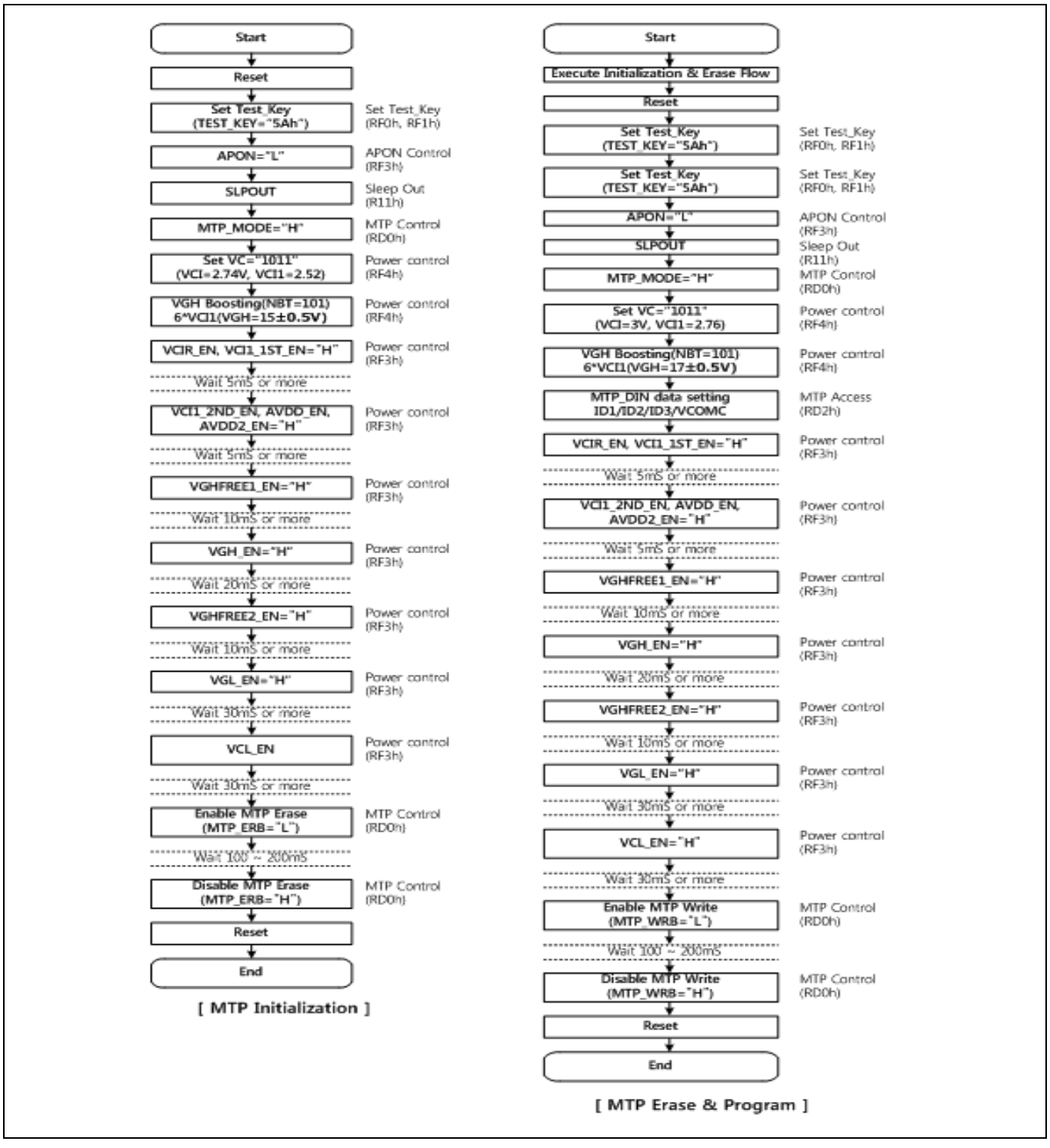


Figure82. MTP Initialization, Erase and Program Internal Power Mode(VCI)

4.4.1.3. Using External Power for MTP

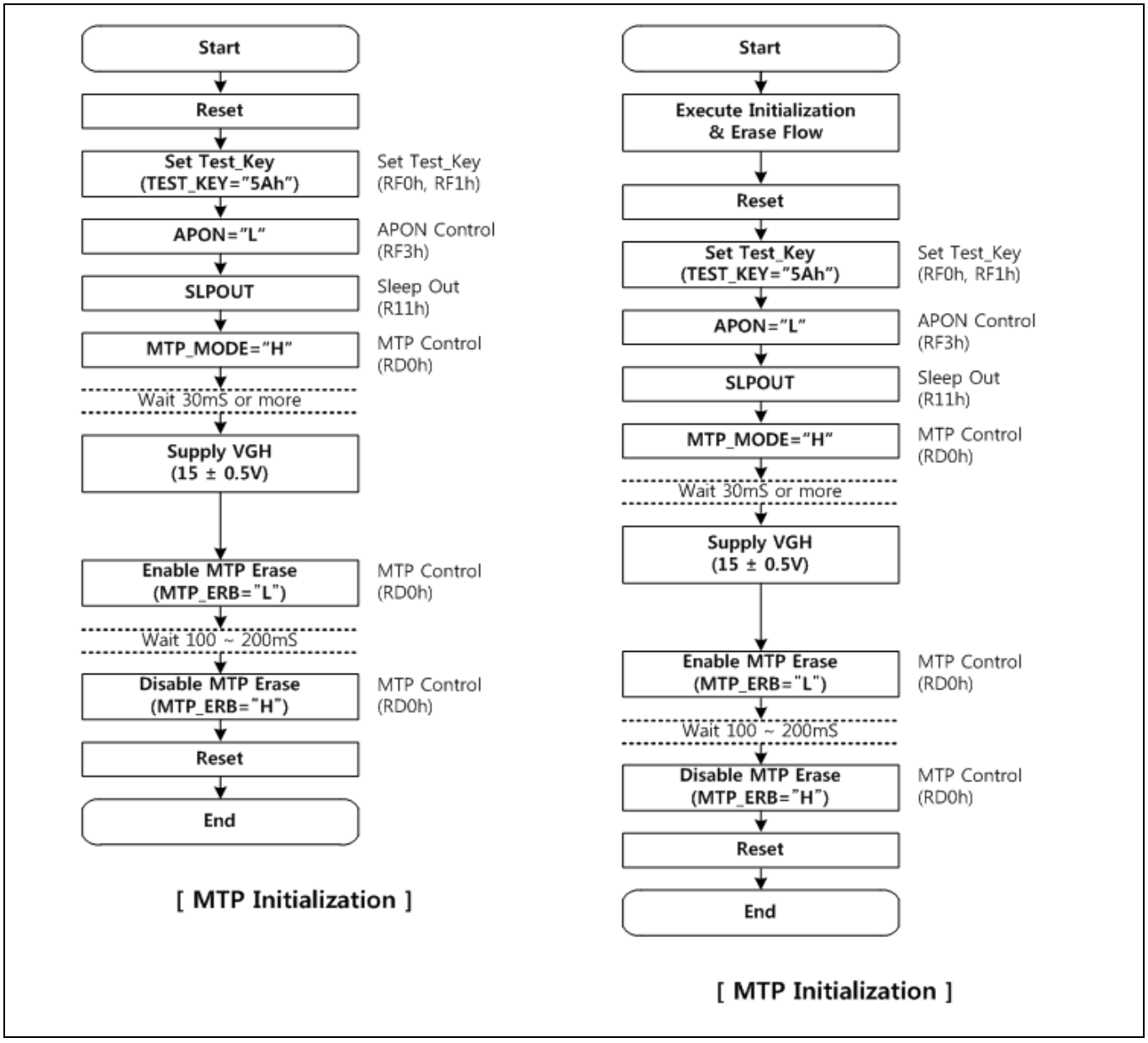


Figure83. MTP Initialization, Erase and Program External Power Mode

4.4.2. TIMING OF MTP CONTROL

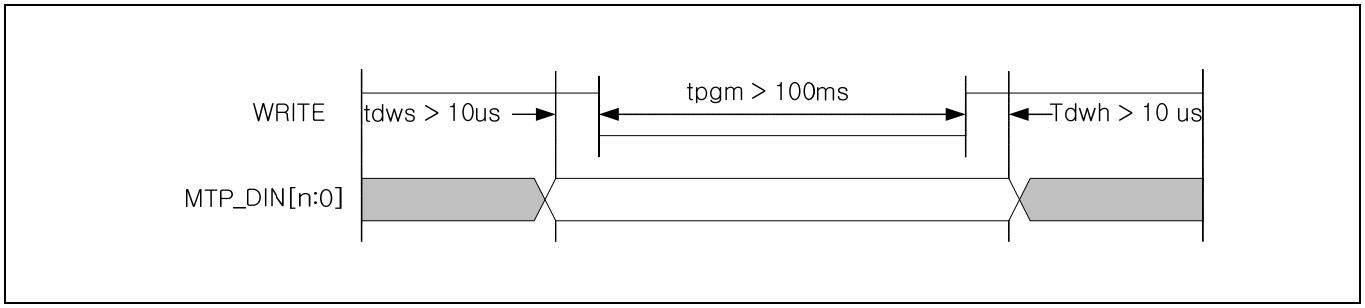


Figure84. Timing of MTP Program

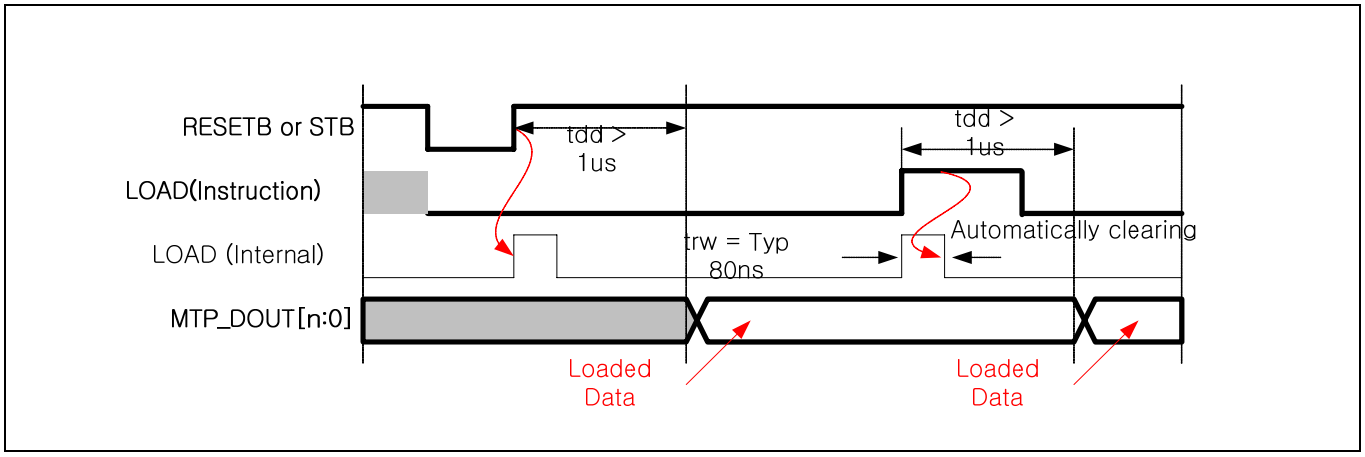


Figure85. Timing of MTP Load

4.5. TEARING EFFECT OUTPUT LINE

Tearing Effect is the effect that the overwritten two frames are shown as they are torn when Display Data RAM (DDRAM) is updated during Display Driver IC (DDI) scans the panel. This effect caused by the asynchronous timing between scanning of the DDI timing controller and frame transfer of the host processor.

To help the host processor avoid this effect, DDI generates Tearing Effect output line (TE) signal which has the timing of the period in which the DDI does not do panel-scan and the timing of vertical or horizontal synchronization. Host processor can avoid Tearing Effect by transfer only during TE signal is high.

The period in which the DDI does not panel-scan is the vertical blanking time. By TEON Command (35h) with parameter 0, the host can make the TE pin high in the vertical blanking time. With parameter 1, the TE signal includes the vertical blanking time and horizontal sync. By TEOFF Command (34h), the host can turn off the TE signal and this is the default state.

4.5.1. TEARING EFFECT LINE MODES

Mode 1, TEON (35h) Command, Parameter 0: The Tearing Effect Output signal consists of V-Blanking Information only

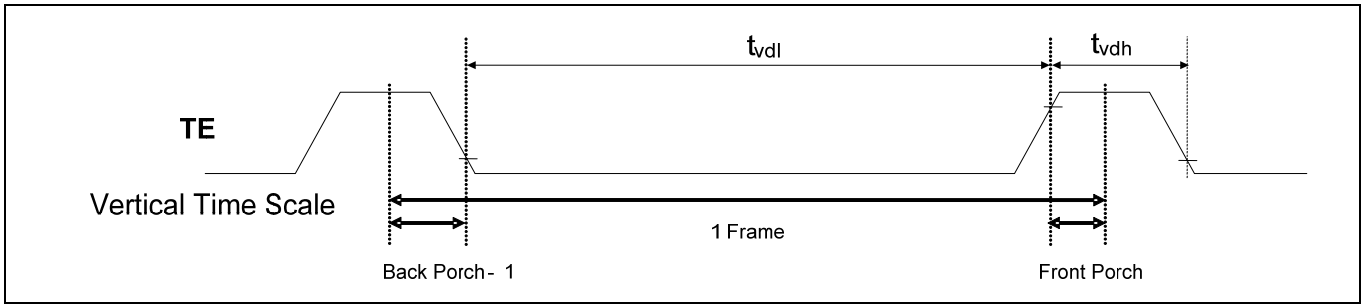


Figure86. Tearing Effect Line Mode 1

t_{vdh} = The LCD display is not updated from the Frame Memory

t_{vdl} = The LCD display is updated from the Frame Memory(except Invisible Line – see below).

Mode 2, TEON (35h) Command, Parameter 1: the Tearing Effect Output signal consists of V-Blanking and H-Sync

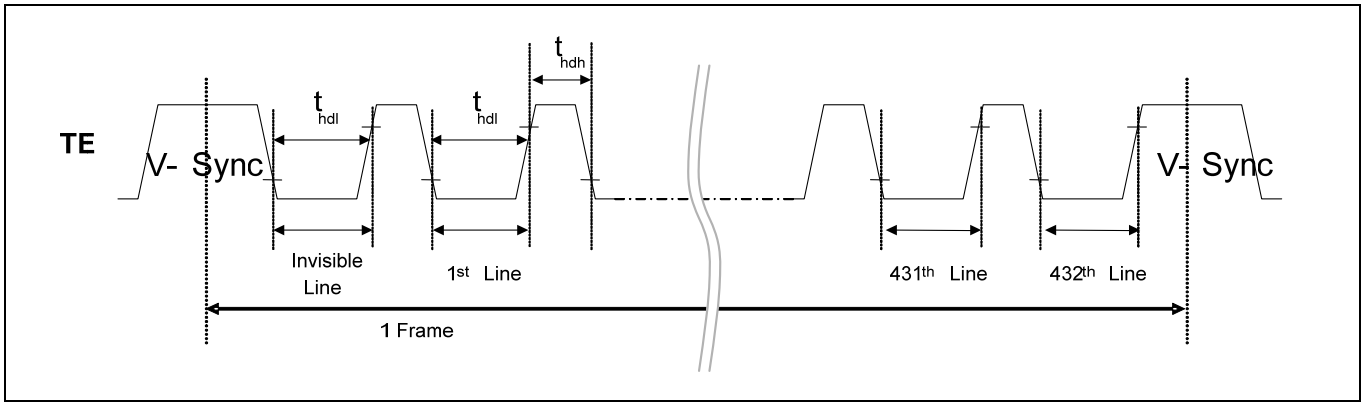
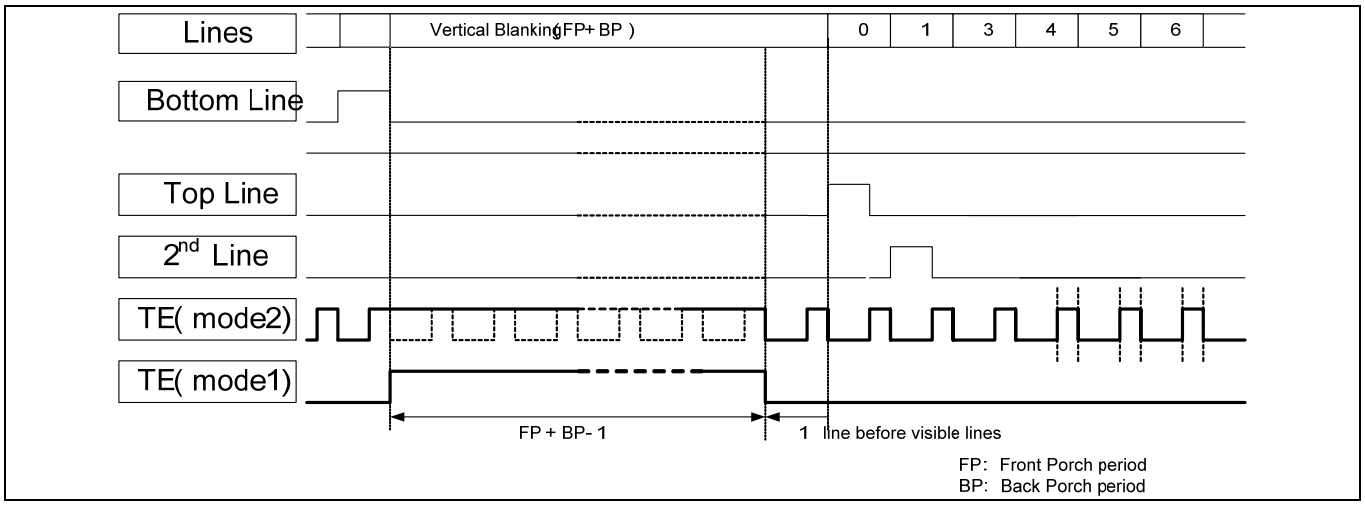


Figure87. Tearing Effect Line Mode 2

t_{hdh} = The LCD display is not updated from the Frame Memory

t_{hdl} = The LCD display is updated from the Frame Memory(except Invisible Line – see below).



Note.

During Sleep In Mode, the Tearing Effect Pin Output is Low.

4.5.2. TEARING EFFECT LINE TIMINGS

The Tearing Effect signal is described below

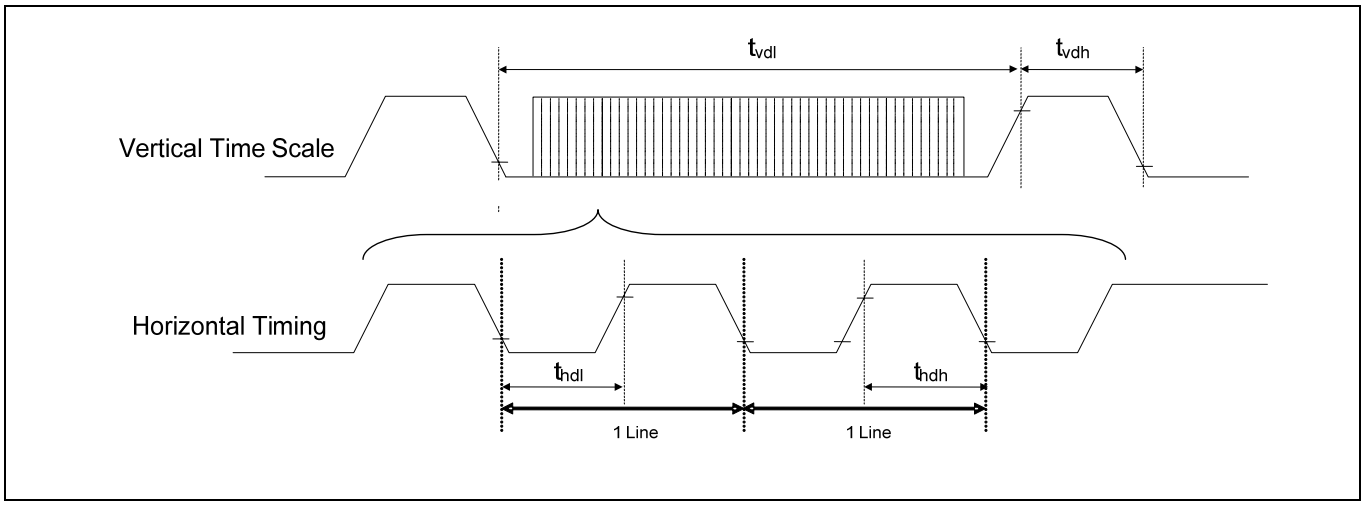


Figure88. Tearing Effect Line Timing

Table 66. AC Characteristics of Tearing Effect Signal

Symbol	Parameter	Min	Max	Unit	Description
tvdl	Vertical Timing Low Duration	-	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	-	-	µs	
thdh	Horizontal Timing High Duration	-	500	µs	

Note.

1. Idle Mode Off/On (Frame Rate = 60 Hz)
2. The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns.

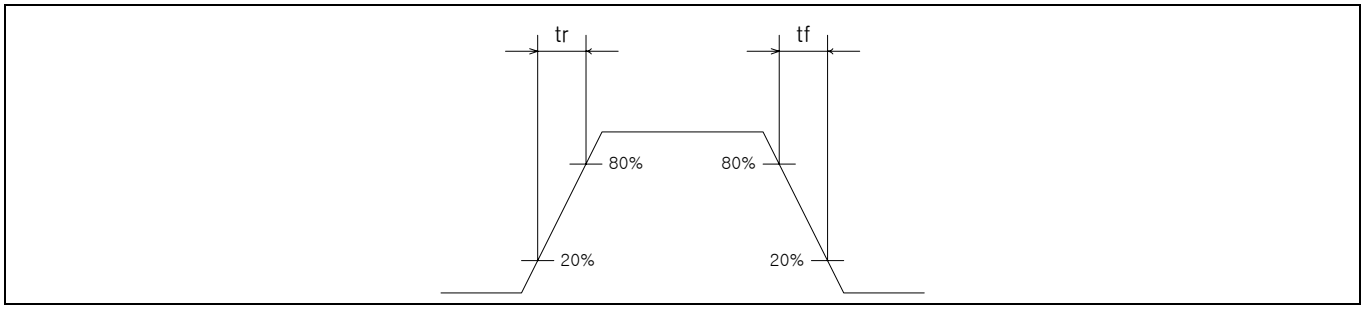


Figure89. Rising and Falling Times

The Tearing Effect Output Line is fed back to the MPU and should be below to avoid Tearing Effect.

4.6. SLEEP OUT COMMAND AND SELF-DIAGNOSTIC FUNCTIONS

4.6.1. REGISTER LOADING DETECTION

Sleep out command (See “Sleep out (11h) command”) is a trigger for an internal function of the display module which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: Compares register and EEPROM) values, 2nd step: Loads EEPROM value to register. If those both values (EEPROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command 5.1.10 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

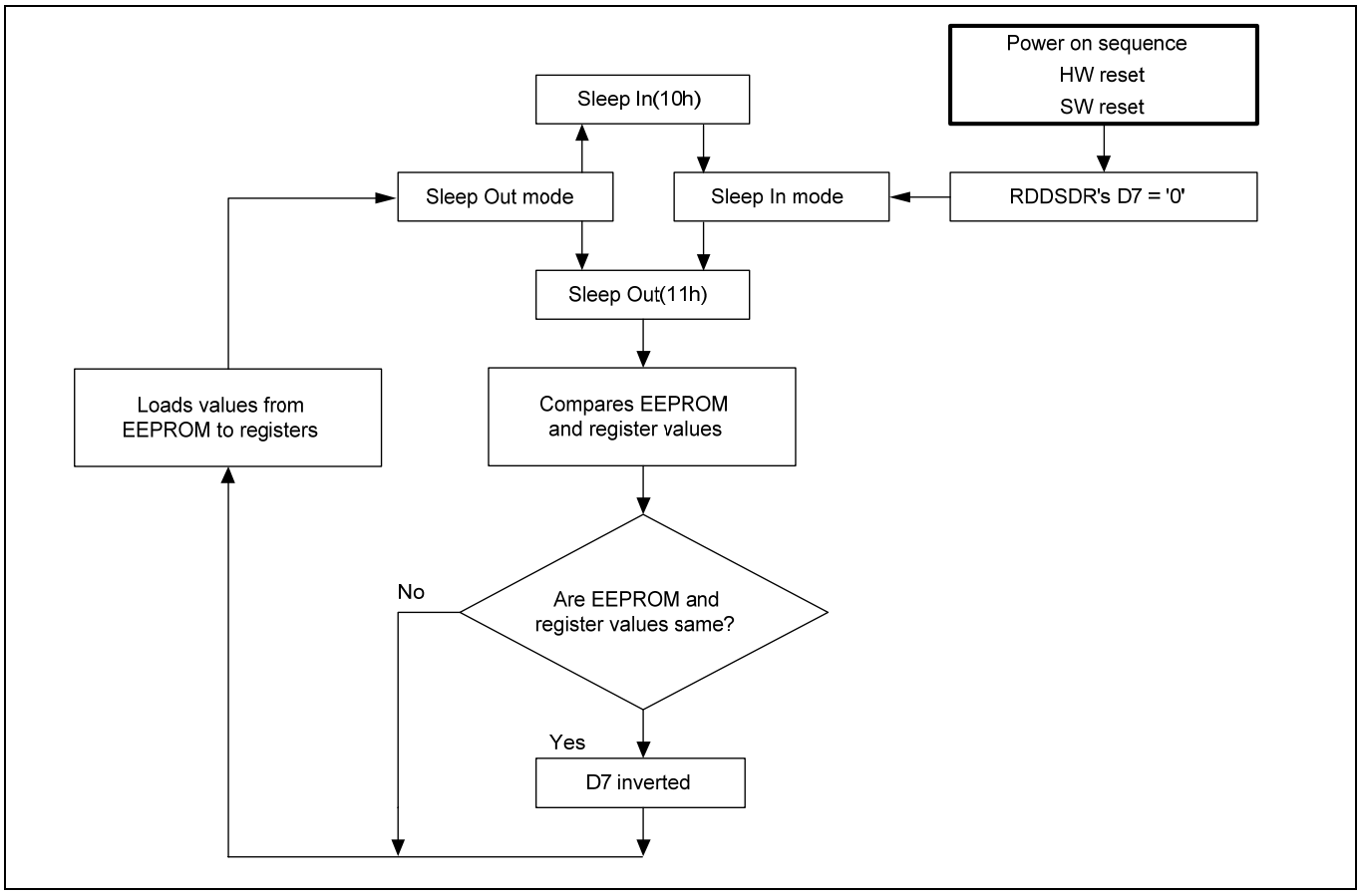


Figure90. Flowchart of Register Loading Detection

Note.

There is not compared and loaded register values, which can be changed by the display module.

4.6.2. FUNCTIONALITY DETECTION

Sleep out command (See section 5.1.12 “Sleep Out (11h) command”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. step up circuit voltage levels, timings, etc.) If functionality requirement is met, there is inverted (=increased by 1) a bit, which defined in command 5.1.10 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

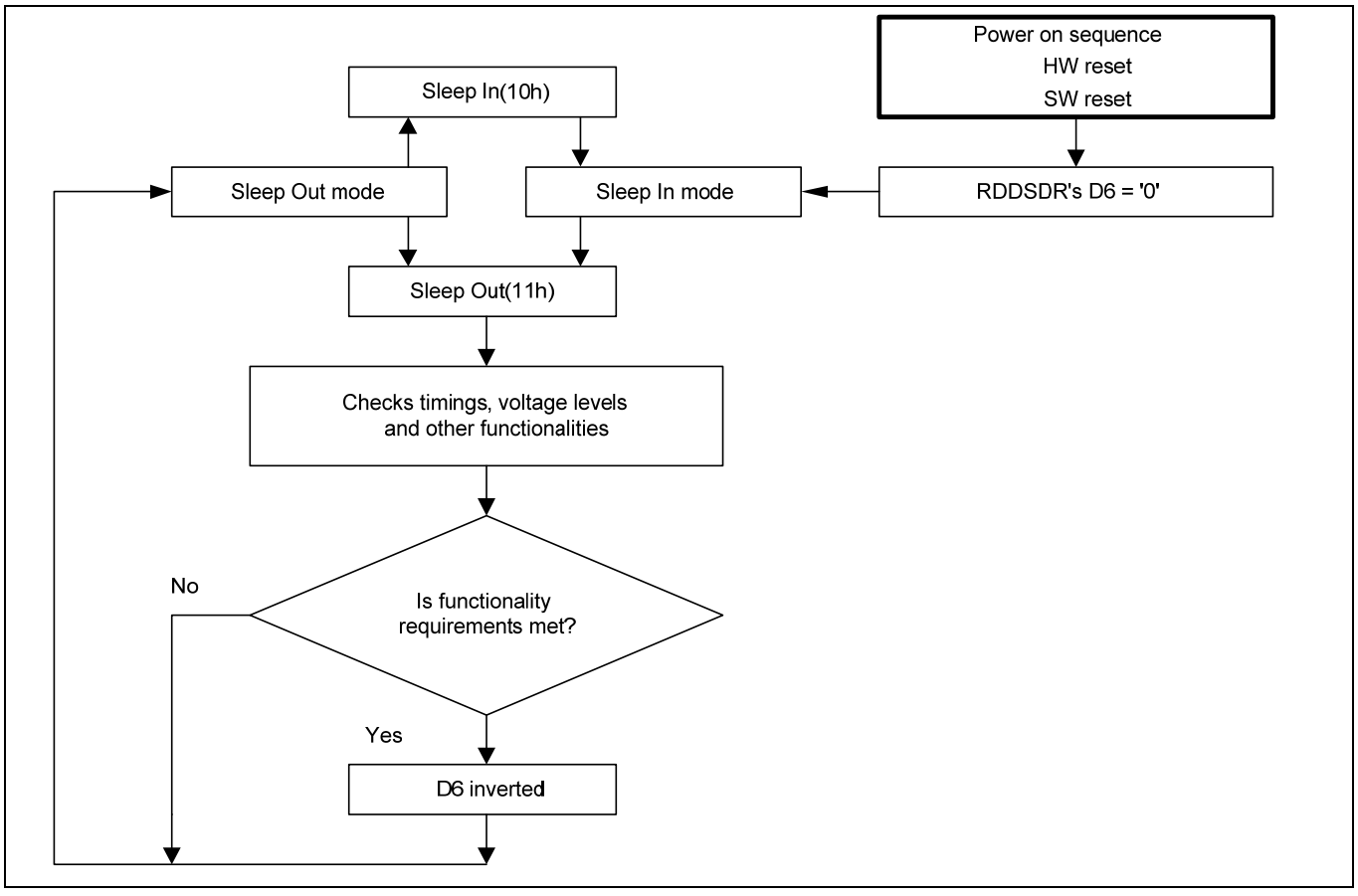


Figure91. Flowchart of Functionality Detection

Note.

There is needed 120msec after Sleep out command, when there is changing from Sleep in mode to Sleep out mode, before there is possible to check if functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep out command is sent in Sleep out mode.

4.7. MIE FUNCTION

S6D04H0 has a special image enhancement function. MIE (Mobile Image Enhancement) reduces power consumption of backlight unit by adaptive enhancement of luminance and contrast. According the brightness enhancement rate of input image, the power reduction of BLU is controlled automatically.'

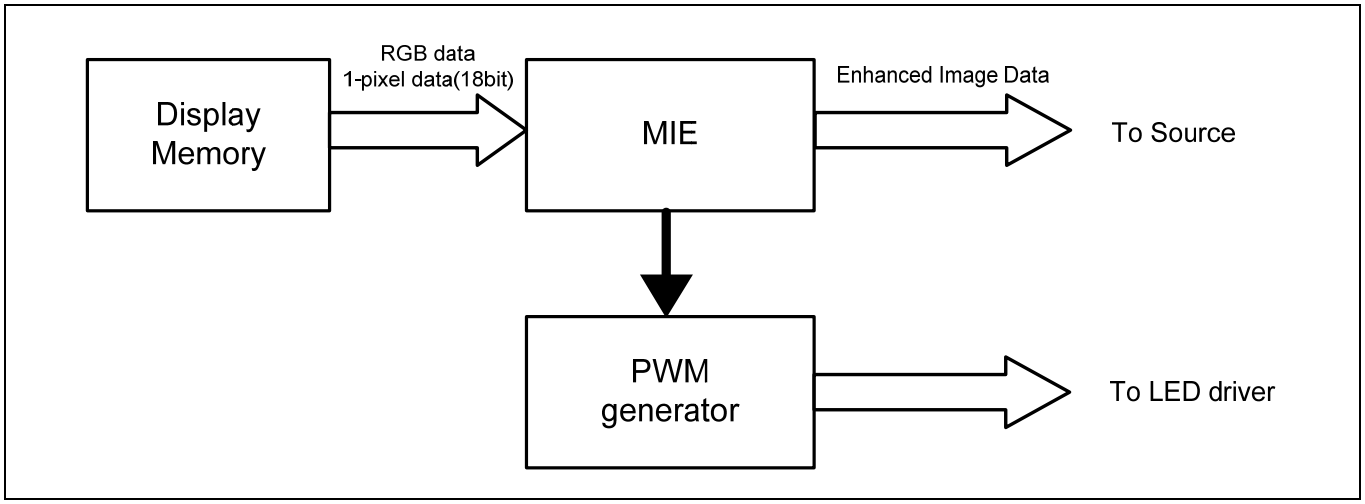


Figure92. Flowchart of MIE Function

When MIE is enabled, MIE dynamically changes the brightness of backlight unit by on-chip PWM Generator. Host can control the rate of BLU power reduction by setting RRC value (Refer to E9h Command.)

When MIE is enabled, the enhanced data is applied after written Display Memory data and in case MIE mode, data transfer shift register method to Source block. Host processor should select movie or still-Image mode (Refer to E9h Command).

*MIE applied, ML = 1'b0. Recommended MIE applied, when ML = 1 'b0.

4.8. DEEP STANDBY MODE

4.8.1. DEEP STANDBY SEQUENCE

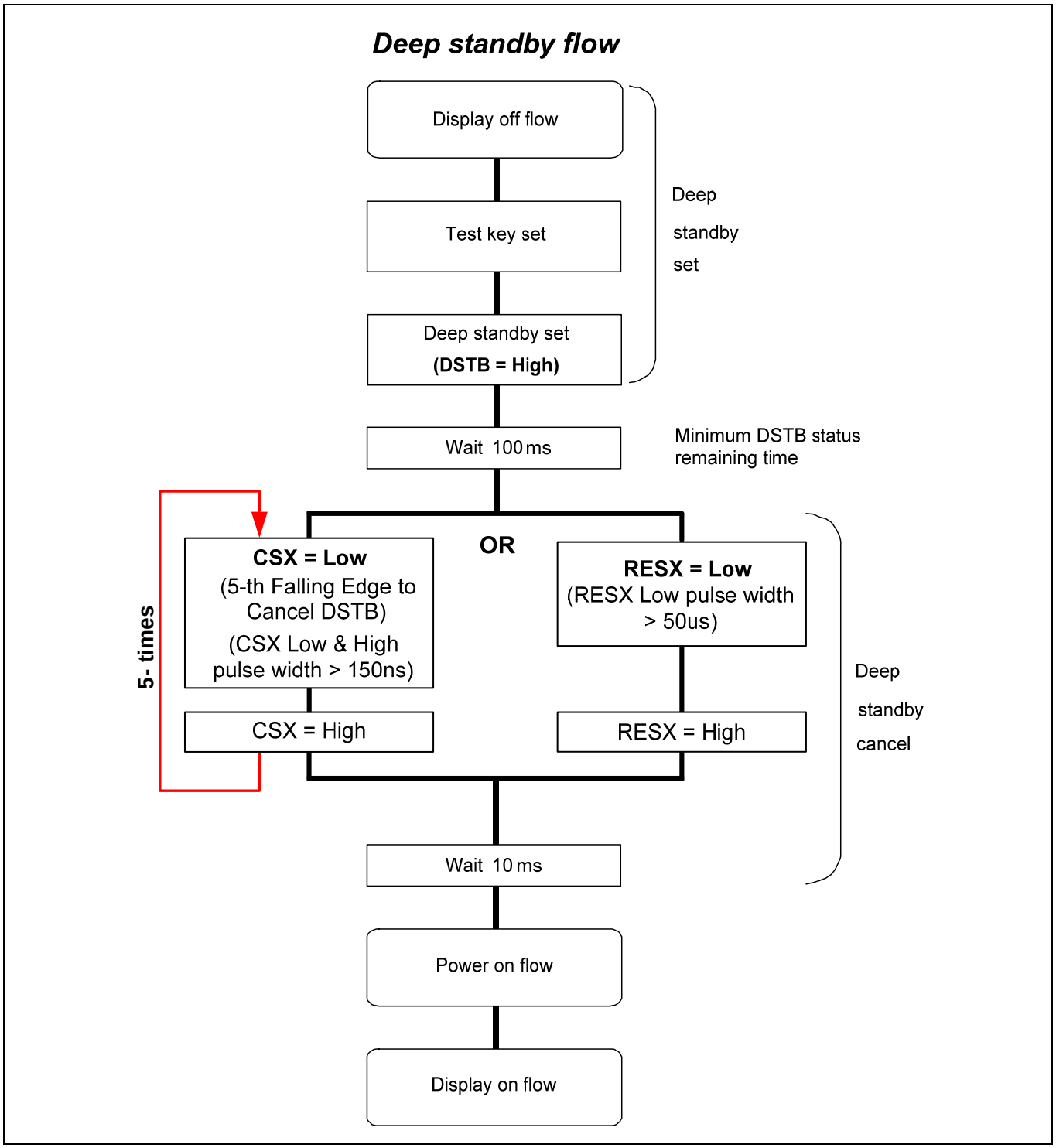


Figure93. Flowchart of Deep Standby Mode

4.8.2. DEEP STANDBY EXIT FLOW

4.8.2.1. Using CSX to wake-up

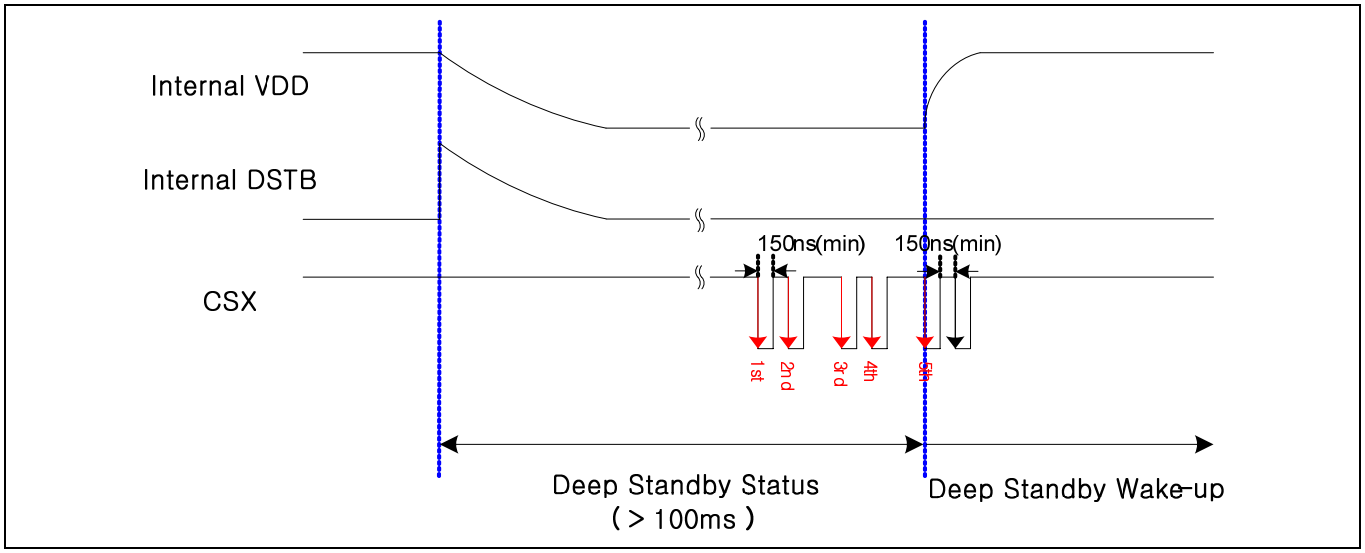


Figure94. Using CSX to Wake-Up

4.8.2.2. Using RESX to wake-up

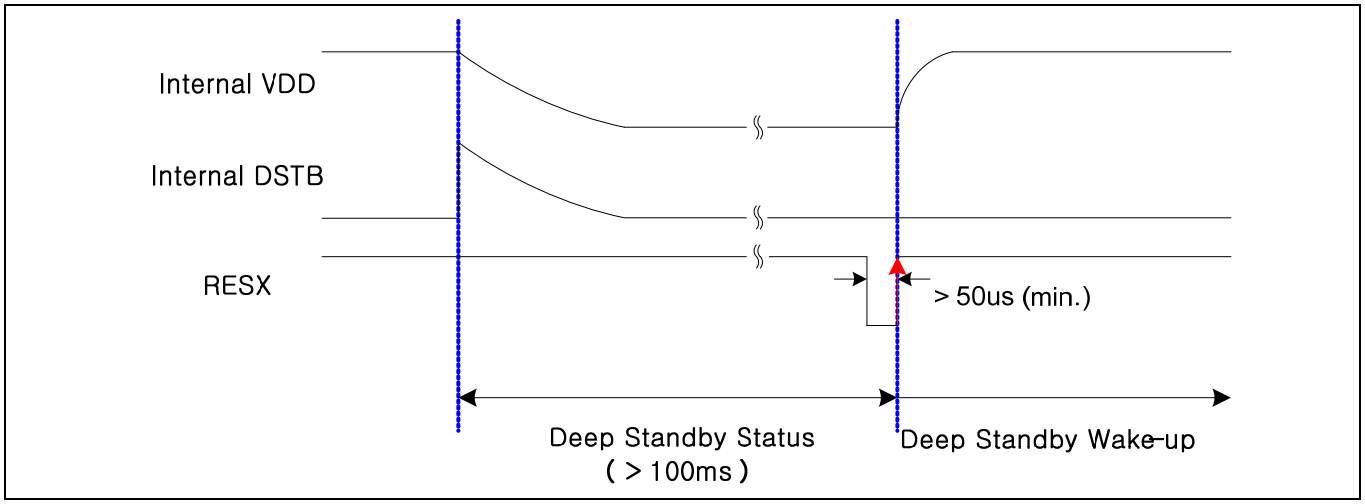


Figure95. Using RESX to Wake-Up

4.8.3. DEEP STANDBY ENTER FLOW

4.8.3.1. During display state

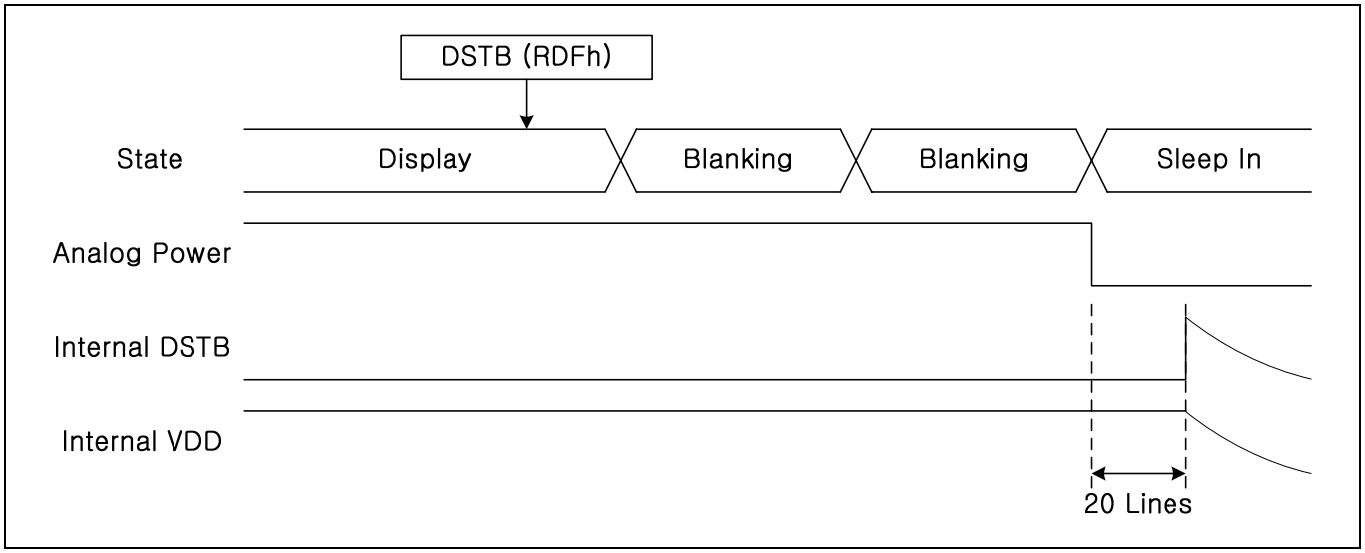


Figure96. DSTB Enter During Display State

4.8.3.2. During sleep in state

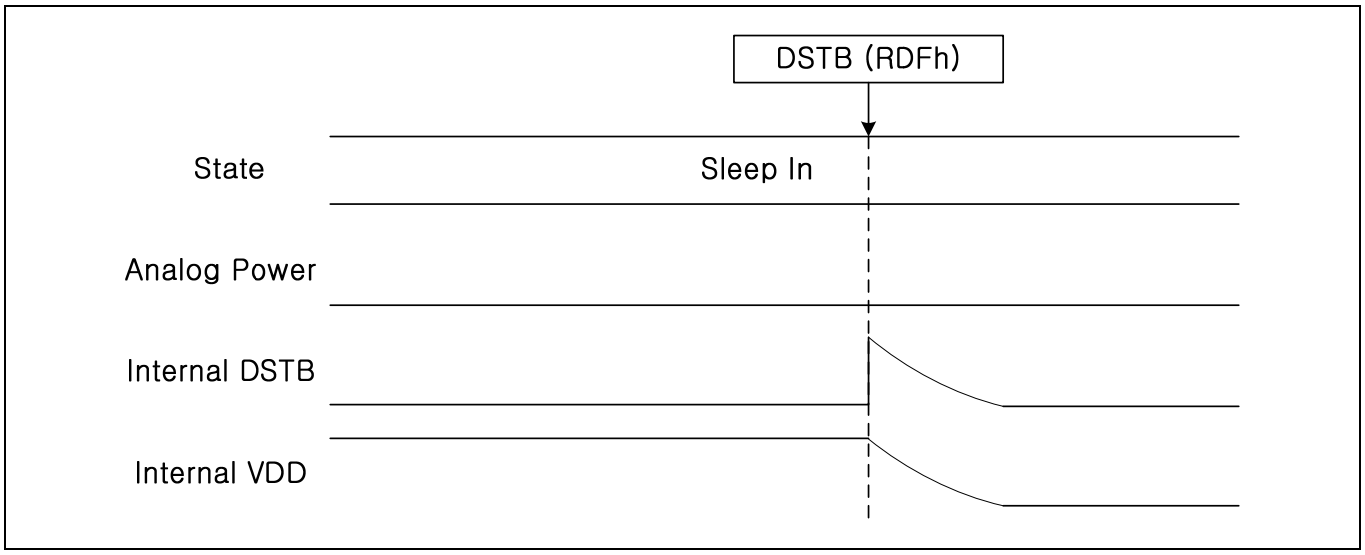


Figure97. DSTB Enter During Sleep in State

4.9. DISPLAY ON/OFF SEQUENCE

4.9.1. DISPLAY ON SEQUENCE

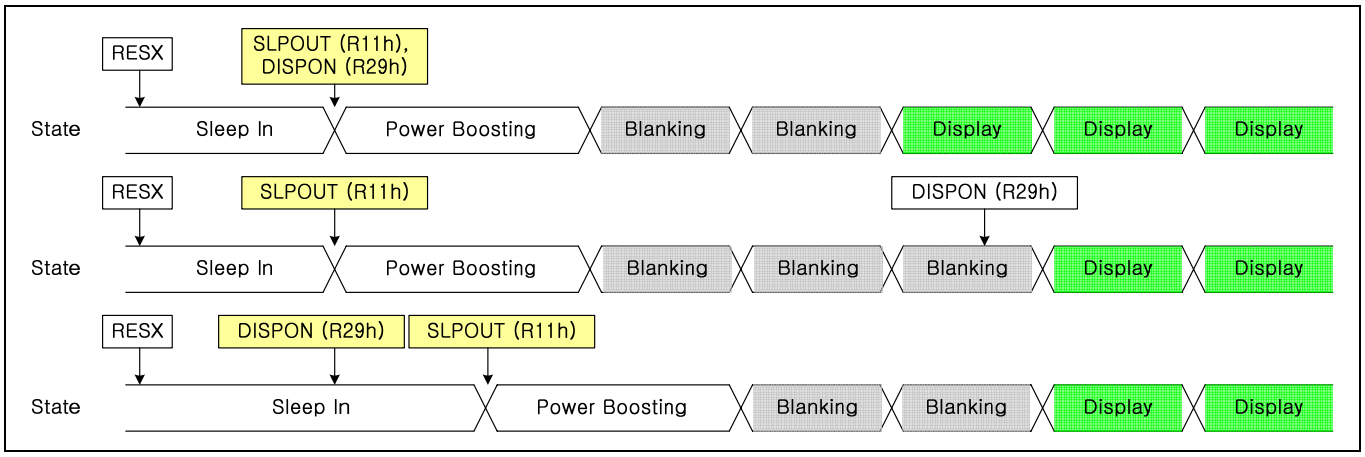


Figure98. Display On Sequence (APON=1)

4.9.2. DISPLAY OFF SEQUENCE

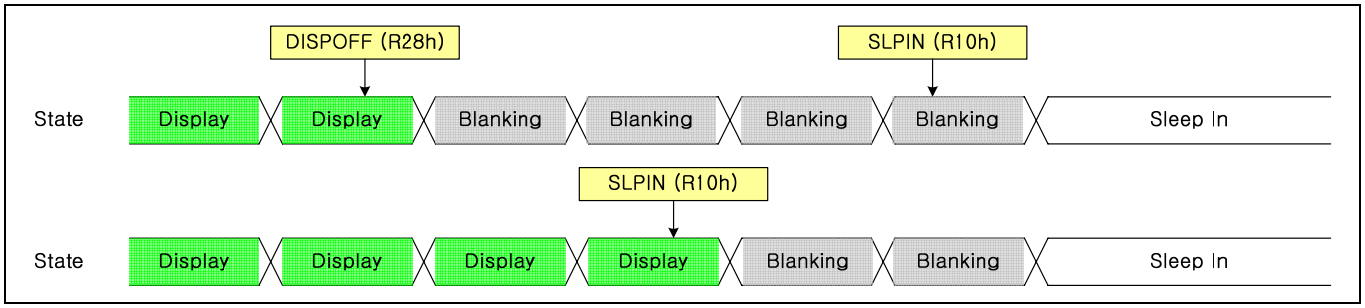


Figure99. Display Off Sequence (APON=1)

CHAPTER 5

COMMAND

5. COMMAND

5.1. DESCRIPTION OF LEVEL 1 COMMAND

Table 67. List of Level 1 Command

Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	Parameters
00	No Operation	C	0	-
01	Software Reset	C	0	-
04	Read Display Identification Information	R	4	
09	Read Display Status	R	5	
0A	Read Display Power Mode	R	2	
0B	Read Display MADCTL	R	2	
0C	Read Display Pixel Format	R	2	
0D	Read Display Image Mode	R	2	
0E	Read Display Signal Mode	R	2	
0F	Read Display Self Diagnostic Result	R	2	
10	Sleep In	C	0	-
11	Sleep Out	C	0	-
12	Partial Mode On	C	0	-
13	Normal Display Mode On	C	0	-
20	Display Inversion Off	C	0	-
21	Display Inversion On	C	0	-
26	Gamma Set	W	1	format: 1 byte for curve selection
28	Display Off	C	0	-
29	Display On	C	0	-
2A	Column Address Set	W	4	format: 2 byte for leftmost Column counter 2 byte for rightmost Column counter

Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	Parameters
2B	Page Address Set	W	4	format: 2 byte for top line pointer 2 byte for bottom line pointer
2C	Memory Write	W	Any Length	Successive video data stream Format in all color modes
2E	Memory Read	R	Any length	Successive video data stream Format in all color modes.
30	Partial Area	W	4	format: 2 byte for top line pointer 2 byte for bottom line pointer
33	Vertical Scrolling Definition	W	6	format: 2 byte for fixed area top line pointer 2 byte for scrolling area height 2 byte for fixed area bottom line pointer
34	Tearing Effect Line Off	C	0	-
35	Tearing Effect Line On	W	1	1 byte for Tearing Effect Line Mode selection
36	Memory Data Access Control	W	1	1 byte for memory scan direction
37	Vertical Scrolling Start Address	W	2	2 byte for line pointer
38	Idle Mode Off	C	0	-
39	Idle Mode On	C	0	-
3A	Interface Pixel format	W	1	Refer to Section 5.1.33
3C	Memory Write Continue	W	Any length	
3E	Memory Read Continue	R	Any length	
44	Set Tear Scanline	W	2	format: 2 byte for TE signal turns on when the display module reaches line N.
45	Get Scanline	R	2	
51	Write Manual Brightness	W	1	MAN_BRIGHT[7:0]
52	Read Display Brightness	R	2	DISP_BRIGHT[7:0]
53	Write BL Control	W	1	BCTRL, DD, BL

Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	Parameters
54	Read BL Control	R	2	BCTRL, DD, BL
55	Write MIE Mode	W	1	MIE_MODE[1:0]
56	Read MIE Mode	R	2	MIE_MODE[1:0]
5E	Write Minimum Brightness	W	1	MIN_BRIGHT[7:0]
5F	Read Minimum Brightness	R	2	MIN_BRIGHT[7:0]
A1	Read DDB Start	R	Any lenth	
A8	Read DDB Continue	R	Any lenth	
DA	Read ID1	R	2	
DB	Read ID2	R	2	
DC	Read ID3	R	2	

Note.

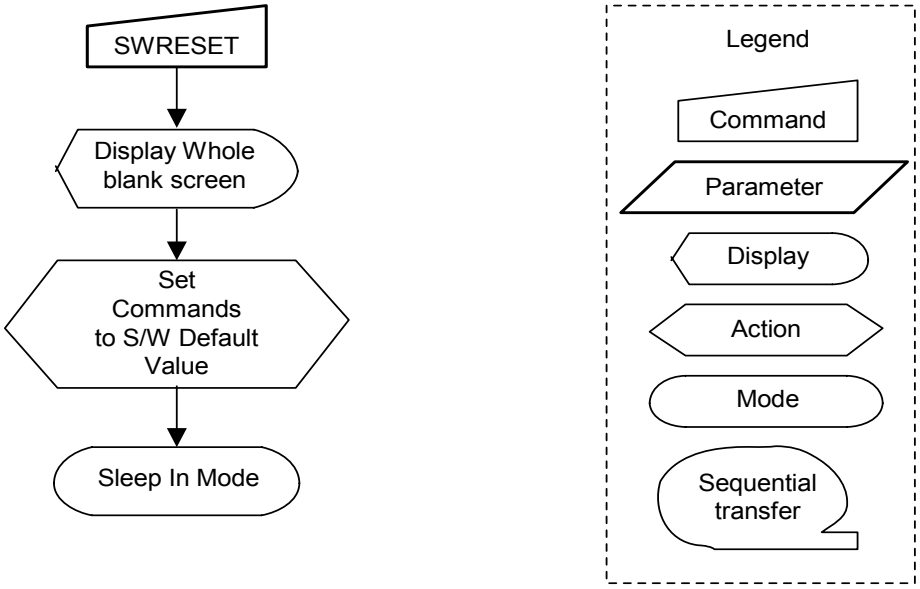
1. Undefined commands are treated as NOP (00h) command.
2. B0h to D9h and DEh to FFh are for factory (= display supplier) use. These commands are treated as NOP (00h) commands after shipping to factory. Default value is NOP (00h).
3. Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-sync when Module is in Sleep Out mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

5.1.1. NO OPERATION (00H)

<table>
<tr><th>00H</th><th colspan="11">NOP (No Operation)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"></td></tr>
</table>

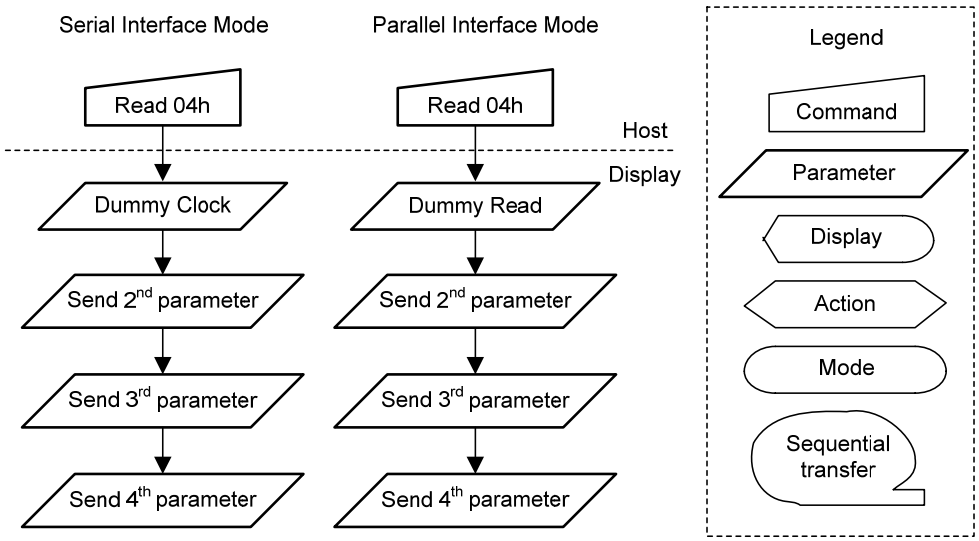
5.1.2. SOFTWARE RESET (01H)

<table>
<tr><th>01H</th><th colspan="12">SWRESET (Software Reset)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
Note: The Frame Memory contents are unaffected by this command.</td></tr>
<tr><td>Restriction</td><td colspan="12">It will be necessary to wait 5 msec before sending new command following software reset.
The display module loads all display suppliers’ factory default values to the registers during this 5 msec.
If Software Reset is applied during Sleep out mode, it will be necessary to wait 120 msec before sending Sleep out command.
Software Reset command cannot be sent during Sleep out sequence.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
</table>

01H	SWRESET (Software Reset)
Flow Chart	

5.1.3. READ DISPLAY IDENTIFICATION INFORMATION (04H)

<table>
<tr><th>04H</th><th colspan="12">RDDIDIF (Read Display Identification Information)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04</td></tr>
<tr><td>1st para</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd para</td><td>1</td><td>↑</td><td>1</td><td>ID17</td><td>ID16</td><td>ID15</td><td>ID14</td><td>ID13</td><td>ID12</td><td>ID11</td><td>ID10</td><td>-</td></tr>
<tr><td>3rd para</td><td>1</td><td>↑</td><td>1</td><td>ID27</td><td>ID26</td><td>ID25</td><td>ID24</td><td>ID23</td><td>ID22</td><td>ID21</td><td>ID20</td><td>-</td></tr>
<tr><td>4th para</td><td>1</td><td>↑</td><td>1</td><td>ID37</td><td>ID36</td><td>ID35</td><td>ID34</td><td>ID33</td><td>ID32</td><td>ID31</td><td>ID30</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">This read byte returns 24-bits display identification information.
The 1st Parameter is dummy data.
The 2nd Parameter (ID17 to ID10): LCD module’s manufacture ID.
The 3rd Parameter (ID27 to ID20): LCD module / driver version ID.
The 4th Parameter (ID37 to ID30): LCD module / driver.
Note: Commands RDID1 / RDID2 / RDID3 (DAh, DBh and DCh) read data correspond to the parameter 2, 3, 4 of the command 04h, respectively.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12">ID1, ID2 and ID3 default value<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>ID1</th><th>ID2</th><th>ID3</th></tr><tr><td>Power On Sequence</td><td>00h</td><td>00h</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td><td>00h</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td><td>00h</td><td>00h</td></tr></table></td></tr>
</table>

04H	RDDIDIF (Read Display Identification Information)
Flow Chart	

5.1.4. READ DISPLAY STATUS (09H)

09H	RDDST (Read Display Status)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	0	1	09
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D31	D30	D29	D28	D27	D26	0	0	xx
3rd para	1	↑	1	0	D22	D21	D20	D19	D18	D17	D16	xx
4th para	1	↑	1	D15	0	D13	0	0	D10	D9	D8	xx
5th para	1	↑	1	D7	D6	D5	0	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

The 1st Parameter is dummy data.

Bit	Description	Comment
D31	Step up circuit Voltage Status	
D30	Page Address Order	
D29	Column Address Order	
D28	Page/Column Order	
D27	Vertical Order	
D26	RGB/BGR Order	
D25	Not used	Set to ‘0’
D24	Not used	Set to ‘0’
D23	Not used	Set to ‘0’
D22	Interface Color Pixel Format Definition	
D21		
D20		
D19	Idle Mode On/Off	
D18	Partial Mode On/Off	
D17	Sleep In/Out	
D16	Display Normal Mode On/Off	
D15	Vertical Scroll Mode On/Off	
D14	Not used	Set to ‘0’
D13	Inversion Status	
D12	Not used	Set to ‘0’
D11	Not used	Set to ‘0’

09H	RDDST (Read Display Status)		
	D10	Display On/Off	
	D9	Tearing Effect Line On/Off	
	D8	Gamma Curve Selection	
	D7		
	D6		
	D5	Tearing Effect Output Line Mode	
	D4	Not used	Set to ‘0’
	D3	Not used	Set to ‘0’
	D2	Not used	Set to ‘0’
	D1	Not used	Set to ‘0’
	D0	Not used	Set to ‘0’

Bit Values are explained overleaf.

D31: Step up circuit Voltage status.

”0”: Step up circuit Off or has a fault.

”1”: Step up circuit On and working OK.

D30: Page Address Order.

“0”: Top to Bottom (When MADCTL B7 = ‘0’).

“1”: Bottom to Top (When MADCTL B7 = ‘1’).

D29: Column Address Order.

“0”: Left to Right (When MADCTL B6 = ‘0’).

“1”: Right to Left (When MADCTL B6 = ‘1’).

D28: Page/Column Order.

“0”: Normal Mode (When MADCTL B5 = ‘0’).

“1”: Reverse Mode (When MADCTL B5 = ‘1’).

D27: Line Address Order

“0”: LCD Refresh Top to Bottom (When MADCTL B4 = ‘0’).

“1”: LCD Refresh Bottom to Top (When MADCTL B4 = ‘1’).

D26: RGB/BGR Order

“0”: RGB (When MADCTL B3 = ‘0’).

“1”: BGR (When MADCTL B3 = ‘1’).

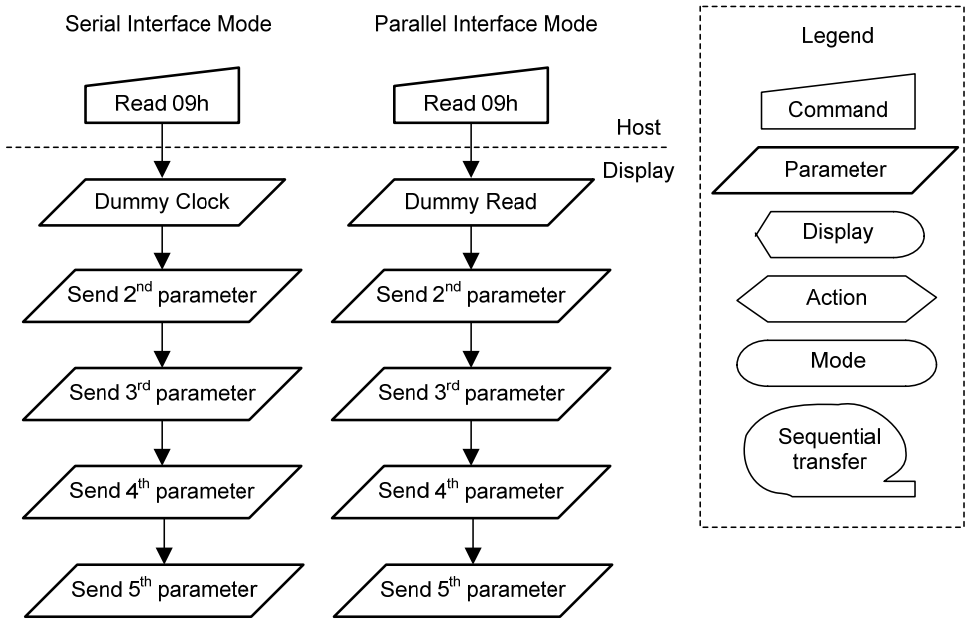
D25: Set to “0”

D24: Set to “0”

D23: Set to “0”

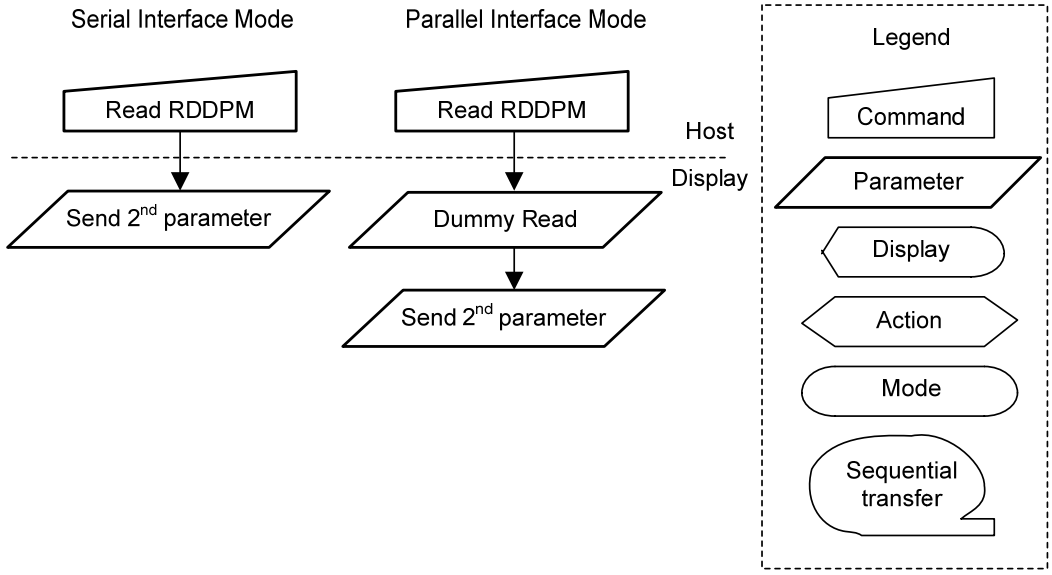
<table>
<tr><th>09H</th><th>RDDST (Read Display Status)</th></tr>
<tr><td></td><td>
D22, D21, D20: Interface Color Pixel Format Definition.
D19: Idle Mode On/Off
“0”: Idle Mode Off.
“1” : Idle Mode On.
D18: Partial Mode On/Off
“0”: Partial Mode Off.
“1” : Partial Mode On.
D17: Sleep In/Out
“0”: Sleep In Mode.
“1”: S0leep Out Mode.
D16: Display Normal Mode
“0”: Display Normal Mode Off.
“1”: Display Normal Mode On.
D15: Vertical Scroll Mode
“0”: Vertical Scroll Mode Off.
“1”: Vertical Scroll Mode On.
D14: Set to “0”
D13: Inversion Status
“0”: Inversion is Off.
“1”: Inversion is On.
D12: Set to “0”
D11: Set to “0”
D10: Display On/Off
“0”: Display is Off.
“1”: Display is On.
D9: Tearing Effect Line On/Off
“0”: Tearing Effect Line Off.
“1”: Tearing Effect Line On.
D8, D7, D6: Gamma Curve Selection
<table>
<tr><th>Gamma Curve Selected</th><th>D8</th><th>D7</th><th>D6</th><th>Gamma Set (26h) Parameter</th></tr>
<tr><td>Gamma Curve 1</td><td>0</td><td>0</td><td>0</td><td>GC0</td></tr>
<tr><td>Gamma Curve 2</td><td>0</td><td>0</td><td>1</td><td>GC1</td></tr>
<tr><td>Gamma Curve 3</td><td>0</td><td>1</td><td>0</td><td>GC2</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>09H</th><th>RDDST (Read Display Status)</th></tr>
<tr><td></td><td>
<table>
<tr><td>Gamma Curve 4</td><td>0</td><td>1</td><td>1</td><td>GC3</td></tr>
<tr><td>Not Defined</td><td>1</td><td>-</td><td>-</td><td>Not Defined</td></tr>
</table>
D5: Tearing Effect Line Output Mode
“0”: TE Mode1.
“1”: TE Mode2.
D4: Set to “0”
D3: Set to “0”
D2: Set to “0”
D1: Set to “0”
D0: Set to “0”
</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000 0000_0110 0001_0000 0000_0000 0000</td></tr>
<tr><td>S/W Reset</td><td>0xxx xx00_0xxx 0001_0000 0000_0000 0000</td></tr>
<tr><td>H/W Reset</td><td>0000 0000_0110 0001_0000 0000_0000 0000</td></tr>
</table>
</td></tr>
</table>

09H	RDDST (Read Display Status)
Flow Chart	

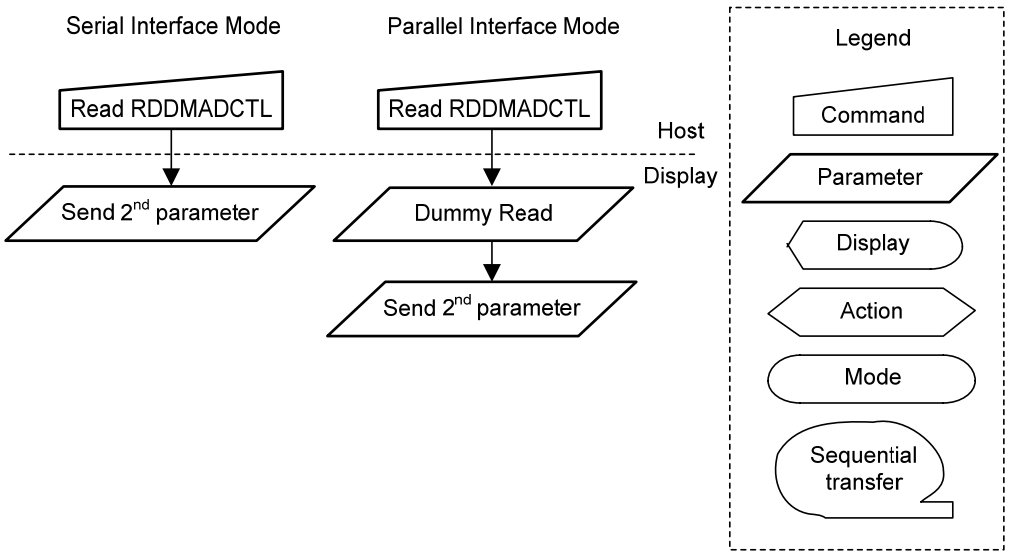
5.1.5. READ DISPLAY POWER MODE (0AH)

<table>
<tr><th>0AH</th><th colspan="12">RDDPM (Read Display Power Mode)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>1st para</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd para</td><td>1</td><td>↑</td><td>1</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>Step up circuit Voltage Status</td><td></td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td></td></tr>
<tr><td>D5</td><td>Partial Mode On/Off</td><td></td></tr>
<tr><td>D4</td><td>Sleep In/Out</td><td></td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td></td></tr>
<tr><td>D2</td><td>Display On/Off</td><td></td></tr>
<tr><td>D1</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>-</td><td>Set to ‘0’</td></tr>
</table>
Bit D7 : Step up circuit Voltage Status
“0”: Step up circuit Off or has a fault.
“1”: Step up circuit On and working OK (Meets optical requirements).
Bit D6 : Idle Mode On/Off
“0”: Idle Mode Off.
“1” : Idle Mode On.
Bit D5 : Partial Mode On/Off
“0”: Partial Mode Off.
“1”: Partial Mode On.
Bit D4 : Sleep In/Out
“0”: Sleep In Mode.
“1”: Sleep Out Mode.
Bit D3 : Display Normal Mode On/Off
“0”: Display Normal Mode Off.
“1”: Display Normal Mode On.
Bit D2 : Display On/Off
“0”: Display Off.</td></tr>
</table>

<table>
<tr><th>0AH</th><th>RDDPM (Read Display Power Mode)</th></tr>
<tr><td></td><td>“1”: Display On.
Bit D1, D0 : Set to ‘0’</td></tr>
<tr><td>Restrictions</td><td>There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>08HEX</td></tr>
<tr><td>S/W Reset</td><td>08HEX</td></tr>
<tr><td>H/W Reset</td><td>08HEX</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

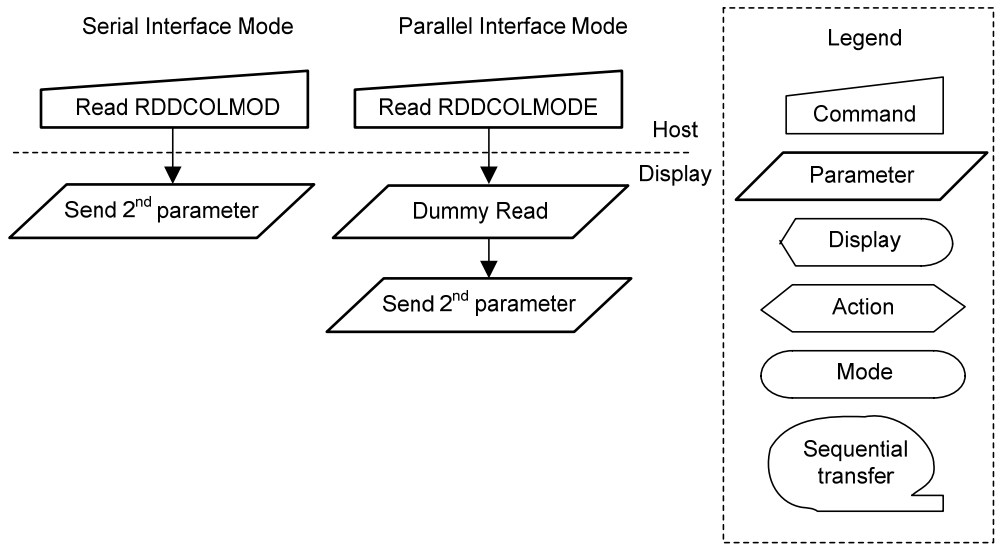
5.1.6. READ DISPLAY MADCTL (0BH)

<table>
<tr><th>0BH</th><th colspan="12">RDDMADCTL (Read Display MADCTL)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0B</td></tr>
<tr><td>1st para</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd para</td><td>1</td><td>↑</td><td>1</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>0</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td></td></tr>
<tr><td>D6</td><td>Column Address Order</td><td></td></tr>
<tr><td>D5</td><td>Page/Column Order</td><td></td></tr>
<tr><td>D4</td><td>Line Address Order</td><td></td></tr>
<tr><td>D3</td><td>RGB/BGR Order</td><td></td></tr>
<tr><td>D2</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D1</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>-</td><td>Set to ‘0’</td></tr>
</table>
Bit D7 : Page Address Order
“0”: Top to Bottom (When MADCTL B7=’0’).
“1”: Bottom to Top (When MADCTL B7=’1’).
Bit D6 : Column Address Order
“0”: Left to Right (When MADCTL B6=’0’).
“1”: Right to Left (when MADCTL B6=’1’).
Bit D5 : Page/column Order
“0”: Normal Mode (When MADCTL B5=’0’).
“1”: Reverse Mode (When MADCTL B5=’1’)
Bit D4 : Line Address Order
“0”: LCD Refresh Top to Bottom (When MADCTL B4=’0’).
“1”: LCD Refresh Bottom to Top (When MADCTL B4=’1’).
Bit D3 : RGB/BGR Order
“0”: RGB (When MADCTL B3=’0’).
“1”: BGR (When MADCTL B3=’1’).
Bit D2, D1, D0 : Set to ‘0’</td></tr>
<tr><td>Restrictions</td><td colspan="12">There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2</td></tr>
</table>

<table>
<tr><th>0BH</th><th>RDDMADCTL (Read Display MADCTL)</th></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00HEX</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>00HEX</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

5.1.7. READ DISPLAY PIXEL FORMAT (0CH)

<table>
<tr><th>0CH</th><th colspan="12">RDDCOLMOD (Read Display COLMOD)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0C</td></tr>
<tr><td>1st para</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd para</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>D2</td><td>D1</td><td>D0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>“0” (Not used)</td></tr>
<tr><td>D6</td><td rowspan="3">RGB Interface Color Format</td><td rowspan="3">“101”=16 bit/pixel
“110”=18 bit/pixel</td></tr>
<tr><td>D5</td></tr>
<tr><td>D4</td></tr>
<tr><td>D3</td><td>-</td><td>“0” (Not used)</td></tr>
<tr><td>D2</td><td rowspan="3">Control Interface Color Format</td><td rowspan="3">“101”=16 bit/pixel
“110”=18 bit/pixel</td></tr>
<tr><td>D1</td></tr>
<tr><td>D0</td></tr>
</table></td></tr>
<tr><td>Restrictions</td><td colspan="12">There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000_0110 (18 bit/pixel)</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>0000_0110 (18 bit/pixel)</td></tr>
</table></td></tr>
</table>

0CH	RDDCOLMOD (Read Display COLMOD)
Flow Chart	

5.1.8. READ DISPLAY IMAGE MODE (0DH)

0DH	RDDIM (Read Display Image Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	0	1	0D
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D7	0	D5	0	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit D7 : Vertical Scroll Mode On/Off

"0": Vertical Scroll Mode Off.

"1": Vertical Scroll Mode On.

Bit D6 : Set to '0'

Bit D5 : Inversion On/Off

"0": Inversion Off.

"1": Inversion On.

Bit D4 : Set to '0'

Bit D3 : Set to '0'

Bit D2, D1, D0 : Gamma Curve Selection

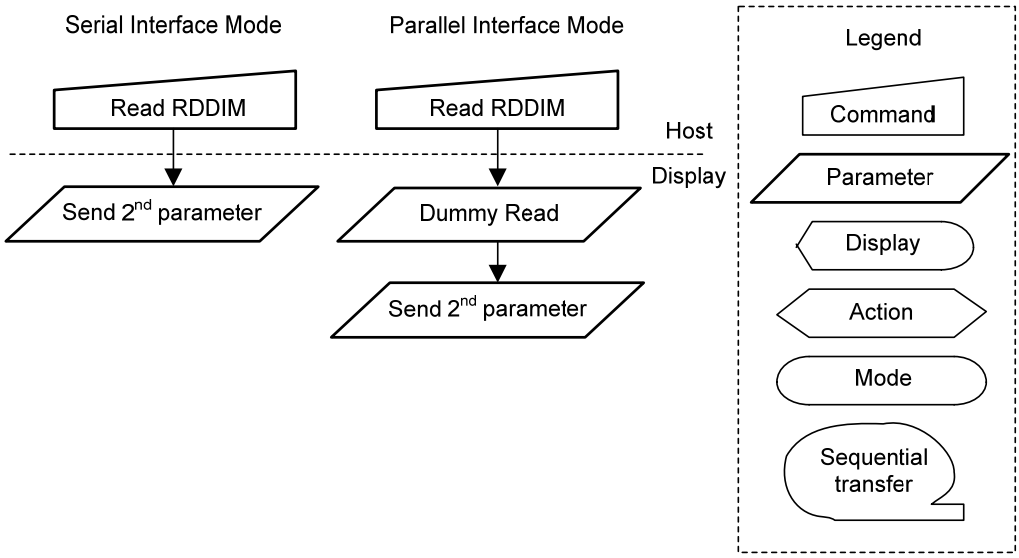
Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Restrictions

There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

<table>
<tr><th>0DH</th><th>RDDIM (Read Display Image Mode)</th></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00HEX</td></tr>
<tr><td>S/W Reset</td><td>00HEX</td></tr>
<tr><td>H/W Reset</td><td>00HEX</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

5.1.9. READ DISPLAY SIGNAL MODE (0EH)

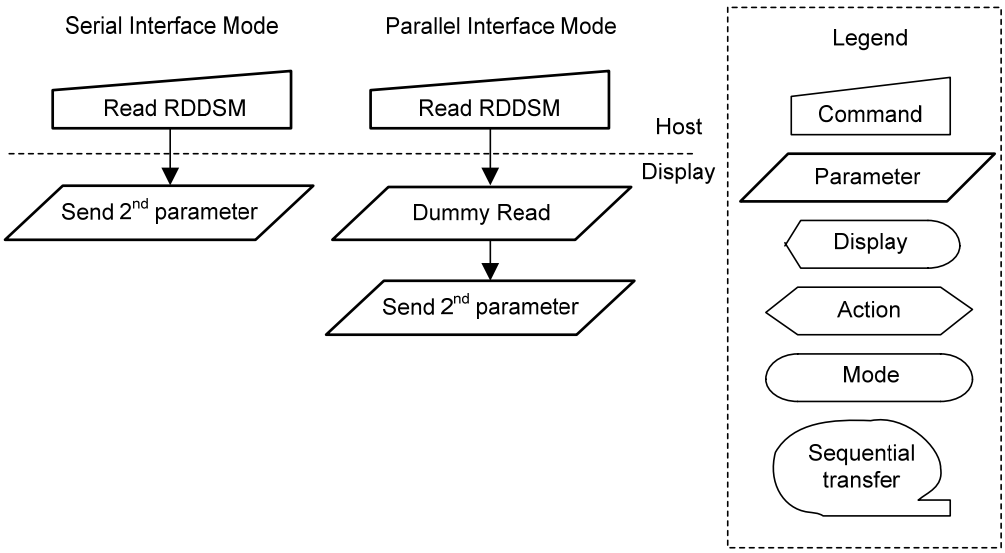
0EH	RDDSM (Read Display Signal Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	1	0	0E
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D7	D6	0	0	0	0	0	0	xx
Description	This command indicates the current status of the display as described in the table below: Bit D7 : Tearing Effect Line On/Off. "0": Tearing Effect Line Off. "1": Tearing Effect On. Bit D6 : Tearing Effect Line Output Mode. "0" : Mode 1. "1" : Mode 2. Bit D5 to D0 : Set to '0'											
Restrictions	There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2											

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
S/W Reset	00_{HEX}
H/W Reset	00_{HEX}

0EH	RDDSM (Read Display Signal Mode)
Flow Chart	

5.1.10. READ DISPLAY SELF-DIAGNOSTIC RESULT (0FH)

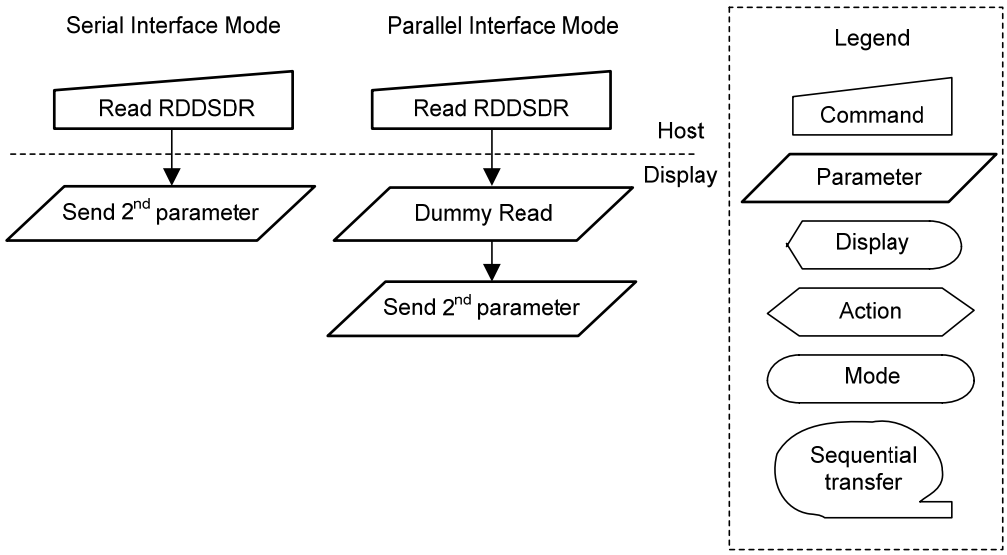
0FH	RDDSDR (Read Display Self-Diagnostic Result)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	1	1	0F
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	D7	D6	0	0	0	0	0	0	xx
Description	This command indicates the status of the display self-diagnostic result after Sleep Out command as described in the table below: Bit D7 : Register Loading Detection Bit D6 : Functionality Detection Bit D5 to D0 : Set to “0”											
Restrictions	There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2											

Register Availability

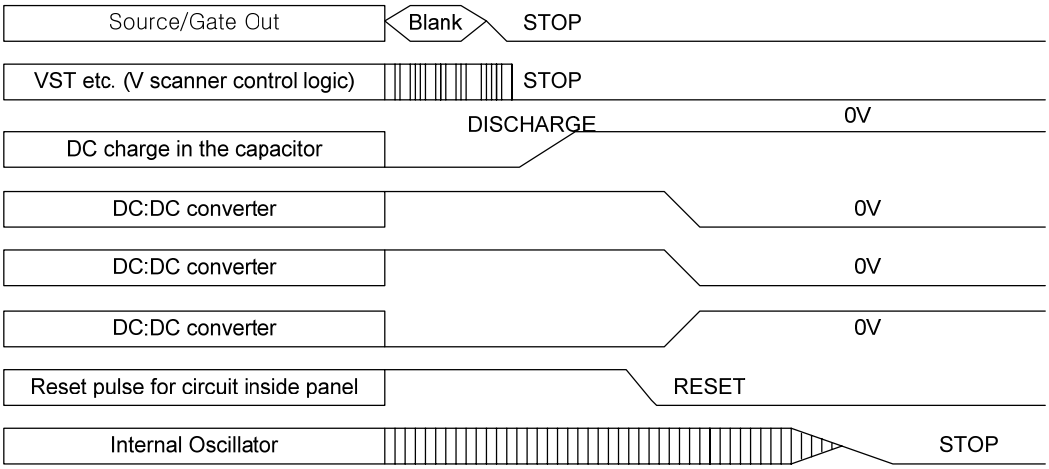
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
S/W Reset	00_{HEX}
H/W Reset	00_{HEX}

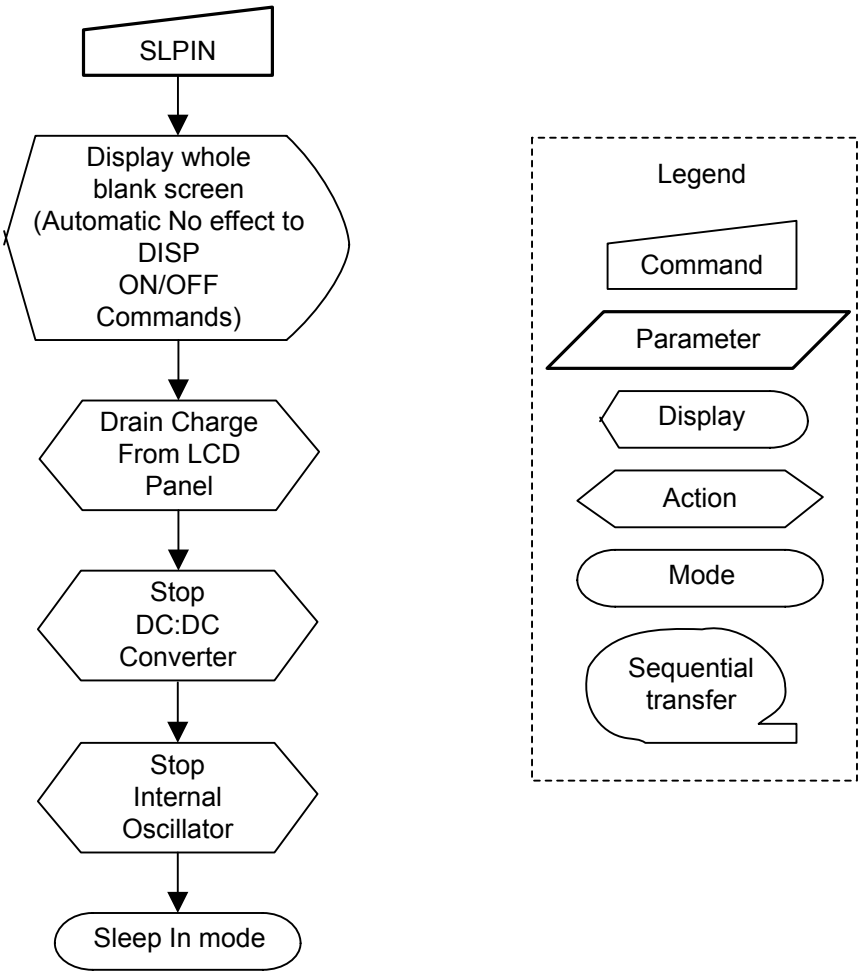
0FH	RDDSDR (Read Display Self-Diagnostic Result)
Flow Chart	

5.1.11. SLEEP IN (10H)

10H	SLPIN (Sleep In)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	0	0	10
Parameter	NO PARAMETER											
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  MPU interface and memory are still working and the memory keeps its contents.											
Restriction	This command has no effect when module is already in Sleep In mode. Sleep In mode can only be left by the Sleep Out command (11h). It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In mode) before Sleep In command can be sent.											

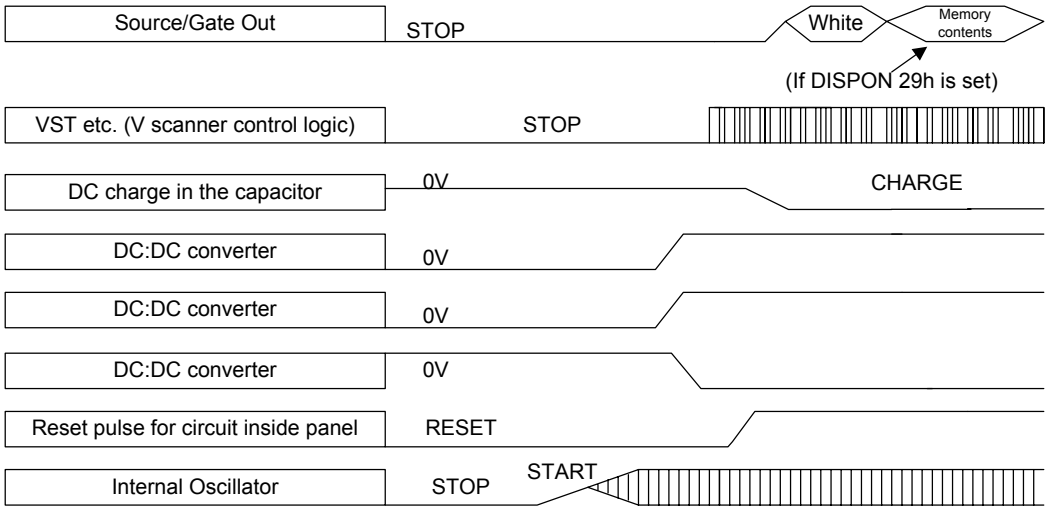
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

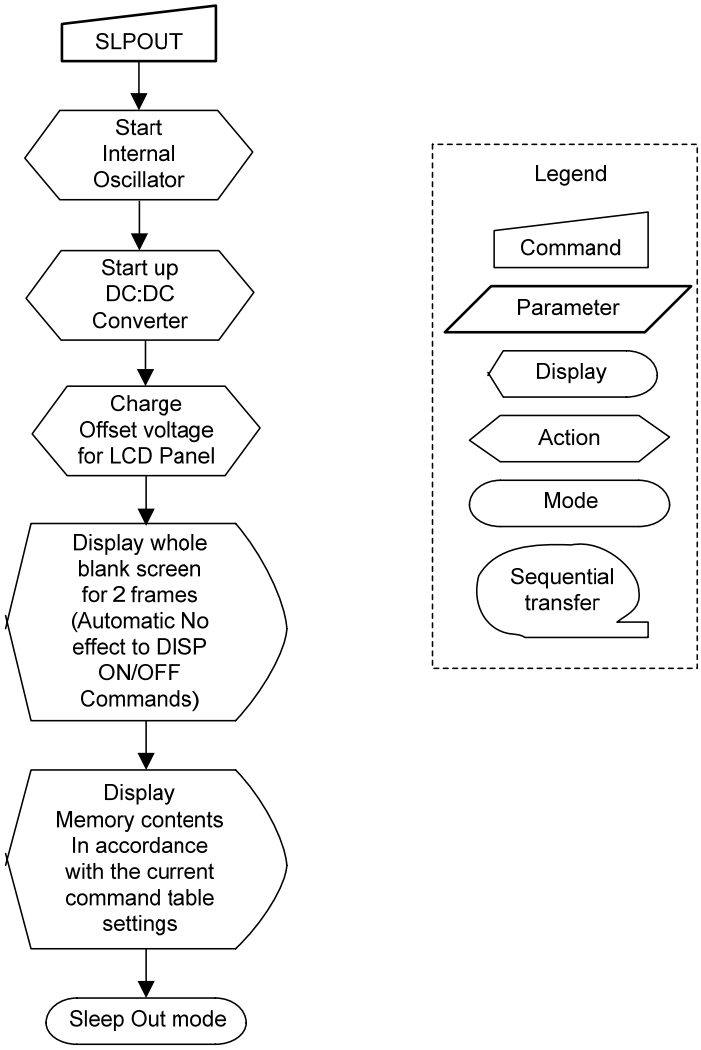
<table>
<tr><th>10H</th><th>SLPIN (Sleep In)</th></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr>
<tr><td>S/W Reset</td><td>Sleep In Mode</td></tr>
<tr><td>H/W Reset</td><td>Sleep In Mode</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


It takes 120msec to get into Sleep In mode after SLPIN command issued.
</td></tr>
</table>

5.1.12. SLEEP OUT (11H)

11H	SLPOUT (Sleep Out)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER											
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  											
Restriction	This command has no effect when module is already in Sleep Out mode, Sleep Out Mode can only be left by the Sleep In command (10h) It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done when the display module is already Sleep Out mode. The display module is doing self-diagnostic function during this 5msec. See also section "Sleep Out Command and Self-Diagnostic Functions of the Display Module". It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.											

<table>
<tr><th>11H</th><th>SLPOUT (Sleep Out)</th></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr>
<tr><td>S/W Reset</td><td>Sleep In Mode</td></tr>
<tr><td>H/W Reset</td><td>Sleep In Mode</td></tr>
</table>
</td></tr>
</table>

11H	SLPOUT (Sleep Out)
Flow Chart	 It takes 120msec to become Sleep Out mode after SLPOUT command issued.

5.1.13. PARTIAL MODE ON (12H)

12H	PTLON (Partial Mode On)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	1	0	12
Parameter	NO PARAMETER											
Description	This command turns on partial mode. The partial mode window is described by the Partial Area command (30h). To leave Partial mode, the Normal Display Mode command (13h) should be written.											
Restriction	This command has no effect when Partial mode is active.											

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

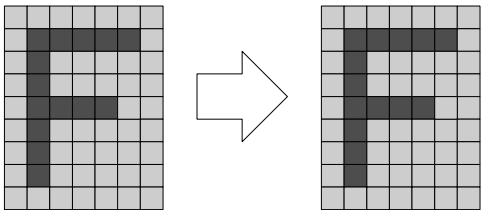
Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

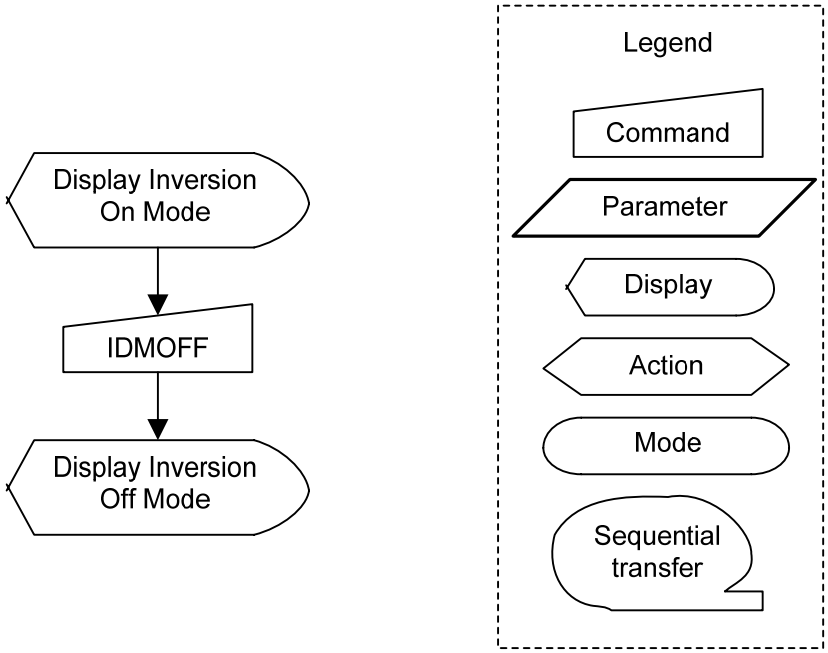
Flow Chart: See Partial Area (30h)

5.1.14. NORMAL DISPLAY MODE ON (13H)

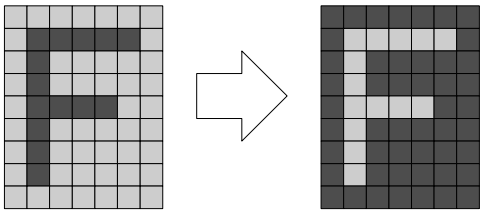
<table>
<tr><th>13 H</th><th colspan="12">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command returns the display to normal mode.
Normal Display Mode On means Partial mode off.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area Descriptions for details when use this command</td></tr>
</table>

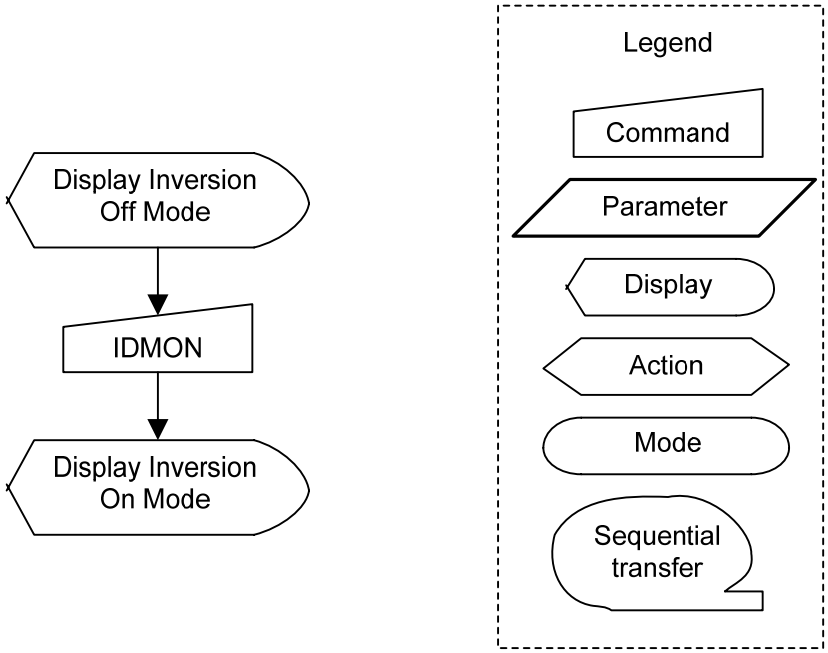
5.1.15. DISPLAY INVERSION OFF (20H)

<table>
<tr><th>20H</th><th colspan="12">INVOFF (Display Inversion Off)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>20</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status
(Example)
Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in inversion off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table></td></tr>
</table>

20H	INVOFF (Display Inversion Off)
Flow Chart	

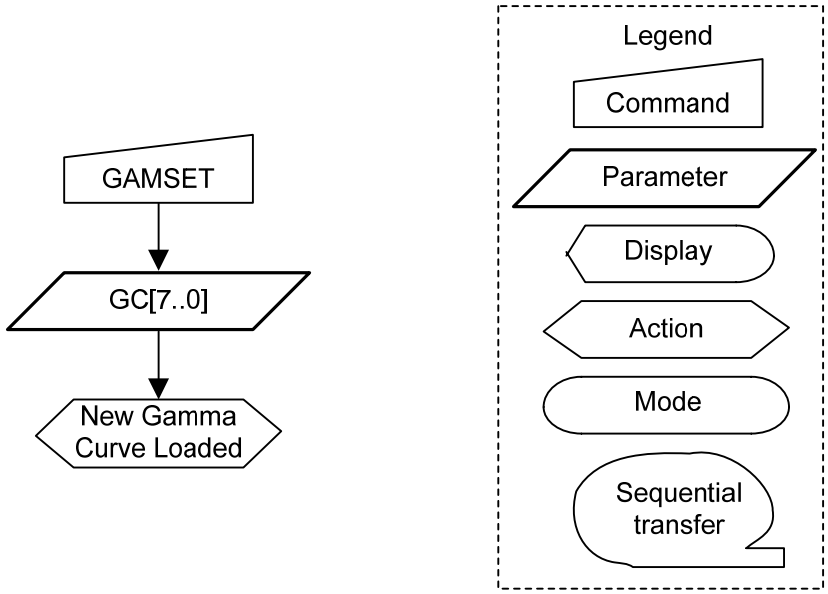
5.1.16. DISPLAY INVERSION ON (21H)

<table>
<tr><th>21H</th><th colspan="12">INVON (Display Inversion On)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into display inversion mode.
This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.
This command does not change any other status.
(Example)
Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in inversion on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table></td></tr>
</table>

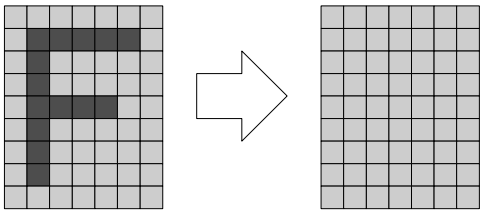
21H	INVON (Display Inversion On)
Flow Chart	

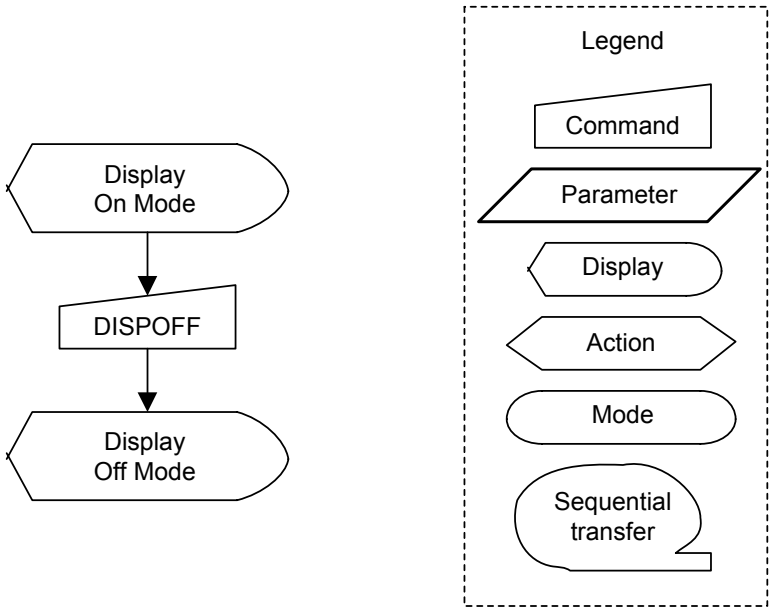
5.1.17. GAMMA SET (26H)

<table>
<tr><th>26H</th><th colspan="12">GAMSET (Gamma Set)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>26</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>GC7</td><td>GC6</td><td>GC5</td><td>GC4</td><td>GC3</td><td>GC2</td><td>GC1</td><td>GC0</td><td>Note</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to select the desired Gamma curve for the current display.
A maximum of 4 curves can be selected. Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:
<table>
<tr><th>GC[7..0]</th><th>Parameter</th><th>Curve Selected</th></tr>
<tr><td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr>
<tr><td>02h</td><td>GC1</td><td>Gamma Curve 2</td></tr>
<tr><td>04h</td><td>GC2</td><td>Gamma Curve 3</td></tr>
<tr><td>08h</td><td>GC3</td><td>Gamma Curve 4</td></tr>
</table>
Note.
All other values are undefined.</td></tr>
<tr><td>Restriction</td><td colspan="12">Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>01h</td></tr>
<tr><td>S/W Reset</td><td>01h</td></tr>
<tr><td>H/W Reset</td><td>01h</td></tr>
</table></td></tr>
</table>

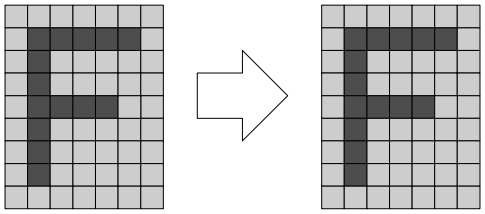
26H	GAMSET (Gamma Set)
Flow Chart	

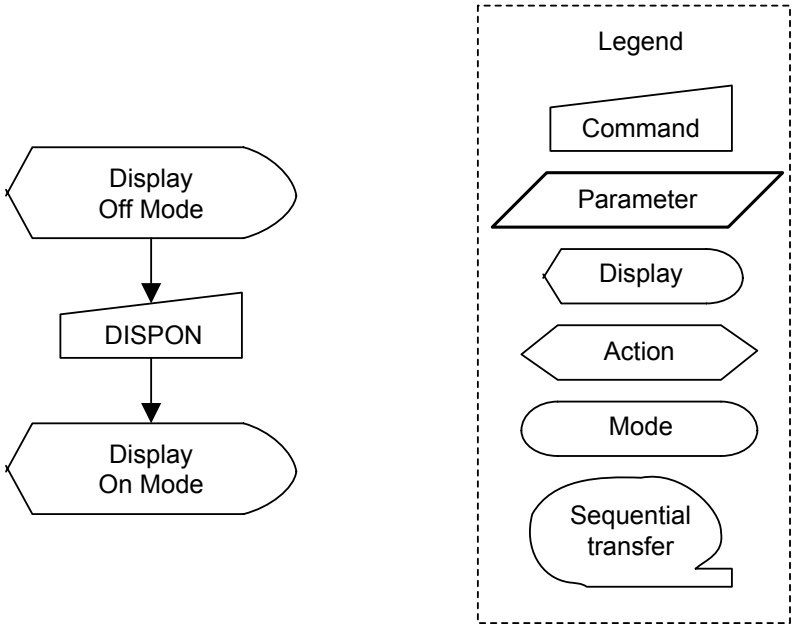
5.1.18. DISPLAY OFF (28H)

<table>
<tr><th>28H</th><th colspan="12">DISPOFF (Display Off)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into Display Off mode.
In this mode, the output from Frame Memory is disabled and blank page is inserted.
This command is makes No Change of contents of frame memory
This command does not change any other status.
There will be no abnormal visible effect on the display
(Example)
Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table></td></tr>
</table>

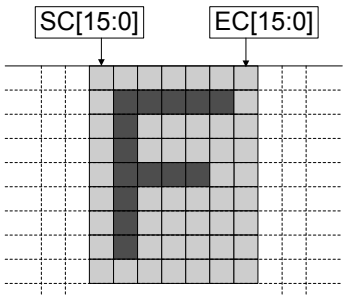
28H	DISPOFF (Display Off)
Flow Chart	

5.1.19. DISPLAY ON (29H)

<table>
<tr><th>29H</th><th colspan="12">DISPON (Display On)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to recover from Display Off Mode. Output from the Frame Memory is enabled.
This command makes No Change of contents of frame memory
This command does not change any other status.
(Example)
Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table></td></tr>
</table>

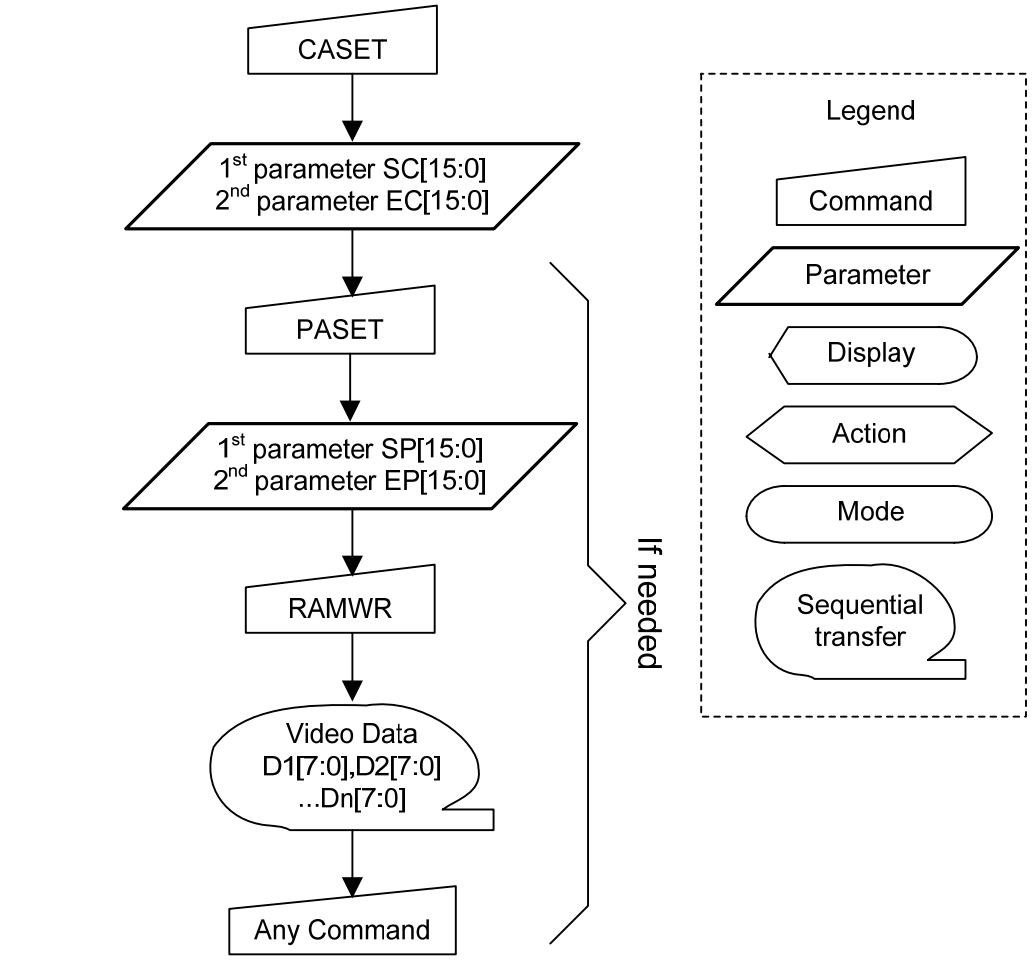
29H	DISPON (Display On)
Flow Chart	

5.1.20. COLUMN ADDRESS SET (2AH)

2AH	CASET (Column Address Set)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	1	0	2A
1st para	1	1	↑	SC[15]	SC[14]	SC[13]	SC[12]	SC[11]	SC[10]	SC[9]	SC[8]	Note
2nd para	1	1	↑	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]	
3rd para	1	1	↑	EC[15]	EC[14]	EC[13]	EC[12]	EC[11]	EC[10]	EC[9]	EC[8]	Note
4th para	1	1	↑	EC[7]	EC[6]	EC[5]	EC[4]	EC[3]	EC[2]	EC[1]	EC[0]	
Description	This command is used to define area of frame memory where MPU can access. This command makes No Change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory. (Example) 											
Restriction	SC[15:0] always must be equal to or less than EC[15:0]. When SC[15:0] or EC[15:0] is greater than maximum address as below, data of out of range will be ignored. **Note.** (Parameter range: 0 ≤ SC[15:0], EC[15:0] ≤ 239 (00EFh) (B5=0) (Parameter range: 0 ≤ SC[15:0], EC[15:0] ≤ 319 (013Fh) (B5=1)											

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

<table>
<tr><th>2AH</th><th>CASET (Column Address Set)</th></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>SC[15:0]=0000h</td><td>EC[15:0]=00EFh</td></tr>
<tr><td>S/W Reset</td><td>When MADCTL’s B5=0:
SC[15:0]=0000h
When MADCTL’s B5=1:
SC[15:0]=0000h</td><td>When MADCTL’s B5=0:
EC[15:0]=00EFh
When MADCTL’s B5=1:
EC[15:0]=013Fh</td></tr>
<tr><td>H/W Reset</td><td>SC[15:0]=0000h</td><td>EC[15:0]=00EFh</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

5.1.21. PAGE ADDRESS SET (2BH)

2BH	PASET (Page Address Set)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	1	1	2B
1st para	1	1	↑	SP[15]	SP[14]	SP[13]	SP[12]	SP[11]	SP[10]	SP[9]	SP[8]	Note
2nd para	1	1	↑	SP[7]	SP[6]	SP[5]	SP[4]	SP[3]	SP[2]	SP[1]	SP[0]	
3rd para	1	1	↑	EP[15]	EP[14]	EP[13]	EP[12]	EP[11]	EP[10]	EP[9]	EP[8]	Note
4th para	1	1	↑	EP[7]	EP[6]	EP[5]	EP[4]	EP[3]	EP[2]	EP[1]	EP[0]	

Description

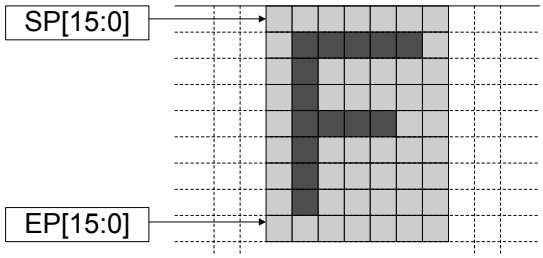
This command is used to define area of frame memory where MPU can access.

This command makes No Change on the other driver status.

The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.

Each value represents one Page line in the Frame Memory.

(Example)



Restriction

SP[15:0] always must be equal to or less than EP[15:0]. When SP[15:0] or EP[15:0] is greater than maximum address as below, data of out of range will be ignored.

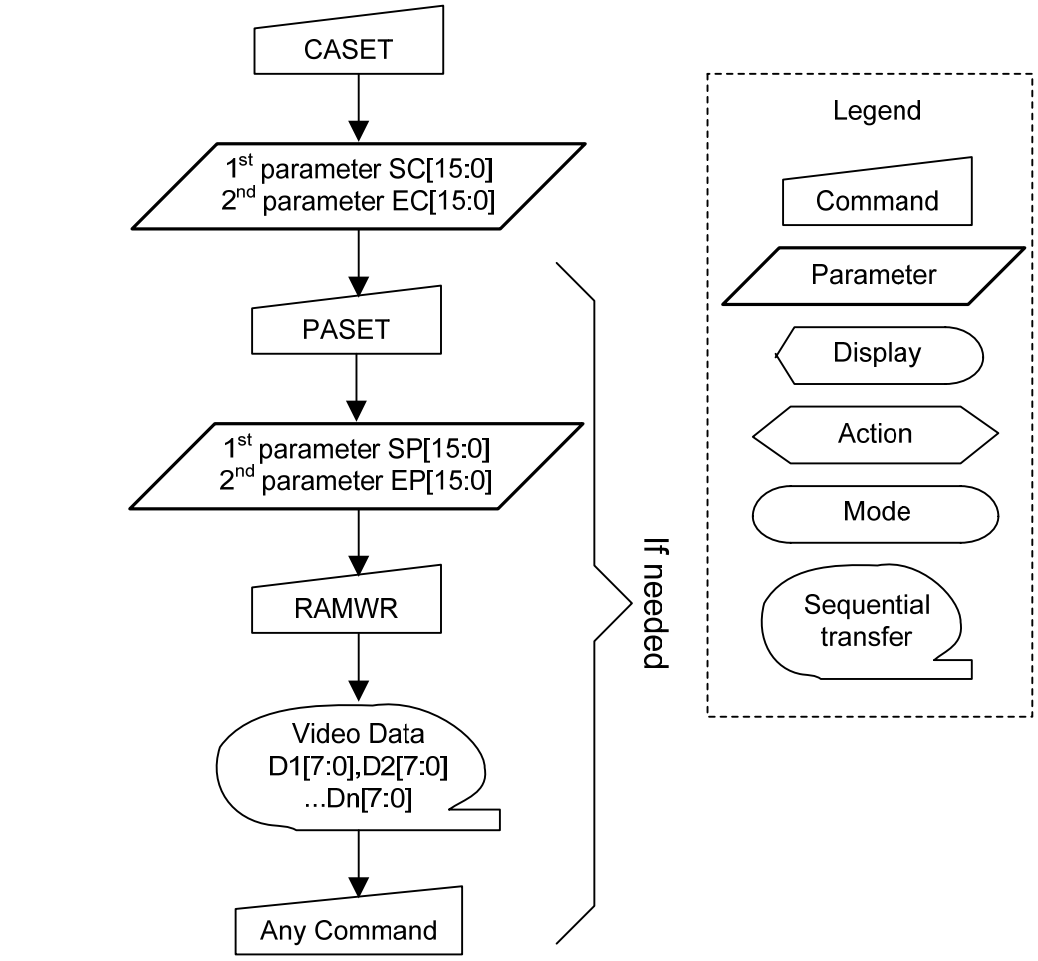
Note.

(Parameter range: 0 ≤ SP[15:0], EP[15:0] ≤ 319 (013Fh) (B5=0)

(Parameter range: 0 ≤ SP[15:0], EP[15:0] ≤ 239 (00EFh) (B5=1)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

<table>
<tr><th>2BH</th><th>PASET (Page Address Set)</th></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>SC[15:0]=0000h</td><td>EC[15:0]=01AFh</td></tr>
<tr><td>S/W Reset</td><td>When MADCTL’s B5=0:
SC[15:0]=0000h
When MADCTL’s B5=1:
SC[15:0]=0000h</td><td>When MADCTL’s B5=0:
EC[15:0]=013Fh
When MADCTL’s B5=1:
EC[15:0]=00EFh</td></tr>
<tr><td>H/W Reset</td><td>SC[15:0]=0000h</td><td>EC[15:0]=013Fh</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

5.1.22. MEMORY WRITE (2CH)

2CH	RAMWR (Memory Write)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	1	0	0	2C
1st para	1	1	↑	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00..FF
:	1	1	↑	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00..FF
Nth para	1	1	↑	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00..FF

Description

This command is used to transfer data from MPU to frame memory.

This command makes No Change to the other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column/Start Page position.

The Start Column/Start Page positions are different in accordance with MADCTL setting. Then D[7:0] is stored in frame memory and the column register and the page register incremented.

Sending any other command can stop frame Write.

Restriction

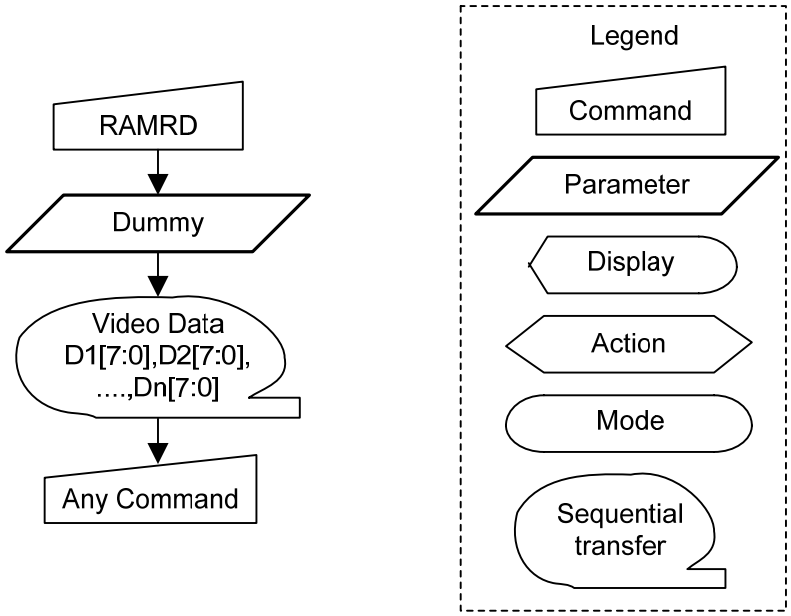
In all color modes, there is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

2CH	RAMWR (Memory Write)
Flow Chart	

5.1.23. MEMORY READ (2EH)

2EH	RAMRD (Memory Read)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	1	1	0	2E
1st para	1	↑	1	X	X	X	X	X	X	X	X	00..FF
:	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00..FF
(N+1)th para	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00..FF

Description

This command is used to transfer data from frame memory to MPU.

This command makes No Change to the other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column / Start Page position.

The Start Column / Start positions are different in accordance with MADCTL setting.

Then D[7:0] is read back from the frame memory and the column register and the page register incremented. Frame memory read can be stopped by sending any other command.

Restriction

In all color modes, the frame memory read is always 18bit, so there is no restriction on length of parameters.

Note.

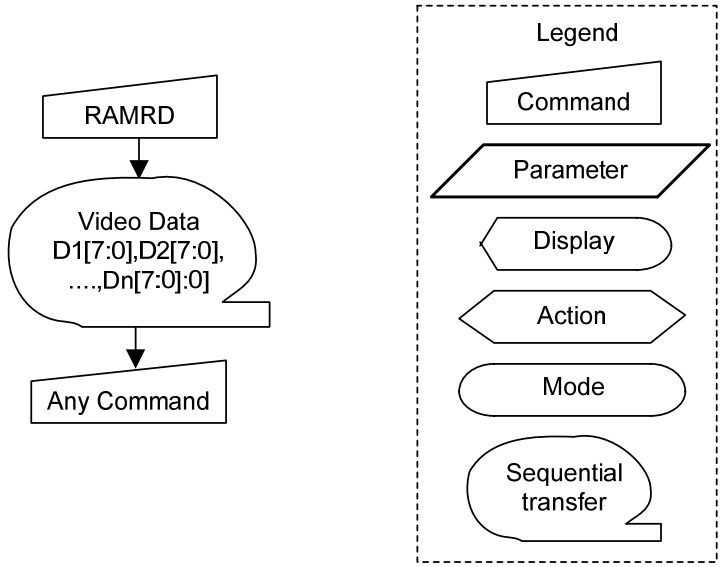
Frame memory read is only possible via the Parallel Interface.

Register Availability

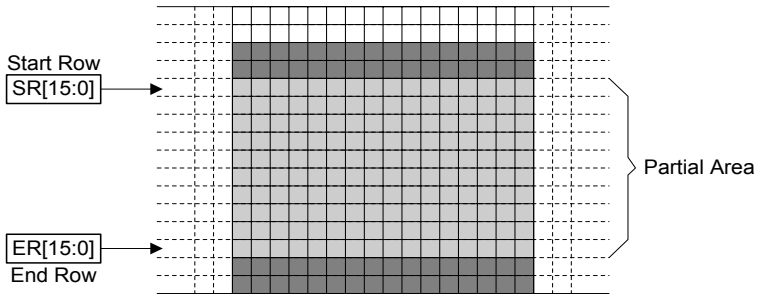
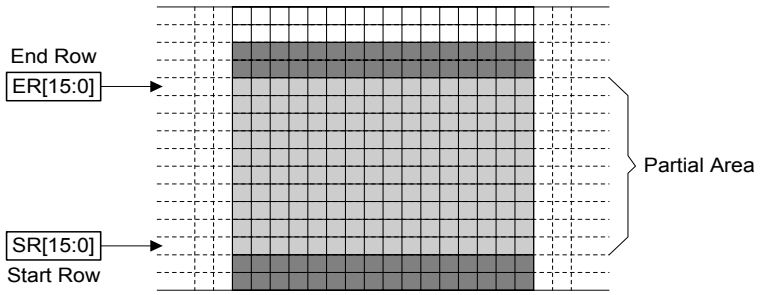
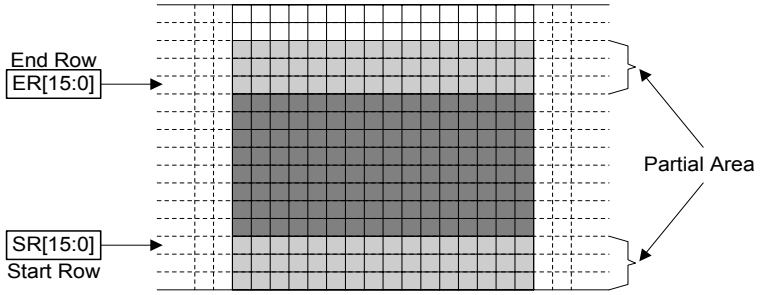
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

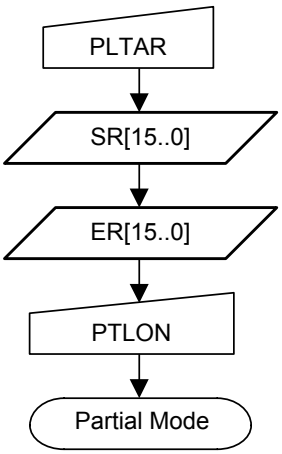
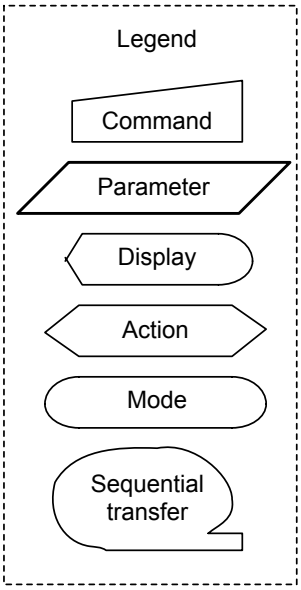
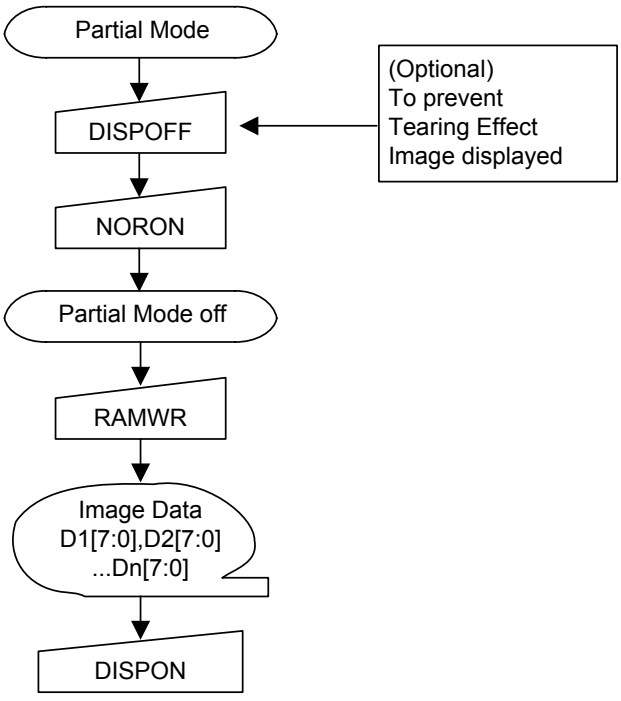
Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

2EH	RAMRD (Memory Read)
Flow Chart	

5.1.24. PARTIAL AREA (30H)

30H	PLTAR (Partial Area)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	0	0	30
1st para	1	1	↑	SR[15]	SR[14]	SR[13]	SR[12]	SR[11]	SR[10]	SR[9]	SR[8]	0000..
2nd para	1	1	↑	SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]	013F
3rd para	1	1	↑	ER[15]	ER[14]	ER[13]	ER[12]	ER[11]	ER[10]	ER[9]	ER[8]	0000..
4th para	1	1	↑	ER[7]	ER[6]	ER[5]	ER[4]	ER[3]	ER[2]	ER[1]	ER[0]	013F
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row(SR) and the second defines the End Row(ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row When MADCTL B4=0:  If End Row>Start Row When MADCTL B4=1:  If End Row<Start Row When MADCTL B4=0:  If End Row=Start Row then the Partial Area will be one row deep.											

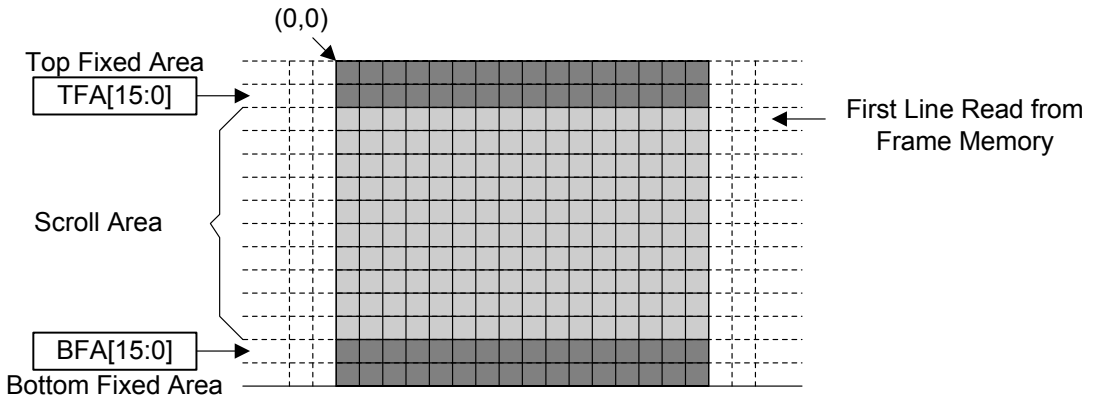
<table>
<tr><th>30H</th><th>PLTAR (Partial Area)</th></tr>
<tr><td>Restriction</td><td>Each detail initial values by the display resolution will be updated.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>SR[15:0]=0000h ER[15:0]=013Fh</td></tr>
<tr><td>H/W Reset</td><td>SR[15:0]=0000h ER[15:0]=013Fh</td></tr>
<tr><td>H/W Reset</td><td>SR[15:0]=0000h ER[15:0]=013Fh</td></tr>
</table>
</td></tr>
</table>

30H	PLTAR (Partial Area)
Flow Chart	1. To enter Partial Mode:   2. To exit Partial Mode: 

5.1.25. VERTICAL SCROLLING DEFINITION (33H)

33 H	VSCRDEF (Vertical Scrolling Definition)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	TFA [15]	TFA [14]	TFA [13]	TFA [12]	TFA [11]	TFA [10]	TFA [9]	TFA [8]	0000 …. 013F
2nd parameter	1	1	↑	TFA [7]	TFA [6]	TFA [5]	TFA [4]	TFA [3]	TFA [2]	TFA [1]	TFA [0]	
3rd parameter	1	1	↑	VSA [15]	VSA [14]	VSA [13]	VSA [12]	VSA [11]	VSA [10]	VSA [9]	VSA [8]	0000 …. 013F
4th parameter	1	1	↑	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]	
5th parameter	1	1	↑	BFA [15]	BFA [14]	BFA [13]	BFA [12]	BFA [11]	BFA [10]	BFA [9]	BFA [8]	0000 …. 013F
6th parameter	1	1	↑	BFA [7]	BFA [6]	BFA [5]	BFA [4]	BFA [3]	BFA [2]	BFA [1]	BFA [0]	
Description	This command defines the Vertical Scrolling Area of the display. (refer to Restriction) When MADCTL B4 = 0 The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. Of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area(in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.											

33 H	VSCRDEF (Vertical Scrolling Definition)



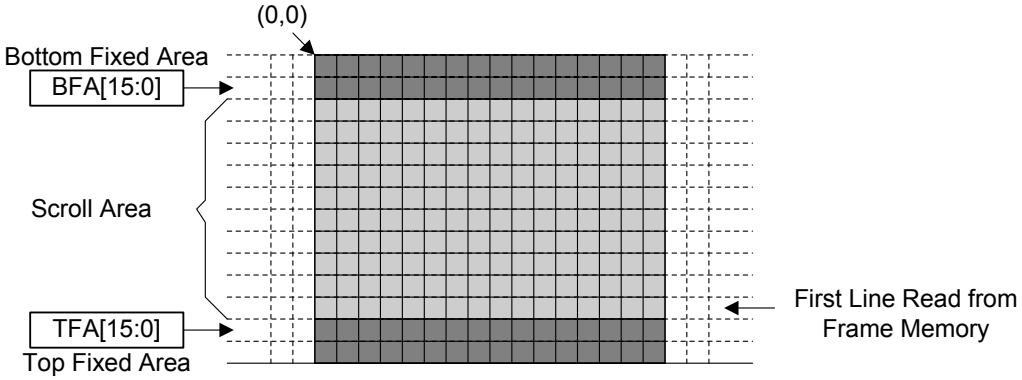
When MADCTL B4 = 1

The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area(in No. of lines from Top of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Restriction	**Note.** The condition is (TFA+VSA+BFA)≥320, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to “0” – this only affects the Frame Memory Write.

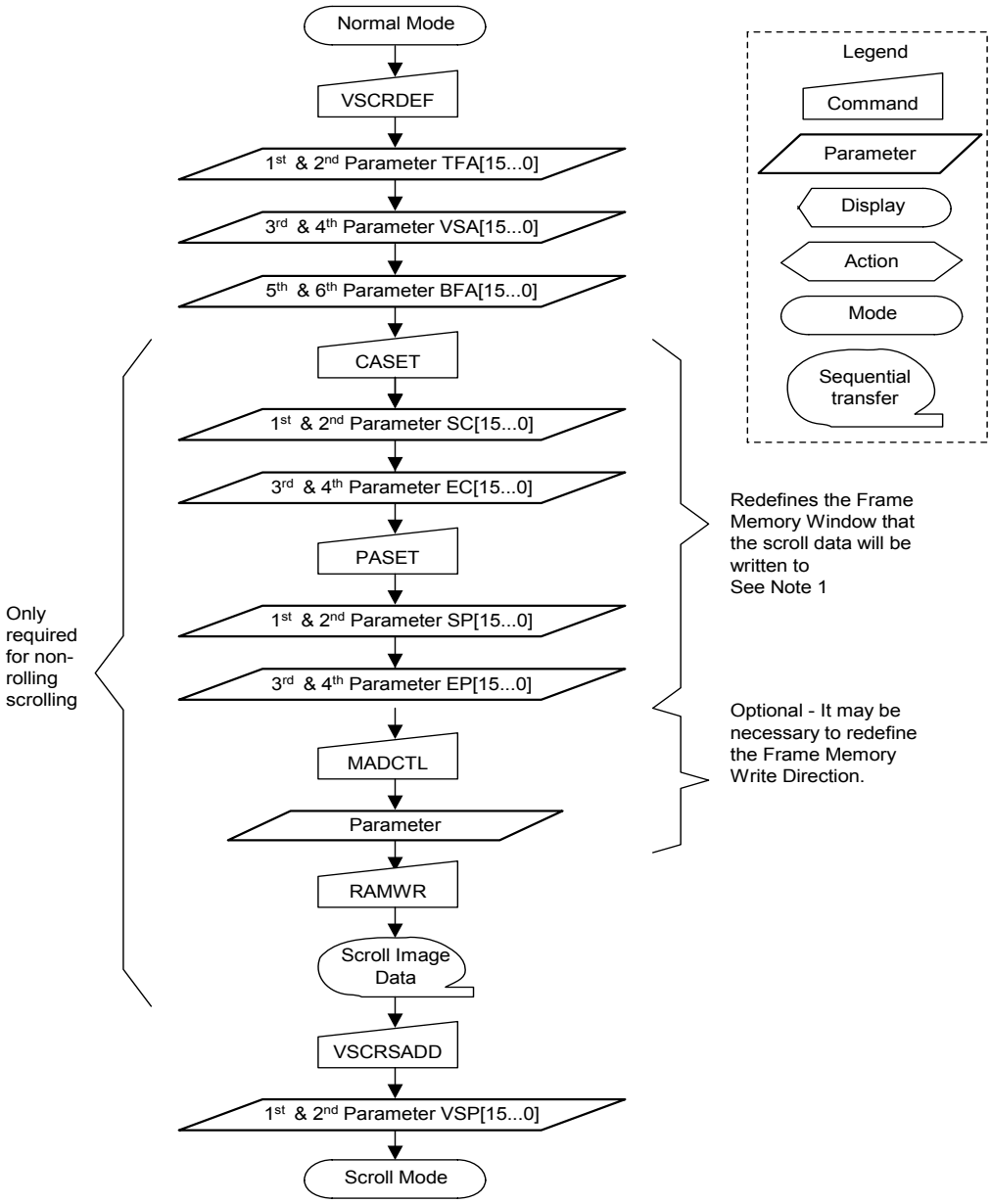
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes

33 H	VSCRDEF (Vertical Scrolling Definition)	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

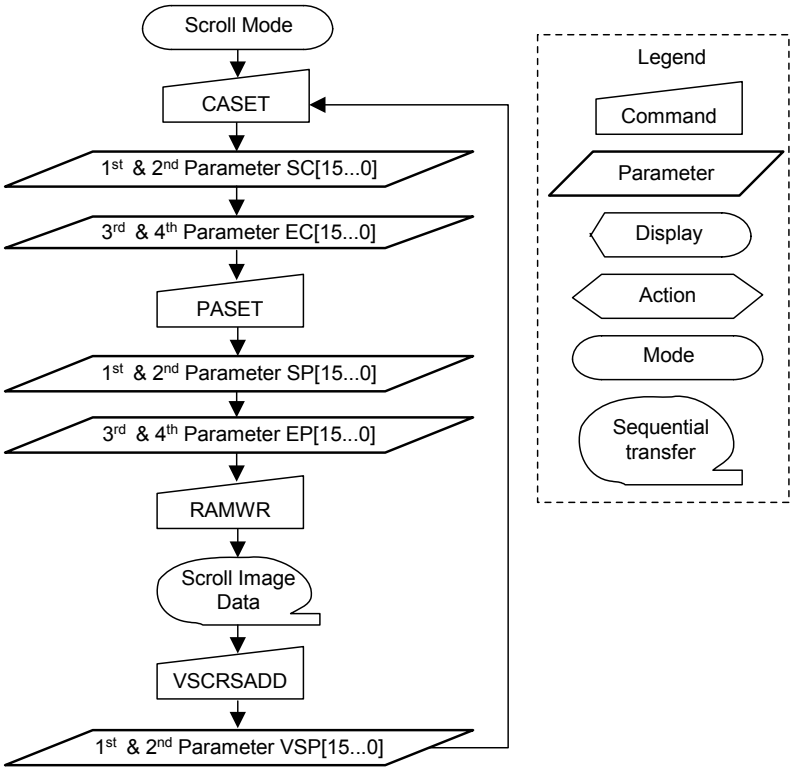
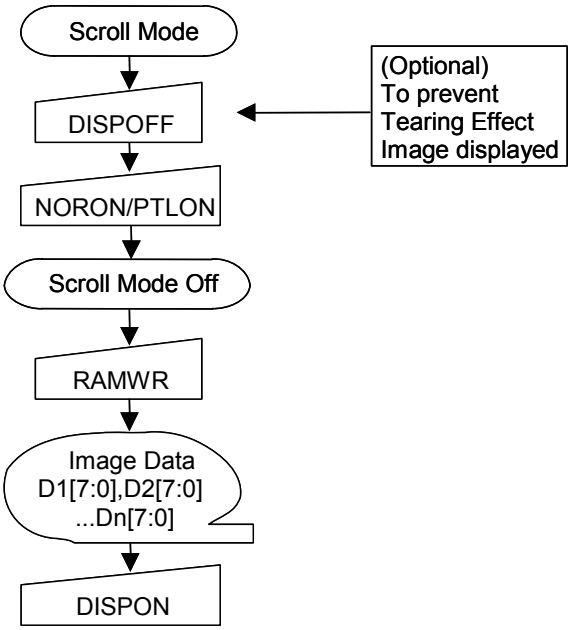
Flow Chart

To enter Vertical Scroll Mode:

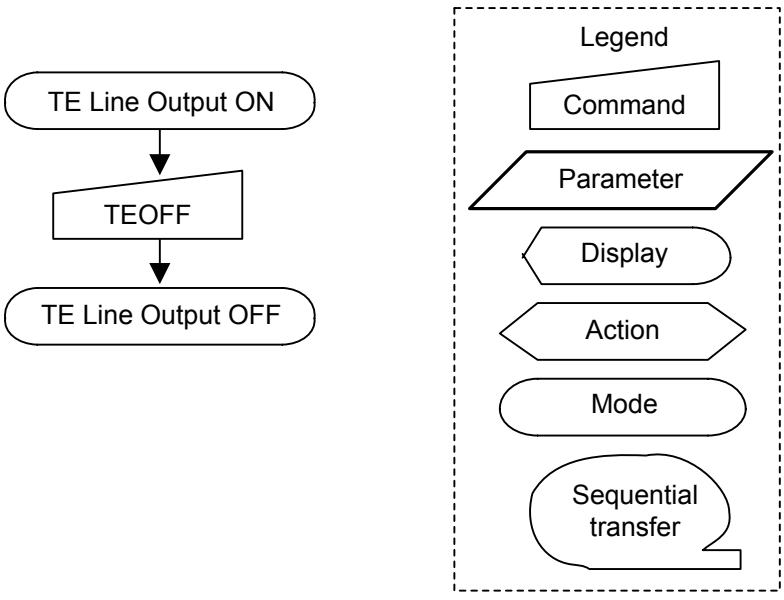


Note.

The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed

33 H	VSCRDEF (Vertical Scrolling Definition)
Flow Chart	Continuous Scroll:  To leave Vertical Scroll Mode:  **Note.** Scroll Mode can be exit by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

5.1.26. TEARING EFFECT LINE OFF (34H)

<table>
<tr><th>34 H</th><th colspan="12">TEOFF (Tearing Effect Line OFF)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to turn Off (Active Low) the Tearing Effect output signal from TE signal line.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Tearing Effect output is already Off.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>S/W Reset</td><td>Off</td></tr><tr><td>H/W Reset</td><td>Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

5.1.27. TEARING EFFECT LINE ON (35H)

35 H	TEON (Tearing Effect Line ON)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	X	X	X	X	X	X	X	M	xx

Description

This command is used to turn On the Tearing Effect output signal from the TE signal line.

This output is not affected by changing Memory Address Control command bit “B4”.

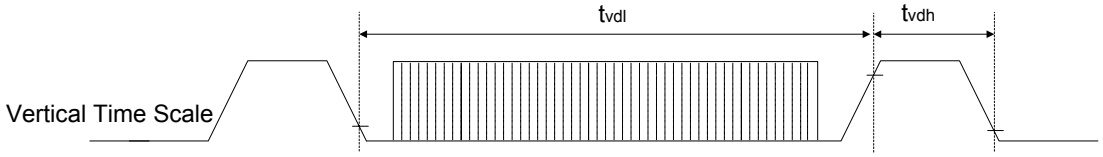
The Tearing Effect Line On has one parameter that describes the mode of the Tearing Effect Output Line. (X = don’t care).

When M=0:

The Tearing Effect Output line consists of V-Blanking information only:

When M=1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



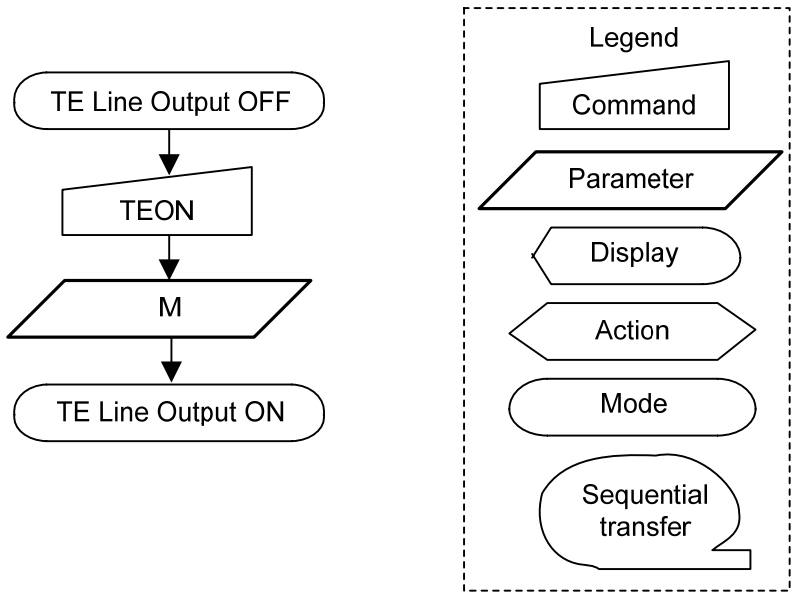
During Sleep In mode with Tearing Effect Line On, Tearing Effect output pin will be active low.

Restriction

This command has no effect when Tearing Effect output is already On.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

<table>
<tr><th>35 H</th><th>TEON (Tearing Effect Line ON)</th></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Off</td></tr>
<tr><td>S/W Reset</td><td>Off</td></tr>
<tr><td>H/W Reset</td><td>Off</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

5.1.28. MEMORY DATA ACCESS CONTROL (36H)

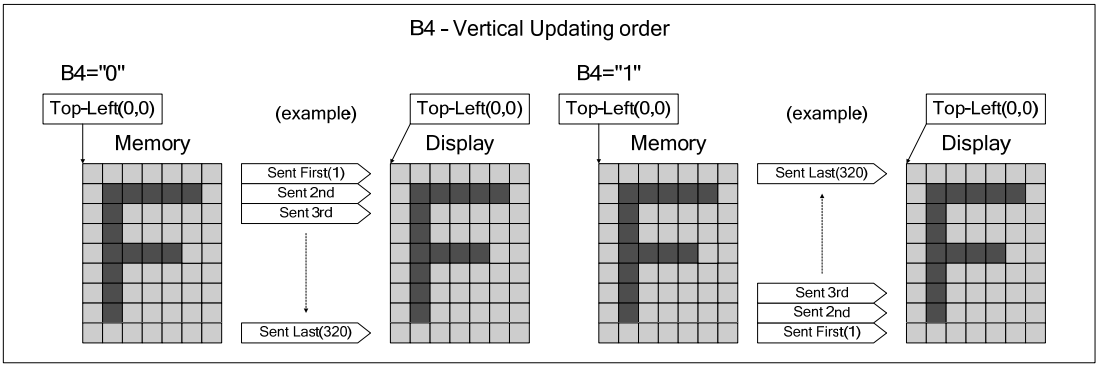
36 H	MADCTL (Memory Data Access Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	0	36
parameter	1	1	↑	B7	B6	B5	B4	B3	X	X	X	xx

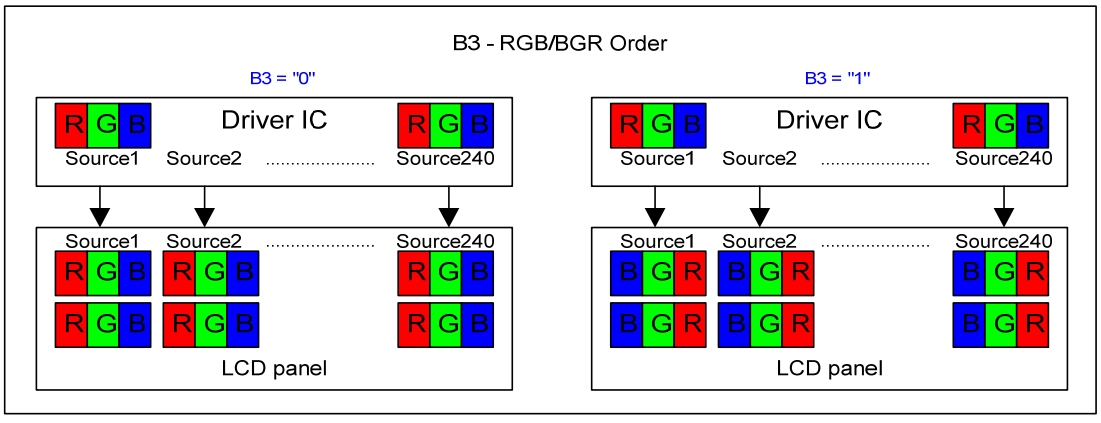
Description

This command defines read/write scanning direction of frame memory.

This command makes No Change on the other driver status.

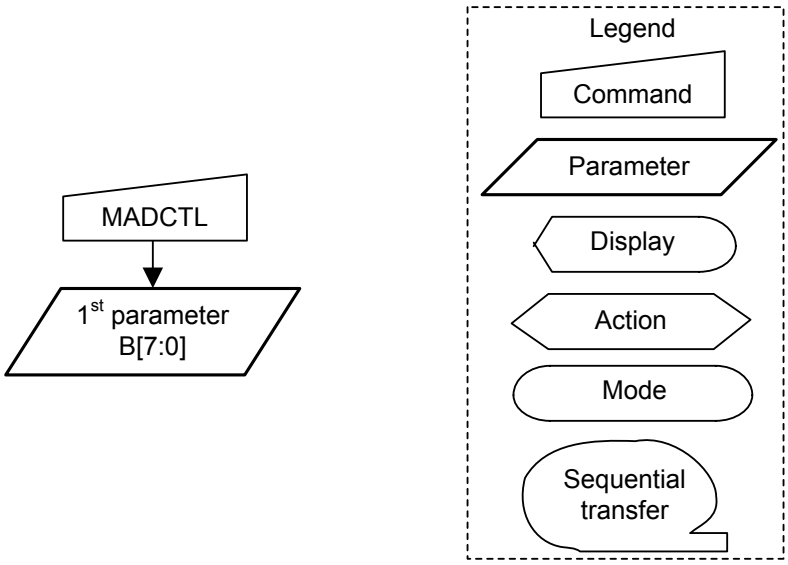
Bit	Name	Description
B7	Page Address Order	These 3 bits control MPU to memory write/read Direction.
B6	Column Address Order	
B5	Page/Column Selection	
B4	Line Address Order	LCD refresh direction control
B3	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)





Note.

Top-Left (0,0) means a physical memory location

<table>
<tr><th>36 H</th><th>MADCTL (Memory Data Access Control)</th></tr>
<tr><td>Restriction</td><td>D2, D1 and D0 are set to “000” internally.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>B7=0, B6=0, B5=0, B4=0, B3=0, B2=0, B1=0, B0=0</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>B7=0, B6=0, B5=0, B4=0, B3=0, B2=0, B1=0, B0=0</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

5.1.29. VERTICAL SCROLLING START ADDRESS (37H)

37H	VSCRSADD (Vertical Scrolling Start Address)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	0000 …. 013F
2nd parameter	1	1	↑	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	

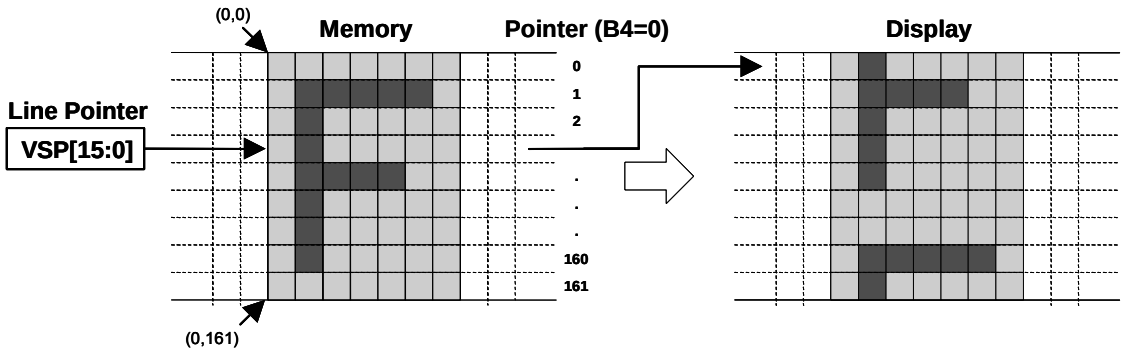
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. (refer to Restriction)

The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below.

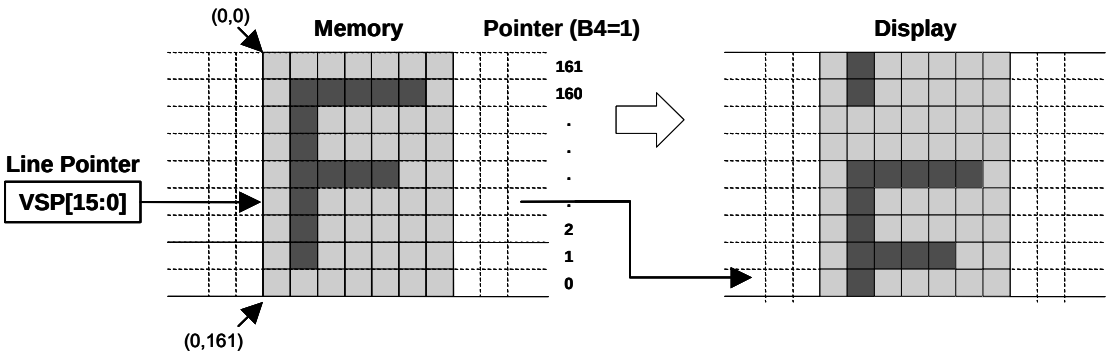
When MADCTL B4 = 0

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP= ‘3’.



When MADCTL B4 = 1

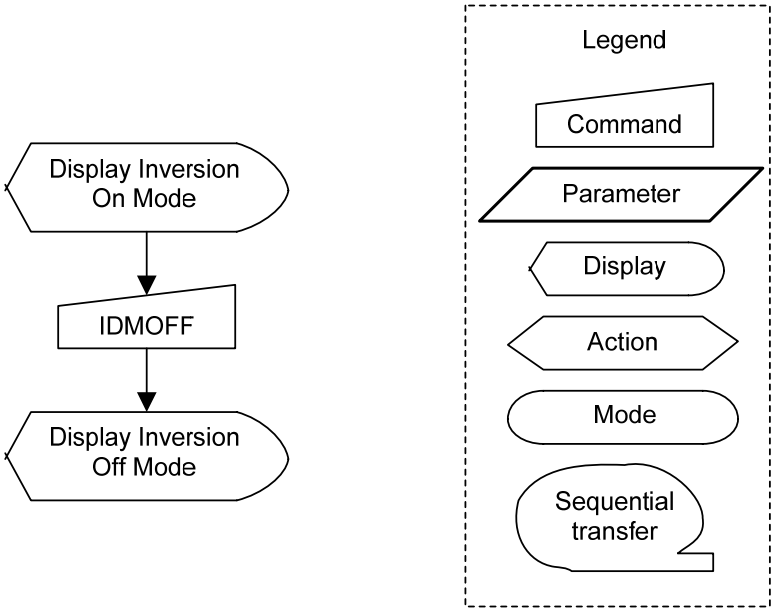
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP = ‘3’.



<table>
<tr><th>37H</th><th>VSCRSADD (Vertical Scrolling Start Address)</th></tr>
<tr><td></td><td>Note.
1. When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
2. VSP refers to the Vertical Scrolling Start Address.</td></tr>
<tr><td>Restriction</td><td>Note.
Each detail initial values by the display resolution will be updated.

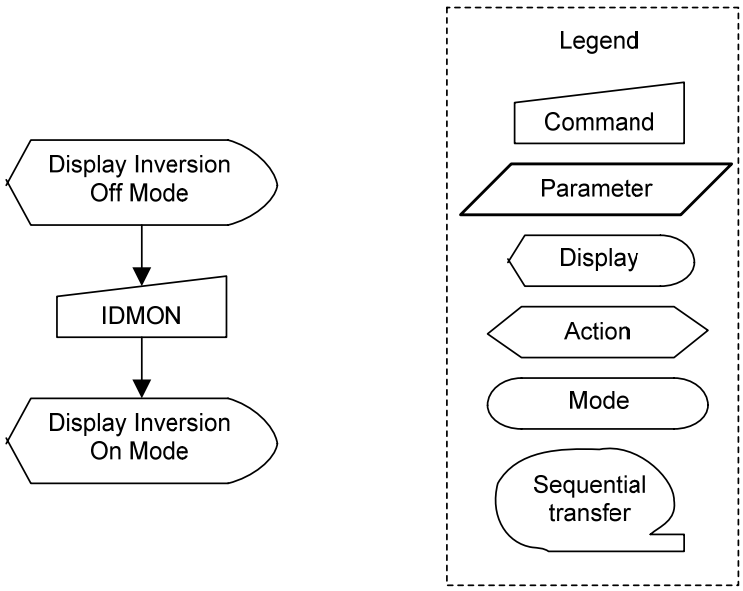
Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition 33h) – otherwise undesirable image will be displayed on the Panel.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000</td></tr>
<tr><td>S/W Reset</td><td>0000</td></tr>
<tr><td>H/W Reset</td><td>0000</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

5.1.30. IDLE MODE OFF (38H)

<table>
<tr><th>38H</th><th colspan="11">IDMOFF (Idle Mode Off)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38</td></tr>
<tr><td>Parameter</td><td colspan="11">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to recover from idle mode on. In the idle off mode, LCD can display maximum 262k-color.</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle off mode</td></tr><tr><td>S/W Reset</td><td>Idle off mode</td></tr><tr><td>H/W Reset</td><td>Idle off mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="11"> 
</td></tr>
</table>

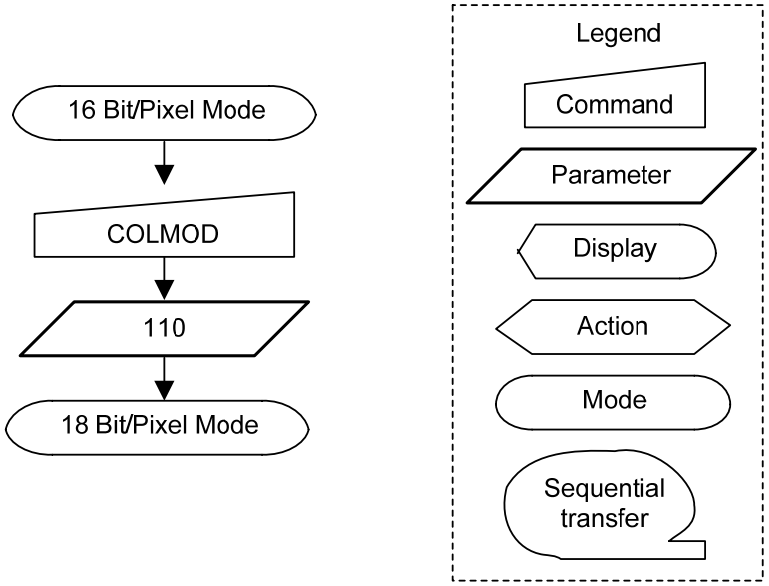
5.1.31. IDLE MODE ON (39H)

<table>
<tr><th>39H</th><th colspan="12">IDMON (Idle Mode On)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
Memory contents vs Display Color X=don’t care
<table>
<tr><th>Color</th><th>R5,R4,R3,R2,R1,R0</th><th>G5,G4,G3,G2,G1,G0</th><th>B5,B4,B3,B2,B1,B0</th></tr>
<tr><td>Red</td><td>1 x x x x x</td><td>0 x x x x x</td><td>0 x x x x x</td></tr>
<tr><td>Green</td><td>0 x x x x x</td><td>1 x x x x x</td><td>0 x x x x x</td></tr>
<tr><td>Blue</td><td>0 x x x x x</td><td>0 x x x x x</td><td>1 x x x x x</td></tr>
<tr><td>White</td><td>1 x x x x x</td><td>1 x x x x x</td><td>1 x x x x x</td></tr>
<tr><td>Black</td><td>0 x x x x x</td><td>0 x x x x x</td><td>0 x x x x x</td></tr>
<tr><td>Cyan</td><td>0 x x x x x</td><td>1 x x x x x</td><td>1 x x x x x</td></tr>
<tr><td>Magenta</td><td>1 x x x x x</td><td>0 x x x x x</td><td>1 x x x x x</td></tr>
<tr><td>Yellow</td><td>1 x x x x x</td><td>1 x x x x x</td><td>0 x x x x x</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in idle on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle Off Mode</td></tr>
<tr><td>S/W Reset</td><td>Idle Off Mode</td></tr>
<tr><td>H/W Reset</td><td>Idle Off Mode</td></tr>
</table></td></tr>
</table>

39H	IDMON (Idle Mode On)
Flow Chart	

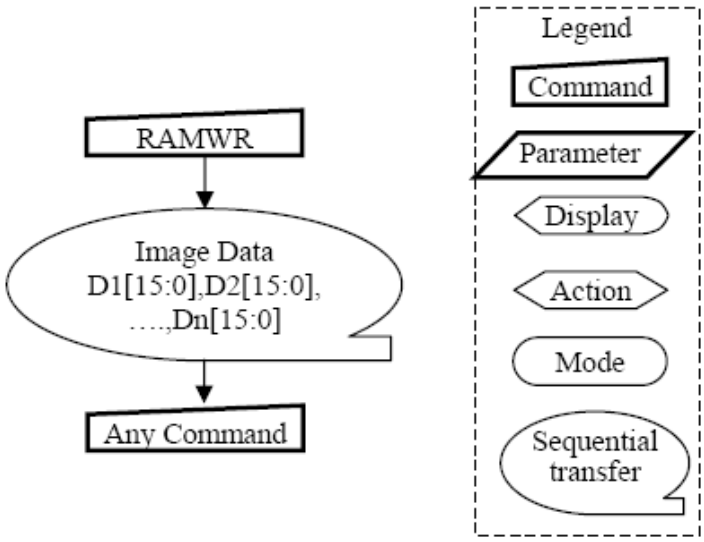
5.1.32. INTERFACE PIXEL FORMAT (3AH)

<table>
<tr><th>3AH</th><th colspan="12">COLMOD (Interface Pixel Format)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3A</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>D6</td><td>D5</td><td>D4</td><td>X</td><td>D2</td><td>D1</td><td>D0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to define the format of RGB picture data, which is to be transferred via the MPU interface. The formats are shown in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>“0” (Not used)</td></tr>
<tr><td>D6</td><td rowspan="3">RGB Interface Color Format</td><td rowspan="3">“101”=16 bit/pixel
“110”=18 bit/pixel</td></tr>
<tr><td>D5</td></tr>
<tr><td>D4</td></tr>
<tr><td>D3</td><td>-</td><td>“0” (Not used)</td></tr>
<tr><td>D2</td><td rowspan="3">Control Interface Color Format</td><td rowspan="3">“101”=16 bit/pixel
“110”=18 bit/pixel</td></tr>
<tr><td>D1</td></tr>
<tr><td>D0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">There is no visible effect until the Frame Memory is written to.</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>18 bit / pixel</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>18 bit / pixel</td></tr>
</table></td></tr>
</table>

3AH	COLMOD (Interface Pixel Format)
Flow Chart	Example: 

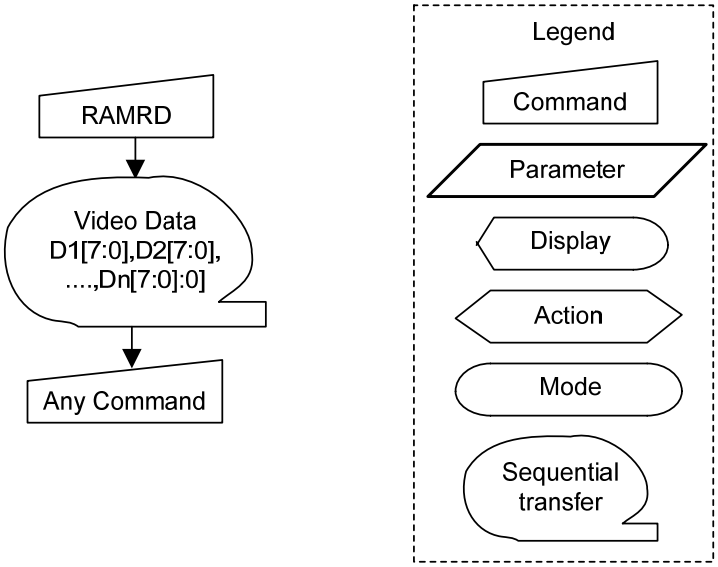
5.1.33. MEMORY WRITE CONTINUE (3CH)

3CH	RAMWRC (Memory Write Continue)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	1	0	0	3C
1st Parameter	1	1	↑	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00.. FF
:	1	1	↑	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00.. FF
Nth Parameter	1	1	↑	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00.. FF
Description	This command is transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. If set_address_mode B5=0: Data is written continuing from the pixel location after the write range of the previous write_memory_continue or write_memory_start. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to the Start Column (SC) and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC +1) * (EP – SP + 1) the extra pixels are ignored. If set_address_mode B5=1: Data is written continuing from the pixel location after the write range of the previous write_memory_continue or write_memory_start. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to the Start Page (SP) and the column register is incremented. Pixels are written to the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC +1) * (EP – SP + 1) the extra pixels are ignored.											

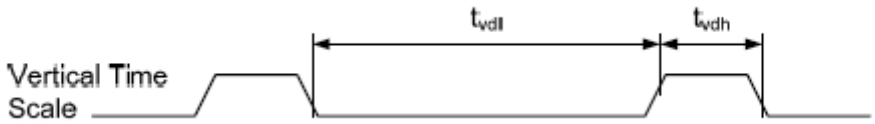
<table>
<tr><td>Restriction</td><td>A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr>
<tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr>
<tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

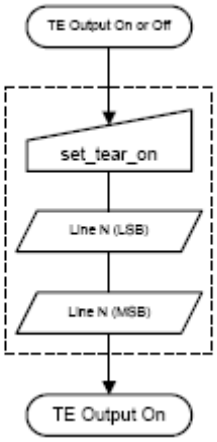
5.1.34. MEMORY READ CONTINUE (3EH)

3EH	RAMRDC (Memory Read Continue)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	1	1	0	3E
1st Parameter	1	↑	1	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00.. FF
:	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00.. FF
Nth Parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00.. FF
Description	This command is transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If set_address_mode B5=0: Pixels are read continuing from the pixel location after the read range of the previous read_memory_continue or read_memory_start. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If set_address_mode B5=1: Pixels are read continuing from the pixel location after the read range of the previous read_memory_continue or read_memory_start. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command.											
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 18-bit so there is no restriction on the length of data. A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read address. Otherwise, data read with											

<table>
<tr><td></td><td>read_memory_continue is undefined.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr>
<tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr>
<tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

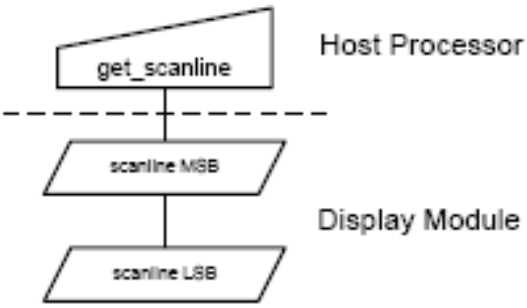
5.1.35. SET TEAR SCANLINE (44H)

<table>
<tr><th>44H</th><th colspan="12">TESCAN (Set Tear Scanline)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>N[15]</td><td>N[14]</td><td>N[13]</td><td>N[12]</td><td>N[11]</td><td>N[10]</td><td>N[9]</td><td>N[8]</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>N[7]</td><td>N[6]</td><td>N[5]</td><td>N[4]</td><td>N[3]</td><td>N[2]</td><td>N[1]</td><td>N[0]</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command turns on the display module’s Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing set_address_mode bit B4.
The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.
The Tearing Effect Output line consists of V-Blanking information only.
 
Note that set_tear_scanline with N=0 is equivalent to set_tear_on with M=0.
The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command takes affect on the frame following the current frame. Therefore, if the Tear Effect (TE) output is already ON, the TE output shall continue to operate as programmed by the previous set_tear_on, or set_tear_scanline, command until the end of the frame.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>16’h0000</td></tr><tr><td>S/W Reset</td><td>16’h0000</td></tr><tr><td>H/W Reset</td><td>16’h0000</td></tr></table></td></tr>
</table>

Flow Chart	 TE Output On or Off set_tear_on Line N (LSB) Line N (MSB) TE Output On

5.1.36. GET SCANLINE (45H)

<table>
<tr><th>45H</th><th colspan="12">RDTESCAN (Get Scanline)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>45</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>N[15]</td><td>N[14]</td><td>N[13]</td><td>N[12]</td><td>N[11]</td><td>N[10]</td><td>N[9]</td><td>N[8]</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>N[7]</td><td>N[6]</td><td>N[5]</td><td>N[4]</td><td>N[3]</td><td>N[2]</td><td>N[1]</td><td>N[0]</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of Vsync and is denoted as Line 0.

When in Sleep Mode, the value returned by get_scanline is undefined.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>16’h0000</td></tr><tr><td>S/W Reset</td><td>16’h0000</td></tr><tr><td>H/W Reset</td><td>16’h0000</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

5.1.37. WRITE MANUAL BRIGHTNESS (51H)

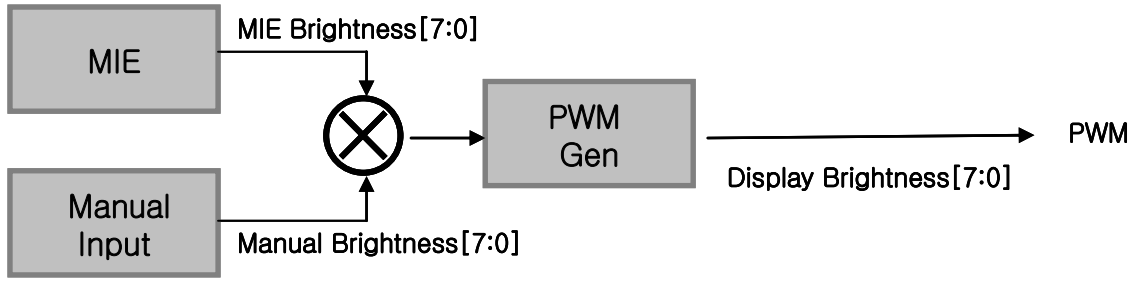
51H	WRDISBV (Write Manual Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	0	1	51
Parameter	1	1	↑	MAN_ BR[7]	MAN_ BR[6]	MAN_ BR[5]	MAN_ BR[4]	MAN_ BR[3]	MAN_ BR[2]	MAN_ BR[1]	MAN_ BR[0]	xx

Description

This command is used to set the manual brightness value. If the manual brightness is used (BC_MODE = “01” or “11”), the value of register “MAN_BR [7:0] is selected or merged with the MIE brightness to generate PWM.

MAN_BR [7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Manual Birightness



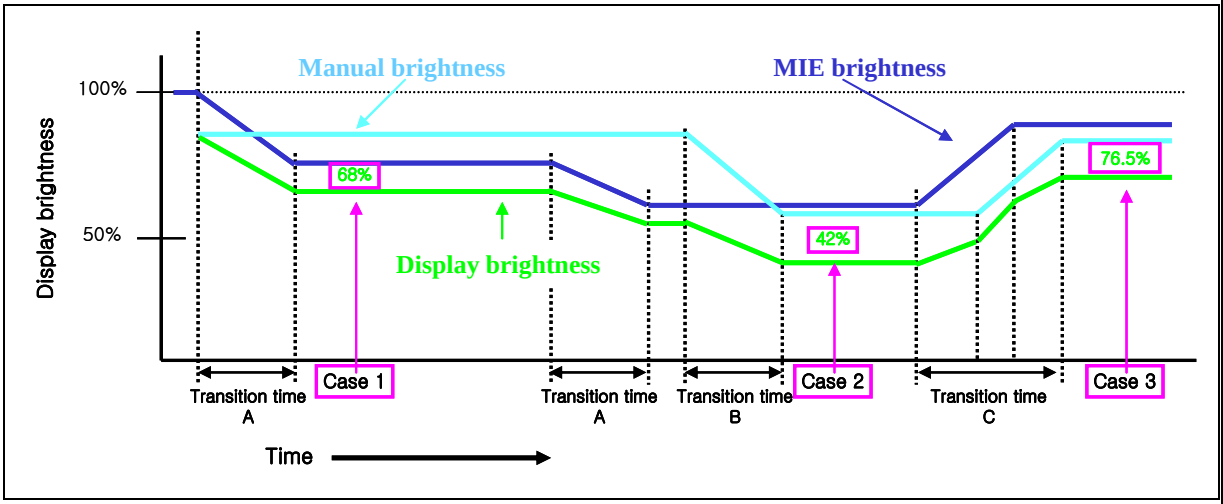
The display brightness level is calculated with the following formula.

$$Display\_Brightness = MIE\_Brightness \; X \; Manual\_Brightness \; / \; 255$$

The MIE brightness has transition time A and the manual brightness has transition time B.

The maximum transition time is transition time C (C ≤ A + B).

Example of manual brightness



Operation Mode	Manual Brightness	MIE Brightness	Display Brightness
Case 1	85 %	80 %	68 %
Case 2	60 %	70 %	42 %
Case 3	85 %	90 %	76.5 %

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

5.1.38. READ DISPLAY BRIGHTNESS (52H)

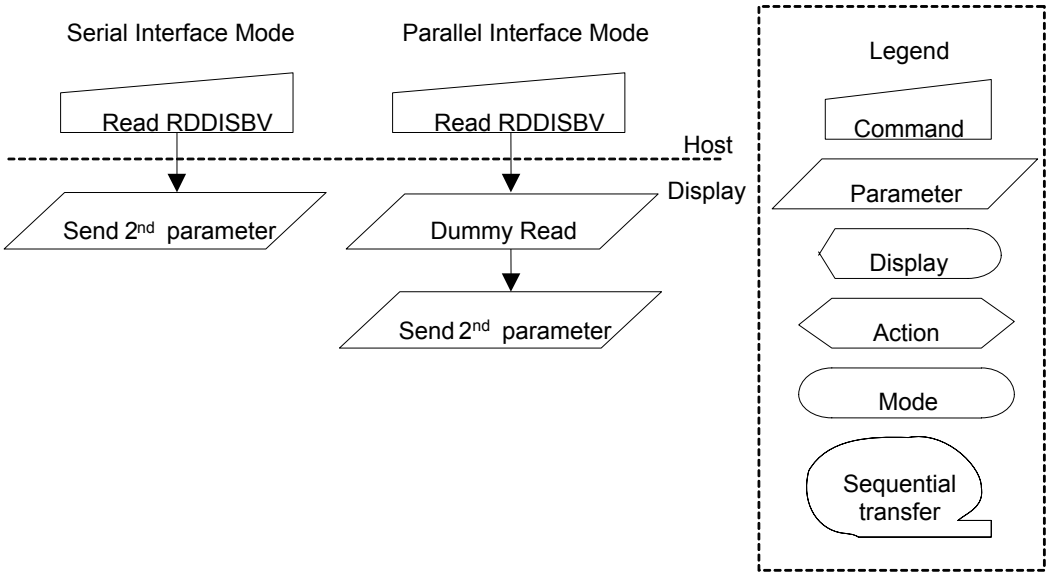
52H	RDDISBV (Read Display Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	1	0	52
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	BR_ OUT[7]	BR_ OUT[6]	BR_ OUT[5]	BR_ OUT[4]	BR_ OUT[3]	BR_ OUT[2]	BR_ OUT[1]	BR_ OUT[0]	xx
Description	This command is used to read the display brightness value. It is a real brightness value of PWM output which is calculated with MIE brightness and manual brightness. The value of this register is updated after display V-sync and host can read exact value after display V-sync. RDDISBV is valid in case that BCTRL(WRCTRLD 53h) = 1.											
Restriction	There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2											

BR_OUT [7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

	Status	Default Value
Default	Power On Sequence	8'h00
	S/W Reset	8'h00
	H/W Reset	8'h00

Flow Chart



5.1.39. WRITE BL CONTROL (53H)

53H	WRCTRLD (Write BL Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	1	1	53
Parameter	1	1	↑	0	0	BCTRL	0	DD	BL	0	0	xx

Description

- BCTRL

This register is used to enable the backlight control block. If BCTRL is turned off, the BL control block is not working and PWM output is fixed to low.

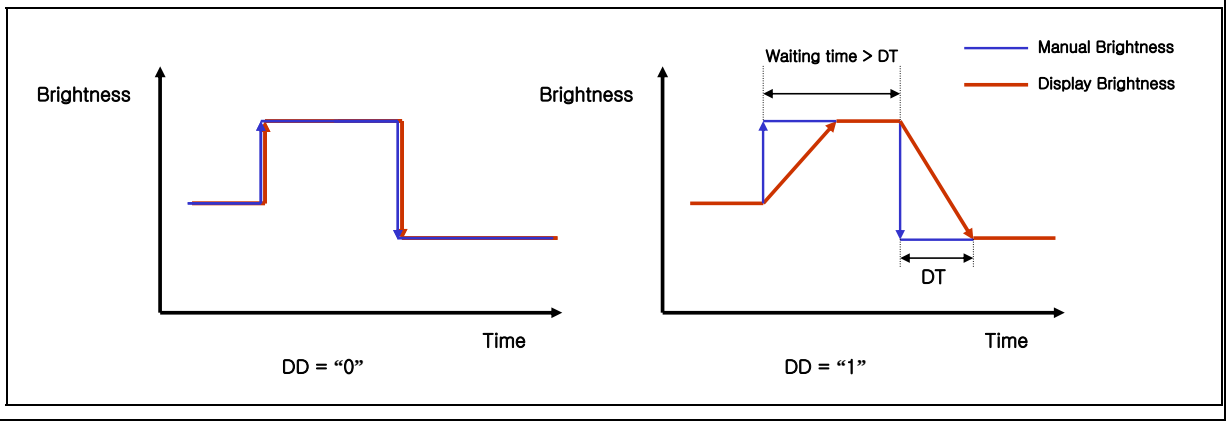
BRCTRL	BL Control
0	Off
1	On

- DD

This register is used to enable the manual brightness dimming function. The manual brightness should be changed smoothly for preventing a visible artifact, e.g. flicker. So the dimming function is needed when the transition of input manual brightness is fast to make a visible artifact. When the manual dimming is enabled, the new manual brightness value has to be changed after former dimming transition is finished. The transition time is controlled by DT[2:0].

DD	Manual Dimming Function
0	Off
1	On

Manual dimming function



- BL

This register is used to enable the PWM output. Even if the value of BL is “0”, the backlight control block is working when BCTRL is “1”. And the host can read the display brightness value(DISP_BRIGHT[7:0]) and control the BLU directly.

BL	PWM state
0	Low
1	Active

Restriction

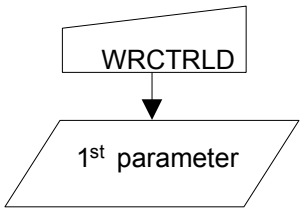
Register Availability

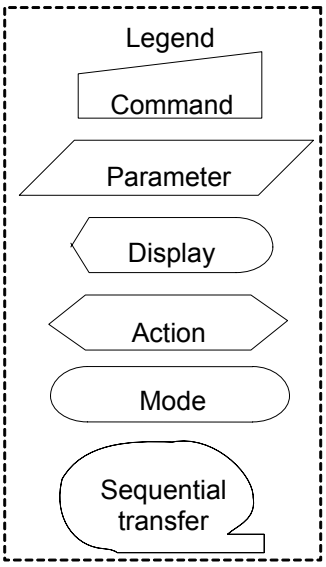
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8’h00
S/W Reset	8’h00
H/W Reset	8’h00

Flow Chart





5.1.40. READ BL CONTROL (54H)

54H	RDCTRLD (Read BL Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	0	0	54
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	0	0	BCTRL	0	DD	BL	0	0	xx
Description	This command is used to read BL control register. For details, refer to Write BL Control (53h).											
Restriction	There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2											

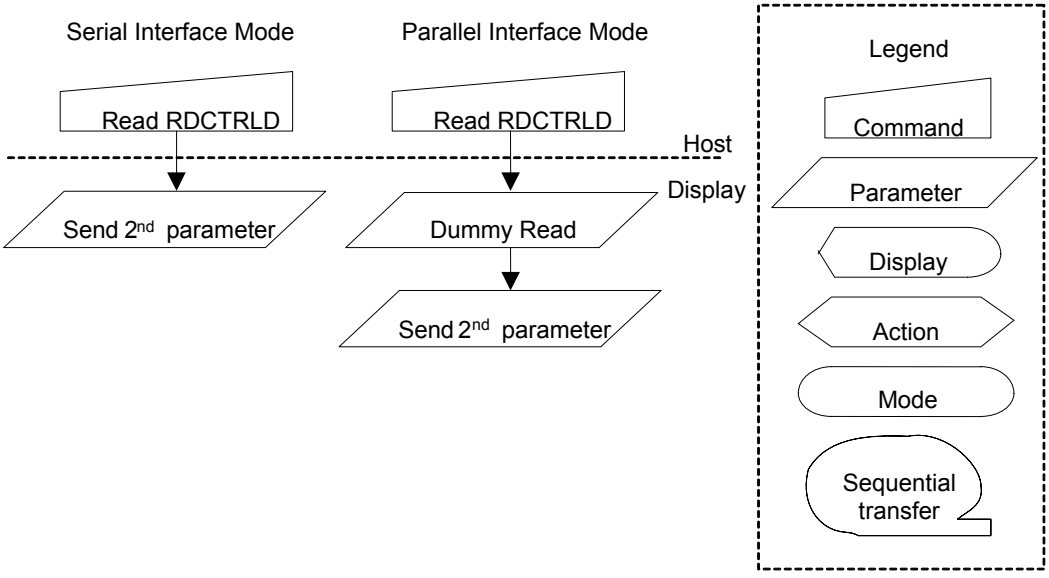
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart



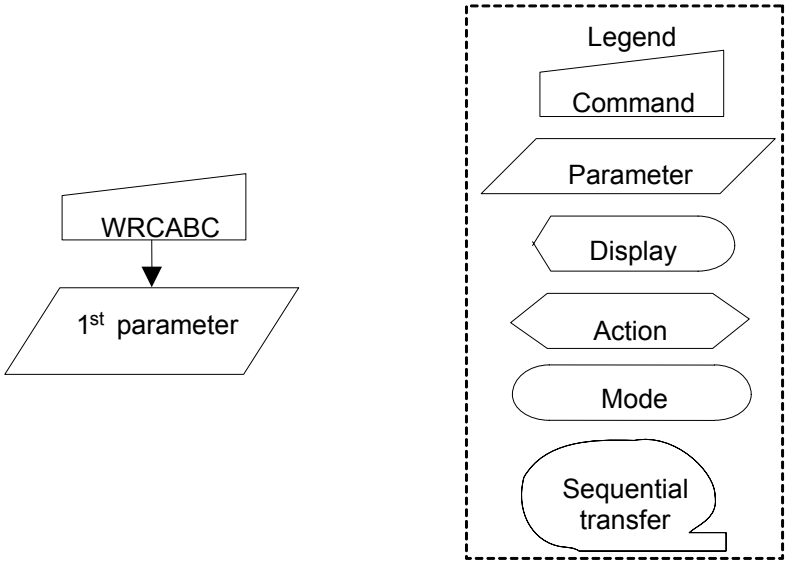
5.1.41. WRITE MIE MODE (55H)

55H	WRCABC (Write MIE Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	0	1	55
Parameter	1	1	↑	0	0	0	0	0	0	MIE_ MODE[1]	MIE_ MODE[0]	xx
Description	This command is used to select the operation mode of MIE. In UI or Still-image mode, the host should send same image at least two times to apply MIE algorithm exactly. If the MIE is off mode, the BLU brightness value of MIE is set to 255.											
Restriction												
Register Availability												
Default												

MIE_MODE[1:0]	Operation Mode
00	Off
01	UI (User Interface)
10	Still Image
11	Moving Image

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart	

WRCABC
1st parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

5.1.42. READ MIE MODE (56H)

56H	RDCABC (Read MIE Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	1	0	56
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	0	0	0	0	0	0	MIE_ MODE[1]	MIE_ MODE[0]	xx
Description	This command is used to read MIE mode register. For details, refer to Write MIE Mode (55h).											
Restriction	There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2											

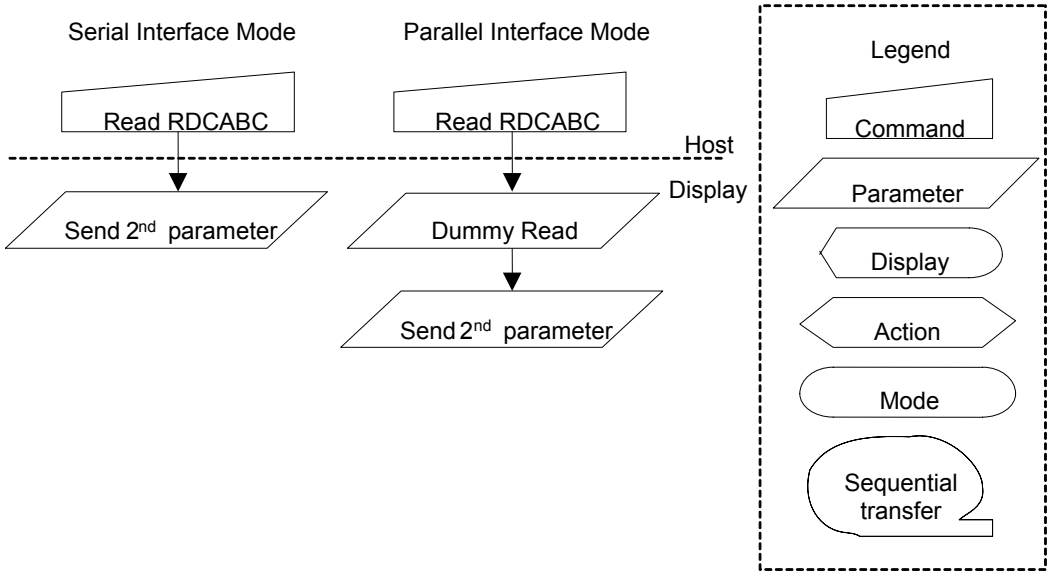
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

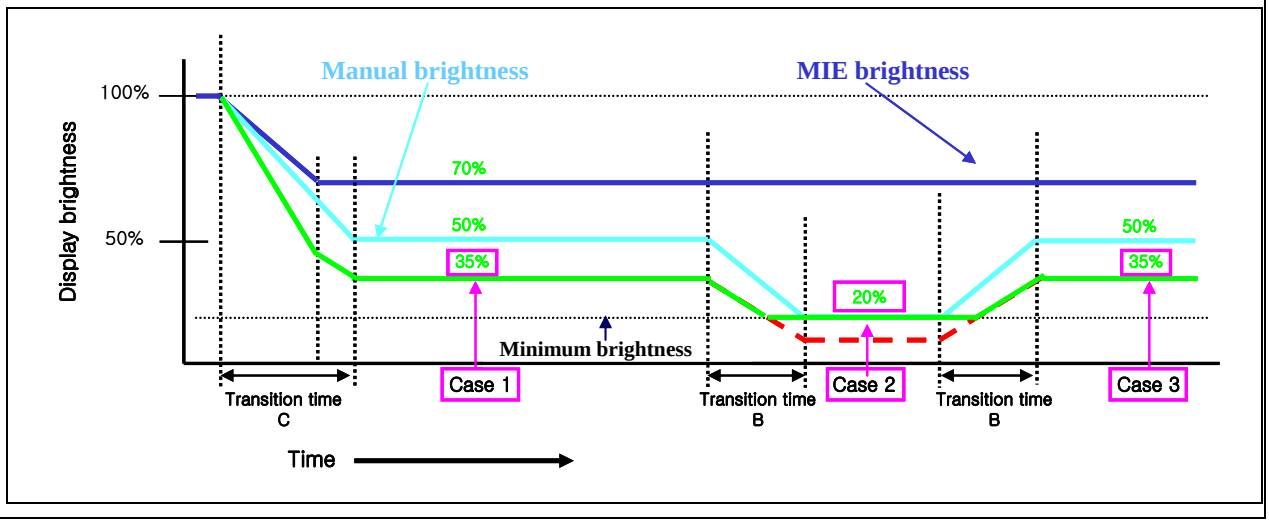
Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart



5.1.43. WRITE MINIMUM BRIGHTNESS (5EH)

5EH	WRCABCMB (Write Minimum Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	1	1	1	0	5E
Parameter	1	1	↑	MIN_ BRIGHT [7]	MIN_ BRIGHT [6]	MIN_ BRIGHT [5]	MIN_ BRIGHT [4]	MIN_ BRIGHT [3]	MIN_ BRIGHT [2]	MIN_ BRIGHT [1]	MIN_ BRIGHT [0]	xx
Description	This command is used to set the minimum brightness value. The MIE function is automatically reduced the backlight brightness based on the content of image. In the case of the combination with the manual brightness setting, the display brightness can be too dark. It must affect to image quality degradation. So the minimum brightness setting is used to avoid too much brightness reduction. When the MIE is activated, the display brightness can not be reduced less than the value of minimum brightness setting. The image processing function is worked as normal, even if the display brightness can not be decreased by the minimum brightness setting. This function of the manual brightness setting does not affect to the other functions. The smooth transition and dimming function can be worked as normal. The manual brightness shouldn't be set less than the minimum brightness. When the BL control block is turned off (BCTRL=0), the MIE minimum brightness setting is ignored. Example of minimum brightness  											

Operation Mode	Manual Brightness	MIE Brightness	Calculated Display Brightness	Display Brightness
Case 1	50 %	70 %	35%	35 %
Case 2	20 %	70 %	14%	20 %
Case 3	50 %	70 %	35%	35 %

MIN_BRIGHT[7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Status	Default Value
Initial	MIN_BRIGHT[7:0] = 0000_0000

Restriction

Set the minimum brightness value to 00h before brightness control block turns on(BCTRL = 0 → 1)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

5.1.44. READ MINIMUM BRIGHTNESS (5FH)

5FH	RDCABCMB (Read Minimum Brightness)											
	DC X	RD X	WR X	D7	D6	D5	D4	D3	D2	D1	D0	HE X
Command	0	1	↑	0	1	0	1	1	1	1	1	5F
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	MIN_ BRIGHT [7]	MIN_ BRIGHT [6]	MIN_ BRIGHT [5]	MIN_ BRIGHT [4]	MIN_ BRIGHT [3]	MIN_ BRIGHT [2]	MIN_ BRIGHT [1]	MIN_ BRIGHT [0]	xx
Description	This command is used to read Minimum Brightness register. For details, refer to Write Minimum Brightness (5Eh). RDCABCMB is valid in case that BCTRL(WRCTRLD 53h) = 1.											
Restriction	There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2											

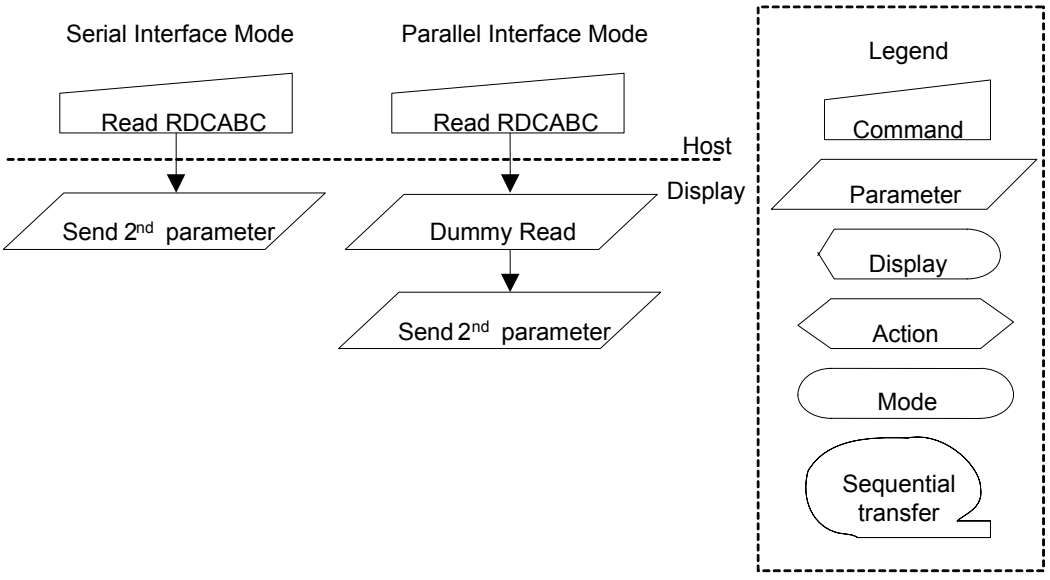
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

Flow Chart



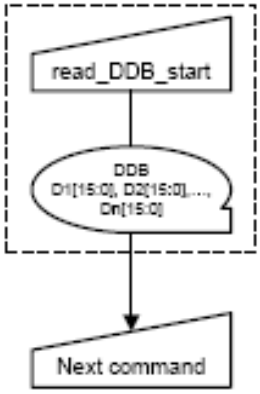
5.1.45. READ DDB START (A1H)

A1H	RDDDBS (Read DDB Start)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	0	0	0	1	A1
1st Parameter	1	↑	1	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00.. FF
:	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00.. FF
Nth Parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00.. FF
Description	This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data. Parameter 1 : MS (most significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization. Parameter 2 : LS (least significant) byte of Supplier ID. Parameter 3 : MS (most significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example. Parameter 4 : LS (least significant) byte of Supplier Elective Data. Parameter 5 : single-byte Escape of Exit Code (EEC). The code is interpreted as follows : - FFh : Exit code - there is no more data in the Descriptor Block - 00h : Escape code - there is supplier-proprietary data in the Descriptor Block(does not conform to any MIPI Alliance standard) - Any other value : there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in MIPI Alliance Standard for Device Descriptor Block (DDB). DDBs may contain many more data fields providing information about the peripheral. In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command read_DDB_start from host processor to peripheral, which includes the											

<table>
<tr><td></td><td>bus turn-around token.
The peripheral then takes control of the bus and returns the requested data. The peripheral response to read_DDB_start is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command.

The response to a read_DDB_start command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a read_DDB_continue command to access the next portion of the DDB. A read_DDB_continue command begins the next read at the location following the last byte of the previous data read from the DDB.

Subsequent read_DDB_continue commands can be used to read a DDB or supplier-proprietary block of arbitary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any read_DDB_xxx command.</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

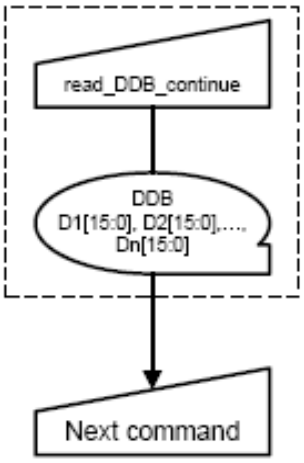
Flow Chart	

5.1.46. READ DDB CONTINUE (A8H)

A8H	RDDDBC (Read DDB Continue)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	1	0	0	0	A8
1st Parameter	1	↑	1	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	00.. FF
:	1	↑	1	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	00.. FF
Nth Parameter	1	↑	1	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00.. FF
Description	See section 5.1.48 (A1h)											
Restriction	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.											

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

Flow Chart	 read_DDB_continue DDB D1[15:0], D2[15:0],…, Dn[15:0] Next command

5.1.47. READ ID1 (DAH)

DAH	RDID1 (Read ID1)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	1	0	DA
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	-
2nd para	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
Description	The 1st Parameter is dummy data. This read byte identifies the LCD module's manufacturer.											
Restriction	There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2											

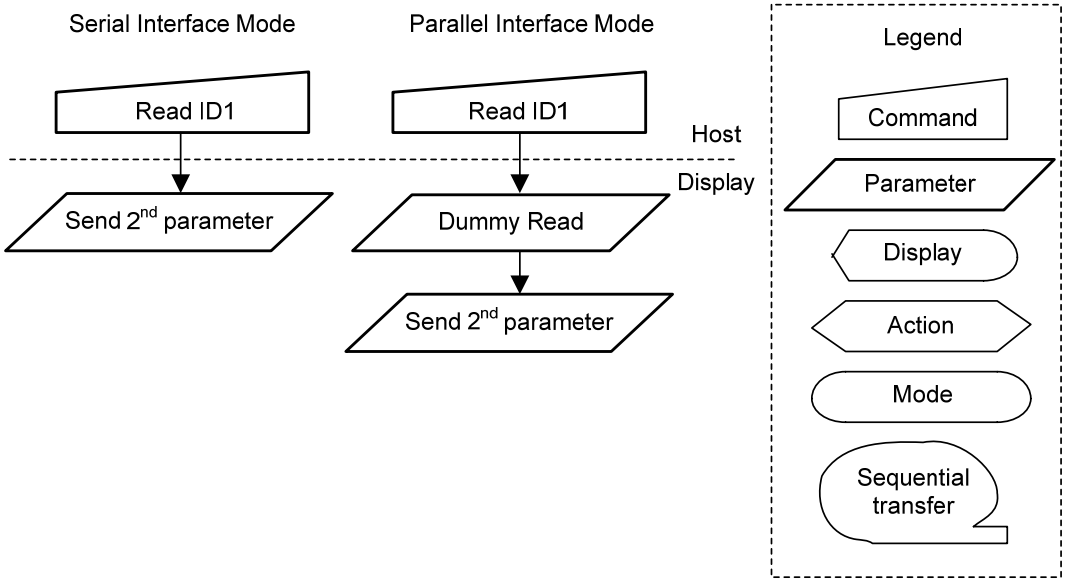
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.1.48. READ ID2 (DBH)

DBH	RDID2 (Read ID2)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	1	1	DB
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	-
2nd para	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
Description	The 1st Parameter is dummy data. This read byte identifies the LCD module / driver version ID.											
Restriction	There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2											

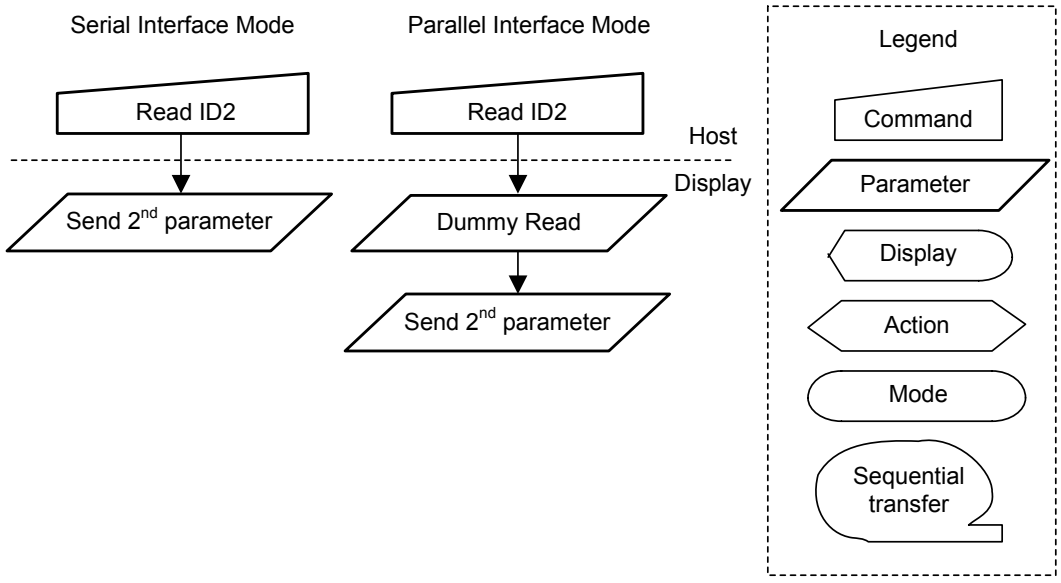
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.1.49. READ ID3 (DCH)

DCH	RDID3 (Read ID3)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	0	0	DC
1st para	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd para	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	xx
Description	The 1st Parameter is dummy data. This read byte identifies the LCD module/driver.											
Restriction	There is no dummy read parameter(1st para) at serial I/F, refer to 3.1.4.2, 3.1.5.2											

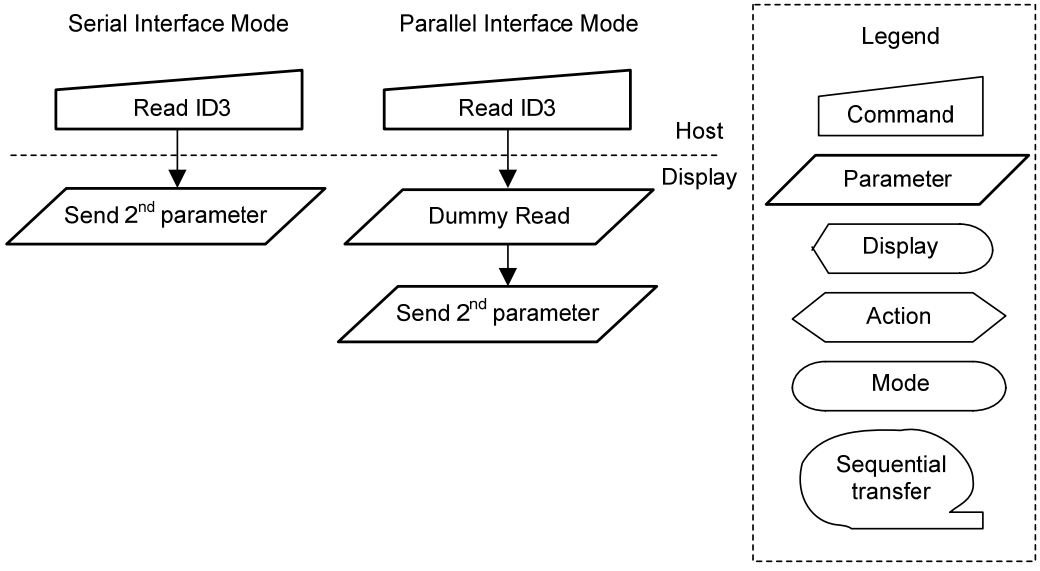
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.2. DESCRIPTION OF LEVEL 2 COMMAND

Table 68. List of level 2 command

Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	Parameters
C0h	MIECTL	W	3	MIE control
C1h	BCMODE	W	1	MIE control
C2h	WRMIECTL	W	9	MIE control
C3h	WRBLCTL	W	2	MIE control
D0h	MTPCTL	W	1	MTP control
D2h	MTPACCS	W	2	MTP control
D3h	MTPRD	R	8	MTP control
DFh	DSTB	W	1	Deep Standby
F0h	PASSWD1	W	2	Test Key
F1h	PASSWD2	W	2	Test Key
F2h	DISCTL	W	17	Display control
F3h	MANPWRSEQ	W	5	Power sequence control
F4h	PWRCTL	W	20	Power control
F5h	VCMCTL	W	12	VCOM control
F6h	SRCCTL	W	9	Source control
F7h	IFCTL	W	4	Interface control
F8h	PANELCTL	W	3	Gate control
F9h	GAMMASEL	W	1	Gamma selection
FAh	PGAMMACTL	W	12	Positive gamma control
FBh	NGAMMACTL	W	12	Negative gamma control

Note: The number of parameter is the number of real parameter except dummy parameter.

5.2.1. MIECTL1 (C0H)

C0h	MIECTL1 (MIE Control1)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	0	0	C0
1st Parameter	1	1	↑	RRC[7]	RRC[6]	RRC[5]	RRC[4]	RRC[3]	RRC[2]	RRC[1]	RRC[0]	8'h80
2nd Parameter	1	1	↑	IERC[7]	IERC[6]	IERC[5]	IERC[4]	IERC[3]	IERC[2]	IERC[1]	IERC[0]	8'h80
3rd Parameter	1	1	↑	-	-	ONOFF DIMMEN	SERC[4]	SERC[3]	SERC[2]	SERC[1]	SERC[0]	8'h10

5.2.1.1. RRC [7:0]: Reduction Rate Control of backlight power. Default value is RRC[7:0]=10000000.

$$Power\_Reduction\_Rate = Contents\_Based\_Reduction\_Rate \; X \; \frac{RRC}{128}$$

Figure100. Expression of power reduction rate

Contents_Based_Reduction_Rate is the power reduction rate. Reduction range is from '0' (no reduction) to two times of contents adaptive backlight power.

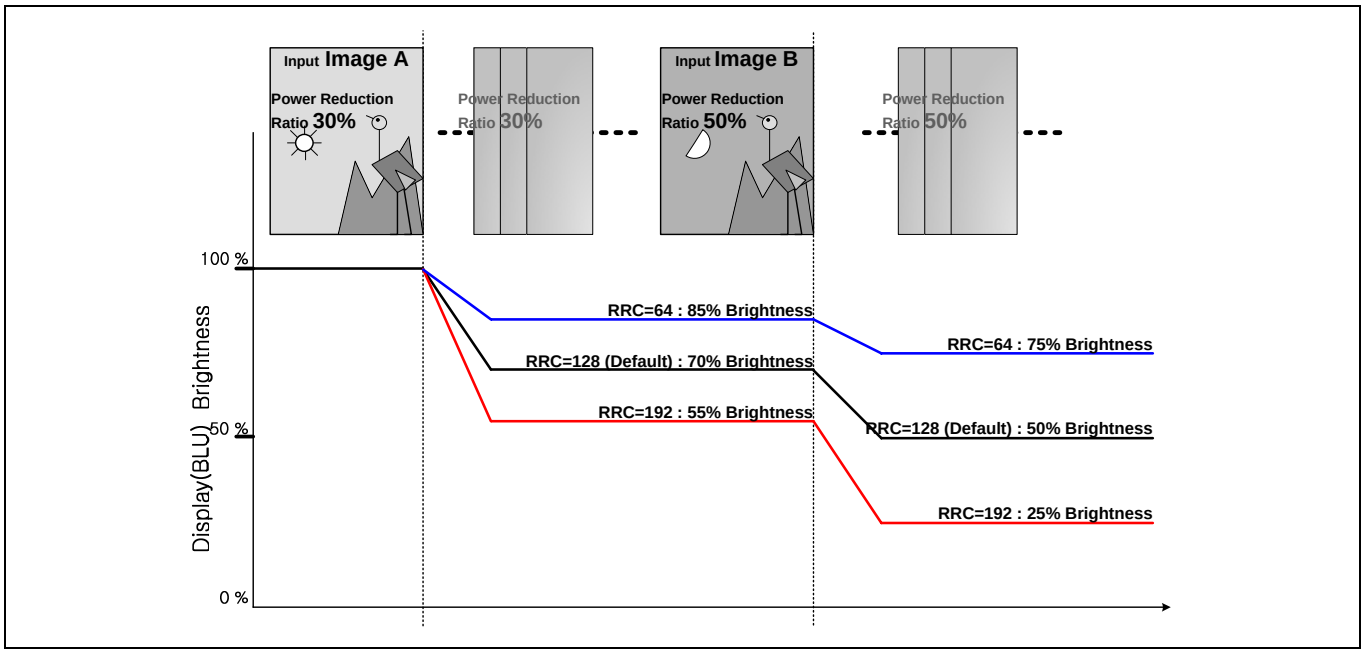


Figure101. According to RRC value, brightness variation

5.2.1.2. IERC [7:0]: Image Enhancement Rate Control. If IERC is '0', there is no enhancement of input image. If its value is '255', enhancement rate is two times of Image_Enhancement_Rate. Default value is RRC[7:0]=10000000.

$$Adjusted\_Image\_Enhancement\_Rate = Image\_Enhancement\_Rate \; X \; \frac{IERC}{128}$$

Figure102. Expression of adjusted image enhancement rate

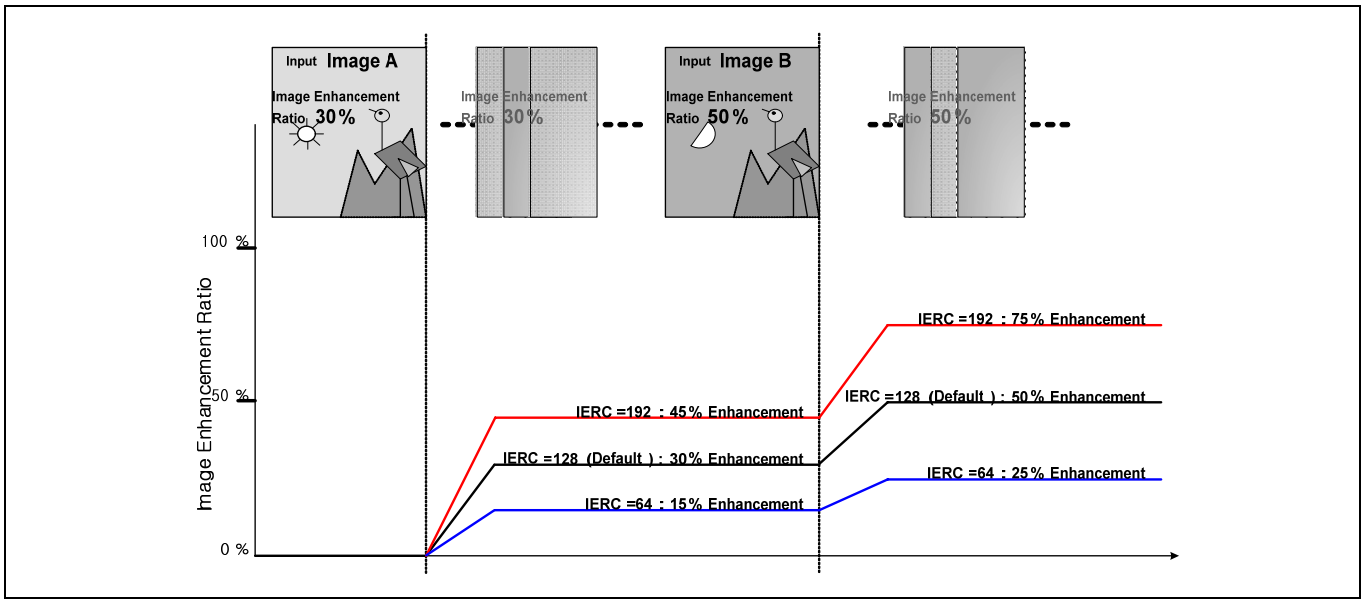


Figure103. According to IERC value, image enhancement ratio variation

5.2.1.3. ONOFF_DIMM_EN

This register is used to enable the on/off dimming function of MIE.

The MIE has a dimming function for preventing abnormal visible artifacts when the MIE is turning on or off.
If the ONOFF_DIMM_EN is “1”, the MIE is smoothly turning on or off. When the ONOFF_DIMM_EN is “0”, the MIE is turning on or off immediately. The transition time is controlled by CST[1:0].
If this dimming function is enabled in UI or STILL mode, the host must write frames more than the transition time of CST[1:0] to finish the dimming transition. If the MIE mode is changed during on/off dimming transition, it will be updated after finishing the dimming transition.

Table 69. ONOFF_DIMM_EN

ONOFF_DIMM_EN	On / Off Dimming Function
0	Disable
1	Enable

Status	Default Value
Initial	ONOFF_DIMM_EN = 0

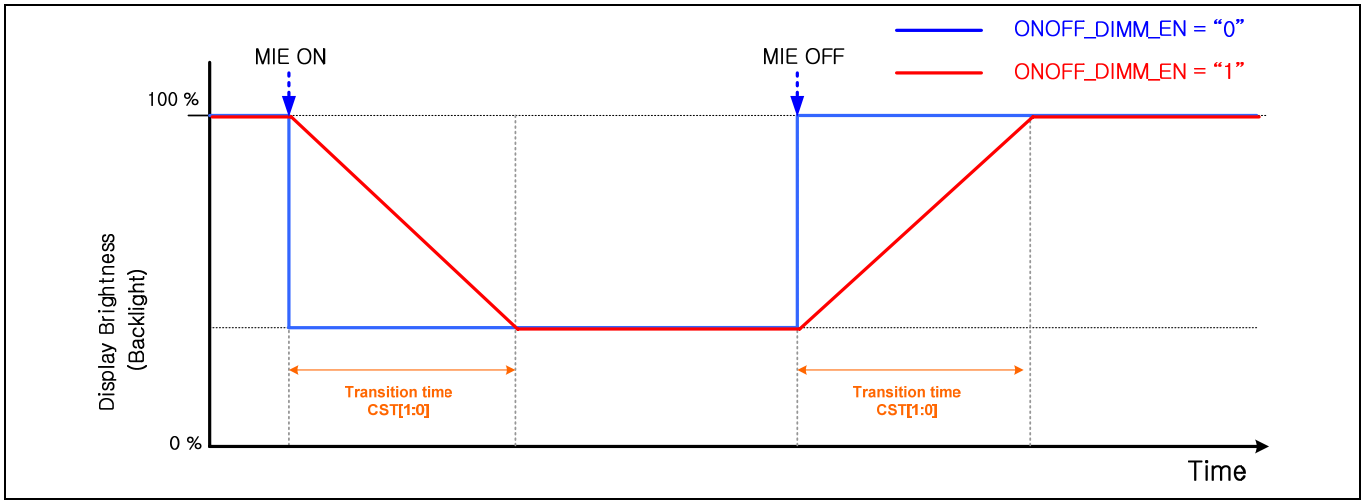


Figure104. Example of MIE On / Off dimming transition control

5.2.1.4. SERC[4:0]

This register is used to adjust the Image Saturation Enhancement Rate.

$$Adjusted\_Saturation\_Enhancement\_Rate = Saturation\_Enhancement\_Rate\ X\ \frac{SERC}{16}$$

Figure105. Saturation enhancement rate

If the value of SERC is '0', there is no saturation enhancement in output image. If the value of SERC is increased, the saturation enhancement rate will be increased and more vivid image is obtained. The other way, if the value of SERC is decreased, the saturation enhancement rate will be decreased.

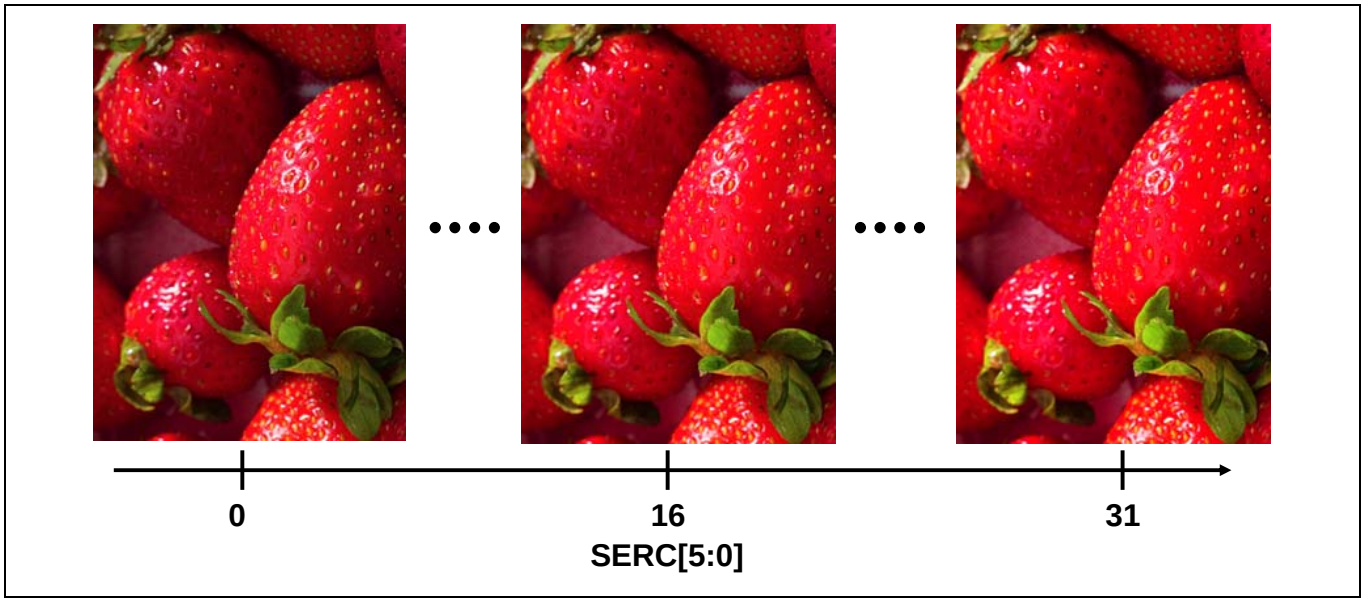


Figure106. Example of SERC

Table 70. SERC[4:0]

SERC[4:0]	Adjust Saturation Enhancement Rate
00000	Saturation Enhancement Rate x 0/16
00001	Saturation Enhancement Rate x 1/16
00010	Saturation Enhancement Rate x 2/16
…	…
10000	Saturation Enhancement Rate x 16/16
…	…

SERC[4:0]	Adjust Saturation Enhancement Rate
11101	Saturation Enhancement Rate x 29/16
11110	Saturation Enhancement Rate x 30/16
11111	Saturation Enhancement Rate x 31/16

Status	Default Value
Initial	SERC[4:0] = 10000

5.2.2. BCMODE (C1H)

C1h	BCMODE											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	0	1	C1
Parameter	1	1	↑	-	-	-	-	-	-	BC_ MODE[1]	BC_ MODE[0]	8'h01

5.2.2.1. BC_MODE[1:0]

Table 71. BC_MODE[1:0]

BC_MODE[1:0]	BLU Control Mode
0	Off
1	Manual Only
2	MIE Brightness
3	Both

5.2.3. WRMIECTL2 (C2H)

C2h	Write MIE Control 2											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	0	C2
1st Parameter	1	1	↑	-	-	-	-	CAT [1]	CAT [0]	CST [1]	CST [0]	8'h00-

5.2.3.1. CAT[1:0]

This register is used to select the abrupt transition time. The MIE has two transition times based on image contents for preventing abnormal visible artifacts (e.g. flicker). The MIE controls transition time between CAT and CST automatically in moving mode (MIE_MODE = "11").

- Abrupt transition time : If input image is changed abruptly, short transition time is needed.
- Smooth transition time : If input image is changed smoothly, long transition time is needed.

Table 72. CAT[1:0]

CAT[1:0]	Abrupt Transition Time
00	1 frame
01	2 frames
10	4 frames
11	8 frames

Status	Default Value
Initial	CAT[1:0] = 00

5.2.3.2. CST[1 :0]

This register is used to select the smooth transition time

Table 73. CST[1:0]

CST[1:0]	Smooth Transition Time
00	32 frames
01	64 frames
10	96 frames
11	128 frames

Status	Default Value
Initial	CST[1:0] = 00

An example of MIE transition time is illustrated as below. If the input image is changed abruptly, the MIE has an abrupt transition time “case (1)” and if the input image is changed smoothly, the MIE has a smooth transition time “case (2)”. The display brightness changes to target brightness abruptly “case (4)” when the abrupt change of image is happened during the smooth transition “case (3)”.

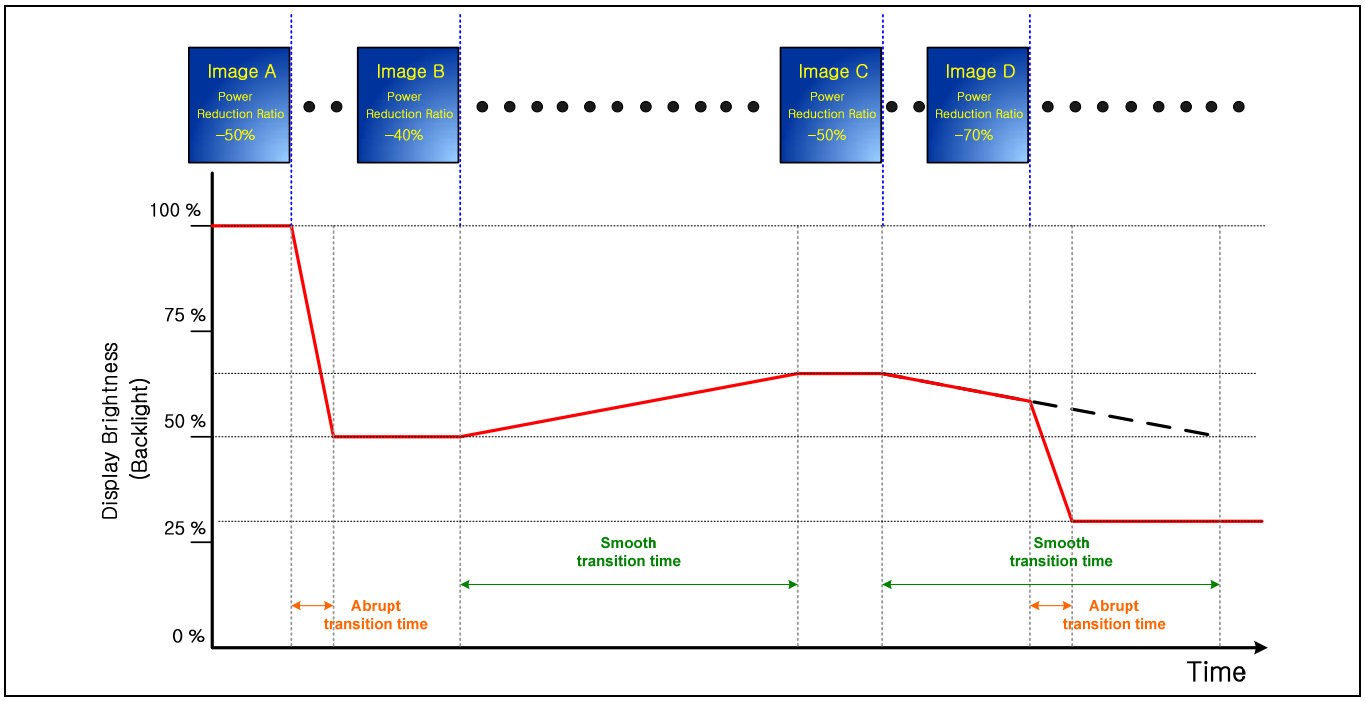


Figure107. Example of MIE transition control

5.2.4. WRBLCTL (C3H)

C3h	WRBLCTL											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	1	C3
1st Parameter	1	1	↑	-	BCFRQ SEL[6]	BCFRQ SEL [5]	BCFRQ SEL [4]	BCFRQ SEL [3]	BCFRQ SEL [2]	BCFRQ SEL [1]	BCFRQ SEL [0]	-
2nd Parameter	1	1	↑	BL_ MODE_ INSLP	-	DT [2]	DT [1]	DT [0]	BL_ DRV_EN	BL_ DIMM_ STEP[1]	BL_ DIMM_ STEP[0]	-

5.2.4.1. BCFRQSEL[6:0]

This register is used to select the frequency of PWM. To select the PWM frequency, two registers are needed. Those register are BCFRQSEL[6:0] and BL_DIMM_STEP[1:0].

For details, refer to the table of PWM frequency.

Status	Default Value
Initial	BCFRQSEL[6:0] = 100_0000

5.2.4.2. BL_DIMM_STEP[1:0]

This register is used to select the dimming step of PWM level. It is used to select the frequency of PWM with BCFRQSEL[6:0].

Table 74. BL_DIMM_STEP[1:0]

BL_DIMM_STEP[1:0]	Dimming Steps of PWM
00	256
01	128
10	64
11	Disable

Status	Default Value
Initial	BL_DIMM_STEP[1:0] = 00

The PWM frequency is calculated with the following formula.

$$Num.\ of\ PWM\ /\ 1\ frame = (PWM\_FRQ\_SEL + 1)\ X\ 2^{BL\_DIMM\_SETP}$$

Figure108. Calculation formula of PWM frequency

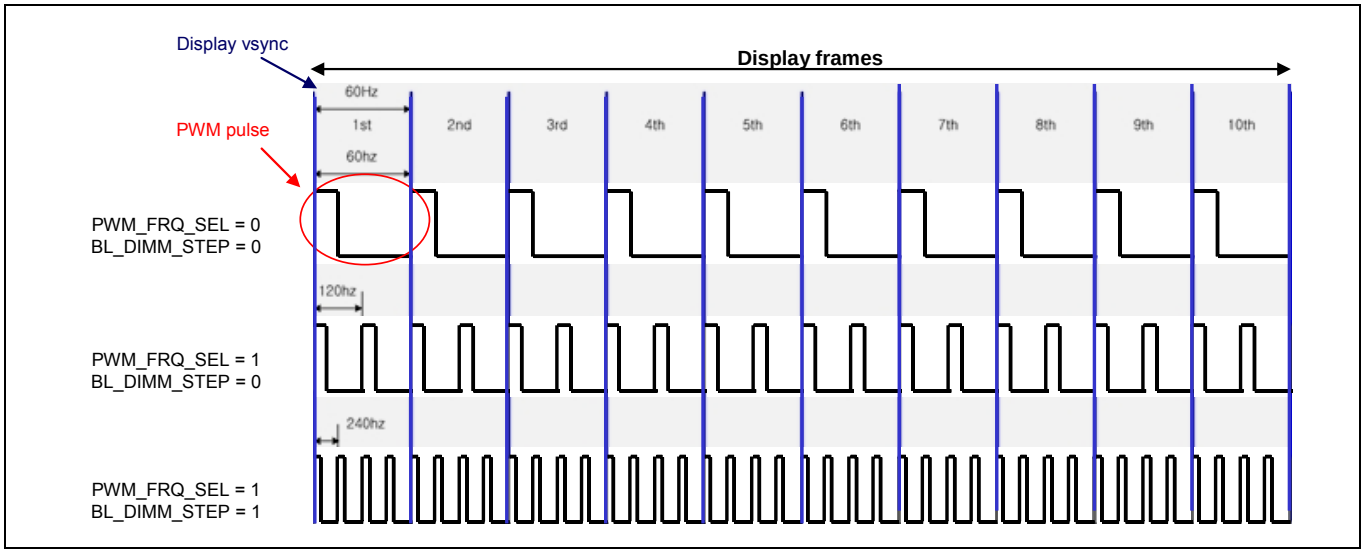


Figure109. Example of PWM frequency selection

Table 75. PWM Frequency

PWM_FRQ_SEL[6:0]	BL_DIMM_STEP[1:0]	PWM Frequency [Hz] 00	01	10	11
	Dimming Step No.	256	128	64	32
0000000		F.F. x 1	F.F. x 2	F.F. x 4	
0000001		F.F. x 2	F.F. x 4	F.F. x 8	
0000010		F.F. x 3	F.F. x 6	F.F. x 12	
0000011		F.F. x 4	F.F. x 8	F.F. x 16	
0000100		F.F. x 5	F.F. x 10	F.F. x 20	
0000101		F.F. x 6	F.F. x 12	F.F. x 24	
0000110		F.F. x 7	F.F. x 14	F.F. x 28	
0000111		F.F. x 8	F.F. x 16	F.F. x 32	
0001000		F.F. x 9	F.F. x 18	F.F. x 36	
0001001		F.F. x 10	F.F. x 20	F.F. x 40	
0001010		F.F. x 11	F.F. x 22	F.F. x 44	
0001011		F.F. x 12	F.F. x 24	F.F. x 48	
0001100		F.F. x 13	F.F. x 26	F.F. x 52	
0001101		F.F. x 14	F.F. x 28	F.F. x 56	
0001110		F.F. x 15	F.F. x 30	F.F. x 60	
0001111		F.F. x 16	F.F. x 32	F.F. x 64	
0010000		F.F. x 17	F.F. x 34	F.F. x 68	
0010001		F.F. x 18	F.F. x 36	F.F. x 72	
0010010		F.F. x 19	F.F. x 38	F.F. x 76	
0010011		F.F. x 20	F.F. x 40	F.F. x 80	
0010100		F.F. x 21	F.F. x 42	F.F. x 84	
0010101		F.F. x 22	F.F. x 44	F.F. x 88	
0010110		F.F. x 23	F.F. x 46	F.F. x 92	
0010111		F.F. x 24	F.F. x 48	F.F. x 96	
0011000		F.F. x 25	F.F. x 50	F.F. x 100	
0011001		F.F. x 26	F.F. x 52	F.F. x 104	
0011010		F.F. x 27	F.F. x 54	F.F. x 108	
0011011		F.F. x 28	F.F. x 56	F.F. x 112	
0011100		F.F. x 29	F.F. x 58	F.F. x 116	
0011101		F.F. x 30	F.F. x 60	F.F. x 120	
0011110		F.F. x 31	F.F. x 62	F.F. x 124	
0011111		F.F. x 32	F.F. x 64	F.F. x 128	
0100000		F.F. x 33	F.F. x 66	F.F. x 132	
0100001		F.F. x 34	F.F. x 68	F.F. x 136	
0100010		F.F. x 35	F.F. x 70	F.F. x 140	
0100011		F.F. x 36	F.F. x 72	F.F. x 144	
0100100		F.F. x 37	F.F. x 74	F.F. x 148	
0100101		F.F. x 38	F.F. x 76	F.F. x 152	
0100110		F.F. x 39	F.F. x 78	F.F. x 156	
0100111		F.F. x 40	F.F. x 80	F.F. x 160	
0101000		F.F. x 41	F.F. x 82	F.F. x 164	
0101001		F.F. x 42	F.F. x 84	F.F. x 168	
0101010		F.F. x 43	F.F. x 86	F.F. x 172	
0101011		F.F. x 44	F.F. x 88	F.F. x 176	
0101100		F.F. x 45	F.F. x 90	F.F. x 180	
0101101		F.F. x 46	F.F. x 92	F.F. x 184	
0101110		F.F. x 47	F.F. x 94	F.F. x 188	
0101111		F.F. x 48	F.F. x 96	F.F. x 192	
0110000		F.F. x 49	F.F. x 98	F.F. x 196	
0110001		F.F. x 50	F.F. x 100	F.F. x 200	
0110010		F.F. x 51	F.F. x 102	F.F. x 204	
0110011		F.F. x 52	F.F. x 104	F.F. x 208	
0110100		F.F. x 53	F.F. x 106	F.F. x 212	
0110101		F.F. x 54	F.F. x 108	F.F. x 216	
0110110		F.F. x 55	F.F. x 110	F.F. x 220	
0110111		F.F. x 56	F.F. x 112	F.F. x 224	
0111000		F.F. x 57	F.F. x 114	F.F. x 228	
0111001		F.F. x 58	F.F. x 116	F.F. x 232	
0111010		F.F. x 59	F.F. x 118	F.F. x 236	
0111011		F.F. x 60	F.F. x 120	F.F. x 240	
0111100		F.F. x 61	F.F. x 122	F.F. x 244	
0111101		F.F. x 62	F.F. x 124	F.F. x 248	
0111110		F.F. x 63	F.F. x 126	F.F. x 252	
0111111		F.F. x 64	F.F. x 128	F.F. x 256	

PWM_FRQ_SEL[6:0]	BL_DIMM_STEP[1:0]	PWM Frequency [Hz] 00	01	10	11
	Dimming Step No.	256	128	64	32
1000000		F.F. x 65	F.F. x 130	F.F. x 260	
1000001		F.F. x 66	F.F. x 132	F.F. x 264	
1000010		F.F. x 67	F.F. x 134	F.F. x 268	
1000011		F.F. x 68	F.F. x 136	F.F. x 272	
1000100		F.F. x 69	F.F. x 138	F.F. x 276	
1000101		F.F. x 70	F.F. x 140	F.F. x 280	
1000110		F.F. x 71	F.F. x 142	F.F. x 284	
1000111		F.F. x 72	F.F. x 144	F.F. x 288	
1001000		F.F. x 73	F.F. x 146	F.F. x 292	
1001001		F.F. x 74	F.F. x 148	F.F. x 296	
1001010		F.F. x 75	F.F. x 150	F.F. x 300	
1001011		F.F. x 76	F.F. x 152	F.F. x 304	
1001100		F.F. x 77	F.F. x 154	F.F. x 308	
1001101		F.F. x 78	F.F. x 156	F.F. x 312	
1001110		F.F. x 79	F.F. x 158	F.F. x 316	
1001111		F.F. x 80	F.F. x 160	F.F. x 320	
1010000		F.F. x 81	F.F. x 162	F.F. x 324	
1010001		F.F. x 82	F.F. x 164	F.F. x 328	
1010010		F.F. x 83	F.F. x 166	F.F. x 332	
1010011		F.F. x 84	F.F. x 168	F.F. x 336	
1010100		F.F. x 85	F.F. x 170	F.F. x 340	
1010101		F.F. x 86	F.F. x 172	F.F. x 344	
1010110		F.F. x 87	F.F. x 174	F.F. x 348	
1010111		F.F. x 88	F.F. x 176	F.F. x 352	
1011000		F.F. x 89	F.F. x 178	F.F. x 356	
1011001		F.F. x 90	F.F. x 180	F.F. x 360	
1011010		F.F. x 91	F.F. x 182	F.F. x 364	
1011011		F.F. x 92	F.F. x 184	F.F. x 368	
1011100		F.F. x 93	F.F. x 186	F.F. x 372	
1011101		F.F. x 94	F.F. x 188	F.F. x 376	
1011110		F.F. x 95	F.F. x 190	F.F. x 380	
1011111		F.F. x 96	F.F. x 192	F.F. x 384	
1100000		F.F. x 97	F.F. x 194	F.F. x 388	
1100001		F.F. x 98	F.F. x 196	F.F. x 392	
1100010		F.F. x 99	F.F. x 198	F.F. x 396	
1100011		F.F. x 100	F.F. x 200	F.F. x 400	
1100100		F.F. x 101	F.F. x 202	F.F. x 404	
1100101		F.F. x 102	F.F. x 204	F.F. x 408	
1100110		F.F. x 103	F.F. x 206	F.F. x 412	
1100111		F.F. x 104	F.F. x 208	F.F. x 416	
1101000		F.F. x 105	F.F. x 210	F.F. x 420	
1101001		F.F. x 106	F.F. x 212	F.F. x 424	
1101010		F.F. x 107	F.F. x 214	F.F. x 428	
1101011		F.F. x 108	F.F. x 216	F.F. x 432	
1101100		F.F. x 109	F.F. x 218	F.F. x 436	
1101101		F.F. x 110	F.F. x 220	F.F. x 440	
1101110		F.F. x 111	F.F. x 222	F.F. x 444	
1101111		F.F. x 112	F.F. x 224	F.F. x 448	
1110000		F.F. x 113	F.F. x 226	F.F. x 452	
1110001		F.F. x 114	F.F. x 228	F.F. x 456	
1110010		F.F. x 115	F.F. x 230	F.F. x 460	
1110011		F.F. x 116	F.F. x 232	F.F. x 464	
1110100		F.F. x 117	F.F. x 234	F.F. x 468	
1110101		F.F. x 118	F.F. x 236	F.F. x 472	
1110110		F.F. x 119	F.F. x 238	F.F. x 476	
1110111		F.F. x 120	F.F. x 240	F.F. x 480	
1111000		F.F. x 121	F.F. x 242	F.F. x 484	
1111001		F.F. x 122	F.F. x 244	F.F. x 488	
1111010		F.F. x 123	F.F. x 246	F.F. x 492	
1111011		F.F. x 124	F.F. x 248	F.F. x 496	
1111100		F.F. x 125	F.F. x 250	F.F. x 500	
1111101		F.F. x 126	F.F. x 252	F.F. x 504	
1111110		F.F. x 127	F.F. x 254	F.F. x 508	
1111111		F.F. x 128	F.F. x 256	F.F. x 512	

Note: F.F. means Frame Frequency.

When the display frame frequency is 60Hz, PWM frequency is represented at the table below.

Table 76. Example of PWM Frequency Selection

PWM_FRQ_SEL[6:0]	PWM Frequency [Hz]			
BL_DIMM_STEP[1:0]	00	01	10	11
Dimming Step No.	256	128	64	32
0000000	60	120	240	
0000001	120	240	480	
0000010	180	360	720	
0000011	240	480	960	
0000100	300	600	1200	
0000101	360	720	1440	
0000110	420	840	1680	
0000111	480	960	1920	
0001000	540	1080	2160	
0001001	600	1200	2400	
0001010	660	1320	2640	
0001011	720	1440	2880	
0001100	780	1560	3120	
0001101	840	1680	3360	
0001110	900	1800	3600	
0001111	960	1920	3840	
0010000	1020	2040	4080	
0010001	1080	2160	4320	
0010010	1140	2280	4560	
0010011	1200	2400	4800	
0010100	1260	2520	5040	
0010101	1320	2640	5280	
0010110	1380	2760	5520	
0010111	1440	2880	5760	
0011000	1500	3000	6000	
0011001	1560	3120	6240	
0011010	1620	3240	6480	
0011011	1680	3360	6720	
0011100	1740	3480	6960	
0011101	1800	3600	7200	
0011110	1860	3720	7440	
0011111	1920	3840	7680	
0100000	1980	3960	7920	
0100001	2040	4080	8160	
0100010	2100	4200	8400	
0100011	2160	4320	8640	
0100100	2220	4440	8880	
0100101	2280	4560	9120	
0100110	2340	4680	9360	
0100111	2400	4800	9600	
0101000	2460	4920	9840	
0101001	2520	5040	10080	
0101010	2580	5160	10320	
0101011	2640	5280	10560	
0101100	2700	5400	10800	
0101101	2760	5520	11040	
0101110	2820	5640	11280	
0101111	2880	5760	11520	
0110000	2940	5880	11760	
0110001	3000	6000	12000	
0110010	3060	6120	12240	
0110011	3120	6240	12480	
0110100	3180	6360	12720	
0110101	3240	6480	12960	
0110110	3300	6600	13200	
0110111	3360	6720	13440	
0111000	3420	6840	13680	
0111001	3480	6960	13920	
0111010	3540	7080	14160	
0111011	3600	7200	14400	
0111100	3660	7320	14640	
0111101	3720	7440	14880	
0111110	3780	7560	15120	
0111111	3840	7680	15360	

PWM_FRQ_SEL[6:0]	PWM Frequency [Hz]			
BL_DIMM_STEP[1:0]	00	01	10	11
Dimming Step No.	256	128	64	32
1000000	3900	7800	15600	
1000001	3960	7920	15840	
1000010	4020	8040	16080	
1000011	4080	8160	16320	
1000100	4140	8280	16560	
1000101	4200	8400	16800	
1000110	4260	8520	17040	
1000111	4320	8640	17280	
1001000	4380	8760	17520	
1001001	4440	8880	17760	
1001010	4500	9000	18000	
1001011	4560	9120	18240	
1001100	4620	9240	18480	
1001101	4680	9360	18720	
1001110	4740	9480	18960	
1001111	4800	9600	19200	
1010000	4860	9720	19440	
1010001	4920	9840	19680	
1010010	4980	9960	19920	
1010011	5040	10080	20160	
1010100	5100	10200	20400	
1010101	5160	10320	20640	
1010110	5220	10440	20880	
1010111	5280	10560	21120	
1011000	5340	10680	21360	
1011001	5400	10800	21600	
1011010	5460	10920	21840	
1011011	5520	11040	22080	
1011100	5580	11160	22320	
1011101	5640	11280	22560	
1011110	5700	11400	22800	
1011111	5760	11520	23040	
1100000	5820	11640	23280	
1100001	5880	11760	23520	
1100010	5940	11880	23760	
1100011	6000	12000	24000	
1100100	6060	12120	24240	
1100101	6120	12240	24480	
1100110	6180	12360	24720	
1100111	6240	12480	24960	
1101000	6300	12600	25200	
1101001	6360	12720	25440	
1101010	6420	12840	25680	
1101011	6480	12960	25920	
1101100	6540	13080	26160	
1101101	6600	13200	26400	
1101110	6660	13320	26640	
1101111	6720	13440	26880	
1110000	6780	13560	27120	
1110001	6840	13680	27360	
1110010	6900	13800	27600	
1110011	6960	13920	27840	
1110100	7020	14040	28080	
1110101	7080	14160	28320	
1110110	7140	14280	28560	
1110111	7200	14400	28800	
1111000	7260	14520	29040	
1111001	7320	14640	29280	
1111010	7380	14760	29520	
1111011	7440	14880	29760	
1111100	7500	15000	30000	
1111101	7560	15120	30240	
1111110	7620	15240	30480	
1111111	7680	15360	30720	

5.2.4.3. BL_MODE_IN_SLP

This register is used to select the state of PWM when driver IC is sleep in mode.

Table 77. BL_MODE_IN_SLP

BL_MODE_IN_SLP	State of PWM
0	Low
1	High

Status	Default Value
Initial	BL_MODE_IN_SLP = 0

Table 78. State of PWM

Pin	State					
	Hard Reset	SW Reset	SLPIN		SPLOUT	
			Display On	Display Off	Display On	Display Off
PWM	Low	Low	Fixed as BL_MODE_IN_SLP		Active	Low

5.2.4.4. BL_DRV_EN

This register is used to enable the LED driver IC when the IC needs the chip enable signal.

Table 79. BL_DRV_EN

BL_DRV_EN	State of BL_DRV_EN Pin
0	Low
1	High

Status	Default Value
Initial	BL_DRV_EN = 1

5.2.4.5. DT[2:0]

This register is used to select the transition time of the manual dimming function.

Table 80. DT[2:0]

DT[2:0]	Transition Time	Dimming Step
000	16 frames	16
001	24 frames	24
010	32 frames	32
011	40 frames	40
100	48 frames	48
101	56 frames	56
110	64 frames	64
111	72 frames	72

$$※\ Transition\_Time = (DT[2:0] + 2)\ X\ 8\ X \frac{1}{Display\_Frequency}$$

Figure110. Transition time of manual dimming function

Status	Default Value
Initial	DT[2:0] = 010

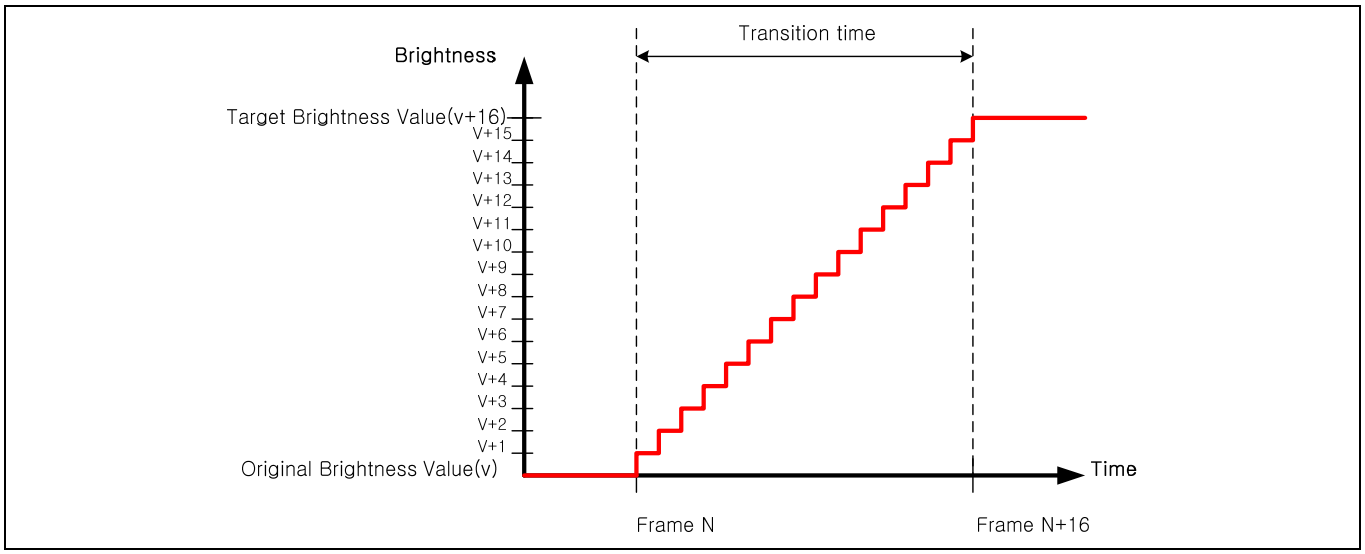


Figure111. Example of dimming function (DT[2:0] = 000)

5.2.5. MTPCTL (D0H)

D0h	MTPCTL (MTP control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	0	0	D0
Parameter	1	1	↑	-	MTP_ MODE	-	RDMTPO FFSET	MTP_ SEL	MTP_ WRB	MTP_ ERB	MTP_ LOAD	-

This command is used to control MTP.

MTP initial operation is advanced after set both MTP Test Key Command is enable.

5.2.5.1. MTP_MODE

: Set the 2nd booster operating condition.

MTP_MODE = 0: The 2nd booster operates as a user-specified condition. VGH/VGL voltages are generated as a designated level by BT2-0 setting.

MTP_MODE = 1: Available BT2-0 settings are limited only '101'.

Table 81. MTP_MODE

MTP_MODE	MTP operation mode
0	All BT2-0 settings are available (Normal operating condition)
1	Setting of BT2-0 is limited. (An MTP-programming / erasing condition)

Note. Do not execute MTP programming / erasing operation when MTP_MODE = 0.

5.2.5.2. RDMTPOFFSET

: This command selects whether reading data of 4th Parameter(D3h) is VCMOC_PO, VCMOC[4:0] or VCMH_SET[6:0].

Setting RDMTPOFFSET = "0": VCMOC_PO, VCMOC[4:0]

Setting RDMTPOFFSET = "1": VCMH_SET[6:0] = VCMH[6:0] ± VCMOC[4:0]

5.2.5.3. MTP_ERB

: This command is a setting for using MTP Data Initialization or Erase.

Setting MTP_ERB = "0": MTP Data Initialization or Erase Enable.

Setting MTP_ERB = "1": MTP Data Initialization or Erase Disable.

5.2.5.4. MTP_LOAD

: This command is a setting for using MTP data load from MTP to post-register.

Setting MTP_LOAD = “0”: MTP data load disable.

Setting MTP_LOAD = “1”: MTP data load enable.

5.2.5.5. MTP_SEL

: This command is to select ID1[7:0],ID2[7:0],ID3[7:0], VCMOC_PO, VCMOC[4:0] for using MTP value or register value.

MTP_SEL = “1”: select ID1[7:0],ID2[7:0],ID3[7:0], VCMOC_PO, VCMOC[4:0] from pre-register value.

MTP_SEL = “0”: select ID1[7:0],ID2[7:0],ID3[7:0], VCMOC_PO, VCMOC[4:0] from post-register(loaded data from MTP) value.

5.2.5.6. MTP_WRB

: This command is used to MTP programming

MTP_WRB = “0”: MTP writing enable.

MTP_WRB = “1”: MTP writing disable.

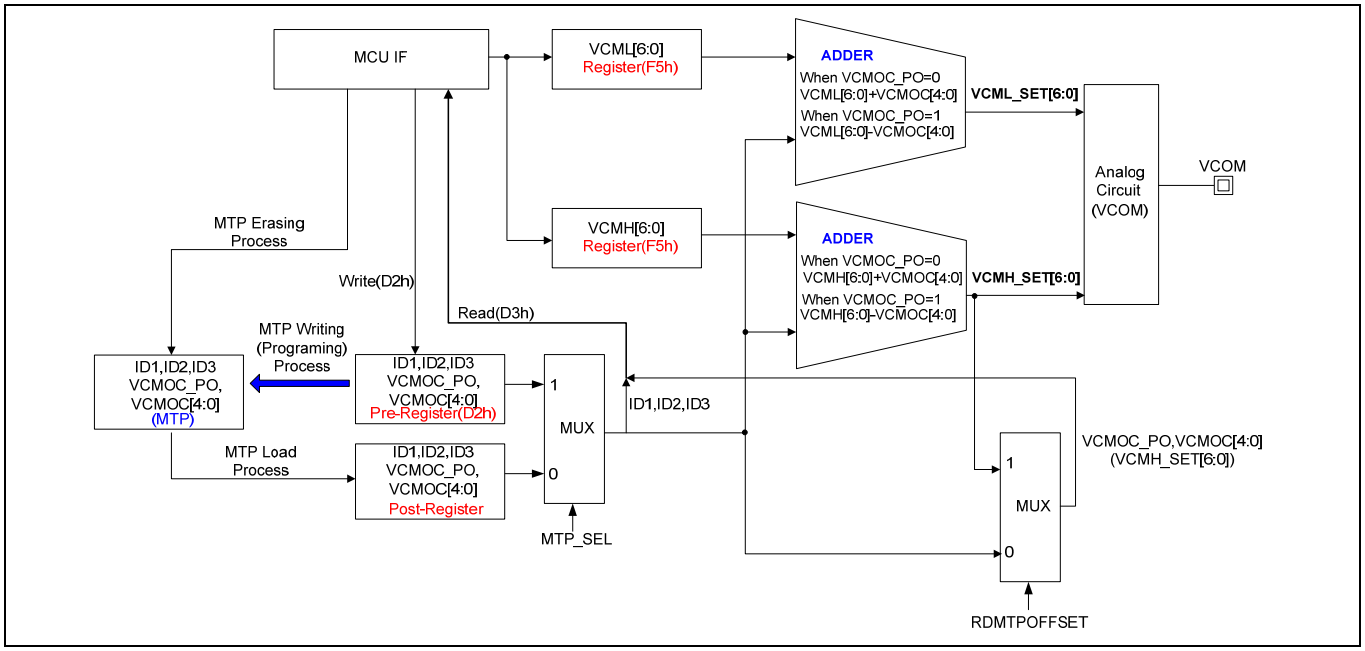


Figure112. MTP block diagram

Status	Default Value
Initial	MTP_MODE = 0, RDMTPOFFSET=0, MTP_SEL=0, MTP_WRB=1,MTP_ERB=1, MTP_LOAD=0

5.2.6. MTPACCS (D2H)

D2h	MTPACCS											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	1	0	D2
1st Parameter	1	1	↑	ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]	-
2nd Parameter	1	1	↑	DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]	-

This command writes pre-registers.

5.2.6.1. ADDR[7:0]

This is the address (Parameter) of pre-register. Refer to MTPRD(D3h) command.

Ex) When ADDR[7:0] = 1, This command accesses ID1[7:0] of pre-register.

5.2.6.2. DATA[7:0]

This is the writing data of pre-register.

Status	Default Value
Initial	ADDR[7:0]=00h, DATA[7:0]=00h

5.2.7. MTPRD (D3H)

D3h	MTPRD											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	1	1	D3
1st Parameter	1	↑	1	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	-
2nd Parameter	1	↑	1	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	-
3rd Parameter	1	↑	1	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	-
4th Parameter	1	↑	1	-	-	VCMOC_PO	VCMOC[4]	VCMOC[3]	VCMOC[2]	VCMOC[1]	VCMOC[0]	-
5th Parameter	1	↑	1	-	-	-	-	-	-	-	-	-
6th Parameter	1	↑	1	-	-	-	-	-	-	-	-	-
7th Parameter	1	↑	1	MIPIIDMS[7]	MIPIIDMS[6]	MIPIIDMS[5]	MIPIIDMS[4]	MIPIIDMS[3]	MIPIIDMS[2]	MIPIIDMS[1]	MIPIIDMS[0]	-
8th Parameter	1	↑	1	MIPIIDLS[7]	MIPIIDLS[6]	MIPIIDLS[5]	MIPIIDLS[4]	MIPIIDLS[3]	MIPIIDLS[2]	MIPIIDLS[1]	MIPIIDLS[0]	-

5.2.7.1. ID1[7:0]

This read byte identifies the LCD module's manufacturer.

5.2.7.2. ID2[7:0]

This read byte identifies the LCD module / driver version ID.

5.2.7.3. ID3[7:0]

This read byte identifies the LCD module/driver.

5.2.7.4. VCMOC_PO/VCMOC[4:0]

This read byte identifies the VCOM Offset.

VCMH_SET[6:0] = VCMH[6:0] ± VCMOC[4:0]

VCML_SET[6:0] = VCML[6:0] ± VCMOC[4:0]

Table 82. VCMOC_PO/ VCMOC[4:0]

VCMOC_PO/ VCMOC[4:0]	VCM_OFFSET	VCMOC_PO/ VCMOC[4:0]	VCM_OFFSET
000000	0	100000	0
000001	+1	100001	-1
000010	+2	100010	-2
000011	+3	100011	-3
000100	+4	100100	-4
000101	+5	100101	-5
000110	+6	100110	-6
000111	+7	100111	-7
001000	+8	101000	-8
001001	+9	101001	-9
001010	+10	101010	-10
001011	+11	101011	-11
001100	+12	101100	-12
001101	+13	101101	-13
001110	+14	101110	-14
001111	+15	101111	-15
010000	+16	110000	-16
010001	+17	110001	-17
010010	+18	110010	-18
010011	+19	110011	-19
010100	+20	110100	-20
010101	+21	110101	-21
010110	+22	110110	-22
010111	+23	110111	-23
011000	+24	111000	-24
011001	+25	111001	-25
011010	+26	111010	-26
011011	+27	111011	-27
011100	+28	111100	-28
011101	+29	111101	-29
011110	+30	111110	-30
011111	+31	111111	-31

For example, if VCMH[6:0] = “1001101”(4.0V) and VCML[6:0] = “1100110”(-0.5V) and VCMOC_PO/VCMOC[4:0] = 100011 are selected, then VCM_OFFSET is “-3,” and therefore VCMH_SET[6:0] is “1001010,” which results in VCOM high level voltage = 3.94V from VCMH[6:0] table, VCML_SET[6:0] is “1100011,” which results in VCOM low level voltage = 0.56V from VCML[6:0] table.

Note that VCMH_SET[6:0]/VCML_SET[6:0] cannot be set to the value above “1111111” or below “0000000,” that is, 128 ≥ VCMH[6:0](VCML[6:0]) + VCMOC_PO/VCMOC[4:0] ≥ 0.

Note: VCMH_SET[6:0] is VCMH[6:0] ± Post-register(VCOMOC) when MTP_SEL=0 and is VCMH[6:0] ± Pre-register(VCOMOC) when MTP_SEL=1. Refer to figure 112. MTP block diagram.

5.2.7.5. MIPIIDMS[7:0]

This read byte identifies the MS byte of Supplier ID.

5.2.7.6. MIPIIDLS[7:0]

This read byte identifies the LS byte of Supplier ID.

* MIPIIDMS and MIPIIDLS are NOT stored in MTP(post-register) but stored in pre-register.

5.2.8. DSTB (DFH)

DFh	DSTB											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	1	1	DF
Parameter	1	1	↑	-	-	-	-	-	-	-	DSTB	-

This command enters deep standby mode. Refer to 4.8 Deep Standby Mode.

Table 83. DSTB

DSTB	State
0	Deep Standby Off
1	Deep Standby In

Status	Default Value
Initial	DSTB = 0

5.2.9. PASSWD1 (F0H)

F0h	Password command for level 2											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	0	0	F0
1st Parameter	1	1	↑	TEST_KEY[7]	TEST_KEY[6]	TEST_KEY[5]	TEST_KEY[4]	TEST_KEY[3]	TEST_KEY[2]	TEST_KEY[1]	TEST_KEY[0]	-
2nd Parameter	1	1	↑	TEST_KEY[7]	TEST_KEY[6]	TEST_KEY[5]	TEST_KEY[4]	TEST_KEY[3]	TEST_KEY[2]	TEST_KEY[1]	TEST_KEY[0]	-

When the Parameter (TEST_KEY[7:0]) of this command is inputted by 5Ah, this command enable level 2 command input. When the Parameter (TEST_KEY[7:0]) of this command is inputted by except 5Ah, this command disable level 2 command input.

Status	Default Value
Initial	TEST_KEY[7:0]=8'b01011010(5Ah)

5.2.10. PASSWD2 (F1H)

F1h	Password command for level 2											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	0	1	F1
1st Parameter	1	1	↑	TEST_KEY7	TEST_KEY6	TEST_KEY5	TEST_KEY4	TEST_KEY3	TEST_KEY2	TEST_KEY1	TEST_KEY0	-
2nd Parameter	1	1	↑	TEST_KEY7	TEST_KEY6	TEST_KEY5	TEST_KEY4	TEST_KEY3	TEST_KEY2	TEST_KEY1	TEST_KEY0	-

When the Parameter (TEST_KEY[7:0]) of this command is inputted by 5Ah, this command enable level 2 command input. When the Parameter (TEST_KEY[7:0]) of this command is inputted by except 5Ah, this command disable level 2 command input.

Status	Default Value
Initial	TEST_KEY[7:0]=8'b01011010(5Ah)

5.2.11. DISCTL (F2H)

F2h	DISCTL (Display Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	1	0	F2
1st Parameter	1	1	↑	-	-	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	-
2nd Parameter	1	1	↑	NHW [7]	NHW [6]	NHW [5]	NHW [4]	NHW [3]	NHW [2]	NHW [1]	NHW [0]	-
3rd Parameter	1	1	↑	-	BLKINV	PINDINV	PNDINV	PIINV	IINV	PINV	NINV	-
4th Parameter	1	1	↑	NVBP [7]	NVBP [6]	NVBP [5]	NVBP [4]	NVBP [3]	NVBP [2]	NVBP [1]	NVBP [0]	-
5th Parameter	1	1	↑	NVFP [7]	NVFP [6]	NVFP [5]	NVFP [4]	NVFP [3]	NVFP [2]	NVFP [1]	NVFP [0]	-
6th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
7th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
8th Parameter	1	1	↑	-	DIV_SRC [4]	DIV_SRC [3]	DIV_SRC [2]	DIV_SRC [1]	DIV_SRC [0]	TE_ST [9]	TE_ST [8]	-
9th Parameter	1	1	↑	TE_ST [7]	TE_ST [6]	TE_ST [5]	TE_ST [4]	TE_ST [3]	TE_ST [2]	TE_ST [1]	TE_ST [0]	-
10th Parameter	1	1	↑	-	-	-	-	-	TE_SEL	TE_ED [9]	TE_ED [8]	-
11th Parameter	1	1	↑	TE_ED [7]	TE_ED [6]	TE_ED [5]	TE_ED [4]	TE_ED [3]	TE_ED [2]	TE_ED [1]	TE_ED [0]	-
12th Parameter	1	1	↑	-	-	-	-	-	-	-	REV	-
13th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
14th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
15th Parameter	1	1	↑	PIHW [7]	PIHW [6]	PIHW [5]	PIHW [4]	PIHW [3]	PIHW [2]	PIHW [1]	PIHW [0]	-
16th Parameter	1	1	↑	PIVBP [7]	PIVBP [6]	PIVBP [5]	PIVBP [4]	PIVBP [3]	PIVBP [2]	PIVBP [1]	PIVBP [0]	-
17th Parameter	1	1	↑	PIVFP [7]	PIVFP [6]	PIVFP [5]	PIVFP [4]	PIVFP [3]	PIVFP [2]	PIVFP [1]	PIVFP [0]	-

5.2.11.1. NL[5:0]

: Set the display duty. The total number of scan line can be set in the range between 8-line and 320-line. A step size is 8-line.

Table 84. NL[5:0]

NL[5:0]	Total number of scan line
000000	Setting disabled
000001	8
000010	16
….	….
101000	320
110110~111111	Setting disabled

Status	Default Value
Initial	NL[5:0] = 101000 (320)

Note: ML (MADCTL D4) setting low when Display size < 320.

5.2.11.2. NHW[7:0]/PIHW[7:0]

: Set the horizontal clock (CL1) period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

Table 85. NHW[7:0]/PIHW[7:0]

*HW[7:0]	Number of Display Clock
00000000~00011010	Setting disabled
01001000	72
01001001	73
…….	……
11111110	254
11111111	255

Note: OSCK is the internal oscillator clock.

Status	Default Value
Initial	NHW[7:0] = 10010100 (148) PIHW[7:0] = 10010100 (148)

5.2.11.3. NINV / PINV / IINV / PIINV / PNDINV / PINDINV / BLKINV

: Select the panel driving method in the Normal mode / Partial mode (display area) / Idle mode / Partial-Idle mode (display area) / Partial mode (non-display area) / Partial-Idle mode (non-display area) / Blanking display, respectively. Either frame inversion method or line inversion method can be selected.

Table 86. NINV/PINV/IINV/PIINV/PNDINV/PINDINV/BLKINV

*INV	Panel driving method
0	Frame inversion
1	Line inversion

Status	Default Value
Initial	NINV, PINV = 1 IINV, PIINV, PNDINV, PINDINV,BLKINV = 0

*non-display area is (porch + non display area) when partial mode.

5.2.11.4. NVBP[7:0]/ PIVBP[7:0]

: Set the vertical back-porch period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

Table 87. NVBP[7.0]/ PIVBP[7.0]

*VBP[7:0]	Number of Horizontal Line
00000000	Setting disable
00000001	Setting disable
00000010	2
…….	……
11111101	253
11111110	254
11111111	255

Status	Default Value
Initial	*BP[7:0] = 00001000 (8)

5.2.11.5. NVFP[7:0]/PIVFP[7:0]

: Set the vertical front-porch period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

Table 88. NVFP[7:0]/PIVFP[7:0]

*VFP[7:0]	Number of Horizontal Line
00000000	Setting disable
00000001	Setting disable
00000010	2
…….	……
11111101	253
11111110	254
11111111	255

Status	Default Value
Initial	*FP[7:0] = 00001000 (8)

5.2.11.6. REV

: Select whether the liquid crystal type is normally white type or normally black type.

Table 89. REV

REV	Liquid crystal type
0	Normally black
1	Normally white

Status	Default Value
Initial	REV = 0

5.2.11.7. DIV_SRC[4:0]

: This controls the period of internal track signal.

Table 90. DIV_SRC[4:0]

DIV_SRC	Track Period(number of oscillator clock)
00000	Settting disable
…..	…..
00100	Setting disable
00101	5
00110	6
…..	…..
01101	13
01110	14
01111	15
10000	16
10001	17
10010	18
10010	Setting disable
…..	….
11111	Setting disable

Status	Default Value
Initial	DIV_SRC [4:0] = 00101

5.2.11.8. TE_ST[9:0]

: Select the time when TE signal rises to high level(VDD3).

This command is available when TE_SEL = 1 .

Status	Default Value
Initial	TE_ST[9:0] = 01_0100_1000(328)

5.2.11.9. TE_SEL

: Select whether the liquid crystal type is normally white type or normally black type.

Table 91. TE_SEL

TE_SEL	TE Output Select
0	Level1 TE Ouptut
1	Level2 TE Output

Status	Default Value
Initial	TE_SEL = 0

5.2.11.10. TE_ED[9:0]

: Select the time when TE signal falls to low level(VSS3).

This command is available when TE_SEL = 1 .

Status	Default Value
Initial	TE_ED[9:0] = 00_0000_0111(7)

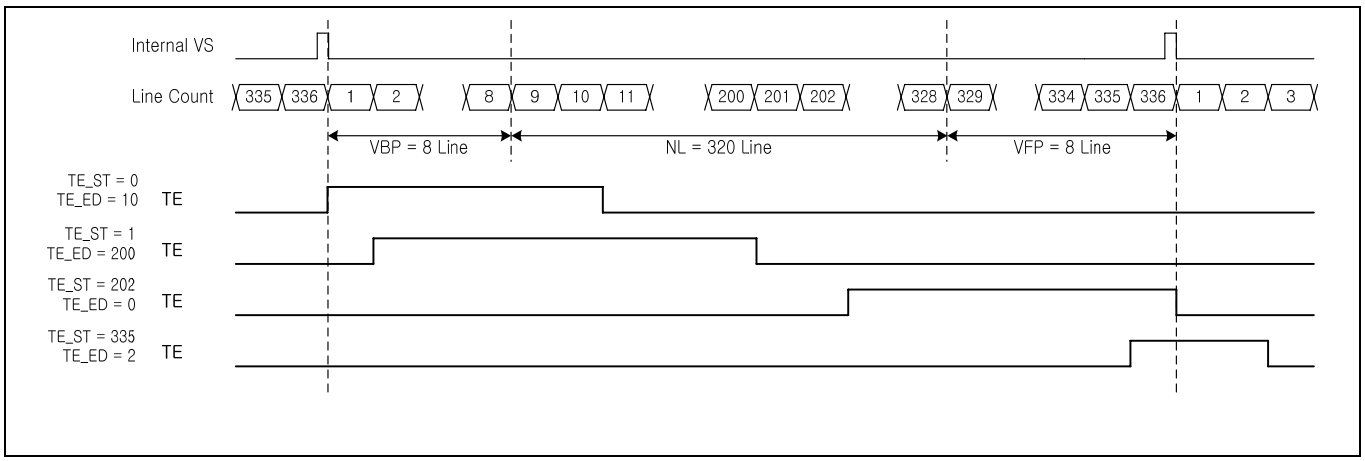


Figure113. TE Timing diagram

5.2.12. MANPWRSEQ (F3H)

F3h	MANPWRSEQ (Power Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	1	1	F3
1st Parameter	1	1	↑	-	-	-	-	-	-	-	APON	-
2nd Parameter	1	1	↑	VCL_EN	VGL_EN	VGH_EN	VGHFREE1_EN	AVDD_EN	VCI1_2ND_EN	VCI1_1ST_EN	VCIR_EN	-
3rd Parameter	1	1	↑	-	-	-	GATE_ON	VCOM_EN	GVDD_EN	VGHFREE2_EN	AVDD2_EN	-
4th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
5th Parameter	1	1	↑	-	-	-	-	-	-	D1	D0	-

5.2.12.1. APON

: This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the automatic boosting sequence starter is halted and the booster circuits are operated independently by AVDD_EN, VGH_EN, VGL_EN and VCL_EN bits. In case of APON=1, booster circuits are operated automatically and sequentially.

Status	Default Value
Initial	APON = 1

5.2.12.2. VCIR_EN

: Internal VCIR generation amplifier operation control bit. When VCIR_EN=0, VCIR voltage is not generated.

Status	Default Value
Initial	VCIR_EN = 0

5.2.12.3. VCI1_1ST_EN/VCI1_2ND_EN

: Internal VCI1 generation amplifier operation control bit. When VCI1_1ST_EN=0, VCI1 voltage is not generated.

Status	Default Value
Initial	VCI1_1ST_EN = 0, VCI1_2ND_EN = 0

5.2.12.4. AVDD_EN

: This is an operation-starting bit for the booster circuit1. In case of AVDD_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the AVDD_EN = 1

Status	Default Value
Initial	AVDD_EN = 0

5.2.12.5. VGHFREE1_EN/VGHFREE2_EN

: These are about the booster circuit 2(VGH). These prevent latch-up event.

Status	Default Value
Initial	VGHFREE1_EN = 0,VGHFREE2_EN = 0

5.2.12.6. VGH_EN

: This is an operation-starting bit for the booster circuit 2(VGH). In case of VGH_EN, the circuit is stopped and vice versa. For further information about timing for adjusting to the VGH_EN= 1.

Status	Default Value
Initial	VGH_EN = 0

5.2.12.7. VGL_EN

: This is an operation-starting bit for the booster circuit 2(VGL). In case of VGL_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the VGL_EN = 1.

Status	Default Value
Initial	VGL_EN = 0

5.2.12.8. VCL_EN

: This is an operation-starting bit for the booster circuit 3(VCL). In case of VCL_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the VCL_EN= 1.

Status	Default Value
Initial	VCL_EN = 0

5.2.12.9. VCOM_EN/GVDD_EN

: This is an operation-starting bit for GVDD/VCOM amplifiers. In case of VCOM/_ENVCOM_EN = 0, the amplifier circuits are stopped. On the other hand, the operation of the amplifiers is getting started when VCOM_EN/GVDD_EN = 1. For further information about timing for adjusting to VCOM_EN/GVDD_EN = 1.

Status	Default Value
Initial	VCOM_EN = 0, GVDD_EN = 0

5.2.12.10. GATE_ON

: This is a gate on/off control signal. All gate outputs are set to be gate off level when GATE_ON = 0.
When GATE_ON = 1, gate driver is working: G1 to G320 output is either VGH or VGL level.

Status	Default Value
Initial	GATE_ON = 0

5.2.12.11. D[1:0]

: This controls the status of source, VCOM, gate.

Table 92. D[1:0]

D[1:0]	GATE_ON	Source	VCOM	Gate
00	Don't care	AVSS	AVSS	VGL
01	0	AVSS	AVSS	VGL
01	1	AVSS	AVSS	Operate
10	0	Binary	Operate	VGL
10	1	Binary	Operate	Operate
11	0	Amplifier	Operate	VGL
11	1	Amplifier	Operate	Operate

Status	Default Value
Initial	D[1:0] = 00

5.2.13. PWRCTL (F4H)

F4h	PWRCTL (Power Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	0	0	F4
1st Parameter	1	1	↑	-	-	-	-	VC[3]	VC[2]	VC[1]	VC[0]	-
2nd Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
3rd Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
4th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
5th Parameter	1	1	↑	-	SEQ2 [2]	SEQ2 [1]	SEQ2 [0]	-	SEQ1 [2]	SEQ1 [1]	SEQ1 [0]	-
6th Parameter	1	1	↑	-	SEQ4 [2]	SEQ4 [1]	SEQ4 [0]	-	SEQ3 [2]	SEQ3 [1]	SEQ3 [0]	-
7th Parameter	1	1	↑	-	-	-	-	-	SEQ5 [2]	SEQ5 [1]	SEQ5 [0]	-
8th Parameter	1	1	↑	-	-	BLK_SEL	BLK_OFF	-	-	BLK_FRAME[1]	BLK_FRAM[0]	-
9th Parameter	1	1	↑	-	-	NDC3[1]	NDC3[0]	NDC2[1]	NDC2[0]	NDC1[1]	NDC1[0]	-
10th Parameter	1	1	↑	-	NGVD[6]	NGVD[5]	NGVD[4]	NGVD[3]	NGVD[2]	NGVD[1]	NGVD[0]	-
11th Parameter	1	1	↑	-	-	-	-	-	NBT[2]	NBT[1]	NBT[0]	-
12th Parameter	1	1	↑	-	-	PIDC3[1]	PIDC3[0]	PIDC2[1]	PIDC2[0]	PIDC1[1]	PIDC1[0]	-
13th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
14th Parameter	1	1	↑	-	-	-	-	-	PIBT[2]	PIBT[1]	PIBT[0]	-
15th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
16th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
17th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
18th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
19th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
20th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-

5.2.13.1. VC[3:0]

: This register is used to set the VCI1 voltage. These bits set the VCI1 voltage up to 3V as the nominal output (upper limit value may depend on VCI voltage)

Table 93. VC[3:0]

VC3	VC2	VC1	VC0	VCI1
0	0	0	0	2.100V
0	0	0	1	2.160V
0	0	1	0	2.220V
0	0	1	1	2.280V
0	1	0	0	2.340V
0	1	0	1	2.400V
0	1	1	0	2.460V
0	1	1	1	2.520V
1	0	0	0	2.580V
1	0	0	1	2.640V
1	0	1	0	2.700V
1	0	1	1	2.760V
1	1	0	0	2.820V
1	1	0	1	2.880V
1	1	1	0	2.940V
1	1	1	1	3.000V

Note: Do not set any higher VCI1 level than VCI -0.15V.

Status	Default Value
Initial	VC[3:0] = 1011

5.2.13.2. SEQ1[2:0]

: : This register is used to set the period between from start of AVDD boosting to start of VGH charging when sleep-out command is applied on sleep-in mode. (APON = 1)

Table 94. SEQ1[2:0]

SEQ1[2:0]	VGHFREE1_EN on timing
	Period time from AVDD boosting start to VGH charging start (unit : frame)
000	Set disable
001	1/4
010	2/4
011	3/4
100	1
101	5/4
110	6/4
111	7/4

Status	Default Value
Initial	SEQ1[2:0] = 001

5.2.13.3. SEQ2[2:0]

: This register is used to set the period between from start of VGH charging to start of VGH boosting when sleep-out command is applied on sleep-in mode. (APON = 1)

Table 95. SEQ2[2:0]

SEQ2[2:0]	VGH_EN on timing
	Period time from VGH charging start to VGH boosting start (unit : frame)
000	Set disable
001	Set disable
010	2/4
011	3/4
100	1
101	5/4
110	6/4
111	7/4

Status	Default Value
Initial	SEQ2[2:0] = 010

5.2.13.4. SEQ3[2:0]

: This register is used to set the period between from start of VGH boosting to start of VGL boosting when sleep-out command is applied on sleep-in mode. (APON = 1)

Table 96. SEQ3[2:0]

SEQ3[2:0]	VGL_EN on timing
	Period time from VGH boosting start to VGL boosting start (unit : frame)
000	Set disable
001	Set disable
010	Set disable
011	Set disable
100	Set disable
101	Set disable
110	Set disable
111	7/4

Status	Default Value
Initial	SEQ3[2:0] = 111

5.2.13.5. SEQ4[2:0]

: This register is used to set the period between from start of VGL boosting to VCL boosting when sleep-out command is applied on sleep-in mode. (APON = 1)

Table 97. SEQ4[2:0]

SEQ4[2:0]	VCL_EN on timing
	Period time from VGL boosting start to VCL boosting start (unit : frame)
000	Set disable
001	Set disable
010	Set disable
011	Set disable
100	1
101	5/4
110	6/4
111	7/4

Status	Default Value
Initial	SEQ4[2:0] = 100

5.2.13.6. SEQ5[2:0]

: This register is used to set the period between from VCL boosting to GVDD/VCOM amplifier turn-on when sleep-out command is applied on sleep-in mode(APON = 1)

Table 98. SEQ5[2:0]

SEQ5[2:0]	VGL_EN on timing
	Period time from VCL boosting start to AMP_EN boosting start (unit : frame)
000	Set disable
001	1/4
010	2/4
011	3/4
100	1
101	5/4
110	6/4
111	7/4

Status	Default Value
Initial	SEQ5[2:0] = 001

5.2.13.7. BLK_SEL

: BLK_SEL selects the source driving method(Amplifier or Binary mode) in blanking display period.

BLK_SEL = 0 : Source operates in amplifier mode in normal display mode, Source operates in binary mode in idle display mode.

BLK_SEL = 1 : Source only operates in binary mode.

Status	Default Value
Initial	BLK_SEL=0

5.2.13.8. BLK_OFF

: BLK_OFF selects whether blanking display uses or not on display off sequence.

BLK_OFF = 0 : Blanking display uses on display off sequence.

BLK_OFF = 1 : Blanking display don’t use on display off sequence.

Status	Default Value
Initial	BLK_OFF=0

5.2.13.9. BLK_FRAME[1:0]

: BLK_FRAME[1:0] select the period of blanking display(0~ 3frames) on display on/off sequence.

Status	Default Value
Initial	BLK_FRAME[1:0] = 10 (2frames)

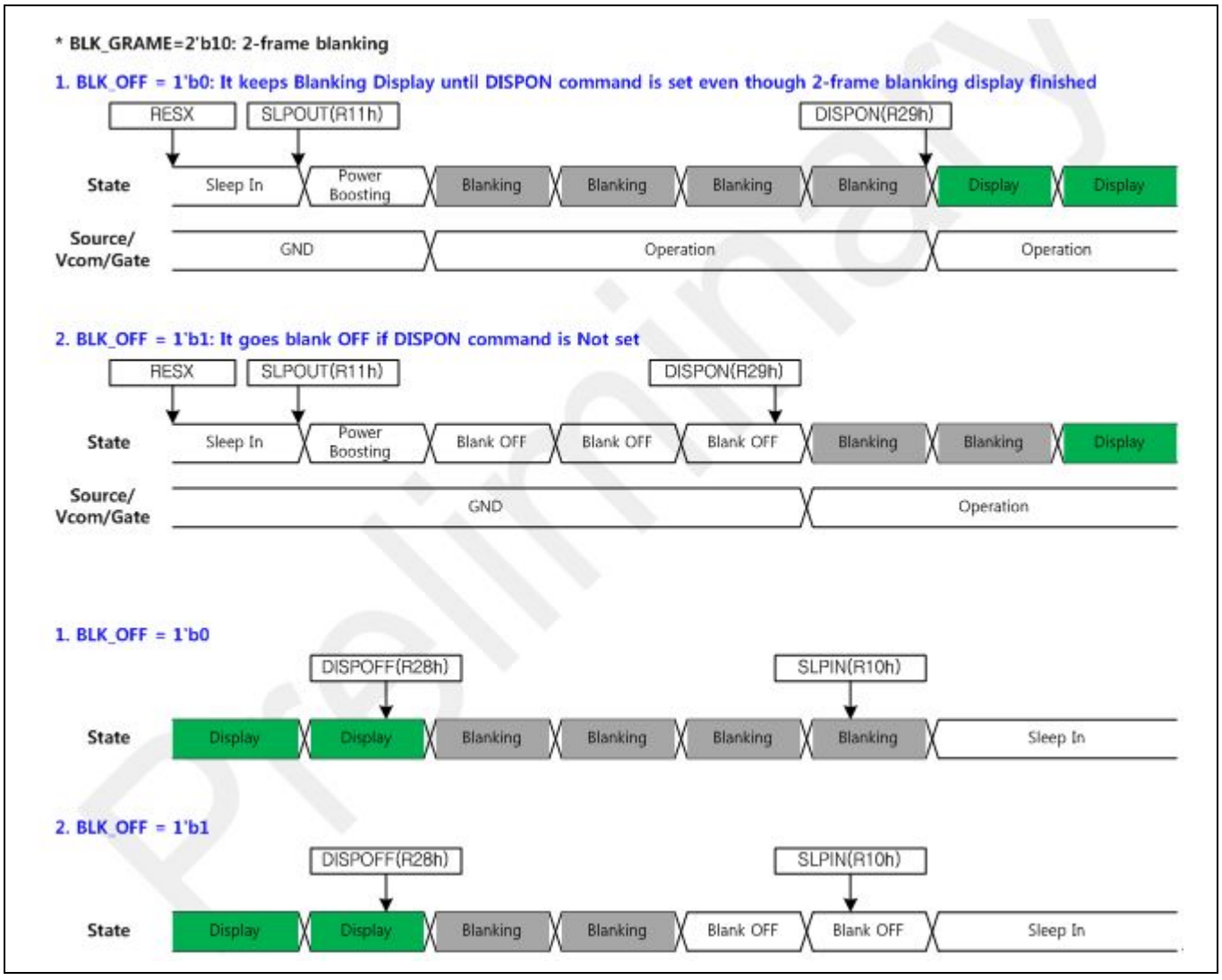


Figure114. BLK_OFF Timing diagram

5.2.13.10. NDC3[1:0] / PIDC3[1:0]

: The operating frequency in the booster circuit 3 is selected. PIDC3 is applied in Idle Partial mode.

Table 99. NDC3[1:0] / PIDC3[1:0]

NDC31/ PIDC31	NDC30/ PIDC30	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK3)
0	0	1:4
0	1	1:2
1	0	1:1
1	1	Setting disabled

Note. DCCLK3 is pumping clock for booster circuit3

Status	Default Value
Initial	NDC3[1:0], PIDC3[1:0] = 10

5.2.13.11. NDC2[1:0] / PIDC2[1:0]

: The operating frequency in the booster circuit 2 is selected. PIDC2 is applied in Idle Partial mode.

Table 100.NDC2[1:0] / PIDC2[1:0]

NDC21/ PIDC21	DC20/ PIDC20	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK2)
0	0	1:2
0	1	1:1
1	0	1:0.5
1	1	1:0.25

Note. DCCLK2 is pumping clock for booster circuit2

Status	Default Value
Initial	NDC2[1:0], PIDC2[1:0] = 10

5.2.13.12. NDC1[1:0] / PIDC1[1:0]

: The operating frequency in the booster circuit1 is selected. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption. PIDC1 is applied in Idle Partial mode.

Table 101.NDC1[1:0] / PIDC1[1:0]

NDC11/ PIDC11	NDC10/ PIDC10	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK1)
0	0	1:4
0	1	1:2
1	0	1:1
1	1	Setting disabled

Note. DCCLK1 is pumping clock for booster circuit1. f(1H) is horizontal frequency (1 raster-row)

Status	Default Value
Initial	NDC1[1:0], PIDC1[1:0] = 10

5.2.13.13. PIBT[2:0] / NBT[2:0]

: The output factor of booster is switched. Adjust scale factor of the booster circuit by the voltage used. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

PIBT is applied in Idle Partial mode.

Table 102.PIBT[2:0] / NBT[2:0]

PIBT1/ NBT2	PIBT1/ NBT1	IPBP0/ NBT0	VGH	VGL	Notes*	
0	0	0	4 X VCI1	-3 X VCI1	11.00V	-8.25V
0	0	1	4 X VCI1	-4 X VCI1	11.00V	-11.00V
0	1	0	5 X VCI1	-3 X VCI1	13.75V	-8.25V
0	1	1	5 X VCI1	-4 X VCI1	13.75V	-11.00V
1	0	0	5 X VCI1	-5 X VCI1	13.75V	-13.75V
1	0	1	6 X VCI1	-3 X VCI1	16.50V	-8.25V
1	1	0	6 X VCI1	-4 X VCI1	16.50V	-11.00V
1	1	1	6 X VCI1	-5 X VCI1	16.50V	-13.75V

Note: The values in table above are example of nominal upper-limit by register setting when VCI1=3.0V.

Do not set any higher VGH level than 16.5V.

Status	Default Value
Initial	PIBT[2:0], NBT[2:0] = 101

5.2.13.14. NGVD[5:0]

: This register is used to set the amplifying factor of the GVDD voltage on Normal Mode (the voltage for the Gamma voltage). It allows ranging from 2.46V to 5.00V.

Table 103.NGVD[6:0]

NGVD6-0	GVDD Voltage	NGVD6-0	GVDD Voltage	NGVD6-0	GVDD Voltage	NGVD6-0	GVDD Voltage
0000000	2.46V	0100000	3.10V	1000000	3.74V	1100000	4.38V
0000001	2.48V	0100001	3.12V	1000001	3.76V	1100001	4.40V
0000010	2.50V	0100010	3.14V	1000010	3.78V	1100010	4.42V
0000011	2.52V	0100011	3.16V	1000011	3.80V	1100011	4.44V
0000100	2.54V	0100100	3.18V	1000100	3.82V	1100100	4.46V
0000101	2.56V	0100101	3.20V	1000101	3.84V	1100101	4.48V
0000110	2.58V	0100110	3.22V	1000110	3.86V	1100110	4.50V
0000111	2.60V	0100111	3.24V	1000111	3.88V	1100111	4.52V
0001000	2.62V	0101000	3.26V	1001000	3.90V	1101000	4.54V
0001001	2.64V	0101001	3.28V	1001001	3.92V	1101001	4.56V
0001010	2.66V	0101010	3.30V	1001010	3.94V	1101010	4.58V
0001011	2.68V	0101011	3.32V	1001011	3.96V	1101011	4.60V
0001100	2.70V	0101100	3.34V	1001100	3.98V	1101100	4.62V
0001101	2.72V	0101101	3.36V	1001101	4.00V	1101101	4.64V
0001110	2.74V	0101110	3.38V	1001110	4.02V	1101110	4.66V
0001111	2.76V	0101111	3.40V	1001111	4.04V	1101111	4.68V
0010000	2.78V	0110000	3.42V	1010000	4.06V	1110000	4.70V
0010001	2.78V	0110001	3.44V	1010001	4.08V	1110001	4.72V
0010010	2.80V	0110010	3.46V	1010010	4.10V	1110010	4.74V
0010011	2.82V	0110011	3.48V	1010011	4.12V	1110011	4.76V
0010100	2.84V	0110100	3.50V	1010100	4.14V	1110100	4.78V
0010101	2.86V	0110101	3.52V	1010101	4.16V	1110101	4.80V
0010110	2.88V	0110110	3.54V	1010110	4.18V	1110110	4.82V
0010111	2.90V	0110111	3.56V	1010111	4.20V	1110111	4.84V
0011000	2.92V	0111000	3.58V	1011000	4.22V	1111000	4.86V
0011001	2.94V	0111001	3.60V	1011001	4.24V	1111001	4.88V
0011010	2.96V	0111010	3.62V	1011010	4.26V	1111010	4.90V
0011011	2.98V	0111011	3.64V	1011011	4.28V	1111011	4.92V
0011100	3.02V	0111100	3.66V	1011100	4.20V	1111100	4.94V
0011101	3.04V	0111101	3.68V	1011101	4.32V	1111101	4.96V
0011110	3.06V	0111110	3.70V	1011110	4.34V	1111110	4.98V
0011111	3.08V	0111111	3.72V	1011111	4.36V	1111111	5.00V

Note. Don't set any higher GVDD level than AVDD-0.3V

Status	Default Value
Initial	NGVD[5:0] = 1100110(4.5V)

5.2.14. VCMCTL (F5H)

F5h	VCMCTL (VCOM Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	0	1	F5
1st Parameter	1	1	↑	-	-	-	-	-	-	-	VCOMG	-
2nd Parameter	1	1	↑	-	VCMH[6]	VCMH[5]	VCMH[4]	VCMH[3]	VCMH[2]	VCMH[1]	VCMH[0]	-
3rd Parameter	1	1	↑	-	VCML[6]	VCML[5]	VCML[4]	VCML[3]	VCML[2]	VCML[1]	VCML[0]	-
4th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
5th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
6th Parameter	1	1	↑	-	-	-	VCIR1[4]	VCIR1[3]	VCIR1[2]	VCIR1[1]	VCIR1[0]	-
7th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
8th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
9th Parameter	1	1	↑	-	-	-	-	NVC_BLK[1]	NVC_BLK[0]	-	NVC_ND	-
10th Parameter	1	1	↑	-	-	-	-	PIVC_BLK[1]	PIVC_BLK[0]	-	PIVC_ND	-
11th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
12th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-

5.2.14.1. VCOMG

When VCOMG = 1, low level of VCOM signal is to be fixed at VSSA. Therefore, the amplitude of VCOM signal is determined as |VCOMH – VSSA| regardless of VCML setting.

Status	Default Value
Initial	VCOMG = 0

5.2.14.2. VCMH[6:0]

Set the VCOMH voltage (a high level voltage at the Vcom alternating drive), It allows ranging from 2.46V to 5.00V.

Table 104.VCOMH setting

VCMH6-0	VCOMH Voltage	VCMH6-0	VCOMH Voltage	VCMH6-0	VCOMH Voltage	VCMH6-0	VCOMH Voltage
0000000	2.46V	0100000	3.10V	1000000	3.74V	1100000	4.38V
0000001	2.48V	0100001	3.12V	1000001	3.76V	1100001	4.40V
0000010	2.50V	0100010	3.14V	1000010	3.78V	1100010	4.42V
0000011	2.52V	0100011	3.16V	1000011	3.80V	1100011	4.44V
0000100	2.54V	0100100	3.18V	1000100	3.82V	1100100	4.46V
0000101	2.56V	0100101	3.20V	1000101	3.84V	1100101	4.48V
0000110	2.58V	0100110	3.22V	1000110	3.86V	1100110	4.50V
0000111	2.60V	0100111	3.24V	1000111	3.88V	1100111	4.52V
0001000	2.62V	0101000	3.26V	1001000	3.90V	1101000	4.54V
0001001	2.64V	0101001	3.28V	1001001	3.92V	1101001	4.56V
0001010	2.66V	0101010	3.30V	1001010	3.94V	1101010	4.58V
0001011	2.68V	0101011	3.32V	1001011	3.96V	1101011	4.60V
0001100	2.70V	0101100	3.34V	1001100	3.98V	1101100	4.62V
0001101	2.72V	0101101	3.36V	1001101	4.00V	1101101	4.64V
0001110	2.74V	0101110	3.38V	1001110	4.02V	1101110	4.66V
0001111	2.76V	0101111	3.40V	1001111	4.04V	1101111	4.68V
0010000	2.78V	0110000	3.42V	1010000	4.06V	1110000	4.70V
0010001	2.78V	0110001	3.44V	1010001	4.08V	1110001	4.72V
0010010	2.80V	0110010	3.46V	1010010	4.10V	1110010	4.74V
0010011	2.82V	0110011	3.48V	1010011	4.12V	1110011	4.76V
0010100	2.84V	0110100	3.50V	1010100	4.14V	1110100	4.78V
0010101	2.86V	0110101	3.52V	1010101	4.16V	1110101	4.80V
0010110	2.88V	0110110	3.54V	1010110	4.18V	1110110	4.82V
0010111	2.90V	0110111	3.56V	1010111	4.20V	1110111	4.84V
0011000	2.92V	0111000	3.58V	1011000	4.22V	1111000	4.86V
0011001	2.94V	0111001	3.60V	1011001	4.24V	1111001	4.88V
0011010	2.96V	0111010	3.62V	1011010	4.26V	1111010	4.90V
0011011	2.98V	0111011	3.64V	1011011	4.28V	1111011	4.92V
0011100	3.02V	0111100	3.66V	1011100	4.20V	1111100	4.94V
0011101	3.04V	0111101	3.68V	1011101	4.32V	1111101	4.96V
0011110	3.06V	0111110	3.70V	1011110	4.34V	1111110	4.98V
0011111	3.08V	0111111	3.72V	1011111	4.36V	1111111	5.00V

Note. Don’t set any higher VCOM high level than AVDD-0.3V. VCOMH voltage should be higher than VCI.

Status	Default Value
Initial	VCMH[6:0] = 1001101 (4.0V)

5.2.14.3. VCML[6:0]

Set the VCOML voltage (a low level voltage at the Vcom alternating drive), It allows ranging from -2.54V to 0V.

Table 105.VCOML setting

VCML6-0	VCOML Voltage	VCML6-0	VCOML Voltage	VCML6-0	VCOML Voltage	VCML6-0	VCOML Voltage
0000000	-2.54V	0100000	-1.90V	1000000	-1.26V	1100000	-0.62V
0000001	-2.52V	0100001	-1.88V	1000001	-1.24V	1100001	-0.60V
0000010	-2.50V	0100010	-1.86V	1000010	-1.22V	1100010	-0.58V
0000011	-2.48V	0100011	-1.84V	1000011	-1.10V	1100011	-0.56V
0000100	-2.46V	0100100	-1.82V	1000100	-1.18V	1100100	-0.54V
0000101	-2.44V	0100101	-1.80V	1000101	-1.16V	1100101	-0.52V
0000110	-2.42V	0100110	-1.78V	1000110	-1.14V	1100110	-0.50V
0000111	-2.40V	0100111	-1.76V	1000111	-1.12V	1100111	-0.48V
0001000	-2.38V	0101000	-1.74V	1001000	-1.10V	1101000	-0.46V
0001001	-2.36V	0101001	-1.72V	1001001	-1.08V	1101001	-0.44V
0001010	-2.34V	0101010	-1.70V	1001010	-1.06V	1101010	-0.42V
0001011	-2.32V	0101011	-1.68V	1001011	-1.04V	1101011	-0.40V
0001100	-2.30V	0101100	-1.66V	1001100	-1.02V	1101100	-0.38V
0001101	-2.28V	0101101	-1.64V	1001101	-1.00V	1101101	-0.36V
0001110	-2.26V	0101110	-1.62V	1001110	-0.98V	1101110	-0.34V
0001111	-2.24V	0101111	-1.60V	1001111	-0.96V	1101111	-0.32V
0010000	-2.22V	0110000	-1.58V	1010000	-0.94V	1110000	-0.30V
0010001	-2.20V	0110001	-1.56V	1010001	-0.92V	1110001	-0.28V
0010010	-2.18V	0110010	-1.54V	1010010	-0.90V	1110010	-0.26V
0010011	-2.16V	0110011	-1.52V	1010011	-0.88V	1110011	-0.24V
0010100	-2.14V	0110100	-1.50V	1010100	-0.86V	1110100	-0.22V
0010101	-2.12V	0110101	-1.48V	1010101	-0.84V	1110101	-0.20V
0010110	-2.10V	0110110	-1.46V	1010110	-0.82V	1110110	-0.18V
0010111	-2.08V	0110111	-1.44V	1010111	-0.80V	1110111	-0.16V
0011000	-2.06V	0111000	-1.42V	1011000	-0.78V	1111000	-0.14V
0011001	-2.04V	0111001	-1.40V	1011001	-0.76V	1111001	-0.12V
0011010	-2.02V	0111010	-1.38V	1011010	-0.74V	1111010	-0.10V
0011011	-2.00V	0111011	-1.36V	1011011	-0.72V	1111011	-0.08V
0011100	-1.98V	0111100	-1.34V	1011100	-0.70V	1111100	-0.06V
0011101	-1.96V	0111101	-1.32V	1011101	-0.68V	1111101	-0.04V
0011110	-1.94V	0111110	-1.30V	1011110	-0.66V	1111110	-0.02V
0011111	-1.92V	0111111	-1.28V	1011111	-0.64V	1111111	-0.00V

Note. Available setting range of VCOM low level is from VCL+0.5V to 0V.

Status	Default Value
Initial	VCML[6:0] = 1100110 (-0.5V)

5.2.14.4. VCIR1[4:0]

VCI recycling clock cycle of VCOM driver is sustained for the number of clock cycles that is set in VCIR1[4:0].

Note. When VCI Recycling is used, VCOMH level must be larger than VCI level.

Table 106.VCIR1 setting

VCIR14-0	Recycling Period (number of display clock)	VCIR14-0	Recycling Period (number of display clock)
00000	0	10000	64
00001	4	10001	68
00010	8	10010	72
00011	12	10011	76
00100	16	10100	80
00101	20	10101	84
00110	24	10110	88
00111	28	10111	92
01000	32	11000	96
01001	36	11001	100
01010	40	11010	104
01011	44	11011	108
01100	48	11100	112
01101	52	11101	116
01110	56	11110	120
01111	60	11111	124

Status	Default Value
Initial	VCIR1[4:0] = 10010 (72)

5.2.14.5. NVC_BLK/PIVC_BLK

: This register controls VCOM state in porch period.

Table 107.NVC_BLK/PIVC_BLK

VC_BLK	Operation
00	VCOM is GND in porch period.
01	VCOM is GND in porch period.
10	VCOM holds end line polarity in porch period.
11	VCOM is continuously toggled in porch period.

Status	Default Value
Initial	PIVC_BLK[1:0]=00, NVC_BLK[1:0] = 11

5.2.14.6. NVC_ND/PIVC_ND

: This register controls VCOM state in nod-display period.

Table 108.NVC_ND/PIVC_ND

VC_ND	Operation
0	VCOM is the opposite polarity with Source.
1	VCOM is the same polarity with Source.

Status	Default Value
Initial	PIVC_ND =1, NVC_ND = 1

5.2.15. SRCCTL (F6H)

F6h	SRCCTL (Source Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	1	0	F6
1st Parameter	1	1	↑	SVCIR_SEL	-	-	-	-	SVCIR[2]	SVCIR[1]	SVCIR[0]	-
2nd Parameter	1	1	↑	-	-	-	-	-	-	-	SG	-
3rd Parameter	1	1	↑	-	-	-	-	-	SAP[2]	SAP[1]	SAP[0]	-
4th Parameter	1	1	↑	-	-	-	-	-	-	-	-	-
5th Parameter	1	1	↑	-	-	-	-	NSDT[3]	NSDT[2]	NSDT[1]	NSDT[0]	-
6th Parameter	1	1	↑	-	-	-	-	NSR_BLK[1]	NSR_BLK[0]	-	NSR_ND	-
7th Parameter	1	1	↑	-	-	-	-	PISDT[3]	PISDT[2]	PISDT[1]	PISDT[0]	-
8th Parameter	1	1	↑	-	-	-	-	PISR_BLK[1]	PISR_BLK[0]	-	PISR_ND	-
9th Parameter	1	1	↑	-	-	-	-	-	HBLK_SRC[2]	HBLK_SRC[1]	HBLK_SRC[0]	-

5.2.15.1. SVCIR_SEL

: This controls the period of source Output Enable.

SVCIR_SEL	Source Output Enable
0	When SVCIR=000,, Source Output Enable Fix High.
1	When SVCIR=000, Source Output Enable Output Enable On (After HBLK_SRC+15*DIV_SRC)

Status	Default Value
Initial	SVCIR_SEL=0

5.2.15.2. SVCIR[2 :0]

: This controls the period of source VCI recycling

Table 109.SVCIR[2:0]

SVCIR	Source VCI Recycling Period
000	Select SVCIR_SEL
001	VCI Recycling On (HBLK_SRC+15*DIV_SRC)
010	VCI Recycling On (HBLK_SRC+16*DIV_SRC)
011	VCI Recycling On (HBLK_SRC+17*DIV_SRC)
100	VCI Recycling On (HBLK_SRC+18*DIV_SRC)
101	VCI Recycling On (HBLK_SRC+19*DIV_SRC)
110	VCI Recycling On (HBLK_SRC+20*DIV_SRC)
111	VCI Recycling On (HBLK_SRC+21*DIV_SRC)

Status	Default Value
Initial	SVCIR[2:0] = 001

5.2.15.3. HBLK_SRC [2:0]

: This controls the high pulse width of internal track0 signal.

Table 110.HB LK_SRC[2:0]

HBLK_SRC[2:0]	Track0 Width Period(number of display clock)
000 ~ 010	Set disable
011	3 * DIV_SRC
100	4 * DIV_SRC
101	5 * DIV_SRC
110	6 * DIV_SRC
111	7 * DIV_SRC

Status	Default Value
Initial	HBLK_SRC [2:0] = 011

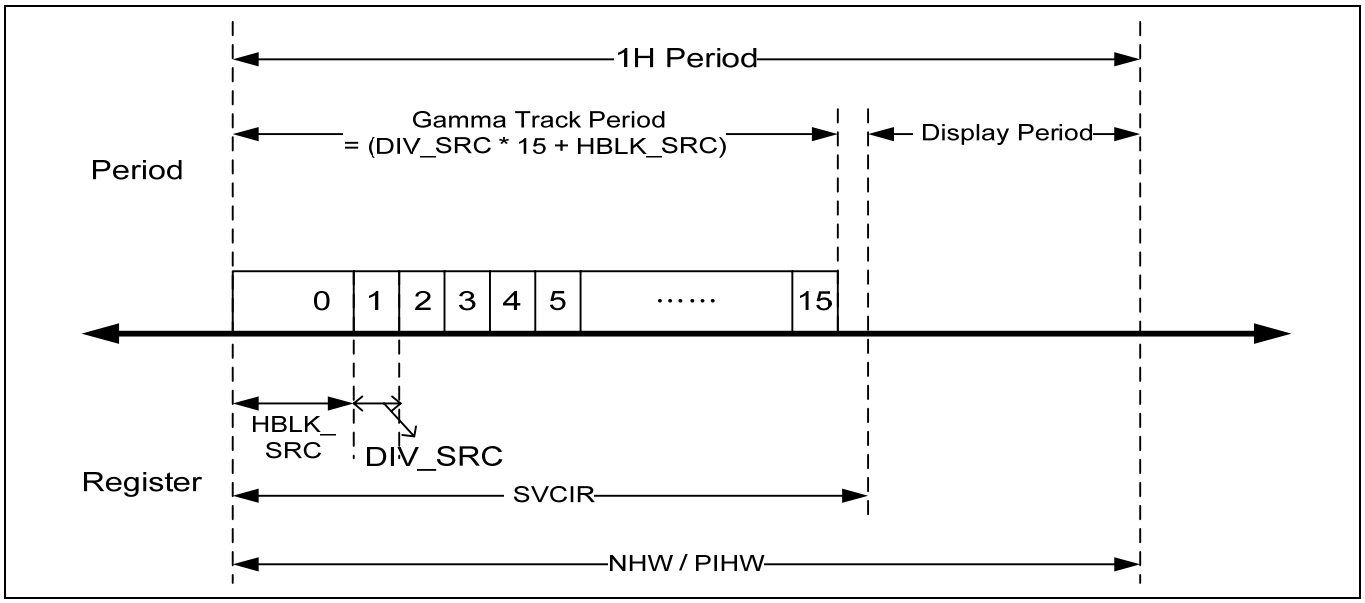


Figure115. 1H Period Timing control

5.2.15.4. NSR_BLK/PISR_BLK

: This register controls source state in porch period.

Table 111.NSR_BLK/PISR_BLK

SR_BLK	Operation
00	Source is hi-z in porch period.
01	Source is GND in porch period.
10	Source is binary driving mode in porch period.
11	Source is amplifier driving mode in porch period.

Status	Default Value
Initial	PISR_BLK[1:0]=10, NSR_BLK[1:0] = 11

5.2.15.5. NSR_ND/PISR_ND

: This register controls source state in nod-display period.

Table 112.NSR_ND/PISR_ND

SR_ND	Operation
0	Source is binary driving mode in non-display period.
1	Source is amplifier driving mode in non-display period.

Status	Default Value
Initial	PISR_ND =0, NSR_ND = 0

5.2.15.6. SG

: This controls the gamma symmetric axis.

SG = 0 : The adjustment register is to adjust X-axis symmetric of the grayscale voltage.

SG = 1 : The adjustment register is to adjust Y-axis symmetric of the grayscale voltage.

Status	Default Value
Initial	SG = 1

5.2.15.7. SAP[2:0]

: Adjust the slew-rate of the operational amplifier for the source driver. If higher SAP2-0 is set, LCD panel having higher resolution or higher frame frequency can be driven because the slew-rate of the operational amplifier is increased. But these bits must be set as adequate value because the amount of fixed current of the operational amplifier is also adjusted. During non-display, when SAP2-0 =”000,” operational amplifiers are turned off, so current consumption can be reduced.

Table 113.SAP[2:0]

SAP2	SAP1	SAP0	Source Amp. Current Level	Slew rate of Operational amplifier
0	0	0	Amp. Stop	
0	0	1	Setting Disable	
0	1	0	Setting Disable	
0	1	1	Slow	
1	0	0	Medium Slow 1	
1	0	1	Medium Slow 2	
1	1	0	Medium Slow 3	
1	1	1	Medium Slow 4	

Status	Default Value
Initial	SAP[2:0]= 011

5.2.15.8. PISDT[3:0] / NSDT[3:0]

: This register is used to set delay amount from gate falling(end) to source output. PISDT is applied in Idle Partial mode.

Table 114.PISDT[3:0] / NSDT[3:0]

NSDT3/ PISDT3	NSDT2/ PISDT2	NSDT1/ PISDT1	NSDT0/ PISDT0	Delay amount of the source output		
				Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)	
					18-bit RGB	6-bit RGB
0	0	0	0	Setting Disable	Setting Disable	Setting Disable
0	0	0	1	1 INCLK	2 DOTCLK	2 * 3 DOTCLK
0	0	1	0	2 INCLK	4 DOTCLK	4 * 3 DOTCLK
0	0	1	1	3 INCLK	6 DOTCLK	6 * 3 DOTCLK
0	1	0	0	4 INCLK	8 DOTCLK	8 * 3 DOTCLK
0	1	0	1	5 INCLK	10 DOTCLK	10 * 3 DOTCLK
0	1	1	0	6 INCLK	12 DOTCLK	12 * 3 DOTCLK
0	1	1	1	7 INCLK	14 DOTCLK	14 * 3 DOTCLK
1	0	0	0	8 INCLK	16 DOTCLK	16 * 3 DOTCLK
1	0	0	1	9 INCLK	18 DOTCLK	18 * 3 DOTCLK
1	0	1	0	10 INCLK	20 DOTCLK	20 * 3 DOTCLK
1	0	1	1	11 INCLK	22 DOTCLK	22 * 3 DOTCLK
1	1	0	0	12 INCLK	24 DOTCLK	24 * 3 DOTCLK
1	1	0	1	13 INCLK	26 DOTCLK	26 * 3 DOTCLK
1	1	1	0	14 INCLK	28 DOTCLK	28 * 3 DOTCLK
1	1	1	1	15 INCLK	30 DOTCLK	30 * 3 DOTCLK

Status	Default Value
Initial	PISDT[3:0], NSDT[3:0] = 0010

*note : INCLK is about 3Mhz.

When 18-bit RGB I/F, DOTCLK is about 5~6Mhz.

When 6-bit RGB I/F, DOTCLK is about 15~18Mhz .

5.2.16. IFCTL (F7H)

F7h	IFCTL (Interface Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	1	1	F7
1st Parameter	1	1	↑	MY_EOR	MX_EOR	MV_EOR	-	BGR_EOR	-	GS	SS	-
2nd Parameter	1	1	↑	-	IPM[1]	IPM[0]	MDT[1]	MDT[0]	-	DM[1]	DM[0]	-
3rd Parameter	1	1	↑	VPL	HPL	DPL	EPL	ENDIAN	-	-	RIM	-
4th Parameter	1	1	↑	RAM_ACCS	-	-	SPR_SEL	-	-	-	-	-

5.2.16.1. MY_EOR / MX_EOR / MV_EOR / BGR_EOR

: Each of these register will be used inside the IC. The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

Status	Default Value
Initial	MY_EOR, MX_EOR, MV_EOR, BGR_EOR = 0

5.2.16.2. GS

: Set the order of Gate Clock generation. When GS = 0, the order of GATE_ON is from G1 to G320, and then GS = 1, from G320 to G1.

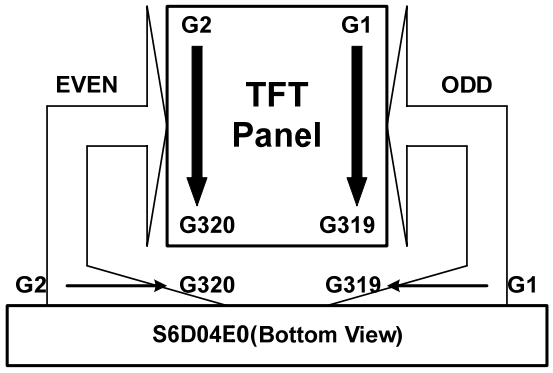
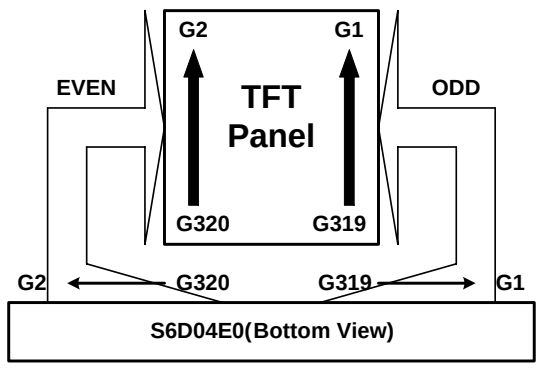
GS = 0	GS = 1
	
G1 -> G2 -> G3 -> ... -> G318 -> G319 -> G320	G320 -> G319 -> G318 -> ... -> G3 -> G2 -> G1

Figure116. Gate Clock order selection

Status	Default Value
Initial	GS = 0

5.2.16.3. SS

: Set the order of Shift Register. When SS = 0, the order of Shift Register is from S1 to S720, and then SS = 1, from S720 to S1.

This command is available when MIE_ON or RAM_ACCS=0 in RGB mode .

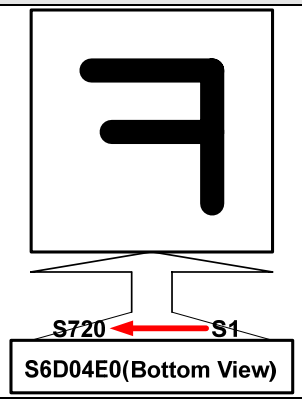
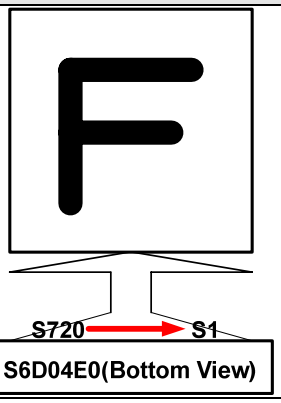
SS = 0	SS = 1
	
S1 -> S2 -> S3 -> ... -> S718 -> S719 -> S720	S720 -> S719 -> S718 -> ... -> S3 -> S2 -> S1

Figure117. Shift Register order selection

Status	Default Value
Initial	SS = 0

5.2.16.4. IPM[2:0]

Controls what value the lowest 1 bits (565→666) are set to in the 65k color mode.

Table 115. IPM[1:0]

IPM1	IPM0	Value of the Lowest 1 Bits in the 65k Color MODE
0	0	Normal 65k color mode operation
0	1	Copy the highest 1-bit
1	0	0
1	1	1

Status	Default Value
Initial	IPM[1:0] = 00

5.2.16.5. MDT[1:0]

: refer to the 3.3 Display Data Format section.

Status	Default Value
Initial	MDT[1:0] = 00

5.2.16.6. DM[1:0]

: Specify the display operation mode. The interface can be set based on the bits of DM. This setting enables switching interface between internal operation and the external display interface.

Table 116.DM[1:0]

DM1	DM0	Display Operation Mode
0	0	CPU interface mode
0	1	RGB interface mode
1	0	VSYNC interface mode
1	1	Setting disabled

Status	Default Value
Initial	DM = 00

5.2.16.7. ENDIAN

: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

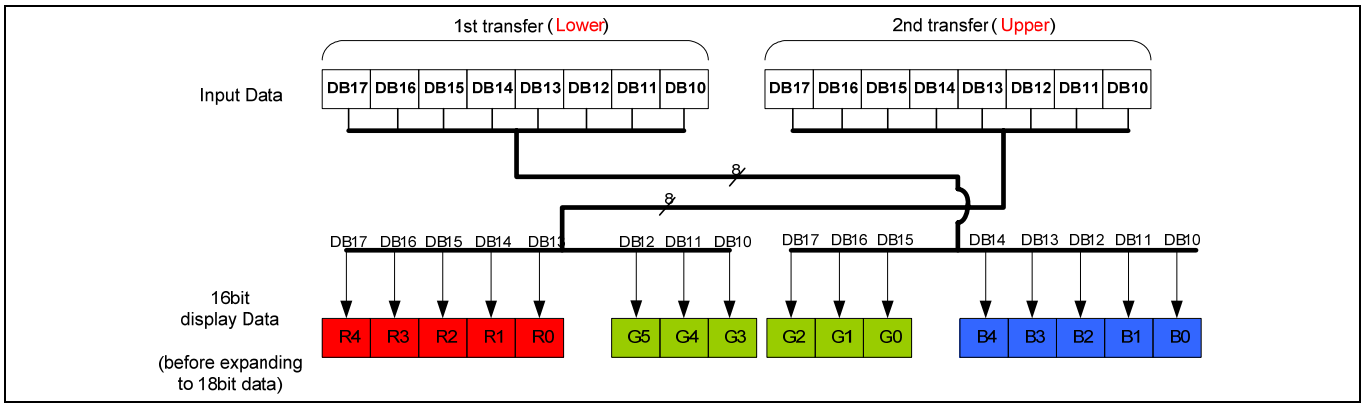


Figure118. Little endian (65K 8bit I/F type II)

Table 117.ENDIAN

ENDIAN	Data transfer mode
0	Normal (MSB first)
1	Little Endian (LSB first)

Note. Little Endian is valid on only 65K 8bit, 9bit I/F mode.

Status	Default Value
Initial	ENDIAN = 0

5.2.16.8. VPL

: Reverse the polarity of the VSYNC signal.

Table 118. VPL

VPL	Operation
0	VSYNC is low active
1	VSYNC is high active

Status	Default Value
Initial	VPL = 0

5.2.16.9. HPL

: Reverse the polarity of the HSYNC signal.

Table 119. HPL

HPL	Operation
0	HSYNC is low active
1	HSYNC is high active

Status	Default Value
Initial	HPL = 0

5.2.16.10. DPL

: Reverse the polarity of the DOTCLK signal.

Table 120. DPL

DPL	Operation
0	Display data is fetched at DOTCLK's rising edge
1	Display data is fetched at DOTCLK's falling edge

Status	Default Value
Initial	DPL = 0

5.2.16.11. EPL

: Set the polarity of ENABLE pad while using RGB interface.

Table 121.Relationship between EPL, ENABLE and RAM Access

EPL	ENABLE	RAM write	RAM address
0	0	Valid	Updated
0	1	Invalid	Held
1	0	Invalid	Held
1	1	Valid	Update

Status	Default Value
Initial	EPL = 1

5.2.16.12. RIM

: Specify the RGB interface mode when the RGB interface is used. Specifically, this setting specifies the mode when the bit of DM is set to RGB interface. These bits should be set before display operation through the RGB interface and should not be set during operation.

Table 122.RIM

RIM	RGB Interface Mode
0	18-bit RGB interface (one transfer/pixel)
1	6-bit RGB interface (three transfer /pixel)

Status	Default Value
Initial	RIM = 0

You should notice that some display functions, which will be described later, cannot be used according to the display mode shown below.

Table 123. Display functions and display modes

Function	RGB interface	Internal Clock Operation Mode
Partial Display	Cannot be used	Can be used
Scroll Function	Cannot be used	Can be used
Rotation	Cannot be used	Can be used
Mirroring	Cannot be used	Can be used
Window Function	Cannot be used	Can be used

Depending on the external display interface setting, various interfaces can be specified to match the display state. While displaying motion pictures (RGB interface), the data for display can be written in high-speed write mode, which achieves both low power consumption and high-speed access.

5.2.16.13. RAM_ACCS

: Select display data path whether Memory or Shift register when RGB Interface .

Table 124.RAM_ACCS

RAM_ACCS	Display Data Path
0	Shift Register
1	Memory

Status	Default Value
Initial	RAM_ACCS = 0

5.2.16.14. SPR_SEL

: Select the usage of Short Pulse Rejection (SPR) circuit to Logic input signals.

Table 125.SPR_SEL

SPR_SEL	Description
0	Apply SPR circuit
1	Do not apply SPR circuit

Status	Default Value
Initial	SPR_SEL = 0

5.2.17. PANELCTL (F8H)

F8h	PANELCTL (Panel Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	0	0	F8
1st Parameter	1	1	↑	PINO[3]	PINO[2]	PINO[1]	PINO[0]	NNO[3]	NNO[2]	NNO[1]	NNO[0]	-
2nd Parameter	1	1	↑	-	-	SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]	SCN[0]	-
3rd Parameter	1	1	↑	-	-	-	-	-	-	-	-	-

5.2.17.1. PINO[3:0] / NNO[3:0]

: Set amount of non-overlap for the gate output. PINO is applied in Idle Partial mode.

Table 126.PINO[3:0] / NNO[3:0]

PINO3 / NNO3	PINO2 / NNO2	PINO1 / NNO1	PINO0 /NNO0	Amount of non-overlap		
				Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)	
					18-bit RGB	6-bit RGB
0	0	0	0	Setting disable	Setting disable	Setting disable
0	0	0	1	3 INCLK	6 DOTCLK	6 *3 DOTCLK
0	0	1	0	6 INCLK	12 DOTCLK	12 *3 DOTCLK
0	0	1	1	9 INCLK	18 DOTCLK	18 *3 DOTCLK
0	1	0	0	12 INCLK	24 DOTCLK	24 *3 DOTCLK
0	1	0	1	15 INCLK	30 DOTCLK	30 *3 DOTCLK
0	1	1	0	18 INCLK	36 DOTCLK	36 *3 DOTCLK
0	1	1	1	21 INCLK	42 DOTCLK	42 *3 DOTCLK
1	0	0	0	24 INCLK	48 DOTCLK	48 *3 DOTCLK
1	0	0	1	27 INCLK	54 DOTCLK	54 *3 DOTCLK
1	0	1	0	30 INCLK	60 DOTCLK	60 *3 DOTCLK
1	0	1	1	33 INCLK	66 DOTCLK	66 *3 DOTCLK
1	1	0	0	36 INCLK	72 DOTCLK	72 *3 DOTCLK
1	1	0	1	39 INCLK	78 DOTCLK	78 *3 DOTCLK
1	1	1	0	42 INCLK	84 DOTCLK	84 *3 DOTCLK
1	1	1	1	45 INCLK	90 DOTCLK	90 *3 DOTCLK

Note: The amount of non-overlap time is defined from starting time of 1H.

Status	Default Value
Initial	IPON[3:0], NNO[3:0] = 0011

5.2.17.2. SCN[5:0]

: Set the gate output start position.

Table 127.SCN[5:0]

SCN[5:0]	Gate Start position	
	GS = 0	GS = 1
000000	G1	G320
000001	G9	G312
000010	G17	G304
….	....	….
100110	G305	G16
100111	G313	G8
101000~111111	Setting disabled	Setting disabled

Status	Default Value
Initial	SCN[5:0] = 000000

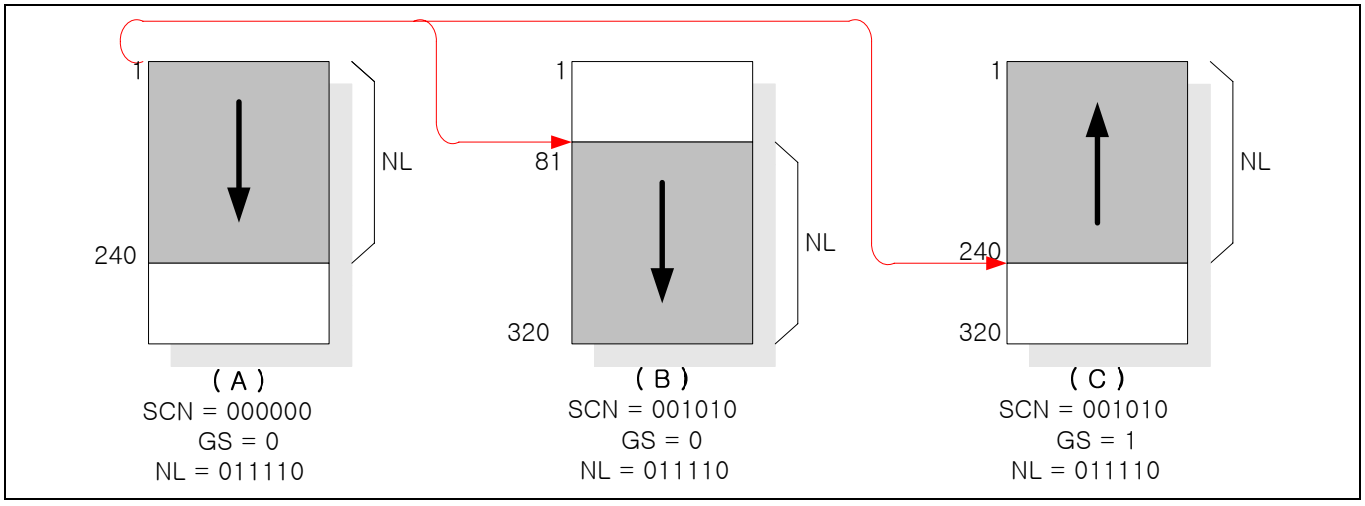


Figure119. SCN

5.2.18. GAMMASEL (F9H)

F9h	GAMMASEL(Gamma Selection)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	0	1	F9
Parameter	1	1	↑	-	-	-	NGF	-	R	G	B	-

5.2.18.1. NGF

: Set the negative polarity gamma register to positive polarity gamma register or user setting value. Refer to the section 4.2

NGF = 0 : negative polarity gamma is applied by the negative polarity gamma register.

NGF = 1 : negative polarity gamma is applied by the same data as positive polarity gamma register.

5.2.18.2. R,G,B

: These register selects the RBG seperate gamma register. Refer to the section 4.2

Table 128.R,G,B

R	G	B	Selected gamma preset register
1	0	0	Red gamma preset register is selected.
0	1	0	Green gamma preset register is selected.
0	0	1	Blue gamma preset register is selected.
others			Setting disable

Status	Default Value
Initial	NGF = 0, R = 1, G =0, B = 0

5.2.19. PGAMMACTL (FAH)

FAh	PGAMMACTL (Positive Gamma Control Register)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	0	FA
1st Parameter	1	1	↑	-	-	RFP[5]	RFP[4]	RFP[3]	RFP[2]	RFP[1]	RFP[0]	--
2nd Parameter	1	1	↑	-	-	OSP[5]	OSP[4]	OSP[3]	OSP[2]	OSP[1]	OSP[0]	--
3rd Parameter	1	1	↑	-	-	PKP0[5]	PKP0[4]	PKP0[3]	PKP0[2]	PKP0[1]	PKP[0]	--
4th Parameter	1	1	↑	-	-	PKP1[5]	PKP1[4]	PKP1[3]	PKP1[2]	PKP1[1]	PKP1[0]	--
5th Parameter	1	1	↑	-	-	PKP2[5]	PKP2[4]	PKP2[3]	PKP2[2]	PKP2[1]	PKP2[0]	--
6th Parameter	1	1	↑	-	-	PKP3[5]	PKP3[4]	PKP3[3]	PKP3[2]	PKP3[1]	PKP3[0]	--
7th Parameter	1	1	↑	-	-	PKP4[5]	PKP4[4]	PKP4[3]	PKP4[2]	PKP4[1]	PKP4[0]	--
8th Parameter	1	1	↑	-	-	PKP5[5]	PKP5[4]	PKP5[3]	PKP5[2]	PKP5[1]	PKP5[0]	--
9th Parameter	1	1	↑	-	-	PKP6[5]	PKP6[4]	PKP6[3]	PKP6[2]	PKP6[1]	PKP6[0]	--
10th Parameter	1	1	↑	-	-	PKP7[5]	PKP7[4]	PKP7[3]	PKP7[2]	PKP7[1]	PKP7[0]	--
11th Parameter	1	1	↑	-	-	PKP8[5]	PKP8[4]	PKP8[3]	PKP8[2]	PKP8[1]	PKP8[0]	--
12th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
13th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
14th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
15th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
16th Parameter	1	1	↑	-	-	-	-	-	-	GLP[1]	GLP[0]	--

This command is used to set the gamma preset register for positive.

GLP[1:0] : The positive voltage of grayscale number from V1 or V62 is mainly adjusted.

RFP[5:0] : The positive voltage of grayscale number from V0 is mainly adjusted.

OSP[5:0] : The positive voltage of grayscale number from V63 is mainly adjusted.

PKP0[5:0] ~ PKP10[5:0] : The positive voltage of grayscale number from V1 to V62 is finely adjusted.

Table 129.Gamma preset for positive

Status	Default Value
Initial	RFP[5:0],OSP[5:0],PKP0[5:0]~PKP8[5:0],GLP[1:0] 00h, 0Ch, 01h, 0Dh, 13h, 1Ch, 15h, 3Ah, 26h, 1Bh, 0Eh, 00h

5.2.20. NGAMMACTL (FBH)

FBh	NGAMMACTL (Negative Gamma Control Register)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	0	FB
1st Parameter	1	1	↑	-	-	RFN[5]	RFN[4]	RFN[3]	RFN[2]	RFN[1]	RFN[0]	--
2nd Parameter	1	1	↑	-	-	OSN[5]	OSN[4]	OSN[3]	OSN[2]	OSN[1]	OSN[0]	--
3rd Parameter	1	1	↑	-	-	PKN0[5]	PKN0[4]	PKN0[3]	PKN0[2]	PKN0[1]	PKN[0]	--
4th Parameter	1	1	↑	-	-	PKN1[5]	PKN1[4]	PKN1[3]	PKN1[2]	PKN1[1]	PKN1[0]	--
5th Parameter	1	1	↑	-	-	PKN2[5]	PKN2[4]	PKN2[3]	PKN2[2]	PKN2[1]	PKN2[0]	--
6th Parameter	1	1	↑	-	-	PKN3[5]	PKN3[4]	PKN3[3]	PKN3[2]	PKN3[1]	PKN3[0]	--
7th Parameter	1	1	↑	-	-	PKN4[5]	PKN4[4]	PKN4[3]	PKN4[2]	PKN4[1]	PKN4[0]	--
8th Parameter	1	1	↑	-	-	PKN5[5]	PKN5[4]	PKN5[3]	PKN5[2]	PKN5[1]	PKN5[0]	--
9th Parameter	1	1	↑	-	-	PKN6[5]	PKN6[4]	PKN6[3]	PKN6[2]	PKN6[1]	PKN6[0]	--
10th Parameter	1	1	↑	-	-	PKN7[5]	PKN7[4]	PKN7[3]	PKN7[2]	PKN7[1]	PKN7[0]	--
11th Parameter	1	1	↑	-	-	PKN8[5]	PKN8[4]	PKN8[3]	PKN8[2]	PKN8[1]	PKN8[0]	--
12th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
13th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
14th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
15th Parameter	1	1	↑	-	-	-	-	-	-	-	-	--
16th Parameter	1	1	↑	-	-	-	-	-	-	GLN[1]	GLN[0]	--

This command is used to set the gamma preset register for negative.

GLN[1:0] : The negative voltage of grayscale number from V1 or V62 is mainly adjusted.

RFN[5:0] : The negative voltage of grayscale number from V0 is mainly adjusted.

OSN[5:0] : The negative voltage of grayscale number from V63 is mainly adjusted.

PKN0[5:0] ~ PKN10[5:0] : The negative voltage of grayscale number from V1 to V62 is finely adjusted.

Table 130.Gamma preset for negative

Status	Default Value
Initial	RFN[5:0],OSN[5:0],PKN0[5:0]~PKN8[5:0],GLN[1:0] 00h, 0Ch, 01h, 0Dh, 13h, 1Ch, 15h, 3Ah, 26h, 1Bh, 0Eh, 00h

CHAPTER 6

APPENDIX

6. APPENDIX

6.1. APPLICATION CIRCUIT

A typical application circuit is shown in following figure. All black-colored capacitors are 1uF capacitors.

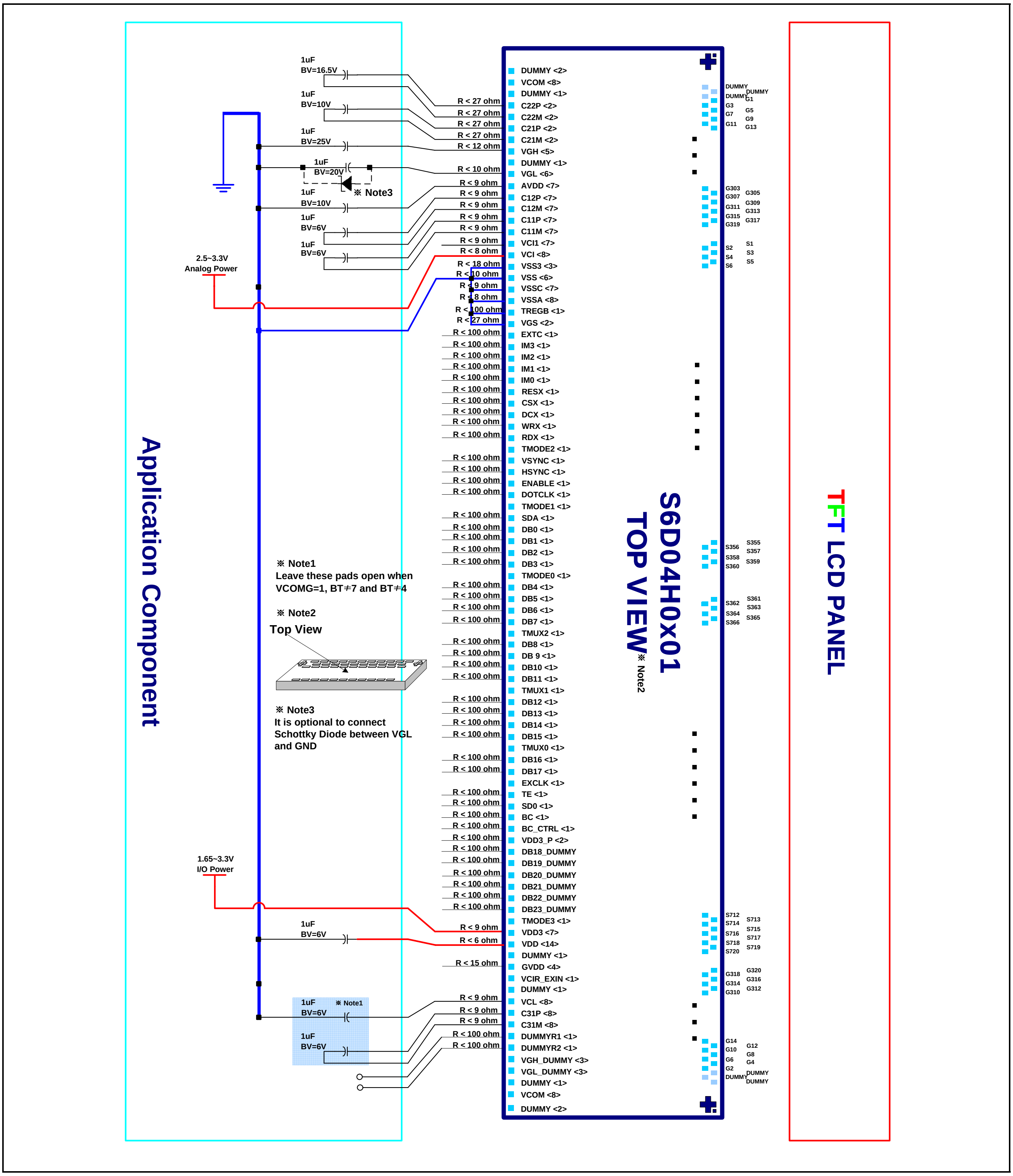


Figure120. Application circuit.

6.2. EXTERNAL COMPONENTS

Table 131. External Components

Name	Device	Value	Connection	Note	
C1	Capacitor	1uF	AVDD – GND	Maximum Ratings Voltage	10V
C2	Capacitor	1uF	VGH – GND		25V
C3	Capacitor	1uF	VGL – GND		20V
C4	Capacitor	1uF	C11P – C11M		6V
C5	Capacitor	1uF	C12P – C12M		6V
C6	Capacitor	1uF	C21P – C21M		10V
C7	Capacitor	1uF	C22P – C22M		16.5V
C8	Capacitor	1uF	C31P – C31M		6V
C9	Capacitor	1uF	VCL-GND		6V
C10	Capacitor	1uF	RVDD – GND		6V
D1*note	Diode	-	(+)VGL – GND(-)	VF < 0.4V (@ IF = 20mA, Ta = 25℃) VR ≥ max.25V (Option) *Recommanded diode RB521	

Note1: It is optional to connect S/D between VGL and GND

Note2: Maximum Ratings Voltage should not be exceed 25volt.

6.3. PAD CENTER COORDINATES

6.3.1. INPUT PAD

Table 132. Pad Center Coordinates [Unit: μm]

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
I - 1	DUMMY	-7292.5	-285	I - 51	C12M	-4292.5	-285	I - 101	VSSA	-1292.5	-285
I - 2	DUMMY	-7232.5	-285	I - 52	C12M	-4232.5	-285	I - 102	VSSA	-1232.5	-285
I - 3	VCOM	-7172.5	-285	I - 53	C11P	-4172.5	-285	I - 103	VSSA	-1172.5	-285
I - 4	VCOM	-7112.5	-285	I - 54	C11P	-4112.5	-285	I - 104	VSSA	-1112.5	-285
I - 5	VCOM	-7052.5	-285	I - 55	C11P	-4052.5	-285	I - 105	VSSA	-1052.5	-285
I - 6	VCOM	-6992.5	-285	I - 56	C11P	-3992.5	-285	I - 106	TREGB	-992.5	-285
I - 7	VCOM	-6932.5	-285	I - 57	C11P	-3932.5	-285	I - 107	VGS	-932.5	-285
I - 8	VCOM	-6872.5	-285	I - 58	C11P	-3872.5	-285	I - 108	VGS	-872.5	-285
I - 9	VCOM	-6812.5	-285	I - 59	C11P	-3812.5	-285	I - 109	EXTC	-812.5	-285
I - 10	VCOM	-6752.5	-285	I - 60	C11M	-3752.5	-285	I - 110	IM<3>	-752.5	-285
I - 11	DUMMY	-6692.5	-285	I - 61	C11M	-3692.5	-285	I - 111	IM<2>	-692.5	-285
I - 12	C22P	-6632.5	-285	I - 62	C11M	-3632.5	-285	I - 112	IM<1>	-632.5	-285
I - 13	C22P	-6572.5	-285	I - 63	C11M	-3572.5	-285	I - 113	IM<0>	-572.5	-285
I - 14	C22M	-6512.5	-285	I - 64	C11M	-3512.5	-285	I - 114	RESX	-512.5	-285
I - 15	C22M	-6452.5	-285	I - 65	C11M	-3452.5	-285	I - 115	CSX	-452.5	-285
I - 16	C21P	-6392.5	-285	I - 66	C11M	-3392.5	-285	I - 116	DCX	-392.5	-285
I - 17	C21P	-6332.5	-285	I - 67	VCI1	-3332.5	-285	I - 117	WRX	-332.5	-285
I - 18	C21M	-6272.5	-285	I - 68	VCI1	-3272.5	-285	I - 118	RDX	-272.5	-285
I - 19	C21M	-6212.5	-285	I - 69	VCI1	-3212.5	-285	I - 119	TMODE<2>	-212.5	-285
I - 20	VGH	-6152.5	-285	I - 70	VCI1	-3152.5	-285	I - 120	VSYNC	-152.5	-285
I - 21	VGH	-6092.5	-285	I - 71	VCI1	-3092.5	-285	I - 121	HSYNC	-92.5	-285
I - 22	VGH	-6032.5	-285	I - 72	VCI1	-3032.5	-285	I - 122	ENABLE	-32.5	-285
I - 23	VGH	-5972.5	-285	I - 73	VCI1	-2972.5	-285	I - 123	DOTCLK	27.5	-285
I - 24	VGH	-5912.5	-285	I - 74	VCI	-2912.5	-285	I - 124	TMODE<1>	87.5	-285
I - 25	DUMMY	-5852.5	-285	I - 75	VCI	-2852.5	-285	I - 125	SDA	160	-285
I - 26	VGL	-5792.5	-285	I - 76	VCI	-2792.5	-285	I - 126	DB<0>	245	-285
I - 27	VGL	-5732.5	-285	I - 77	VCI	-2732.5	-285	I - 127	DB<1>	330	-285
I - 28	VGL	-5672.5	-285	I - 78	VCI	-2672.5	-285	I - 128	DB<2>	415	-285
I - 29	VGL	-5612.5	-285	I - 79	VCI	-2612.5	-285	I - 129	DB<3>	500	-285
I - 30	VGL	-5552.5	-285	I - 80	VCI	-2552.5	-285	I - 130	TMODE<0>	572.5	-285
I - 31	VGL	-5492.5	-285	I - 81	VCI	-2492.5	-285	I - 131	DB<4>	645	-285
I - 32	AVDD	-5432.5	-285	I - 82	VSS3	-2432.5	-285	I - 132	DB<5>	730	-285
I - 33	AVDD	-5372.5	-285	I - 83	VSS3	-2372.5	-285	I - 133	DB<6>	815	-285
I - 34	AVDD	-5312.5	-285	I - 84	VSS3	-2312.5	-285	I - 134	DB<7>	900	-285
I - 35	AVDD	-5252.5	-285	I - 85	VSS	-2252.5	-285	I - 135	TMUX<2>	972.5	-285
I - 36	AVDD	-5192.5	-285	I - 86	VSS	-2192.5	-285	I - 136	DB<8>	1045	-285
I - 37	AVDD	-5132.5	-285	I - 87	VSS	-2132.5	-285	I - 137	DB<9>	1130	-285
I - 38	AVDD	-5072.5	-285	I - 88	VSS	-2072.5	-285	I - 138	DB<10>	1215	-285
I - 39	C12P	-5012.5	-285	I - 89	VSS	-2012.5	-285	I - 139	DB<11>	1300	-285
I - 40	C12P	-4952.5	-285	I - 90	VSS	-1952.5	-285	I - 140	TMUX<1>	1372.5	-285
I - 41	C12P	-4892.5	-285	I - 91	VSSC	-1892.5	-285	I - 141	DB<12>	1445	-285
I - 42	C12P	-4832.5	-285	I - 92	VSSC	-1832.5	-285	I - 142	DB<13>	1530	-285

No.	Pad Name	X	Y		No.	Pad Name	X	Y		No.	Pad Name	X	Y
I - 43	C12P	-4772.5	-285		I - 93	VSSC	-1772.5	-285		I - 143	DB<14>	1615	-285
I - 44	C12P	-4712.5	-285		I - 94	VSSC	-1712.5	-285		I - 144	DB<15>	1700	-285
I - 45	C12P	-4652.5	-285		I - 95	VSSC	-1652.5	-285		I - 145	TMUX<0>	1772.5	-285
I - 46	C12M	-4592.5	-285		I - 96	VSSC	-1592.5	-285		I - 146	DB<16>	1845	-285
I - 47	C12M	-4532.5	-285		I - 97	VSSC	-1532.5	-285		I - 147	DB<17>	1930	-285
I - 48	C12M	-4472.5	-285		I - 98	VSSA	-1472.5	-285		I - 148	EXCLK	2002.5	-285
I - 49	C12M	-4412.5	-285		I - 99	VSSA	-1412.5	-285		I - 149	TE	2075	-285
I - 50	C12M	-4352.5	-285		I - 100	VSSA	-1352.5	-285		I - 150	SD0	2160	-285

Table 133. Pad Center Coordinates [Unit: μm]

No.	Pad Name	X	Y		no.	Pad Name	X	Y
I - 151	BC	2245	-285		I - 201	C31P	5432.5	-285
I - 152	BC_CTRL	2330	-285		I - 202	C31P	5492.5	-285
I - 153	VDD3_P	2402.5	-285		I - 203	C31P	5552.5	-285
I - 154	VDD3_P	2462.5	-285		I - 204	C31P	5612.5	-285
I - 155	DB18_DUMMY	2535	-285		I - 205	C31P	5672.5	-285
I - 156	DB19_DUMMY	2620	-285		I - 206	C31M	5732.5	-285
I - 157	DB20_DUMMY	2705	-285		I - 207	C31M	5792.5	-285
I - 158	DB21_DUMMY	2790	-285		I - 208	C31M	5852.5	-285
I - 159	DB22_DUMMY	2875	-285		I - 209	C31M	5912.5	-285
I - 160	DB23_DUMMY	2960	-285		I - 210	C31M	5972.5	-285
I - 161	TMODE<3>	3032.5	-285		I - 211	C31M	6032.5	-285
I - 162	VDD3	3092.5	-285		I - 212	C31M	6092.5	-285
I - 163	VDD3	3152.5	-285		I - 213	C31M	6152.5	-285
I - 164	VDD3	3212.5	-285		I - 214	DUMMYR1	6212.5	-285
I - 165	VDD3	3272.5	-285		I - 215	DUMMYR2	6272.5	-285
I - 166	VDD3	3332.5	-285		I - 216	VGH_DUMMY	6332.5	-285
I - 167	VDD3	3392.5	-285		I - 217	VGH_DUMMY	6392.5	-285
I - 168	VDD3	3452.5	-285		I - 218	VGH_DUMMY	6452.5	-285
I - 169	VDD	3512.5	-285		I - 219	VGL_DUMMY	6512.5	-285
I - 170	VDD	3572.5	-285		I - 220	VGL_DUMMY	6572.5	-285
I - 171	VDD	3632.5	-285		I - 221	VGL_DUMMY	6632.5	-285
I - 172	VDD	3692.5	-285		I - 222	DUMMY	6692.5	-285
I - 173	VDD	3752.5	-285		I - 223	VCOM	6752.5	-285
I - 174	VDD	3812.5	-285		I - 224	VCOM	6812.5	-285
I - 175	VDD	3872.5	-285		I - 225	VCOM	6872.5	-285
I - 176	VDD	3932.5	-285		I - 226	VCOM	6932.5	-285
I - 177	VDD	3992.5	-285		I - 227	VCOM	6992.5	-285
I - 178	VDD	4052.5	-285		I - 228	VCOM	7052.5	-285
I - 179	VDD	4112.5	-285		I - 229	VCOM	7112.5	-285
I - 180	VDD	4172.5	-285		I - 230	VCOM	7172.5	-285
I - 181	VDD	4232.5	-285		I - 231	DUMMY	7232.5	-285
I - 182	VDD	4292.5	-285		I - 232	DUMMY	7292.5	-285
I - 183	DUMMY	4352.5	-285					
I -184	GVDD	4412.5	-285					
I - 185	GVDD	4472.5	-285					
I - 186	GVDD	4532.5	-285					

No.	Pad Name	X	Y		no.	Pad Name	X	Y
I - 187	GVDD	4592.5	-285					
I - 188	VCIR_EXIN	4652.5	-285					
I - 189	DUMMY	4712.5	-285					
I - 190	VCL	4772.5	-285					
I - 191	VCL	4832.5	-285					
I - 192	VCL	4892.5	-285					
I - 193	VCL	4952.5	-285					
I - 194	VCL	5012.5	-285					
I - 195	VCL	5072.5	-285					
I - 196	VCL	5132.5	-285					
I - 197	VCL	5192.5	-285					
I - 198	C31P	5252.5	-285					
I - 199	C31P	5312.5	-285					
I - 200	C31P	5372.5	-285					

6.3.2. OUTPUT PAD

Table 134. Pad Center Coordinates [Unit: μm]

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 1	DUMMY	7399	261	O - 51	G96	6699	261	O - 101	G196	5999	261
O - 2	DUMMY	7385	126	O - 52	G98	6685	126	O - 102	G198	5985	126
O - 3	DUMMY	7371	261	O - 53	G100	6671	261	O - 103	G200	5971	261
O - 4	G2	7357	126	O - 54	G102	6657	126	O - 104	G202	5957	126
O - 5	G4	7343	261	O - 55	G104	6643	261	O - 105	G204	5943	261
O - 6	G6	7329	126	O - 56	G106	6629	126	O - 106	G206	5929	126
O - 7	G8	7315	261	O - 57	G108	6615	261	O - 107	G208	5915	261
O - 8	G10	7301	126	O - 58	G110	6601	126	O - 108	G210	5901	126
O - 9	G12	7287	261	O - 59	G112	6587	261	O - 109	G212	5887	261
O - 10	G14	7273	126	O - 60	G114	6573	126	O - 110	G214	5873	126
O - 11	G16	7259	261	O - 61	G116	6559	261	O - 111	G216	5859	261
O - 12	G18	7245	126	O - 62	G118	6545	126	O - 112	G218	5845	126
O - 13	G20	7231	261	O - 63	G120	6531	261	O - 113	G220	5831	261
O - 14	G22	7217	126	O - 64	G122	6517	126	O - 114	G222	5817	126
O - 15	G24	7203	261	O - 65	G124	6503	261	O - 115	G224	5803	261
O - 16	G26	7189	126	O - 66	G126	6489	126	O - 116	G226	5789	126
O - 17	G28	7175	261	O - 67	G128	6475	261	O - 117	G228	5775	261
O - 18	G30	7161	126	O - 68	G130	6461	126	O - 118	G230	5761	126
O - 19	G32	7147	261	O - 69	G132	6447	261	O - 119	G232	5747	261
O - 20	G34	7133	126	O - 70	G134	6433	126	O - 120	G234	5733	126
O - 21	G36	7119	261	O - 71	G136	6419	261	O - 121	G236	5719	261
O - 22	G38	7105	126	O - 72	G138	6405	126	O - 122	G238	5705	126
O - 23	G40	7091	261	O - 73	G140	6391	261	O - 123	G240	5691	261
O - 24	G42	7077	126	O - 74	G142	6377	126	O - 124	G242	5677	126
O - 25	G44	7063	261	O - 75	G144	6363	261	O - 125	G244	5663	261
O - 26	G46	7049	126	O - 76	G146	6349	126	O - 126	G246	5649	126
O - 27	G48	7035	261	O - 77	G148	6335	261	O - 127	G248	5635	261
O - 28	G50	7021	126	O - 78	G150	6321	126	O - 128	G250	5621	126
O - 29	G52	7007	261	O - 79	G152	6307	261	O - 129	G252	5607	261
O - 30	G54	6993	126	O - 80	G154	6293	126	O - 130	G254	5593	126
O - 31	G56	6979	261	O - 81	G156	6279	261	O - 131	G256	5579	261
O - 32	G58	6965	126	O - 82	G158	6265	126	O - 132	G258	5565	126
O - 33	G60	6951	261	O - 83	G160	6251	261	O - 133	G260	5551	261
O - 34	G62	6937	126	O - 84	G162	6237	126	O - 134	G262	5537	126
O - 35	G64	6923	261	O - 85	G164	6223	261	O - 135	G264	5523	261
O - 36	G66	6909	126	O - 86	G166	6209	126	O - 136	G266	5509	126
O - 37	G68	6895	261	O - 87	G168	6195	261	O - 137	G268	5495	261
O - 38	G70	6881	126	O - 88	G170	6181	126	O - 138	G270	5481	126
O - 39	G72	6867	261	O - 89	G172	6167	261	O - 139	G272	5467	261
O - 40	G74	6853	126	O - 90	G174	6153	126	O - 140	G274	5453	126
O - 41	G76	6839	261	O - 91	G176	6139	261	O - 141	G276	5439	261
O - 42	G78	6825	126	O - 92	G178	6125	126	O - 142	G278	5425	126
O - 43	G80	6811	261	O - 93	G180	6111	261	O - 143	G280	5411	261
O - 44	G82	6797	126	O - 94	G182	6097	126	O - 144	G282	5397	126
O - 45	G84	6783	261	O - 95	G184	6083	261	O - 145	G284	5383	261
O - 46	G86	6769	126	O - 96	G186	6069	126	O - 146	G286	5369	126

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 47	G88	6755	261	O - 97	G188	6055	261	O - 147	G288	5355	261
O - 48	G90	6741	126	O - 98	G190	6041	126	O - 148	G290	5341	126
O - 49	G92	6727	261	O - 99	G192	6027	261	O - 149	G292	5327	261
O - 50	G94	6713	126	O - 100	G194	6013	126	O - 150	G294	5313	126

Table 135. Pad Center Coordinates [Unit: μm]

no.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 151	G296	5299	261	O - 201	S683	4557	261	O - 251	S633	3857	261
O - 152	G298	5285	126	O - 202	S682	4543	126	O - 252	S632	3843	126
O - 153	G300	5271	261	O - 203	S681	4529	261	O - 253	S631	3829	261
O - 154	G302	5257	126	O - 204	S680	4515	126	O - 254	S630	3815	126
O - 155	G304	5243	261	O - 205	S679	4501	261	O - 255	S629	3801	261
O - 156	G306	5229	126	O - 206	S678	4487	126	O - 256	S628	3787	126
O - 157	G308	5215	261	O - 207	S677	4473	261	O - 257	S627	3773	261
O - 158	G310	5201	126	O - 208	S676	4459	126	O - 258	S626	3759	126
O - 159	G312	5187	261	O - 209	S675	4445	261	O - 259	S625	3745	261
O - 160	G314	5173	126	O - 210	S674	4431	126	O - 260	S624	3731	126
O - 161	G316	5159	261	O - 211	S673	4417	261	O - 261	S623	3717	261
O - 162	G318	5145	126	O - 212	S672	4403	126	O - 262	S622	3703	126
O - 163	G320	5131	261	O - 213	S671	4389	261	O - 263	S621	3689	261
O - 164	S720	5075	126	O - 214	S670	4375	126	O - 264	S620	3675	126
O - 165	S719	5061	261	O - 215	S669	4361	261	O - 265	S619	3661	261
O - 166	S718	5047	126	O - 216	S668	4347	126	O - 266	S618	3647	126
O - 167	S717	5033	261	O - 217	S667	4333	261	O - 267	S617	3633	261
O - 168	S716	5019	126	O - 218	S666	4319	126	O - 268	S616	3619	126
O - 169	S715	5005	261	O - 219	S665	4305	261	O - 269	S615	3605	261
O - 170	S714	4991	126	O - 220	S664	4291	126	O - 270	S614	3591	126
O - 171	S713	4977	261	O - 221	S663	4277	261	O - 271	S613	3577	261
O - 172	S712	4963	126	O - 222	S662	4263	126	O - 272	S612	3563	126
O - 173	S711	4949	261	O - 223	S661	4249	261	O - 273	S611	3549	261
O - 174	S710	4935	126	O - 224	S660	4235	126	O - 274	S610	3535	126
O - 175	S709	4921	261	O - 225	S659	4221	261	O - 275	S609	3521	261
O - 176	S708	4907	126	O - 226	S658	4207	126	O - 276	S608	3507	126
O - 177	S707	4893	261	O - 227	S657	4193	261	O - 277	S607	3493	261
O - 178	S706	4879	126	O - 228	S656	4179	126	O - 278	S606	3479	126
O - 179	S705	4865	261	O - 229	S655	4165	261	O - 279	S605	3465	261
O - 180	S704	4851	126	O - 230	S654	4151	126	O - 270	S604	3451	126
O - 181	S703	4837	261	O - 231	S653	4137	261	O - 281	S603	3437	261
O - 182	S702	4823	126	O - 232	S652	4123	126	O - 282	S602	3423	126
O - 183	S701	4809	261	O - 233	S651	4109	261	O - 283	S601	3409	261
O - 184	S700	4795	126	O - 234	S650	4095	126	O - 284	S600	3395	126
O - 185	S699	4781	261	O - 235	S649	4081	261	O - 285	S599	3381	261
O - 186	S698	4767	126	O - 236	S648	4067	126	O - 286	S598	3367	126
O - 187	S697	4753	261	O - 237	S647	4053	261	O - 287	S597	3353	261
O - 188	S696	4739	126	O - 238	S646	4039	126	O - 288	S596	3339	126
O - 189	S695	4725	261	O - 239	S645	4025	261	O - 289	S595	3325	261
O - 190	S694	4711	126	O - 240	S644	4011	126	O - 290	S594	3311	126
O - 191	S693	4697	261	O - 241	S643	3997	261	O - 291	S593	3297	261

no.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 192	S692	4683	126	O - 242	S642	3983	126	O - 292	S592	3283	126
O - 193	S691	4669	261	O - 243	S641	3969	261	O - 293	S591	3269	261
O - 194	S690	4655	126	O - 244	S640	3955	126	O - 294	S590	3255	126
O - 195	S689	4641	261	O - 245	S639	3941	261	O - 295	S589	3241	261
O - 196	S688	4627	126	O - 246	S638	3927	126	O - 296	S588	3227	126
O - 197	S687	4613	261	O - 247	S637	3913	261	O - 297	S587	3213	261
O - 198	S686	4599	126	O - 248	S636	3899	126	O - 298	S586	3199	126
O - 199	S685	4585	261	O - 249	S635	3885	261	O - 299	S585	3185	261
O - 200	S684	4571	126	O - 250	S634	3871	126	O - 300	S584	3171	126

Table 136. Pad Center Coordinates [Unit: μm]

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 301	S583	3157	261	O - 351	S533	2457	261	O - 401	S483	1757	261
O - 302	S582	3143	126	O - 352	S532	2443	126	O - 402	S482	1743	126
O - 303	S581	3129	261	O - 353	S531	2429	261	O - 403	S481	1729	261
O - 304	S580	3115	126	O - 354	S530	2415	126	O - 404	S480	1715	126
O - 305	S579	3101	261	O - 355	S529	2401	261	O - 405	S479	1701	261
O - 306	S578	3087	126	O - 356	S528	2387	126	O - 406	S478	1687	126
O - 307	S577	3073	261	O - 357	S527	2373	261	O - 407	S477	1673	261
O - 308	S576	3059	126	O - 358	S526	2359	126	O - 408	S476	1659	126
O - 309	S575	3045	261	O - 359	S525	2345	261	O - 409	S475	1645	261
O - 310	S574	3031	126	O - 360	S524	2331	126	O - 410	S474	1631	126
O - 311	S573	3017	261	O - 361	S523	2317	261	O - 411	S473	1617	261
O - 312	S572	3003	126	O - 362	S522	2303	126	O - 412	S472	1603	126
O - 313	S571	2989	261	O - 363	S521	2289	261	O - 413	S471	1589	261
O - 314	S570	2975	126	O - 364	S520	2275	126	O - 414	S470	1575	126
O - 315	S569	2961	261	O - 365	S519	2261	261	O - 415	S469	1561	261
O - 316	S568	2947	126	O - 366	S518	2247	126	O - 416	S468	1547	126
O - 317	S567	2933	261	O - 367	S517	2233	261	O - 417	S467	1533	261
O - 318	S566	2919	126	O - 368	S516	2219	126	O - 418	S466	1519	126
O - 319	S565	2905	261	O - 369	S515	2205	261	O - 419	S465	1505	261
O - 320	S564	2891	126	O - 370	S514	2191	126	O - 420	S464	1491	126
O - 321	S563	2877	261	O - 371	S513	2177	261	O - 421	S463	1477	261
O - 322	S562	2863	126	O - 372	S512	2163	126	O - 422	S462	1463	126
O - 323	S561	2849	261	O - 373	S511	2149	261	O - 423	S461	1449	261
O - 324	S560	2835	126	O - 374	S510	2135	126	O - 424	S460	1435	126
O - 325	S559	2821	261	O - 375	S509	2121	261	O - 425	S459	1421	261
O - 326	S558	2807	126	O - 376	S508	2107	126	O - 426	S458	1407	126
O - 327	S557	2793	261	O - 377	S507	2093	261	O - 427	S457	1393	261
O - 328	S556	2779	126	O - 378	S506	2079	126	O - 428	S456	1379	126
O - 329	S555	2765	261	O - 379	S505	2065	261	O - 429	S455	1365	261
O - 330	S554	2751	126	O - 380	S504	2051	126	O - 430	S454	1351	126
O - 331	S553	2737	261	O - 381	S503	2037	261	O - 431	S453	1337	261
O - 332	S552	2723	126	O - 382	S502	2023	126	O - 432	S452	1323	126
O - 333	S551	2709	261	O - 383	S501	2009	261	O - 433	S451	1309	261
O - 334	S550	2695	126	O - 384	S500	1995	126	O - 434	S450	1295	126
O - 335	S549	2681	261	O - 385	S499	1981	261	O - 435	S449	1281	261
O - 336	S548	2667	126	O - 386	S498	1967	126	O - 436	S448	1267	126

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 337	S547	2653	261	O - 387	S497	1953	261	O - 437	S447	1253	261
O - 338	S546	2639	126	O - 388	S496	1939	126	O - 438	S446	1239	126
O - 339	S545	2625	261	O - 389	S495	1925	261	O - 439	S445	1225	261
O - 340	S544	2611	126	O - 390	S494	1911	126	O - 440	S444	1211	126
O - 341	S543	2597	261	O - 391	S493	1897	261	O - 441	S443	1197	261
O - 342	S542	2583	126	O - 392	S492	1883	126	O - 442	S442	1183	126
O - 343	S541	2569	261	O - 393	S491	1869	261	O - 443	S441	1169	261
O - 344	S540	2555	126	O - 394	S490	1855	126	O - 444	S440	1155	126
O - 345	S539	2541	261	O - 395	S489	1841	261	O - 445	S439	1141	261
O - 346	S538	2527	126	O - 396	S488	1827	126	O - 446	S438	1127	126
O - 347	S537	2513	261	O - 397	S487	1813	261	O - 447	S437	1113	261
O - 348	S536	2499	126	O - 398	S486	1799	126	O - 448	S436	1099	126
O - 349	S535	2485	261	O - 399	S485	1785	261	O - 449	S435	1085	261
O - 350	S534	2471	126	O - 400	S484	1771	126	O - 450	S434	1071	126

Table 137. Pad Center Coordinates [Unit: μm]

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 451	S433	1057	261	O - 501	S383	357	261	O - 551	S333	-427	261
O - 452	S432	1043	126	O - 502	S382	343	126	O - 552	S332	-441	126
O - 453	S431	1029	261	O - 503	S381	329	261	O - 553	S331	-455	261
O - 454	S430	1015	126	O - 504	S380	315	126	O - 554	S330	-469	126
O - 455	S429	1001	261	O - 505	S379	301	261	O - 555	S329	-483	261
O - 456	S428	987	126	O - 506	S378	287	126	O - 556	S328	-497	126
O - 457	S427	973	261	O - 507	S377	273	261	O - 557	S327	-511	261
O - 458	S426	959	126	O - 508	S376	259	126	O - 558	S326	-525	126
O - 459	S425	945	261	O - 509	S375	245	261	O - 559	S325	-539	261
O - 460	S424	931	126	O - 510	S374	231	126	O - 560	S324	-553	126
O - 461	S423	917	261	O - 511	S373	217	261	O - 561	S323	-567	261
O - 462	S422	903	126	O - 512	S372	203	126	O - 562	S322	-581	126
O - 463	S421	889	261	O - 513	S371	189	261	O - 563	S321	-595	261
O - 464	S420	875	126	O - 514	S370	175	126	O - 564	S320	-609	126
O - 465	S419	861	261	O - 515	S369	161	261	O - 565	S319	-623	261
O - 466	S418	847	126	O - 516	S368	147	126	O - 566	S318	-637	126
O - 467	S417	833	261	O - 517	S367	133	261	O - 567	S317	-651	261
O - 468	S416	819	126	O - 518	S366	119	126	O - 568	S316	-665	126
O - 469	S415	805	261	O - 519	S365	105	261	O - 569	S315	-679	261
O - 470	S414	791	126	O - 520	S364	91	126	O - 570	S314	-693	126
O - 471	S413	777	261	O - 521	S363	77	261	O - 571	S313	-707	261
O - 472	S412	763	126	O - 522	S362	63	126	O - 572	S312	-721	126
O - 473	S411	749	261	O - 523	S361	49	261	O - 573	S311	-735	261
O - 474	S410	735	126	O - 524	S360	-49	126	O - 574	S310	-749	126
O - 475	S409	721	261	O - 525	S359	-63	261	O - 575	S309	-763	261
O - 476	S408	707	126	O - 526	S358	-77	126	O - 576	S308	-777	126
O - 477	S407	693	261	O - 527	S357	-91	261	O - 577	S307	-791	261
O - 478	S406	679	126	O - 528	S356	-105	126	O - 578	S306	-805	126
O - 479	S405	665	261	O - 529	S355	-119	261	O - 579	S305	-819	261
O - 480	S404	651	126	O - 530	S354	-133	126	O - 580	S304	-833	126
O - 481	S403	637	261	O - 531	S353	-147	261	O - 581	S303	-847	261

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 482	S402	623	126	O - 532	S352	-161	126	O - 582	S302	-861	126
O - 483	S401	609	261	O - 533	S351	-175	261	O - 583	S301	-875	261
O - 484	S400	595	126	O - 534	S350	-189	126	O - 584	S300	-889	126
O - 485	S399	581	261	O - 535	S349	-203	261	O - 585	S299	-903	261
O - 486	S398	567	126	O - 536	S348	-217	126	O - 586	S298	-917	126
O - 487	S397	553	261	O - 537	S347	-231	261	O - 587	S297	-931	261
O - 488	S396	539	126	O - 538	S346	-245	126	O - 588	S296	-945	126
O - 489	S395	525	261	O - 539	S345	-259	261	O - 589	S295	-959	261
O - 490	S394	511	126	O - 540	S344	-273	126	O - 590	S294	-973	126
O - 491	S393	497	261	O - 541	S343	-287	261	O - 591	S293	-987	261
O - 492	S392	483	126	O - 542	S342	-301	126	O - 592	S292	-1001	126
O - 493	S391	469	261	O - 543	S341	-315	261	O - 593	S291	-1015	261
O - 494	S390	455	126	O - 544	S340	-329	126	O - 594	S290	-1029	126
O - 495	S389	441	261	O - 545	S339	-343	261	O - 595	S289	-1043	261
O - 496	S388	427	126	O - 546	S338	-357	126	O - 596	S288	-1057	126
O - 497	S387	413	261	O - 547	S337	-371	261	O - 597	S287	-1071	261
O - 498	S386	399	126	O - 548	S336	-385	126	O - 598	S286	-1085	126
O - 499	S385	385	261	O - 549	S335	-399	261	O - 599	S285	-1099	261
O - 500	S384	371	126	O - 550	S334	-413	126	O - 600	S284	-1113	126

Table 138. Pad Center Coordinates [Unit: μm]

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 601	S283	-1127	261	O - 651	S233	-1827	261	O - 701	S183	-2527	261
O - 602	S282	-1141	126	O - 652	S232	-1841	126	O - 702	S182	-2541	126
O - 603	S281	-1155	261	O - 653	S231	-1855	261	O - 703	S181	-2555	261
O - 604	S280	-1169	126	O - 654	S230	-1869	126	O - 704	S180	-2569	126
O - 605	S279	-1183	261	O - 655	S229	-1883	261	O - 705	S179	-2583	261
O - 606	S278	-1197	126	O - 656	S228	-1897	126	O - 706	S178	-2597	126
O - 607	S277	-1211	261	O - 657	S227	-1911	261	O - 707	S177	-2611	261
O - 608	S276	-1225	126	O - 658	S226	-1925	126	O - 708	S176	-2625	126
O - 609	S275	-1239	261	O - 659	S225	-1939	261	O - 709	S175	-2639	261
O - 610	S274	-1253	126	O - 660	S224	-1953	126	O - 710	S174	-2653	126
O - 611	S273	-1267	261	O - 661	S223	-1967	261	O - 711	S173	-2667	261
O - 612	S272	-1281	126	O - 662	S222	-1981	126	O - 712	S172	-2681	126
O - 613	S271	-1295	261	O - 663	S221	-1995	261	O - 713	S171	-2695	261
O - 614	S270	-1309	126	O - 664	S220	-2009	126	O - 714	S170	-2709	126
O - 615	S269	-1323	261	O - 665	S219	-2023	261	O - 715	S169	-2723	261
O - 616	S268	-1337	126	O - 666	S218	-2037	126	O - 716	S168	-2737	126
O - 617	S267	-1351	261	O - 667	S217	-2051	261	O - 717	S167	-2751	261
O - 618	S266	-1365	126	O - 668	S216	-2065	126	O - 718	S166	-2765	126
O - 619	S265	-1379	261	O - 669	S215	-2079	261	O - 719	S165	-2779	261
O - 620	S264	-1393	126	O - 670	S214	-2093	126	O - 720	S164	-2793	126
O - 621	S263	-1407	261	O - 671	S213	-2107	261	O - 721	S163	-2807	261
O - 622	S262	-1421	126	O - 672	S212	-2121	126	O - 722	S162	-2821	126
O - 623	S261	-1435	261	O - 673	S211	-2135	261	O - 723	S161	-2835	261
O - 624	S260	-1449	126	O - 674	S210	-2149	126	O - 724	S160	-2849	126
O - 625	S259	-1463	261	O - 675	S209	-2163	261	O - 725	S159	-2863	261
O - 626	S258	-1477	126	O - 676	S208	-2177	126	O - 726	S158	-2877	126

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 627	S257	-1491	261	O - 677	S207	-2191	261	O - 727	S157	-2891	261
O - 628	S256	-1505	126	O - 678	S206	-2205	126	O - 728	S156	-2905	126
O - 629	S255	-1519	261	O - 679	S205	-2219	261	O - 729	S155	-2919	261
O - 630	S254	-1533	126	O - 680	S204	-2233	126	O - 730	S154	-2933	126
O - 631	S253	-1547	261	O - 681	S203	-2247	261	O - 731	S153	-2947	261
O - 632	S252	-1561	126	O - 682	S202	-2261	126	O - 732	S152	-2961	126
O - 633	S251	-1575	261	O - 683	S201	-2275	261	O - 733	S151	-2975	261
O - 634	S250	-1589	126	O - 684	S200	-2289	126	O - 734	S150	-2989	126
O - 635	S249	-1603	261	O - 685	S199	-2303	261	O - 735	S149	-3003	261
O - 636	S248	-1617	126	O - 686	S198	-2317	126	O - 736	S148	-3017	126
O - 637	S247	-1631	261	O - 687	S197	-2331	261	O - 737	S147	-3031	261
O - 638	S246	-1645	126	O - 688	S196	-2345	126	O - 738	S146	-3045	126
O - 639	S245	-1659	261	O - 689	S195	-2359	261	O - 739	S145	-3059	261
O - 640	S244	-1673	126	O - 690	S194	-2373	126	O - 740	S144	-3073	126
O - 641	S243	-1687	261	O - 691	S193	-2387	261	O - 741	S143	-3087	261
O - 642	S242	-1701	126	O - 692	S192	-2401	126	O - 742	S142	-3101	126
O - 643	S241	-1715	261	O - 693	S191	-2415	261	O - 743	S141	-3115	261
O - 644	S240	-1729	126	O - 694	S190	-2429	126	O - 744	S140	-3129	126
O - 645	S239	-1743	261	O - 695	S189	-2443	261	O - 745	S139	-3143	261
O - 646	S238	-1757	126	O - 696	S188	-2457	126	O - 746	S138	-3157	126
O - 647	S237	-1771	261	O - 697	S187	-2471	261	O - 747	S137	-3171	261
O - 648	S236	-1785	126	O - 698	S186	-2485	126	O - 748	S136	-3185	126
O - 649	S235	-1799	261	O - 699	S185	-2499	261	O - 749	S135	-3199	261
O - 650	S234	-1813	126	O - 700	S184	-2513	126	O - 750	S134	-3213	126

Table 139. Pad Center Coordinates [Unit: µm]

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 751	S133	-3227	261	O - 801	S83	-3927	261	O - 851	S33	-4627	261
O - 752	S132	-3241	126	O - 802	S82	-3941	126	O - 852	S32	-4641	126
O - 753	S131	-3255	261	O - 803	S81	-3955	261	O - 853	S31	-4655	261
O - 754	S130	-3269	126	O - 804	S80	-3969	126	O - 854	S30	-4669	126
O - 755	S129	-3283	261	O - 805	S79	-3983	261	O - 855	S29	-4683	261
O - 756	S128	-3297	126	O - 806	S78	-3997	126	O - 856	S28	-4697	126
O - 757	S127	-3311	261	O - 807	S77	-4011	261	O - 857	S27	-4711	261
O - 758	S126	-3325	126	O - 808	S76	-4025	126	O - 858	S26	-4725	126
O - 759	S125	-3339	261	O - 809	S75	-4039	261	O - 859	S25	-4739	261
O - 760	S124	-3353	126	O - 810	S74	-4053	126	O - 860	S24	-4753	126
O - 761	S123	-3367	261	O - 811	S73	-4067	261	O - 861	S23	-4767	261
O - 762	S122	-3381	126	O - 812	S72	-4081	126	O - 862	S22	-4781	126
O - 763	S121	-3395	261	O - 813	S71	-4095	261	O - 863	S21	-4795	261
O - 764	S120	-3409	126	O - 814	S70	-4109	126	O - 864	S20	-4809	126
O - 765	S119	-3423	261	O - 815	S69	-4123	261	O - 865	S19	-4823	261
O - 766	S118	-3437	126	O - 816	S68	-4137	126	O - 866	S18	-4837	126
O - 767	S117	-3451	261	O - 817	S67	-4151	261	O - 867	S17	-4851	261
O - 768	S116	-3465	126	O - 818	S66	-4165	126	O - 868	S16	-4865	126
O - 769	S115	-3479	261	O - 819	S65	-4179	261	O - 869	S15	-4879	261
O - 770	S114	-3493	126	O - 820	S64	-4193	126	O - 870	S14	-4893	126
O - 771	S113	-3507	261	O - 821	S63	-4207	261	O - 871	S13	-4907	261

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 772	S112	-3521	126	O - 822	S62	-4221	126	O - 872	S12	-4921	126
O - 773	S111	-3535	261	O - 823	S61	-4235	261	O - 873	S11	-4935	261
O - 774	S110	-3549	126	O - 824	S60	-4249	126	O - 874	S10	-4949	126
O - 775	S109	-3563	261	O - 825	S59	-4263	261	O - 875	S9	-4963	261
O - 776	S108	-3577	126	O - 826	S58	-4277	126	O - 876	S8	-4977	126
O - 777	S107	-3591	261	O - 827	S57	-4291	261	O - 877	S7	-4991	261
O - 778	S106	-3605	126	O - 828	S56	-4305	126	O - 878	S6	-5005	126
O - 779	S105	-3619	261	O - 829	S55	-4319	261	O - 879	S5	-5019	261
O - 780	S104	-3633	126	O - 830	S54	-4333	126	O - 880	S4	-5033	126
O - 781	S103	-3647	261	O - 831	S53	-4347	261	O - 881	S3	-5047	261
O - 782	S102	-3661	126	O - 832	S52	-4361	126	O - 882	S2	-5061	126
O - 783	S101	-3675	261	O - 833	S51	-4375	261	O - 883	S1	-5075	261
O - 784	S100	-3689	126	O - 834	S50	-4389	126	O - 884	G319	-5131	126
O - 785	S99	-3703	261	O - 835	S49	-4403	261	O - 885	G317	-5145	261
O - 786	S98	-3717	126	O - 836	S48	-4417	126	O - 886	G315	-5159	126
O - 787	S97	-3731	261	O - 837	S47	-4431	261	O - 887	G313	-5173	261
O - 788	S96	-3745	126	O - 838	S46	-4445	126	O - 888	G311	-5187	126
O - 789	S95	-3759	261	O - 839	S45	-4459	261	O - 889	G309	-5201	261
O - 790	S94	-3773	126	O - 840	S44	-4473	126	O - 890	G307	-5215	126
O - 791	S93	-3787	261	O - 841	S43	-4487	261	O - 891	G305	-5229	261
O - 792	S92	-3801	126	O - 842	S42	-4501	126	O - 892	G303	-5243	126
O - 793	S91	-3815	261	O - 843	S41	-4515	261	O - 893	G301	-5257	261
O - 794	S90	-3829	126	O - 844	S40	-4529	126	O - 894	G299	-5271	126
O - 795	S89	-3843	261	O - 845	S39	-4543	261	O - 895	G297	-5285	261
O - 796	S88	-3857	126	O - 846	S38	-4557	126	O - 896	G295	-5299	126
O - 797	S87	-3871	261	O - 847	S37	-4571	261	O - 897	G293	-5313	261
O - 798	S86	-3885	126	O - 848	S36	-4585	126	O - 898	G291	-5327	126
O - 799	S85	-3899	261	O - 849	S35	-4599	261	O - 899	G289	-5341	261
O - 800	S84	-3913	126	O - 850	S34	-4613	126	O - 900	G287	-5355	126

Table 140. Pad Center Coordinates [Unit: μm]

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 901	G285	-5369	261	O - 951	G185	-6069	261	O - 1001	G85	-6769	261
O - 902	G283	-5383	126	O - 952	G183	-6083	126	O - 1002	G83	-6783	126
O - 903	G281	-5397	261	O - 953	G181	-6097	261	O - 1003	G81	-6797	261
O - 904	G279	-5411	126	O - 954	G179	-6111	126	O - 1004	G79	-6811	126
O - 905	G277	-5425	261	O - 955	G177	-6125	261	O - 1005	G77	-6825	261
O - 906	G275	-5439	126	O - 956	G175	-6139	126	O - 1006	G75	-6839	126
O - 907	G273	-5453	261	O - 957	G173	-6153	261	O - 1007	G73	-6853	261
O - 908	G271	-5467	126	O - 958	G171	-6167	126	O - 1008	G71	-6867	126
O - 909	G269	-5481	261	O - 959	G169	-6181	261	O - 1009	G69	-6881	261
O - 910	G267	-5495	126	O - 960	G167	-6195	126	O - 1010	G67	-6895	126
O - 911	G265	-5509	261	O - 961	G165	-6209	261	O - 1011	G65	-6909	261
O - 912	G263	-5523	126	O - 962	G163	-6223	126	O - 1012	G63	-6923	126
O - 913	G261	-5537	261	O - 963	G161	-6237	261	O - 1013	G61	-6937	261
O - 914	G259	-5551	126	O - 964	G159	-6251	126	O - 1014	G59	-6951	126
O - 915	G257	-5565	261	O - 965	G157	-6265	261	O - 1015	G57	-6965	261
O - 916	G255	-5579	126	O - 966	G155	-6279	126	O - 1016	G55	-6979	126

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
O - 917	G253	-5593	261	O - 967	G153	-6293	261	O - 1017	G53	-6993	261
O - 918	G251	-5607	126	O - 968	G151	-6307	126	O - 1018	G51	-7007	126
O - 919	G249	-5621	261	O - 969	G149	-6321	261	O - 1019	G49	-7021	261
O - 920	G247	-5635	126	O - 970	G147	-6335	126	O - 1020	G47	-7035	126
O - 921	G245	-5649	261	O - 971	G145	-6349	261	O - 1021	G45	-7049	261
O - 922	G243	-5663	126	O - 972	G143	-6363	126	O - 1022	G43	-7063	126
O - 923	G241	-5677	261	O - 973	G141	-6377	261	O - 1023	G41	-7077	261
O - 924	G239	-5691	126	O - 974	G139	-6391	126	O - 1024	G39	-7091	126
O - 925	G237	-5705	261	O - 975	G137	-6405	261	O - 1025	G37	-7105	261
O - 926	G235	-5719	126	O - 976	G135	-6419	126	O - 1026	G35	-7119	126
O - 927	G233	-5733	261	O - 977	G133	-6433	261	O - 1027	G33	-7133	261
O - 928	G231	-5747	126	O - 978	G131	-6447	126	O - 1028	G31	-7147	126
O - 929	G229	-5761	261	O - 979	G129	-6461	261	O - 1029	G29	-7161	261
O - 930	G227	-5775	126	O - 980	G127	-6475	126	O - 1030	G27	-7175	126
O - 931	G225	-5789	261	O - 981	G125	-6489	261	O - 1031	G25	-7189	261
O - 932	G223	-5803	126	O - 982	G123	-6503	126	O - 1032	G23	-7203	126
O - 933	G221	-5817	261	O - 983	G121	-6517	261	O - 1033	G21	-7217	261
O - 934	G219	-5831	126	O - 984	G119	-6531	126	O - 1034	G19	-7231	126
O - 935	G217	-5845	261	O - 985	G117	-6545	261	O - 1035	G17	-7245	261
O - 936	G215	-5859	126	O - 986	G115	-6559	126	O - 1036	G15	-7259	126
O - 937	G213	-5873	261	O - 987	G113	-6573	261	O - 1037	G13	-7273	261
O - 938	G211	-5887	126	O - 988	G111	-6587	126	O - 1038	G11	-7287	126
O - 939	G209	-5901	261	O - 989	G109	-6601	261	O - 1039	G9	-7301	261
O - 940	G207	-5915	126	O - 990	G107	-6615	126	O - 1040	G7	-7315	126
O - 941	G205	-5929	261	O - 991	G105	-6629	261	O - 1041	G5	-7329	261
O - 942	G203	-5943	126	O - 992	G103	-6643	126	O - 1042	G3	-7343	126
O - 943	G201	-5957	261	O - 993	G101	-6657	261	O - 1043	G1	-7357	261
O - 944	G199	-5971	126	O - 994	G99	-6671	126	O - 1044	DUMMY	-7371	126
O - 945	G197	-5985	261	O - 995	G97	-6685	261	O - 1045	DUMMY	-7385	261
O - 946	G195	-5999	126	O - 996	G95	-6699	126	O - 1046	DUMMY	-7399	126
O - 947	G193	-6013	261	O - 997	G93	-6713	261				
O - 948	G191	-6027	126	O - 998	G91	-6727	126				
O - 949	G189	-6041	261	O - 999	G89	-6741	261				
O - 950	G187	-6055	126	O -	G87	-6755	126				

6.4. DISPLAY MODULE DEFAULT POSITION

The default position (display driver, glass, filter order, etc) of the display module is always as follow, when MADCTL's (36h) parameter is 00h. The color filter is always RGB (if color filters are used).

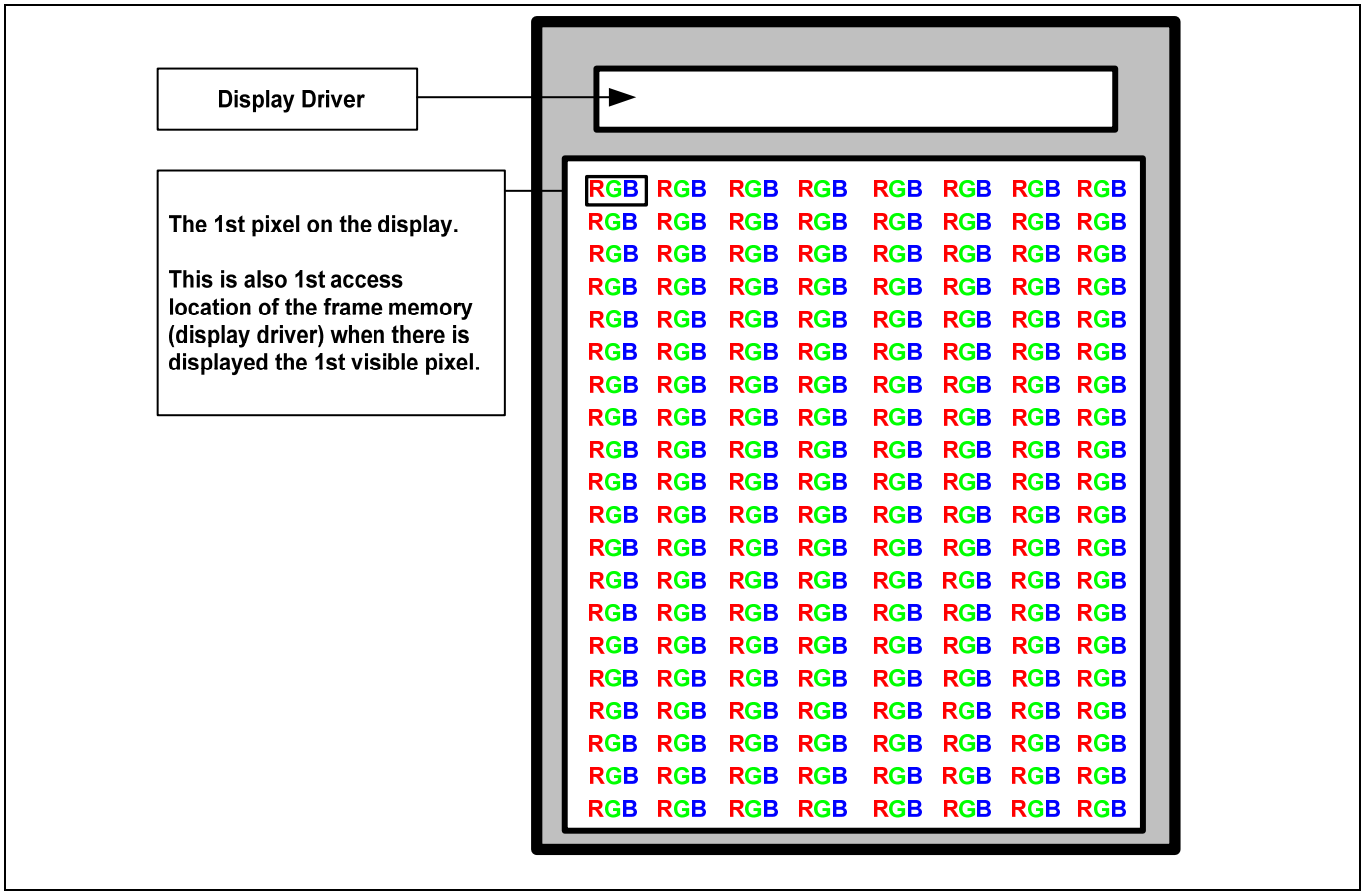


Figure121. Display Module Default Position