

# 16Mb Async. FAST SRAM Specification

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**S6R1616V1M, S6R1616C1M, S6R1616W1M  
S6R1608V1M, S6R1608C1M, S6R1608W1M**

**16M Async FAST SRAM**

**Document Title**

**1Mx16 & 2Mx8 Bit Asynchronous FAST SRAM**

**Revision History**

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Aug. 2012	Preliminary
1.0	Final spec release	Jan. 2013	Final
1.1	Add x8 org (3.3V) and 5.0V product	Aug. 2013	Final
1.2	Add wide Vcc range support 1.65 ~ 3.6V	Sep. 2013	Final
1.3	Add 48FBGA PKG information	Sep. 2013	Final
1.4	Add 8ns and 12ns speed binning Change ordering information table format Remove the ordering information of -YC(I)15, -UC(I)15, -XC(I)15	Nov. 2013	Final
1.5	Decrease operating current value (Icc) 110mA => 85mA @8ns 90mA => 75mA @10ns 80mA => 70mA @12ns 70mA => 65mA @15ns	Sep. 2014	Final

# S6R1616V1M, S6R1616C1M, S6R1616W1M S6R1608V1M, S6R1608C1M, S6R1608W1M      16M Async FAST SRAM

## 1Mx16 & 2Mx8 Bit Asynchronous FAST SRAM

### Features

- Fast Access Time : 8, 10, 12, 15ns(Max)
- CMOS Low Power Dissipation  
Standby (TTL) : 35mA (Max.)  
(CMOS) : 28mA (Max.)  
Operating : 85mA (8ns, Max.)  
75mA (10ns, Max.)
- Single 3.3±0.3V or 5.0±0.5V Power Supply  
- S6R16xxV1M : 3.3 ±0.3V Power Supply  
- S6R16xxC1M : 5.0 ±0.5V Power Supply
- Wide range of Power Supply  
- S6R16xxW1M : 1.65V ~ 3.6V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control(x16 Mode)  
LB : I/O0~ I/O7, UB : I/O8~ I/O15
- Standard 48 TSOP1 and 48FBGA Package pin configurations for 1M x 16
- Standard 44 TSOP2 and 48FBGA Package pin configurations for 2M x 8
- ROHS compliant
- Operating in Commercial and Industrial Temperature range.

### General Description

The S6R1616(V/C/W)1M and S6R1608(V/C/W)1M is a 16,789,216-bit high-speed Static Random Access Memory organized as 1M(2M) words by 16(8) bits. The S6R1616(V/C/W)1M (S6R1608(V/C/W)1M) uses 16(8) common input and output lines and have an output enable pin which operates faster than address access time at read cycle. And S6R1616(V/C/W)1M allows that lower and upper byte access by data byte control( $\overline{UB}$ ,  $\overline{LB}$ ). The device is fabricated using advanced CMOS process, 6-TR based cell technology and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The S6R1616(V/C/W)1M is packaged in industry standard 48 TSOP1 and 48FBGA.

The S6R1608(V/C/W)1M is packaged in industrial standard 44TSOP2 and 48FBGA.

### 16Mb Asynchronous FAST SRAM Ordering Information (1Mx16)

Density	Org.	Part Number	Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
16Mb	1Mx16	S6R1616V1M-YC(I)08	3.3	8	4	48 TSOP1	C : Commercial Temperature I : Industrial Temperature
		S6R1616W1M-YC(I)08	3.3	8	4	48 TSOP1	
		S6R1616W1M-YC(I)08	2.5	10	5	48 TSOP1	
		S6R1616W1M-YC(I)08	1.8	12	6	48 TSOP1	
		S6R1616V1M-XC(I)08	3.3	8	4	48 FBGA	
		S6R1616W1M-XC(I)08	3.3	8	4	48 FBGA	
		S6R1616W1M-XC(I)08	2.5	10	5	48 FBGA	
		S6R1616W1M-XC(I)08	1.8	12	6	48 FBGA	
		S6R1616C1M-YC(I)10	5.0	10	5	48 TSOP1	
		S6R1616V1M-YC(I)10	3.3	10	5	48 TSOP1	
		S6R1616W1M-YC(I)10	3.3	10	5	48 TSOP1	
		S6R1616W1M-YC(I)10	2.5	10	5	48 TSOP1	
		S6R1616W1M-YC(I)10	1.8	15	7	48 TSOP1	
		S6R1616C1M-XC(I)10	5.0	10	5	48 FBGA	
		S6R1616V1M-XC(I)10	3.3	10	5	48 FBGA	
		S6R1616W1M-XC(I)10	3.3	10	5	48 FBGA	
		S6R1616W1M-XC(I)10	2.5	10	5	48 FBGA	
		S6R1616W1M-XC(I)10	1.8	15	7	48 FBGA	

**S6R1616V1M, S6R1616C1M, S6R1616W1M  
S6R1608V1M, S6R1608C1M, S6R1608W1M      16M Async FAST SRAM**

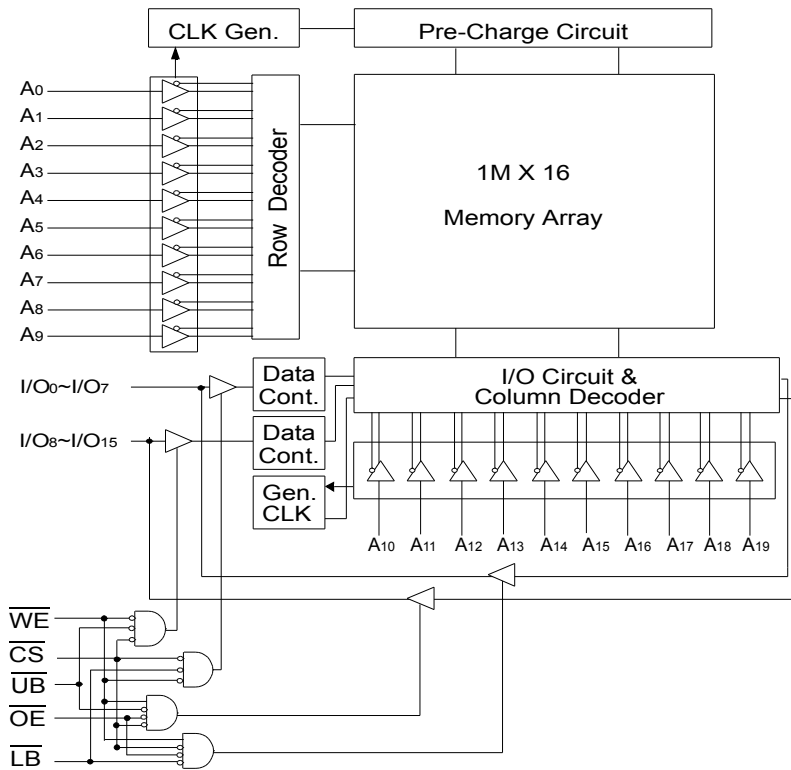
**16Mb Asynchronous FAST SRAM Ordering Information (2Mx8)**

Density	Org.	Part Number	Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
16Mb	2Mx8	S6R1608V1M-UC(I)08	3.3	8	4	44 TSOP2	C : Commercial Temperature I : Industrial Temperature
		S6R1608W1M-UC(I)08	3.3	8	4	44 TSOP2	
		S6R1608W1M-UC(I)08	2.5	10	5	44 TSOP2	
		S6R1608W1M-UC(I)08	1.8	12	6	44 TSOP2	
		S6R1608V1M-XC(I)08	3.3	8	4	48 FBGA	
		S6R1608W1M-XC(I)08	3.3	8	4	48 FBGA	
		S6R1608W1M-XC(I)08	2.5	10	5	48 FBGA	
		S6R1608W1M-XC(I)08	1.8	12	6	48 FBGA	
		S6R1608C1M-UC(I)10	5.0	10	5	44 TSOP2	
		S6R1608V1M-UC(I)10	3.3	10	5	44 TSOP2	
		S6R1608W1M-UC(I)10	3.3	10	5	44 TSOP2	
		S6R1608W1M-UC(I)10	2.5	10	5	44 TSOP2	
		S6R1608W1M-UC(I)10	1.8	15	7	44 TSOP2	
		S6R1608C1M-XC(I)10	5.0	10	5	48 FBGA	
		S6R1608V1M-XC(I)10	3.3	10	5	48 FBGA	
		S6R1608W1M-XC(I)10	3.3	10	5	48 FBGA	
		S6R1608W1M-XC(I)10	2.5	10	5	48 FBGA	
		S6R1608W1M-XC(I)10	1.8	15	7	48 FBGA	

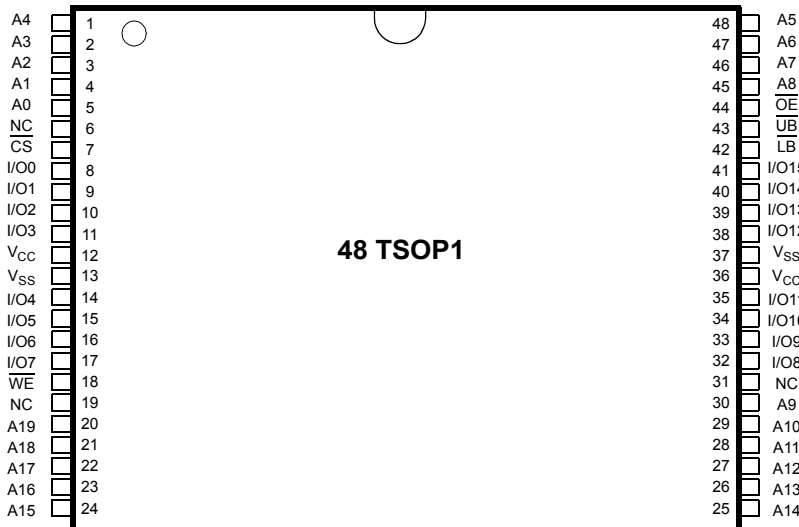
**S6R1616V1M, S6R1616C1M, S6R1616W1M  
S6R1608V1M, S6R1608C1M, S6R1608W1M**

**16M Async FAST SRAM**

**Logic Block Diagram - S6R1616(V/C/W)1M (1M x 16)**



**48 TSOP1 Package Pin Configurations (Top View) - S6R1616(V/C/W)1M (1M x 16)**



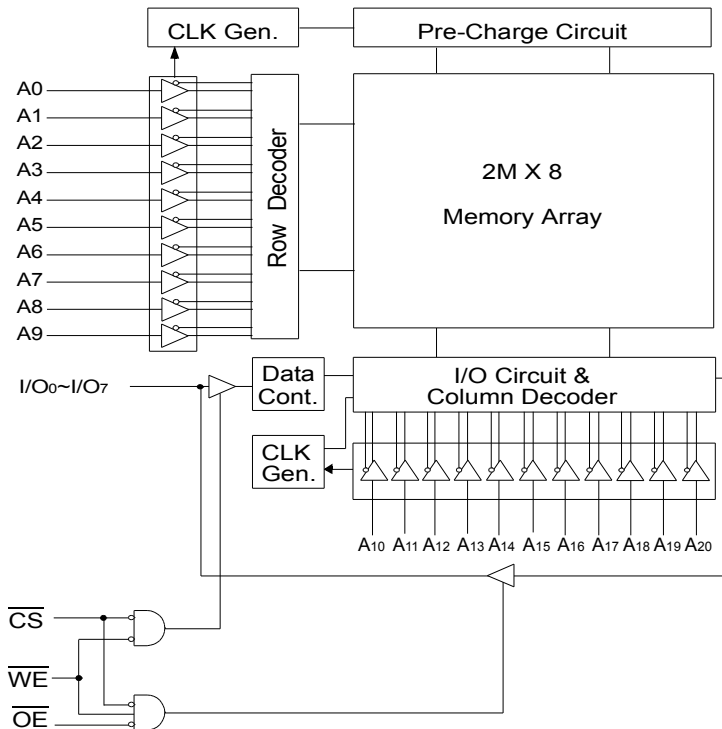
**Pin Function**

Pin Name	Pin Function
A0 - A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O0~I/O7)
$\overline{UB}$	Upper-byte Control(I/O8~I/O15)
I/O0 ~ I/O15	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

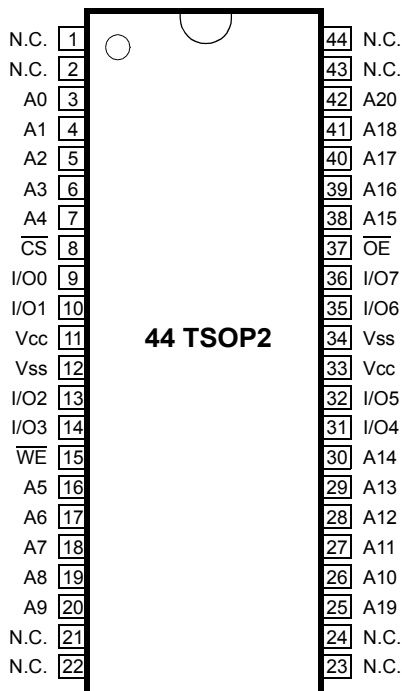
**S6R1616V1M, S6R1616C1M, S6R1616W1M  
S6R1608V1M, S6R1608C1M, S6R1608W1M**

**16M Async FAST SRAM**

**Logic Block Diagram - S6R1608(V/C/W)1M (2M x 8)**



**44 TSOP2 Package Pin Configurations (Top View) - S6R1608(V/C/W)1M (2M x 8)**



**Pin Function**

Pin Name	Pin Function
A0 - A20	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O0 ~ I/O7	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

# S6R1616V1M, S6R1616C1M, S6R1616W1M S6R1608V1M, S6R1608C1M, S6R1608W1M 16M Async FAST SRAM

## 48FBGA - S6R1616(V/C/W)1M, 1Mx16 - Top View

### PKG Pin Configurations

	1	2	3	4	5	6
<b>A</b>	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	NC
<b>B</b>	I/O <sub>8</sub>	$\overline{\text{UB}}$	A <sub>3</sub>	A <sub>4</sub>	$\overline{\text{CS}}$	I/O <sub>0</sub>
<b>C</b>	I/O <sub>9</sub>	I/O <sub>10</sub>	A <sub>5</sub>	A <sub>6</sub>	I/O <sub>1</sub>	I/O <sub>2</sub>
<b>D</b>	V <sub>ss</sub>	I/O <sub>11</sub>	A <sub>17</sub>	A <sub>7</sub>	I/O <sub>3</sub>	V <sub>cc</sub>
<b>E</b>	V <sub>cc</sub>	I/O <sub>12</sub>	NC	A <sub>16</sub>	I/O <sub>4</sub>	V <sub>ss</sub>
<b>F</b>	I/O <sub>14</sub>	I/O <sub>13</sub>	A <sub>14</sub>	A <sub>15</sub>	I/O <sub>5</sub>	I/O <sub>6</sub>
<b>G</b>	I/O <sub>15</sub>	A <sub>19</sub>	A <sub>12</sub>	A <sub>13</sub>	$\overline{\text{WE}}$	I/O <sub>7</sub>
<b>H</b>	A <sub>18</sub>	A <sub>8</sub>	A <sub>9</sub>	A <sub>10</sub>	A <sub>11</sub>	NC

### Pin Function

Pin Name	Pin Function
A <sub>0</sub> - A <sub>19</sub>	Address Inputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CS}}$	Chip Select
$\overline{\text{OE}}$	Output Enable
$\overline{\text{LB}}$	Lower-byte Control(I/O <sub>0</sub> ~I/O <sub>7</sub> )
$\overline{\text{UB}}$	Upper-byte Control(I/O <sub>8</sub> ~I/O <sub>15</sub> )
I/O <sub>0</sub> ~ I/O <sub>15</sub>	Data Inputs/Outputs
V <sub>cc</sub>	Power
V <sub>ss</sub>	Ground
NC	No Connection

## 48FBGA - S6R1608(V/C/W)1M, 2Mx8 - Top View

### PKG Pin Configurations

	1	2	3	4	5	6
<b>A</b>	NC	$\overline{\text{OE}}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	NC
<b>B</b>	NC	NC	A <sub>3</sub>	A <sub>4</sub>	$\overline{\text{CS}}$	I/O <sub>0</sub>
<b>C</b>	NC	NC	A <sub>5</sub>	A <sub>6</sub>	I/O <sub>1</sub>	I/O <sub>2</sub>
<b>D</b>	V <sub>ss</sub>	NC	A <sub>17</sub>	A <sub>7</sub>	I/O <sub>3</sub>	V <sub>cc</sub>
<b>E</b>	V <sub>cc</sub>	NC	NC	A <sub>16</sub>	I/O <sub>4</sub>	V <sub>ss</sub>
<b>F</b>	NC	NC	A <sub>14</sub>	A <sub>15</sub>	I/O <sub>5</sub>	I/O <sub>6</sub>
<b>G</b>	NC	A <sub>19</sub>	A <sub>12</sub>	A <sub>13</sub>	$\overline{\text{WE}}$	I/O <sub>7</sub>
<b>H</b>	A <sub>18</sub>	A <sub>8</sub>	A <sub>9</sub>	A <sub>10</sub>	A <sub>11</sub>	A <sub>20</sub>

### Pin Function

Pin Name	Pin Function
A <sub>0</sub> - A <sub>20</sub>	Address Inputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CS}}$	Chip Select
$\overline{\text{OE}}$	Output Enable
I/O <sub>0</sub> ~ I/O <sub>7</sub>	Data Inputs/Outputs
V <sub>cc</sub>	Power
V <sub>ss</sub>	Ground
NC	No Connection

# S6R1616V1M, S6R1616C1M, S6R1616W1M S6R1608V1M, S6R1608C1M, S6R1608W1M

## 16M Async FAST SRAM

### Absolute Maximum Ratings\*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to VSS	3.3V Product	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5V	V
	5.0V Product			
	Wide V <sub>CC</sub> ** Product			
Voltage on V <sub>CC</sub> Supply Relative to VSS	3.3V Product	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 4.6	V
	5.0V Product		-0.5 to 7.0	
	Wide V <sub>CC</sub> ** Product		-0.5 to 4.6	
Power Dissipation		P <sub>D</sub>	1.0	W
Storage Temperature		T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	Commercial	T <sub>A</sub>	0 to 70	°C
	Industrial	T <sub>A</sub>	-40 to 85	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\* Wide V<sub>CC</sub> Range is 1.65V ~ 3.6V

### Recommended DC Operating Conditions\* (T<sub>A</sub>=0 to 70°C)

Parameter	Operating V <sub>CC</sub> (V)	Symbol	Min	Typ	Max	Unit
Supply Voltage	5.0	V <sub>CC</sub>	4.5	5.0	5.5	V
	3.3	V <sub>CC</sub>	3.0	3.3	3.6	
	Wide 2.4 ~ 3.6	V <sub>CC</sub>	2.4	2.5/3.3	3.6	
	Wide 1.65 ~ 2.2	V <sub>CC</sub>	1.65	1.8	2.2	
Ground		V <sub>SS</sub>	0	0	0	V
Input High Voltage	5.0	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5	V
	3.3	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.5	
	Wide 2.4 ~ 3.6	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3	
	Wide 1.65 ~ 2.2	V <sub>IH</sub>	1.4	-	V <sub>CC</sub> +0.2	
Input Low Voltage	5.0	V <sub>IL</sub>	-0.3	-	0.8	V
	3.3	V <sub>IL</sub>	-0.3	-	0.8	
	Wide 2.4 ~ 3.6	V <sub>IL</sub>	-0.3	-	0.7	
	Wide 1.65 ~ 2.2	V <sub>IL</sub>	-0.2	-	0.4	

\* The above parameters are also guaranteed for industrial temperature range.



# S6R1616V1M, S6R1616C1M, S6R1616W1M S6R1608V1M, S6R1608C1M, S6R1608W1M

## 16M Async FAST SRAM

### DC and Operating Characteristics\* (TA=0 to 70°C)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-2	2	μA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-2	2	μA	
Operating Current**	I <sub>CC</sub>	Min. Cycle, 100% Duty CS=V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	8ns	-	85	mA
			10ns	-	75	
			12ns	-	70	
			15ns	-	65	
Standby Current	I <sub>SB</sub>	Min. Cycle, $\overline{CS}=V_{IH}$	-	35	mA	
	I <sub>SB1</sub>	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	-	28		
Output Low Voltage Level	V <sub>OL</sub>	V <sub>CC</sub> =4.5V, I <sub>OL</sub> =8mA, 5.0V Product	-	0.4	V	
		V <sub>CC</sub> =3.0V, I <sub>OL</sub> =8mA, 3.3V & Wide V <sub>CC</sub> ** Product	-	0.4		
		V <sub>CC</sub> =2.4V, I <sub>OL</sub> =1mA, Wide V <sub>CC</sub> ** Product	-	0.4		
		V <sub>CC</sub> =1.65V, I <sub>OL</sub> =0.1mA, Wide V <sub>CC</sub> ** Product	-	0.2		
Output High Voltage Level	V <sub>OH</sub>	V <sub>CC</sub> =4.5V, I <sub>OH</sub> =-4mA, 5.0V Product	2.4	-	V	
		V <sub>CC</sub> =3.0V, I <sub>OH</sub> =-4mA, 3.3V & Wide V <sub>CC</sub> ** Product	2.4	-		
		V <sub>CC</sub> =2.4V, I <sub>OH</sub> =-1mA, Wide V <sub>CC</sub> ** Product	1.8	-		
		V <sub>CC</sub> =1.65V, I <sub>OH</sub> =-0.1mA, Wide V <sub>CC</sub> ** Product	1.4	-		

\* The above parameters are also guaranteed for industrial temperature range.

\*\* Wide V<sub>CC</sub> Range is 1.65V ~ 3.6V

### Capacitance\* (TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	TYP	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	8	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF

\* Capacitance is sampled and not 100% tested.

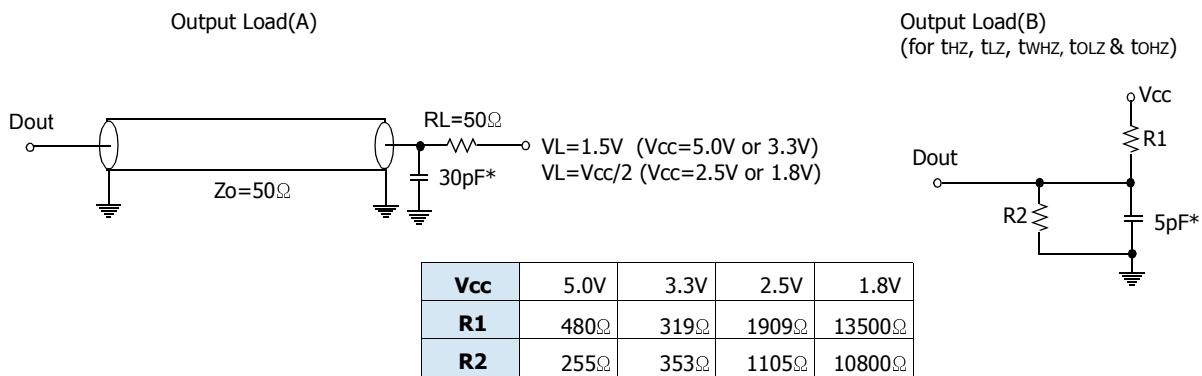
# S6R1616V1M, S6R1616C1M, S6R1616W1M S6R1608V1M, S6R1608C1M, S6R1608W1M

## 16M Async FAST SRAM

### Test Conditions\*

Parameter	Value
Input Pulse Level	0 to 3.0V (Vcc=3.3V or 5.0V)
	0 to 2.5V (Vcc=2.5V)
	0 to 1.8V (Vcc=1.8V)
Input Rise and Fall Time	1V/1ns
Input and Output Timing Reference Levels	1.5V (Vcc=3.3V or 5.0V)
	1/2Vcc (Vcc= 1.8V or 2.5V)
Output Load	See Fig. 1

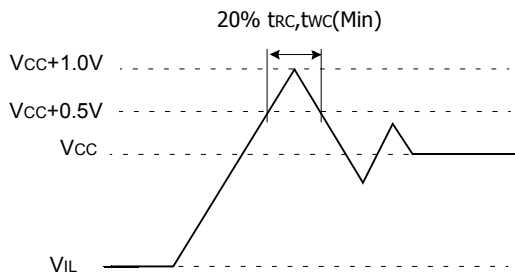
\* The above parameters are also guaranteed at industrial temperature range.



\* Including Scope and Jig Capacitance

Fig. 1

### Overshoot Timing



### Undershoot Timing

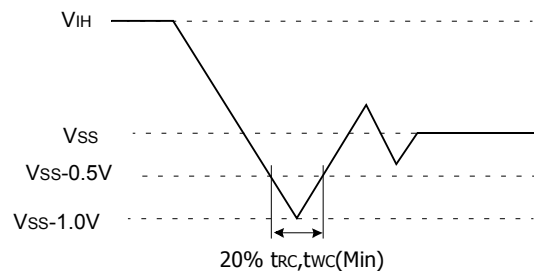


Fig. 2

### Functional Description (x8 Mode)

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	DOUT	Icc
L	L	X	Write	DIN	Icc

\* X means Don't Care.

# S6R1616V1M, S6R1616C1M, S6R1616W1M S6R1608V1M, S6R1608C1M, S6R1608W1M

## 16M Async FAST SRAM

### Functional Description (x16 Mode)

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}^{**}$	$\overline{UB}^{**}$	Mode	I/O Pin		Supply Current
						I/O <sub>0</sub> ~I/O <sub>7</sub>	I/O <sub>8</sub> ~I/O <sub>15</sub>	
H	X	X*	X	X	Not Select	High-Z	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
L	H	H	X	X	Output Disable	High-Z	High-Z	I <sub>CC</sub>
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	I <sub>CC</sub>
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	I <sub>CC</sub>
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

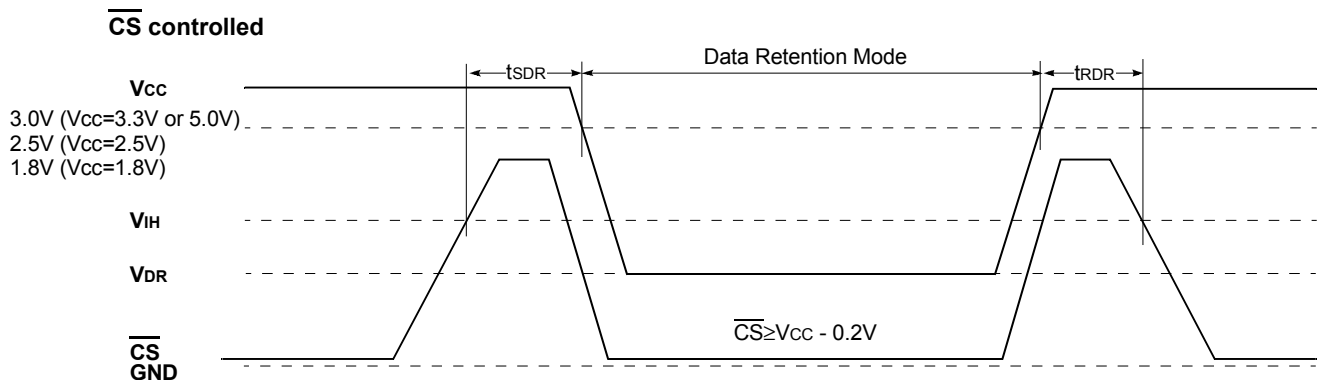
\* X means Don't Care.

### Data Retention Characteristics\* (T<sub>A</sub>=0 to 70°C)

Parameter	Product	Operating V <sub>CC</sub> (V)	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V <sub>CC</sub> for Data Retention	5.0V Product	5.0	V <sub>DR</sub>	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	5.5	V
	3.3V Product	3.3			2.0	-	3.6	
	Wide 2.4V ~ 3.6V	2.5/3.3			2.0	-	3.6	
	Wide 1.65V ~ 2.2V	1.8			1.5	-	3.6	
Data Retention Current	5.0V Product	5.0	I <sub>DR</sub>	$V_{CC}=2.0V$ $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	20	mA
	3.3V Product	3.3			-	-	20	
	Wide 2.4V ~ 3.6V	2.5/3.3			-	-	28	
	Wide 1.65V ~ 2.2V	1.8		$V_{CC}=1.5V$ $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	28	
Data Retention Set-Up Time			t <sub>SDR</sub>	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time			t <sub>RDR</sub>		5	-	-	ms

\* The above parameters are also guaranteed at industrial temperature range.

### Data Retention Wave Form



# S6R1616V1M, S6R1616C1M, S6R1616W1M S6R1608V1M, S6R1608C1M, S6R1608W1M

## 16M Async FAST SRAM

### Read Cycle\*

Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	8	-	10	-	12	-	15	-	ns
Address Access Time	t <sub>AA</sub>	-	8	-	10	-	12	-	15	ns
Chip Select to Output	t <sub>CO</sub>	-	8	-	10	-	12	-	15	ns
Output Enable to Valid Output	t <sub>OE</sub>	-	4	-	5	-	6	-	7	ns
$\overline{UB}$ , $\overline{LB}$ Access Time **	t <sub>BA</sub>	-	4	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t <sub>LZ</sub>	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	0	-	0	-	0	-	0	-	ns
$\overline{UB}$ , $\overline{LB}$ Enable to Low-Z Output **	t <sub>BLZ</sub>	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	0	4	0	5	0	6	0	7	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	4	0	5	0	6	0	7	ns
$\overline{UB}$ , $\overline{LB}$ Disable to High-Z Output **	t <sub>BHZ</sub>	0	4	0	5	0	6	0	7	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t <sub>PU</sub>	0	-	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t <sub>PD</sub>	-	8	-	10	-	12	-	15	ns

\* The above parameters are also guaranteed for industrial temperature range.

### Write Cycle\*

Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	8	-	10	-	12	-	15	-	ns
Chip Select to End of Write	t <sub>CW</sub>	6	-	7	-	9	-	12	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t <sub>AW</sub>	6	-	7	-	9	-	12	-	ns
Write Pulse Width( $\overline{OE}$ High)	t <sub>WP</sub>	6	-	7	-	9	-	12	-	ns
Write Pulse Width( $\overline{OE}$ Low)	t <sub>WP1</sub>	8	-	10	-	12	-	15	-	ns
$\overline{UB}$ , $\overline{LB}$ Valid to End of Write **	t <sub>BW</sub>	6	-	7	-	9	-	12	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	t <sub>WHZ</sub>	0	4	0	5	0	6	0	7	ns
Data to Write Time Overlap	t <sub>DW</sub>	4	-	5	-	7	-	8	-	ns
Data Hold from Write Time	t <sub>DH</sub>	0	-	0	-	0	-	0	-	ns
End of Write to Output Low-Z	t <sub>OW</sub>	3	-	3	-	3	-	3	-	ns

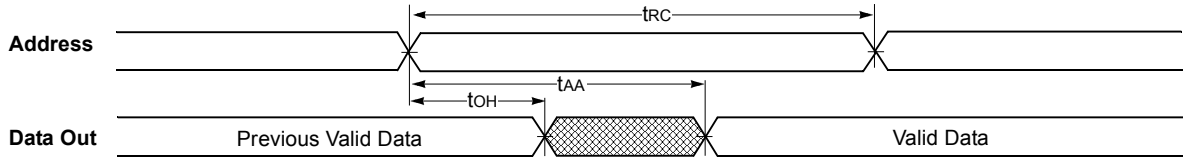
\* The above parameters are also guaranteed for industrial temperature range.

**S6R1616V1M, S6R1616C1M, S6R1616W1M  
S6R1608V1M, S6R1608C1M, S6R1608W1M**

**16M Async FAST SRAM**

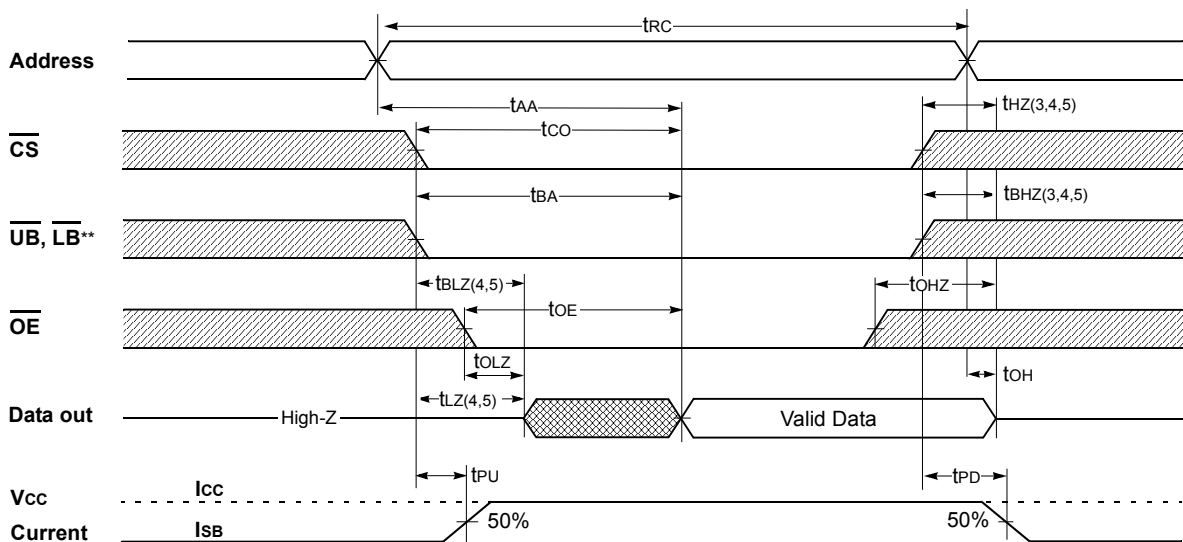
**Timing Diagrams**

**Timing Waveform Of Read Cycle(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}, \overline{LB}=V_{IL}$  \*\*)



\*\* Those parameters are applied for x16 mode only.

**Timing Waveform Of Read Cycle(2)** ( $\overline{WE}=V_{IH}$ )

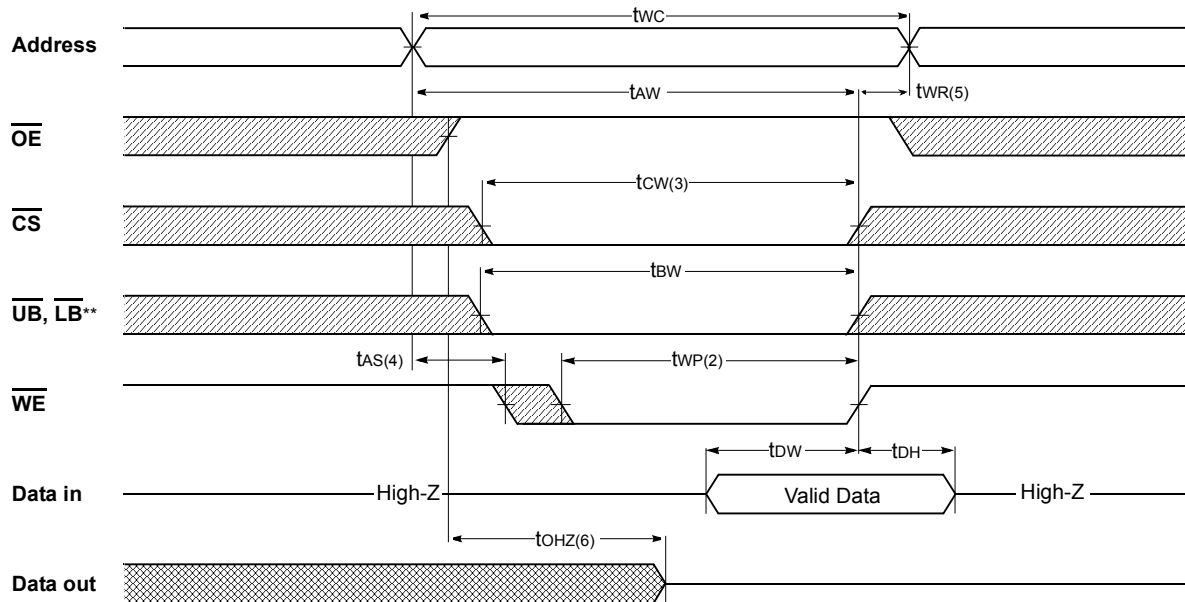


**NOTES(Read Cycle)**

1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device.
5. Transition is measured  $\pm 200\text{mV}$  from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CS}=V_{IL}$ .
7. Address valid prior to coincident with  $\overline{CS}$  transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

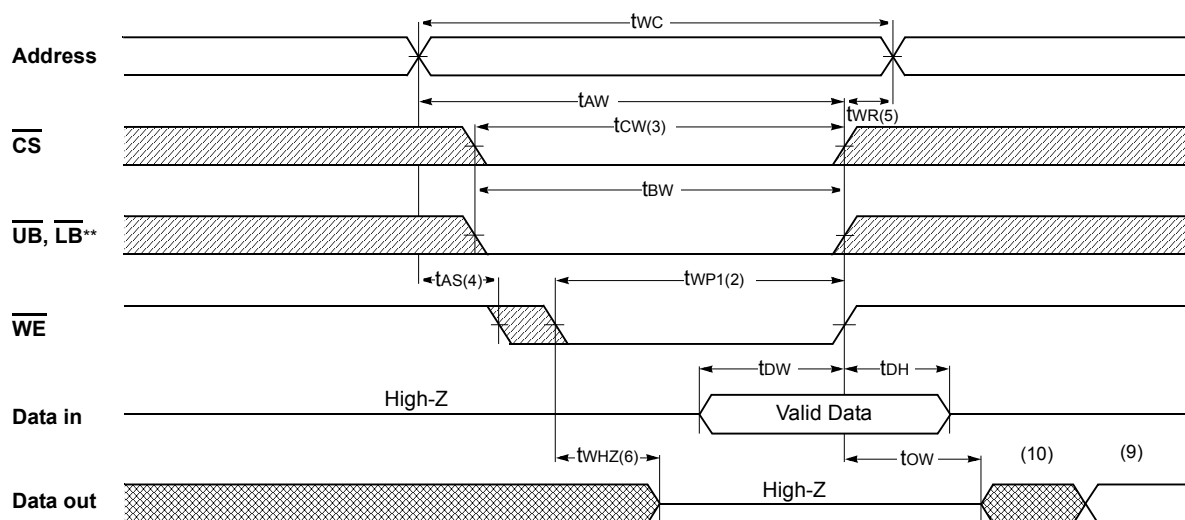
\*\* Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(1) ( $\overline{OE}$  Clock)



\*\* Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(2) ( $\overline{OE}$ =Low fixed)

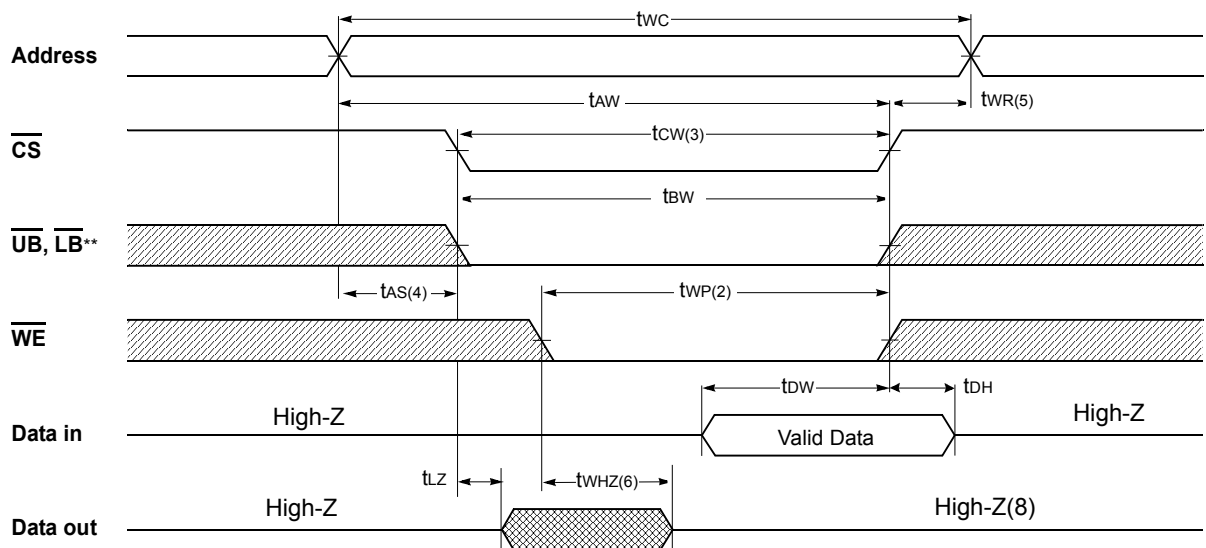


\*\* Those parameters are applied for x16 mode only.

**S6R1616V1M, S6R1616C1M, S6R1616W1M  
S6R1608V1M, S6R1608C1M, S6R1608W1M**

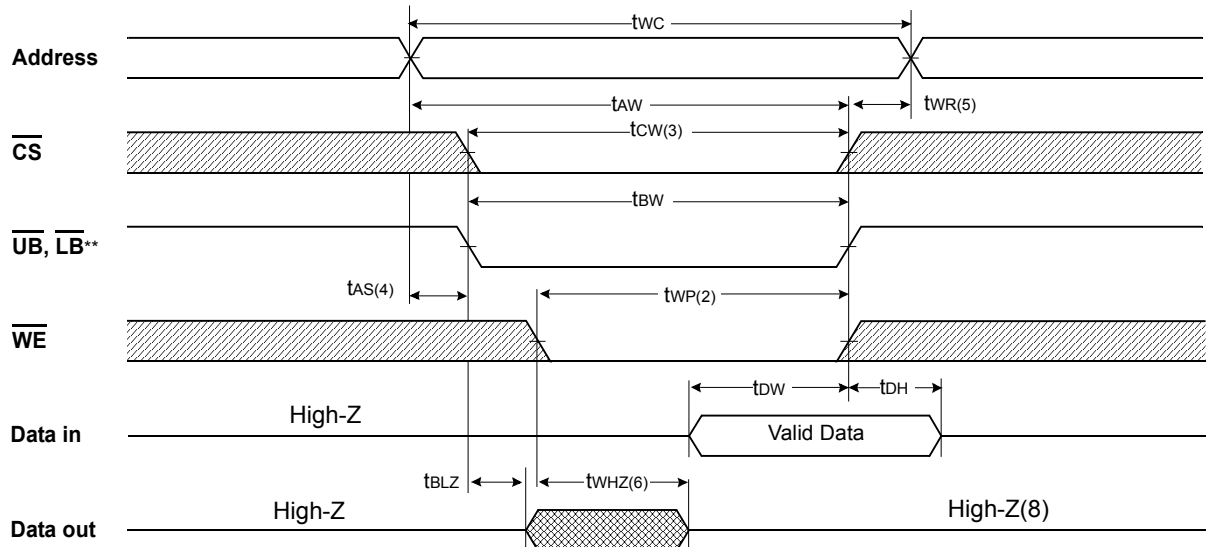
**16M Async FAST SRAM**

**Timing Waveform Of Write Cycle(3) ( $\overline{CS}$ =Controlled)**



\*\* Those parameters are applied for x16 mode only.

**Timing Waveform Of Write Cycle(4) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)**



**NOTES(Write Cycle)**

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low  $\overline{CS}$ ,  $\overline{WE}$ ,  $\overline{LB}$  and  $\overline{UB}$ . A write begins at the latest transition  $\overline{CS}$  going low and  $\overline{WE}$  going low ; A write ends at the earliest transition  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
3.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to end of write.
4.  $t_{AS}$  is measured from the address valid to the beginning of write.
5.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.
6. If  $\overline{OE}$ ,  $\overline{CS}$  and  $\overline{WE}$  are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If  $\overline{CS}$  goes low simultaneously with  $\overline{WE}$  going or after  $\overline{WE}$  going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When  $\overline{CS}$  is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

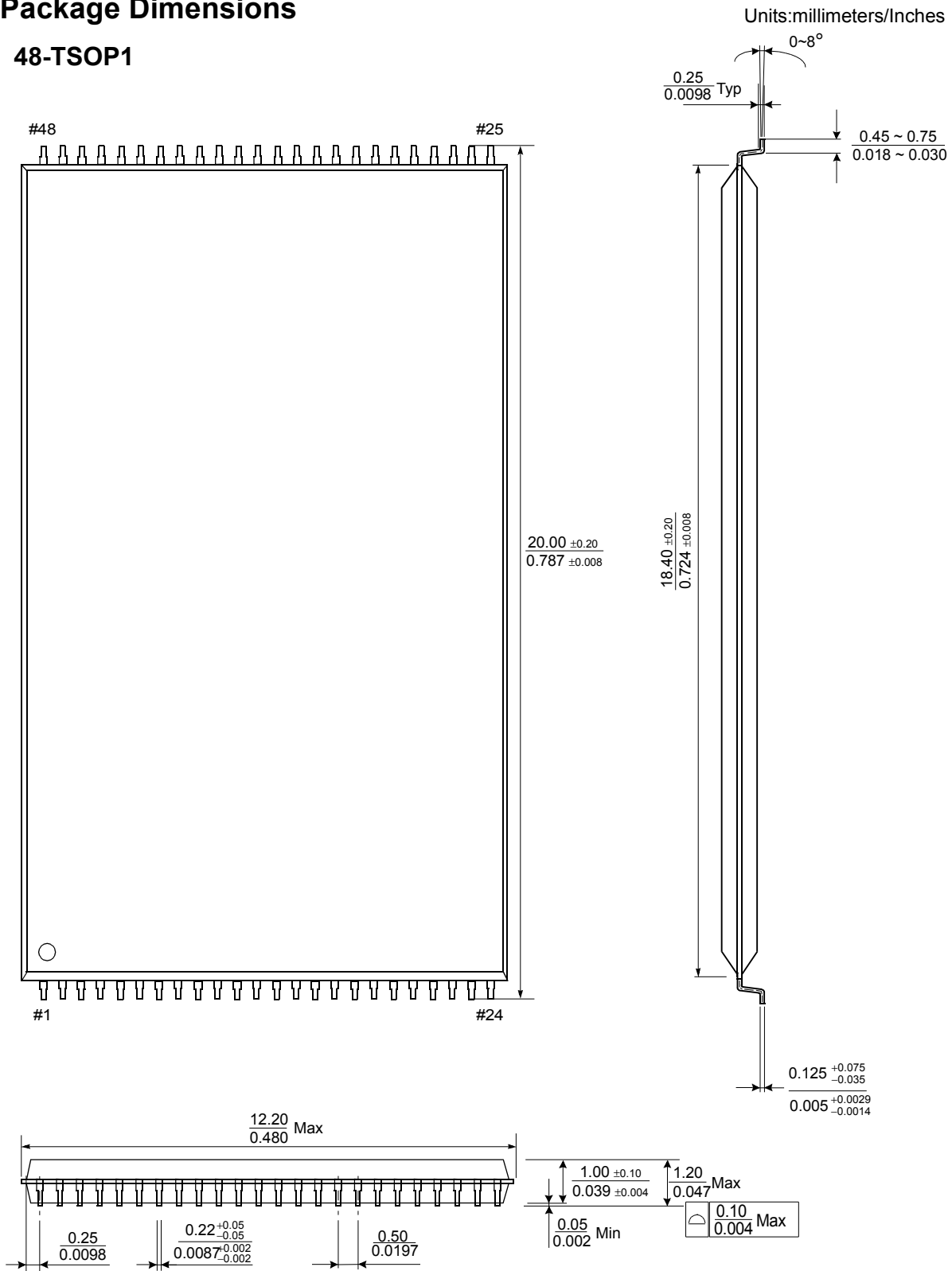
\*\* Those parameters are applied for x16 mode only.

S6R1616V1M, S6R1616C1M, S6R1616W1M  
 S6R1608V1M, S6R1608C1M, S6R1608W1M

16M Async FAST SRAM

Package Dimensions

48-TSOP1



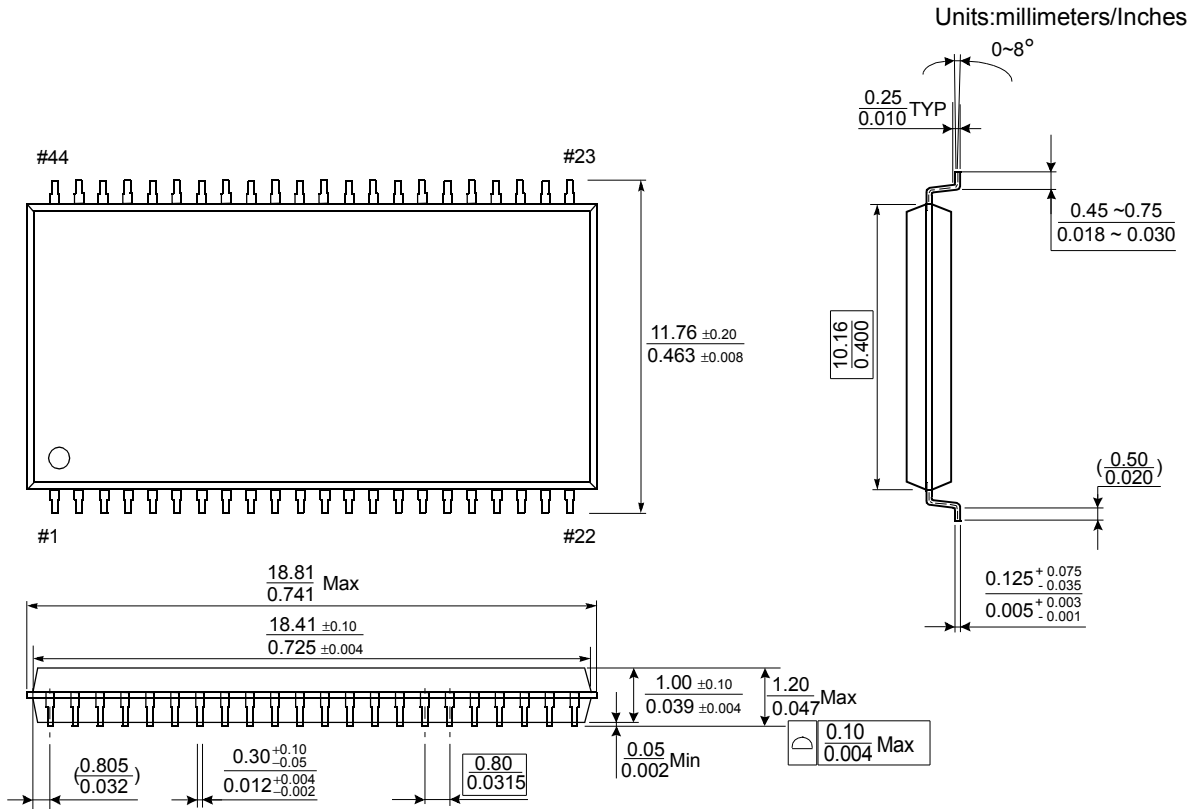


**S6R1616V1M, S6R1616C1M, S6R1616W1M  
S6R1608V1M, S6R1608C1M, S6R1608W1M**

**16M Async FAST SRAM**

**Package Dimensions**

**44-TSOP2-400BF**



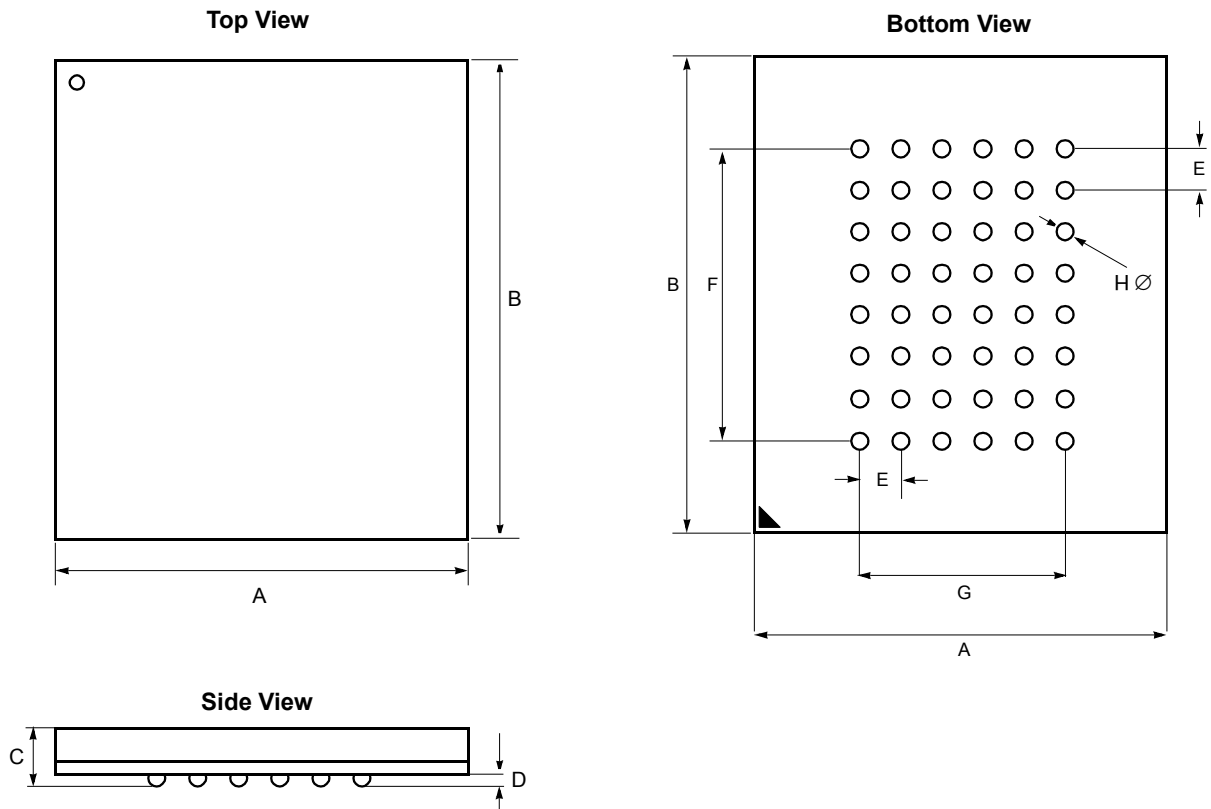
**S6R1616V1M, S6R1616C1M, S6R1616W1M  
S6R1608V1M, S6R1608C1M, S6R1608W1M**

**16M Async FAST SRAM**

**Package Dimensions**

**48-FBGA**

6mm x 8mm Body, 0.75mm Bump Pitch, 6 x 8 Ball Grid Array



Symbol	Value	Units	Note	Symbol	Value	Units	Note
<b>A</b>	6 ± 0.1	mm		<b>E</b>	0.75	mm	
<b>B</b>	8 ± 0.1	mm		<b>F</b>	5.25	mm	
<b>C</b>	1.1 ± 0.1	mm		<b>G</b>	3.75	mm	
<b>D</b>	0.25 ± 0.05	mm		<b>H</b>	0.35 ± 0.05	mm	