S70FL01GS

1 Gbit (128 Mbyte) 3.0V SPI Flash

Features

- CMOS 3.0V Core
- Serial Peripheral Interface (SPI) with Multi-I/O
  - SPI Clock polarity and phase modes 0 and 3
  - Double Data Rate (DDR) option
  - Extended Addressing: 32-bit address
  - Serial Command set and footprint compatible with S25FL-A, S25FL-K, and S25FL-P SPI families
  - Multi I/O Command set and footprint compatible with S25FL-P SPI family
- READ Commands
  - Normal, Fast, Dual, Quad, Fast DDR, Dual DDR, Quad DDR
  - AutoBoot – power up or reset and execute a Normal or Quad read command automatically at a preselected address
  - Common Flash Interface (CFI) data for configuration information
- Programming (1.5 Mbytes/s)
  - 512-byte Page Programming buffer
  - Quad-Input Page Programming (QPP) for slow clock systems
- Erase (0.5 Mbytes/s)
  - Uniform 256-kbyte sectors
- Cycling Endurance
  - 100,000 Program-Erase Cycles, minimum
- Data Retention
  - 20 Year Data Retention, minimum

Security Features

- One Time Program (OTP) array of 2048 bytes
- Block Protection
  - Status Register bits to control protection against program or erase of a contiguous range of sectors.
  - Hardware and software control options
  - Advanced Sector Protection (ASP)
  - Individual sector protection controlled by boot code or password
- Cypress® 65 nm MirrorBit® Technology with Eclipse™ Architecture
- Core Supply Voltage: 2.7V to 3.6V
- I/O Supply Voltage: 1.65V to 3.6V
- Temperature Range / Grade:
  - Industrial (–40 °C to +85 °C)
  - Industrial Plus (–40 °C to +105 °C)
  - Automotive, AEC-Q100 Grade 3 (–40 °C to +85 °C)
  - Automotive, AEC-Q100 Grade 2 (–40 °C to +105 °C)
  - Automotive, AEC-Q100 Grade 1 (–40 °C to +125 °C)
- Packages (all Pb-free)
  - 16-lead SOIC (300 mils)
  - BGA-24, 8 × 6 mm
    - 5 × 5 ball (ZSA024) footprint

General Description

This document contains information for the S70FL01GS device, which is a dual die stack of two S25FL512S die. For detailed specifications, refer to the discrete die datasheet provided in the Affected Documents/Related Documents table.

Affected Documents/Related Documents

Document Title	Publication Number
S25FL512S 512 Mbit (64 Mbyte) 3.0V SPI Flash Memory Datasheet	001-98284

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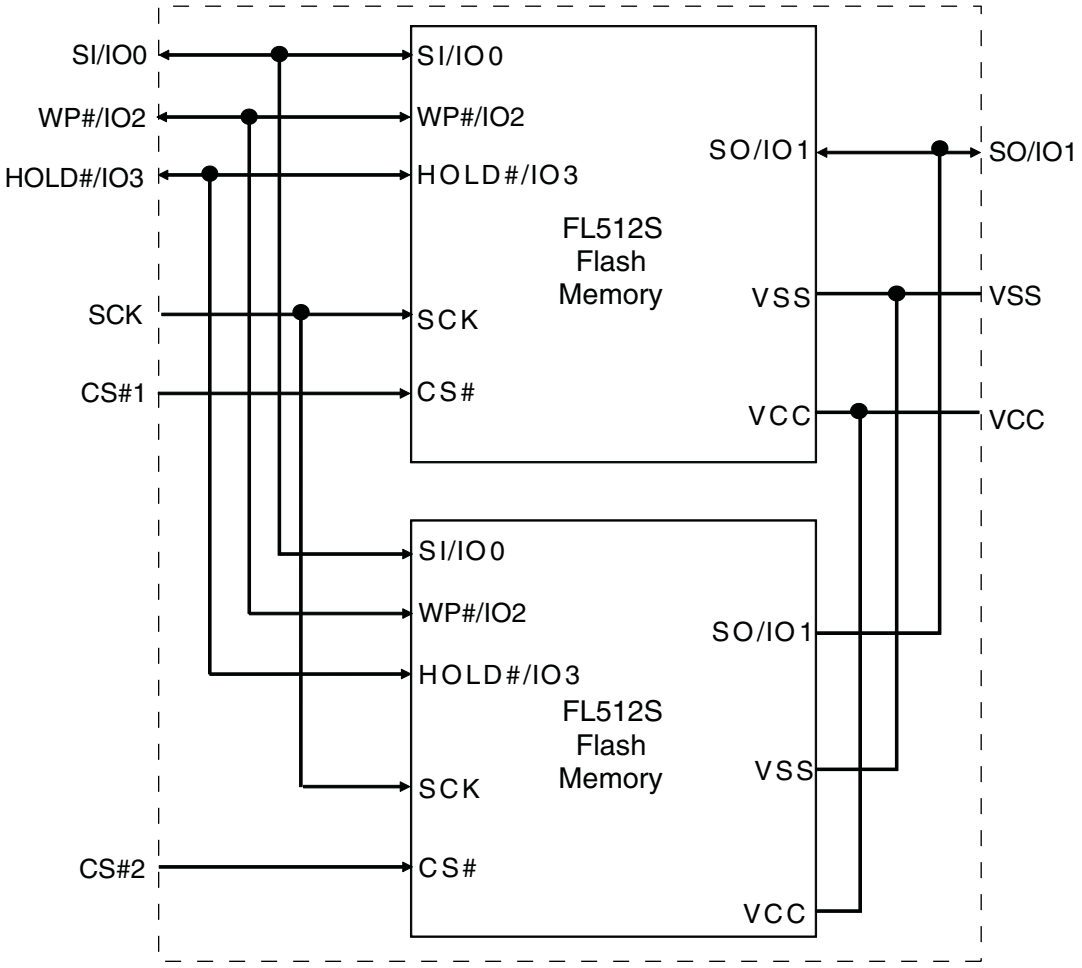
1. Block Diagram



2. Connection Diagrams

Figure 1. 16-Pin Plastic Small Outline Package (SO)

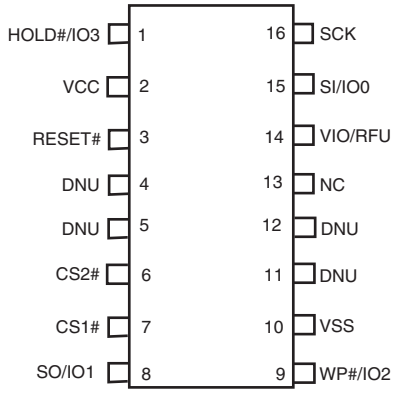
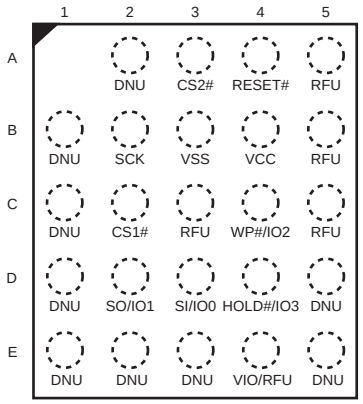


Figure 2. 24-Ball BGA, 5 x 5 Ball Footprint (ZSA024), Top View



Note:

1. V_{IO} is not supported in the S70FL01GS device and is RFU. Refer to Section 7. for more details.

3. Input/Output Summary

Table 2. Signal List

Signal Name	Type	Description
RESET#	Input	**Hardware Reset:** Low = device resets and returns to standby state, ready to receive a command. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used.
SCK	Input	**Serial Clock.**
CS1#	Input	**Chip Select.** FL512S #1.
CS2#	Input	**Chip Select.** FL512S #2.
SI / IO0	I/O	**Serial Input** for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2	I/O	**Write Protect** when not in Quad mode. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
HOLD# / IO3	I/O	**Hold** (pause) serial transfer in single bit or Dual data commands. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
V_{CC}	Supply	**Core Power Supply.**
V_{IO}	Supply	**Versatile I/O Power Supply. Note:** V_{IO} is not supported in the S70FL01GS device. Refer to Section 7. for more details.
V_{SS}	Supply	**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{CC}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

4. Device Operations

4.1 Programming

Each Flash die must be programmed independently due to the nature of the dual die stack.

4.2 Simultaneous Die Operation

The user may only access one Flash die of the dual die stack at a time via its respective Chip Select.

4.3 Sequential Reads

Sequential reads are not supported across the end of the first Flash die to the beginning of the second. If the user desires to sequentially read across the two die, data must be read out of the first die via CS1# and then read out of the second die via CS2#.

4.4 Sector/Bulk Erase

A sector erase command must be issued for sectors in each Flash die separately. Full device Bulk Erase via a single command is not supported due to the nature of the dual die stack. A Bulk Erase command must be issued for each die.

4.5 Status Registers

Each Flash die of the dual die stack is managed by its own Status Registers. Reads and updates to the Status Registers must be managed separately. It is recommended that Status Register control bit settings of each die are kept identical to maintain consistency when switching between die.

4.6 Configuration Register

Each Flash die of the dual die stack is managed by its own Configuration Register. Updates to the Configuration Register control bits must be managed separately. It is recommended that Configuration Register control bit settings of each die are kept identical to maintain consistency when switching between die.

4.7 Bank Address Register

It is recommended that the Bank Address Register bit settings of each die are kept identical to maintain consistency when switching between die.

4.8 Security and DDR Registers

It is recommended that the bit settings for ASP Register, Password Register, PPB Lock Register, PPB Access Register, DYB Access Register, and DDR Data Learning Register in each die are kept identical to maintain consistency when switching between die.

4.9 Block Protection

Each Flash die of the dual die stack will maintain its own Block Protection. Updates to the TBPROT and BPNV bits of each die must be managed separately. By default, each die is configured to be protected starting at the top (highest address) of each array, but no address range is protected. It is recommended that the Block Protection settings of each die are kept identical to maintain consistency when switching between die. In addition, any update to the FREEZE bit must be managed separately for each die. If the FREEZE bit is set to a logic 1, it cannot be cleared to a logic 0 until a power-on-reset is executed on each die that has the FREEZE bit set to 1.

5. Read Identification (RDID)

The Read Identification (RDID) command outputs the one-byte manufacturer identification, followed by the two-byte device identification and the bytes for the Common Flash Interface (CFI) tables. Each die of the FL01GS dual die stack will have identical identification data as the FL512S die, with the exception of the CFI data at byte 27h, as shown in Table 3.

Table 3. Product Group CFI Device Geometry Definition

Byte	Data	Description
27h	1Bh	Device Size = 2^N byte

6. RESET#

Note that the hardware RESET# input (pin 3 on the 16-pin SO package and ball A4 on the 5x5 BGA package) is bonded out and active for the S70FL01GS device. For applications that do NOT require use of the RESET# pin, it is recommended to not use RESET# for PCB routing channels that would cause the RESET# signal to be asserted Low (V_{IL}). Doing so will cause the device to reset to standby state. The RESET# signal has an internal pull-up resistor and may be left unconnected in the host system if not used.

7. Versatile I/O Power Supply (V_{IO})

Note that the Versatile I/O (V_{IO}) power supply (pin 14 on the 16-pin SO package and ball E4 on the 5x5 BGA package) is not supported, and pin 14 and ball E4 are RFU (Reserved for Future Use) in the standard configuration of the S70FL01GS device. Contact your local sales office to confirm availability with the V_{IO} feature enabled.

8. DC Characteristics

This section summarizes the DC Characteristics of the device.

Table 4. DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{IL}	Input Low Voltage	–	-0.5	–	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	–	0.7 x V_{CC}	–	V_{CC} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = V_{CC} min	–	–	0.15 x V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA	0.85 x V_{CC}	–		V
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}	–	–	±4	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}	–	–	±4	µA
I_{CC1}	Active Power Supply Current (READ)	Serial SDR @ 50 MHz Serial SDR @ 133 MHz Quad SDR @ 80 MHz Quad SDR @ 104 MHz Quad DDR @ 66 MHz Quad DDR @ 80 MHz Outputs unconnected during read data return (2)	–	–	18 36 50 61 75 90	mA
I_{CC2}	Active Power Supply Current (Page Program)	CS# = V_{CC}	–	–	100	mA
I_{CC3}	Active Power Supply Current (WRR)	CS# = V_{CC}	–	–	100	mA
I_{CC4}	Active Power Supply Current (SE)	CS# = V_{CC}	–	–	100	mA
I_{CC5}	Active Power Supply Current (BE) (3)	CS# = V_{CC}	–	–	200	mA
I_{SB} (Industrial)	Standby Current	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}, Industrial Temp	–	140	200	µA
I_{SB} (Industrial Plus)	Standby Current	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}, Industrial Plus Temp	–	140	600	µA

Notes:

1. *Typical values are at T_{AI} = 25°C and V_{CC} = 3V.*
2. *Output switching current is not included.*
3. *Bulk Erase current is for both die erasing simultaneously.*

9. AC Test Conditions

Figure 3. Input, Output, and Timing Reference Levels

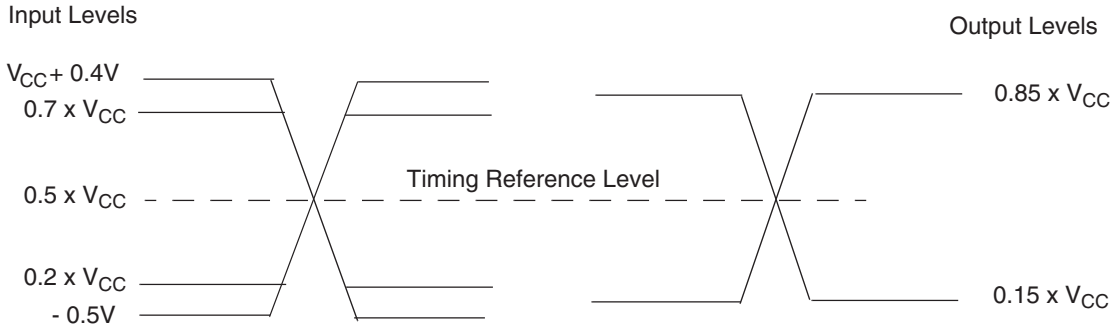


Figure 4. Test Setup

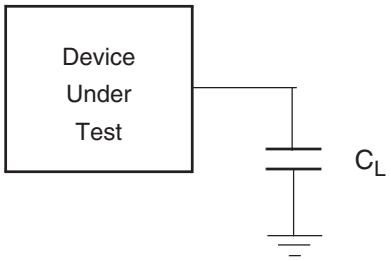


Table 5. AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30 15 (4)		pF
	Input Rise and Fall Times	–	2.4	ns
	Input Pulse Voltage	0.2 x V_{CC} to 0.8 V_{CC}		V
	Input Timing Ref Voltage	0.5 V_{CC}		V
	Output Timing Ref Voltage	0.5 V_{CC}		V

Notes:

1. *Output High-Z is defined as the point where data is no longer driven.*
2. *Input slew rate: 1.5 V/ns.*
3. *AC characteristics tables assume clock and data signals have the same slew rate (slope).*
4. *DDR Operation.*

10. SDR AC Characteristics

Table 6. SDR AC Characteristics (Single Die Package, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK Clock Frequency for READ and 4READ instructions	DC	–	50	MHz
$F_{SCK, C}$	SCK Clock Frequency for single commands (4)	DC	–	133	MHz
$F_{SCK, C}$	SCK Clock Frequency for the following dual and quad commands: DOR, 4DOR, QOR, 4QOR, DIOR, 4DIOR, QIOR, 4QIOR	DC	–	104	MHz
$F_{SCK, QPP}$	SCK Clock Frequency for the QPP, 4QPP commands	DC	–	80	MHz
P_{SCK}	SCK Clock Period	1/ F_{SCK}	–	∞	
t_{WH}, t_{CH}	Clock High Time (5)	45% P_{SCK}	–	–	ns
t_{WL}, t_{CL}	Clock Low Time (5)	45% P_{SCK}	–	–	ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1	–	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1	–	–	V/ns
t_{CS} (7)	CS# High Time (Read Instructions) CS# High Time (Program/Erase)	10 50	–	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3	–	–	ns
t_{SU}	Data in Setup Time	1.5	–	3000 (6)	ns
t_{HD}	Data in Hold Time	2	–	–	ns
t_V	Clock Low to Output Valid	–	–	8.0 (2) 7.65 (3) 6.5 (4)	ns
t_{HO}	Output Hold Time	2	–	–	ns
t_{DIS}	Output Disable Time	0	–	8	ns
t_{WPS}	WP# Setup Time	20 (1)	–	–	ns
t_{WPH}	WP# Hold Time	100 (1)	–	–	ns
t_{HLCH}	HOLD# Active Setup Time (relative to SCK)	3	–	–	ns
t_{CHHH}	HOLD# Active Hold Time (relative to SCK)	3	–	–	ns
t_{HHCH}	HOLD# Non-Active Setup Time (relative to SCK)	3	–	–	ns
t_{CHHL}	HOLD# Non-Active Hold Time (relative to SCK)	3	–	–	ns
t_{HZ}	HOLD# Enable to Output Invalid	–	–	8	ns
t_{LZ}	HOLD# Disable to Output Valid	–	–	8	ns

Notes:

1. *Only applicable as a constraint for WRR instruction when SRWD is set to a 1.*
2. *Full V_{CC} range (2.7 - 3.6V) and CL = 30 pF.*
3. *Regulated V_{CC} range (3.0 - 3.6V) and CL = 30 pF.*
4. *Regulated V_{CC} range (3.0 - 3.6V) and CL = 15 pF.*
5. *±10% duty cycle is supported for frequencies $\leq$ 50 MHz.*
6. *Maximum value only applies during Program/Erase Suspend/Resume commands.*
7. *When switching between die, a minimum time of t_{CS} must be kept between the rising edge of one chip select and the falling edge of the other for operations and data to be valid.*

10.1 DDR AC Characteristics

Table 7. DDR AC Characteristics 66 MHz and 80 MHz Operation

Symbol	Parameter	66 MHz			80 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
$F_{SCK, R}$	SCK Clock Frequency for DDR READ instruction	DC	–	66	DC	–	80	MHz
$P_{SCK, R}$	SCK Clock Period for DDR READ instruction	15	–	∞	12.5	–	∞	ns
t_{WH}, t_{CH}	Clock High Time	45% P_{SCK}	–	–	45% P_{SCK}	–	–	ns
t_{WL}, t_{CL}	Clock Low Time	45% P_{SCK}	–	–	45% P_{SCK}	–	–	ns
t_{CS}	CS# High Time (Read Instructions)	10	–	–	10	–	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	–	3	–	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3	–	–	3	–	–	ns
t_{SU}	IO in Setup Time	2	–	3000 (2)	1.5	–	3000 (2)	ns
t_{HD}	IO in Hold Time	2	–	–	1.5	–	–	ns
t_V	Clock Low to Output Valid	0	–	6.5 (1)	–	–	6.5 (1)	ns
t_{HO}	Output Hold Time	1.5	–	–	1.5	–	–	ns
t_{DIS}	Output Disable Time	–	–	8	–	–	8	ns
t_{LZ}	Clock to Output Low Impedance	0	–	8	0	–	8	ns
t_{IO_skew}	First IO to last IO data valid time	–	–	600	–	–	600	ps

Notes:

1. *Regulated V_{CC} range (3.0 - 3.6V) and CL =15 pF.*
2. *Maximum value only applies during Program/Erase Suspend/Resume commands.*

10.2 Capacitance Characteristics

Table 8. Capacitance

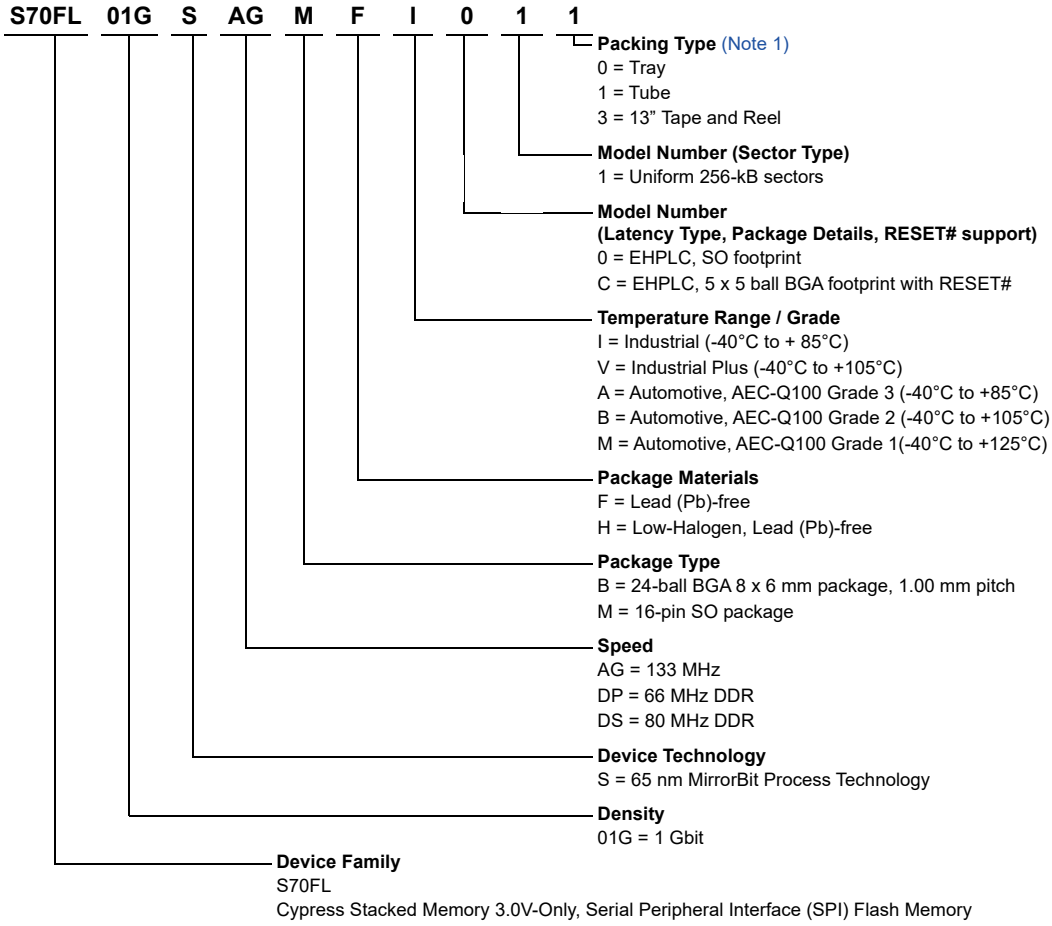
	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, CS#1, CS#2, RESET#)	1 MHz	–	16	pF
C_{OUT}	Output Capacitance (applies to All I/O)	1 MHz	–	16	pF

Note:

1. *For more information on capacitance, please consult the IBIS models.*

11. Ordering Information

The ordering part number is formed by a valid combination of the following:



Notes:

1. *EHPLC = Enhanced High Performance Latency Code table.*
2. *Uniform 256-kB sectors = All sectors are uniform 256-kB with a 512B programming buffer.*

11.1 Valid Combinations — Standard

Table 9 lists the valid combinations configurations planned to be supported in volume for this device.

Table 9. S70FL01GS Valid Combinations — Standard

S70FL01GS Valid Combinations					
Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking (1)
S70FL01GS	AG	MFI, MFV	01	0, 1, 3	FL01GS + A + (temp) + F + (Model Number)
	DP				FL01GS + D + (temp) + F + (Model Number)
	DS				FL01GS + S + (temp) + F + (Model Number)
	AG	BHI, BHV	C1	0, 3	FL01GS + A + (temp) + H + (Model Number)
	DP				FL01GS + D + (temp) + H + (Model Number)
	DS				FL01GS + S + (temp) + H + (Model Number)

Note:
1. Package Marking omits the leading “S70” and package type.

11.2 Valid Combinations — Automotive Grade / AEC-Q100

Table 10 lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 10. S70FL01GS Valid Combinations — Automotive Grade / AEC-Q100

S70FL01GS Valid Combinations					
Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking (1)
S70FL01GS	AG	MFA, MFB, MFM	01	0, 1, 3	FL01GS + A + (temp) + F + (Model Number)
	DS				FL01GS + S + (temp) + F + (Model Number)
	AG	BHA, BHB, BHM	C1	0, 3	FL01GS + A + (temp) + H + (Model Number)
	DS				FL01GS + S + (temp) + H + (Model Number)

Note:
1. Package Marking omits the leading “S70” and package type.

12. Other Resources

12.1 Cypress Flash Memory Roadmap

www.cypress.com/product-roadmaps/cypress-flash-memory-roadmap

12.2 Links to Software

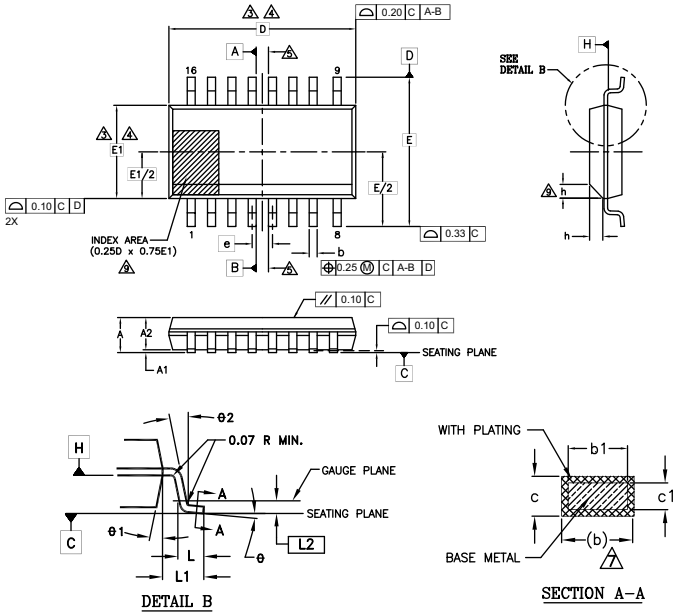
www.cypress.com/software-and-drivers-cypress-flash-memory

12.3 Links to Application Notes

www.cypress.com/appnotes

13. Physical Diagram

13.1 SOIC 16 Lead, 300-mil Body Width

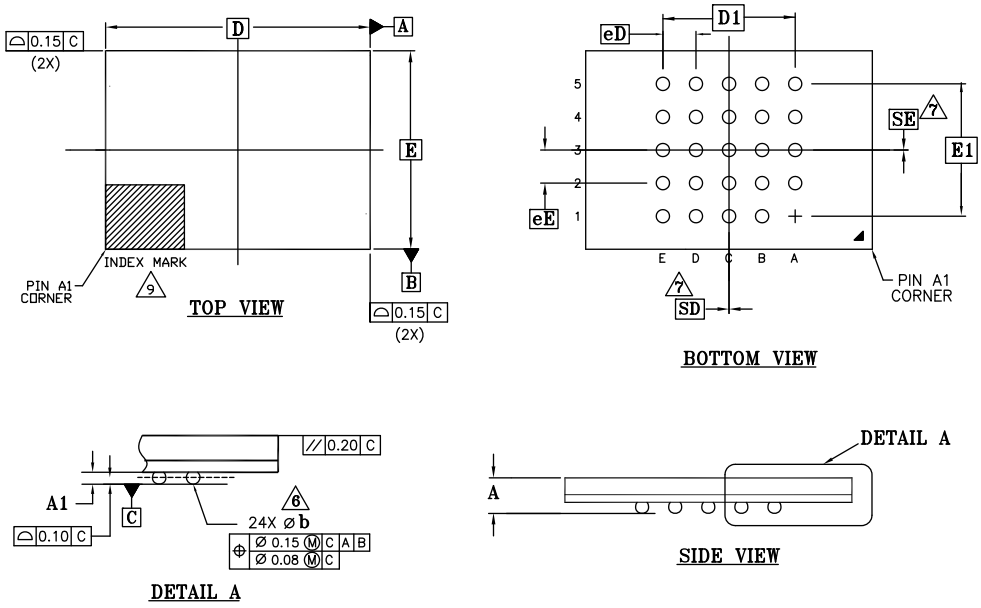


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

13.2 24-Ball BGA 8 x 6 mm (ZSA024)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
n		24	
Ø b	0.35	0.40	0.45
eD		1.00 BSC	
eE		1.00 BSC	
SD		0.00	
SE		0.00	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7 "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

14. Revision History

Document Title: S70FL01GS, 1 Gbit (128 Mbyte) 3.0V SPI Flash Document Number: 001-98295				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	BWHA	11/06/2012	Initial release
*A	–	BWHA	04/25/2013	Global: Datasheet designation updated from Advance Information to Preliminary DC Characteristics: DC Characteristics table: changed Max value of ILI, ILO, ICC1, and ISB
*B	–	BWHA	05/16/2013	SOIC 16 Physical Diagram: Updated package nomenclature from S03016 to SL3016
*C	–	BWHA	08/22/2013	Valid Combinations: Valid Combinations table: added MFV DC Characteristics: DC Characteristics table: added ISB (Automotive)
*D	–	BWHA	11/08/2013	Global: Datasheet designation updated from Preliminary to Full Production
*E	–	BWHA	03/19/2014	Features: Packages (all Pb-free): added BGA-24, 8 x 6 mm Connections Diagrams: Added figure: 24-Ball BGA, 5 x 5 Ball Footprint (FAB024), Top View Ordering Information: Added options to: Model Number, Package Materials, Package Type, and Speed Valid Combinations: Added option to S70FL01GS Valid Combinations Table SDR AC Characteristics: SDR AC Characteristics (Single Die Package, VCC = 2.7V to 3.6V) table: updated tv Min DDR AC Characteristics:Updated DDR AC Characteristics 66 MHz Operation table Capacitance Characteristics: Capacitance table: updated Max values and removed note
*F	–	BWHA	11/07/2014	Valid Combinations: Added DP Speed Option for BGA 5x5 package
*G	–	BWHA	04/21/2015	Valid Combinations: Added BHV option
*H	4871631	BWHA	08/24/2015	Updated to Cypress template. Changed Automotive Temperature Range to Industrial Plus Temperature Range in Features and Section 4.
*I	5123878	BWHA	02/03/2016	Updated General Description.
*J	5536564	BWHA	12/02/2016	Updated Features on page 1: Added Extended and Automotive Grade temperatures. Updated DDR AC Characteristics 66 MHz and 80 MHz Operation on page 11 table: Corrected t_{HO} Min value, t_{CSH} and t_{SU} Max value. Ordering Information on page 12: Added Extended and Automotive Grade. Added Other Resources on page 14.
*K	5612027	ECAO	01/17/2017	Added I_{CC1} value for Quad DDR @ 80 MHz in Table 4, DC Characteristics on page 8 Updated I_{CC5} value in Table 4, DC Characteristics on page 8 Updated DDR AC Characteristics 66 MHz and 80 MHz Operation on page 11 Removed Extended (-40°C to +125°C) temperature option in Ordering Information Updated Physical Diagram: Updated package name and drawing from SL3016 to SS3016. Updated package name and drawing from FAB024 to ZSA024.

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	5669602	ECAO	04/05/2017	Updated Figure 2, 24-Ball BGA, 5 x 5 Ball Footprint (ZSA024), Top View on page 4. Removed SS3016 from Section 13.1, SOIC 16 Lead, 300-mil Body Width on page 15. Removed CS# from Table 2, Signal List on page 5. Updated t_{SU} in Table 6, SDR AC Characteristics (Single Die Package, V_{CC} = 2.7V to 3.6V) on page 10. Updated Cypress logo. Updated Sales page.
*M	5783913	ECAO	06/23/2017	Changed OTP total space in Security Features. Updated I_{SB} values in Table 4.
*N	6104454	BWHA	03/21/2018	Table 6: Removed Typ value for t_{che} and updated t_{su} value as “3000”.

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