

General Description

The Cypress S70GL02GT 2-Gigabit MirrorBit® Flash memory device is fabricated on 45-nm MirrorBit® Eclipse™ process technology. This device offers a fast page access time of 25 ns with a corresponding random access time of 110 ns. It features a Write Buffer that allows a maximum of 256 words/512 bytes to be programmed in one operation, resulting in faster effective programming time than standard single byte/word programming algorithms. This makes the device an ideal product for today's embedded applications that require higher density, better performance and lower power consumption.

This document contains information for the S70GL02GT device, which is a dual-die stack of two S29GL01GT die. For detailed specifications, please refer to the discrete die data sheet:

| Document | Cypress Document Number |
|---------------------------------|-------------------------|
| S29GL01GT, S29GL512T Data Sheet | 002-00247 |

Distinctive Characteristics

- CMOS 3.0 Volt Core with Versatile I/O™
- Two 1024 Megabit (S29GL01GT) in a single 64-ball Fortified-BGA package (see [S29GL01GT datasheet for full specifications](#))
- 45 nm MirrorBit Eclipse process technology
- Single supply (V_{CC}) for read / program / erase (2.7V to 3.6V)
- Versatile I/O Feature
 - Wide I/O voltage (V_{IO}): 1.65V to V_{CC}
- x8 and x16 data bus
- 16-word/32-byte page read buffer
- 512-byte Programming Buffer
 - Programming in Page multiples, up to a maximum of 512 bytes
- Sector Erase
 - Uniform 128-kbytes sectors
 - S70GL02GT: two thousand forty-eight sectors
- Suspend and Resume commands for Program and Erase operations
- Status Register, Data Polling, and Ready/Busy pin methods to determine device status
- Advanced Sector Protection (ASP)
 - Volatile and non-volatile protection methods for each sector
- Separate 1024-byte One Time Program (OTP) array with two lockable regions
 - Available in each device Support for CFI (Common Flash Interface)
- WP# input
 - Protects the last sector of the device, regardless of sector protection settings
- Temperature Range / Grade
 - Industrial (–40°C to +85°C)
 - Industrial Plus (–40°C to +105°C)
 - Automotive, AEC-Q100 Grade 3 (–40°C to +85°C)
 - Automotive, AEC-Q100 Grade 2 (–40°C to +105°C)
- 100,000 Program-Erase cycles
- 20-year data retention
- Packaging Options
 - 64-ball LSH Fortified BGA, 13 mm x 11 mm

Performance Characteristics

| Parameter | Max. Read Access Times (ns) (Note 1) | |
|----------------------------------|--------------------------------------|-----|
| | 2 Gb | |
| Random Access Time (t_{ACC}) | 110 | 120 |
| Page Access Time (t_{PACC}) | 20 | 30 |
| CE# Access Time (t_{CE}) | 110 | 120 |
| OE# Access Time (t_{OE}) | 25 | 35 |

Notes

1. Access times are dependent on V_{IO} operating ranges. See Ordering Information on page 4 for further details.
2. Contact a sales representative for availability.

| Typical Program and Erase Rates | | |
|--|-----------------------|------------------------|
| Operation | -40°C to +85°C | -40°C to +105°C |
| Buffer Programming (512 bytes) | 1.114 MB/s | 1.14 MB/s |
| Sector Erase (128 kbytes) | 245 kB/s | 245 kB/s |

| Maximum Current Consumption | | |
|------------------------------------|-----------------------|------------------------|
| Operation | -40°C to +85°C | -40°C to +105°C |
| Active Read at 5 MHz, 30 pF | 60 mA | 60 mA |
| Program | 100 mA | 100 mA |
| Erase | 100 mA | 100 mA |
| Standby | 200 μ A | 400 μ A |

Contents

| | | | |
|--|----|--|----|
| 1. Ordering Information | 4 | 9. Data Integrity | 12 |
| 1.1 Recommended Combinations..... | 4 | 9.1 Erase Endurance | 12 |
| 2. Input/Output Descriptions and Logic Symbol | 5 | 9.2 Data Retention..... | 12 |
| 3. Block Diagram | 6 | 10. Device ID and Common Flash Interface (ID-CFI) ASO Map | 13 |
| 3.1 Special Handling Instructions for BGA Package..... | 7 | 11. Other Resources | 18 |
| 3.2 LSH064 — 64 ball Fortified Ball Grid Array, 13 x 11 mm | 8 | 11.1 Cypress Flash Memory Roadmap | 18 |
| 4. Memory Map | 9 | 11.2 Links to Software | 18 |
| 5. Autoselect | 9 | 11.3 Links to Application Notes..... | 18 |
| 6. DC Characteristics | 10 | 12. Revision History | 19 |
| 7. BGA Package Capacitance | 12 | Sales, Solutions, and Legal Information | 20 |
| 8. Thermal Resistance | 12 | Worldwide Sales and Design Support | 20 |
| | | Products | 20 |
| | | PSoC® Solutions | 20 |
| | | Cypress Developer Community | 20 |
| | | Technical Support | 20 |

1. Ordering Information

1.1 Recommended Combinations

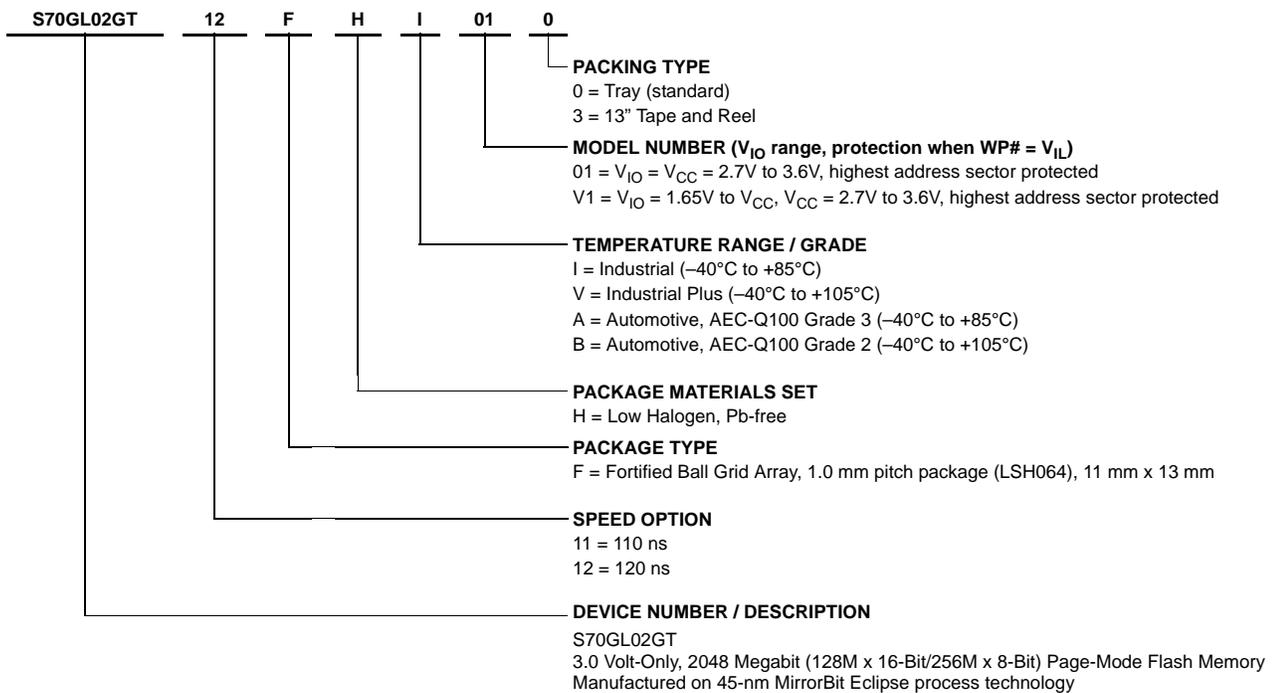
Recommended Combinations table below list various configurations planned to be available in volume. The table below will be updated as new combinations are released. Check with your local sales representative to confirm availability of specific configuration not listed or to check on newly released combinations.

| S29GL-T Valid Combinations | | | | | |
|----------------------------|------------|--------------------------------|--------------|------------------|--|
| Base OPN | Speed (ns) | Package and Temperature | Model Number | Packing Type | Ordering Part Number (yy = Model Number, x = Packing Type) |
| S70GL02GT | 110 | FHI, FHV, FHA, FHB (Note 1) | 01 | 0, 3 (Note 2) | S70GL02GT11FHI01x S70GL02GT11FHV01x S70GL02GT11FHA01x S70GL02GT11FHB01x |
| | 120 | | V1 | | S70GL02GT12FHIV1x S70GL02GT12FHVV1x S70GL02GT12FHAV1x S70GL02GT12FHBV1x |

Notes

- BGA package marking omits leading "S70" and packing type designator from ordering part number.
- Packing Type "0" is standard option.

The ordering part number is formed by a valid combination of the following:



2. Input/Output Descriptions and Logic Symbol

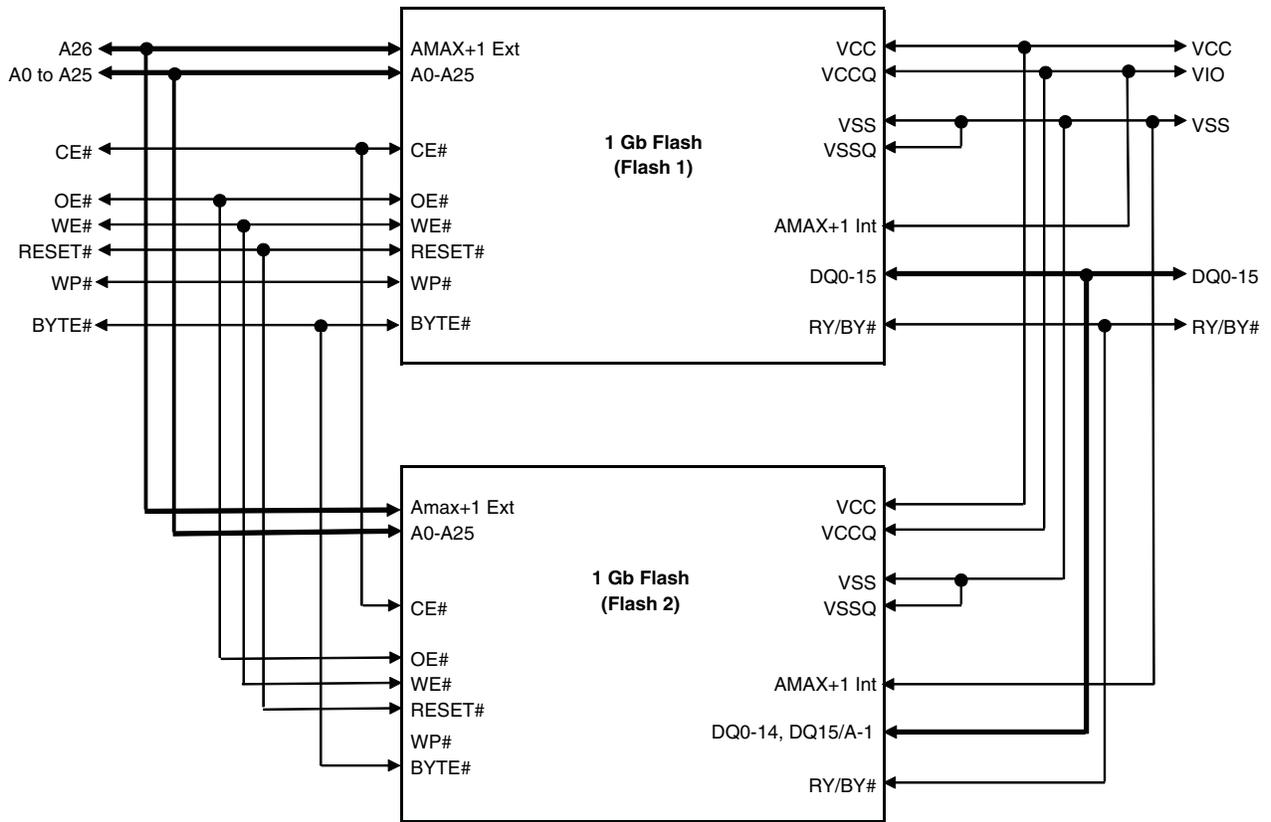
Table 2.1 identifies the input and output package connections provided on the device.

Table 2.1 Input/Output Descriptions

| Symbol | Type | Description |
|----------|---------------------|--|
| DQ14–DQ0 | I/O | Data inputs and outputs. |
| DQ15/A-1 | Input/Output | DQ15: Data inputs and outputs. A-1: LSB address input in byte mode. |
| CE# | Input | Chip Enable. At V_{IL} , selects the device for data transfer with the host memory controller. |
| OE# | Input | Output Enable. At V_{IL} , causes outputs to be actively driven. At V_{IH} , causes outputs to be high impedance (High-Z). |
| WE# | Input | Write Enable. At V_{IL} , indicates data transfer from host to device. At V_{IH} , indicates data transfer is from device to host. |
| A26-A0 | Input | Address lines for S29GL02GT. |
| V_{CC} | Supply | Core power supply. |
| V_{IO} | Supply | Versatile IO power supply. |
| V_{SS} | Supply | Power supplies ground. |
| RY/BY# | Output — open drain | Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL} , the device is actively engaged in an Embedded Algorithm such as erasing or programming. At High-Z, the device is ready for read or a new command write — requires external pull-up resistor to detect the High-Z state. Multiple devices may have their RY/BY# outputs tied together to detect when all devices are ready. |
| BYTE# | Input | Selects data bus width. At V_{IL} , the device is in byte configuration and data I/O pins DQ7–DQ0 are active and DQ15/A-1 becomes the LSB address input. At V_{IH} , the device is in word configuration and data I/O pins DQ15–DQ0 are active. |
| RESET# | Input | Hardware Reset. At V_{IL} , causes the device to reset control logic to its standby state, ready for reading array data. |
| WP# | Input | Write Protect. At V_{IL} , disables program and erase functions in the highest address 64-kword (128-kB) sector of the device. At V_{IH} , the sector is not protected. WP# has an internal pull up; When unconnected WP# is at V_{IH} . |
| NC | No Connect | Not Connected internally. The pin/ball location may be used in Printed Circuit Board (PCB) as part of a routing channel. |
| DNU | Reserved | Do Not Use. Reserved for use by Cypress. The pin/ball is connected internally. The input has an internal pull down resistance to V_{SS} . The pin/ball can be left open or tied to V_{SS} on the PCB. |
| RFU | No Connect | Reserved for Future Use. Not currently connected internally but the pin/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The pin/ball may be used by a signal in the future. |

3. Block Diagram

Figure 3.1 Block Diagram for 2 x GL01GT (Highest Address Sector Protected)



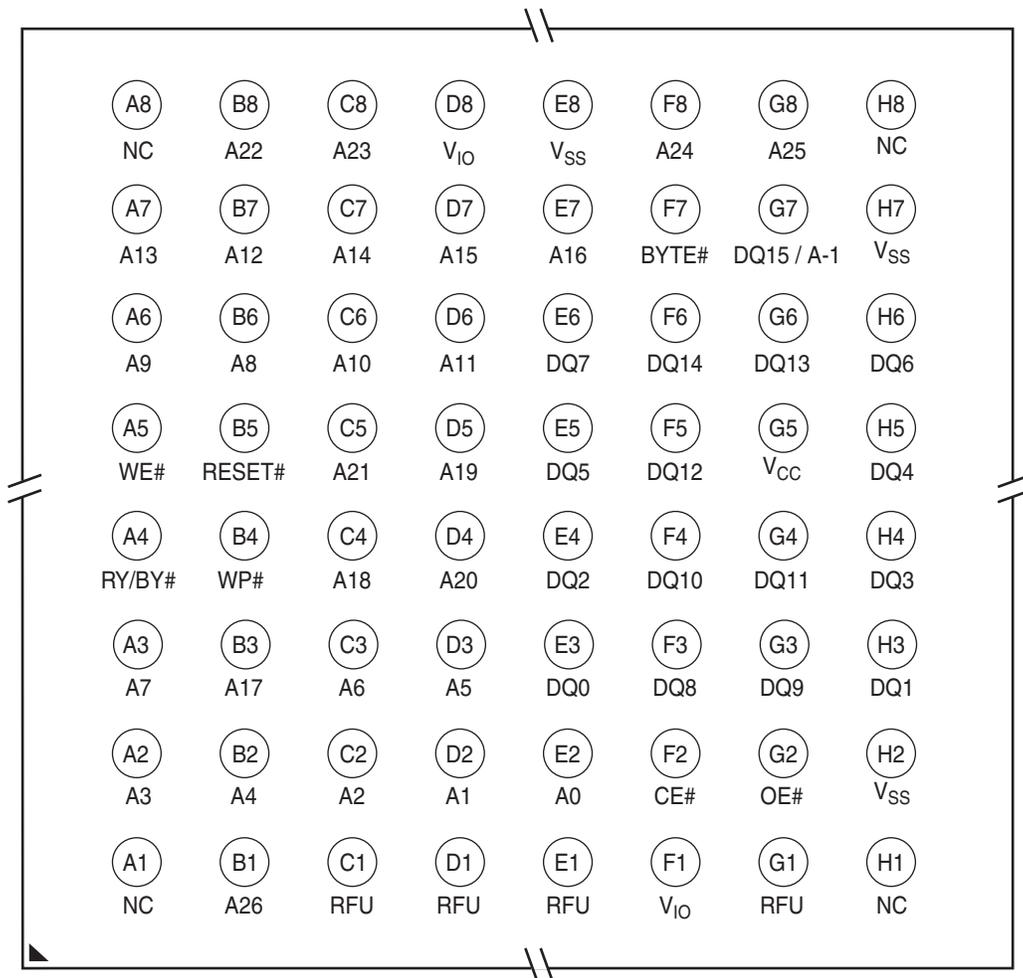
3.1 Special Handling Instructions for BGA Package

Special handling is required for Flash Memory products in BGA packages.

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Figure 3.2 64-ball Fortified Ball Grid Array

64-ball Fortified BGA
Top View, Balls Facing Down

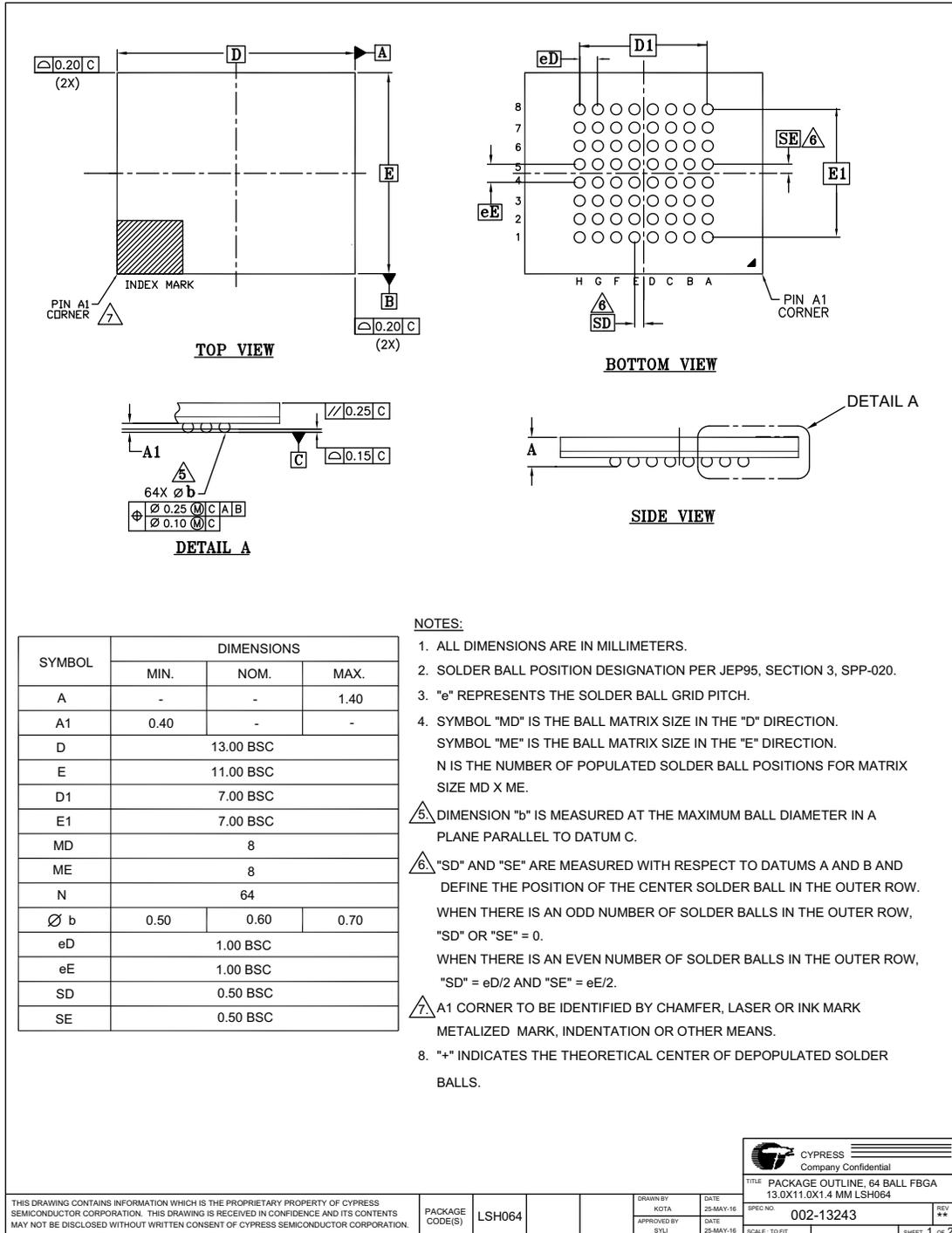


Notes

1. Ball E1, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to V_{CC} or V_{SS} through a series resistor.
2. Balls C1, D1, E1, G1: Reserved for Future Use (RFU).
3. Balls A1, A8, H1, H8: No Connect (NC).

3.2 LSH064 — 64 ball Fortified Ball Grid Array, 13 x 11 mm

Figure 3.3 LSH064—64-ball Fortified Ball Grid Array (FBGA), 13 x 11 mm



4. Memory Map

The S70GL02GT consist of uniform 64 kword (128-kbyte) sectors organized as shown in [Table 4.1](#).

Table 4.1 S70GL02GT Sector and Memory Address Map

| Uniform Sector Size | Sector Count | Sector Range | Address Range (16-bit) | Notes |
|---------------------|--------------|--------------|------------------------|-------------------------|
| 64 kword/128 kB | 2048 | SA00 | 0000000h–000FFFFh | Sector Starting Address |
| | | : | : | |
| | | SA2047 | 7FF0000H–7FFFFFFFh | Sector Ending Address |

Note

This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA001-SA2046) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 kB sectors have the pattern xxx0000h-xxxFFFFh.

5. Autoselect

[Table 5.1](#) provides the device identification codes for the S70GL02GT. For more information on the autoselect function, refer to the S29GL01GT, S29GL512T data sheet (publication number 002-00247).

Table 5.1 Autoselect Addresses in System

| Description | Address | Read Data (word/byte mode) |
|-----------------------|--------------|---|
| Manufacturer ID | (Base) + 00h | 0001h |
| Device ID, Word 1 | (Base) + 01h | 227Eh |
| Device ID, Word 2 | (Base) + 0Eh | 2248h |
| Device ID, Word 3 | (Base) + 0Fh | 2201h |
| Secure Device Verify | (Base) + 03h | For S70GL02GT highest address sector protect: XX3Fh = Not Factory Locked XXBFh = Factory Locked |
| Sector Protect Verify | (SA) + 02h | xx01h/01h = Locked, xx00h/00h = Unlocked |

6. DC Characteristics

Table 6.1 DC Characteristics (–40°C to +85°C)

| Parameter | Description | Test Conditions | | Min | Typ (Note 2) | Max | Unit |
|------------------|--|---|------------|-----|-----------------|------|------|
| I _{LI} | Input Load Current | V _{IN} = V _{SS} to V _{CC} , V _{CC} = V _{CC} max | All Others | | ±0.04 | ±2.0 | μA |
| | | | WP#, BYTE# | | ±1.0 | ±4.0 | |
| I _{LO} | Output Leakage Current | V _{OUT} = V _{SS} to V _{CC} , V _{CC} = V _{CC} max | | | ±0.04 | ±2.0 | μA |
| I _{CC4} | VCC Standby Current | CE#, RESET#, OE# = V _{IH} , V _{IH} = V _{IO} V _{IL} = V _{SS} , V _{CC} = V _{CC} max | | | 140 | 200 | μA |
| I _{CC5} | VCC Reset Current (Notes 2, 7) | CE# = V _{IH} , RESET# = V _{IL} , V _{CC} = V _{CC} max | | | 20 | 40 | mA |
| I _{CC6} | Automatic Sleep Mode (3) | V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC} max, t _{ACC} + 30 ns | | | 6 | 12 | mA |
| | | V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC} max, t _{ASSB} | | | 200 | 300 | μA |
| I _{CC7} | VCC Current during power up (Notes 2, 6) | RESET# = V _{IO} , CE# = V _{IO} , OE# = V _{IO} , V _{CC} = V _{CC} max, | | | 106 | 160 | mA |

Notes

- I_{CC} active while Embedded Algorithm is in progress.
- Not 100% tested.
- Automatic sleep mode enables the lower power mode when addresses remain stable for a designated time.
- V_{IO} = 1.65V to V_{CC} or 2.7V to V_{CC} depending on the model.
- V_{CC} = 3V and V_{IO} = 3V or 1.8V. When V_{IO} is at 1.8V, I/O pins cannot operate at >1.8V.
- During power-up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.
- If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
- For all other DC current values please refer to the [S29GL01GT/S29GL512T](#) data sheet.

Table 6.2 DC Characteristics (–40°C to +105°C)

| Parameter | Description | Test Conditions | | Min | Typ (Note 2) | Max | Unit |
|------------------|--|---|------------|-----|-----------------|------|------|
| I _{LI} | Input Load Current | V _{IN} = V _{SS} to V _{CC} , V _{CC} = V _{CC} max | All Others | | ±0.04 | ±2.0 | µA |
| | | | WP#, BYTE# | | ±0.5 | ±2.0 | |
| I _{LO} | Output Leakage Current | V _{OUT} = V _{SS} to V _{CC} , V _{CC} = V _{CC} max | | | ±0.04 | ±2.0 | µA |
| I _{CC4} | VCC Standby Current | CE#, RESET#, OE# = V _{IH} , V _{IH} = V _{IO} V _{IL} = V _{SS} , V _{CC} = V _{CC} max | | | 140 | 400 | µA |
| I _{CC5} | VCC Reset Current (Notes 2, 7) | CE# = V _{IH} , RESET# = V _{IL} , V _{CC} = V _{CC} max | | | 20 | 40 | mA |
| I _{CC6} | Automatic Sleep Mode (3) | V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC} max, t _{ACC} + 30 ns | | | 6 | 12 | mA |
| | | V _{IH} = V _{IO} , V _{IL} = V _{SS} , V _{CC} = V _{CC} max, t _{ASSB} | | | 200 | 400 | µA |
| I _{CC7} | VCC Current during power up (Notes 2, 6) | RESET# = V _{IO} , CE# = V _{IO} , OE# = V _{IO} , V _{CC} = V _{CC} max, | | | 106 | 160 | mA |

Notes

1. I_{CC} active while Embedded Algorithm is in progress.
2. Not 100% tested.
3. Automatic sleep mode enables the lower power mode when addresses remain stable for a designated time.
4. V_{IO} = 1.65V to V_{CC} or 2.7V to V_{CC} depending on the model.
5. V_{CC} = 3V and V_{IO} = 3V or 1.8V. When V_{IO} is at 1.8V, I/O pins cannot operate at >1.8V.
6. During power-up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.
7. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC7} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
8. For all other DC current values please refer to the [S29GL01GT/S29GL512T](#) data sheet.

7. BGA Package Capacitance

| Parameter Symbol | Parameter Description | Typ | Max | Unit |
|------------------|-----------------------|-----|-----|------|
| C _{IN} | Input Capacitance | 9 | 11 | pF |
| C _{OUT} | Output Capacitance | 7 | 9 | pF |
| A26 | Highest Order Address | 5 | 6 | pF |
| CE# | Separated Control Pin | 4 | 5 | pF |
| OE# | Separated Control Pin | 4 | 5 | pF |
| WE# | Separated Control Pin | 7 | 8 | pF |
| WP# | Separated Control Pin | 5 | 6 | pF |
| RESET# | Separated Control Pin | 39 | 41 | pF |
| RY/BY# | Separated Control Pin | 4 | 5 | pF |

Notes

1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f = 1.0 MHz.

8. Thermal Resistance

| Parameter | Description | LSH064 | Unit |
|-----------|--|--------|------|
| Theta JA | Thermal Resistance (junction to ambient) | 29 | °C/W |

9. Data Integrity

9.1 Erase Endurance

| Parameter | Minimum | Unit |
|---|---------|-----------|
| Program/Erase cycles per main Flash array sectors | 100K | P/E cycle |
| Program/Erase cycles per PPB array or non-volatile register array (1) | 100K | P/E cycle |

Note:

1. Each write command to a non-volatile register causes a P/E cycle on the entire non-volatile register array. OTP bits and registers internally reside in a separate array that is not P/E cycled.

9.2 Data Retention

| Parameter | Test Conditions | Minimum Time | Unit |
|---------------------|---------------------------|--------------|-------|
| Data Retention Time | 1K Program/Erase Cycles | 20 | Years |
| | 10K Program/Erase Cycles | 2 | Years |
| | 100K Program/Erase Cycles | .2 | Years |

Contact Cypress Sales or an FAE representative for additional information regarding data integrity.

10. Device ID and Common Flash Interface (ID-CFI) ASO Map

The Device ID portion of the ASO (word locations 0h to 0Fh) provides manufacturer ID, device ID, Sector Protection State, and basic feature set information for the device.

ID-CFI Location 02h displays sector protection status for the sector selected by the sector address (SA) used in the ID-CFI enter command. To read the protection status of more than one sector it is necessary to exit the ID ASO and enter the ID ASO using the new SA. The access time to read location 02h is always t_{ACC} and a read of this location requires CE# to go High before the read and return Low to initiate the read (asynchronous read access). Page mode read between location 02h and other ID locations is not supported. Page mode read between ID locations other than 02h is supported.

Table 10.1 ID (Autoselect) Address Map

| Description | Address (x16) | Address (x8) | Read Data |
|-------------------------|---------------|--------------|---|
| Manufacture ID | (SA) + 0000h | (SA) + 0000h | 0001h |
| Device ID | (SA) + 0001h | (SA) + 0002h | 227Eh |
| Protection Verification | (SA) + 0002h | (SA) + 0004h | Sector Protection State (1= Sector protected, 0= Sector unprotected). To read a different SA protection state only a new SA needs to be given. |
| Indicator Bits | (SA) + 0003h | (SA) + 0006h | For S70GL02Gt highest address sector protect: XX3Fh = Not Factory Locked XXBFh = Factory Locked For S70GL02GT lowest address sector protect: XX2Fh = Not Factory Locked XXAFh = Factory Locked DQ15-DQ08 = 1 (Reserved) DQ7 - Factory Locked Secure Silicon Region 1 = Locked 0 = Not Locked DQ6 - Customer Locked Secure Silicon Region 1 = Locked 0 = Not Locked DQ5 = 1 (Reserved) DQ4 - WP# Protects 0 = lowest address Sector 1 = highest address Sector DQ3 - DQ0 = 1 (Reserved) |
| RFU | (SA) + 0004h | (SA) + 0008h | Reserved |
| | (SA) + 0005h | (SA) + 000Ah | Reserved |
| | (SA) + 0006h | (SA) + 000Ch | Reserved |
| | (SA) + 0007h | (SA) + 000Eh | Reserved |
| | (SA) + 0008h | (SA) + 0010h | Reserved |
| | (SA) + 0009h | (SA) + 0012h | Reserved |
| | (SA) + 000Ah | (SA) + 0014h | Reserved |
| | (SA) + 000Bh | (SA) + 0016h | Reserved |
| Lower Software Bits | (SA) + 000Ch | (SA) + 0018h | Bit 0 - Status Register Support 1 = Status Register Supported 0 = Status Register not supported Bit 1 - DQ polling Support 1 = DQ bits polling supported 0 = DQ bits polling not supported Bit 3-2 - Command Set Support 11 = reserved 10 = reserved 01 = Reduced Command Set 00 = Classic Command set Bits 4-15 - Reserved = 0 |
| Upper Software Bits | (SA) + 000Dh | (SA) + 001Ah | Reserved |
| Device ID | (SA) + 000Eh | (SA) + 001Ch | 2248h = 2 Gb |
| Device ID | (SA) + 000Fh | (SA) + 000Eh | 2201h |

Table 10.2 CFI Query Identification String

| Word Address | Data | Description |
|--|-------------------------|---|
| (SA) + 0010h (SA) + 0011h (SA) + 0012h | 0051h 0052h 0059h | Query Unique ASCII string "QRY" |
| (SA) + 0013h (SA) + 0014h | 0002h 0000h | Primary OEM Command Set |
| (SA) + 0015h (SA) + 0016h | 0040h 0000h | Address for Primary Extended Table |
| (SA) + 0017h (SA) + 0018h | 0000h 0000h | Alternate OEM Command Set (00h = none exists) |
| (SA) + 0019h (SA) + 001Ah | 0000h 0000h | Address for Alternate OEM Extended Table (00h = none exists) |

Table 10.3 CFI System Interface String

| Word Address | Data | Description |
|--------------|-------------------------------|---|
| (SA) + 001Bh | 0027h | V _{CC} Min. (erase/program) (D7-D4: volts, D3-D0: 100 mV) |
| (SA) + 001Ch | 0036h | V _{CC} Max. (erase/program) (D7-D4: volts, D3-D0: 100 mV) |
| (SA) + 001Dh | 0000h | V _{PP} Min. voltage (00h = no V _{PP} pin present) |
| (SA) + 001Eh | 0000h | V _{PP} Max. voltage (00h = no V _{PP} pin present) |
| (SA) + 001Fh | 0008h | Typical timeout per single word write 2 ^N μs |
| (SA) + 0020h | 0009h | Typical timeout for max multi-byte program, 2 ^N μs (00h = not supported) |
| (SA) + 0021h | 000Ah | Typical timeout per individual block erase 2 ^N ms |
| (SA) + 0022h | 0015h (2 Gb) | Typical timeout for full chip erase 2 ^N ms (00h = not supported) |
| (SA) + 0023h | 0002h (85°C) 0003h (105°C) | Max. timeout for single word write 2 ^N times typical |
| (SA) + 0024h | 0001h (85°C) 0002h (105°C) | Max. timeout for buffer write 2 ^N times typical |
| (SA) + 0025h | 0002h | Max. timeout per individual block erase 2 ^N times typical |
| (SA) + 0026h | 0002h | Max. timeout for full chip erase 2 ^N times typical (00h = not supported) |

Table 10.4 CFI Device Geometry Definition

| Word Address | Data | Description |
|--------------|--------------|--|
| (SA) + 0027h | 001Ch (2 Gb) | Device Size = 2 ^N byte |
| (SA) + 0028h | 0002h | Flash Device Interface Description 0 = x8-only, 1 = x16-only, 2 = x8/x16 capable |
| (SA) + 0029h | 0000h | |
| (SA) + 002Ah | 0009h | |
| (SA) + 002Bh | 0000h | Max. number of byte in multi-byte write = 2 ^N (00 = not supported) |
| (SA) + 002Ch | 0001h | Number of Erase Block Regions within device 1 = Uniform Device, 2 = Boot Device |
| (SA) + 002Dh | 00FFh | Erase Block Region 1 Information (refer to JEDEC JESD68-01 or JEP137 specifications) |
| (SA) + 002Eh | 0007h | |
| (SA) + 002Fh | 0000h | |
| (SA) + 0030h | 0002h | |
| (SA) + 0031h | 0000h | Erase Block Region 2 Information (refer to CFI publication 100) |
| (SA) + 0032h | 0000h | |
| (SA) + 0033h | 0000h | |
| (SA) + 0034h | 0000h | |
| (SA) + 0035h | 0000h | Erase Block Region 3 Information (refer to CFI publication 100) |
| (SA) + 0036h | 0000h | |
| (SA) + 0037h | 0000h | |
| (SA) + 0038h | 0000h | |
| (SA) + 0039h | 0000h | Erase Block Region 4 Information (refer to CFI publication 100) |
| (SA) + 003Ah | 0000h | |
| (SA) + 003Bh | 0000h | |
| (SA) + 003Ch | 0000h | |
| (SA) + 003Dh | FFFFh | Reserved |
| (SA) + 003Eh | FFFFh | |
| (SA) + 003Fh | FFFFh | |

Table 10.5 CFI Primary Vendor-Specific Extended Query

| Word Address | Data | Description |
|--------------|-------|---|
| (SA) + 0040h | 0050h | Query-unique ASCII string "PRI" |
| (SA) + 0041h | 0052h | |
| (SA) + 0042h | 0049h | |
| (SA) + 0043h | 0031h | Major version number, ASCII |
| (SA) + 0044h | 0035h | Minor version number, ASCII |
| (SA) + 0045h | 0024h | Address Sensitive Unlock (Bits 1-0) 00b = Required 01b = Not Required Process Technology (Bits 5-2) 0000b = 0.23 μ m Floating Gate 0001b = 0.17 μ m Floating Gate 0010b = 0.23 μ m MirrorBit 0011b = 0.13 μ m Floating Gate 0100b = 0.11 μ m MirrorBit 0101b = 0.09 μ m Floating Gate 0110b = 0.09 μ m MirrorBit 0111b = 0.065 μ m MirrorBit Eclipse 1000b = 0.065 μ m MirrorBit 1001b = 0.045 μ m MirrorBit |
| (SA) + 0046h | 0002h | Erase Suspend 0 = Not Supported 1 = Read Only 2 = Read and Write |
| (SA) + 0047h | 0001h | Sector Protect 00 = Not Supported X = Number of sectors in smallest group |
| (SA) + 0048h | 0000h | Temporary Sector Unprotect 00 = Not Supported 01 = Supported |
| (SA) + 0049h | 0008h | Sector Protect/Unprotect Scheme 04 = High Voltage Method 05 = Software Command Locking Method 08 = Advanced Sector Protection Method |
| (SA) + 004Ah | 0000h | Simultaneous Operation 00 = Not Supported X = Number of banks |
| (SA) + 004Bh | 0000h | Burst Mode Type 00 = Not Supported 01 = Supported |
| (SA) + 004Ch | 0003h | Page Mode Type 00 = Not Supported 01 = 4 Word Page 02 = 8 Word Page 03=16 Word Page |

Table 10.5 CFI Primary Vendor-Specific Extended Query (Continued)

| Word Address | Data | Description |
|---------------------------------|-------------|--|
| (SA) + 004Dh | 00B5h | ACC (Acceleration) Supply Minimum 00 = Not Supported D7-D4: Volt D3-D0: 100 mV |
| (SA) + 004Eh | 00C5h | ACC (Acceleration) Supply Maximum 00 = Not Supported D7-D4: Volt D3-D0: 100 mV |
| (SA) + 004Fh | 0005h (Top) | WP# Protection 00h = Flash device without WP Protect (No Boot) 01h = Eight 8 kB Sectors at TOP and Bottom with WP (Dual Boot) 02h = Bottom Boot Device with WP Protect (Bottom Boot) 03h = Top Boot Device with WP Protect (Top Boot) 04h = Uniform, Bottom WP Protect (Uniform Bottom Boot) 05h = Uniform, Top WP Protect (Uniform Top Boot) 06h = WP Protect for all sectors 07h = Uniform, Top or Bottom WP Protect |
| (SA) + 0050h | 0001h | Program Suspend 00 = Not Supported 01 = Supported |
| (SA) + 0051h | 0002h | Unlock Bypass 00 = Not Supported 01 = Supported |
| (SA) + 0052h | 0009h | Secured Silicon Sector (Customer OTP Area) Size 2^N (bytes) |
| (SA) + 0053h | 008Fh | Software Features bit 0: status register polling (1 = supported, 0 = not supported) bit 1: DQ polling (1 = supported, 0 = not supported) bit 2: new programsuspend/resumecommands (1 = supported, 0 = not supported) bit 3: word programming (1 = supported, 0 = not supported) bit 4: bit-field programming (1 = supported, 0 = not supported) bit 5: autodetect programming (1 = supported, 0 = not supported) bit 6: RFU bit 7: multiple writes per Line (1 = supported, 0 = not supported) |
| (SA) + 0054h | 0005h | Page Size = 2^N bytes |
| (SA) + 0055h | 0006h | Erase Suspend Timeout Maximum < 2^N (μ s) |
| (SA) + 0056h | 0006h | Program Suspend Timeout Maximum < 2^N (μ s) |
| (SA) + 0057h to (SA) + 0077h | FFFFh | Reserved |
| (SA) + 0078h | 0006h | Embedded Hardware Reset Timeout Maximum < 2^N (μ s) Reset with Reset Pin |
| (SA) + 0079h | 0009h | Non-Embedded Hardware Reset Timeout Maximum < 2^N (μ s) Power on Reset |

11. Other Resources

11.1 Cypress Flash Memory Roadmap

<http://www.cypress.com/Flash-Roadmap>

11.2 Links to Software

<http://www.cypress.com/software-and-drivers-cypress-flash-memory>

11.3 Links to Application Notes

<http://www.cypress.com/cypressappnotes>

12. Revision History

Document History Page

| Document Title: S70GL02GT, 2-Gbit (256-Mbyte) 3.0V Flash Memory Document Number: 002-13915 | | | | |
|---|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | 5415485 | NFB | 08/26/2016 | Initial release |
| *A | 5441037 | NFB | 10/21/2016 | Updated Section 7. , BGA Package Capacitance on page 12. Added Section 8. , Thermal Resistance on page 12. Added Section 9. , Data Integrity on page 12. Added Section 11. , Other Resources on page 18. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|-------------------------------|--|
| ARM® Cortex® Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Lighting & Power Control | cypress.com/powerpsoc |
| Memory | cypress.com/memory |
| PSoC | cypress.com/psoc |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless/RF | cypress.com/wireless |

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.