S71AL016M Based MCPs

Stacked Multi-Chip Product (MCP) Flash Memory and RAM

16 Megabit (1 M x 16-bit) CMOS 3.0 Volt-only Flash Memory and 4 Megabit (256K x 16-bit) Static RAM/ Pseudo Static RAM

ADVANCE INFORMATION

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Publication Number S71AL016M_00 **Revision** A **Amendment** 0 **Issue Date** February 23, 2005

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S71AL0I6M based MCPs

Stacked Multi-Chip Product (MCP) Flash Memory and RAM
I6 Megabit (I M x I6-bit) CMOS 3.0 Volt-only Flash Memory and 4 Megabit (256K x I6-bit) Static RAM/ Pseudo Static RAM

ADVANCE INFORMATION

Distinctive Characteristics

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High performance**
  - — 90 ns
- **Packages**
  - — 7 x 9 x 1.2 mm 56 ball FBGA
- **Operating Temperature**
  - — –25°C to +85°C (Wireless)

General Description

The S71AL series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- One S29AL Flash memory die
- pSRAM or SRAM

The products covered by this document are listed in the table below:

		Flash Memory Density
		I6Mb
SRAM / pSRAM Density	4Mb	S71AL016M40

Notice On Data Sheet Designations

Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion LLC is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion LLC therefore places the following conditions upon Advance Information content:

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Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

Table of Contents

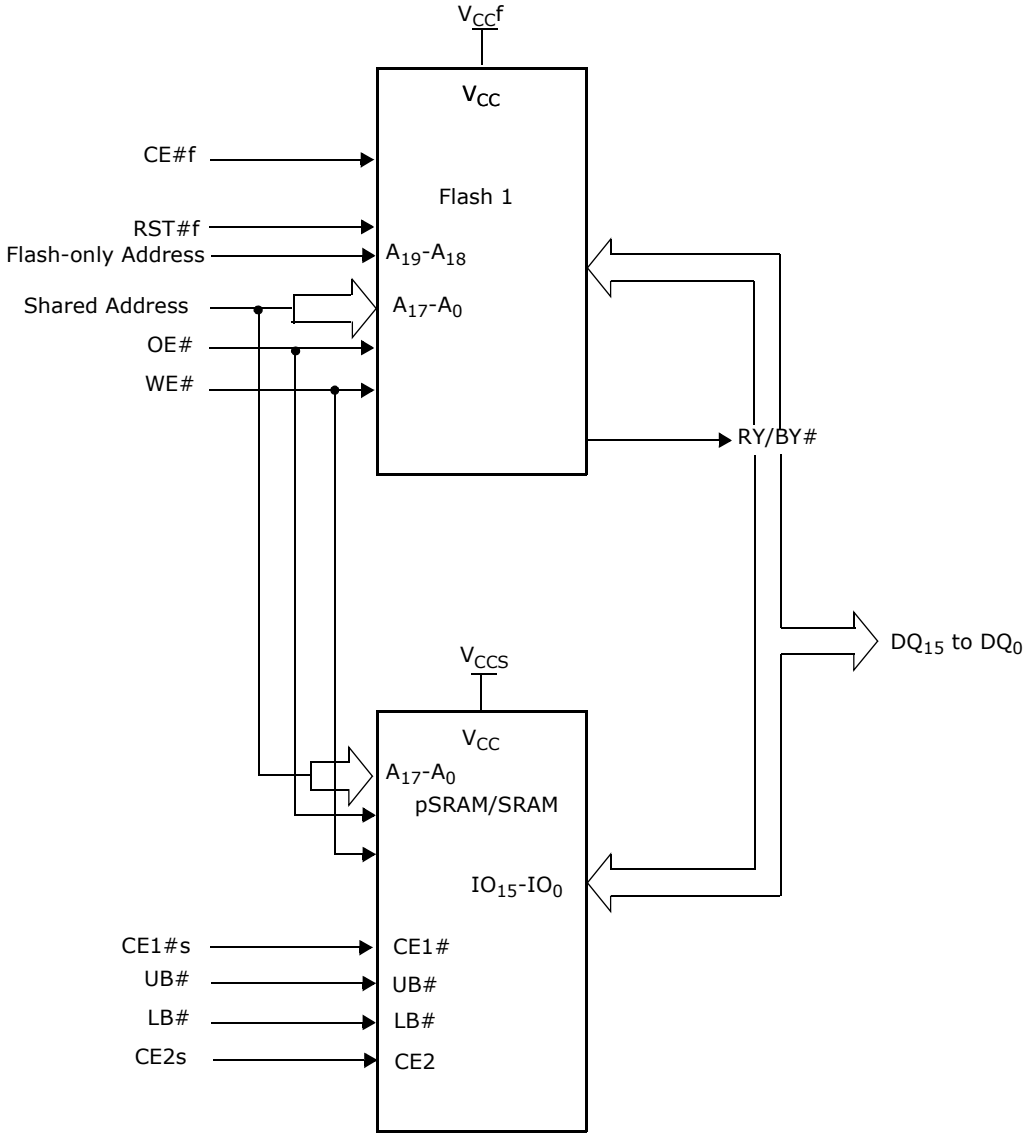
S71AL016M based MCPs 3
Product Selector Guide 6
16 Mb Flash Memory 6
MCP Block Diagram 7
Connection Diagram 8
Pin Description 9
Logic Symbol 9
Ordering Information 10
Valid Combinations 11
Physical Dimensions 12
S29AL016M 13
Distinctive Characteristics 13
General Description 14
Logic Symbol 16
Table 1. S29AL016M Device Bus Operations 17
Requirements for Reading Array Data 17
Writing Commands/Command Sequences 18
Program and Erase Operation Status 18
Standby Mode 18
Automatic Sleep Mode 18
RESET#: Hardware Reset Pin 19
Output Disable Mode 19
Table 2. Sector Address Tables (Model 01, Top Boot Device) 20
Table 3. Sector Address Tables (Model 02, Bottom Boot Device) 21
Autoselect Mode 22
Table 4. Autoselect Codes (High Voltage Method) 22
Sector Protection/Unprotection 22
Temporary Sector Unprotect 23
Figure 1. Temporary Sector Unprotect Operation 23
Figure 2. In-System Single High Voltage Sector Protect/ Unprotect Algorithms 24
SecSi (Secured Silicon) Sector Flash Memory Region 25
Table 5. SecSi Sector Addressing 25
Figure 3. SecSi Sector Protect Verify 26
Common Flash Memory Interface (CFI) 26
Table 6. CFI Query Identification String 27
Table 7. System Interface String 27
Table 8. Device Geometry Definition 28
Table 9. Primary Vendor-Specific Extended Query 28
Hardware Data Protection 29
Reading Array Data 29
Reset Command 30
Autoselect Command Sequence 30
Word Program Command Sequence 31
Figure 4. Program Operation 32
Chip Erase Command Sequence 32
Sector Erase Command Sequence 33
Erase Suspend/Erase Resume Commands 33
Figure 5. Erase Operation 35
Program Suspend/Program Resume Command Sequence 35
Figure 6. Program Suspend/Program Resume 36
Table 10. Command Definitions 37
DQ7: Data# Polling 38
Figure 7. Data# Polling Algorithm 39
RY/BY#: Ready/Busy# 39
DQ6: Toggle Bit I 40
DQ2: Toggle Bit II 40
Reading Toggle Bits DQ6/DQ2 41
Figure 8. Toggle Bit Algorithm 42
DQ5: Exceeded Timing Limits 42
DQ3: Sector Erase Timer 43
Table 11. Write Operation Status 43
Figure 9. Maximum Negative Overshoot Waveform 44
Figure 10. Maximum Positive Overshoot Waveform 44
Operating Ranges 44
Table 12. CMOS Compatible 45
Figure 11. Test Setup 46
Table 13. Test Specifications 46
Key to Switching Waveforms 46
Figure 12. Input Waveforms and Measurement Levels 46
Table 14. Read Operations 47
Figure 13. Read Operations Timings 47
Table 15. Hardware Reset (RESET#) 48
Figure 14. RESET# Timings 48
Figure 15. Program Operation Timings 50
Figure 16. Chip/Sector Erase Operation Timings 51
Figure 17. Data# Polling Timings (During Embedded Algorithms) 52
Figure 18. Toggle Bit Timings (During Embedded Algorithms) 52
Figure 19. DQ2 vs. DQ6 for Erase and Erase Suspend Operations 53
Table 16. Temporary Sector Unprotect 53
Figure 20. Temporary Sector Unprotect/Timing Diagram 53
Figure 21. Sector Protect/Unprotect Timing Diagram 54
Table 17. Alternate CD# Controlled Erase/Program Operations 55
Figure 22. Alternate CE# Controlled Write Operation T imings 56
Table 18. Erase and Programming Performance 57
Table 19. TSOP Pin and BGA Package Capcitance 57
Type 4 pSRAM 59
Features 59
Functional Description 59
Product Portfolio 59
Maximum Ratings 60
Operating Range 60
Table 20. DC Electrical Characteristics (Over the Operating Range) 60
Capacitance 61
Thermal Resistance 61
AC Test Loads and Waveforms 61
Figure 23. AC Test Loads and Waveforms 61
Table 21. Switching Characteristics 62
Switching Waveforms 63
Figure 24. Read Cycle 1 (Address Transition Controlled) 63
Figure 25. Read Cycle 2 (OE# Controlled) 63
Figure 26. Write Cycle 1 (WE# Controlled) 64
Figure 27. Write Cycle 2 (CE#1 or CE2 Controlled) 65
Figure 28. Write Cycle 3 (WE# Controlled, OE# Low) 66
Figure 29. Write Cycle 4 (BHE#/BLE# Controlled, OE# Low) 66
Truth Table 67
Revision Summary 68

Product Selector Guide

16 Mb Flash Memory

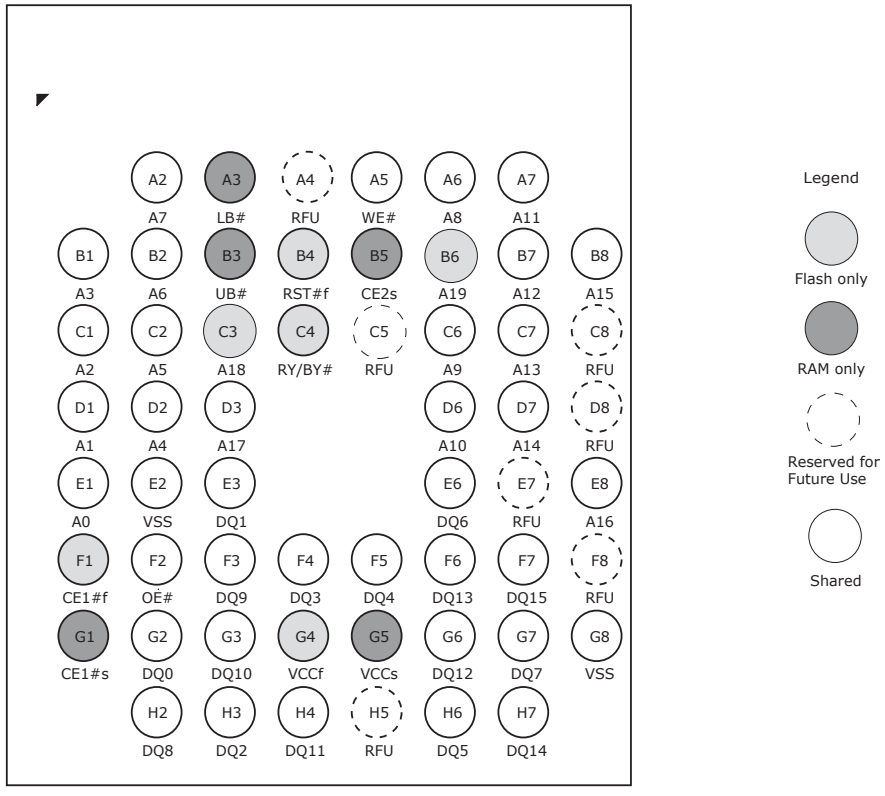
Device-Model#	Flash Access time (ns)	pSRAM density	(p)SRAM Access time (ns)	pSRAM type	Package
S71AL016M40-0B	90	4 M pSRAM	70	pSRAM4	TLC056
S71AL016M40-0F	90	4 M pSRAM	70	pSRAM4	TLC056

MCP Block Diagram



Connection Diagram

56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)

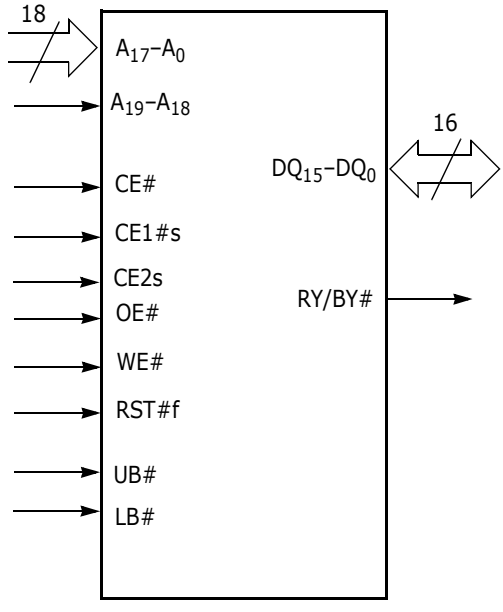


MCP	Flash Only Address	Shared Addresses
S71AL016M40	A_{19} - A_{18}	A_{17} - A_0

Pin Description

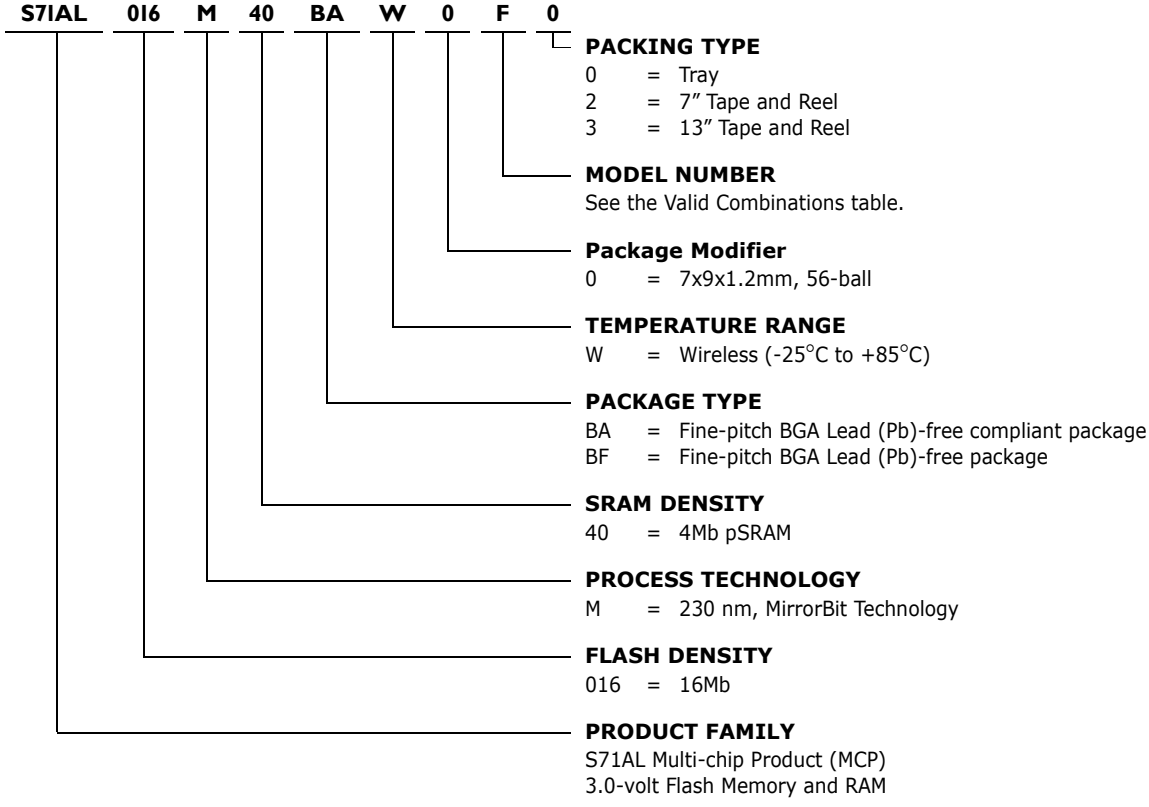
A_{17}–A_0	=	Address Inputs (Common)
A_{19}–A_{18}	=	Address Inputs (Flash-only)
DQ_{15}–DQ_0	=	16 Data Inputs/Outputs (Common)
CE1#f	=	Chip Enable 1 (Flash)
CE1#s	=	Chip Enable 1 (pSRAM)
CE2s	=	Chip Enable 2 (pSRAM)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#	=	Ready/Busy Output (Flash-only)
UB#	=	Upper Byte Control (pSRAM)
LB#	=	Lower Byte Control (pSRAM)
RST#f	=	Hardware Reset Pin, Active Low (Flash)
V_{CC}f	=	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{CC}s	=	pSRAM Power Supply
V_{SS}	=	Device Ground (Common)
NC	=	Pin Not Connected Internally
RFU	=	Reserved for Future Use

Logic Symbol



Ordering Information

The order number is formed by a valid combinations of the following:



Valid Combinations

S71AL016D Valid Combinations				Speed Options (ns)	(p)SRAM Type/Access Time (ns)	Package Marking
Base Ordering Part Number	**Package & Temperature**	**Package Modifier/ Model Number**	**Packing Type**			
S71AL016M40	BAW, BFW	0B	Bottom-Boot	90	pSRAM4/ 70	(Note 2)
S71AL016M40		0F	Top-Boot		pSRAM4 / 70	

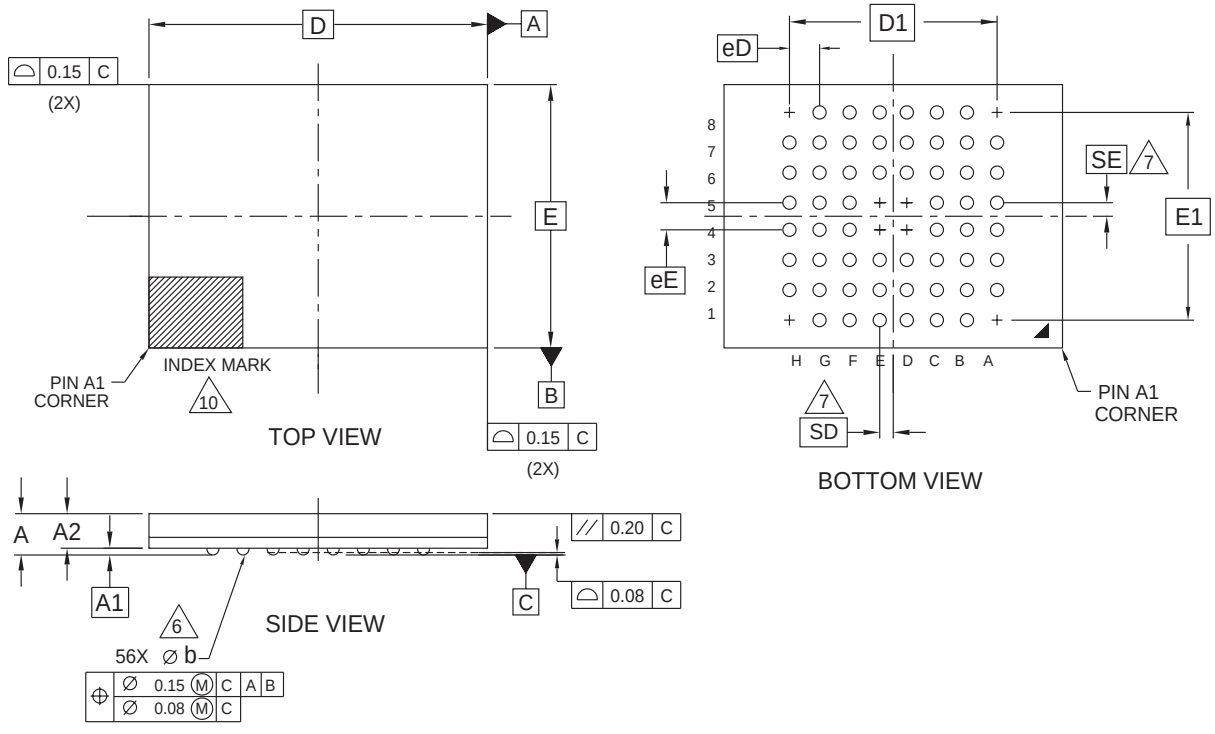
Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading S and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Physical Dimensions

TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA)
9 x 7 mm Package



PACKAGE	TLC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	9.00 BSC.			BODY SIZE
E	7.00 BSC.			BODY SIZE
D1	5.60 BSC.			MATRIX FOOTPRINT
E1	5.60 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A1,A8,D4,D5,E4,E5,H1,H8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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S29AL016M

16 Megabit (M x 16-Bit)
3.0 Volt-only Boot Sector Flash Memory
Featuring MirrorBit™ Technology

MCP Flash Module

ADVANCE INFORMATION

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - 3 V for read, erase, and program operations
- **Manufactured on 0.23 µm MirrorBit™ process technology**
- **SecSi™ (Secured Silicon) Sector region**
  - 128-word sector for permanent, secure identification through an 8-word random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **Top or bottom boot block configurations available**
- **100,000 erase cycle typical per sector**
- **20-year typical data retention**

Performance Characteristics

- **High performance**
  - 90/100 ns access time
  - 0.7 s typical sector erase time
- **Low power consumption (typical values at 5 MHz)**
  - 400 nA standby mode current
  - 15 mA read current
  - 40 mA program/erase current
  - 400 nA Automatic Sleep mode current

Software Features

- Program Suspend & Resume: read other sectors before programming operation is completed
- Erase Suspend & Resume: read/program other sectors before an erase operation is completed
- Data# polling & toggle bits provide status
- Unlock Bypass Program command reduces overall multiple-word programming time
- CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices

Hardware Features

- Sector Protection: hardware-level method of preventing write operations within a sector
- Temporary Sector Unprotect: V_{ID}-level method of changing code in locked sectors
- Hardware reset input (RESET#) resets device
- Ready/Busy# output (RY/BY#) indicates program or erase cycle completion

Publication Number S71AL016M_M0 **Revision** A **Amendment** 0 **Issue Date** February 23, 2005

General Description

The S29AL016M is a 16 Mbit, 3.0 Volt-only Flash memory organized as 1,048,576 words. The word-wide data (x16) appears on DQ15–DQ0. The device requires only a **single 3.0 volt power supply** for both read and write functions, designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. The device can also be programmed in standard EPROM programmers.

To eliminate bus contention the device contains separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation begins, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses are stable for a specified period of time.

The **SecSi™ (Secured Silicon) Sector** provides a 128-word area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

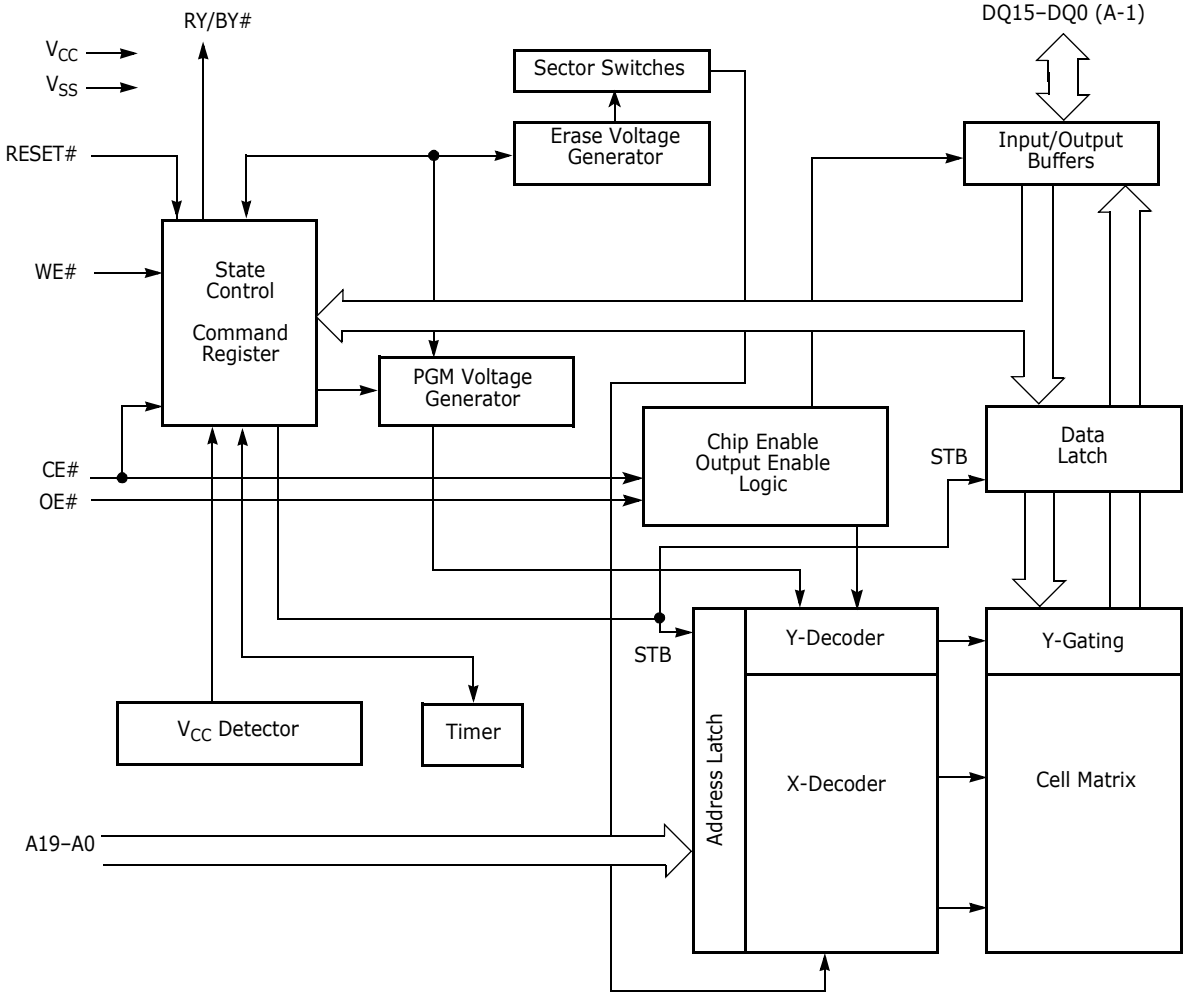
Product Selector Guide

Family Part Number		S29AL016M	
Speed Option	Full Voltage Range: V_{CC} = 2.7–3.6 V	**90**	**100**
Max access time (ns)		90	100
Max CE# access time (ns)		90	100
Max OE# access time (ns)		25	25

Notes:

1. *See AC Characteristics on page 47 for full specifications.*
2. *Contact sales office or representative for availability and ordering information.*

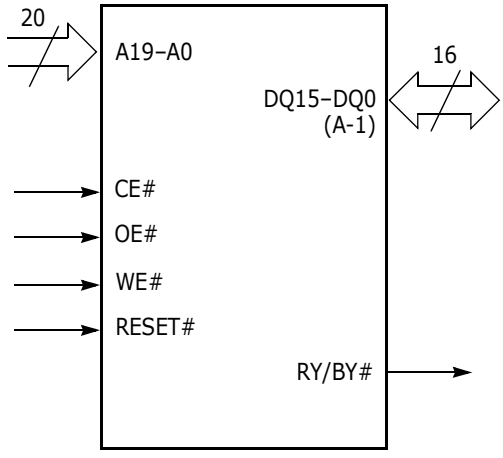
Block Diagram



Pin Configuration

A19–A0	=	20 addresses
DQ14–DQ0	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode),
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin
RY/BY#	=	Ready/Busy output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

Logic Symbol



Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table I. S29AL016M Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	Addresses (Note 1)	DQ00–DQ15
Read	L	L	H	H	A_{IN}	D_{OUT}
Write	L	H	L	H	A_{IN}	D_{IN}
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	X	High-Z
Output Disable	L	H	H	H	X	High-Z
Reset	X	X	X	L	X	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}
Sector Unprotect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are A19:A0 in word mode.*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See *Reading Array Data on page 29* for more information. Refer to Table 14 on page 47 for timing specifications and to Figure 13, on page 47 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The *Word Program Command Sequence on page 31* contains details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 2 and 3 indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The *Command Definitions on page 29* contains details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the *Autoselect Mode on page 22* and *Autoselect Command Sequence on page 30* sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The *AC Characteristics on page 47* section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to *Write Operation Status on page 38* for more information, and to *AC Characteristics on page 47* for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device is in the standby mode, but the standby current is greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the DC Characteristics table, I_{CC3} and I_{CC4} represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always

available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin to V_{IL} for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current is greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the *AC Characteristics on page 47* tables for RESET# parameters and to Figure 14, on page 48 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Tables (Model 0I, Top Boot Device)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
										Word Mode (x16)
SA0	0	0	0	0	0	X	X	X	64/32	000000–007FFF
SA1	0	0	0	0	1	X	X	X	64/32	008000–00FFFF
SA2	0	0	0	1	0	X	X	X	64/32	010000–017FFF
SA3	0	0	0	1	1	X	X	X	64/32	018000–01FFFF
SA4	0	0	1	0	0	X	X	X	64/32	020000–027FFF
SA5	0	0	1	0	1	X	X	X	64/32	028000–02FFFF
SA6	0	0	1	1	0	X	X	X	64/32	030000–037FFF
SA7	0	0	1	1	1	X	X	X	64/32	038000–03FFFF
SA8	0	1	0	0	0	X	X	X	64/32	040000–047FFF
SA9	0	1	0	0	1	X	X	X	64/32	048000–04FFFF
SA10	0	1	0	1	0	X	X	X	64/32	050000–057FFF
SA11	0	1	0	1	1	X	X	X	64/32	058000–05FFFF
SA12	0	1	1	0	0	X	X	X	64/32	060000–067FFF
SA13	0	1	1	0	1	X	X	X	64/32	068000–06FFFF
SA14	0	1	1	1	0	X	X	X	64/32	070000–077FFF
SA15	0	1	1	1	1	X	X	X	64/32	078000–07FFFF
SA16	1	0	0	0	0	X	X	X	64/32	080000–087FFF
SA17	1	0	0	0	1	X	X	X	64/32	088000–08FFFF
SA18	1	0	0	1	0	X	X	X	64/32	090000–097FFF
SA19	1	0	0	1	1	X	X	X	64/32	098000–09FFFF
SA20	1	0	1	0	0	X	X	X	64/32	0A0000–0A7FFF
SA21	1	0	1	0	1	X	X	X	64/32	0A8000–AFFFF
SA22	1	0	1	1	0	X	X	X	64/32	0B0000–0B7FFF
SA23	1	0	1	1	1	X	X	X	64/32	0B8000–0BFFFF
SA24	1	1	0	0	0	X	X	X	64/32	0C0000–0C7FFF
SA25	1	1	0	0	1	X	X	X	64/32	0C8000–0CFFFF
SA26	1	1	0	1	0	X	X	X	64/32	0D0000–0D7FFF
SA27	1	1	0	1	1	X	X	X	64/32	0D8000–0DFFFF
SA28	1	1	1	0	0	X	X	X	64/32	0E0000–0E7FFF
SA29	1	1	1	0	1	X	X	X	64/32	0E8000–0EFFFF
SA30	1	1	1	1	0	X	X	X	64/32	0F0000–0F7FFF
SA31	1	1	1	1	1	0	X	X	32/16	0F8000–0FBFFF
SA32	1	1	1	1	1	1	0	0	8/4	0FC000–0FCFFF
SA33	1	1	1	1	1	1	0	1	8/4	0FD000–0FDFFF
SA34	1	1	1	1	1	1	1	X	16/8	0FE000–0FFFFF

Note: *Address range is A19:A0 in word mode.*

Table 3. Sector Address Tables (Model 02, Bottom Boot Device)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
										Word Mode (x16)
SA0	0	0	0	0	0	0	0	X	16/8	000000–001FFF
SA1	0	0	0	0	0	0	1	0	8/4	002000–002FFF
SA2	0	0	0	0	0	0	1	1	8/4	003000–003FFF
SA3	0	0	0	0	0	1	X	X	32/16	004000–007FFF
SA4	0	0	0	0	1	X	X	X	64/32	008000–00FFFF
SA5	0	0	0	1	0	X	X	X	64/32	010000–017FFF
SA6	0	0	0	1	1	X	X	X	64/32	018000–01FFFF
SA7	0	0	1	0	0	X	X	X	64/32	020000–027FFF
SA8	0	0	1	0	1	X	X	X	64/32	028000–02FFFF
SA9	0	0	1	1	0	X	X	X	64/32	030000–037FFF
SA10	0	0	1	1	1	X	X	X	64/32	038000–03FFFF
SA11	0	1	0	0	0	X	X	X	64/32	040000–047FFF
SA12	0	1	0	0	1	X	X	X	64/32	048000–04FFFF
SA13	0	1	0	1	0	X	X	X	64/32	050000–057FFF
SA14	0	1	0	1	1	X	X	X	64/32	058000–05FFFF
SA15	0	1	1	0	0	X	X	X	64/32	060000–067FFF
SA16	0	1	1	0	1	X	X	X	64/32	068000–06FFFF
SA17	0	1	1	1	0	X	X	X	64/32	070000–077FFF
SA18	0	1	1	1	1	X	X	X	64/32	078000–07FFFF
SA19	1	0	0	0	0	X	X	X	64/32	080000–087FFF
SA20	1	0	0	0	1	X	X	X	64/32	088000–08FFFF
SA21	1	0	0	1	0	X	X	X	64/32	090000–097FFF
SA22	1	0	0	1	1	X	X	X	64/32	098000–09FFFF
SA23	1	0	1	0	0	X	X	X	64/32	0A0000–0A7FFF
SA24	1	0	1	0	1	X	X	X	64/32	0A8000–0AFFFF
SA25	1	0	1	1	0	X	X	X	64/32	0B0000–0B7FFF
SA26	1	0	1	1	1	X	X	X	64/32	0B8000–0BFFFF
SA27	1	1	0	0	0	X	X	X	64/32	0C0000–0C7FFF
SA28	1	1	0	0	1	X	X	X	64/32	0C8000–0CFFFF
SA29	1	1	0	1	0	X	X	X	64/32	0D0000–0D7FFF
SA30	1	1	0	1	1	X	X	X	64/32	0D8000–0DFFFF
SA31	1	1	1	0	0	X	X	X	64/32	0E0000–0E7FFF
SA32	1	1	1	0	1	X	X	X	64/32	0E8000–0EFFFF
SA33	1	1	1	1	0	X	X	X	64/32	0F0000–0F7FFF
SA34	1	1	1	1	1	X	X	X	64/32	0F8000–0FFFFF

Note: *Address range is A19:A0. n.*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 4. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 2 on page 20 and Table 3 on page 21). Table 4 on page 22 shows the remaining address bits that are don't care. When all necessary bits are set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 10 on page 37 and Table 11 on page 43. This method does not require V_{ID}. See *Command Definitions on page 29* for details on using the autoselect mode.

Table 4. Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A19 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID (Spansion Products)	L	L	H	X	X	V_{ID}	X	L	X	L	L	X	01h
Device ID: S29AL016M (Model 01) (Top Boot Block)	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	C4h
												X	C4h
Device ID: S29AL016M (Model 02) (Bottom Boot Block)	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	49h
												X	49h
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	01h (protected)
												X	00h (unprotected)
SecSi Sector Indicator Bit (DQ7)	L	L	H	X	X	V_{ID}	X	H	X	L	H	X	83 (factory locked 03h (not factory locked)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Note: *The autoselect codes may also be accessed in-system via command sequences. See Table 10 on page 37 and Table 11 on page 43.*

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

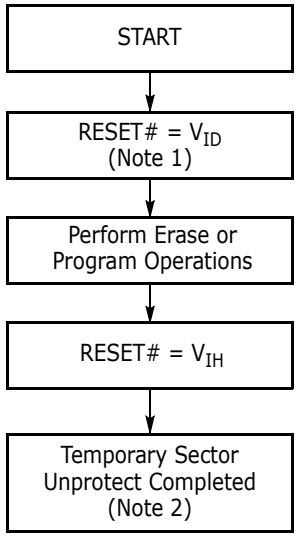
The device is normally shipped with all sectors unprotected. However, the ExpressFlash™ Service offers the option of programming and protecting sectors at the factory prior to shipping the device. Contact a sales office or representative for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode on page 22* for details.

Sector protection and unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2, on page 24 shows the algorithms and Figure 21, on page 54 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and Figure 22, on page 56 shows the timing diagrams, for this feature.



Notes:

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure I. Temporary Sector Unprotect Operation

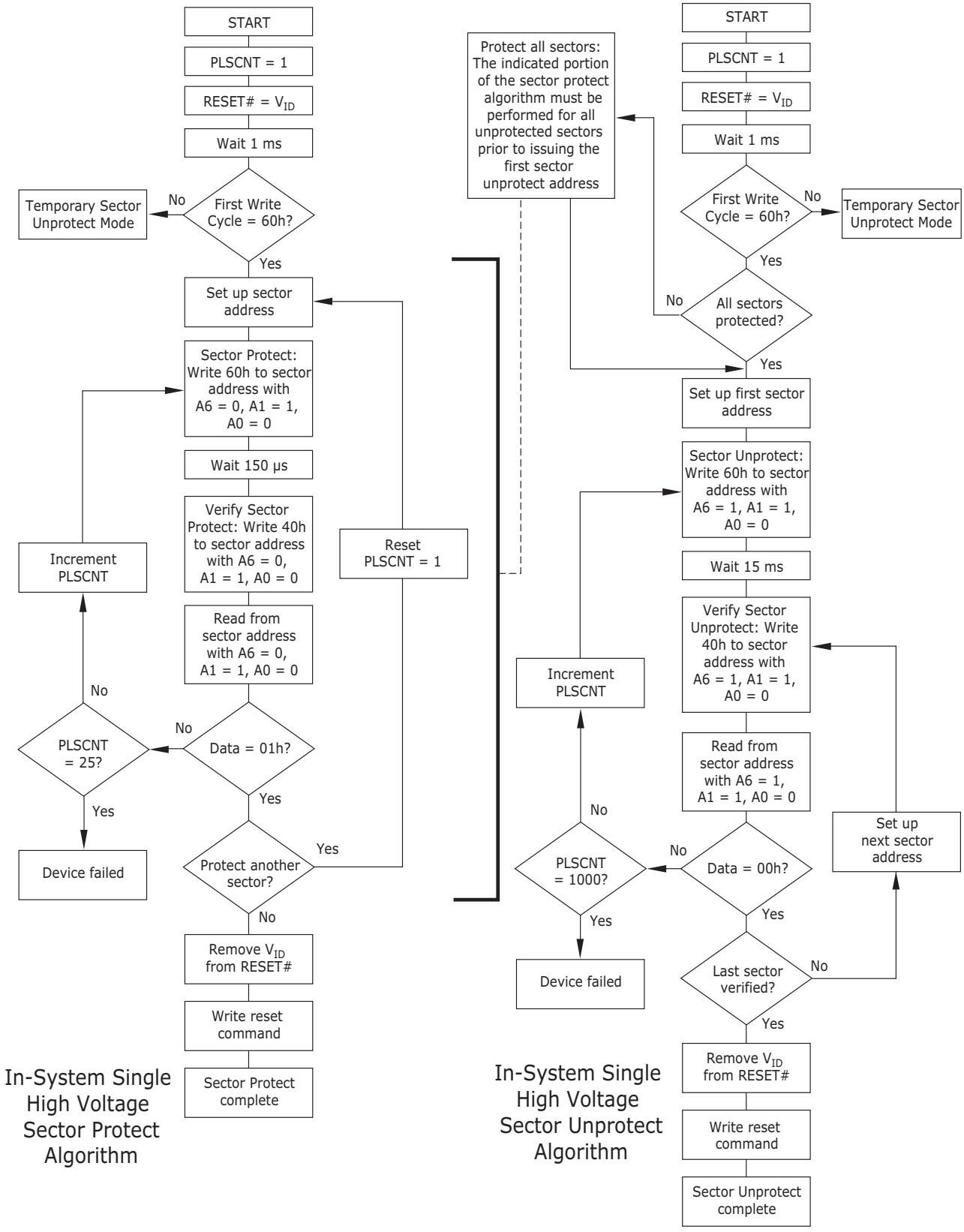


Figure 2. In-System Single High Voltage Sector Protect/Unprotect Algorithms

SecSi (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 256 bytes in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The device is offered with the SecSi Sector either customer lockable (standard shipping option) or factory locked (contact a sales office or representative for ordering information). The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also contains the SecSi Sector Indicator Bit permanently set to a *0*. The factory-locked version is always protected when shipped from the factory, and contains the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a *1*. Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

The SecSi sector address space in this device is allocated as follows:

Table 5. SecSi Sector Addressing

SecSi Sector Address Range x16	Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
0F8000h–0F8007h	Determined by customer	ESN	ESN or determined by customer
0F8008h–0F807Fh		Unavailable	Determined by customer

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi Sector/Exit SecSi Sector Command Sequence"). After the system writes the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses given in Table 5. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte SecSi sector.

The system may program the SecSi Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions.

Programming and protecting the SecSi Sector must be used with caution since, once protected, there is no procedure available for unprotecting the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, on page 24, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-sys-

tem protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.

- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 3, on page 26.

Once the SecSi Sector is programmed, locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing within the remainder of the array.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In devices with an ESN, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. An ESN Factory Locked device has a 16-byte random ESN at addresses given in Table 5 on page 25. Please contact your local sales office or representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by the manufacturer through the ExpressFlash service (Express Flash Factory Locked). The devices are then shipped from the factory with the SecSi Sector permanently locked. Contact an sales office or representative for details on using the ExpressFlash service.

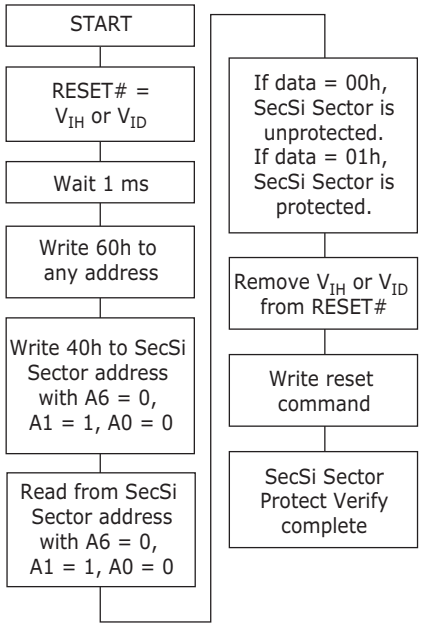


Figure 3. SecSi Sector Protect Verify

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h anytime the device is ready to read array data. The system can read CFI information at the addresses given in Table 6 on page 27, Table 7 on page 27, Table 8 on page 28, and Table 9 on page 28. In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 6 on page 27, Table 7 on page 27, Table 8 on page 28, and Table 9 on page 28. The system must write the reset command to return the device to the read/reset mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available online at http://www.amd.com/flash/cfi. Alternatively, contact an sales office or representative for copies of these documents.

Table 6. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 7. System Interface String

Addresses	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase). D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase). D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0007h	Typical timeout per single word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0001h	Reserved for future use
24h	0000h	Max. timeout for buffer write 2^N times typical (00h = not supported)
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Note: *CFI data related to timeouts may differ from actual timeouts of the product. Consult the Ordering the Erase and Programming Performance table for timeout guidelines.*

Table 8. Device Geometry Definition

Addresses	Data	Description
27h	0015h	Device Size = 2^N byte
28h 29h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0004h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0000h 0000h 0040h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	0001h 0000h 0020h 0000h	Erase Block Region 2 Information
35h 36h 37h 38h	0000h 0000h 0080h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	001Eh 0000h 0000h 0001h	Erase Block Region 4 Information

Table 9. Primary Vendor-Specific Extended Query (Sheet 1 of 2)

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string "PRI"
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0008h	Address Sensitive Unlock (Bit 1–0) 0b = Required, 1b = Not Required Process Technology (Bits 7–2) 0010b = 0.23 µm MirrorBit
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0004h	Sector Protect/Unprotect scheme 04 = Standard Mode
4Ah	0000h	Simultaneous Operation 00 = Not Supported, 01 = Supported

Table 9. Primary Vendor-Specific Extended Query (Sheet 2 of 2)

Addresses	Data	Description
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 10 on page 37 and Table 11 on page 43 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse *Glitch* Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 10 on page 37 and Table 11 on page 43 define the valid register command sequences. *Note that writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A reset command is then required to set the device for the next operation.*

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in *AC Characteristics on page 47*.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read

timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See *Erase Suspend/Erase Resume Commands on page 33* for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also *Requirements for Reading Array Data on page 17* for more information. The Table 14 on page 47 provides the read parameters, and Figure 13, on page 47 shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 10 on page 37 and Table 11 on page 43 show the address and data requirements. This method is an alternative to that shown in Table 4 on page 22, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address XX02h in word mode returns XX01h if that sector is protected, or 00h if it is unprotected. Refer to Table 2 on page 20 and Table 3 on page 21 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Tables 10–11 show the address and data requirements for the program command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See *Write Operation Status on page 38* for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Program command sequence should be reinitiated once the device resets to reading array data, to ensure data integrity.

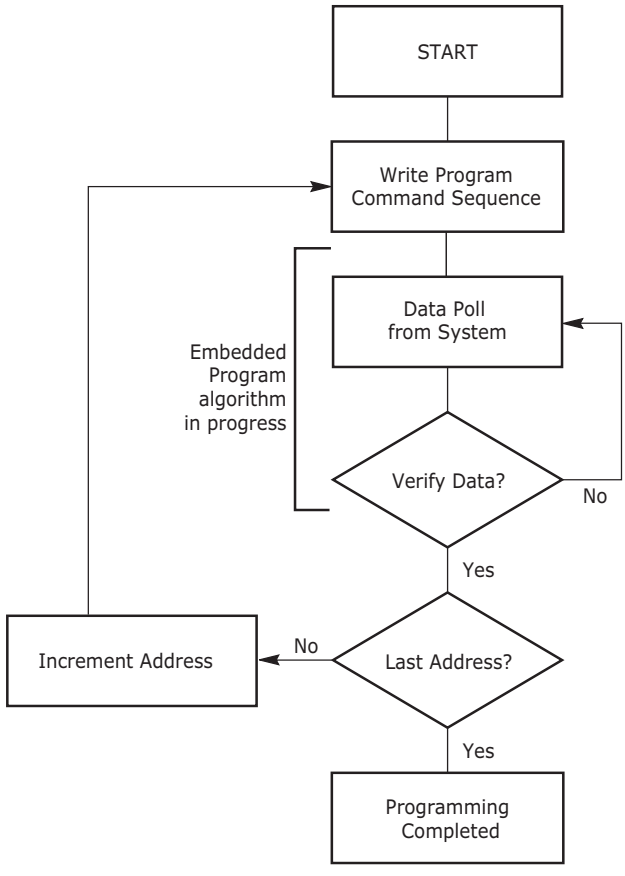
Programming is allowed in any sequence and across sector boundaries. Programming to the same address multiple times without intervening erases is limited. For such application requirements, please contact your local Spansion representative. Any bit in a word or byte **cannot be programmed from *0* back to a *1*.** Attempting to do so may halt the operation and set DQ5 to "1," or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read shows that the data is still *0*. Only erase operations can convert a *0* to a *1*.

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 10 on page 37 and Table 11 on page 43 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

Figure 4, on page 32 illustrates the algorithm for the program operation. See Table 18 on page 57 for parameters, and to Figure 17, on page 55 for timing diagrams.



Notes: *See Tables 10 and for program command sequence.*

Figure 4. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 10 on page 37 and Table 11 on page 43 show the address and data requirements for the chip erase command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.*

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See *Autoselect Command Sequence on page 30* for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 5, on page 35 illustrates the algorithm for the erase operation. See the Table 18 on page 57 for parameters, and to Figure 18, on page 57 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 10 on page 37 and Table 11 on page 43 show the address and data requirements for the sector erase command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation is in progress.*

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See *DQ3: Sector Erase Timer on page 43*.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation begins, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to *Write Operation Status on page 38* for information on these status bits.)

Figure 5, on page 35 illustrates the algorithm for the erase operation. Refer to the Table 18 on page 57 for parameters, and to Figure 18, on page 52 for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the

Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

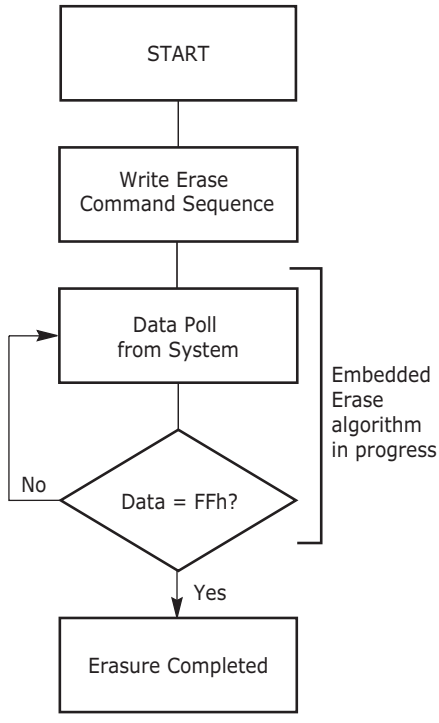
After the erase operation is suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See *Write Operation Status on page 38* for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See *Write Operation Status on page 38* for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See *Autoselect Command Sequence on page 30* for more information.

The system must write the Erase Resume command (address bits are *don't care*) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device resumes erasing.

Note: *During an erase operation, this flash device performs multiple internal operations that are invisible to the system. When an erase operation is suspended, any of the internal operations that were not fully completed must be restarted. As such, if this flash device is continually issued suspend/resume commands in rapid succession, erase progress is impeded as a function of the number of suspends. The result is a longer cumulative erase time than without suspends. Note that the additional suspends do not affect device reliability or future performance. In most systems rapid erase/suspend activity occurs only briefly. In such cases, erase performance is not significantly impacted.*



Notes:

1. *See Table 10 on page 37 and Table 11 on page 43 for erase command sequence.*
2. *See DQ3: Sector Erase Timer on page 43 for more information.*

Figure 5. Erase Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 µs maximum (5 µs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation is suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See *Write Operation Status on page 38* for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming.

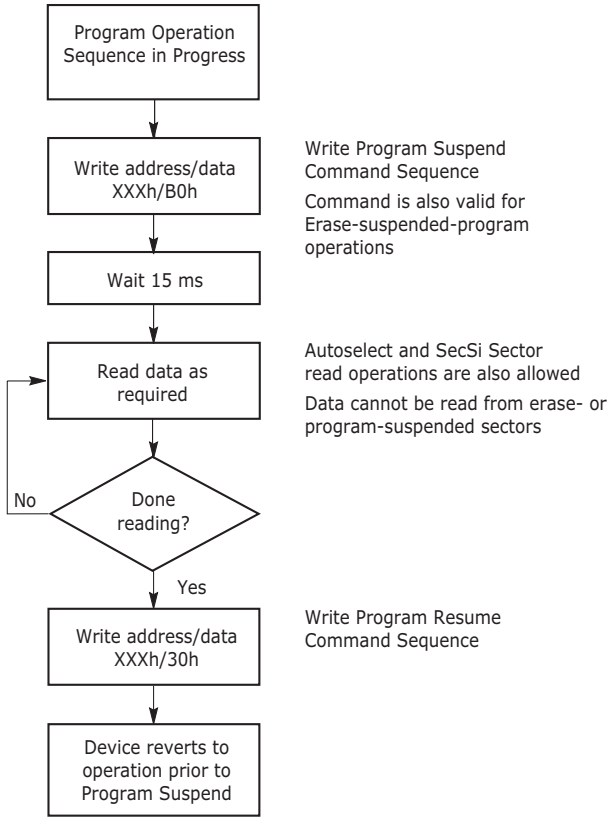


Figure 6. Program Suspend/Program Resume

Command Definitions Tables

Table 10. Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID, Top Boot (Note 8)	6	555	AA	2AA	55	555	90	X01	22C4				
	Device ID, Bottom Boot (Note 8)	6	555	AA	2AA	55	555	90	X01	2249				
	SecSi™ Sector Factory Protect	4	555	AA	2AA	55	555	90	X41	(Note 9)				
	Sector Group Protect Verify (Note 9)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
Enter SecSi Sector Region		3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 10)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 12)		1	XXX	B0										
Program/Erase Resume (Note 13)		1	XXX	30										
CFI Query (Note 14)		1	55	98										

Legend:

X = Don't care

RA = Read Address of memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A19–A15 uniquely select any sector.

Notes:

1. *See Table 1 on page 17 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells indicate read cycles. All others are write cycles.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AA as shown in table, address bits above A11 and data bits above DQ7 are don't care.*
5. *No unlock or command cycles required when device is in read mode.*
6. *Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.*
7. *Fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See Autoselect Command Sequence on page 30 for more information.*
8. *Device ID must be read in three cycles.*
9. *Data is 00h for an unprotected sector group and 01h for a protected sector group.*
10. *Unlock Bypass command is required prior to Unlock Bypass Program command.*
11. *Unlock Bypass Reset command is required to return to read mode when device is in unlock bypass mode.*
12. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.*
13. *Erase Resume command is valid only during Erase Suspend mode.*
14. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

Write Operation Status

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 12 on page 45 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

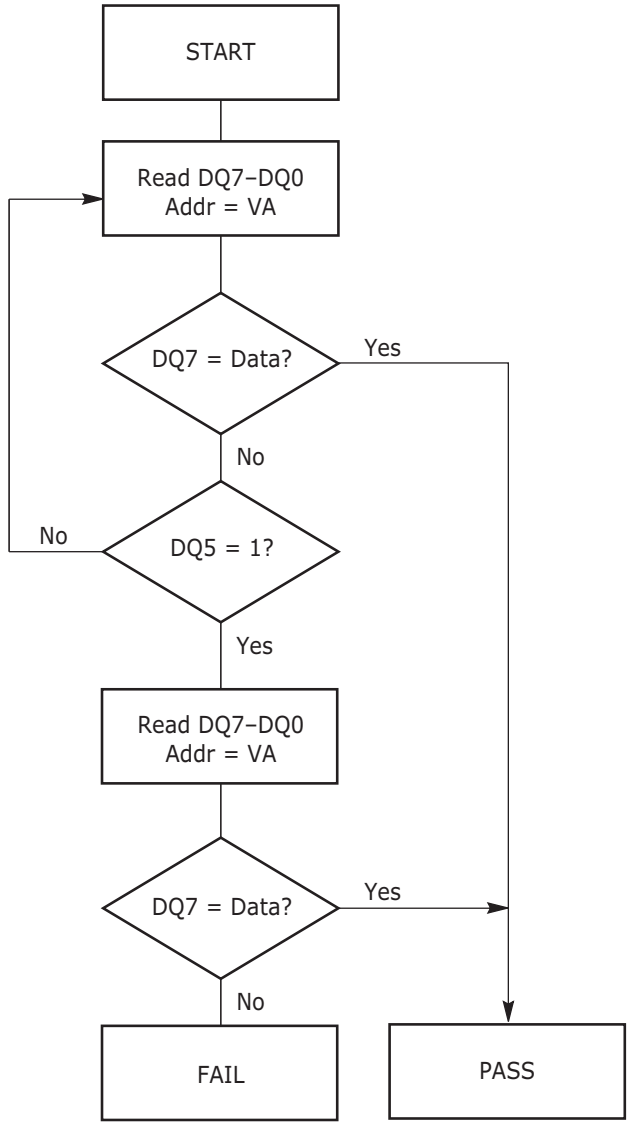
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a *0* on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a *1* on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to *1*; prior to this, the device outputs the *complement*, or *0*. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 changes from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 17, on page 52 illustrates this.

Table 12 on page 45 shows the outputs for Data# Polling on DQ7. Figure 7, on page 39 shows the Data# Polling algorithm.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.*

Figure 7. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 11 on page 43 shows the outputs for RY/BY#. Figure 13, on page 47; Figure 14, on page 48; Figure 17, on page 52; and Figure 18, on page 52 show RY/BY# for read, reset, program, and erase operations, respectively.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection *DQ7: Data# Polling on page 38*).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 12 shows the outputs for Toggle Bit I on DQ6. Figure 8, on page 42 shows the toggle bit algorithm in flowchart form, and the section *Reading Toggle Bits DQ6/DQ2 on page 41* explains the algorithm. Figure 20, on page 53 shows the toggle bit timing diagrams. Figure 21, on page 54 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection *DQ2: Toggle Bit II on page 40*.

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that were selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are

selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 11 on page 43 to compare outputs for DQ2 and DQ6.

Figure 8, on page 42 shows the toggle bit algorithm in flowchart form, and the section *Reading Toggle Bits DQ6/DQ2 on page 41* explains the algorithm. See also the *DQ6: Toggle Bit I on page 40* subsection. Figure 18, on page 52 shows the toggle bit timing diagram. Figure 19, on page 53 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 8, on page 42 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 did not go high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 8, on page 42).

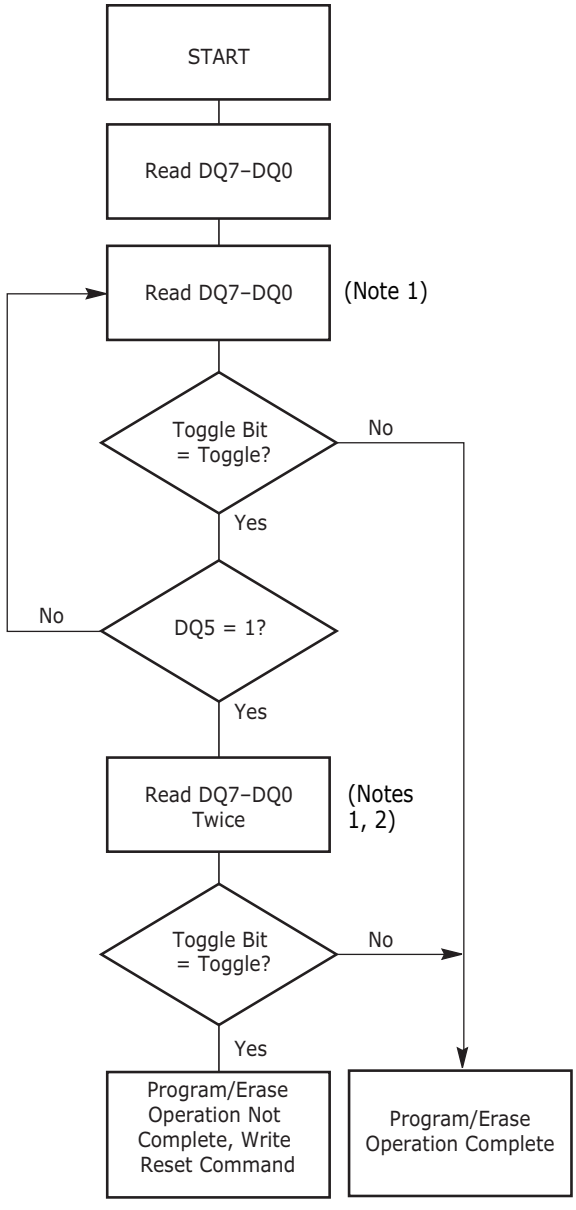


Figure 8. Toggle Bit Algorithm

Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to* 1*. See text.*

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*. This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a *1* to a location that is previously programmed to *0*. **Only an erase operation can change a *0* back to a *1*.** Under this condition, the device halts the operation, and when the operation exceeds the timing limits, DQ5 produces a *1*.

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from *0* to *1*. The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands is always less than 50 µs. See also *Sector Erase Command Sequence on page 33*.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device accepted the command sequence, and then read DQ3. If DQ3 is *1*, the internally controlled erase cycle began; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *0*, the device accepts additional sector erase commands. To ensure the command is accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 11 shows the outputs for DQ3.

Table II. Write Operation Status

Operation			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)					1
		Non-Program Suspended Sector	Data					1
Erase Suspend Mode	Reading within Erase Suspended Sector		1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector		Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to 1 when an Embedded Program or Embedded Erase operation exceeds the maximum timing limits. See DQ5: Exceeded Timing Limits on page 42 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

Absolute Maximum Ratings

Storage Temperature, Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#, and RESET# (Note 2) . . . . . –0.5 V to +12.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC}+0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 10.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

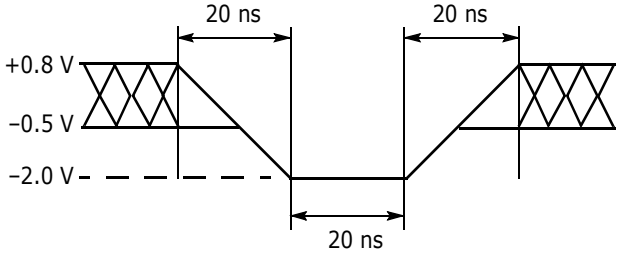


Figure 9. Maximum Negative Overshoot Waveform

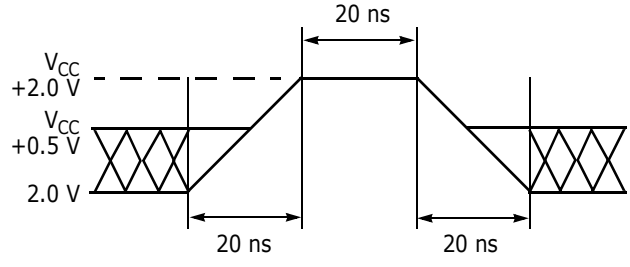


Figure 10. Maximum Positive Overshoot Waveform

Operating Ranges

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for full voltage range . . . . . 2.7 V to 3.6 V

V_{CC} for regulated range . . . . . 3.0 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics

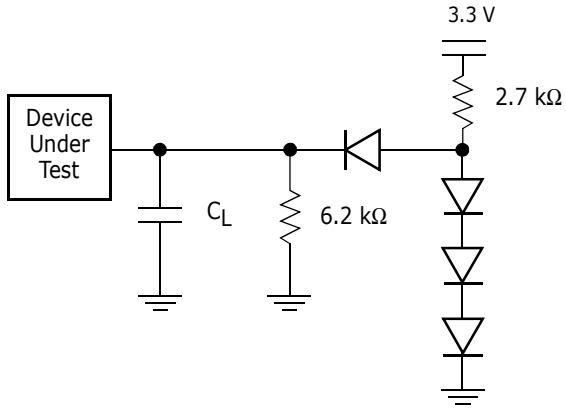
Table 12. CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	V_{CC} = $V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LR}	Reset Leakage Current	V_{CC} = $V_{CC\ max}$; RESET# = 12.5 V				35	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH},	10 MHz		35	50	mA
			5 MHz		15	20	
			1 MHz		2.5	10	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3, 5)	CE# = V_{IL}, OE# = V_{IH}			40	60	mA
I_{CC3}	V_{CC} Standby Current (Notes 2, 4)	CE#, RESET# = V_{CC} ± 0.3 V			0.4	5	µA
I_{CC4}	V_{CC} Standby Current During Reset (Notes 2, 4)	RESET# = V_{SS} ± 0.3 V			0.8	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4, 6)	V_{IH} = V_{CC} ± 0.3 V; -0.1 < V_{IL} ≤ 0.3 V			0.4	5	µA
V_{IL}	Input Low Voltage (Notes 6, 7)			-0.5		0.6	V
V_{IH}	Input High Voltage (Notes 6, 7)			0.7 V_{CC}		V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, V_{CC} = $V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA, V_{CC} = $V_{CC\ min}$		0.85 x V_{CC}			V
V_{OH2}		I_{OH} = -100 µA, V_{CC} = $V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.*
2. *Maximum I_{CC} specifications are tested with V_{CC} = V_{CC}max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *At extended temperature range (>+85°C), typical current is 5 µA and maximum current is 10 µA.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*
6. *Not 100% tested.*
7. *V_{CC} voltage requirements.*

Test Conditions



Note: *Diodes are IN3064 or equivalent*

Figure 11. Test Setup

Table 13. Test Specifications

Test Condition	90, 100	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0 or V_{CC}	V
Input timing measurement reference levels	0.5 V_{CC}	V
Output timing measurement reference levels	0.5 V_{CC}	V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

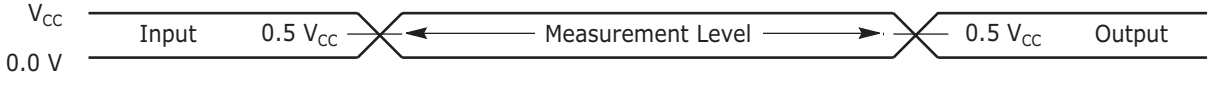


Figure 12. Input Waveforms and Measurement Levels

AC Characteristics

Table 14. Read Operations

Parameter		Description		Test Setup		Speed Options		Unit
JEDEC	Std					90	100	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	90	100	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	90	100	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	90	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25		ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	20		ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	20		ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0		ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11, on page 46 and Table 13 on page 46 for test specifications.*

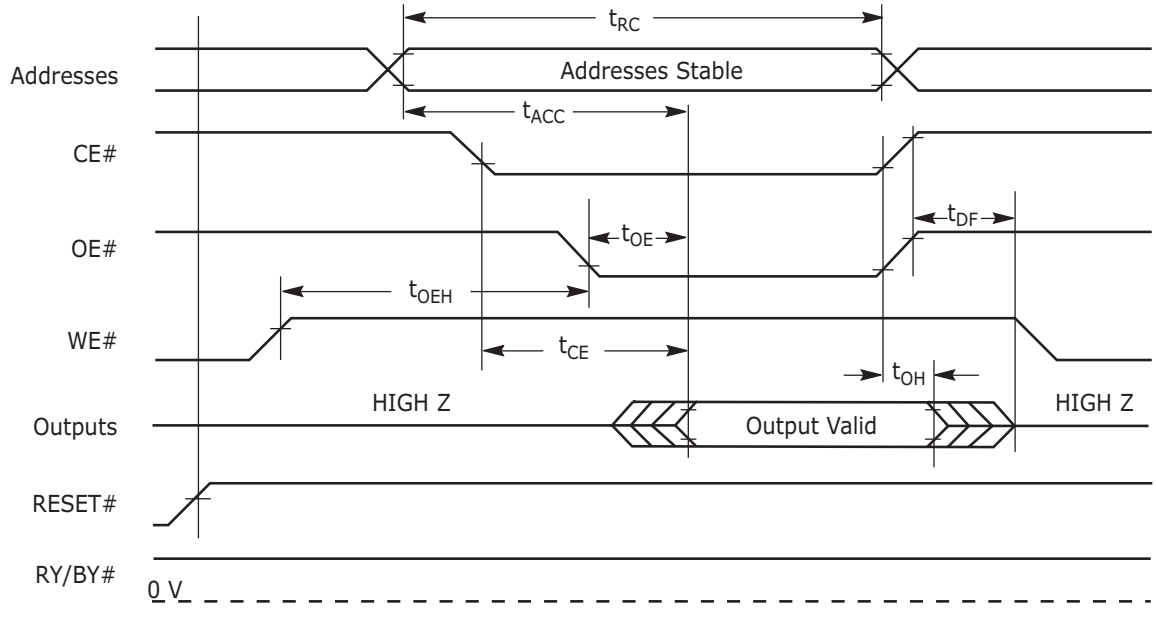


Figure 13. Read Operations Timings

AC Characteristics

Table 15. Hardware Reset (RESET#)

Parameter		Description	Test Setup	All Speed Options	Unit
JEDEC	Std				
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)	Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

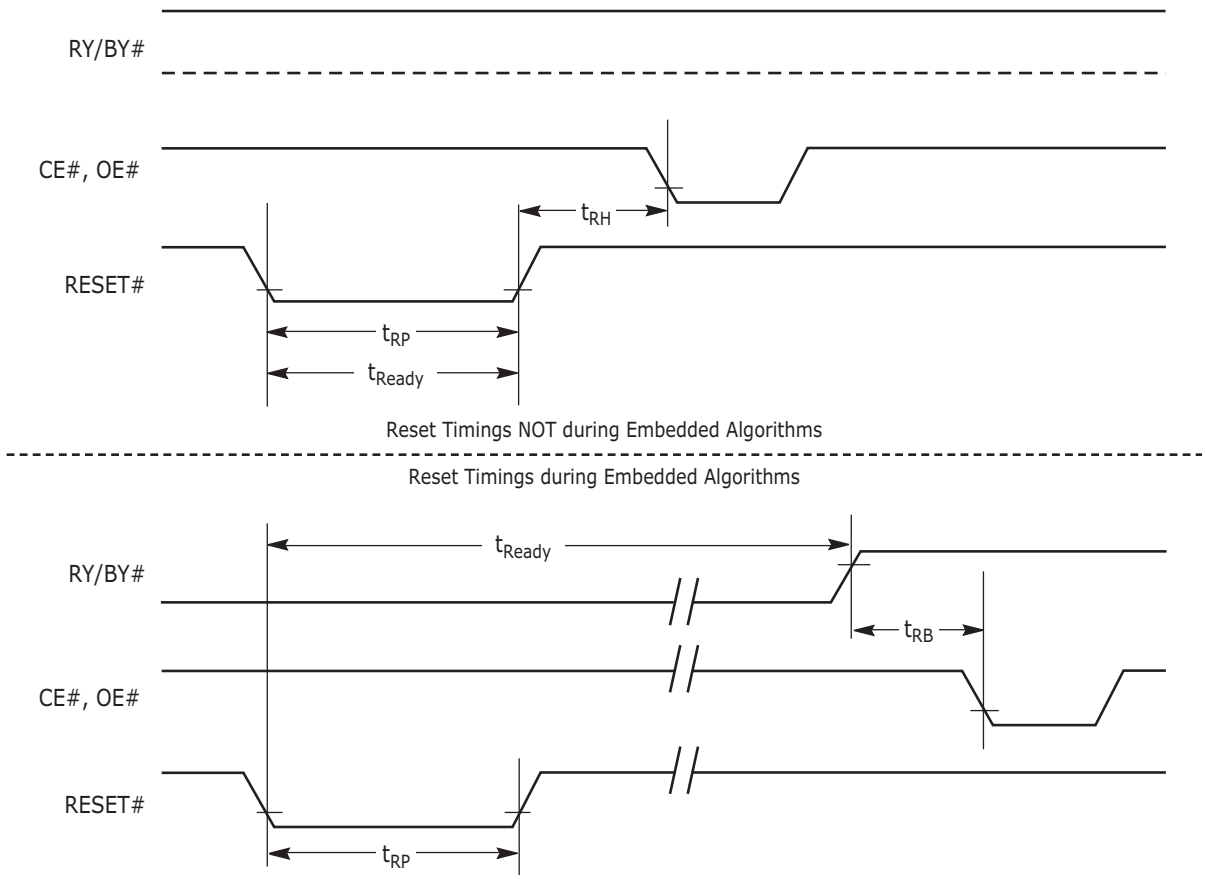


Figure 14. RESET# Timings

AC Characteristics

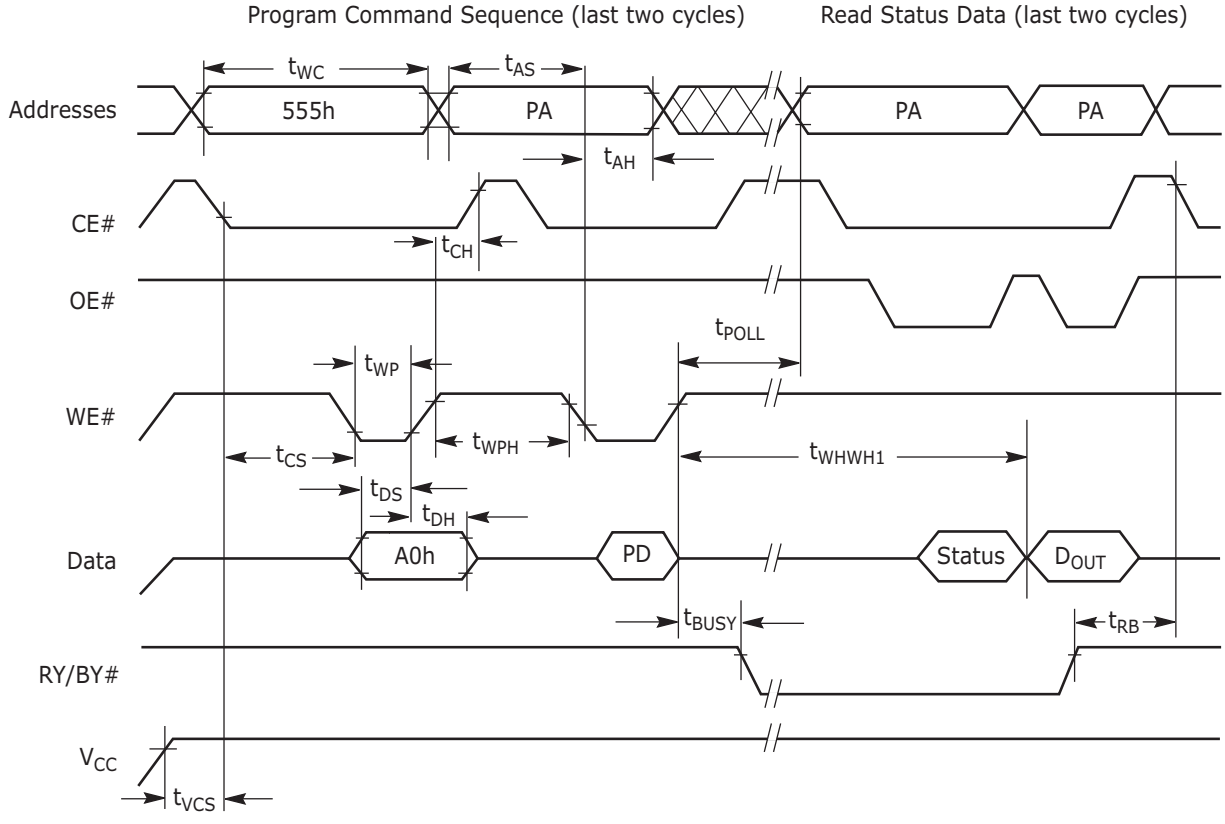
Erase/Program Operations

Parameter		Description		Speed Options		Unit
JEDEC	Std			90	100	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	100	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45		ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35		ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
	t_{OES}	Output Enable Setup Time	Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35		ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	18		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1		sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50		µs
	t_{RB}	Recovery Time from RY/BY#	Min	0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Max	90	100	ns
	t_{POLL}	Program Valid Before Status Polling (Note 3)	Max	4		µs

Notes:

1. *Not 100% tested.*
2. *See Table 18 on page 57 for more information.*
3. *If a program suspend command is issued within t_{POLL}, the device requires t_{POLL} before reading status data, once programming resumes (that is, the program resume command is written). If the suspend command was issued after t_{POLL}, status data is available immediately after programming resumes. See Figure 15, on page 50.*

AC Characteristics

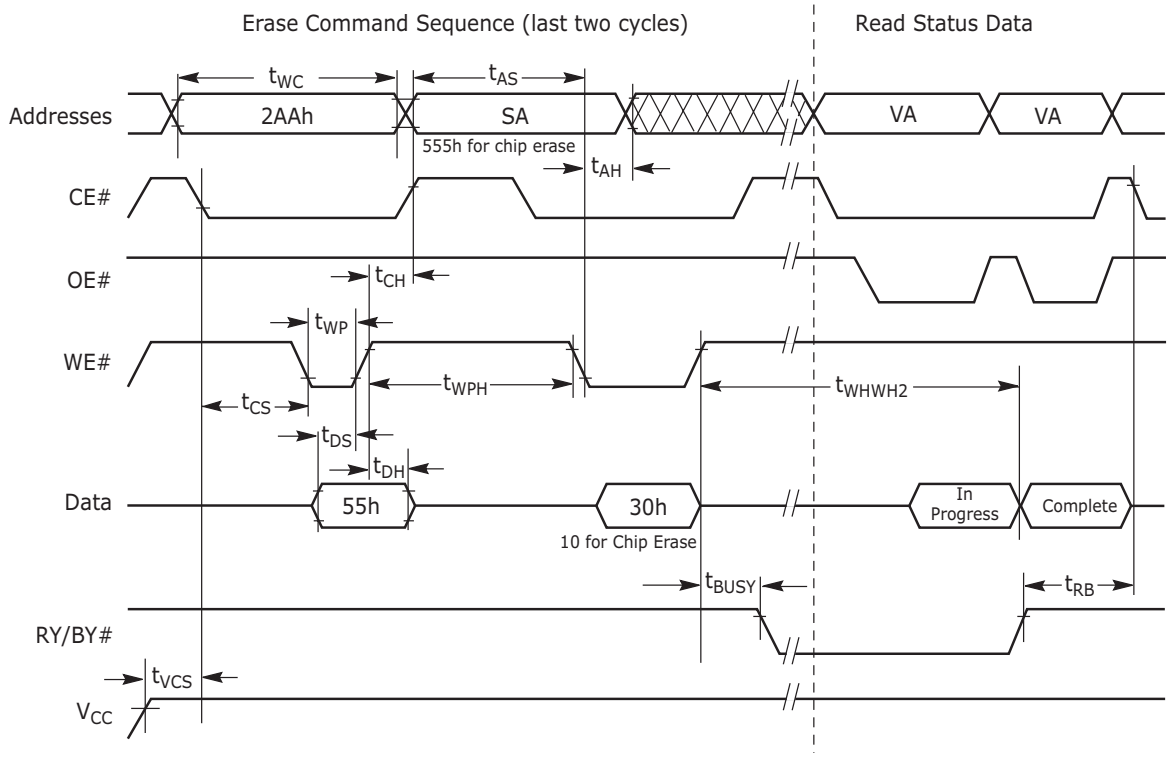


Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 15. Program Operation Timings

AC Characteristics

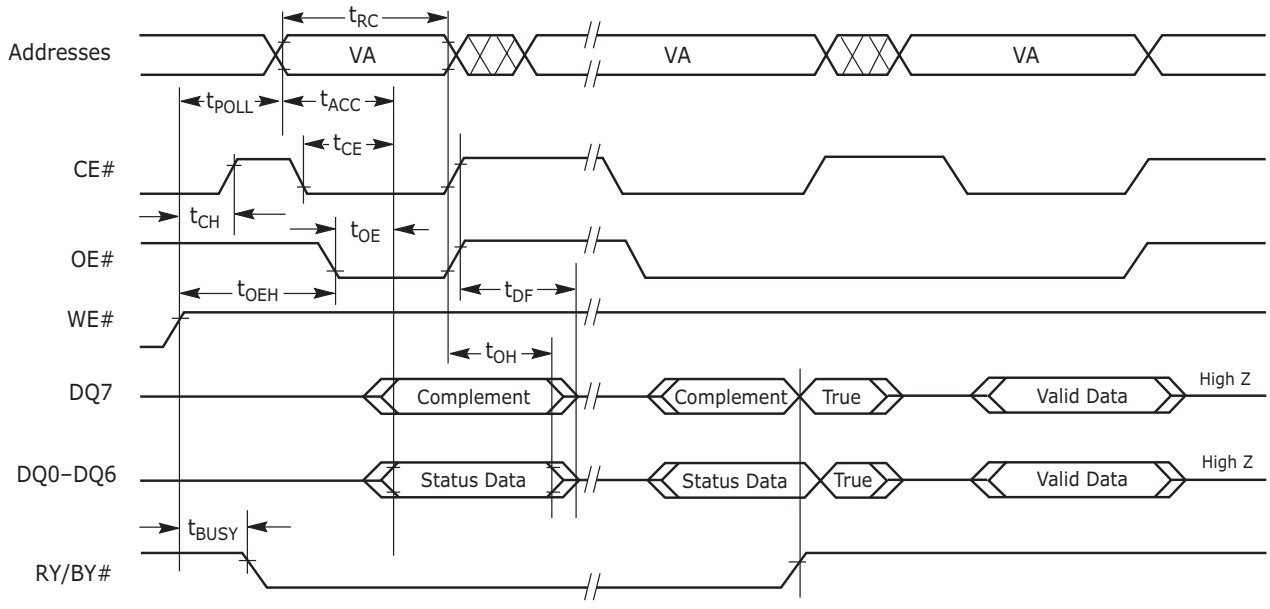


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status on page 38).*
2. *Illustration shows device in word mode.*

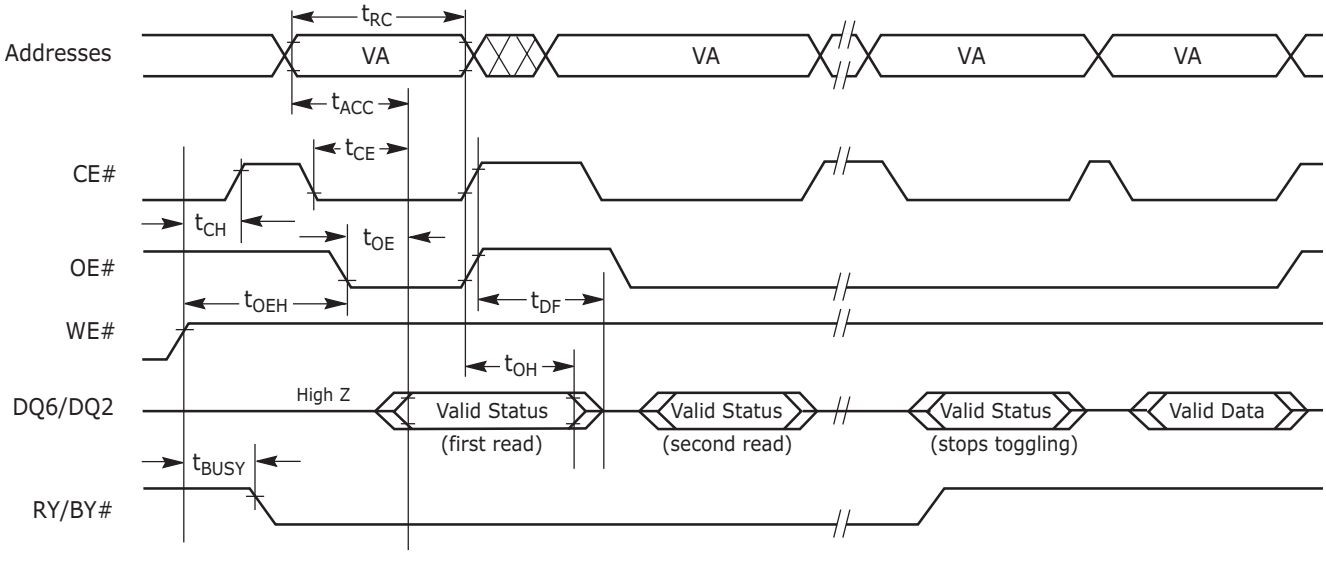
Figure 16. Chip/Sector Erase Operation Timings

AC Characteristics



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

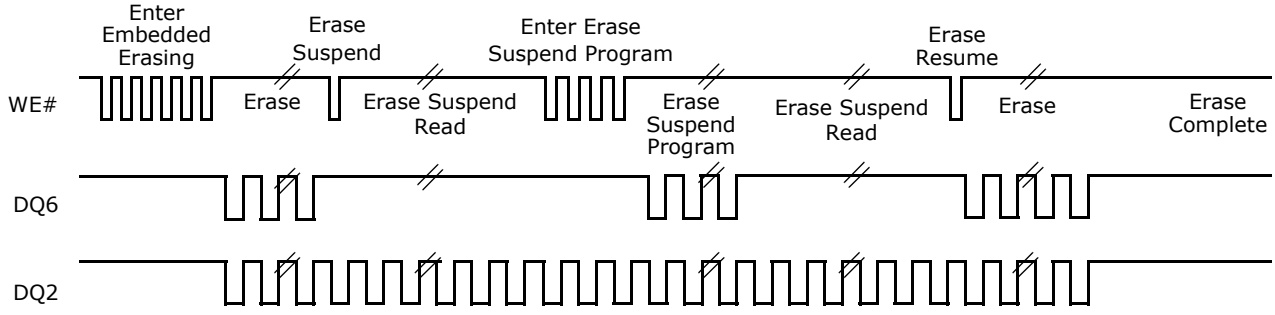
Figure I7. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure I8. Toggle Bit Timings (During Embedded Algorithms)

AC Characteristics



Note: *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

Figure 19. DQ2 vs. DQ6 for Erase and Erase Suspend Operations

Table 16. Temporary Sector Unprotect

Parameter					
JEDEC	**Std**	**Description**		**All Speed Options**	**Unit**
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

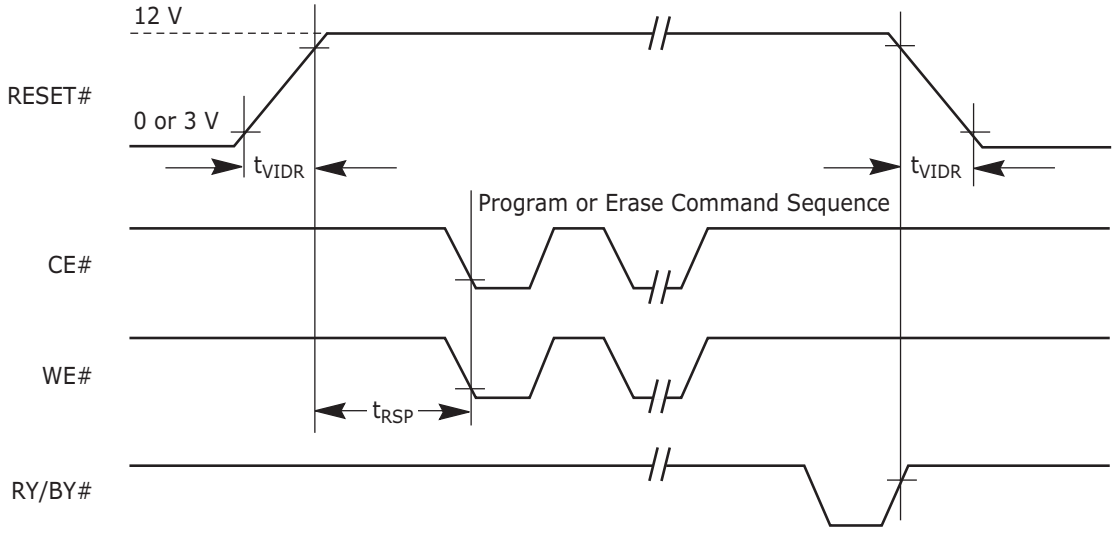
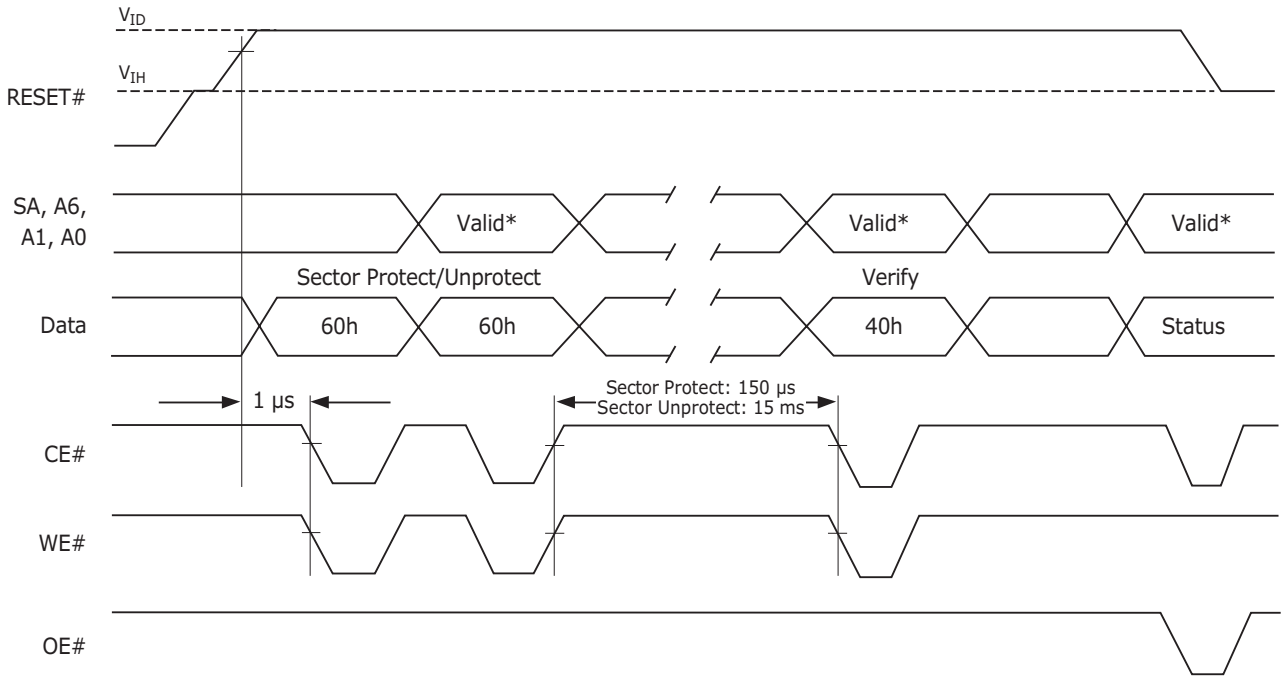


Figure 20. Temporary Sector Unprotect/Timing Diagram

AC Characteristics



Note: *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 21. Sector Protect/Unprotect Timing Diagram

AC Characteristics

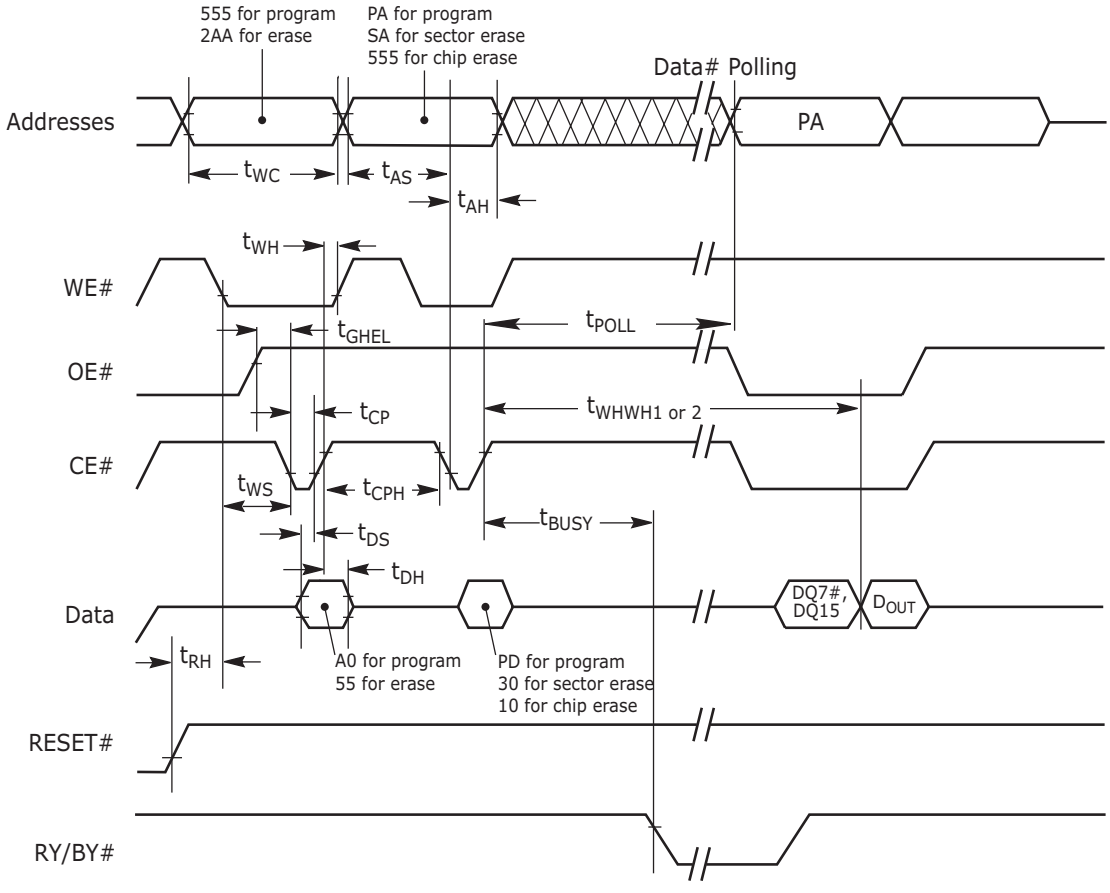
Table 17. Alternate CD# Controlled Erase/Program Operations

Parameter		Description		Speed Options		Unit
JEDEC	Std			90	100	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	100	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45		ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35		ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0		ns
	t_{OES}	Output Enable Setup Time	Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35		ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	25		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	18		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.7		sec
	t_{RH}	RESET# High Time Before Write	Min	50		ns
	t_{POLL}	Program Valid Before Status Polling (Note 3)	Max	4		µs

Notes:

1. *Not 100% tested.*
2. *See Table 18 on page 57 for more information.*
3. *If a program suspend command is issued within t_{POLL}, the device requires t_{POLL} before reading status data, once programming resumes (that is, the program resume command is written). If the suspend command was issued after t_{POLL}, status data is available immediately after programming resumes. See Figure 22, on page 56.*

AC Characteristics



Notes:

1. *PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*
3. *Word mode address used as an example.*

Figure 22. Alternate CE# Controlled Write Operation Timings

Table 18. Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.7	7.5	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		32		s	
Word Programming Time		18		µs	Excludes system level overhead (Note 5)
Chip Programming Time (Note 3)	Word Mode	19		s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0 V, 10,000 cycles, checkerboard data pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 2 on page 20 and Table 3 on page 21 for further information on command definitions.*

Table 19. TSOP Pin and BGA Package Capcitance

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			BGA	3.9	4.7	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

Type 4 pSRAM

4 Mbit (256K x 16)

Features

- Wide voltage range: 2.7V to 3.3V
- Typical active current: 3 mA @ f = 1 MHz
- Low standby power
- Automatic power-down when deselected

Functional Description

The Type 4 pSRAM is a high-performance CMOS pseudo static RAM (pSRAM) organized as 256K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. The device can be put into standby mode reducing power consumption dramatically when deselected (CE1# Low, CE2 High or both BHE# and BLE# are High). The input/output pins (I/O0 through I/O15) are placed in a high-impedance state when: deselected (CE1# High, CE2 Low, OE# is deasserted High), or during a write operation (Chip Enabled and Write Enable WE# Low). Reading from the device is accomplished by asserting the Chip Enables (CE1# Low and CE2 High) and Output Enable (OE#) Low while forcing the Write Enable (WE#) High. If Byte Low Enable (BLE#) is Low, then data from the memory location specified by the address pins will appear on I/O0 to I/O7. If Byte High Enable (BHE#) is Low, then data from memory will appear on I/O8 to I/O15. See Table 22 for a complete description of read and write modes.

Product Portfolio

V_{CC} Range (V)			Speed (ns)	Power Dissipation					
				Operating, I_{CC} (mA)				Standby (I_{SB2}) (µA)	
				f = 1 MHz		f = f_{max}			
Min	Typ	Max		Typ. (note 1)	Max	Typ. (note 1)	Max	Typ. (note 1)	Max
2.7V	3.0V	3.3V	70 ns	3	5	TBD	25 mA	15	40

Notes:

1. *Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (typ) and T_A = 25°C.*

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature . . . . . -65°C to +150°C
Ambient Temperature with Power Applied . . . . . -40°C to +85°C
Supply Voltage to Ground Potential . . . . . -0.4V to 4.6V
DC Voltage Applied to Outputs in High-Z State (note 1, 2, 3) . . . . . -0.4V to 3.7V
DC Input Voltage (note 1, 2, 3) . . . . . -0.4V to 3.7V
Output Current into Outputs (Low). . . . . 20 mA
Static Discharge Voltage . . . . . >2001V (per MIL-STD-883, Method 3015)
Latch-up Current . . . . . >200 mA

Notes:

1. *$V_{IH(MAX)} = V_{CC} + 0.5V$ for pulse durations less than 20 ns.*
2. *$V_{IL(MIN)} = -0.5V$ for pulse durations less than 20 ns.*
3. *Overshoot and undershoot specifications are characterized and are not 100% tested.*

Operating Range

Ambient Temperature (T_A)	V_{CC}
-25°C to +85°C	2.7V to 3.3V

Table 20. DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		Min.	Typ. (note 1)	Max	Unit
V_{CC}	Supply Voltage			2.7		3.3	V
V_{OH}	Output High Voltage	$I_{OH} = -1.0$ mA		V_{CC} - 0.4			
V_{OL}	Output Low Voltage	$I_{OL} = 0.1$ mA				0.4	
V_{IH}	Input High Voltage			0.8 * V_{CC}		V_{CC} + 0.4	
V_{IL}	Input Low Voltage	F = 0		-0.4		0.4	
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		-1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		-1		+1	
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = 3.3V, I_{OUT} = 0 mA, CMOS Levels		TBD	15	mA
		f = 1 MHz				3	
I_{SB1}	Automatic CE# Power-Down Current—CMOS Inputs	CE# ≥ V_{CC} – 0.2V, CE2 ≤ 0.2V V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V, f = f_{max} (Address and Data Only), f=0 (OE#, WE#, BHE# and BLE#)				250	µA
I_{SB2}	Automatic CE# Power-Down Current—CMOS Inputs	CE# ≥ V_{CC} – 0.2V, CE2 ≤ 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.3V				40	

Notes:

1. *Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25°C.*

Capacitance

Parameter	Description	Test Condition	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ.)}$	8	pF
C_{OUT}	Output Capacitance		8	

Note: *Tested initially and after any design or process changes that may affect these parameters.*

Thermal Resistance

Parameter	Description	Test Conditions	VFBGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	55	°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		17	

Note: *Tested initially and after any design or process changes that may affect these parameters.*

AC Test Loads and Waveforms

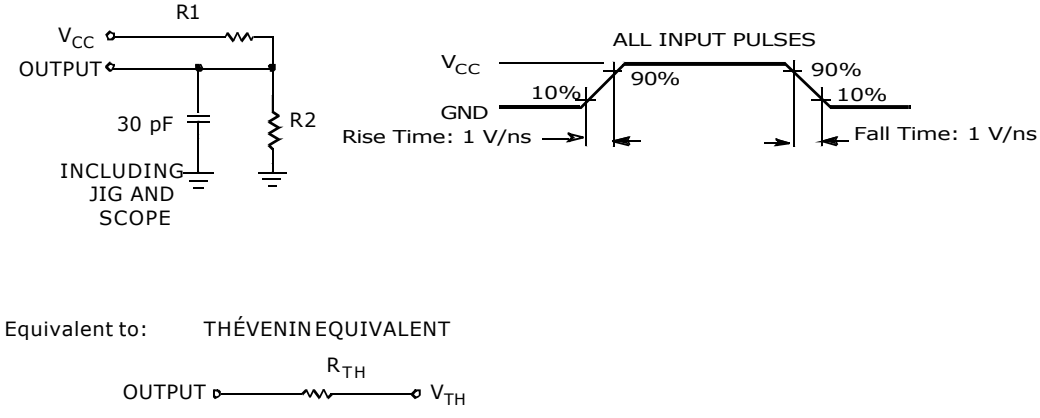


Figure 23. AC Test Loads and Waveforms

Parameters	3.0V V_{CC}	Unit
R1	22000	Ω
R2	22000	
R_{TH}	11000	
V_{TH}	1.50	V

Table 21. Switching Characteristics

Parameter	Description	Min	Max	Unit
Read Cycle				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	
t_{OHA}	Data Hold from Address Change	10		
t_{ACE}	CE#1 Low and CE2 High to Data Valid		70	
t_{DOE}	OE# Low to Data Valid		35	
t_{LZOE}	OE# Low to Low Z (note 2, 3)	5		
t_{HZOE}	OE# High to High Z (note 2, 3)		25	
t_{LZCE}	CE#1 Low and CE2 High to Low Z (note 2, 3)	5		
t_{HZCE}	CE#1 High and CE2 Low to High Z (note 2, 3)		25	
t_{DBE}	BHE# / BLE# Low to Data Valid		70	
t_{LZBE}	BHE# / BLE# Low to Low Z (note 2, 3)	5		
t_{HZBE}	BHE# / BLE# High to High Z (note 2, 3)		25	
t_{SK} (note 4)	Address Skew		10	
Write Cycle (note 5)				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	CE#1 Low an CE2 High to Write End	55		
t_{AW}	Address Set-Up to Write End	55		
t_{HA}	Address Hold from Write End	0		
t_{SA}	Address Set-Up to Write Start	0		
t_{PWE}	WE# Pulse Width	55		
t_{BW}	BLE# / BHE# LOW to Write End	55		
t_{SD}	Data Set-up to Write End	25		
t_{HD}	Data Hold from Write End	0		
t_{HZWE}	WE# Low to High Z (note 2, 3)		25	
t_{LZWE}	WE# High to Low Z (note 2, 3)	5		

Notes:

1. *Test conditions assume signal transition time of 1V/ns or higher, timing reference levels of $V_{CC(typ.)}$ /2, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.*
2. *t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.*
3. *High-Z and Low-Z parameters are characterized and are not 100% tested.*
4. *To achieve 55-ns performance, the read access should be CE# controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.*
5. *The internal write time of the memory is defined by the overlap of WE#, CE#1 = V_{IL}, CE2 = V_{IH}, B_{HE} and/or B_{LE} =V_{IL}. All signals must be Active to initiate a write and any of these signals can terminate a write by going Inactive. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.*

Switching Waveforms

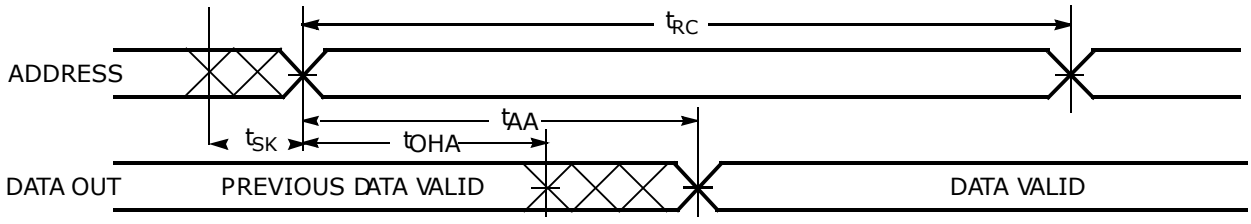


Figure 24. Read Cycle I (Address Transition Controlled)

Notes:

1. *To achieve 55-ns performance, the read access should be CE# controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.*
2. *Device is continuously selected. OE#, CE# = V_{IL}.*
3. *WE# is High for Read Cycle.*

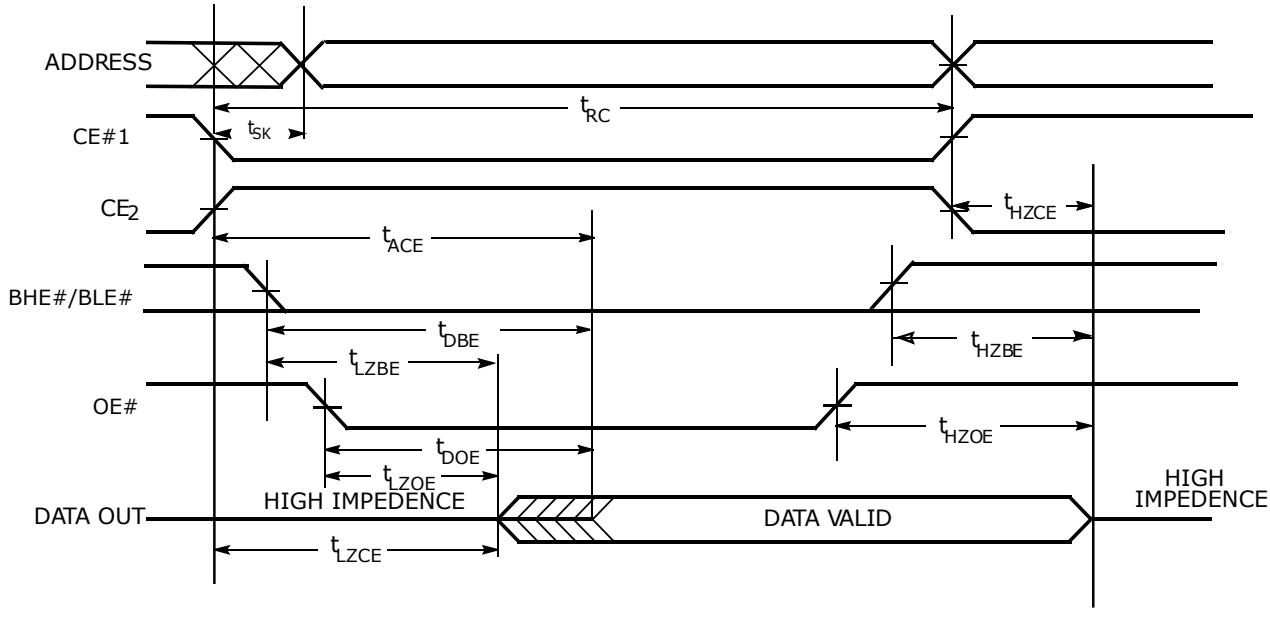


Figure 25. Read Cycle 2 (OE# Controlled)

Notes:

1. *To achieve 55-ns performance, the read access should be CE# controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.*
2. *WE# is High for Read Cycle.*

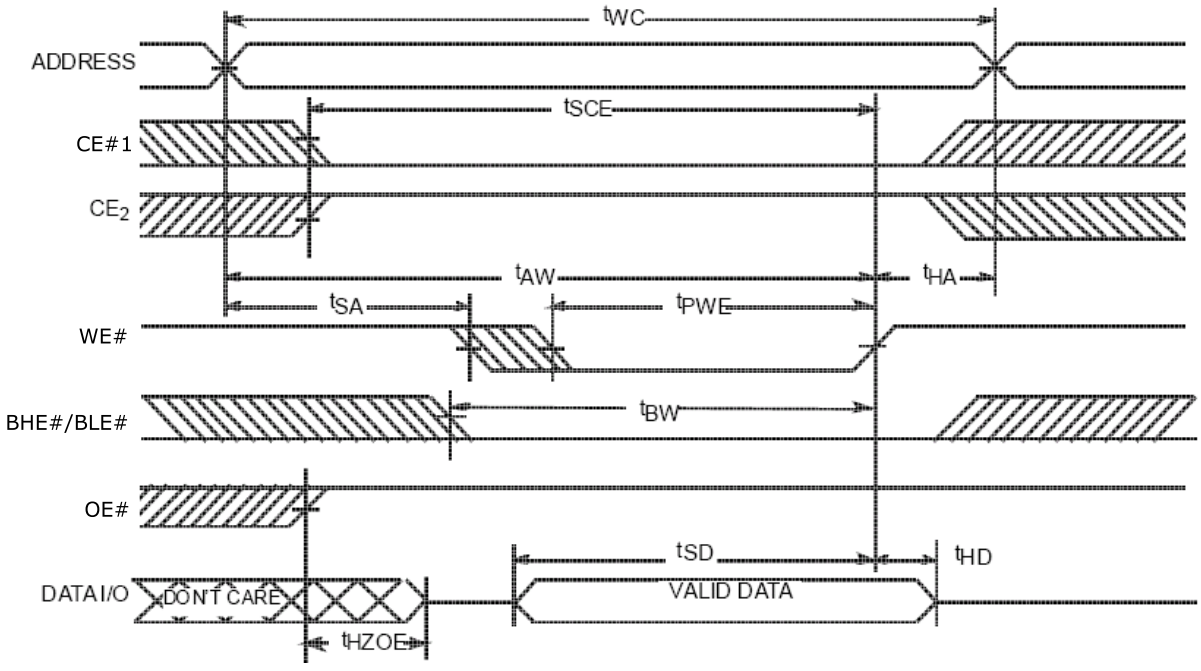


Figure 26. Write Cycle I (WE# Controlled)

Notes:

1. *High-Z and Low-Z parameters are characterized and are not 100% tested.*
2. *The internal write time of the memory is defined by the overlap of WE#, CE#1 = V_{IL}, CE2 = V_{IH}, B_{HE} and/or B_{LE} =V_{IL}. All signals must be Active to initiate a write and any of these signals can terminate a write by going Inactive. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.*
3. *Data I/O is high impedance if OE# $\geq V_{IH}$.*
4. *If Chip Enable goes Inactive simultaneously with WE# = High, the output remains in a high-impedance state.*
5. *During the Don't Care period in the Data I/O waveform, the I/Os are in output state and input signals should not be applied.*

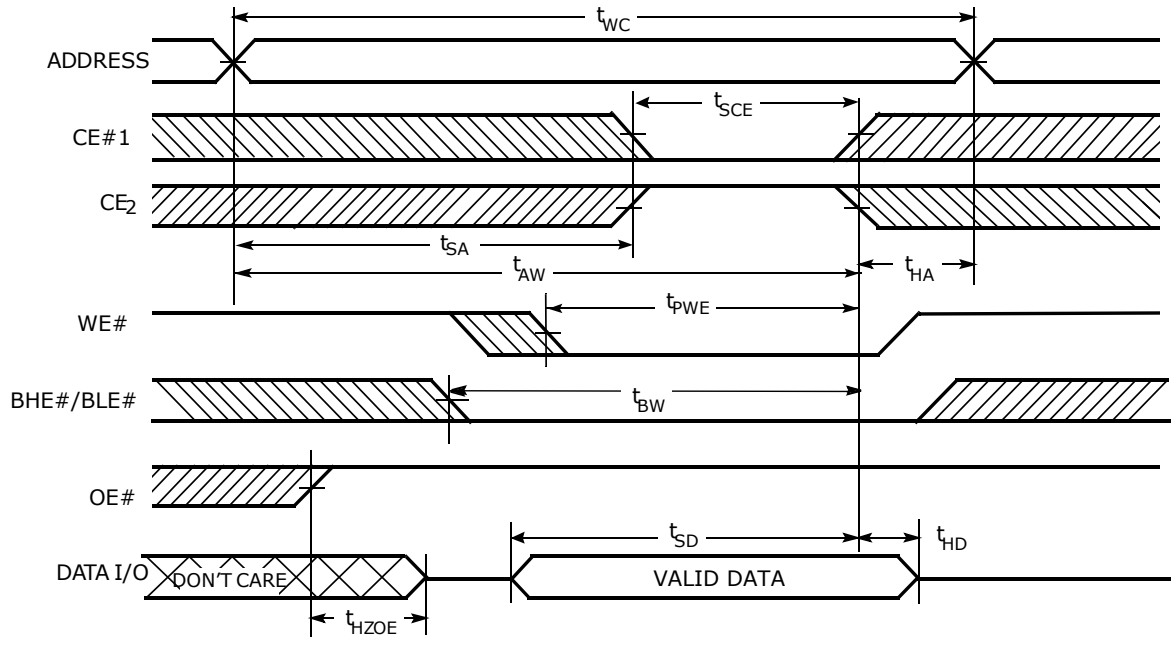


Figure 27. Write Cycle 2 (CE#I or CE2 Controlled)

Notes:

1. *High-Z and Low-Z parameters are characterized and are not 100% tested.*
2. *The internal write time of the memory is defined by the overlap of WE#, CE#1 = V_{IL}, CE2 = V_{IH}, B_{HE} and/or B_{LE} =V_{IL}. All signals must be Active to initiate a write and any of these signals can terminate a write by going Inactive. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.*
3. *Data I/O is high impedance if OE# $\geq V_{IH}$.*
4. *If Chip Enable goes Inactive simultaneously with WE# = High, the output remains in a high-impedance state.*
5. *During the Don't Care period in the Data I/O waveform, the I/Os are in output state and input signals should not be applied.*

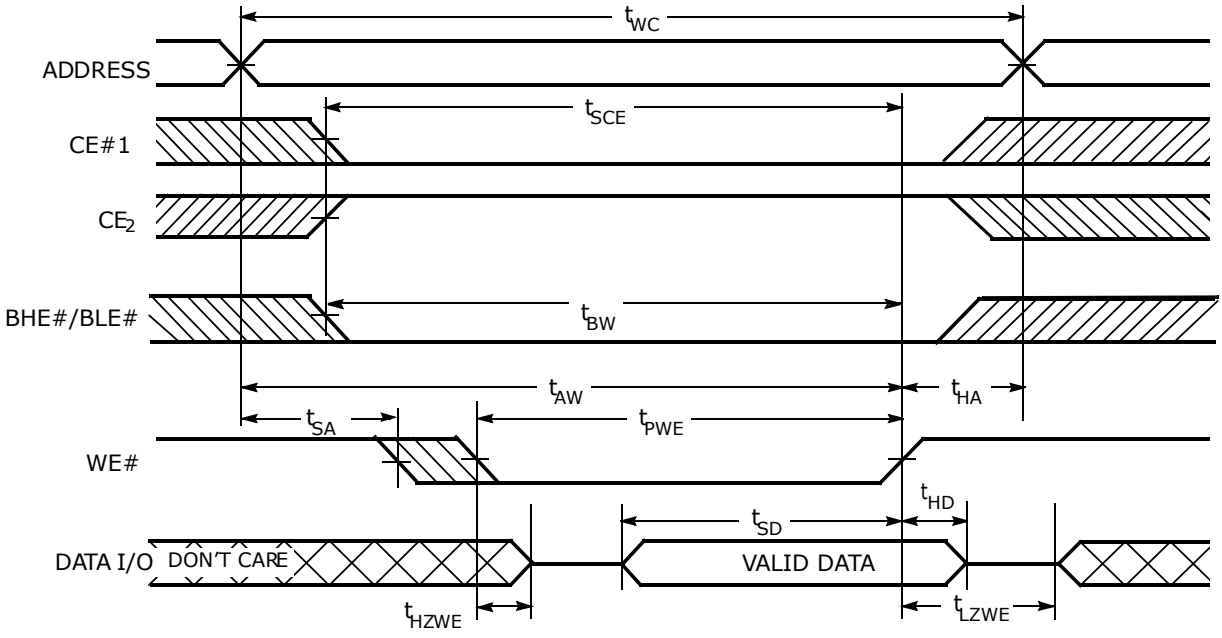


Figure 28. Write Cycle 3 (WE# Controlled, OE# Low)

Notes:

1. *If Chip Enable goes Inactive simultaneously with WE# = High, the output remains in a high-impedance state.*
2. *During the Don't Care period in the Data I/O waveform, the I/Os are in output state and input signals should not be applied.*

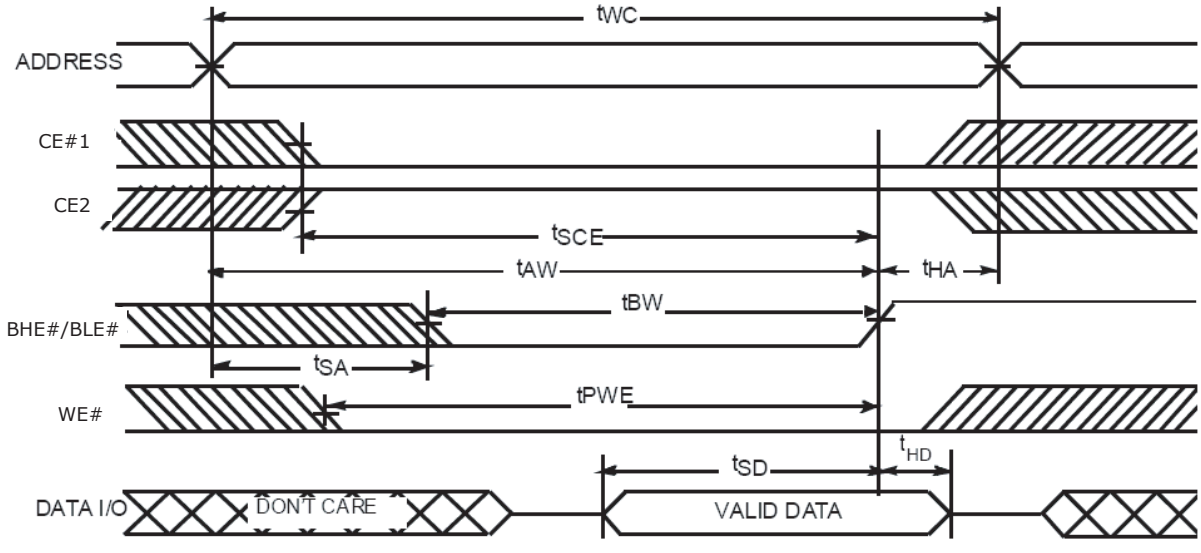


Figure 29. Write Cycle 4 (BHE#/BLE# Controlled, OE# Low)

Notes:

1. *If Chip Enable goes Inactive simultaneously with WE# = High, the output remains in a high-impedance state.*
2. *During the Don't Care period in the Data I/O waveform, the I/Os are in output state and input signals should not be applied.*

Truth Table

Table 22. Truth Table

CE#1	CE2	WE#	OE#	BHE#	BLE#	Inputs / Outputs	Mode	Power
H	X	X	X	X	X	High-Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High-Z		
X	X	X	X	H	H	High-Z		
L	H	H	L	L	L	Data Out (I/O0–I/O15)	Read (Upper Byte and Lower Byte)	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O0 –I/O7); I/O8–I/O15 in High Z	Read (Upper Byte only)	
L	H	H	L	L	H	Data Out (I/O8–I/O15); I/O0–I/O7 in High Z	Read (Lower Byte only)	
L	H	H	H	L	L	High-Z	Output Disabled	
L	H	H	H	H	L	High-Z	Output Disabled	
L	H	H	H	L	H	High-Z	Output Disabled	
L	H	L	X	L	L	Data In (I/O0–I/O15)	Write (Upper Byte and Lower Byte)	
L	H	L	X	H	L	Data In (I/O0–I/O7); I/O8–I/O15 in High Z	Write (Lower Byte Only)	
L	H	L	X	L	H	Data In (I/O8–I/O15); I/O0 –I/O7 in High Z	Write (Upper Byte Only)	

Revision Summary

Revision A 0 (February 23, 2005)

Initial release.

Colophon

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