# 36Mb Sync. Pipelined Burst SRAM Specification

## Document Title

**1Mx36 & 2Mx18 Bit Synchronous Pipelined Burst SRAM**

## Revision History

| Rev. No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.0 | Initial Draft | Nov. 2012 | Preliminary |
| 1.0 | Add Current Value | Jan. 2013 | Final |
| 1.1 | Add 165FBGA information | Mar. 2013 | Final |
| 1.2 | Add 1.8V Vdd support | Nov. 2014 | Final |
| 1.3 | Correct typo in ordering information<br>S7A32xx31M => S7A32xx30M | May 2017 | Final |

# 1Mx36 & 2Mx18 Bit Synchronous Pipelined Burst SRAM

## Features

- $V_{DD}$ = 1.8V (1.7V ~ 2.0V) or
  2.5V (2.3V ~ 2.7V) or
  3.3V (3.1V ~ 3.5V) Power Supply
- $V_{DDQ}$ = 1.7V ~ 2.0V I/O Power Supply (VDD=1.8V) or
  2.3V ~ 2.7V I/O Power Supply (VDD=2.5V) or
  2.3V ~ 3.5V I/O Power Supply (VDD=3.3V)
- Synchronous Operation
- 2 Stage Pipelined operation with 4 Burst
- On-Chip Address Counter
- Self-Timed Write Cycle
- On-Chip Address and Control Registers
- Byte Writable Function
- Global Write Enable Controls a full bus-width write
- Power Down State via ZZ Signal
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP ; 2cycle Enable, 1cycle Disable
- Asynchronous Output Enable Control
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins
- TTL-Level Three-State Output
- Operating in commeical and industrial temperature range
- 100-TQFP-1420A (Lead free package)
- 165FBGA(11x15 ball array) with body size of 13mmx15mm. (Lead free package)

## General Description

The S7A323630M and S7A321830M are 32,748,736-bit Synchronous Static Random Access Memory designed for high performance.

It is organized as 1M(2M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The S7A323630M and S7A321830M are fabricated using high performance CMOS technology and is available in a 100pin TQFP package and 165FBGA package. Multiple power and ground pins are utilized to minimize ground bounce.

## Key Parameters

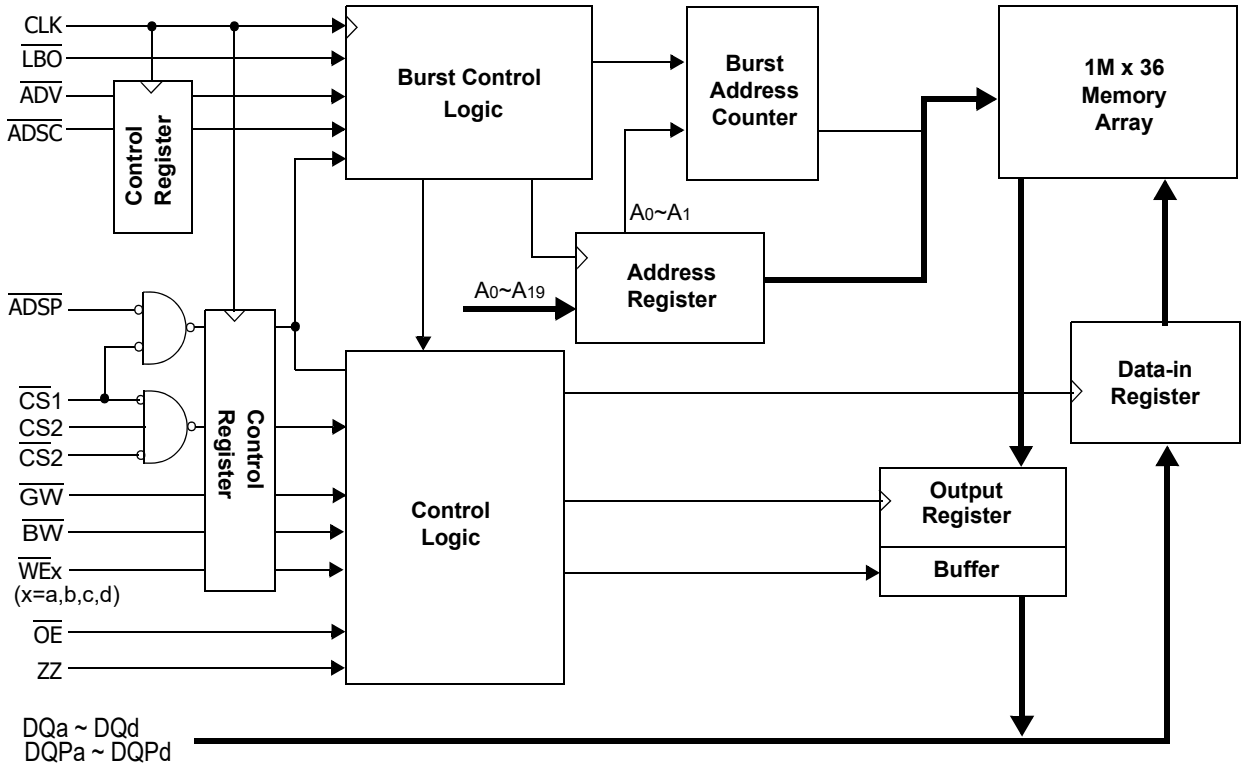
| Parameter | Symbol | -25 | -16 | Unit |
|---|---|---|---|---|
| Cycle Time | tCYC | 4.0 | 6.0 | ns |
| Clock Access Time | tCD | 2.6 | 3.5 | ns |
| Output Enable Access Time | tOE | 2.6 | 3.5 | ns |
| Operating Current | $I_{CC}$ | 300 | 260 | mA |
| Standby Current | $I_{SB2}$ | 120 | 120 | mA |

## 36Mb Synchronous Pipelined Burst SRAM Ordering Information

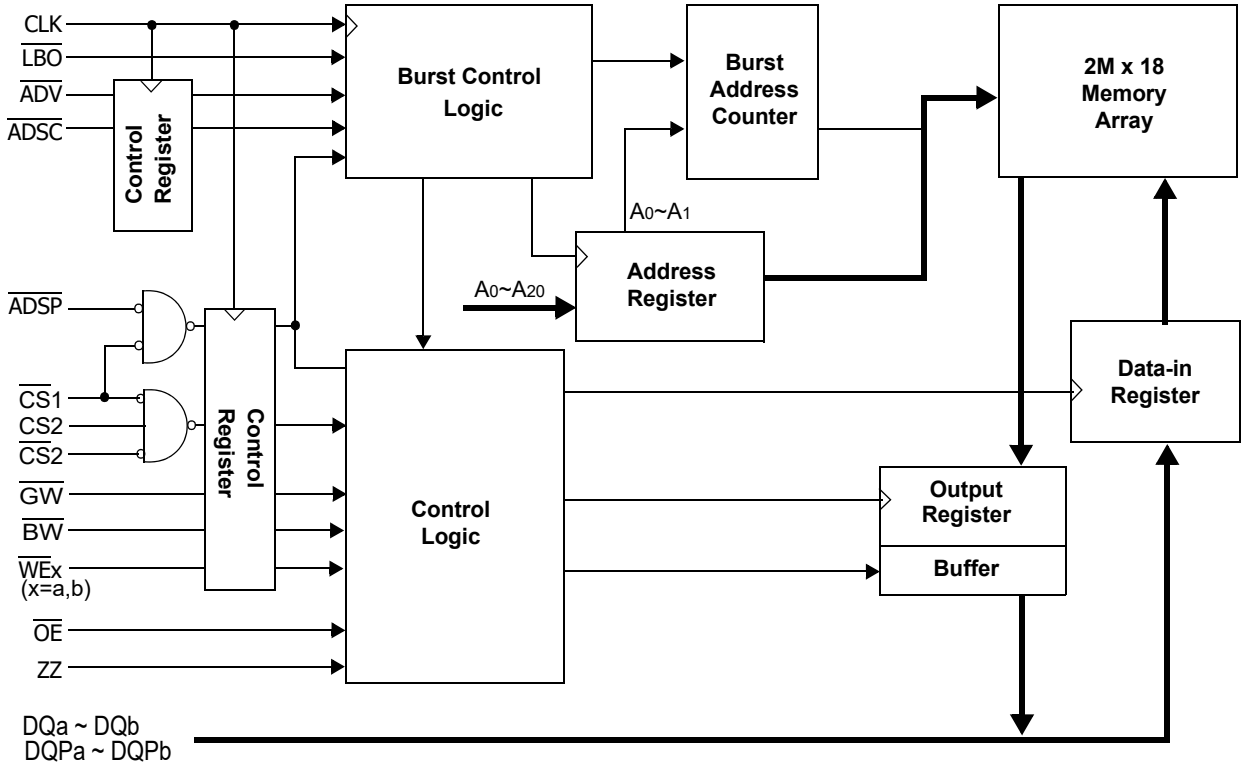
| Org. | VDD (V) | Speed (ns) | Access Time (ns) | Part Number | RoHS Avail. |
|---|---|---|---|---|---|
| 2Mx18 | 1.8 | 4.0 | 3.0 | S7A321830M-P(E)C(I)25 | O |
| | 3.3/2.5 | 4.0 | 2.6 | S7A321830M-P(E)C(I)25 | O |
| | 3.3/2.5/1.8 | 6.0 | 3.5 | S7A321830M-P(E)C(I)16 | O |
| 1Mx36 | 1.8 | 4.0 | 3.0 | S7A323630M-P(E)C(I)25 | O |
| | 3.3/2.5 | 4.0 | 2.6 | S7A323630M-P(E)C(I)25 | O |
| | 3.3/2.5/1.8 | 6.0 | 3.5 | S7A323630M-P(E)C(I)16 | O |

Note 1. P(E) [Package type] : P - 100TQFP Pb Free, E - 165FBGA Pb Free
2. C(I) [Operating Temperature] : C-Commercial, I-Industrial

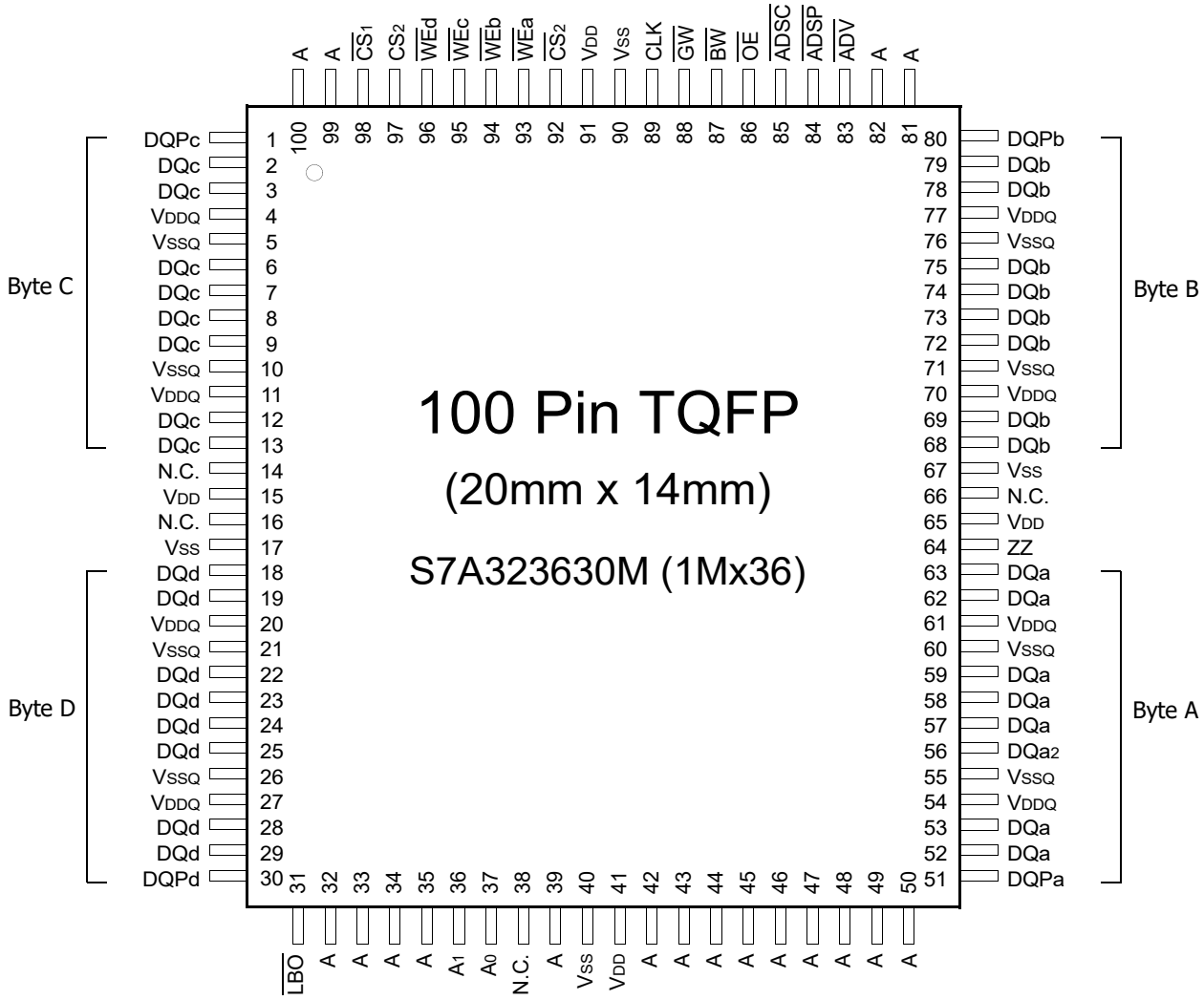
## Logic Block Diagram - S7A323630M (1M x 36)




## Logic Block Diagram - S7A321830M (2M x 18)



## 100 TQFP Package Pin Configurations(Top View)

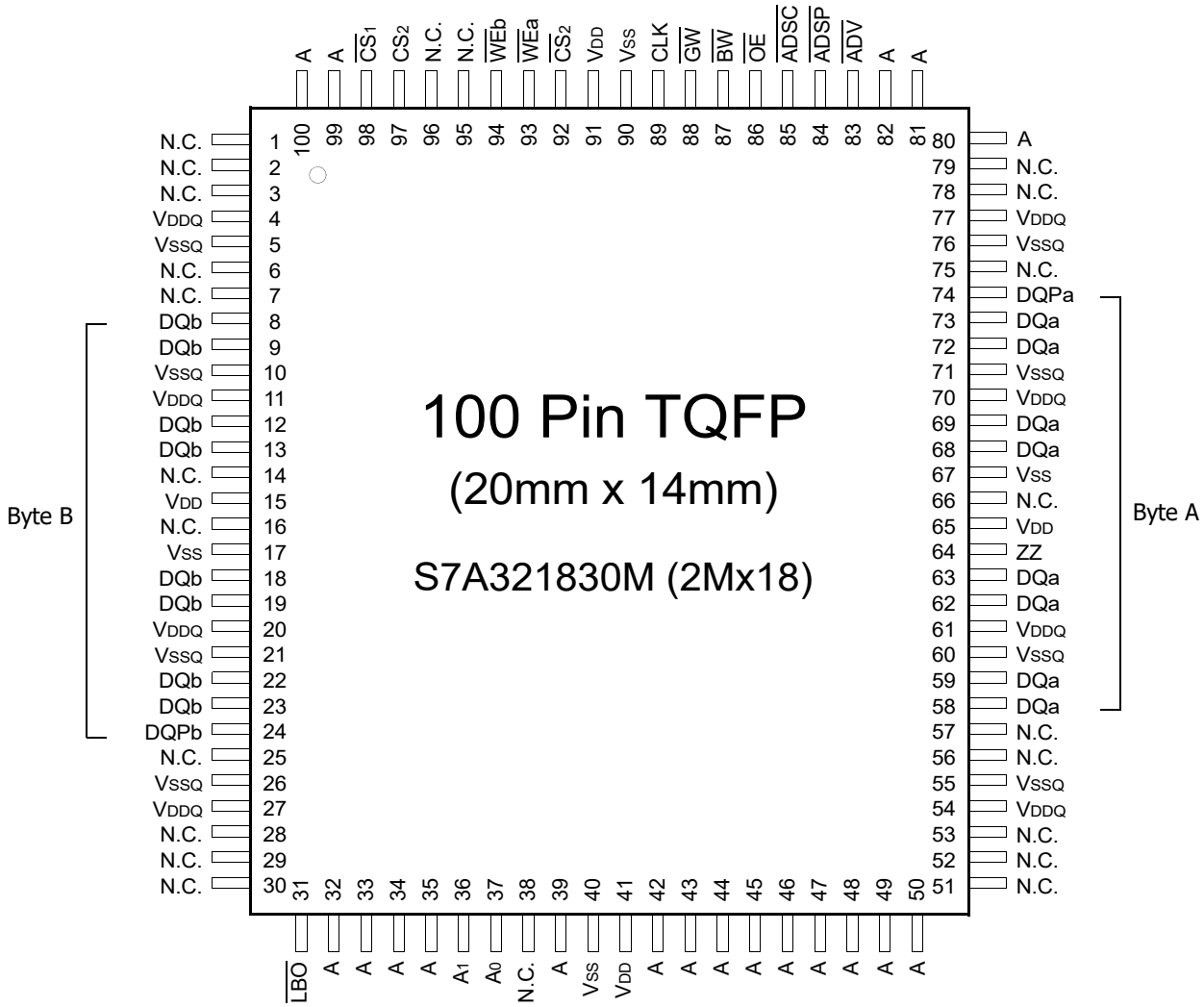



## Pin Name

| Symbol | Pin Name | TQFP Pin NO. | Symbol | Pin Name | TQFP Pin NO. |
|---|---|---|---|---|---|
| A | Address Inputs | 32,33,34,35,39,42,43 ,44,45,46,47,48,49,50 ,81,82,99,100 | VDD | Power Supply | 15,41,65,91 |
| | | | VSS | Ground | 17,40,67,90 |
| A0,A1 | Burst Address Inputs | 37,36 | | | |
| $\overline{ADV}$ | Burst Address Advance | 83 | N.C. | No Connect | 14,16,38,66 |
| $\overline{ADSP}$ | Address Status Processor | 84 | | | |
| $\overline{ADSC}$ | Address Status Controller | 85 | DQa | Data Inputs/Outputs | 52,53,56,57,58,59,62,63 |
| CLK | Clock | 89 | DQb | | 68,69,72,73,74,75,78,79 |
| $\overline{CS1}$ | Chip Select | 98 | DQc | | 2,3,6,7,8,9,12,13 |
| CS2 | Chip Select | 97 | DQd | | 18,19,22,23,24,25,28,29 |
| $\overline{CS2}$ | Chip Select | 92 | DQPa~Pd | | 51,80,1,30 |
| $\overline{WE}$x(x=a,b,c,d) | Byte Write Inputs | 93,94,95,96 | | | |
| $\overline{OE}$ | Output Enable | 86 | VDDQ | Output Power Supply | 4,11,20,27,54,61,70,77 |
| $\overline{GW}$ | Global Write Enable | 88 | | | |
| $\overline{BW}$ | Byte Write Enable | 87 | VSSQ | Output Ground | 5,10,21,26,55,60,71,76 |
| $\overline{ZZ}$ | Power Down Input | 64 | | | |
| $\overline{LBO}$ | Burst Mode Control | 31 | | | |

**Note :** 1. $A_0$ and $A_1$ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

## 100 TQFP Package Pin Configurations(Top View)




## Pin Name

| Symbol | Pin Name | TQFP Pin NO. | Symbol | Pin Name | TQFP Pin NO. |
|---|---|---|---|---|---|
| A | Address Inputs | 32,33,34,35,39,42,43, 44,45,46,47,48,49,50, 80,81,82,99,100 | VDD | Power Supply | 15,41,65,91 |
| | | | VSS | Ground | 17,40,67,90 |
| A0,A1 | Burst Address Inputs | 37,36 | | | |
| $\overline{ADV}$ | Burst Address Advance | 83 | N.C. | No Connect | 1,2,3,6,7,14,16,25,28,29 |
| $\overline{ADSP}$ | Address Status Processor | 84 | | | 30,38,51,52,53,56 |
| $\overline{ADSC}$ | Address Status Controller | 85 | | | 57,66,75,78,79,95,96 |
| CLK | Clock | 89 | | | |
| $\overline{CS1}$ | Chip Select | 98 | DQa | Data Inputs/Outputs | 58,59,62,63,68,69,72,73 |
| CS2 | Chip Select | 97 | DQb | | 8,9,12,13,18,19,22,23 |
| $\overline{CS2}$ | Chip Select | 92 | DQPa, Pb | | 74,24 |
| $\overline{WE}$x(x=a,b) | Byte Write Inputs | 93,94 | | | |
| $\overline{OE}$ | Output Enable | 86 | VDDQ | Output Power Supply | 4,11,20,27,54,61,70,77 |
| $\overline{GW}$ | Global Write Enable | 88 | | | |
| $\overline{BW}$ | Byte Write Enable | 87 | VSSQ | Output Ground | 5,10,21,26,55,60,71,76 |
| $\overline{ZZ}$ | Power Down Input | 64 | | | |
| $\overline{LBO}$ | Burst Mode Control | 31 | | | |

**NOTE :** $A_0$ and $A_1$ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

## 165FBGA PKG Pin Configurations - S7A323630M (1Mx36) - Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC | A | $\overline{CS1}$ | $\overline{WE_c}$ | $\overline{WE_b}$ | $\overline{CS2}$ | $\overline{BW}$ | $\overline{ADSC}$ | $\overline{ADV}$ | A | NC |
| **B** | NC | A | CS2 | $\overline{WE_d}$ | $\overline{WE_a}$ | CLK | $\overline{GW}$ | $\overline{OE}$ | $\overline{ADSP}$ | A | NC |
| **C** | $DQP_c$ | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_b$ |
| **D** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **E** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **F** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **G** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **H** | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **K** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **L** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **M** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **N** | $DQP_d$ | NC | $V_{DDQ}$ | $V_{SS}$ | NC | A | NC | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_a$ |
| **P** | NC | NC | A | A | TDI | A1* | TDO | A | A | A | A |
| **R** | $\overline{LBO}$ | A | A | A | TMS | A0* | TCK | A | A | A | A |

**Notes:** * A0 and A1 are two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

## Pin Name

| Symbol | Pin Name | Symbol | Pin Name |
|---|---|---|---|
| A | Address Inputs | VDD | Power Supply |
| A0,A1 | Burst Address Inputs | | |
| $\overline{ADV}$ | Burst Address Advance | VSS | Ground |
| $\overline{ADSP}$ | Address Status Processor | | |
| $\overline{ADSC}$ | Address Status Controller | N.C. | No Connect |
| CLK | Clock | | |
| $\overline{CS1}$ | Chip Select | DQa | Data Inputs/Outputs |
| CS2 | Chip Select | DQb | |
| $\overline{CS2}$ | Chip Select | DQc | |
| $\overline{WE}$x(x=a,b,c,d) | Byte Write Inputs | DQd | |
| $\overline{OE}$ | Output Enable | DQPa~Pd | |
| $\overline{GW}$ | Global Write Enable | | |
| $\overline{BW}$ | Byte Write Enable | VDDQ | Output Power Supply |
| $\overline{ZZ}$ | Power Down Input | | |
| $\overline{LBO}$ | Burst Mode Control | VSSQ | Output Ground |

**Note :** 1. $A_0$ and $A_1$ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

## 165FBGA PKG Pin Configurations - S7A321830M (2Mx18) - Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | NC | A | $\overline{CS1}$ | $\overline{WE}_b$ | NC | $\overline{CS2}$ | $\overline{BW}$ | $\overline{ADSC}$ | $\overline{ADV}$ | A | A |
| **B** | NC | A | CS2 | NC | $\overline{WE}_a$ | CLK | $\overline{GW}$ | $\overline{OE}$ | $\overline{ADSP}$ | A | NC |
| **C** | NC | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_a$ |
| **D** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **E** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **F** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **G** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **H** | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **K** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **L** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **M** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **N** | $DQP_b$ | NC | $V_{DDQ}$ | $V_{SS}$ | NC | A | NC | $V_{SS}$ | $V_{DDQ}$ | NC | NC |
| **P** | NC | NC | A | A | TDI | A1* | TDO | A | A | A | A |
| **R** | $\overline{LBO}$ | A | A | A | TMS | A0* | TCK | A | A | A | A |

**Notes:** * A0 and A1 are two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

## Pin Name

| Symbol | Pin Name | Symbol | Pin Name |
|---|---|---|---|
| A | Address Inputs | VDD | Power Supply |
| A0,A1 | Burst Address Inputs | | |
| $\overline{ADV}$ | Burst Address Advance | VSS | Ground |
| $\overline{ADSP}$ | Address Status Processor | | |
| $\overline{ADSC}$ | Address Status Controller | N.C. | No Connect |
| CLK | Clock | | |
| $\overline{CS1}$ | Chip Select | DQa | Data Inputs/Outputs |
| CS2 | Chip Select | DQb | |
| $\overline{CS2}$ | Chip Select | DQPa~Pb | |
| $\overline{WE}$x(x=a,b) | Byte Write Inputs | | |
| $\overline{OE}$ | Output Enable | VDDQ | Output Power Supply |
| $\overline{GW}$ | Global Write Enable | | |
| $\overline{BW}$ | Byte Write Enable | VSSQ | Output Ground |
| $\overline{ZZ}$ | Power Down Input | | |
| $\overline{LBO}$ | Burst Mode Control | | |

**Note :** 1. $A_0$ and $A_1$ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

## Function Description

The S7A323630M and S7A321830M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.
When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$)using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS}_1$.
All byte write is done by $\overline{GW}$(regaedless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is high.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regaedless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. The $\overline{WE}$a control DQa and DQPa, $\overline{WE}$b controls DQb and DQPb, $\overline{WE}$c controls DQc and DQPc, and $\overline{WE}$d control DQd and DQPd. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

## Burst Sequence Table

**(Interleaved Burst, $\overline{LBO}$=High)**

| $\overline{LBO}$ PIN | HIGH | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|---|
| | | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ |
| First Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| ↓ | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

**(Linear Burst, $\overline{LBO}$=Low)**

| $\overline{LBO}$ PIN | LOW | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|---|
| | | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ |
| First Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| ↓ | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

**Note** : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

## Asynchronous Truth Table

| Operation | ZZ | $\overline{OE}$ | I/O STATUS |
|---|---|---|---|
| Sleep Mode | H | X | High-Z |
| Read | L | L | DQ |
| | L | H | High-Z |
| Write | L | X | Din, High-Z |
| Deselected | L | X | High-Z |

**Notes**

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

## Truth Tables

### Synchronous Truth Table

| $\overline{CS_1}$ | $CS_2$ | $\overline{CS_2}$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{Write}$ | CLK | Address Accessed | Operation |
|---|---|---|---|---|---|---|---|---|---|
| H | X | X | X | L | X | X | ↑ | N/A | Not Selected |
| L | L | X | L | X | X | X | ↑ | N/A | Not Selected |
| L | X | H | L | X | X | X | ↑ | N/A | Not Selected |
| L | L | X | X | L | X | X | ↑ | N/A | Not Selected |
| L | X | H | X | L | X | X | ↑ | N/A | Not Selected |
| L | H | L | L | X | X | X | ↑ | External Address | Begin Burst Read Cycle |
| L | H | L | H | L | X | L | ↑ | External Address | Begin Burst Write Cycle |
| L | H | L | H | L | X | H | ↑ | External Address | Begin Burst Read Cycle |
| X | X | X | H | H | L | H | ↑ | Next Address | Continue Burst Read Cycle |
| H | X | X | X | H | L | H | ↑ | Next Address | Continue Burst Read Cycle |
| X | X | X | H | H | L | L | ↑ | Next Address | Continue Burst Write Cycle |
| H | X | X | X | H | L | L | ↑ | Next Address | Continue Burst Write Cycle |
| X | X | X | H | H | H | H | ↑ | Current Address | Suspend Burst Read Cycle |
| H | X | X | X | H | H | H | ↑ | Current Address | Suspend Burst Read Cycle |
| X | X | X | H | H | H | L | ↑ | Current Address | Suspend Burst Write Cycle |
| H | X | X | X | H | H | L | ↑ | Current Address | Suspend Burst Write Cycle |

**Notes :** 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ( ↑ ) .

3. $\overline{Write}$ = L means Write operation in Write Truth Table.
   $\overline{Write}$ = H means Read operation in Write Truth Table.

4. Operation finally depends on status of asynchronous input pins(ZZ and OE).

### Write Truth Table(x36)

| $\overline{GW}$ | $\overline{BW}$ | $\overline{WEa}$ | $\overline{WEb}$ | $\overline{WEc}$ | $\overline{WEd}$ | OPERATION |
|---|---|---|---|---|---|---|
| H | H | X | X | X | X | Read |
| H | L | H | H | H | H | Read |
| H | L | L | H | H | H | Write Byte A |
| H | L | H | L | H | H | Write Byte B |
| H | L | H | H | L | L | Write Byte C And D |
| H | L | L | L | L | L | Write All Bytes |
| L | X | X | X | X | X | Write All Bytes |

**Notes :** 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK( ↑ ).

### Write Truth Table(x18)

| $\overline{GW}$ | $\overline{BW}$ | $\overline{WEa}$ | $\overline{WEb}$ | OPERATION |
|---|---|---|---|---|
| H | H | X | X | Read |
| H | L | H | H | Read |
| H | L | L | H | Write Byte A |
| H | L | H | L | Write Byte B |
| H | L | L | L | Write All Bytes |
| L | X | X | X | Write All Bytes |

**Notes :** 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK( ↑ ).

## Absolute Maximum Ratings

| Parameter | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Voltage on $V_{DD}$ Supply Relative to $V_{SS}$ | | $V_{DD}$ | -0.3 to 4.6 | V |
| Voltage on $V_{DDQ}$ Supply Relative to $V_{SS}$ | | $V_{DDQ}$ | $V_{DD}$ | V |
| Voltage on Input Pin Relative to $V_{SS}$ | | $V_{IN}$ | -0.3 to $V_{DD}$+0.3 | V |
| Voltage on I/O Pin Relative to $V_{SS}$ | | $V_{IO}$ | -0.3 to $V_{DDQ}$+0.3 | V |
| Power Dissipation | | $P_D$ | 1.6 | W |
| Storage Temperature | | $T_{STG}$ | -65 to 150 | °C |
| Operating Temperature | Commercial | $T_{OPR}$ | 0 to 70 | °C |
| | Industrial | $T_{OPR}$ | -40 to 85 | °C |
| Storage Temperature Range Under Bias | | $T_{BIAS}$ | -10 to 85 | °C |

**Notes :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Operating Conditions

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD1}$ | 1.7 | 1.8 | 2.0 | V |
| | $V_{DDQ1}$ | 1.7 | 1.8 | 2.0 | V |
| | $V_{DD2}$ | 2.3 | 2.5 | 2.7 | V |
| | $V_{DDQ2}$ | 1.7 | 2.5 | 2.7 | V |
| | $V_{DD3}$ | 3.1 | 3.3 | 3.5 | V |
| | $V_{DDQ3}$ | 2.3 | 3.3 | 3.5 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |

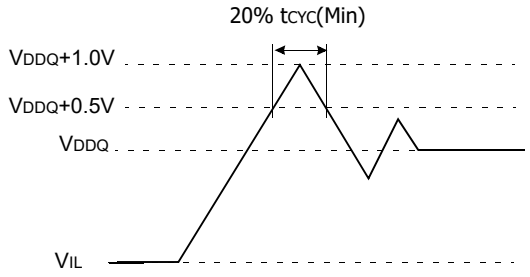
**Notes:** 1. The above parameters are also guaranteed at industrial temperature range.
2. It should be $V_{DDQ} \leq V_{DD}$

## Capacitence($T_A$=25°C, f=1MHz)

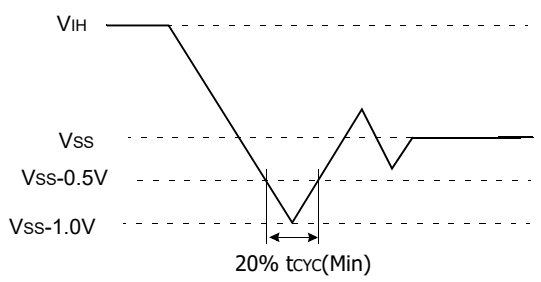
| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 5 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$=0V | - | 7 | pF |

**Note :** Sampled not 100% tested.

## Overshoot Timing




## Undershoot Timing



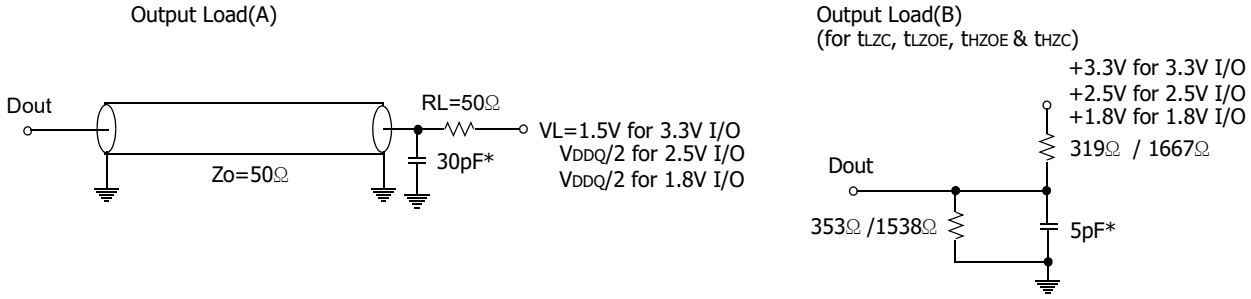
## DC Electrical Caracteristics

| Parameter | Symbol | Test Conditions | | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Input Leakage Current(except | $I_{IL}$ | $V_{DD}$=Max ; $V_{IN}$=$V_{SS}$ to $V_{DD}$ | | -2 | +2 | uA | |
| Output Leakage Current | $I_{OL}$ | Output Disabled, $V_{out}$=$V_{SS}$ to $V_{DDQ}$ | | -2 | +2 | uA | |
| Operating Current | $I_{CC}$ | Device Selected, $I_{OUT}$=0mA, | -25 | - | 300 | mA | 1,2 |
| | | ZZ ≤ $V_{IL}$ , Cycle Time ≥ $t_{CYC}$ Min | -16 | - | 260 | | |
| Standby Current | $I_{SB}$ | Device deselected, $I_{OUT}$=0mA, ZZ≤$V_{IL}$, | -25 | - | 150 | mA | |
| | | f=Max, All Inputs ≤ VIL or ≥ VIH | -16 | | 145 | mA | |
| | $I_{SB1}$ | Device deselected, $I_{OUT}$=0mA, ZZ ≤ 0.2V, f=0, All Inputs=fixed ($V_{DD}$-0.2V or 0.2V) | | - | 120 | mA | |
| | $I_{SB2}$ | Device deselected, $I_{OUT}$=0mA, ZZ ≥ $V_{DD}$-0.2V, f=Max, All Inputs ≤ $V_{IL}$ or ≥ $V_{IH}$ | | - | 120 | mA | |
| Output Low Voltage(3.3V I/O) | $V_{OL}$ | $I_{OL}$=8.0mA | | - | 0.4 | V | |
| Output High Voltage(3.3V I/O) | $V_{OH}$ | $I_{OH}$=-4.0mA | | 2.4 | - | V | |
| Output Low Voltage(2.5V I/O) | $V_{OL}$ | $I_{OL}$=1.0mA | | - | 0.4 | V | |
| Output High Voltage(2.5V I/O) | $V_{OH}$ | $I_{OH}$=-1.0mA | | 2.0 | - | V | |
| Output Low Voltage(1.8V I/O) | $V_{OL}$ | $I_{OL}$=1.0mA | | - | 0.4 | V | |
| Output High Voltage(1.8V I/O) | $V_{OH}$ | $I_{OH}$=-1.0mA | | $V_{DDQ}$-0.4 | - | V | |
| Input Low Voltage(3.3V I/O) | $V_{IL}$ | | | -0.3* | 0.8 | V | |
| Input High Voltage(3.3V I/O) | $V_{IH}$ | | | 2.0 | $V_{DD}$+0.3** | V | 3 |
| Input Low Voltage(2.5V I/O) | $V_{IL}$ | | | -0.3* | 0.7 | V | |
| Input High Voltage(2.5V I/O) | $V_{IH}$ | | | 1.7 | $V_{DD}$+0.3** | V | 3 |
| Input Low Voltage(1.8V I/O) | $V_{IL}$ | | | -0.3* | $V_{DD}$ x 0.3 | V | |
| Input High Voltage(1.8V I/O) | $V_{IH}$ | | | $V_{DD}$ x 0.6 | $V_{DD}$+0.3** | V | 3 |

**Notes :** The above parameters are also guaranteed at industrial temperature range.
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. $V_{IH}$=$V_{DDQ}$+0.3V

## Test Conditions

| Parameter | Value |
|---|---|
| Input Pulse Level for 3.3V I/O | 0 to 3.0V |
| Input Pulse Level for 2.5V I/O | 0 to 2.5V |
| Input Pulse Level for 1.8V I/O | 0 to 1.8V |
| Input Rise and Fall Time (Measured at 20% to 80%) | 1.0V/ns |
| Input and Output Timing Reference Levels for 3.3V I/O | 1.5V |
| Input and Output Timing Reference Levels for 2.5V I/O and 1.8V I/O | $V_{DDQ}/2$ |
| Output Load | See Fig. 1 |




* Including Scope and Jig Capacitance

**Fig. 1**

## AC Timing Characteristics

| Parameter | Symbol | -25 | | -16 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Cycle Time | $t_{CYC}$ | 4.0 | - | 6.0 | - | ns |
| Clock Access Time (Vdd=2.5V and 3.3V) | $t_{CD}$ | - | 2.6 | - | 3.5 | ns |
| Clock Access Time (Vdd=1.8V) | | - | 3.0 | - | 3.5 | ns |
| Output Enable to Data Valid (Vdd=2.5V and 3.3V) | $t_{OE}$ | - | 2.6 | - | 3.5 | ns |
| Output Enable to Data Valid (Vdd=1.8V) | | - | 3.0 | - | 3.5 | ns |
| Clock High to Output Low-Z | $t_{LZC}$ | 1.5 | - | 1.5 | - | ns |
| Output Hold from Clock High | $t_{OH}$ | 1.5 | - | 1.5 | - | ns |
| Output Enable Low to Output Low-Z | $t_{LZOE}$ | 0 | - | 0 | - | ns |
| Output Enable High to Output High-Z | $t_{HZOE}$ | - | 2.6 | - | 3.0 | ns |
| Clock High to Output High-Z | $t_{HZC}$ | - | 2.6 | - | 3.0 | ns |
| Clock High Pulse Width | $t_{CH}$ | 1.7 | - | 2.2 | - | ns |
| Clock Low Pulse Width | $t_{CL}$ | 1.7 | - | 2.2 | - | ns |
| Address Setup to Clock High | $t_{AS}$ | 1.2 | - | 1.5 | - | ns |
| Address Status Setup to Clock High | $t_{SS}$ | 1.2 | - | 1.5 | - | ns |
| Data Setup to Clock High | $t_{DS}$ | 1.2 | - | 1.5 | - | ns |
| Write Setup to Clock High ($\overline{WE}$, $\overline{BW}$x) | $t_{WS}$ | 1.2 | - | 1.5 | - | ns |
| Address Advance Setup to Clock High | $t_{ADVS}$ | 1.2 | - | 1.5 | - | ns |
| Chip Select Setup to Clock High | $t_{CSS}$ | 1.2 | - | 1.5 | - | ns |
| Address Hold from Clock High | $t_{AH}$ | 0.3 | - | 0.5 | - | ns |
| Address Status Hold from Clock High | $t_{SH}$ | 0.3 | - | 0.5 | - | ns |
| Data Hold from Clock High | $t_{DH}$ | 0.3 | - | 0.5 | - | ns |
| Write Hold from Clock High ($\overline{WE}$, $\overline{BW}$x) | $t_{WH}$ | 0.3 | - | 0.5 | - | ns |
| Address Advance Hold from Clock High | $t_{ADVH}$ | 0.3 | - | 0.5 | - | ns |
| Chip Select Hold from Clock High | $t_{CSH}$ | 0.3 | - | 0.5 | - | ns |
| ZZ High to Power Down | $t_{PDS}$ | 2 | - | 2 | - | cycle |
| ZZ Low to Power Up | $t_{PUS}$ | 2 | - | 2 | - | cycle |

**Notes :** 1. The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
4. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

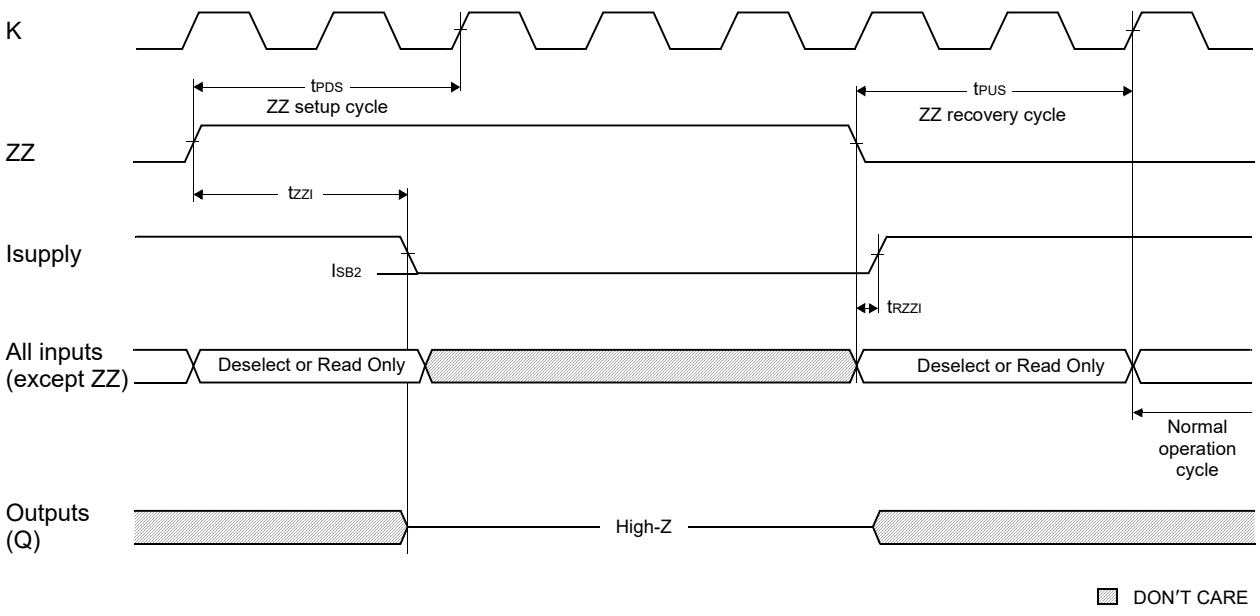
## Sleep Mode

Sleep Mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB2}$. The duration of Sleep Mode is dictated by the length of time the ZZ is in a High state.
After entering Sleep Mode, all inputs except ZZ become disabled and all outputs go to High-Z.
The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep Mode.
When the ZZ pin becomes a logic High, $I_{SB2}$ is guaranteed after the time $t_{ZZI}$ is met. Any operation pending when entering Sleep Mode is not guaranteed to successful complete. Therefore, Sleep Mode (Read or Write) must not be initiated until valid pending operations are completed. similarly, when exiting Sleep Mode during $t_{PUS}$, only a Deselect or Read cycle should be given while the SRAM is transitioning out of Sleep Mode.

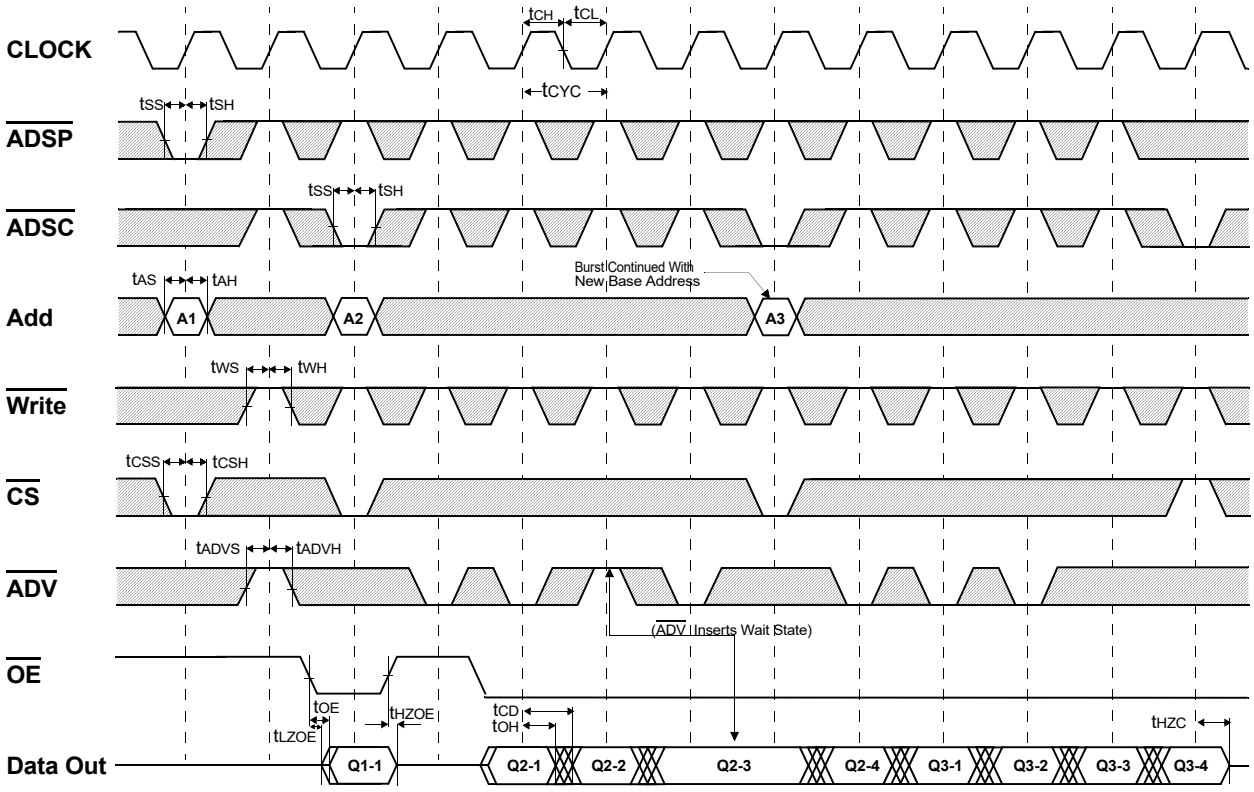
## Sleep Mode Electrical Characteristics

| Description | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Current during SLEEP MODE | ZZ ≥ $V_{IH}$ | $I_{SB2}$ | | 120 | mA |
| ZZ active to input ignored | | $t_{PDS}$ | 2 | | cycle |
| ZZ inactive to input sampled | | $t_{PUS}$ | 2 | | cycle |
| ZZ active to SLEEP current | | $t_{ZZI}$ | | 2 | cycle |
| ZZ inactive to exit SLEEP current | | $t_{RZZI}$ | 0 | | |

## Sleep Mode Waveform



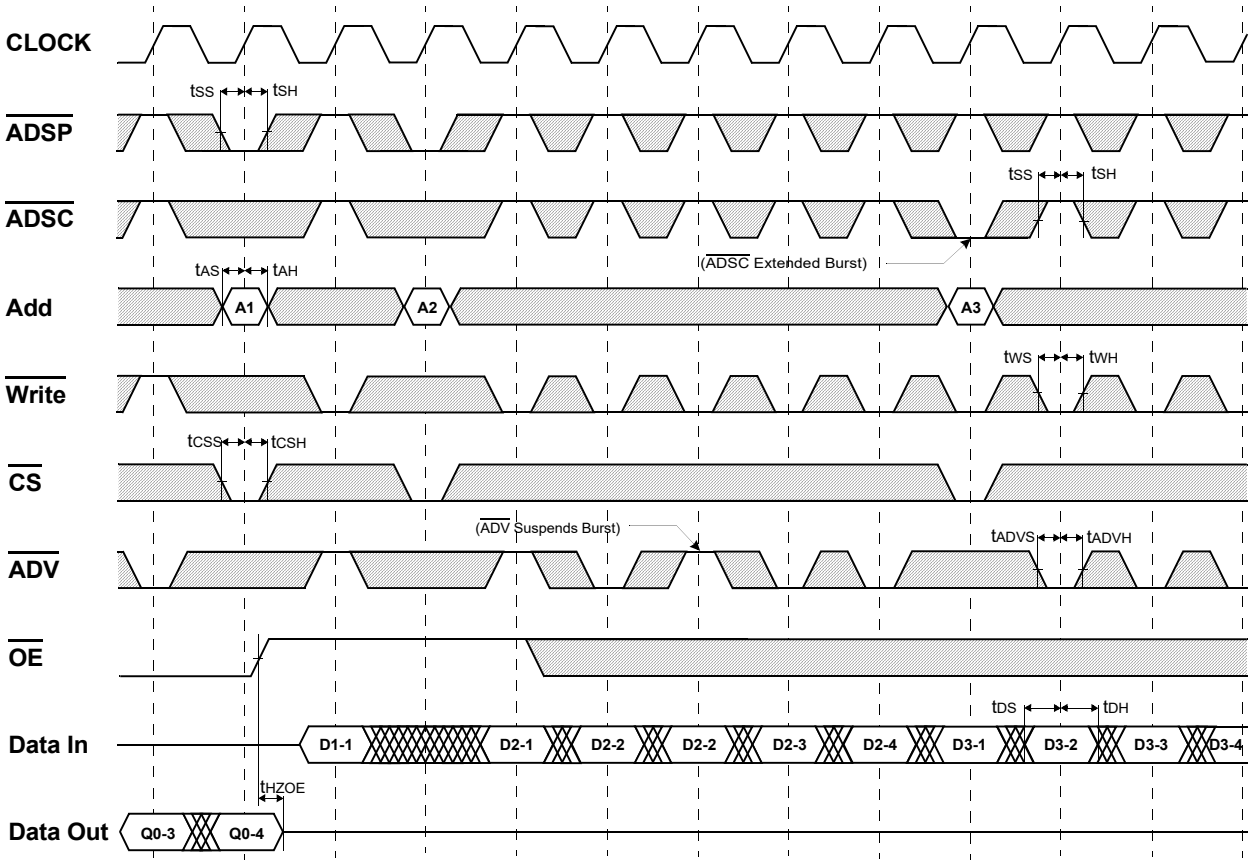
## Timing Waveform of Read Cycle




NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, $CS_2$ = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $CS_2$ = L

Don't Care
Undefined

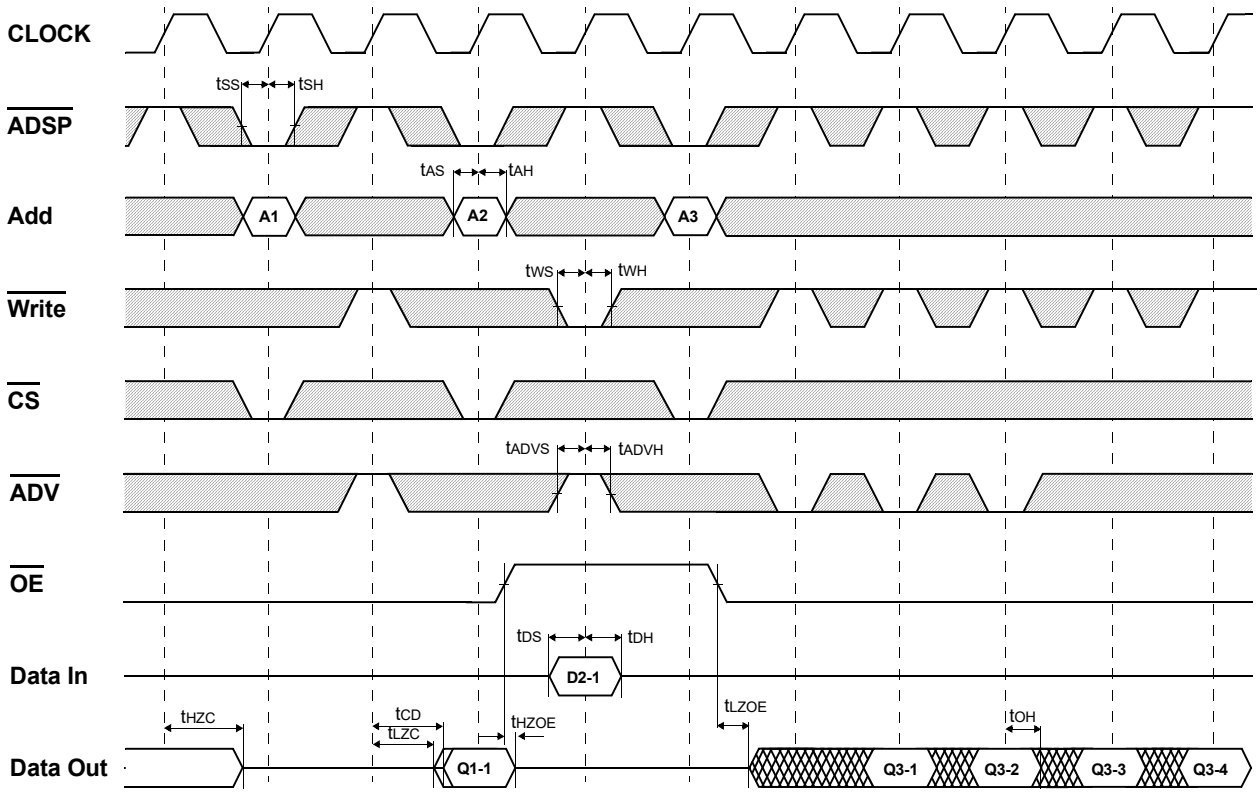
## Timing Waveform of Write Cycle




NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, $CS_2$ = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $CS_2$ = L

Don't Care
Undefined

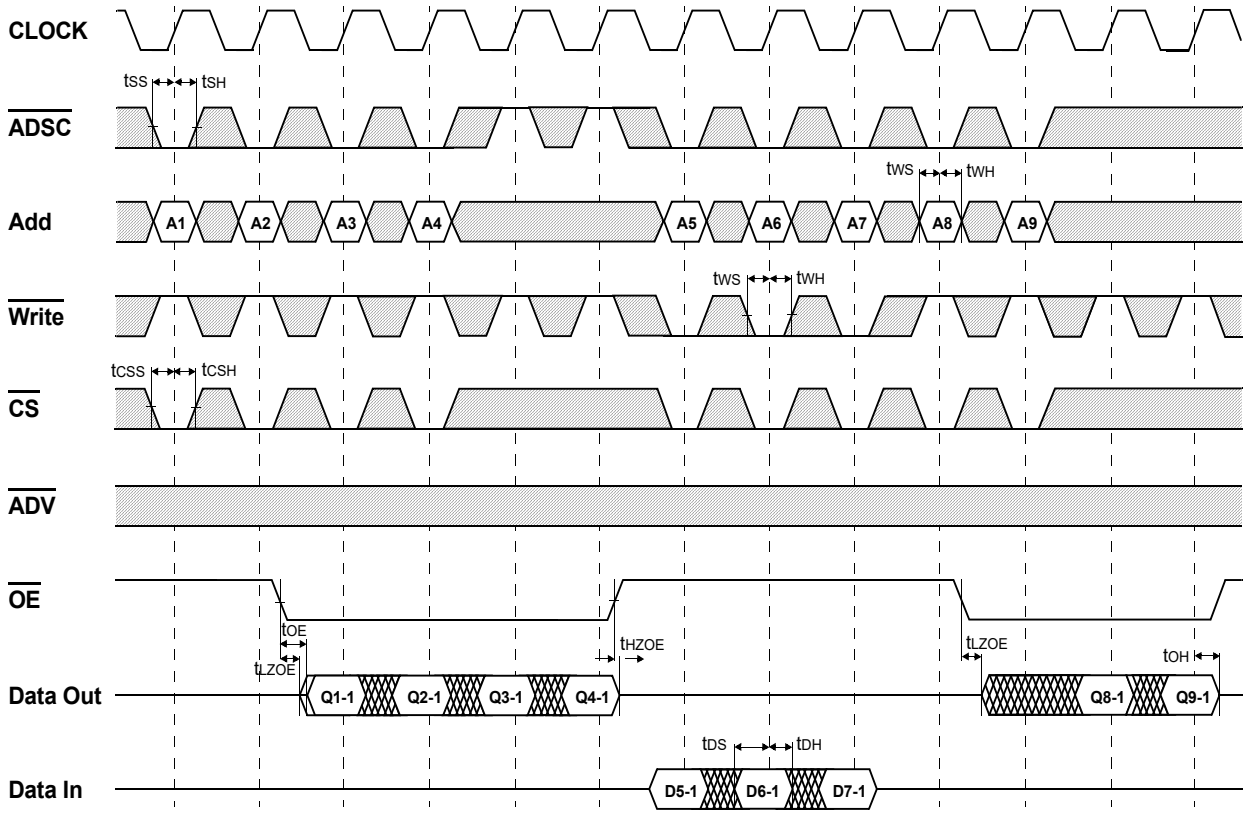
## Timing Waveform of Combination Read/Write Cycle($\overline{ADSP}$ Controlled , $\overline{ADSC}$=High)




NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, $CS_2$ = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $CS_2$ = L

Don't Care
Undefined

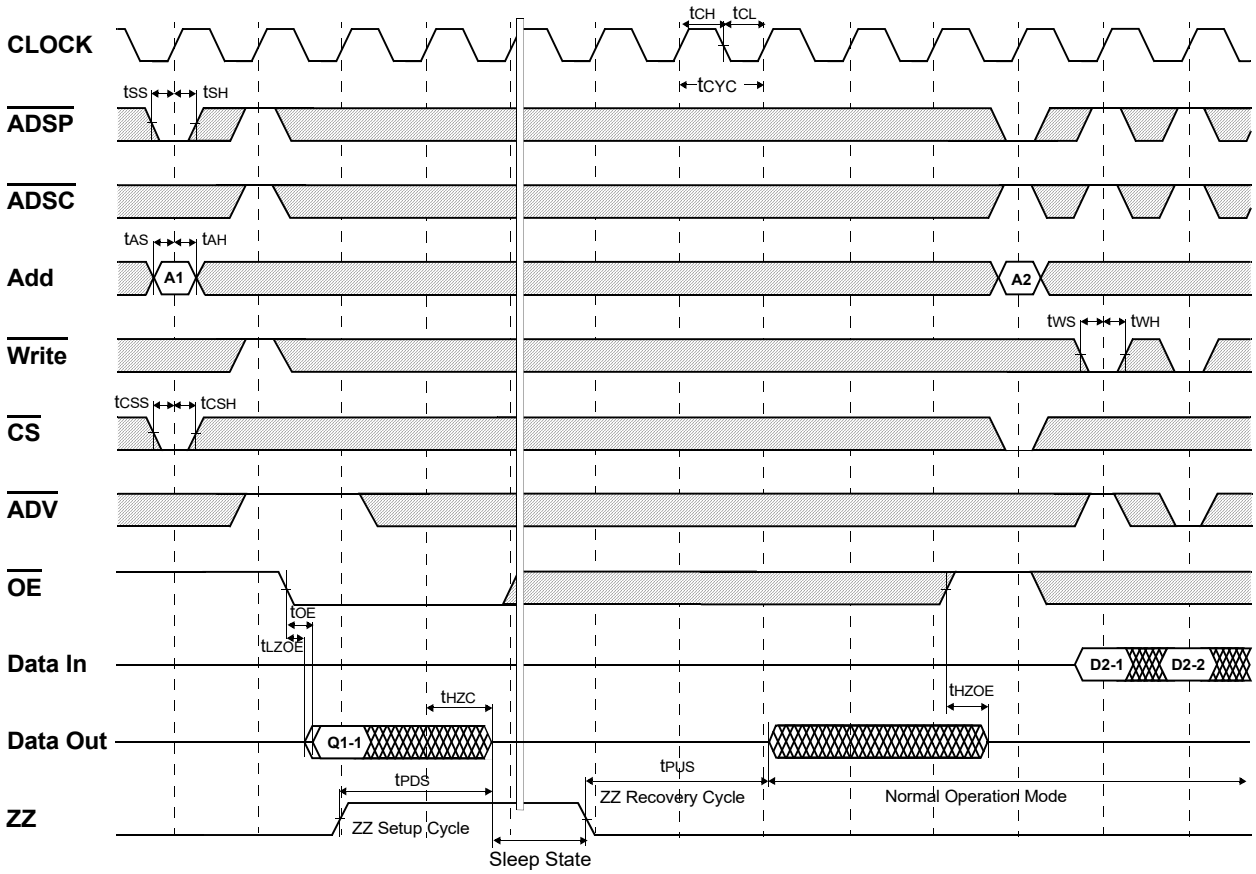
## Timing Waveform of Single Read/Write Cycle ($\overline{ADSC}$ Controlled , $\overline{ADSP}$=High)




NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, $CS_2$ = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $CS_2$ = L

Don't Care
Undefined

## Timing Waveform of Power Down Cycle



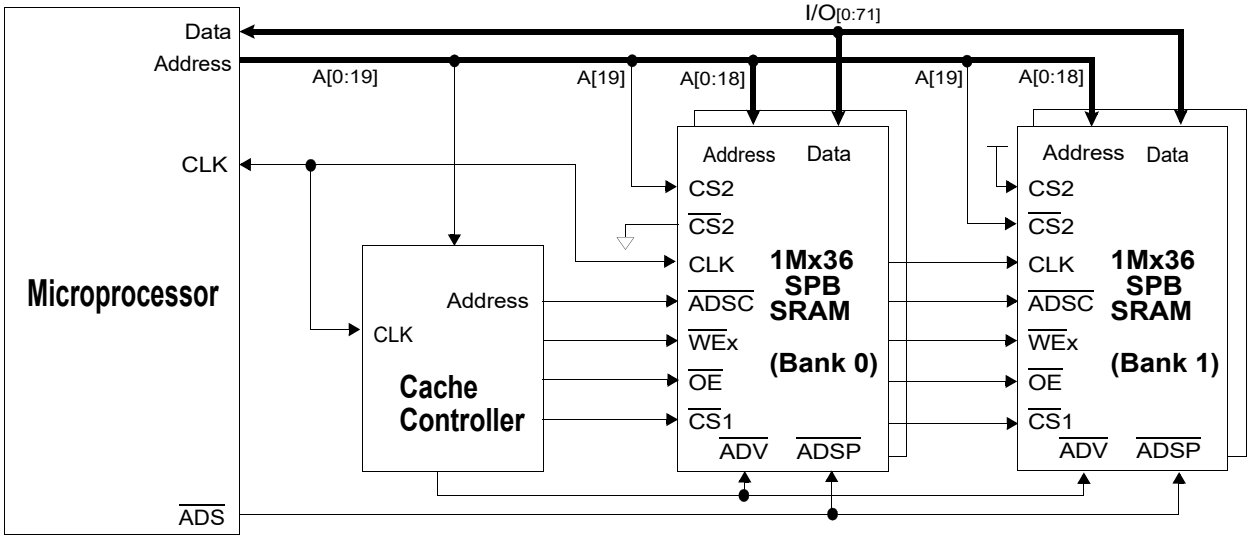

NOTES : $\overline{Write}$ = L means GW = L, or GW = H, BW = L, WEx = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, $CS_2$ = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $CS_2$ = L

Don't Care
Undefined

## Application Information

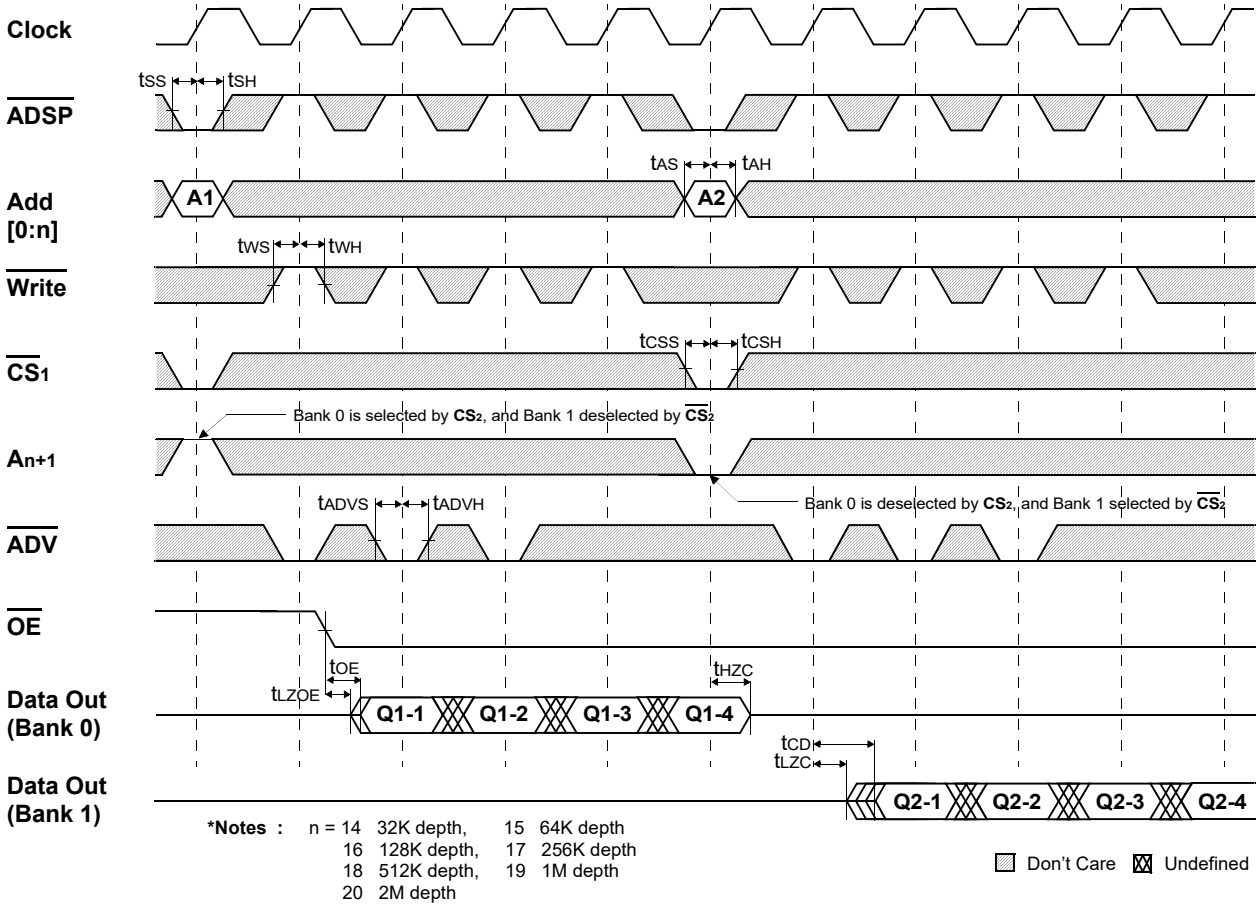
### Depth Expansion

The Netsol 1Mx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.




## Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)

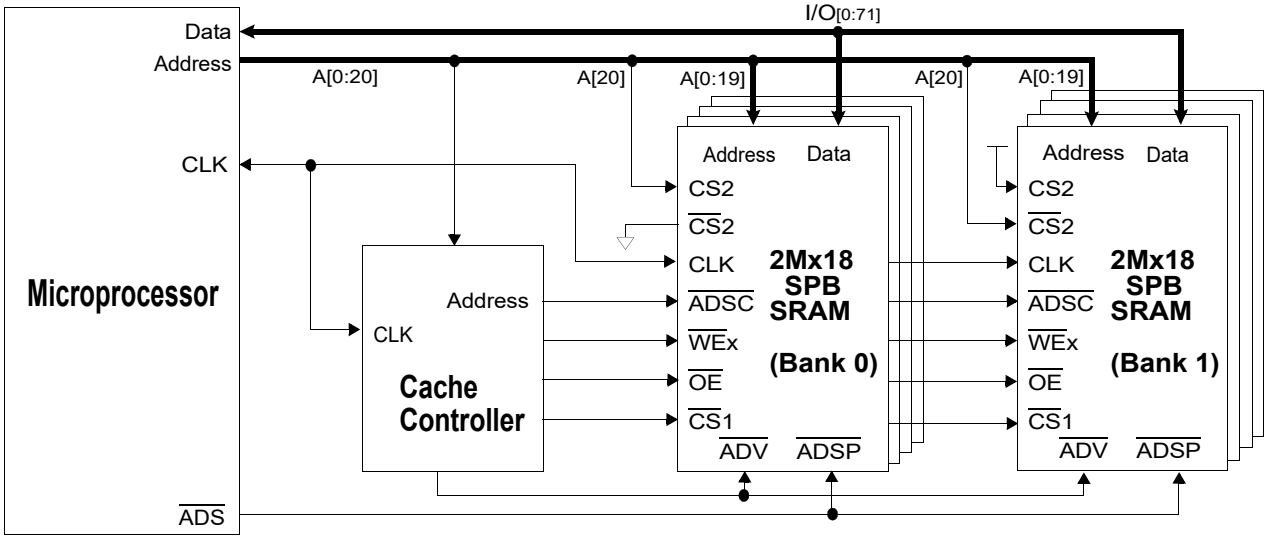
### ($\overline{ADSP}$ Controlled, $\overline{ADSC}$=High)



## Application Information

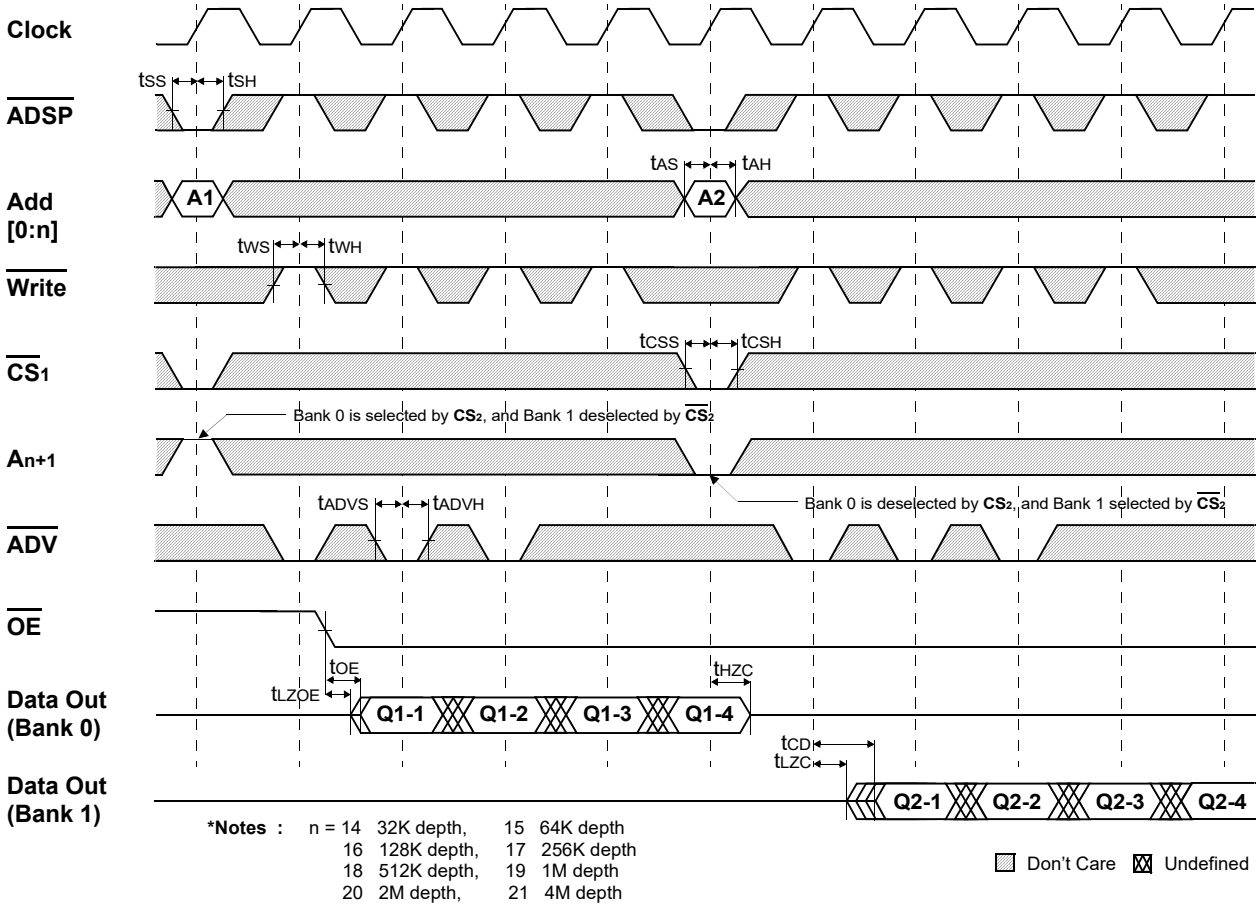
### Depth Expansion

The Netsol 2Mx18 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 2M depth to 4M depth without extra logic.




## Interleave Read Timing (Refer to non-interleave write timing for interleave write timing)

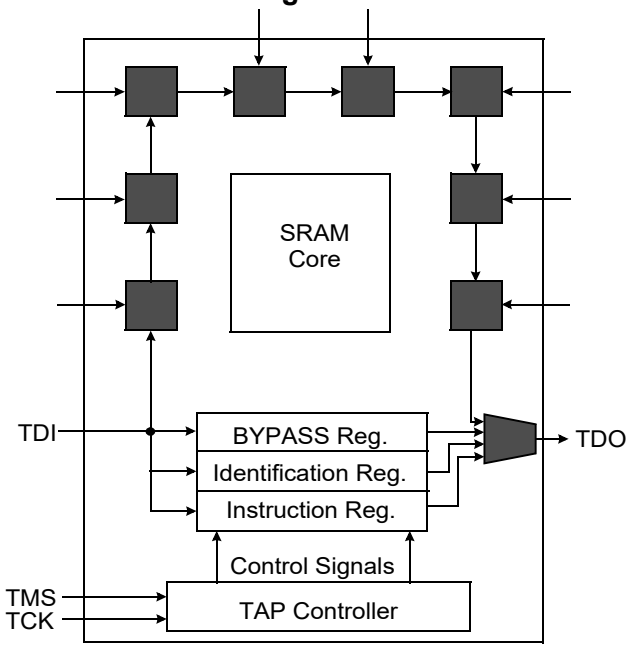
### ($\overline{ADSP}$ Controlled, $\overline{ADSC}$=High)



## IEEE 1149.1 Test Access Port and Boundary Scan-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP).The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to $V_{SS}$ to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to $V_{DD}$ through a resistor. TDO should be left unconnected.

### JTAG Block Diagram



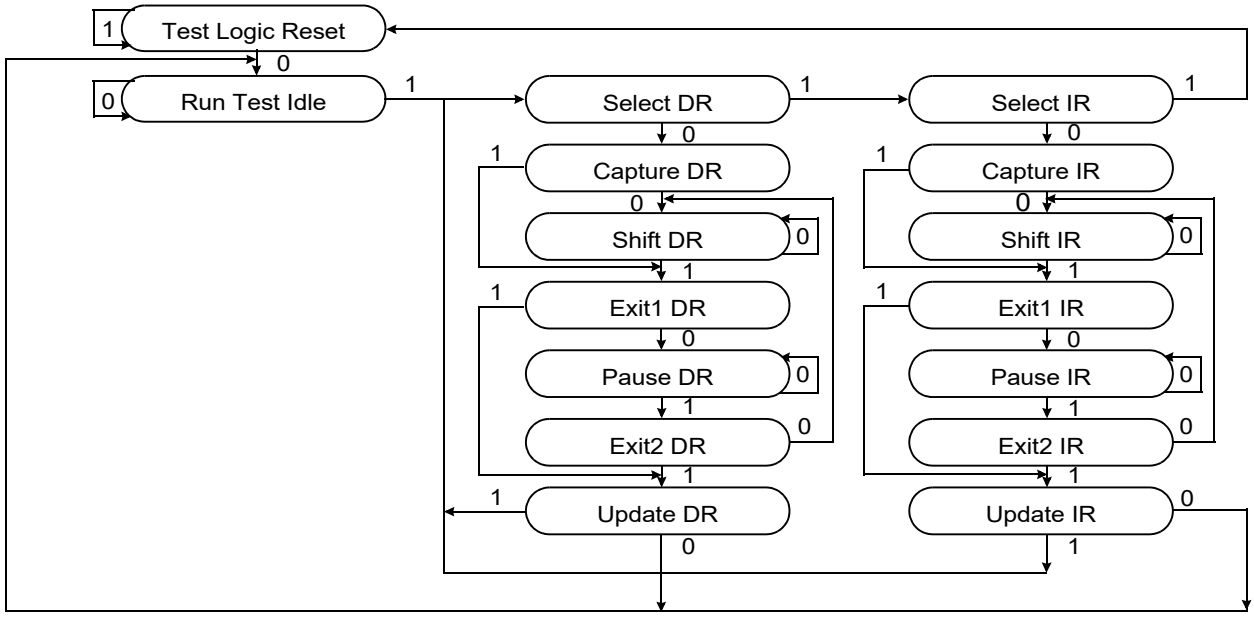

### JTAG Instruction Coding

| IR2 | IR1 | IR0 | Instruction | TDO Output | Notes |
|---|---|---|---|---|---|
| 0 | 0 | 0 | EXTEST | Boundary Scan Register | 1 |
| 0 | 0 | 1 | IDCODE | Identification Register | 3 |
| 0 | 1 | 0 | SAMPLE-Z | Boundary Scan Register | 2 |
| 0 | 1 | 1 | BYPASS | Bypass Register | 4 |
| 1 | 0 | 0 | SAMPLE | Boundary Scan Register | 5 |
| 1 | 0 | 1 | RESERVED | Do Not Use | 6 |
| 1 | 1 | 0 | BYPASS | Bypass Register | 4 |
| 1 | 1 | 1 | BYPASS | Bypass Register | 4 |

**NOTE**:

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to $V_{SS}$ when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

### TAP Controller State Diagram



## Scan Register Definition

| Part | Instruction Register | Bypass Register | ID Register | Boundary Scan |
|---|---|---|---|---|
| 1M x 36<br>2M x 18 | 3 bits | 1 bit | 32 bits | 76 bits |

## ID Registration Definition

| Part | Revision Number (31:28) | Part Configuration (27:18) | Vendor Definition (17:12) | Netsol JEDEC Code (11: 1) | Start Bit(0) |
|---|---|---|---|---|---|
| 1M x 36 | 0000 | 01000 00100 | 000000 | 01111011001 | 1 |
| 2M x 18 | 0000 | 01001 00011 | 000000 | 01111011001 | 1 |

## Boundary Scan Exit Order

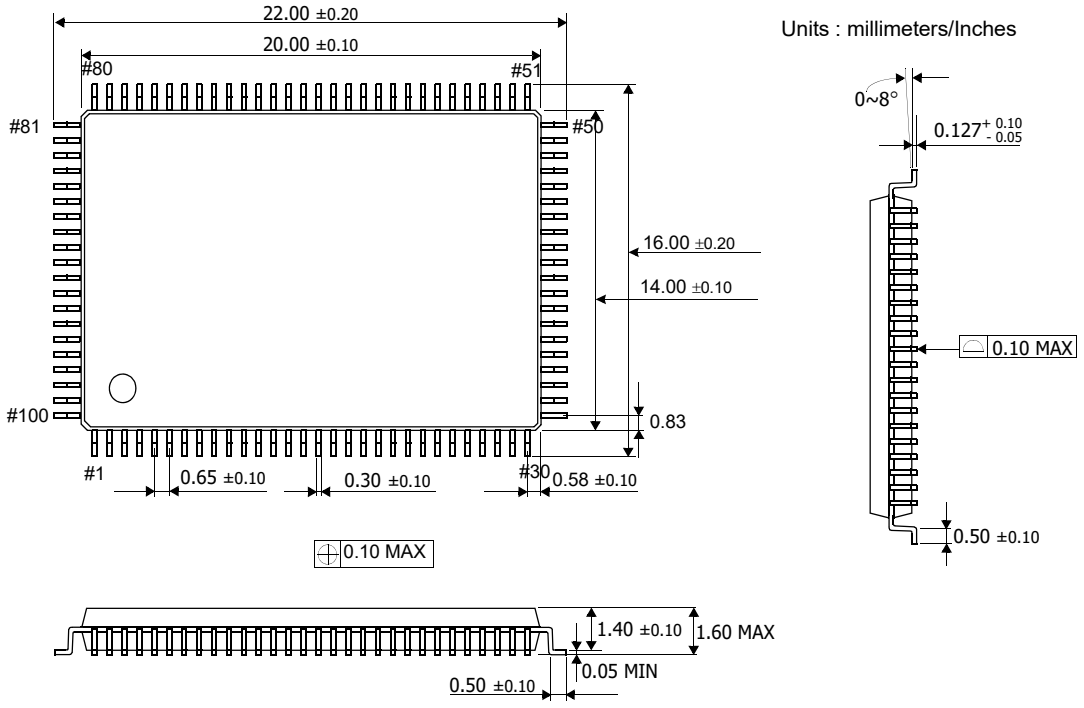
| $\overline{\text{BIT}}$ | Pin ID (x18) | Pin ID (x36) |
|---|---|---|
| 1 | 6N | 6N |
| 2 | 8P | 8P |
| 3 | 8R | 8R |
| 4 | 9R | 9R |
| 5 | 9P | 9P |
| 6 | 10P | 10P |
| 7 | 10R | 10R |
| 8 | 11R | 11R |
| 9 | 11P | 11P |
| 10 | 11H | 11H |
| 11 | 11N | 11N |
| 12 | 11M | 11M |
| 13 | 11L | 11L |
| 14 | 11K | 11K |
| 15 | 11J | 11J |
| 16 | 10M | 10M |
| 17 | 10L | 10L |
| 18 | 10K | 10K |
| 19 | 10J | 10J |
| 20 | 11G | 11G |
| 21 | 11F | 11F |
| 22 | 11E | 11E |
| 23 | 11D | 11D |
| 24 | 11C | 10G |
| 25 | 10F | 10F |
| 26 | 10E | 10E |
| 27 | 10D | 10D |
| 28 | 10G | 11C |
| 29 | 11A | 11A |
| 30 | 11B | 11B |
| 31 | 10A | 10A |
| 32 | 10B | 10B |
| 33 | 9A | 9A |
| 34 | 9B | 9B |
| 35 | 8A | 8A |
| 36 | 8B | 8B |
| 37 | 7A | 7A |
| 38 | 7B | 7B |
| 39 | 6B | 6B |

| $\overline{\text{BIT}}$ | Pin ID (x18) | Pin ID (x36) |
|---|---|---|
| 40 | 6A | 6A |
| 41 | 5B | 5B |
| 42 | 5A | 5A |
| 43 | 4A | 4A |
| 44 | 4B | 4B |
| 45 | 3B | 3B |
| 46 | 3A | 3A |
| 47 | 2A | 2A |
| 48 | 2B | 2B |
| 49 | 1B | 1B |
| 50 | 1A | 1A |
| 51 | 1C | 1C |
| 52 | 1D | 1D |
| 53 | 1E | 1E |
| 54 | 1F | 1F |
| 55 | 1G | 1G |
| 56 | 2D | 2D |
| 57 | 2E | 2E |
| 58 | 2F | 2F |
| 59 | 2G | 2G |
| 60 | 1J | 1J |
| 61 | 1K | 1K |
| 62 | 1L | 1L |
| 63 | 1M | 1M |
| 64 | 1N | 2J |
| 65 | 2K | 2K |
| 66 | 2L | 2L |
| 67 | 2M | 2M |
| 68 | 2J | 1N |
| 69 | 2R | 2R |
| 70 | 1R | 1R |
| 71 | 3P | 3P |
| 72 | 3R | 3R |
| 73 | 4R | 4R |
| 74 | 4P | 4P |
| 75 | 6P | 6P |
| 76 | 6R | 6R |

**Note**: 1. NC pins are read as "X" (i.e. don't care.)

## Package Dimensions

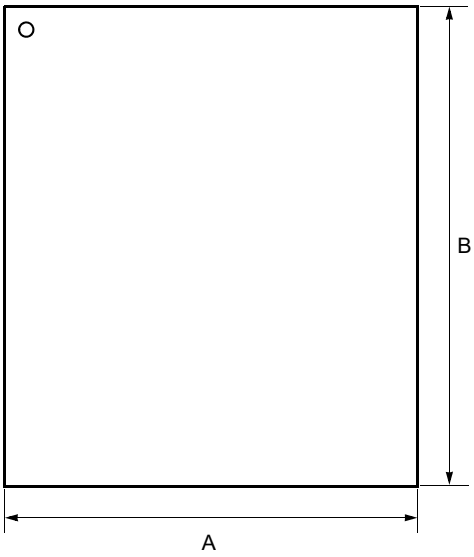
**100-TQFP-1420A (Lead Free)**



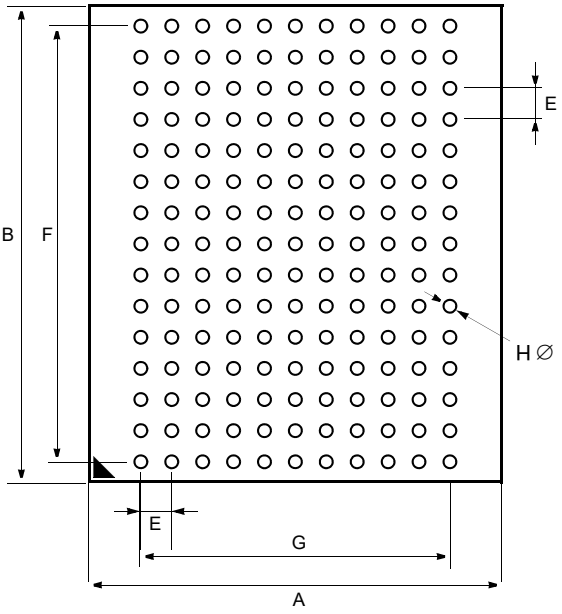
## 165 FBGA Package Dimensions (Lead Free)

**13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Grid Array**

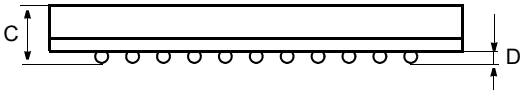
**Top View**




**Bottom View**




**Side View**




| Symbol | Value | Units | Note | Symbol | Value | Units | Note |
|---|---|---|---|---|---|---|---|
| **A** | 13 ± 0.1 | mm | | **E** | 1.0 | mm | |
| **B** | 15 ± 0.1 | mm | | **F** | 14.0 | mm | |
| **C** | 1.3 ± 0.1 | mm | | **G** | 10.0 | mm | |
| **D** | 0.35 ± 0.05 | mm | | **H** | 0.5 ± 0.05 | mm | |