

36Mb NTSRAM Sync-Pipelined Burst Specification

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S7N323631M
S7N321831M

1Mx36 & 2Mx18 NTSRAM Sync-Pipelined Burst

Document Title

1Mx36 & 2Mx18 Bit NTSRAM Synchronous Pipelined Burst

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	May 2012	Preliminary
1.0	Add current spec value Add 165FBGA information	Oct. 2012	Final
1.1	Add 1.8V Vdd support	Oct. 2013	Final
1.2	Correct typo in page 3. 32Mb => 36Mb	Sep. 2014	Final

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1Mx36 & 2Mx18 NTSRAM Sync-Pipelined Burst

1Mx36 & 2Mx18 Bit NTSRAM Synchronous Pipelined Burst

Features

- Fully registered inputs and outputs for pipelined operation
- V_{DD} = 1.8V (1.7V ~ 2.0V) or 2.5V (2.3V ~ 2.7V) or 3.3V (3.1V ~ 3.5V) Power Supply
- V_{DDQ} = 1.7V ~ 2.0V I/O Power Supply (VDD=1.8V) or 2.3V ~ 2.7V I/O Power Supply (VDD=2.5V) or 2.3V ~ 3.5V I/O Power Supply (VDD=3.3V)
- Byte Writable Function
- Enable clock and suspend operation
- Single Read/Write control pin
- Asynchronous output enable control
- Self-timed Write control
- Three Chip Enable for simple depth expansion with no data contention
- An interleaved burst or a linear burst mode
- Power Down mode
- Operating in commercial and industrial temperature range
- 100-TQFP-1420A (Lead free package)
- 165FBGA(11x15 ball array) with body size of 13mmx15mm. (Lead free package)

General Description

The S7N323631M and S7N321831M are 37,748,736-bits Synchronous Static SRAMs. The NTSRAM, or Non-Turnaround Static Random Access Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock.

Burst order control must be tied "High or Low". Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

The S7N323631M and S7N321831M are implemented with high performance CMOS technology and is available in 100pin TQFP package and 165FBGA package. Multiple power and ground pins minimize ground bounce.

Key Parameters

Parameter	Symbol	-25	-16	Unit
Cycle Time	tCYC	4.0	6.0	ns
Clock Access Time	tCD	2.6	3.5	ns
Output Enable Access Time	tOE	2.6	3.5	ns
Operating Current	I _{CC}	300	250	mA
Standby Current	I _{SB2}	120	120	mA

36Mb NTSRAM Pipelined Ordering Information

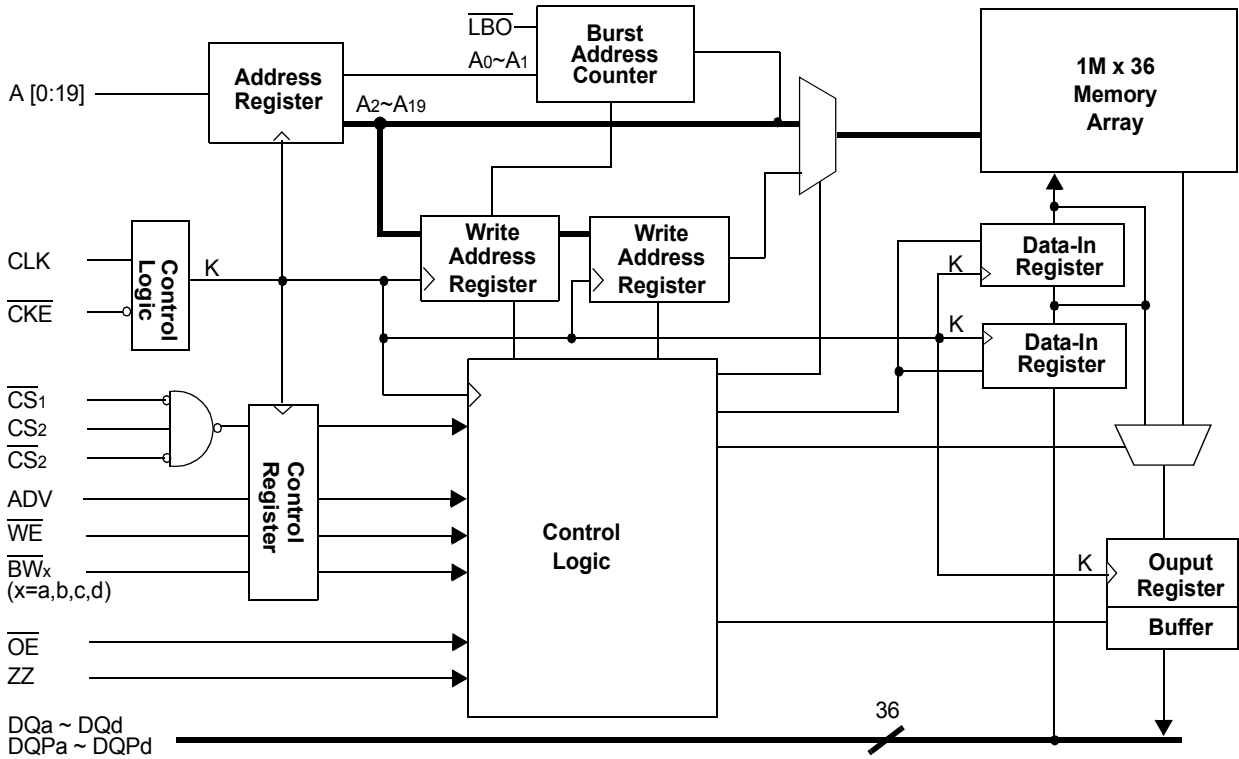
Org.	VDD (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
2Mx18	1.8	4.0	3.0	S7N321831M-P(E)C(I)25	0
	3.3/2.5	4.0	2.6	S7N321831M-P(E)C(I)25	0
	3.3/2.5/1.8	6.0	3.5	S7N321831M-P(E)C(I)16	0
1Mx36	1.8	4.0	3.0	S7N323631M-P(E)C(I)25	0
	3.3/2.5	4.0	2.6	S7N323631M-P(E)C(I)25	0
	3.3/2.5/1.8	6.0	3.5	S7N323631M-P(E)C(I)16	0

Note 1. P [Package type] : P - 100TQFP Pb Free, E - 165FBGA Pb Free
2. C(I) [Operating Temperature] : C-Commercial, I-Industrial

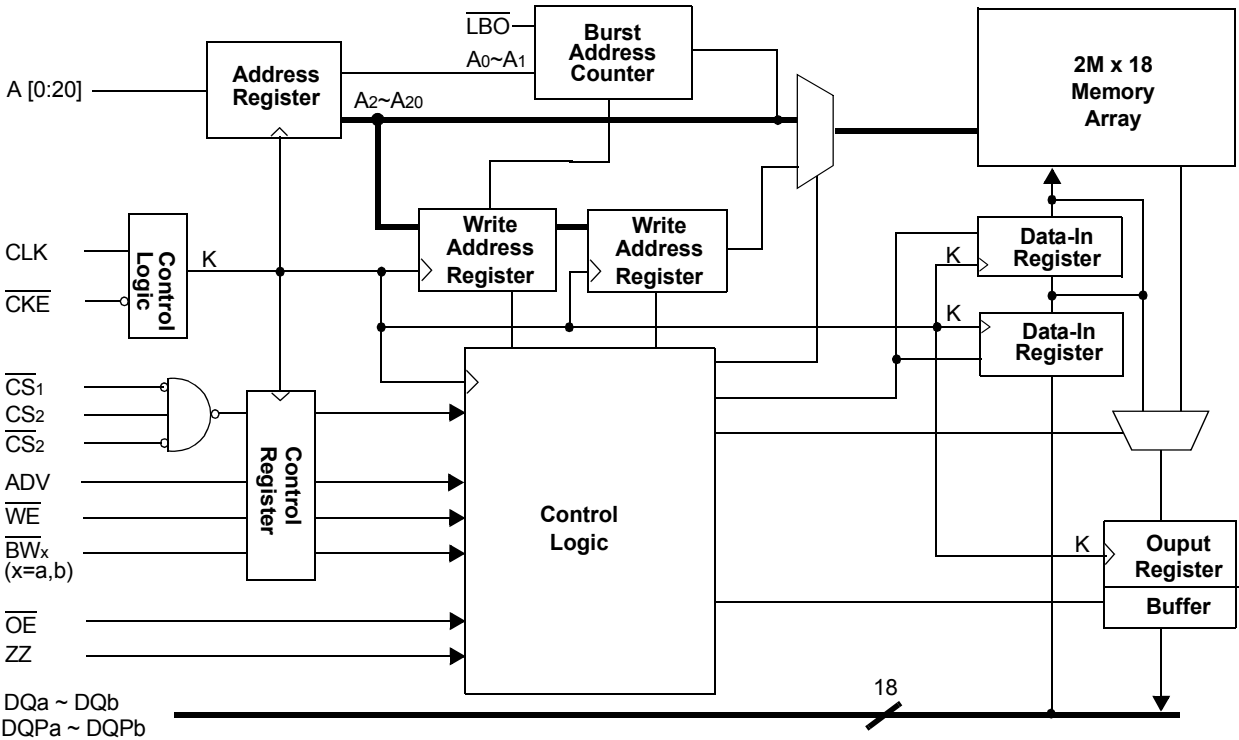
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1Mx36 & 2Mx18 NTSRAM Sync-Pipelined Burst

Logic Block Diagram - S7N323631M (1M x 36)



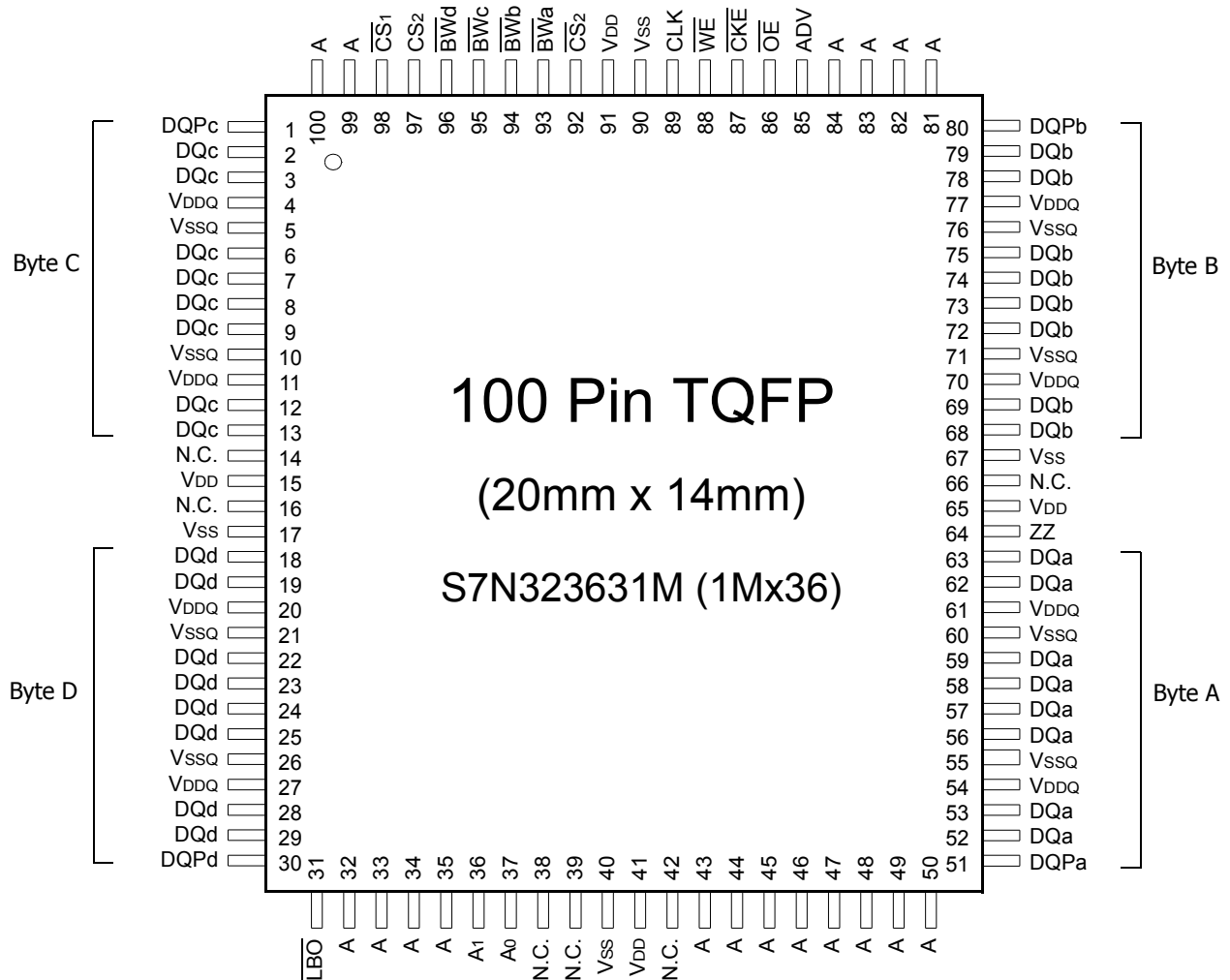
Logic Block Diagram - S7N321831M (2M x 18)



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100 TQFP Package Pin Configurations (Top View)



Pin Name

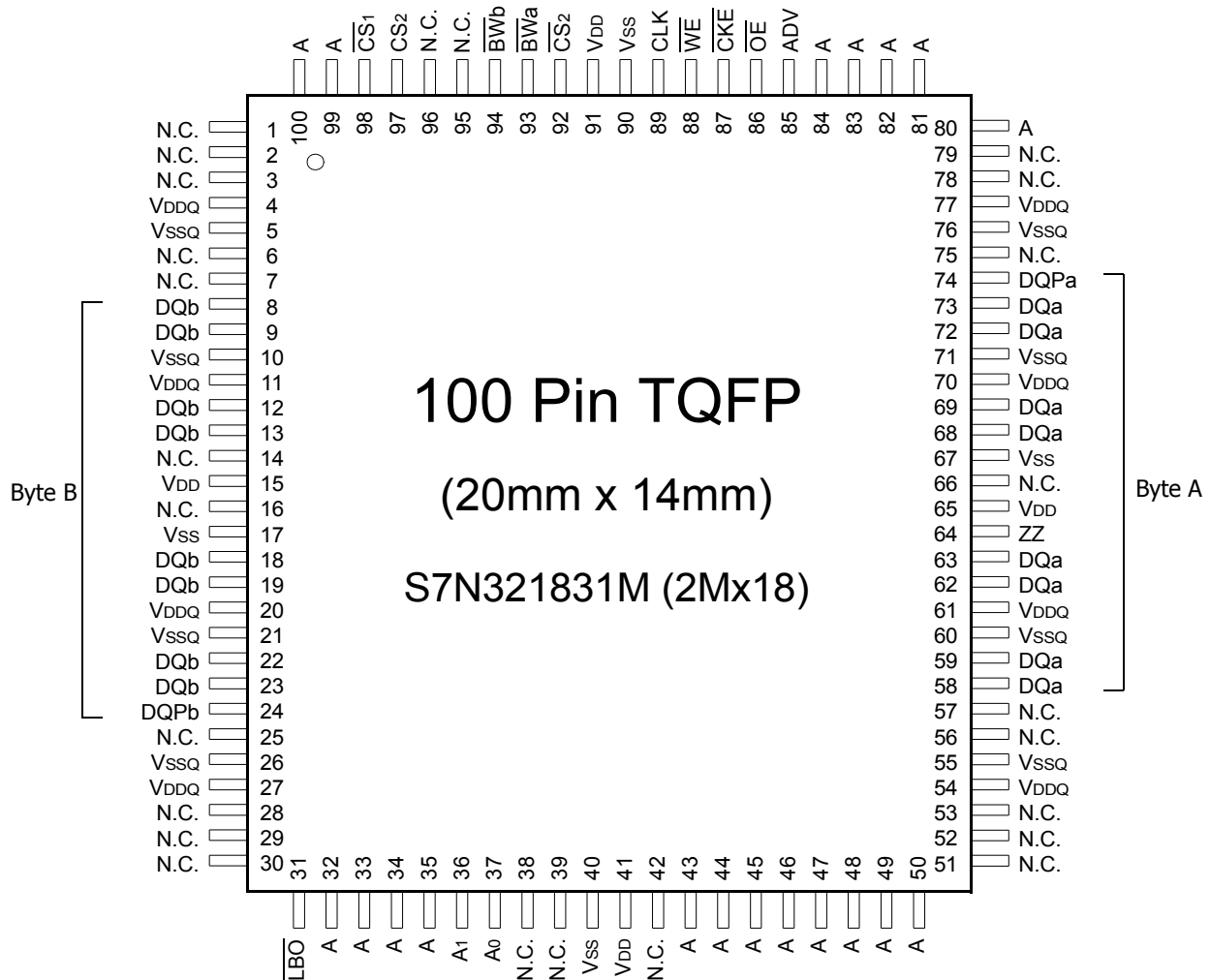
Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,43,44,45,46,47,48,49,50,81,82,83,84,99,100	VDD	Power Supply	15,41,65,91
A0,A1	Burst Address Inputs	37,36	VSS	Ground	17,40,67,90
ADV	Address Advance/Load	85	N.C.	No Connect	14,16,38,39,42,66
\overline{WE}	Read/Write Control Input	88	DQa	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb	Data Inputs/Outputs	68,69,72,73,74,75,78,79
CKE	Clock Enable	87	DQc	Data Inputs/Outputs	2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd	Data Inputs/Outputs	18,19,22,23,24,25,28,29
$\overline{CS2}$	Chip Select	97	DQPa~Pd	Data Inputs/Outputs	51,80,1,30
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{BWx(x=a,b,c,d)}$	Byte Write Inputs	93,94,95,96	VSSQ	Output Ground	5,10,21,26,55,60,71,76
OE	Output Enable	86			
ZZ	Power Sleep Mode	64			
\overline{LBO}	Burst Mode Control	31			

Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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100 TQFP Package Pin Configurations(Top View)



Pin Name

Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,43,44,45,46,47,48,49,50,80,81,82,83,84,99,100	VDD	Power Supply	15,41,65,91
A0,A1	Burst Address Inputs	37,36	VSS	Ground	17,40,67,90
ADV	Address Advance/Load	85	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29,30,38,39,42,51,52,53,56,57,66,75,78,79,95,96
WE	Read/Write Control Input	88	DQa	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CLK	Clock	89	DQb	Data Inputs/Outputs	8,9,12,13,18,19,22,23
CKE	Clock Enable	87	DQPa,DQPb	Data Inputs/Outputs	74,24
CS1	Chip Select	98	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
CS2	Chip Select	97	VSSQ	Output Ground	5,10,21,26,55,60,71,76
CS2	Chip Select	92			
BWx(x=a,b)	Byte Write Inputs	93,94			
OE	Output Enable	86			
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

NOTE : A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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165FBGA PKG Pin Configurations - S7N323631M (1Mx36) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CS1}$	\overline{BWc}	\overline{BWb}	$\overline{CS2}$	\overline{CKE}	ADV	A	A	NC
B	NC	A	CS2	\overline{BWd}	\overline{BWa}	CLK	\overline{WE}	\overline{OE}	A	A	NC
C	DQP _c	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQP _b
D	DQ _c	DQ _c	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _b	DQ _b
E	DQ _c	DQ _c	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _b	DQ _b
F	DQ _c	DQ _c	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _b	DQ _b
G	DQ _c	DQ _c	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _b	DQ _b
H	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQ _d	DQ _d	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _a	DQ _a
K	DQ _d	DQ _d	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _a	DQ _a
L	DQ _d	DQ _d	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _a	DQ _a
M	DQ _d	DQ _d	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _a	DQ _a
N	DQP _d	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQP _a
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	\overline{LBO}	A	A	A	TMS	A0*	TCK	A	A	A	A

Notes: * A0 and A1 are two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

Pin Name

Symbol	Pin Name	Symbol	Pin Name
A	Address Inputs	TCK	JTAG Test Clock
A0,A1	Burst Address Inputs	TMS	JTAG Test Mode Select
ADV	Address Advance/Load	TDI	JTAG Test Data Input
\overline{WE}	Read/Write Control Input	TDO	JTAG Test Data Output
CLK	Clock	VDD	Power Supply
\overline{CKE}	Clock Enable	VSS	Ground
$\overline{CS1}$	Chip Select	NC	No Connect
CS2	Chip Select		
$\overline{CS2}$	Chip Select		
$\overline{BWx(x=a,b,c,d)}$	Byte Write Inputs	DQa, DQb, DQc, DQd	Data Inputs/Outputs
\overline{OE}	Output Enable	DQP _a , DQP _b	Data Inputs/Outputs
ZZ	Power Sleep Mode	DQP _c , DQP _d	Data Inputs/Outputs
\overline{LBO}	Burst Mode Control	VDDQ	Output Power Supply

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165FBGA PKG Pin Configurations - S7N321831M (2Mx18) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CS1}$	$\overline{BW_b}$	NC	$\overline{CS2}$	\overline{CKE}	ADV	A	A	A
B	NC	A	CS2	NC	$\overline{BW_a}$	CLK	\overline{WE}	\overline{OE}	A	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQP _a
D	NC	DQ _b	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQ _a
E	NC	DQ _b	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQ _a
F	NC	DQ _b	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQ _a
G	NC	DQ _b	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQ _a
H	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQ _b	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _a	NC
K	DQ _b	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _a	NC
L	DQ _b	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _a	NC
M	DQ _b	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQ _a	NC
N	DQP _b	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	\overline{LBO}	A	A	A	TMS	A0*	TCK	A	A	A	A

Notes: * A0 and A1 are two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

Pin Name

Symbol	Pin Name	Symbol	Pin Name
A	Address Inputs	TCK	JTAG Test Clock
A0,A1	Burst Address Inputs	TMS	JTAG Test Mode Select
ADV	Address Advance/Load	TDI	JTAG Test Data Input
\overline{WE}	Read/Write Control Input	TDO	JTAG Test Data Output
CLK	Clock	VDD	Power Supply
\overline{CKE}	Clock Enable	VSS	Ground
$\overline{CS1}$	Chip Select	NC	No Connect
CS2	Chip Select		
$\overline{CS2}$	Chip Select		
$\overline{BWx(x=a,b)}$	Byte Write Inputs	DQ _a , DQ _b	Data Inputs/Outputs
\overline{OE}	Output Enable	DQP _a , DQP _b	Data Inputs/Outputs
ZZ	Power Sleep Mode	VDDQ	Output Power Supply
\overline{LBO}	Burst Mode Control		

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Function Description

The S7N323631M and S7N321831M are NTSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of \overline{OE} , \overline{LBO} and \overline{ZZ}) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable(\overline{CKE}) pin allows the operation of the chip to be suspended as long as necessary. When \overline{CKE} is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

NTSRAM latches external address and initiates a cycle, when \overline{CKE} , ADV are driven to low and all three chip enables($\overline{CS1}$, $\overline{CS2}$, $\overline{CS2}$) are active. Output Enable(\overline{OE}) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, \overline{CKE} is driven low, all three chip enables($\overline{CS1}$, $\overline{CS2}$, $\overline{CS2}$) are active, the write enable input signals \overline{WE} are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. Also during read operation \overline{OE} must be driven low for the device to drive out the requested data.

Write operation occurs when \overline{WE} is driven low at the rising edge of the clock. \overline{BW} [d:a] can be used for byte write operation. The pipelined NTSRAM uses a late-late write cycle to utilize 100% of the bandwidth.

At the first rising edge of the clock, \overline{WE} and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the \overline{LBO} pin. When this pin is low, linear burst sequence is selected.

And when this pin is high, Interleaved burst sequence is selected.

During normal operation, \overline{ZZ} must be driven low. When \overline{ZZ} is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When \overline{ZZ} returns to low, the SRAM normally operates after 2 cycles of wake up time.

Burst Sequence Table

(Interleaved Burst, \overline{LBO} =High)

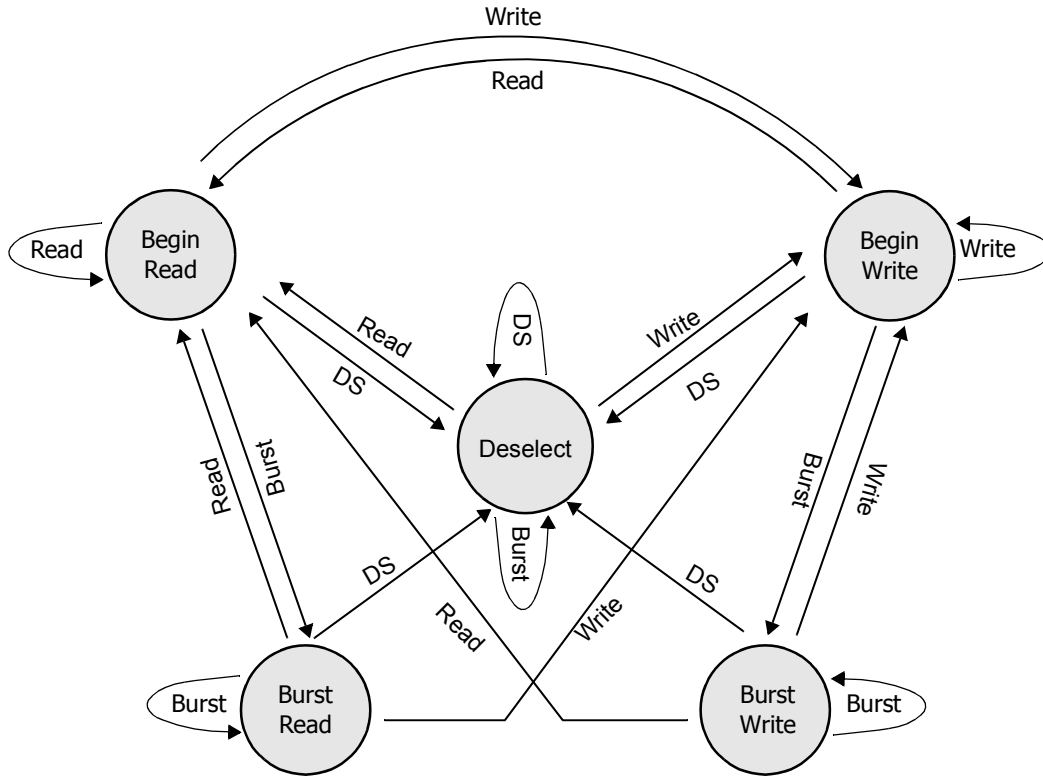
\overline{LBO} PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst, \overline{LBO} =Low)

\overline{LBO} PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. \overline{LBO} pin must be tied to High or Low, and Floating State must not be allowed.

State Diagram For NTSRAM



Command	Action
DS	Deselect
Read	Begin Read
Write	Begin Write
Burst	Begin Read Begin Write Continue Deselect

Notes : 1. An Ignore Clock Edge cycle is not shown in the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

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Truth Tables

Synchronous Truth Table

\overline{CS}_1	CS_2	\overline{CS}_2	ADV	\overline{We}	\overline{BW}_x	\overline{OE}	\overline{CKE}	CLK	Address Accessed	Operation
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

Notes : 1. X means "Don't Care".

- The rising edge of clock is symbolized by (↑).
- A continue deselect cycle can only be entered if a deselect cycle is executed first.
- $\overline{We} = L$ means Write operation in Write Truth Table.
 $\overline{We} = H$ means Read operation in Write Truth Table.
- Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

Write Truth Table(x36)

\overline{WE}	\overline{BW}_a	\overline{BW}_b	\overline{BW}_c	\overline{BW}_d	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

Notes : 1. X means "Don't Care".

- All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

Write Truth Table(x18)

\overline{WE}	\overline{BW}_a	\overline{BW}_b	Operation
H	X	X	Read
L	L	H	Write Byte a
L	H	L	Write Byte b
L	L	L	Write All Bytes
L	H	H	Write Abort/NOP

Notes : 1. X means "Don't Care".

- All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

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Asynchronous Truth Table

Operation	ZZ	\overline{OE}	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.3 to 4.6	V	
Voltage on Any Other Pin Relative to V _{SS}	V _{IN}	-0.3 to V _{DD} +0.3	V	
Power Dissipation	P _D	1.6	W	
Storage Temperature	T _{STG}	-65 to 150	°C	
Operating Temperature	Commercial	T _{OPR}	0 to 70	°C
	Industrial	T _{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias	T _{BIAS}	-10 to 85	°C	

Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V _{DD1}	1.7	1.8	2.0	V
	V _{DDQ1}	1.7	1.8	2.0	V
	V _{DD2}	2.3	2.5	2.7	V
	V _{DDQ2}	1.7	2.5	2.7	V
	V _{DD3}	3.1	3.3	3.5	V
	V _{DDQ3}	2.3	3.3	3.5	V
Ground	V _{SS}	0	0	0	V

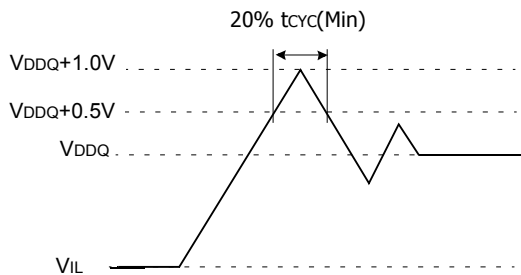
- Notes:** 1. The above parameters are also guaranteed at industrial temperature range.
2. It should be $V_{DDQ} \leq V_{DD}$

Capacitance (T_A=25°C, f=1MHz)

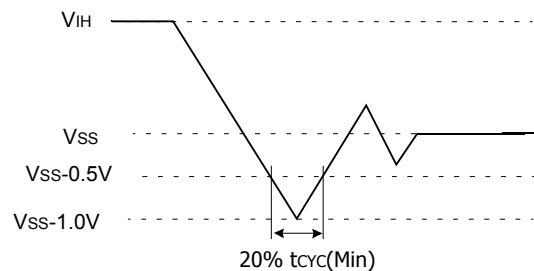
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C _{IN}	V _{IN} =0V	-	5	pF
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	7	pF

Note : Sampled not 100% tested.

Overshoot Timing



Undershoot Timing



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DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit	Notes	
Input Leakage Current(except ZZ)	IIL	VDD=Max ; VIN=VSS to VDD	-2	+2	uA		
Output Leakage Current	IOL	Output Disabled, Vout=VSS to VDDQ	-2	+2	uA		
Operating Current	ICC	Device Selected, IOUT=0mA, ZZ ≤ VIL, Cycle Time ≥ tcyc Min	-25	-	300	mA	1,2
			-16	-	250		
Standby Current	ISB	Device deselected, IOUT=0mA, ZZ ≤ VIL, f=Max, All Inputs ≤ VIL or ≥ VIH	-25	-	130	mA	
			-16	-	125		
	ISB1	Device deselected, IOUT=0mA, ZZ ≤ 0.2V, f=0, All Inputs=fixed (VDD-0.2V or 0.2V)	-	-	120	mA	
ISB2	Device deselected, IOUT=0mA, ZZ ≥ VDD-0.2V, f=Max, All Inputs ≤ VIL or ≥ VIH	-	-	120			
Output Low Voltage(3.3V I/O)	VOL	IOL=8.0mA	-	0.4	V		
Output High Voltage(3.3V I/O)	VOH	IOH=-4.0mA	2.4	-	V		
Output Low Voltage(2.5V I/O)	VOL	IOL=1.0mA	-	0.4	V		
Output High Voltage(2.5V I/O)	VOH	IOH=-1.0mA	2.0	-	V		
Output Low Voltage(1.8V I/O)	VOL	IOL=1.0mA	-	0.4	V		
Output High Voltage(1.8V I/O)	VOH	IOH=-1.0mA	VDDQ-0.4	-	V		
Input Low Voltage(3.3V I/O)	VIL		-0.3*	0.8	V		
Input High Voltage(3.3V I/O)	VIH		2.0	VDD+0.3**	V	3	
Input Low Voltage(2.5V I/O)	VIL		-0.3*	0.7	V		
Input High Voltage(2.5V I/O)	VIH		1.7	VDD+0.3**	V	3	
Input Low Voltage(1.8V I/O)	VIL		-0.3*	VDD x 0.3	V		
Input High Voltage(1.8V I/O)	VIH		VDD x 0.6	VDD+0.3**	V		

Notes : The above parameters are also guaranteed at industrial temperature range.

1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. VIH=VDDQ+0.3V

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1Mx36 & 2Mx18 NTSRAM Sync-Pipelined Burst

Test Conditions

Parameter	Value
Input Pulse Level for 3.3V I/O	0 to 3.0V
Input Pulse Level for 2.5V I/O	0 to 2.5V
Input Pulse Level for 1.8V I/O	0 to 1.8V
Input Rise and Fall Time (Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O and 1.8V I/O	V _{DDQ} /2
Output Load	See Fig. 1

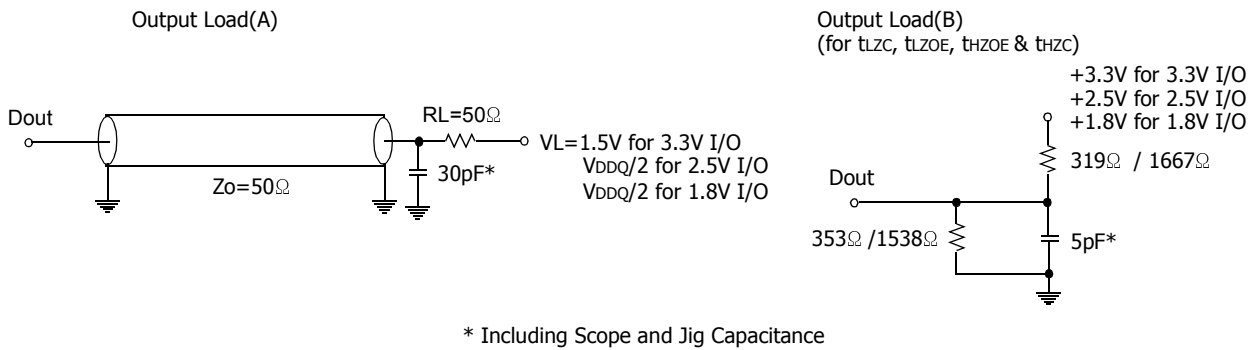


Fig. 1

S7N323631M
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1Mx36 & 2Mx18 NTSRAM Sync-Pipelined Burst

AC Timing Characteristics

Parameter	Symbol	-25		-16		Unit
		Min	Max	Min	Max	
Cycle Time	t _{CYC}	4.0	-	6.0	-	ns
Clock Access Time (V _{dd} =2.5V and 3.3V)	t _{CD}	-	2.6	-	3.5	ns
Clock Access Time (V _{dd} =1.8V)		-	3.0	-	3.5	ns
Output Enable to Data Valid (V _{dd} =2.5V and 3.3V)	t _{OE}	-	2.6	-	3.5	ns
Output Enable to Data Valid (V _{dd} =1.8V)		-	3.0	-	3.5	ns
Clock High to Output Low-Z	t _{LZC}	1.5	-	1.5	-	ns
Output Hold from Clock High	t _{OH}	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t _{LZOE}	0	-	0	-	ns
Output Enable High to Output High-Z	t _{HZOE}	-	2.6	-	3.0	ns
Clock High to Output High-Z	t _{HZC}	-	2.6	-	3.0	ns
Clock High Pulse Width	t _{CH}	1.7	-	2.2	-	ns
Clock Low Pulse Width	t _{CL}	1.7	-	2.2	-	ns
Address Setup to Clock High	t _{AS}	1.2	-	1.5	-	ns
$\overline{\text{CKE}}$ Setup to Clock High	t _{CES}	1.2	-	1.5	-	ns
Data Setup to Clock High	t _{DS}	1.2	-	1.5	-	ns
Write Setup to Clock High ($\overline{\text{WE}}$, $\overline{\text{BWx}}$)	t _{WS}	1.2	-	1.5	-	ns
Address Advance Setup to Clock High	t _{ADVS}	1.2	-	1.5	-	ns
Chip Select Setup to Clock High	t _{CSS}	1.2	-	1.5	-	ns
Address Hold from Clock High	t _{AH}	0.3	-	0.5	-	ns
$\overline{\text{CKE}}$ Hold from Clock High	t _{CEH}	0.3	-	0.5	-	ns
Data Hold from Clock High	t _{DH}	0.3	-	0.5	-	ns
Write Hold from Clock High ($\overline{\text{WE}}$, $\overline{\text{BWx}}$)	t _{WH}	0.3	-	0.5	-	ns
Address Advance Hold from Clock High	t _{ADVH}	0.3	-	0.5	-	ns
Chip Select Hold from Clock High	t _{CSH}	0.3	-	0.5	-	ns
ZZ High to Power Down	t _{PDS}	2	-	2	-	cycle
ZZ Low to Power Up	t _{PUS}	2	-	2	-	cycle

- Notes :**
- The above parameters are also guaranteed at industrial temperature range.
 - All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{\text{CS}}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 - Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
 - A write cycle is defined by $\overline{\text{WE}}$ low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{\text{WE}}$ High with ADV Low, Both cases must meet setup and hold times.
 - To avoid bus contention, At a given voltage and temperature t_{LZC} is more than t_{HZC}.
 The specs as shown do not imply bus contention because t_{LZC} is a Min. parameter that is worst case at totally different test conditions (0 °C, 3.5V) than t_{HZC}, which is a Max. parameter(worst case at 70 °C, 3.1V)
 It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

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Sleep Mode

Sleep Mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of Sleep Mode is dictated by the length of time the ZZ is in a High state.

After entering Sleep Mode, all inputs except ZZ become disabled and all outputs go to High-Z.

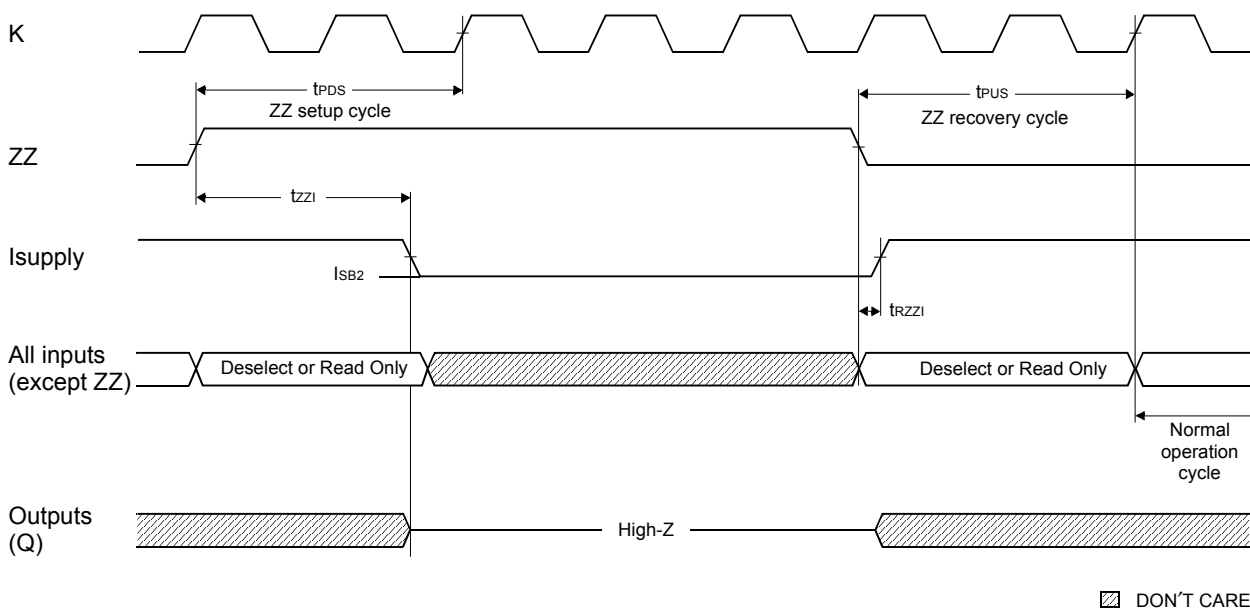
The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep Mode.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering Sleep Mode is not guaranteed to successful complete. Therefore, Sleep Mode (Read or Write) must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep Mode during t_{PUS} , only a Deselect or Read cycle should be given while the SRAM is transitioning out of Sleep Mode.

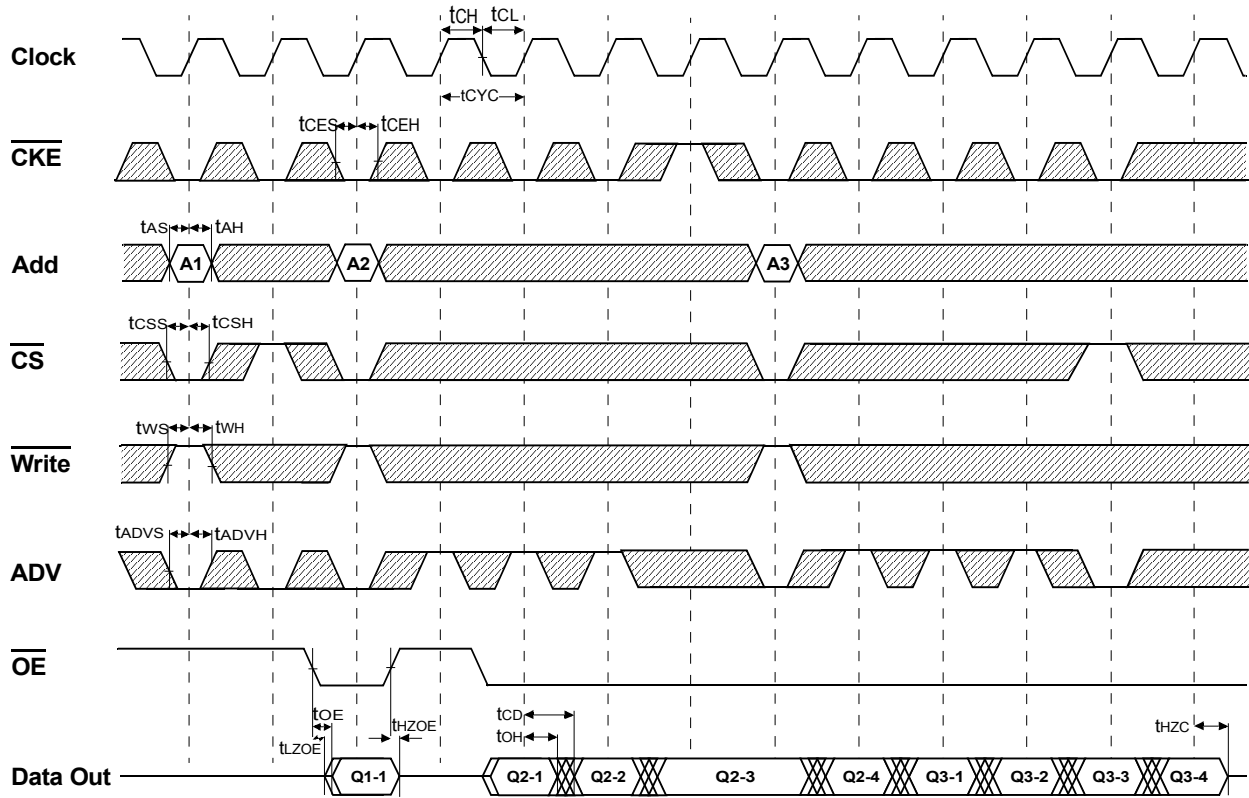
Sleep Mode Electrical Characteristics

Description	Condition	Symbol	Min	Max	Unit
Current during SLEEP MODE	$ZZ \geq V_{IH}$	I_{SB2}		120	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

Sleep Mode Waveform



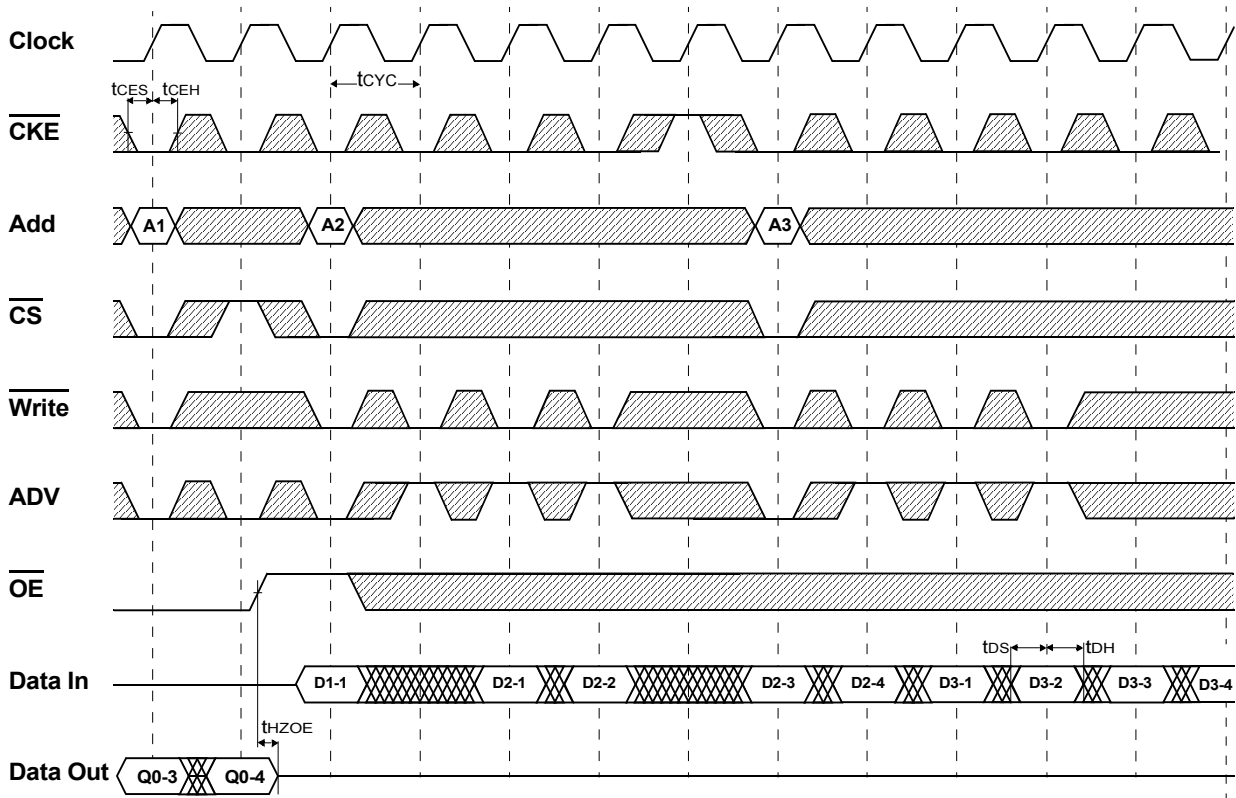
Timing Waveform Of Read Cycle



NOTES: $\overline{\text{Write}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\overline{\text{CS}}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\overline{\text{CS}}_2 = \text{L}$

☐ Don't Care
 ☒ Undefined

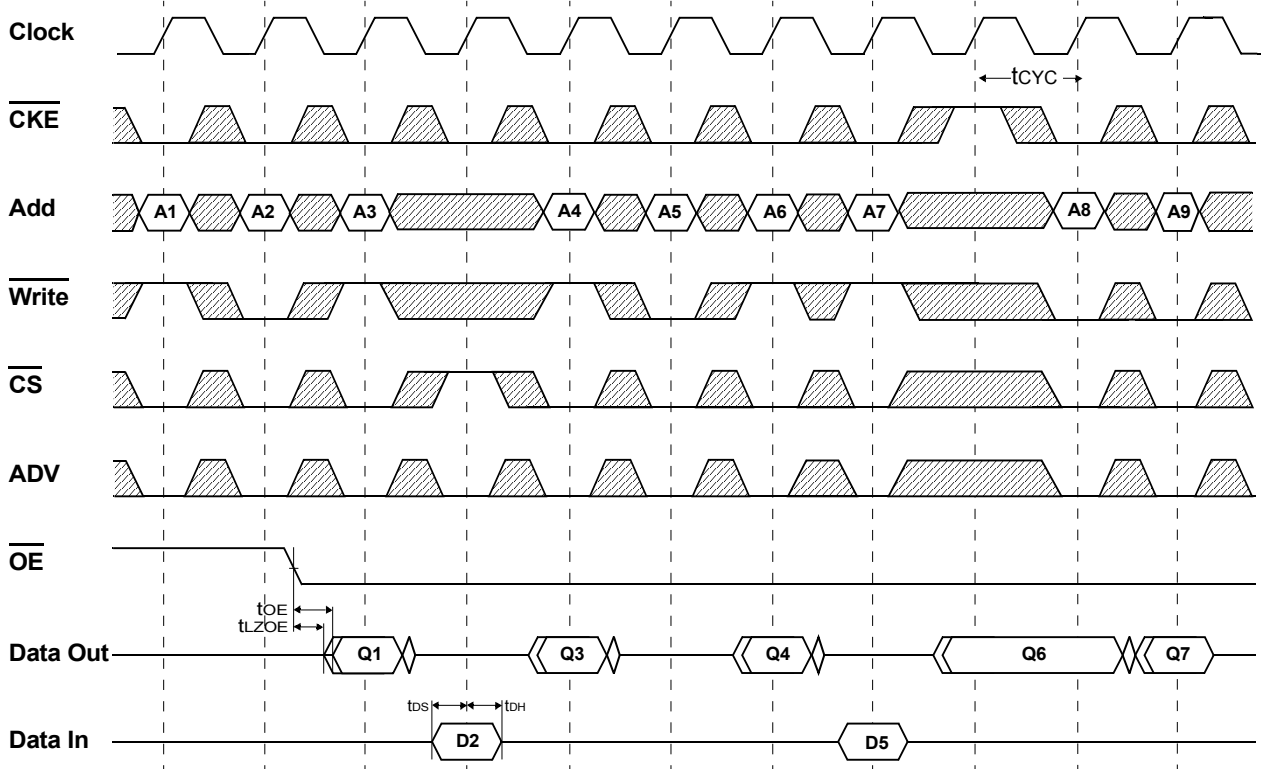
Timing Waveform Of Write Cycle



NOTES : $\overline{\text{Write}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\overline{\text{CS}}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\overline{\text{CS}}_2 = \text{L}$

☐ Don't Care
 ☒ Undefined

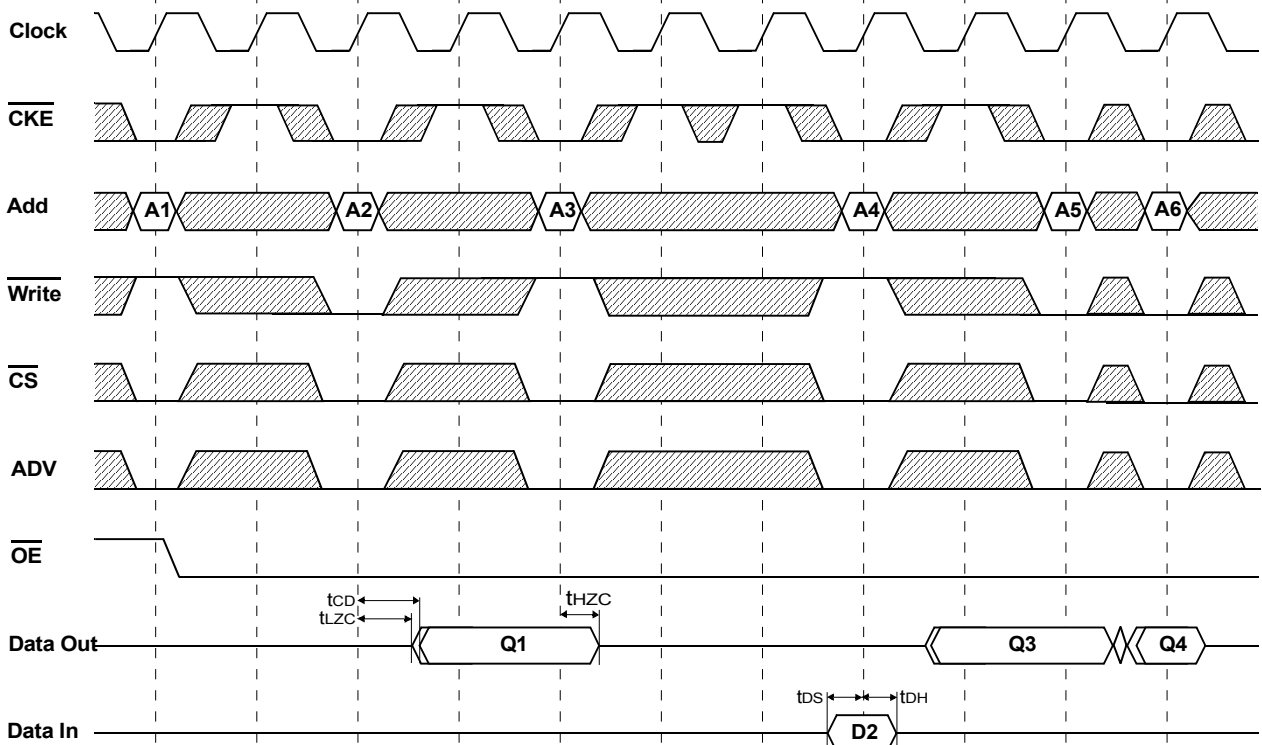
Timing Waveform Of Single Read/Write



NOTES: Write = L means $\overline{WE} = L$, and $\overline{BWx} = L$
 CS = L means $\overline{CS1} = L$, $CS2 = H$ and $\overline{CS2} = L$
 CS = H means $\overline{CS1} = H$, or $\overline{CS1} = L$ and $CS2 = H$, or $\overline{CS1} = L$, and $CS2 = L$

Don't Care
 Undefined

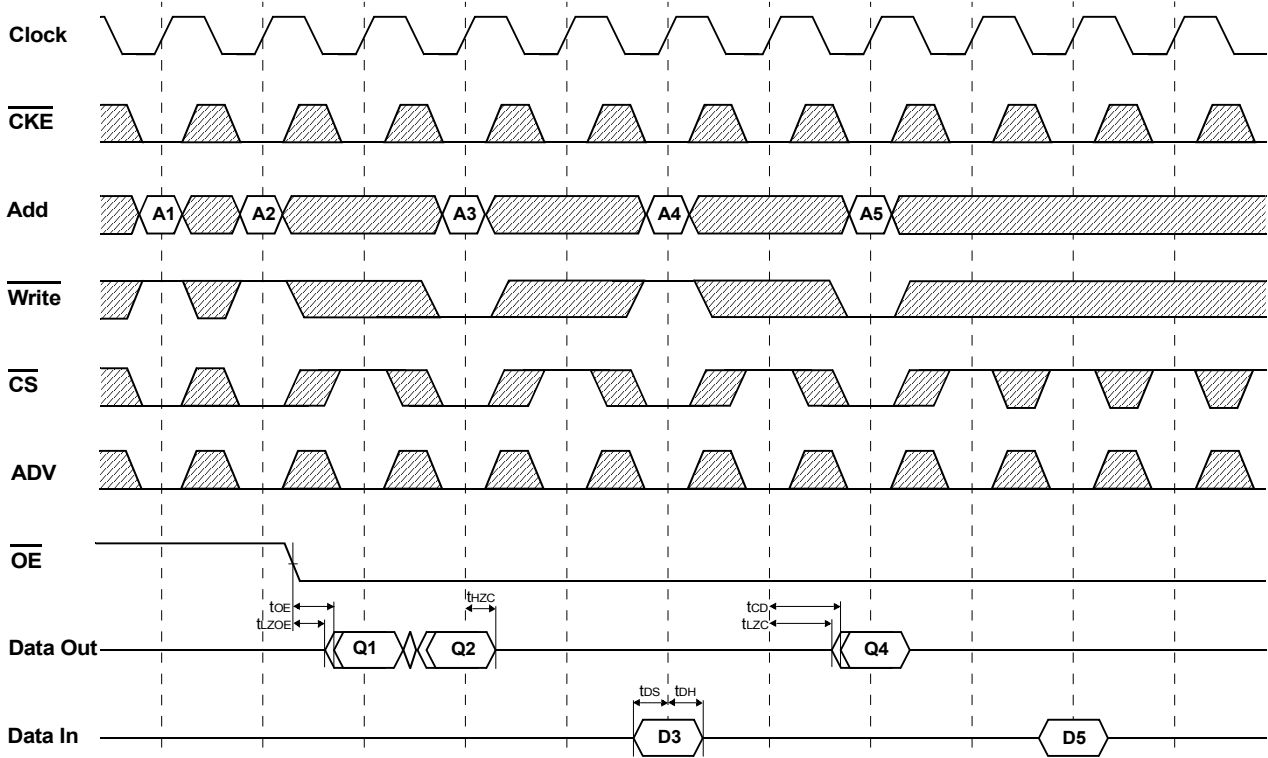
Timing Waveform Of $\overline{\text{CKE}}$ Operation



NOTES : $\overline{\text{Write}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\text{CS}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\text{CS}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\text{CS}_2 = \text{L}$

Don't Care
 Undefined

Timing Waveform Of \overline{CS} Operation



NOTES : $\overline{Write} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS}_1 = L$, $CS_2 = H$ and $\overline{CS}_2 = L$
 $\overline{CS} = H$ means $\overline{CS}_1 = H$, or $\overline{CS}_1 = L$ and $CS_2 = H$, or $\overline{CS}_1 = L$, and $CS_2 = L$

Don't Care
 Undefined

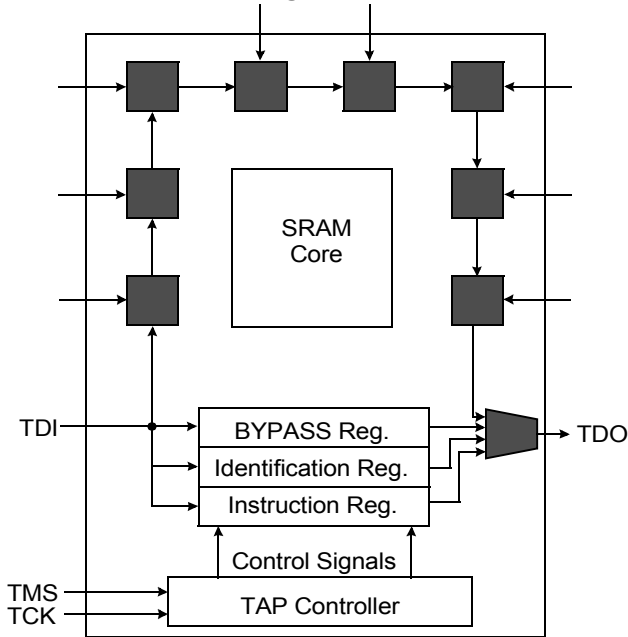
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1Mx36 & 2Mx18 NTSRAM Sync-Pipelined Burst

IEEE 1149.1 Test Access Port and Boundary Scan-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



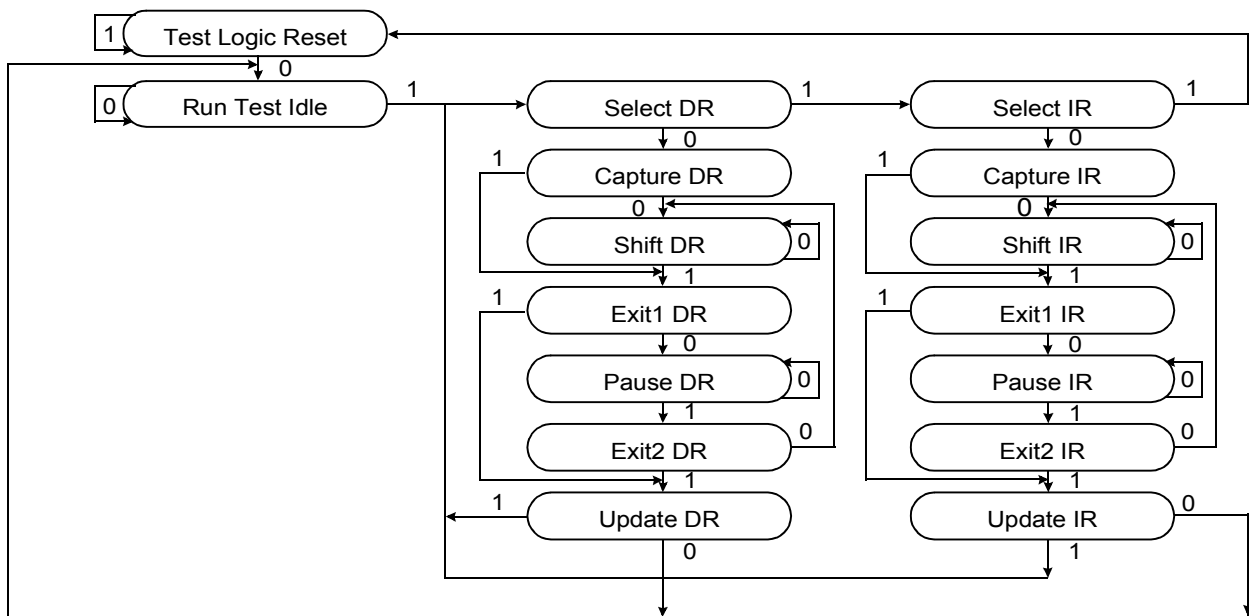
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	BYPASS	Bypass Register	4
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	BYPASS	Bypass Register	4
1	1	1	BYPASS	Bypass Register	4

NOTE:

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram



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Scan Register Definition

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1M x 36 2M x 18	3 bits	1 bit	32 bits	76 bits

ID Registration Definition

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Netsol JEDEC Code (11: 1)	Start Bit(0)
1M x 36	0000	01000 00100	000000	01111011001	1
2M x 18	0000	01001 00011	000000	01111011001	1

Boundary Scan Exit Order

BIT	Pin ID (x18)	Pin ID (x36)
1	6N	6N
2	8P	8P
3	8R	8R
4	9R	9R
5	9P	9P
6	10P	10P
7	10R	10R
8	11R	11R
9	11P	11P
10	11H	11H
11	11N	11N
12	11M	11M
13	11L	11L
14	11K	11K
15	11J	11J
16	10M	10M
17	10L	10L
18	10K	10K
19	10J	10J
20	11G	11G
21	11F	11F
22	11E	11E
23	11D	11D
24	11C	10G
25	10F	10F
26	10E	10E
27	10D	10D
28	10G	11C
29	11A	11A
30	11B	11B
31	10A	10A
32	10B	10B
33	9A	9A
34	9B	9B
35	8A	8A
36	8B	8B
37	7A	7A
38	7B	7B
39	6B	6B

BIT	Pin ID (x18)	Pin ID (x36)
40	6A	6A
41	5B	5B
42	5A	5A
43	4A	4A
44	4B	4B
45	3B	3B
46	3A	3A
47	2A	2A
48	2B	2B
49	1B	1B
50	1A	1A
51	1C	1C
52	1D	1D
53	1E	1E
54	1F	1F
55	1G	1G
56	2D	2D
57	2E	2E
58	2F	2F
59	2G	2G
60	1J	1J
61	1K	1K
62	1L	1L
63	1M	1M
64	1N	2J
65	2K	2K
66	2L	2L
67	2M	2M
68	2J	1N
69	2R	2R
70	1R	1R
71	3P	3P
72	3R	3R
73	4R	4R
74	4P	4P
75	6P	6P
76	6R	6R

Note: 1. NC pins are read as "X" (i.e. don't care.)

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JTAG DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage (3.3V)	V _{DD}	3.135	3.3	3.465	V	
Input High Level (3.3V I/O)	V _{IH}	2.0	-	V _{DD} +0.3	V	
Input Low Level (3.3V I/O)	V _{IL}	-0.3	-	0.8	V	
Output High Voltage (3.3V I/O)	V _{OH}	2.4	-	-	V	
Output Low Voltage (3.3V I/O)	V _{OL}	-	-	0.4	V	
Power Supply Voltage (2.5V)	V _{DD}	2.375	2.5	2.625	V	
Input High Level (2.5V I/O)	V _{IH}	1.7	-	V _{DD} +0.3	V	
Input Low Level (2.5V I/O)	V _{IL}	-0.3	-	0.7	V	
Output High Voltage (2.5V I/O)	V _{OH}	2.0	-	-	V	
Output Low Voltage (2.5V I/O)	V _{OL}	-	-	0.4	V	
Power Supply Voltage (1.8V)	V _{DD}	1.7	1.8	2.0	V	
Input High Level (1.8V I/O)	V _{IH}	V _{DD} x 0.6	-	V _{DD} +0.3	V	
Input Low Level (1.8V I/O)	V _{IL}	-0.3	-	V _{DD} x 0.3	V	
Output High Voltage (1.8V I/O)	V _{OH}	V _{DD} -0.4	-	-	V	
Output Low Voltage (1.8V I/O)	V _{OL}	-	-	0.4	V	

Note: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC Test Conditions

Parameter	Symbol	Min	Unit	Note
Input High/Low Level (3.3V I/O , 2.5V I/O , 1.8V I/O)	V _{IH} /V _{IL}	3.0/0 , 2.5/0 , 1.8/0	V	
Input Rise/Fall Time (3.3V I/O , 2.5V I/O , 1.8V I/O)	TR/TF	1.0/1.0 , 1.0/1.0 , 1.0/1.0	ns	
Input and Output Timing Reference Level		V _{DDQ} /2	V	

Note: 1. See SRAM AC test output load on page 11.

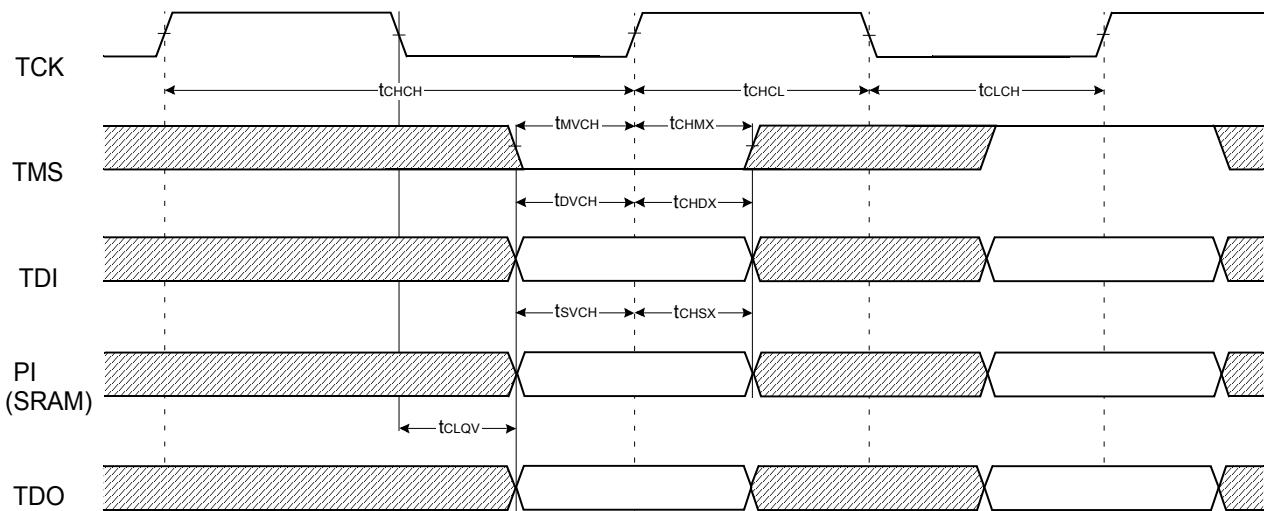
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JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tmVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tdVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
SRAM Input Setup Time	tsVCH	5	-	ns	
SRAM Input Hold Time	tCHSX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

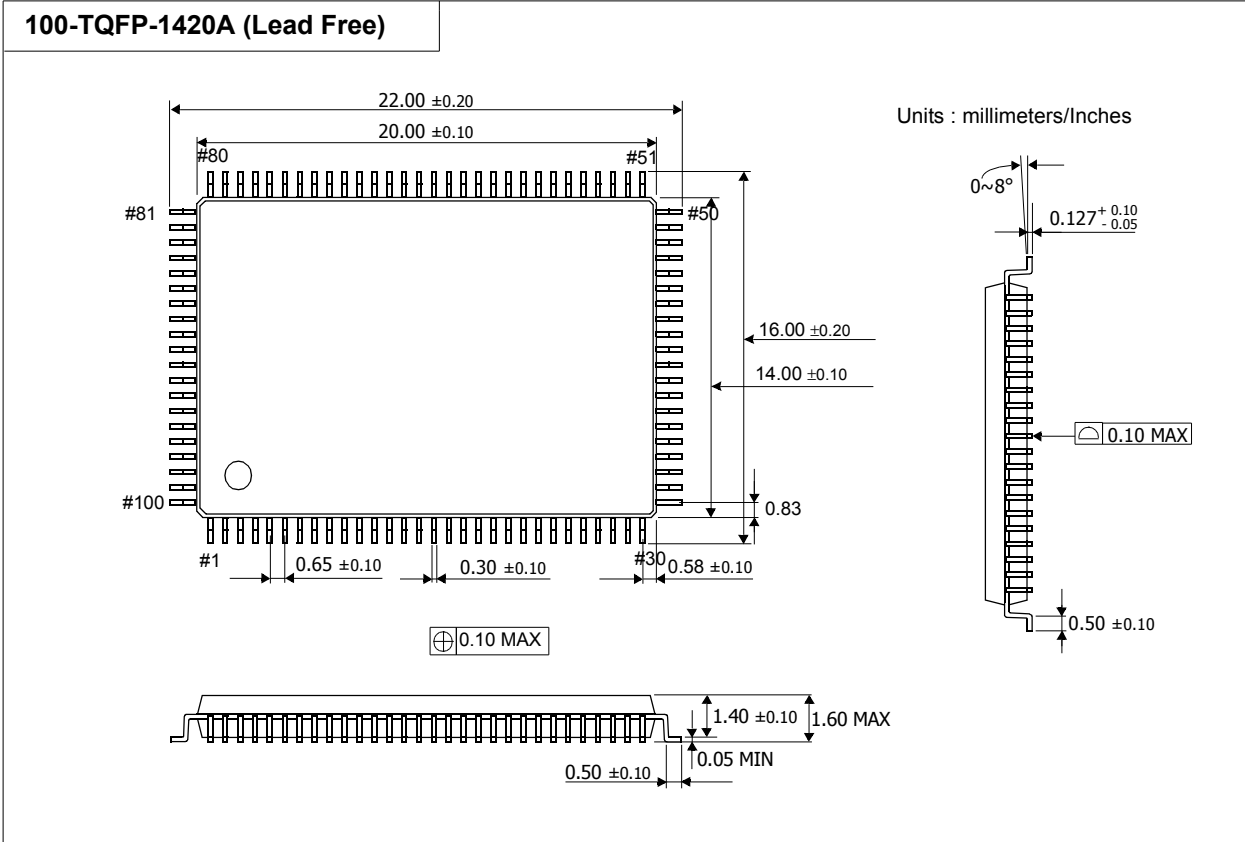
JTAG Timing Diagram



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Package Dimensions

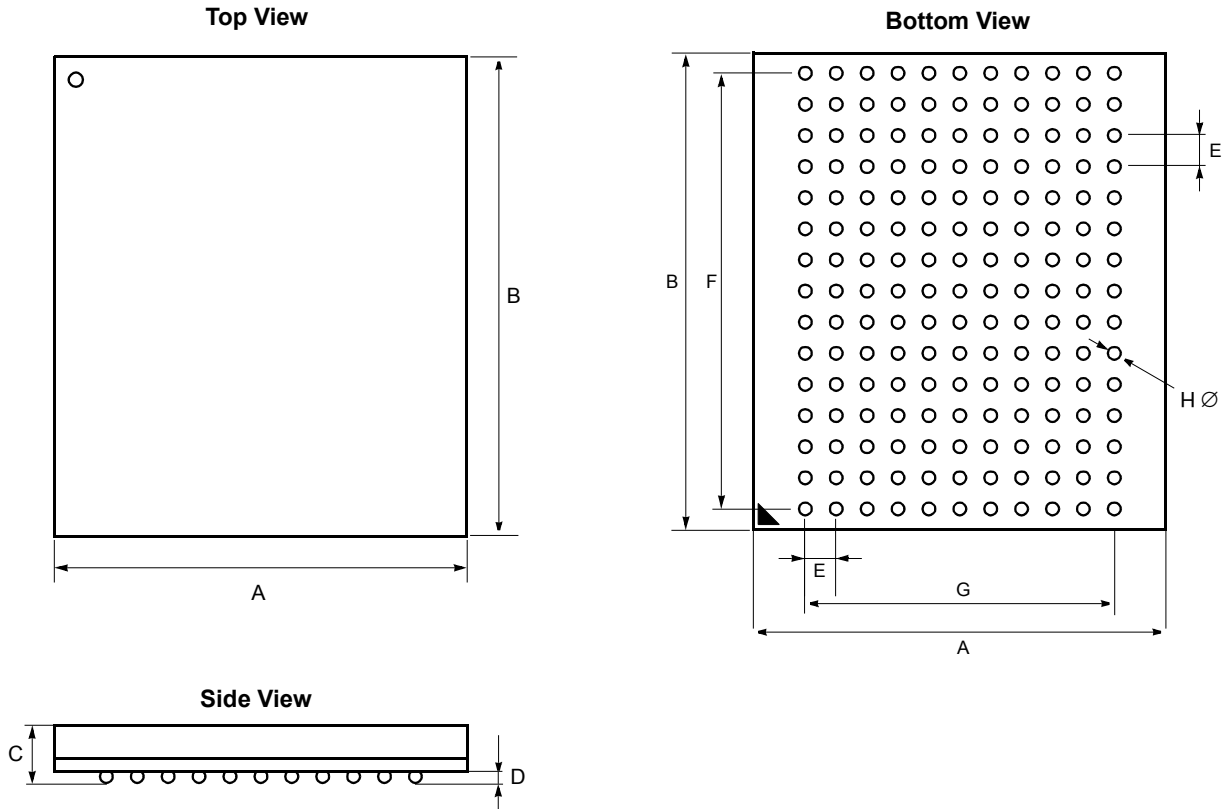


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1Mx36 & 2Mx18 NTSRAM Sync-Pipelined Burst

165 FBGA Package Dimensions (Lead Free)

13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Grid Array



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	13 ± 0.1	mm		E	1.0	mm	
B	15 ± 0.1	mm		F	14.0	mm	
C	1.3 ± 0.1	mm		G	10.0	mm	
D	0.35 ± 0.05	mm		H	0.5 ± 0.05	mm	