72Mb NTSRAM Sync-Pipelined Burst Specification

Document Title

2Mx36 & 4Mx18 Bit NTSRAM Synchronous Pipelined Burst

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Sep. 2012	Preliminary
0.1	Change 165FBGA H2 pin to NC from VDD	Oct. 2013	Preliminary
1.0	Final spec release	Nov. 2013	Final

2Mx36 & 4Mx18 Bit NTSRAM Synchronous Pipelined Burst

Features

- Fully registered inputs and outputs for pipelined operation
- V_{DD} = 2.5V(2.3V ~ 2.7V) or 3.3V(3.1V ~ 3.5V) Power Supply
- V_{DDQ} = 2.3V~2.7V I/O Power Supply (VDD=2.5V) or 2.3V~3.5V I/O Power Supply (VDD=3.3V)
- Byte Writable Function
- Enable clock and suspend operation
- Single Read/Write control pin
- Asynchronous output enable control
- Self-timed Write control
- Three Chip Enable for simple depth expansion with no data contention
- An interleaved burst or a linear burst mode
- Power Down mode
- Operating in commeical and industrial temperature range
- 100-TQFP-1420A (Lead free package)
- 165FBGA(11x15 ball array) with body size of 13mmx15mm. (Lead free package)

General Description

The S7N643631M and S7N641831M are 75,497,472-bits Synchronous Static SRAMs. The NTSRAM, or Non-Turnaround Static Random Access Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock.

Burst order control must be tied "High or Low". Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

The S7N643631M and S7N641831M are implemented with high performance CMOS technology and is available in 100pin TQFP package and 165FBGA package. Multiple power and ground pins minimize ground bounce.

Key Parameters

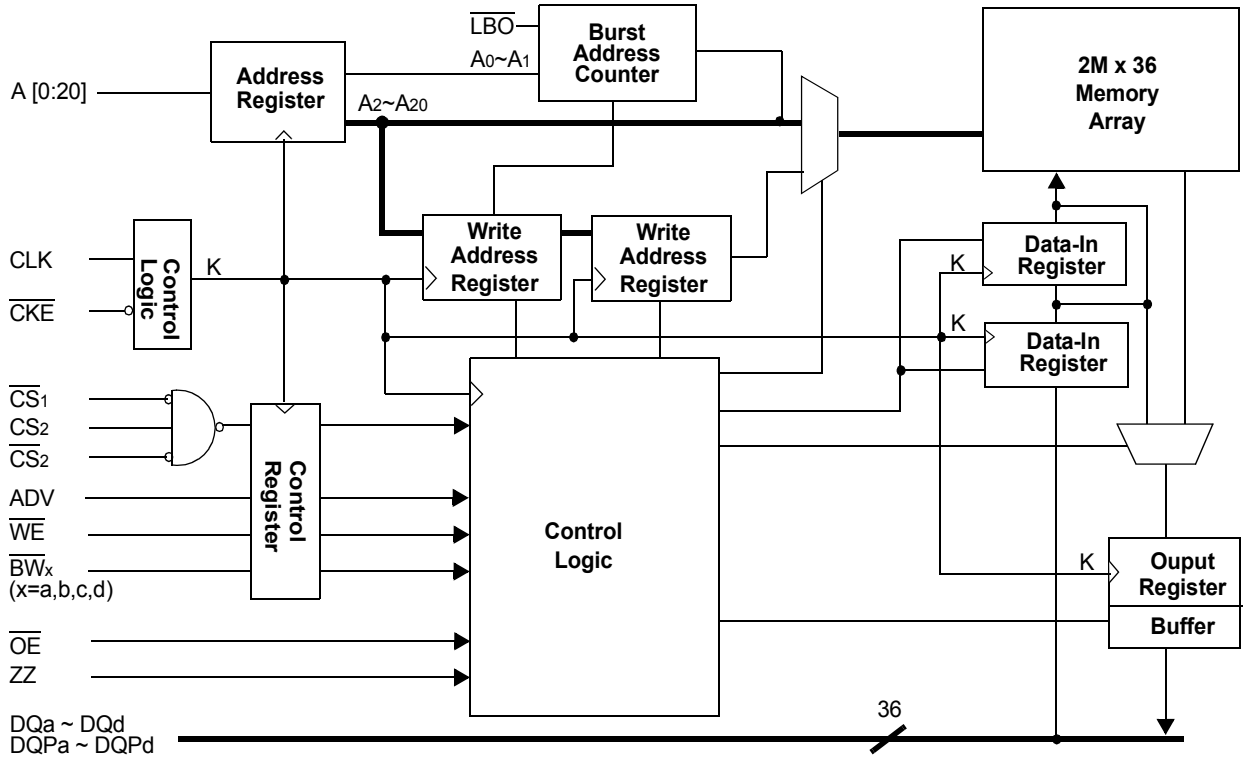
Parameter	Symbol	-25	-16	Unit
Cycle Time	tCYC	4.0	6.0	ns
Clock Access Time	tCD	2.6	3.5	ns
Output Enable Access Time	tOE	2.6	3.5	ns
Operating Current	I_{CC}	370	320	mA
Standby Current	I_{SB2}	200	200	mA

72Mb NTSRAM Pipelined Ordering Information

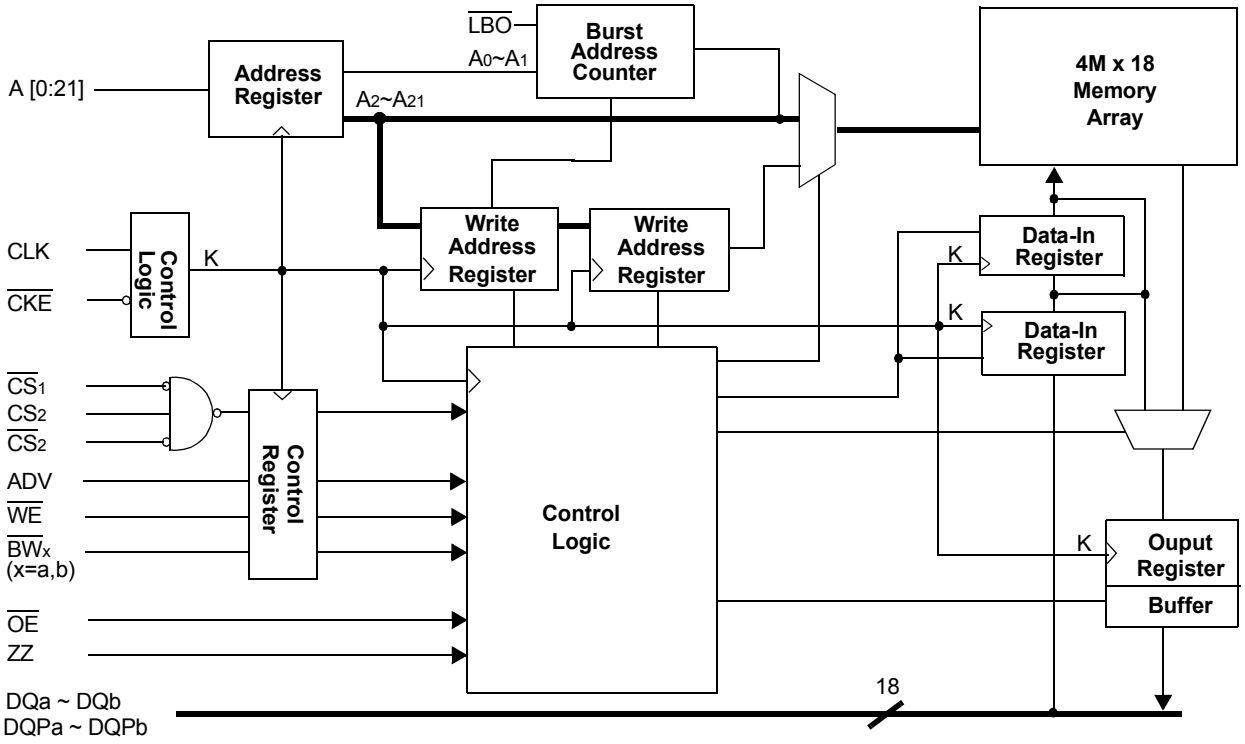
Org.	VDD (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
4Mx18	3.3/2.5	4.0	2.6	S7N641831M-P(E)C(I)25	O
	3.3/2.5	6.0	3.5	S7N641831M-P(E)C(I)16	O
2Mx36	3.3/2.5	4.0	2.6	S7N643631M-P(E)C(I)25	O
	3.3/2.5	6.0	3.5	S7N643631M-P(E)C(I)16	O

Note 1. P [Package type] : P - 100TQFP Pb Free, E - 165FBGA Pb Free
2. C(I) [Operating Temperature] : C-Commercial, I-Industrial

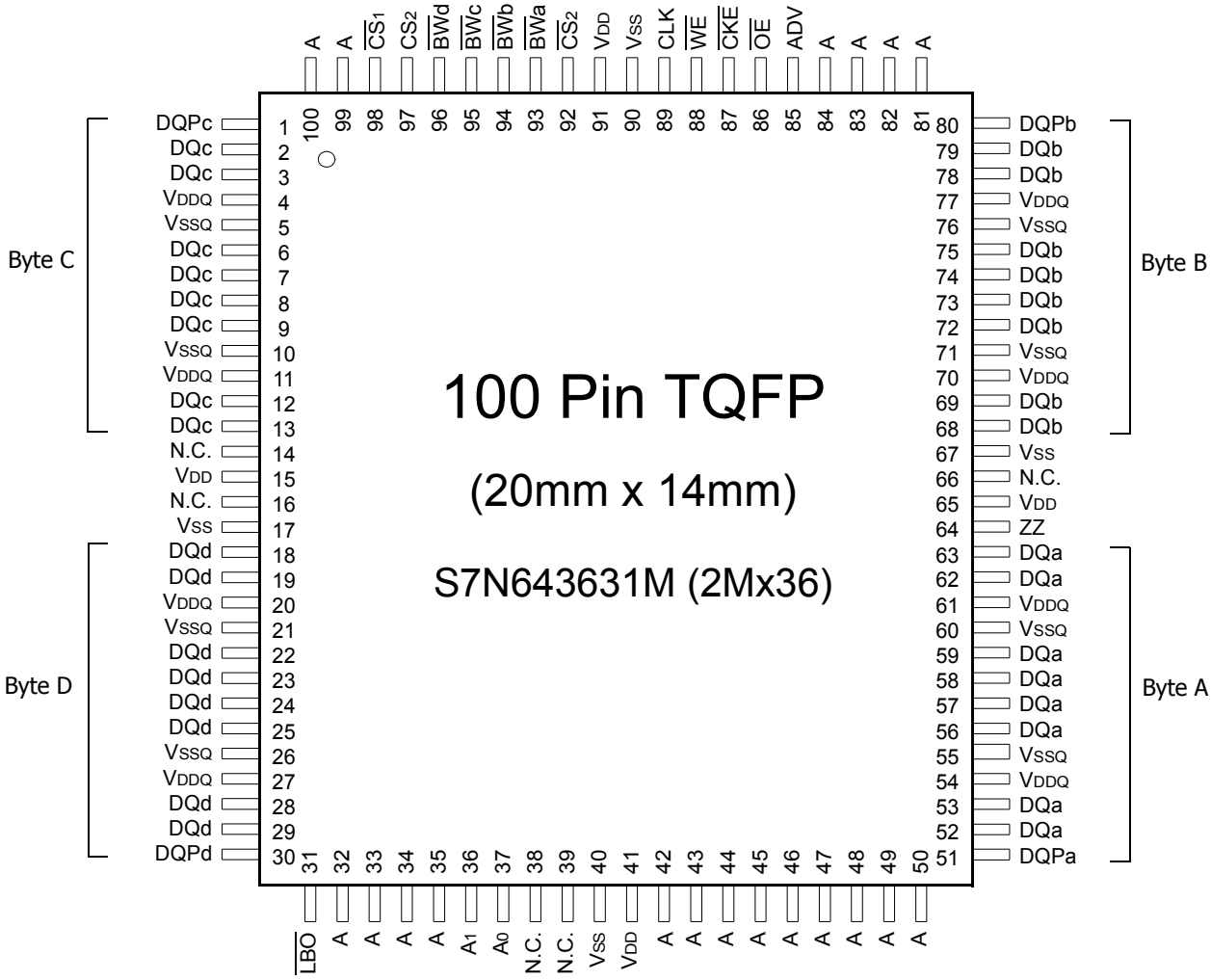
Logic Block Diagram - S7N643631M (2M x 36)



Logic Block Diagram - S7N641831M (4M x 18)



100 TQFP Package Pin Configurations(Top View)

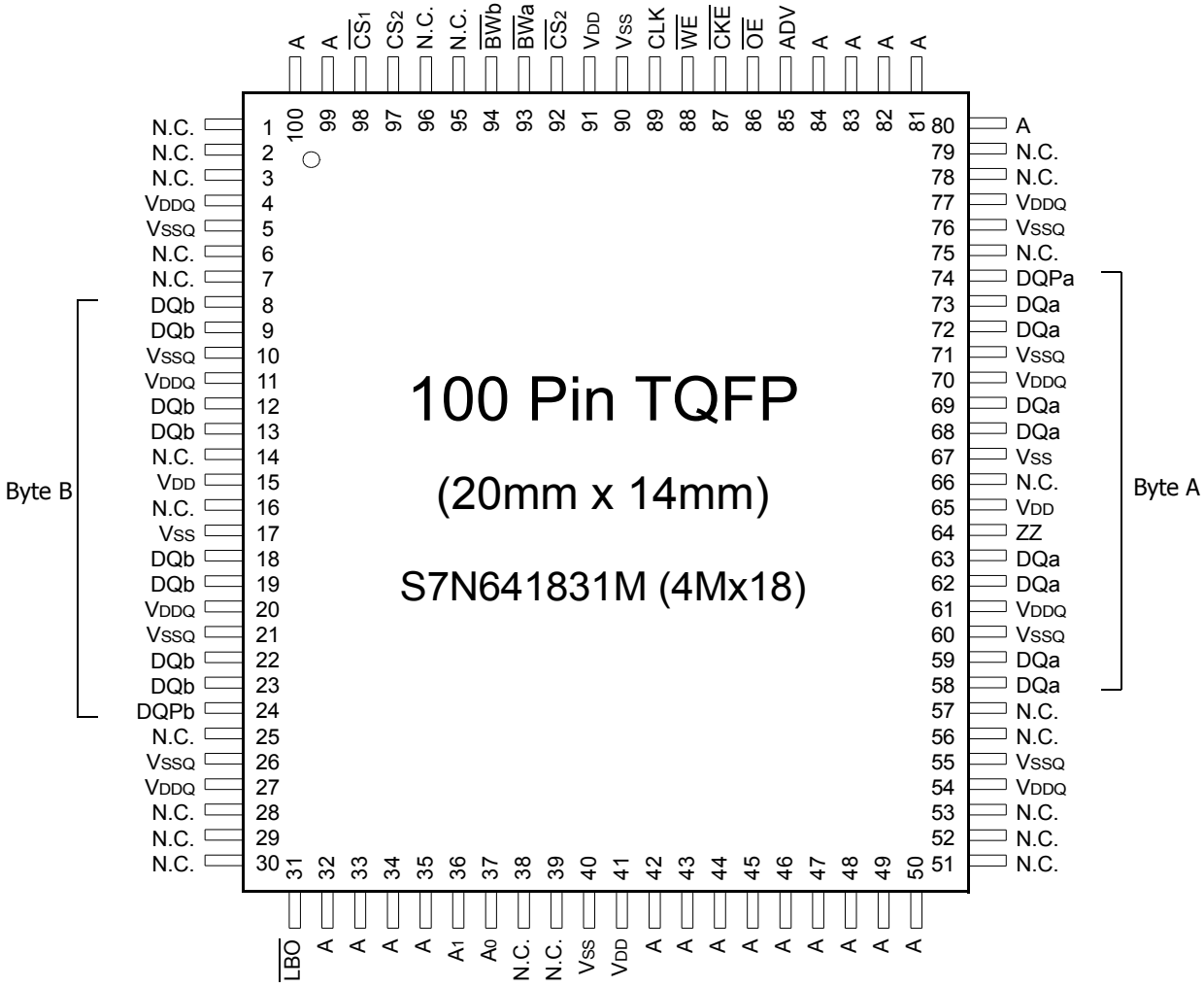


Pin Name

Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,42,43,44 ,45,46,47,48,49,50,81 ,82,83,84,99,100	VDD	Power Supply (2.5V~3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
A0,A1	Burst Address Inputs	37,36			
ADV	Address Advance/Load	85	N.C.	No Connect	14,16,38,39,66
WE	Read/Write Control Input	88			
CLK	Clock	89	DQa	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CKE	Clock Enable	87	DQb	Data Inputs/Outputs	68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc	Data Inputs/Outputs	2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd	Data Inputs/Outputs	18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd	Data Inputs/Outputs	51,80,1,30
BWx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86	VDDQ	Output Power Supply (2.5V~3.3V)	4,11,20,27,54,61,70,77
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31	VSSQ	Output Ground	5,10,21,26,55,60,71,76

Note : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

100 TQFP Package Pin Configurations(Top View)



Pin Name

Symbol	Pin Name	TQFP Pin NO.	Symbol	Pin Name	TQFP Pin NO.
A	Address Inputs	32,33,34,35,42,43,44, 45,46,47,48,49,50,80, 81,82,83,84,99,100	VDD	Power Supply (2.5V~3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
A0,A1	Burst Address Inputs	37,36			
ADV	Address Advance/Load	85	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29, 30,38,39,51,52,53, 56,57,66,75,78,79,95,96
WE	Read/Write Control Input	88			
CLK	Clock	89			
CKE	Clock Enable	87			
CS1	Chip Select	98	DQa	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS2	Chip Select	97	DQb	Data Inputs/Outputs	8,9,12,13,18,19,22,23
CS2	Chip Select	92	DQPa,DQPb	Data Inputs/Outputs	74,24
BWx(x=a,b)	Byte Write Inputs	93,94			
OE	Output Enable	86	VDDQ	Output Power Supply (2.5V~3.3V)	4,11,20,27,54,61,70,77
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31	VSSQ	Output Ground	5,10,21,26,55,60,71,76

NOTE : A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

165FBGA PKG Pin Configurations - S7N643631M (2Mx36) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC**	A	$\overline{CS1}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{CS2}$	$\overline{CKE}$	ADV	A	A	NC
B	NC	A	CS2	$\overline{BW_d}$	$\overline{BW_a}$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC**
C	DQP_c	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_b
D	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
E	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
F	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
G	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
K	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
L	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
M	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
N	DQP_d	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_a
P	NC	A	A	A	TDI	A1*	TDO	A	A	A	NC
R	$\overline{LBO}$	A	A	A	TMS	A0*	TCK	A	A	A	A

Notes: * A0 and A1 are two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
** Checked No Connect(NC) pins are reserved for higher density address, i.e. 11B for 144Mb and 1A for 256Mb.

Pin Name

Symbol	Pin Name	Symbol	Pin Name
A	Address Inputs	TCK	JTAG Test Clock
		TMS	JTAG Test Mode Select
		TDI	JTAG Test Data Input
A0,A1	Burst Address Inputs	TDO	JTAG Test Data Output
$\overline{ADV}$	Address Advance/Load		
$\overline{WE}$	Read/Write Control Input	VDD	Power Supply (2.5V~3.3V)
CLK	Clock	VSS	Ground
$\overline{CKE}$	Clock Enable		
$\overline{CS1}$	Chip Select	NC	No Connect
CS2	Chip Select		
$\overline{CS2}$	Chip Select		
$\overline{BW}$x(x=a,b,c,d)	Byte Write Inputs		
		DQa, DQb, DQc, DQd	Data Inputs/Outputs
$\overline{OE}$	Output Enable	DQPa, DQPb	Data Inputs/Outputs
ZZ	Power Sleep Mode	DQPc, DQPd	Data Inputs/Outputs
$\overline{LBO}$	Burst Mode Control		
		VDDQ	Output Power Supply

165FBGA PKG Pin Configurations - S7N641831M (4Mx18) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC**	A	$\overline{CS1}$	$\overline{BW_b}$	NC	$\overline{CS2}$	$\overline{CKE}$	ADV	A	A	A
B	NC	A	CS2	NC	$\overline{BW_a}$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC**
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_a
D	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
E	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
F	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
G	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
K	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
L	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
M	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
N	DQP_b	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	A	A	A	TDI	A1*	TDO	A	A	A	NC
R	$\overline{LBO}$	A	A	A	TMS	A0*	TCK	A	A	A	A

Notes: * A0 and A1 are two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
** Checked No Connect(NC) pins are reserved for higher density address, i.e. 11B for 144Mb and 1A for 256Mb.

Pin Name

Symbol	Pin Name	Symbol	Pin Name
A	Address Inputs	TCK	JTAG Test Clock
		TMS	JTAG Test Mode Select
		TDI	JTAG Test Data Input
A0,A1	Burst Address Inputs	TDO	JTAG Test Data Output
$\overline{ADV}$	Address Advance/Load		
$\overline{WE}$	Read/Write Control Input	VDD	Power Supply (2.5V~3.3V)
$\overline{CLK}$	Clock	VSS	Ground
$\overline{CKE}$	Clock Enable		
$\overline{CS1}$	Chip Select	NC	No Connect
CS2	Chip Select		
$\overline{CS2}$	Chip Select		
$\overline{BW}$x(x=a,b)	Byte Write Inputs		
		DQa, DQb	Data Inputs/Outputs
$\overline{OE}$	Output Enable	DQPa, DQPb	Data Inputs/Outputs
$\overline{ZZ}$	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control	VDDQ	Output Power Supply

Function Description

The S7N643631M and S7N641831M are NTSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.
All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

NTSRAM latches external address and initiates a cycle, when $\overline{CKE}$, ADV are driven to low and all three chip enables($\overline{CS_1}$, CS_2, $\overline{CS_2}$) are active . Output Enable($\overline{OE}$) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, all three chip enables($\overline{CS_1}$, CS_2, $\overline{CS_2}$) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low.The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. Also during read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$ [d:a] can be used for byte write operation. The pipelined NTSRAM uses a late-late write cycle to utilize 100% of the bandwidth.
At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion.
The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected.
And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

Burst Sequence Table

(Interleaved Burst, $\overline{LBO}$=High)

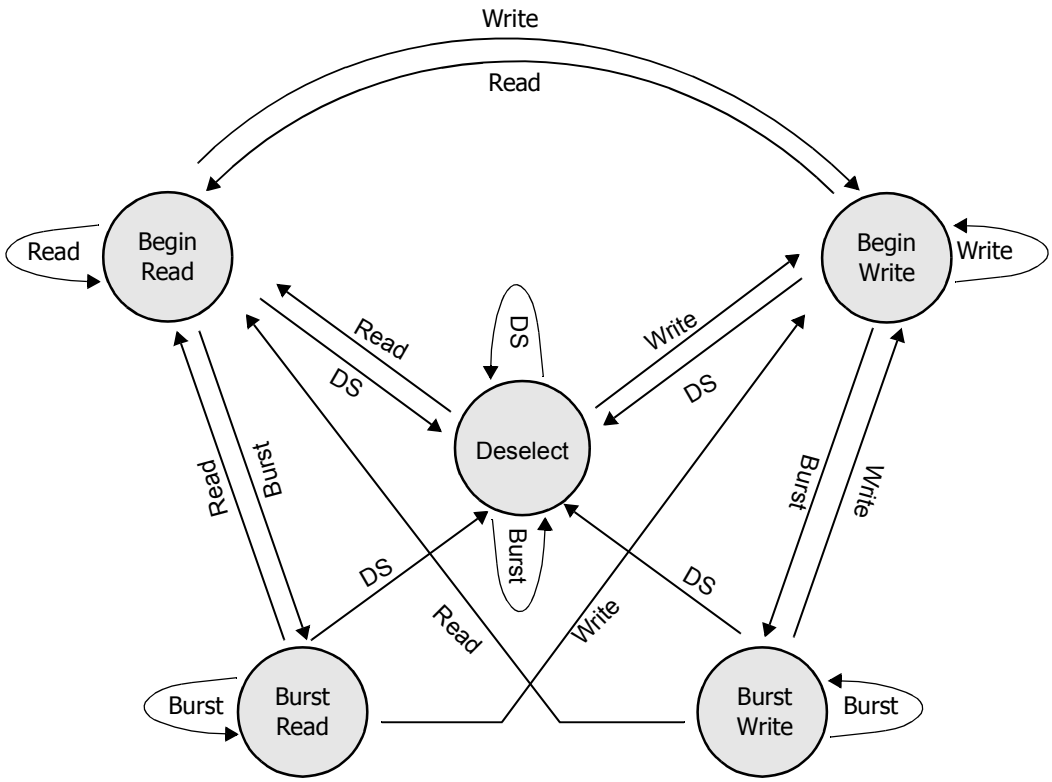
$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$=Low)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

State Diagram For NTSRAM



Command	Action
DS	Deselect
Read	Begin Read
Write	Begin Write
Burst	Begin Read Begin Write Continue Deselect

Notes : 1. An Ignore Clock Edge cycle is not shown is the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

Truth Tables

Synchronous Truth Table

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	ADV	$\overline{We}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CKE}$	CLK	Address Accessed	Operation
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

Notes : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by (↑).
3. A continue deselect cycle can only be enterd if a deselect cycle is executed first.
4. $\overline{We}$ = L means Write operation in Write Truth Table.
   $\overline{We}$ = H means Read operation in Write Truth Table.
5. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

Write Truth Table(x36)

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

Write Truth Table(x18)

$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	Operation
H	X	X	Read
L	L	H	Write Byte a
L	H	L	Write Byte b
L	L	L	Write All Bytes
L	H	H	Write Abort/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

Asynchronous Truth Table

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to V_{SS}		V_{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to V_{SS}		V_{IN}	-0.3 to V_{DD}+0.3	V
Power Dissipation		P_D	1.6	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_{OPR}	0 to 70	°C
	Industrial	T_{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias		T_{BIAS}	-10 to 85	°C

Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD1}	2.3	2.5	2.7	V
	V_{DDQ1}	2.3	2.5	2.7	V
	V_{DD2}	3.1	3.3	3.5	V
	V_{DDQ2}	2.3	3.3	3.5	V
Ground	V_{SS}	0	0	0	V

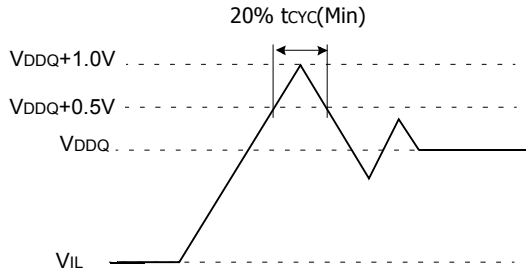
Notes: 1. The above parameters are also guaranteed at industrial temperature range.
2. It should be $V_{DDQ} \leq V_{DD}$

Capacitence(T_A=25°C, f=1MHz)

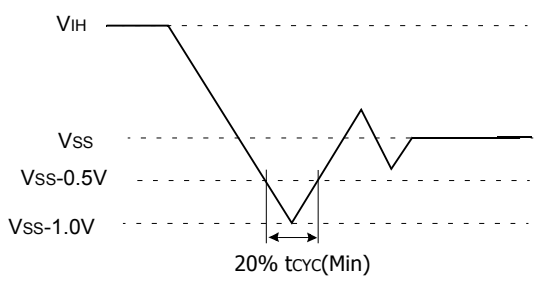
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

Note : Sampled not 100% tested.

Overshoot Timing



Undershoot Timing



DC Electrical Caracteristics

Parameter	Symbol	Test Conditions		Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	uA	
Output Leakage Current	I_{OL}	Output Disabled, V_{out}=V_{SS} to V_{DDQ}		-2	+2	uA	
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, ZZ ≤ V_{IL} , Cycle Time ≥ t_{CYC} Min	-25	-	370	mA	1,2
			-16	-	320		
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ≤V_{IL}, f=Max, All Inputs ≤ VIL or ≥ VIH	-25	-	225	mA	
			-16		220	mA	
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ ≤ 0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	200	mA	
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ ≥ V_{DD}-0.2V, f=Max, All Inputs ≤ V_{IL} or ≥ V_{IH}		-	200	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL}=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH}=-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.3**	V	3
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.3**	V	3

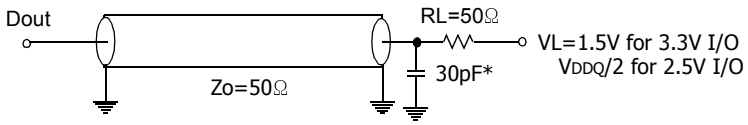
Notes : The above parameters are also guaranteed at industrial temperature range.
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

Test Conditions

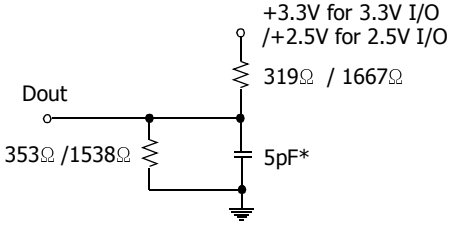
Parameter	Value
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1

The above parameters are also guaranteed at industrial temperature range.

Output Load(A)



Output Load(B)
(for t_{LZC}, t_{LZOE}, t_{HZOE} & t_{HZC})



* Including Scope and Jig Capacitance

Fig. 1

AC Timing Characteristics

Parameter	Symbol	-25		-16		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	4.0	-	6.0	-	ns
Clock Access Time	t_{CD}	-	2.6	-	3.5	ns
Output Enable to Data Valid	t_{OE}	-	2.6	-	3.5	ns
Clock High to Output Low-Z	t_{LZC}	1.5	-	1.5	-	ns
Output Hold from Clock High	t_{OH}	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	2.6	-	3.0	ns
Clock High to Output High-Z	t_{HZC}	-	2.6	-	3.0	ns
Clock High Pulse Width	t_{CH}	1.7	-	2.2	-	ns
Clock Low Pulse Width	t_{CL}	1.7	-	2.2	-	ns
Address Setup to Clock High	t_{AS}	1.2	-	1.5	-	ns
$\overline{CKE}$ Setup to Clock High	t_{CES}	1.2	-	1.5	-	ns
Data Setup to Clock High	t_{DS}	1.2	-	1.5	-	ns
Write Setup to Clock High ($\overline{WE}$, $\overline{BW}$x)	t_{WS}	1.2	-	1.5	-	ns
Address Advance Setup to Clock High	t_{ADVS}	1.2	-	1.5	-	ns
Chip Select Setup to Clock High	t_{CSS}	1.2	-	1.5	-	ns
Address Hold from Clock High	t_{AH}	0.3	-	0.5	-	ns
$\overline{CKE}$ Hold from Clock High	t_{CEH}	0.3	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.3	-	0.5	-	ns
Write Hold from Clock High ($\overline{WE}$, $\overline{BW}$x)	t_{WH}	0.3	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.3	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.3	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	cycle

Notes : 1. The above parameters are also guaranteed at industrial temperature range.

2. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
4. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low, Both cases must meet setup and hold times.
5. To avoid bus contention, At a given voltage and temperature t_{LZC} is more than t_{HZC}.
   The specs as shown do not imply bus contention because t_{LZC} is a Min. parameter that is worst case at totally different test conditions (0 ℃, 3.5V) than t_{HZC}, which is a Max. parameter(worst case at 70 ℃, 3.1V)
   It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

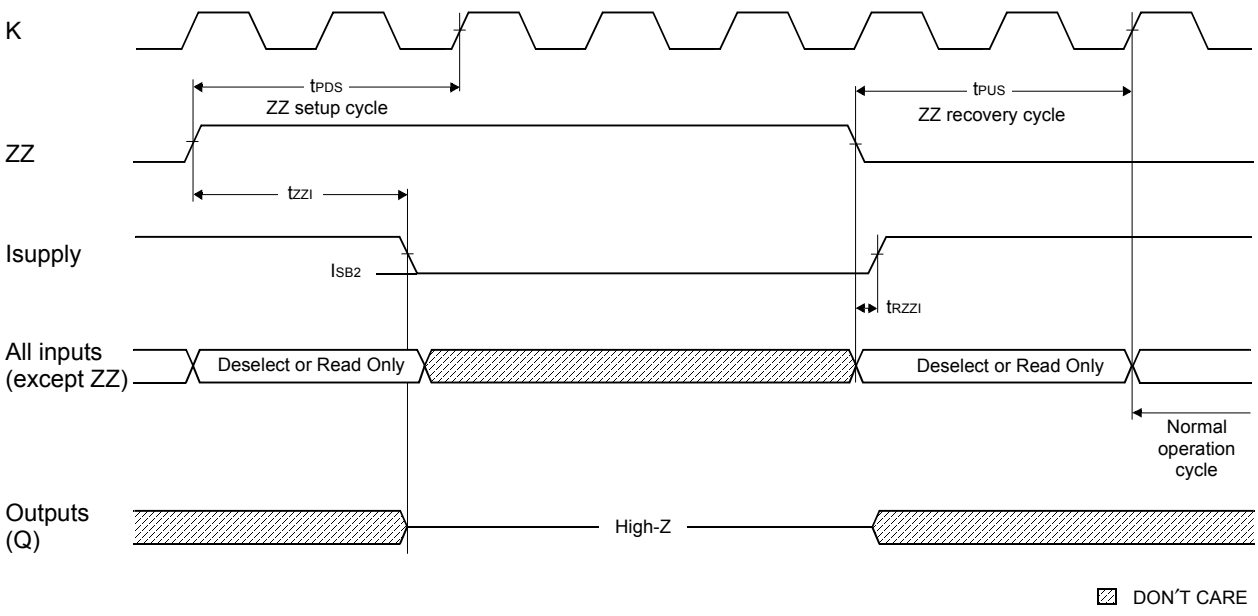
Sleep Mode

Sleep Mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2}. The duration of Sleep Mode is dictated by the length of time the ZZ is in a High state.
After entering Sleep Mode, all inputs except ZZ become disabled and all outputs go to High-Z.
The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep Mode.
When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering Sleep Mode is not guaranteed to successful complete. Therefore, Sleep Mode (Read or Write) must not be initiated until valid pending operations are completed. similarly, when exiting Sleep Mode during t_{PUS}, only a Deselect or Read cycle should be given while the SRAM is transitioning out of Sleep Mode.

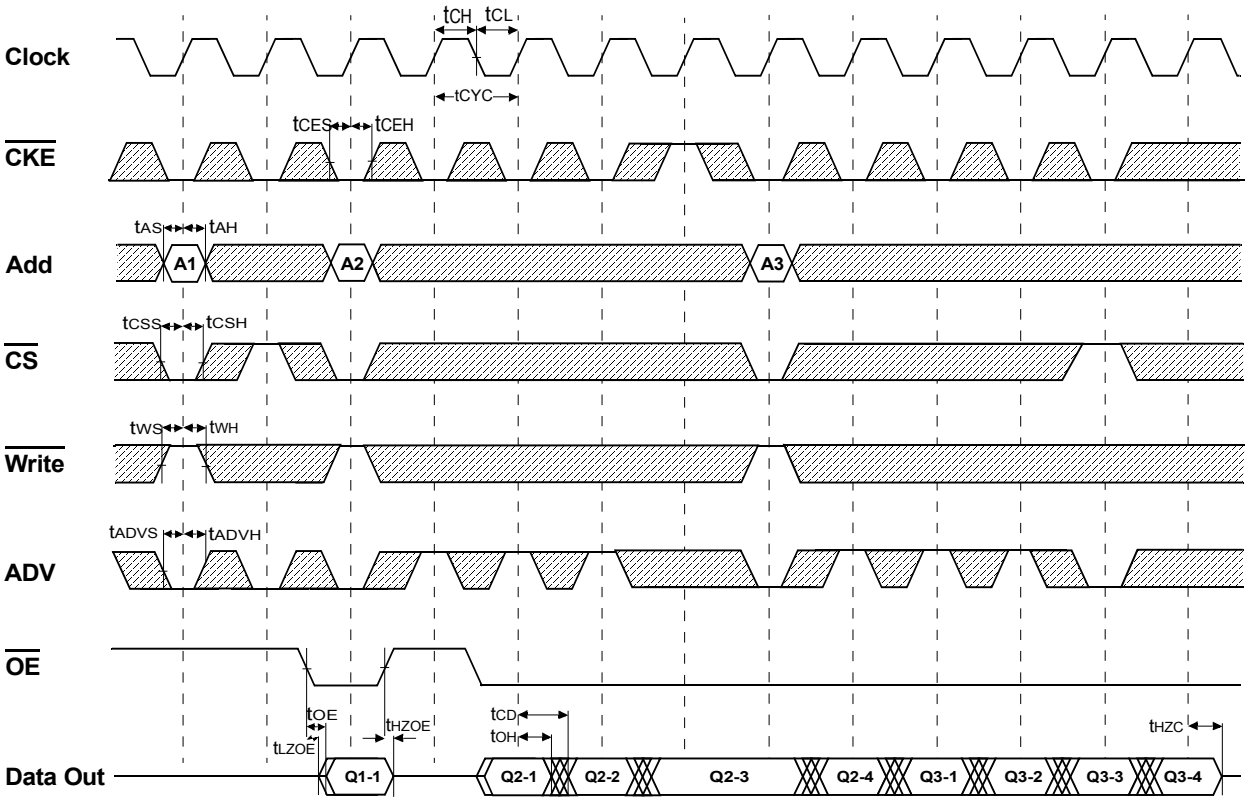
Sleep Mode Electrical Characteristics

Description	Condition	Symbol	Min	Max	Unit
Current during SLEEP MODE	ZZ ≥ V_{IH}	I_{SB2}		200	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

Sleep Mode Waveform

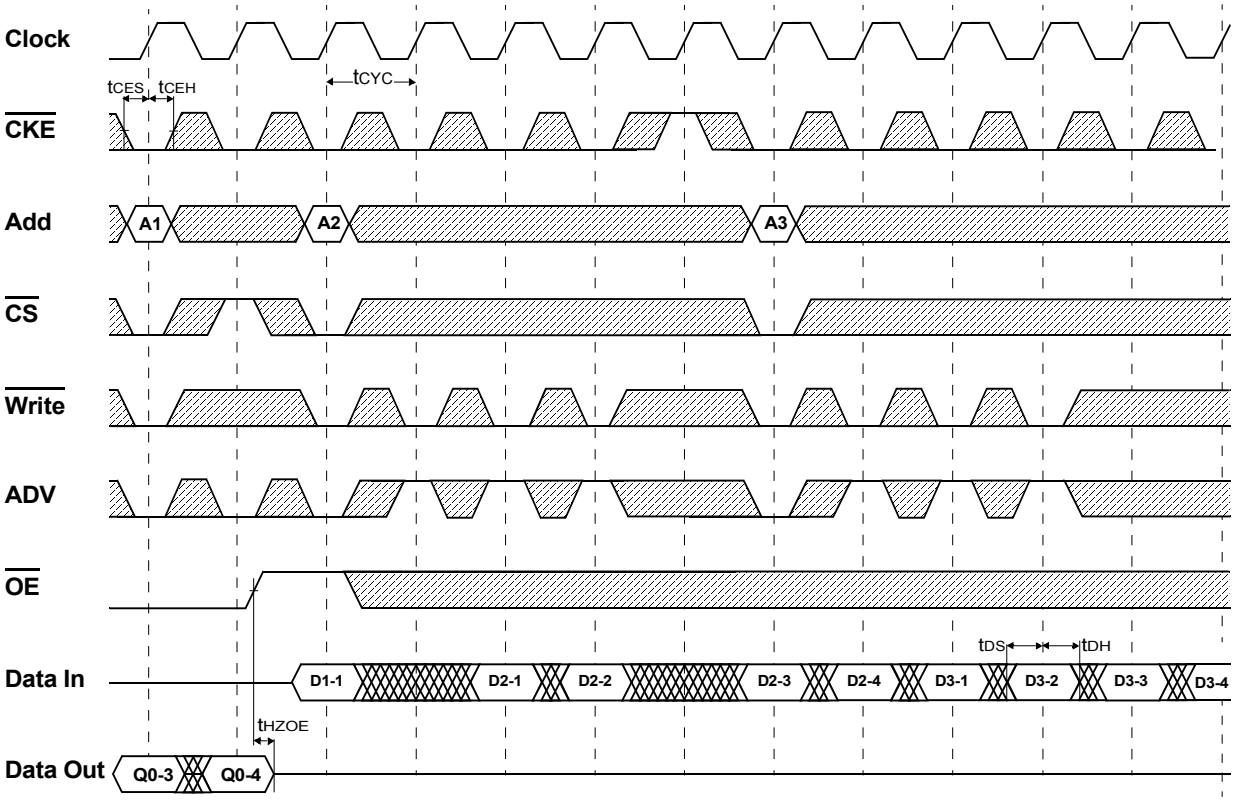


Timing Waveform Of Read Cycle



NOTES : $\overline{\text{Write}}$ = L means $\overline{\text{WE}}$ = L, and $\overline{\text{BW}}$x = L
$\overline{\text{CS}}$ = L means $\overline{\text{CS}}_1$ = L, CS_2 = H and $\overline{\text{CS}}_2$ = L
$\overline{\text{CS}}$ = H means $\overline{\text{CS}}_1$ = H, or $\overline{\text{CS}}_1$ = L and $\overline{\text{CS}}_2$ = H, or $\overline{\text{CS}}_1$ = L, and CS_2 = L

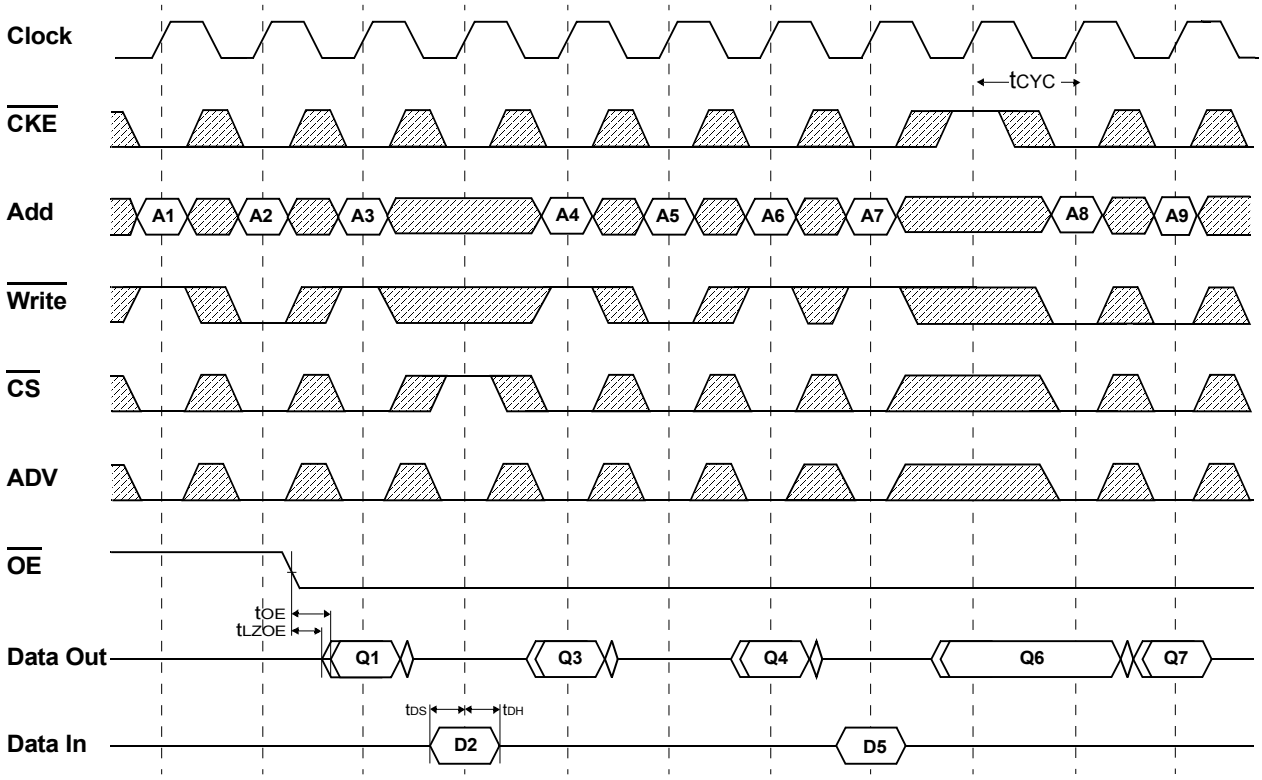
Timing Waveform Of Write Cycle



NOTES : $\overline{\text{Write}}$ = L means $\overline{\text{WE}}$ = L, and $\overline{\text{BW}}$x = L
$\overline{\text{CS}}$ = L means $\overline{\text{CS}}_1$ = L, CS_2 = H and $\overline{\text{CS}}_2$ = L
$\overline{\text{CS}}$ = H means $\overline{\text{CS}}_1$ = H, or $\overline{\text{CS}}_1$ = L and $\overline{\text{CS}}_2$ = H, or $\overline{\text{CS}}_1$ = L, and CS_2 = L

Don't Care
Undefined

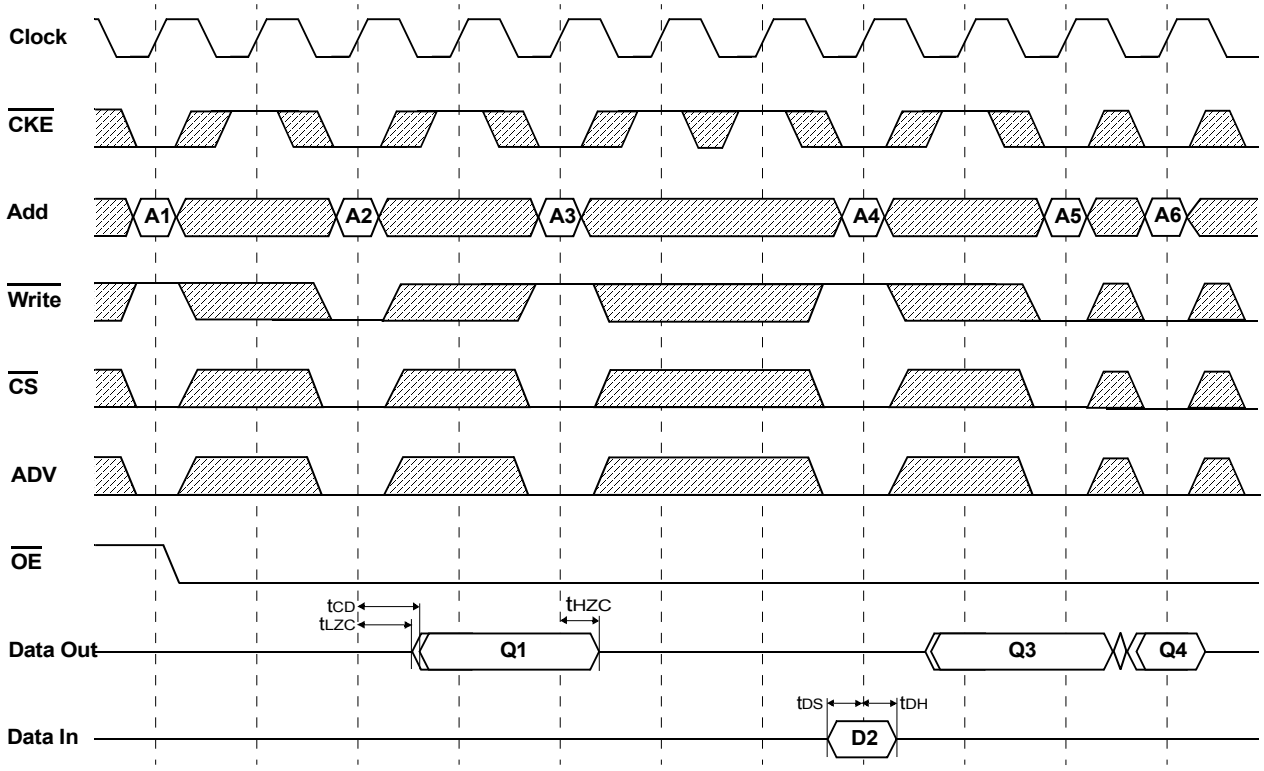
Timing Waveform Of Single Read/Write



NOTES : Write = L means WE = L, and BWx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L

Don't Care
Undefined

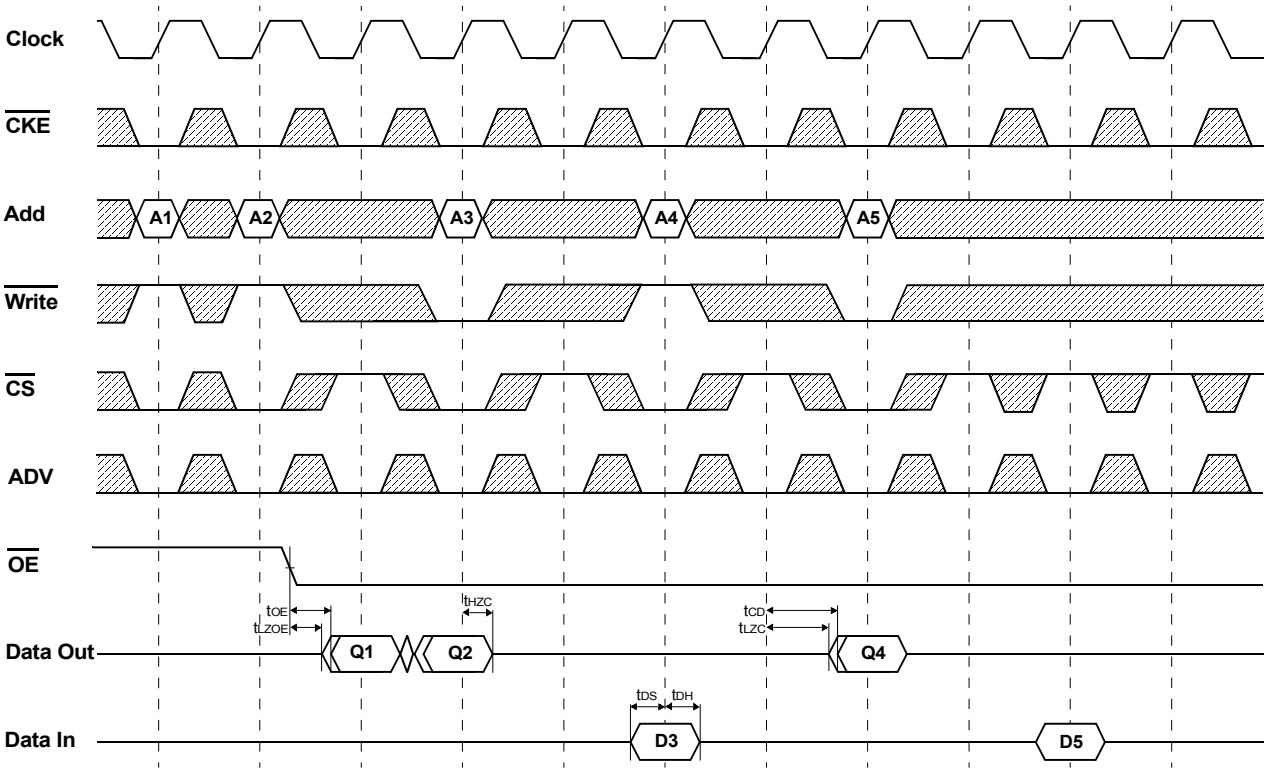
Timing Waveform Of $\overline{CKE}$ Operation



NOTES : $\overline{Write}$ = L means $\overline{WE}$ = L, and $\overline{BW}$x = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

Don't Care
Undefined

Timing Waveform Of $\overline{CS}$ Operation



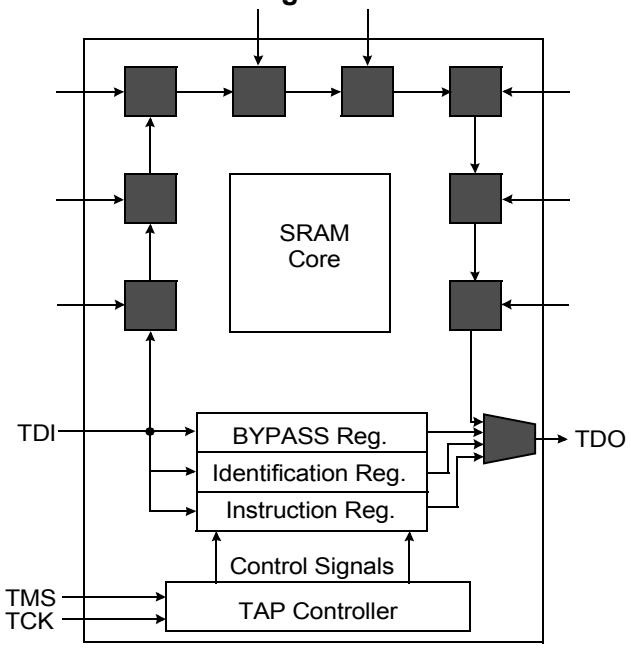
NOTES : $\overline{Write}$ = L means $\overline{WE}$ = L, and $\overline{BW}$x = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

Don't Care
Undefined

IEEE 1149.1 Test Access Port and Boundary Scan-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP).The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



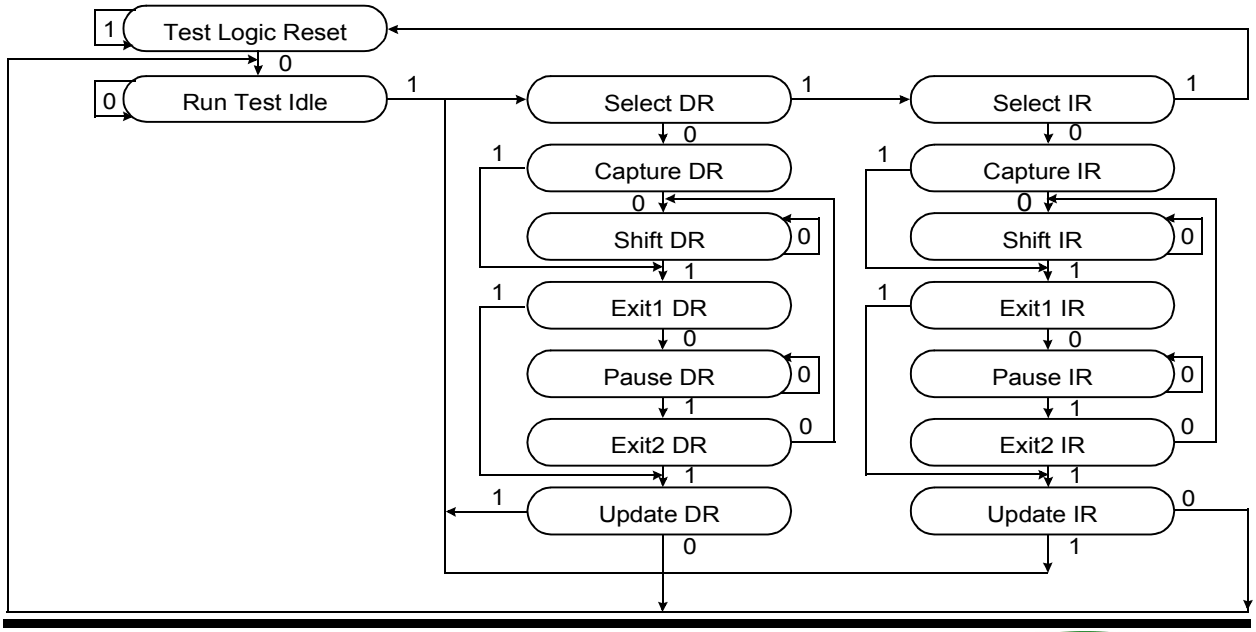
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	BYPASS	Bypass Register	4
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	BYPASS	Bypass Register	4
1	1	1	BYPASS	Bypass Register	4

NOTE:

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram



Scan Register Definition

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
2M x 36 4M x 18	3 bits	1 bit	32 bits	89 bits

ID Registration Definition

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Netsol JEDEC Code (11: 1)	Start Bit(0)
2M x 36	0000	01001 00100	000000	01111011001	1
4M x 18	0000	01010 00011	000000	01111011001	1

Boundary Scan Exit Order

Order	Pin ID
1	6N
2	7N
3	10N
4	11P
5	8P
6	8R
7	9R
8	9P
9	10P
10	10R
11	11R
12	11H
13	11N
14	11M
15	11L
16	11K
17	11J
18	10M
19	10L
20	10K
21	10J
22	9H
23	10H
24	11G
25	11F
26	11E
27	11D
28	10G
29	10F
30	10E
31	10D
32	11C
33	11A
34	11B
35	10A
36	10B

Order	Pin ID
37	9A
38	9B
39	10C
40	8A
41	8B
42	7A
43	7B
44	6B
45	6A
46	5B
47	5A
48	4A
49	4B
50	3B
51	3A
52	2A
53	2B
54	2C
55	1B
56	1A
57	1C
58	1D
59	1E
60	1F
61	1G
62	2D
63	2E
64	2F
65	2G
66	1H
67	3H
68	1J
69	1K
70	1L
71	1M
72	2J

Order	Pin ID
73	2K
74	2L
75	2M
76	1N
77	2N
78	1P
79	1R
80	2R
81	3P
82	3R
83	2P
84	4R
85	4P
86	5N
87	6P
88	6R
89	Internal

JTAG DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage (3.3V / 2.5V)	V_{DD}	3.135/2.375	3.3/2.5	3.465/2.625	V	
Input High Level (3.3V I/O / 2.5V I/O)	V_{IH}	2.0/1.7	-	V_{DD}+0.3	V	
Input Low Level (3.3V I/O / 2.5V I/O)	V_{IL}	-0.3	-	0.8/0.7	V	
Output High Voltage (3.3V I/O / 2.5V I/O)	V_{OH}	2.4/2.0	-	-	V	
Output Low Voltage (3.3V I/O / 2.5V I/O)	V_{OL}	-	-	0.4/0.4	V	

Note: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC Test Conditions

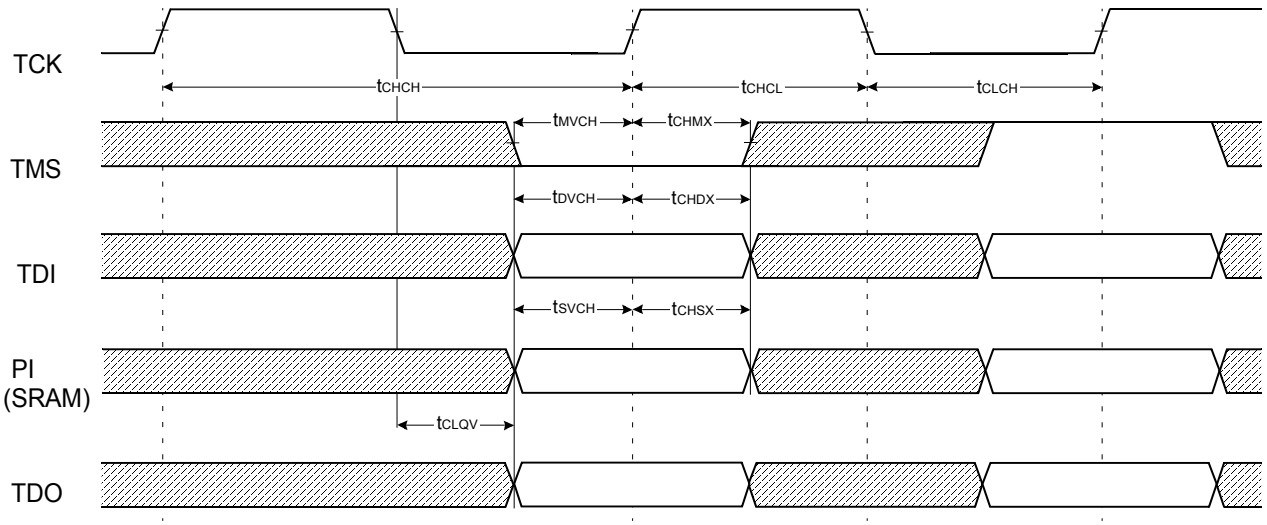
Parameter	Symbol	Min	Unit	Note
Input High/Low Level (3.3V I/O , 2.5V I/O)	V_{IH}/V_{IL}	3.0/0 , 2.5/0	V	
Input Rise/Fall Time (3.3V I/O , 2.5V I/O)	TR/TF	1.0/1.0 , 1.0/1.0	ns	
Input and Output Timing Reference Level		$V_{DDQ}/2$	V	

Note: 1. See SRAM AC test output load on page 11.

JTAG AC Characteristics

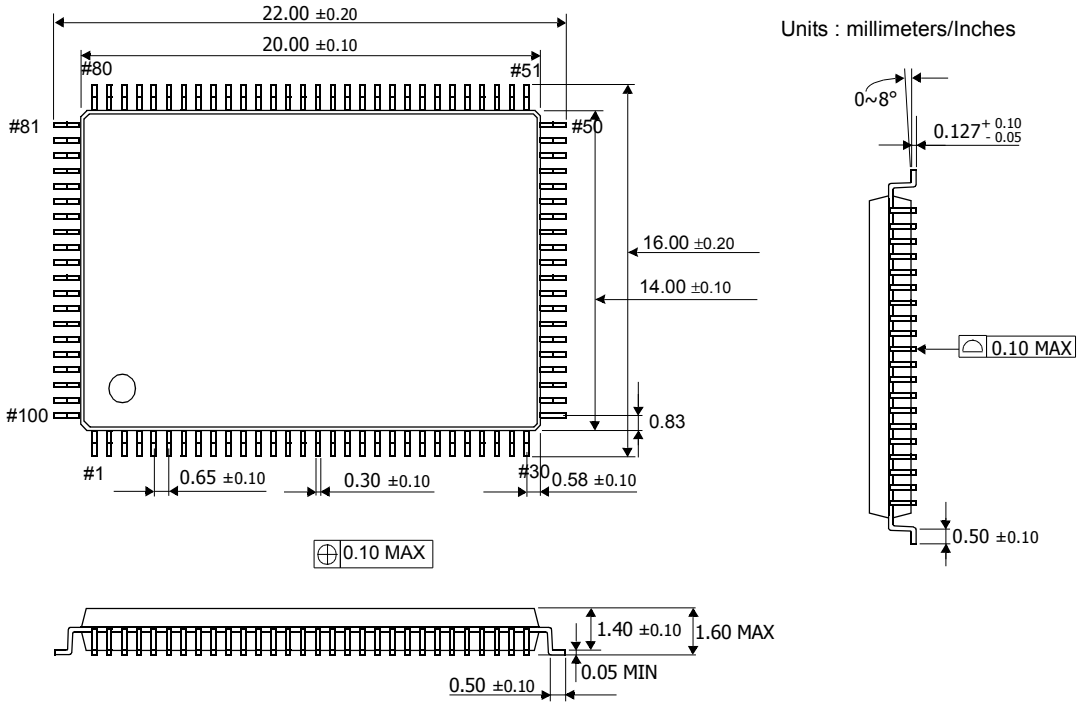
Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG Timing Diagram



Package Dimensions

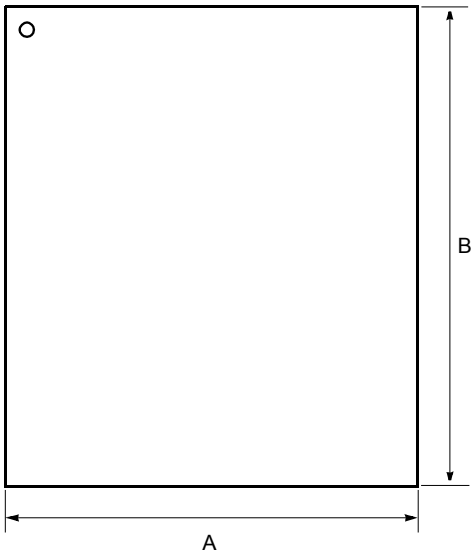
100-TQFP-1420A (Lead Free)



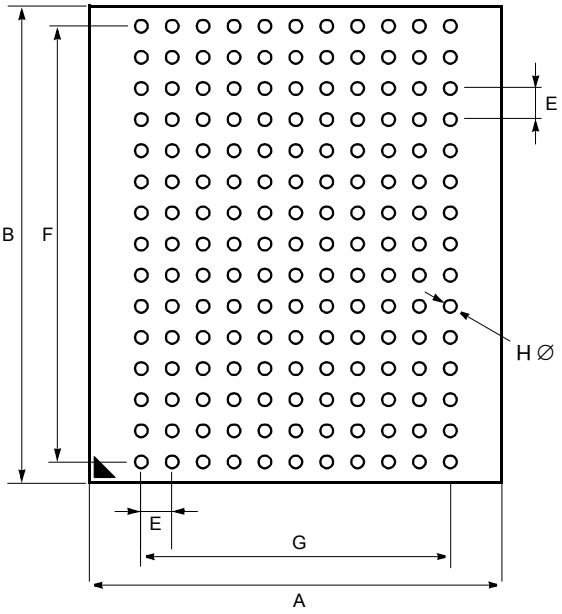
165 FBGA Package Dimensions (Lead Free)

13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Grid Array

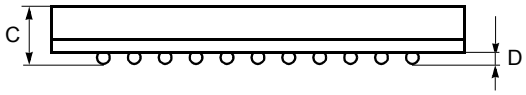
Top View



Bottom View



Side View



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	13 ± 0.1	mm		**E**	1.0	mm	
B	15 ± 0.1	mm		**F**	14.0	mm	
C	1.3 ± 0.1	mm		**G**	10.0	mm	
D	0.35 ± 0.05	mm		**H**	0.5 ± 0.05	mm	