72Mb Quadruple-II BL2 SRAM Specification

165FBGA with Pb & Pb Free

(ROHS Compliant)

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Document Title

2Mx36 & 4Mx18 & 8Mx9 - Bit Quadruple-II Burst Length of 2 SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	May 2012	Preliminary
1.0	Final spec release Remove θ_{JB} parameter in thermal resistance	Feb. 2013	Final
1.1	Correct errata on Setup and Hold Time	Jul. 2014	Final

2Mx36 & 4Mx18 & 8Mx9 - Bit Quadruple-II Burst Length of 2 SRAM

Features

- 1.8V+0.1V/-0.1V Power Supply.
- DLL circuitry for wide output data valid window and future frequency scaling.
- I/O Supply Voltage 1.5V+0.1V/-0.1V for 1.5V I/O, 1.8V+0.1V/ -0.1V for 1.8V I/O.
- Separate independent read and write data ports with concurrent read and write operation
- HSTL I/O
- Full data coherency, providing most current data.
- Synchronous pipeline read with self timed early write.
- Registered address, control and data input/output.
- DDR (Double Data Rate) Interface on read and write ports.
- Fixed 2-bit burst for both read and write operation.
- Clock-stop supports to reduce current.
- Two input clocks (K and $\overline{K}$) for accurate DDR timing at clock rising edges only.
- Two input clocks for output data (C and $\overline{C}$) to minimize clock-skew and flight-time mismatches.
- Two echo clocks (CQ and $\overline{CQ}$) to enhance output data traceability.
- Single address bus.
- Byte write (x9, x18, x36) function.
- Separate read/write control pin ($\overline{R}$ and $\overline{W}$)
- Simple depth expansion with no data contention.
- Programmable output impedance.
- JTAG 1149.1 compatible test access port.
- 165FBGA(11x15 ball array FBGA) with body size of 13x15mm & Lead Free

Key Parameters

Part Number	Org.	Cycle Time	Access Time	Unit	RoHS
S7R643682M-E(F)C(I)33	X36	3.0	0.45	ns	O
S7R643682M-E(F)C(I)30		3.3	0.45	ns	O
S7R643682M-E(F)C(I)25		4.0	0.45	ns	O
S7R641882M-E(F)C(I)33	X18	3.0	0.45	ns	O
S7R641882M-E(F)C(I)30		3.3	0.45	ns	O
S7R641882M-E(F)C(I)25		4.0	0.45	ns	O
S7R640982M-E(F)C(I)33	X9	3.0	0.45	ns	O
S7R640982M-E(F)C(I)30		3.3	0.45	ns	O
S7R640982M-E(F)C(I)25		4.0	0.45	ns	O

* -E(F)C(I)
E(F) [Package type]: E-Pb Free, F-Pb
C(I) [Operating Temperature]: C-Commercial, I-Industrial

GENERAL DESCRIPTION

The S7R643682M, S7R641882M and S7R640982M are 75,497,472-bits Quadruple Synchronous Pipelined Burst SRAMs. They are organized as 2,097,152 words by 36bits for S7R643682M, 4,194,304 words by 18bits for S7R641882M and 8,388,608 words by 9bits for S7R640982M.

The Quadruple operation is possible by supporting DDR read and write operations through separate data output and input ports with the same cycle. Memory bandwidth is maximized as data can be transferred into SRAM on every rising edge of K and $\overline{K}$, and transferred out of SRAM on every rising edge of C and $\overline{C}$. And totally independent read and write ports eliminate the need for high speed bus turn around.

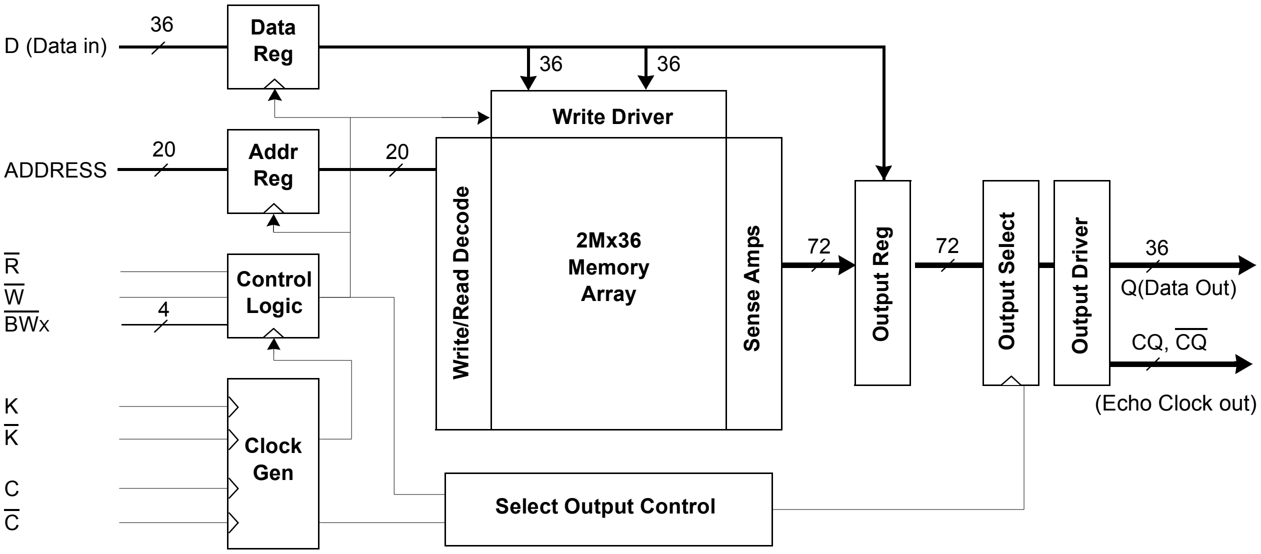
Address, data inputs, and all control signals are synchronized to the input clock (K or $\overline{K}$). Normally data outputs are synchronized to output clocks (C and $\overline{C}$), but when C and $\overline{C}$ are tied high, the data outputs are synchronized to the input clocks (K and $\overline{K}$). Read data are referenced to echo clock (CQ or $\overline{CQ}$) outputs. Read address is registered on rising edges of the input K clocks, and write address is registered on rising edges of the input $\overline{K}$ clocks.

Common address bus is used to access address both for read and write operations. The internal burst counter is fixed to 2-bit sequential for both read and write operations. Synchronous pipeline read and early write enable high speed operations. Simple depth expansion is accomplished by using $\overline{R}$ and $\overline{W}$ for port selection. Byte write operation is supported with $\overline{BW_0}$ and $\overline{BW_1}$ ($\overline{BW_2}$ and $\overline{BW_3}$) pins for x18 (x36) device and only $\overline{BW}$ pin for x9 device.

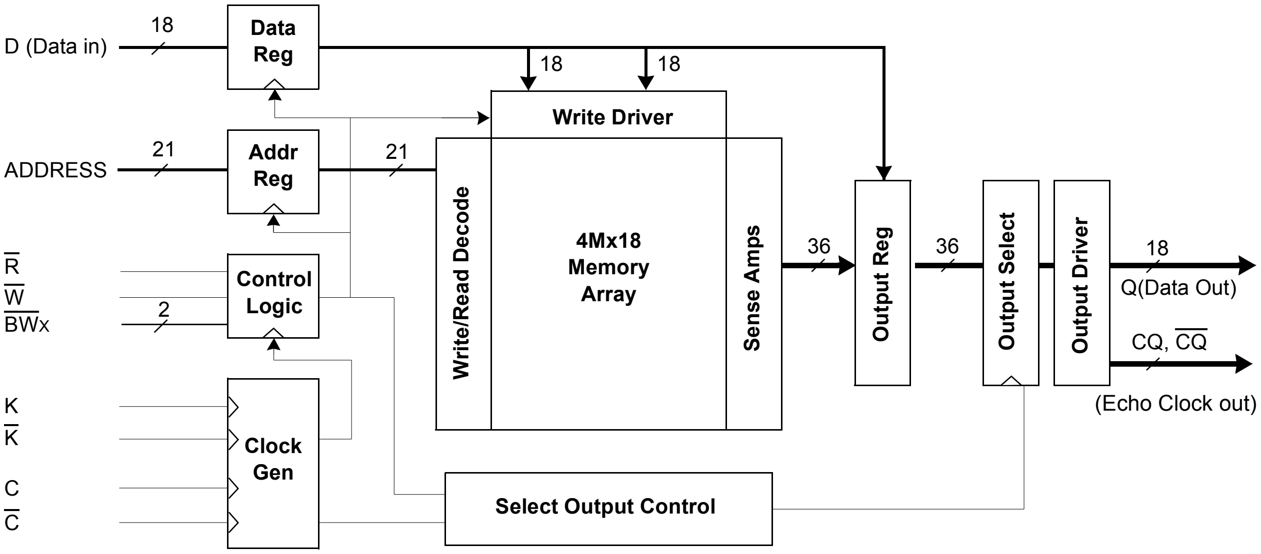
IEEE 1149.1 serial boundary scan (JTAG) simplifies monitoring package pads attachment status with system.

The S7R643682M, S7R641882M and S7R640982M are implemented with Netsol's high performance 6T CMOS technology and is available in 165pin FBGA packages. Multiple power and ground pins minimize ground bounce.

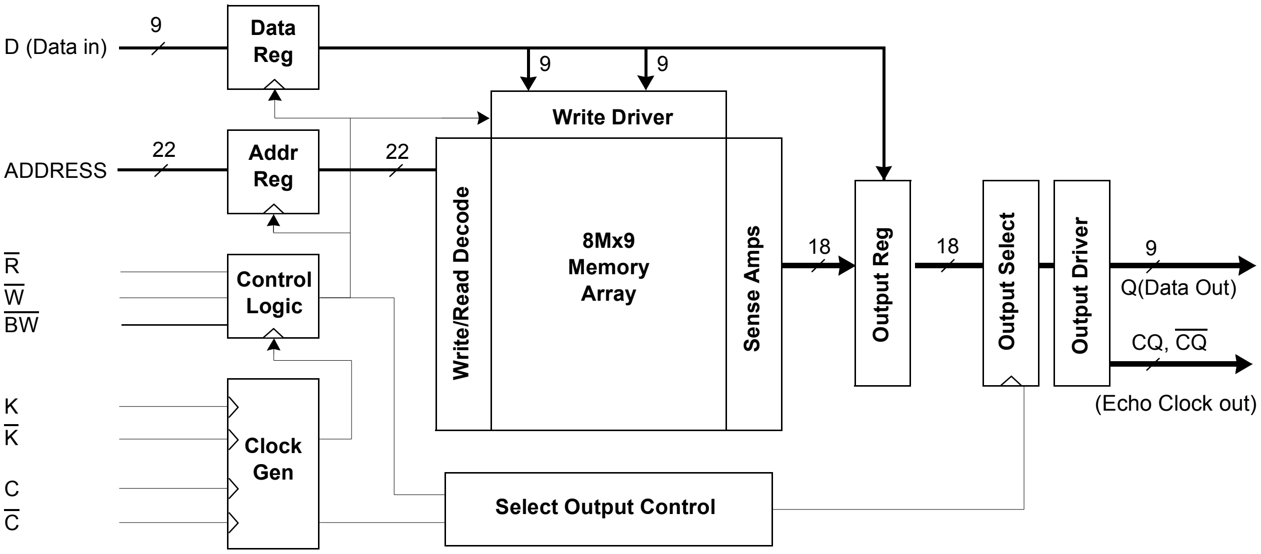
Logic Block Diagram - S7R643682M (2M x 36)



Logic Block Diagram - S7R641882M (4M x 18)



Logic Block Diagram - S7R640982M (8M x 9)



165FBGA PKG Pin Configurations - S7R643682M (2Mx36) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/SA*	SA	$\overline{W}$	$\overline{BW_2}$	$\overline{K}$	$\overline{BW_1}$	$\overline{R}$	SA	NC/SA*	CQ
B	Q27	Q18	D18	SA	$\overline{BW_3}$	K	$\overline{BW_0}$	SA	D17	Q17	Q8
C	D27	Q28	D19	VSS	SA	SA	SA	VSS	D16	Q7	D8
D	D28	D20	Q19	VSS	VSS	VSS	VSS	VSS	Q16	D15	D7
E	Q29	D29	Q20	VDDQ	VSS	VSS	VSS	VDDQ	Q15	D6	Q6
F	Q30	Q21	D21	VDDQ	VDD	VSS	VDD	VDDQ	D14	Q14	Q5
G	D30	D22	Q22	VDDQ	VDD	VSS	VDD	VDDQ	Q13	D13	D5
H	$\overline{Doff}$	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	D31	Q31	D23	VDDQ	VDD	VSS	VDD	VDDQ	D12	Q4	D4
K	Q32	D32	Q23	VDDQ	VDD	VSS	VDD	VDDQ	Q12	D3	Q3
L	Q33	Q24	D24	VDDQ	VSS	VSS	VSS	VDDQ	D11	Q11	Q2
M	D33	Q34	D25	VSS	VSS	VSS	VSS	VSS	D10	Q1	D2
N	D34	D26	Q25	VSS	SA	SA	SA	VSS	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

Notes: 1. * Checked No Connect (NC) or Vss pins are reserved for higher density address, i.e. 10A for 144Mb and 2A for 288Mb.
2. $\overline{BW_0}$ controls write to D0:D8, $\overline{BW_1}$ controls write to D9:D17, $\overline{BW_2}$ controls write to D18:D26 and $\overline{BW_3}$ controls write to D27:D35.

Pin Name

Symbol	Pin Numbers	Description	Note
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA	3A,9A,4B,8B,5C-7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-35	10P,11N,11M,10K,11J,11G,10E,11D,11C,10N,9M,9L 9J,10G,9F,10D,9C,9B,3B,3C,2D,3F,2G,3J,3L,3M,2N 1C,1D,2E,1G,1J,2K,1M,1N,2P	Data Inputs	
Q0-35	11P,10M,11L,11K,10J,11F,11E,10C,11B,9P,9N,10L 9K,9G,10F,9E,9D,10B,2B,3D,3E,2F,3G,3K,2L,3N 3P,1B,2C,1E,1F,2J,1K,1L,2M,1P	Data Outputs	
$\overline{W}$	4A	Write Control Pin, active when low	
$\overline{R}$	8A	Read Control Pin, active when low	
$\overline{BW_0}$, $\overline{BW_1}$,$\overline{BW_2}$, $\overline{BW_3}$	7B,7A,5A,5B	Block Write Control Pin, active when low	
VREF	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
VDD	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (1.8 V)	
VDDQ	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
VSS	4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M, 8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	2A,10A,	No Connect	3

Notes:1. C, $\overline{C}$, K or $\overline{K}$ cannot be set to VREF voltage.
2. When ZQ pin is directly connected to VDD output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

165FBGA PKG Pin Configurations - S7R641882M (4Mx18) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/SA*	SA	$\overline{W}$	$\overline{BW_1}$	$\overline{K}$	NC/SA*	$\overline{R}$	SA	SA	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW_0}$	SA	NC	NC	Q8
C	NC	NC	D10	VSS	SA	SA	SA	VSS	NC	Q7	D8
D	NC	D11	Q10	VSS	VSS	VSS	VSS	VSS	NC	NC	D7
E	NC	NC	Q11	VDDQ	VSS	VSS	VSS	VDDQ	NC	D6	Q6
F	NC	Q12	D12	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	Q5
G	NC	D13	Q13	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	D5
H	$\overline{Doff}$	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	D14	VDDQ	VDD	VSS	VDD	VDDQ	NC	Q4	D4
K	NC	NC	Q14	VDDQ	VDD	VSS	VDD	VDDQ	NC	D3	Q3
L	NC	Q15	D15	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	Q2
M	NC	NC	D16	VSS	VSS	VSS	VSS	VSS	NC	Q1	D2
N	NC	D17	Q16	VSS	SA	SA	SA	VSS	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

Notes: 1. * Checked No Connect(NC) pins are reserved for higher density address, i.e. 2A for 144Mb and 7A for 288Mb.
2. $\overline{BW_0}$ controls write to D0:D8 and $\overline{BW_1}$ controls write to D9:D17.

Pin Name

Symbol	Pin Numbers	Description	Note
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA	3A,9A,10A,4B,8B,5C-7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-17	10P,11N,11M,10K,11J,11G,10E,11D,11C,3B,3C,2D, 3F,2G,3J,3L,3M,2N	Data Inputs	
Q0-17	11P,10M,11L,11K,10J,11F,11E,10C,11B,2B,3D,3E, 2F,3G,3K,2L,3N,3P	Data Outputs	
$\overline{W}$	4A	Write Control Pin, active when low	
$\overline{R}$	8A	Read Control Pin, active when low	
$\overline{BW_0}$, $\overline{BW_1}$	7B, 5A	Block Write Control Pin, active when low	
VREF	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
VDD	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (1.8 V)	
VDDQ	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
VSS	4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	2A,7A,1B,5B,9B,10B,1C,2C,9C,1D,9D,10D,1E,2E,9E, 1F,9F,10F,1G,9G,10G,1J,2J,9J,1K,2K,9J,1L,9L,10L,1M,2M, 9M,1N,9N,10N,1P,2P,9P	No Connect	3

Notes: 1. C, $\overline{C}$, K or $\overline{K}$ cannot be set to VREF voltage.
2. When ZQ pin is directly connected to VDD output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

165FBGA PKG Pin Configurations - S7R640982M (8Mx9) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	$\overline{W}$	NC	$\overline{K}$	NC/SA*	$\overline{R}$	SA	SA	CQ
B	NC	NC	NC	SA	NC/SA*	K	$\overline{BW}$	SA	NC	NC	Q4
C	NC	NC	NC	VSS	SA	SA	SA	VSS	NC	NC	D4
D	NC	D5	NC	VSS	VSS	VSS	VSS	VSS	NC	NC	NC
E	NC	NC	Q5	VDDQ	VSS	VSS	VSS	VDDQ	NC	D3	Q3
F	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
G	NC	D6	Q6	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
H	$\overline{Doff}$	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	Q2	D2
K	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
L	NC	Q7	D7	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	Q1
M	NC	NC	NC	VSS	VSS	VSS	VSS	VSS	NC	NC	D1
N	NC	D8	NC	VSS	SA	SA	SA	VSS	NC	NC	NC
P	NC	NC	Q8	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

Notes: 1. * Checked No Connect(NC) pins are reserved for higher density address, i.e. 7A for 144Mb, 5B for 288Mb.
2. $\overline{BW}$ controls write to D0:D8.

Pin Name

Symbol	Pin Numbers	Description	Note
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA	2A,3A,9A,10A,4B,8B,5C-7C,5N-7N,4P,5P,7P,8P,3R-5R, 7R-9R	Address Inputs	
D0-8	11M,11J,10E,11C,2D,2G,3L,2N,10P	Data Inputs	
Q0-8	11L,10J,11E,11B,3E,3G,2L,3P,11P	Data Outputs	
$\overline{W}$	4A	Write Control Pin, active when low	
$\overline{R}$	8A	Read Control Pin, active when low	
$\overline{BW}$	7B	Block Write Control Pin, active when low	
VREF	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
VDD	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (1.8 V)	
VDDQ	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
VSS	4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	5A,7A,1B,2B,3B,5B,9B,10B,1C,2C,3C,9C,10,1D,3D, 9D,10D,11D,1E,2E,9E,1F,2F,3F,9F,10F,11F,1G,9G,10G,11G, 1J,2J,3J,9J,1K,2K,3K,9K,10K,11K,1L,9L,10L,1M,2M,3M,9M 10M,1N,3N,9N,10N,11N,1P,2P,9P	No Connect	3

Notes: 1. C, $\overline{C}$, K or $\overline{K}$ cannot be set to VREF voltage.
2. When ZQ pin is directly connected to VDD output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

Read Operations

Read cycles are initiated by activating $\overline{R}$ at the rising edge of the positive input clock K. Address is presented and stored in the read address register synchronized with K clock. For 2-bit burst DDR operation, it will access two 36-bit or 18-bit or 9-bit data words with each read command.
The first pipelined data is transferred out of the device triggered by $\overline{C}$ clock following next $\overline{K}$ clock rising edge. Next burst data is triggered by the rising edge of following C clock rising edge. Continuous read operations are initiated with K clock rising edge. And pipelined data are transferred out of device on every rising edge of both C and $\overline{C}$ clocks. In case C and $\overline{C}$ tied to high, output data are triggered by K and $\overline{K}$ instead of C and $\overline{C}$.
When the $\overline{R}$ is disabled after a read operation, the S7R643682M, S7R641882M and S7R640982M will first complete burst read operation before entering into deselect mode at the next K clock rising edge. Then output drivers disabled automatically to high impedance state.

Write Operations

Write cycles are initiated by activating $\overline{W}$ at the rising edge of the positive input clock K. Address is presented and stored in the write address register synchronized with following $\overline{K}$ clock. For 2-bit burst DDR operation, it will write two 36-bit or 18-bit or 9-bit data words with each write command.
The first “early” data is transferred and registered in to the device synchronous with same K clock rising edge with $\overline{W}$ presented. Next burst data is transferred and registered synchronous with following $\overline{K}$ clock rising edge. Continuous write operations are initiated with K rising edge. And “early write” data is presented to the device on every rising edge of both K and $\overline{K}$ clocks.
When the $\overline{W}$ is disabled, the S7R643682M, S7R641882M and S7R640982M will enter into deselect mode. The device disregards input data presented on the same cycle $\overline{W}$ disabled.
The S7R643682M, S7R641882M and S7R640982M support byte write operations. With activating $\overline{BW_0}$ or $\overline{BW_1}$ ($\overline{BW_2}$ or $\overline{BW_3}$) in write cycle, only one byte of input data is presented. In S7R641882M, $\overline{BW_0}$ controls write operation to D0:D8, $\overline{BW_1}$ controls write operation to D9:D17. And in S7R643682M, $\overline{BW_2}$ controls write operation to D18:D26, $\overline{BW_3}$ controls write operation to D27:D35. And in S7R640982M, $\overline{BW}$ controls write operation to D0:D8.

Single Clock Mode

S7R643682M, S7R641882M and S7R640982M can be operated with the single clock pair K and $\overline{K}$, instead of C or $\overline{C}$ for output clocks.
To operate these devices in single clock mode, C and $\overline{C}$ must be tied high during power up and must be maintained high during operation. After power up, this device can’t change to or from single clock mode. System flight time and clock skew could not be compensated in this mode.

Depth Expansion

Separate input and output ports enables easy depth expansion. Each port can be selected and deselected independently and read and write operation do not affect each other. Before chip deselected, all read and write pending operations are completed.

Programmable Impedance Output Buffer Operation

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to V_{SS} through a precision resistor (RQ). The value of RQ (within 15%) is five times the output impedance desired. For example, 250Ω resistor will give an output impedance of 50Ω. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM.
To guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

Echo clock operation

To assure the output traceability, the SRAM provides the output Echo clock, pair of compliment clock CQ and $\overline{CQ}$, which are synchronized with internal data output. Echo clocks run free during normal operation.
The Echo clock is triggered by internal output clock signal, and transferred to external through same structures as output driver.

Clock Consideration

S7R643682M,S7R641882M and S7R640982M utilizes internal DLL (Delay-Locked Loops) for maximum output data valid window. It can be placed into a stopped-clock state to minimize power with a modest restart time of 1024 clock cycles.
Circuitry automatically resets the DLL when absence of input clock is detected.

Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, then V_{IN}. V_{DD} and V_{DDQ} can be applied simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN}, V_{REF}, V_{DDQ}, V_{DD}, V_{SS}. V_{DD} and V_{DDQ} can be removed simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-down.

Detail Specification of Power-Up Sequence in Quadruple-II SRAM

Quadruple-II SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

• Power-Up Sequence

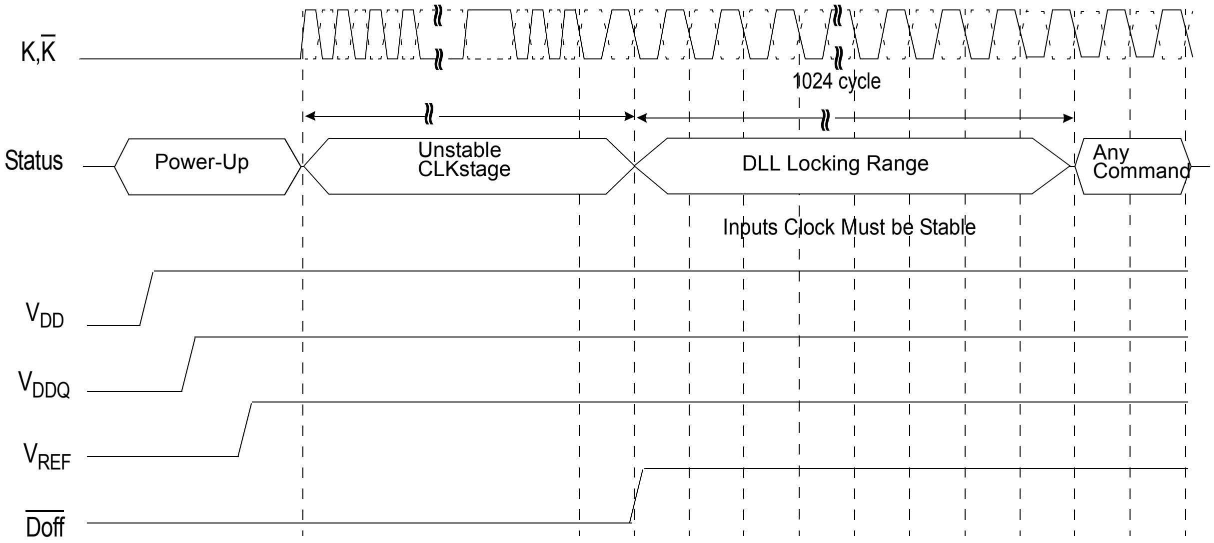
1. Apply power and keep $\overline{\text{Doff}}$ at low state (All other inputs may be undefined)
   - Apply VDD before VDDQ
   - Apply VDDQ before VREF or the same time with VREF
2. Just after the stable power and clock (K, $\overline{\text{K}}$, C, $\overline{\text{C}}$), take $\overline{\text{Doff}}$ to be high.
3. The additional 1024 cycles of clock input is required to lock the DLL after enabling DLL

* **Notes**: If you want to tie up the $\overline{\text{Doff}}$ pin to High with unstable clock, then you must stop the clock for a few seconds (Min. 30ns) to reset the DLL after it become a stable clock status.

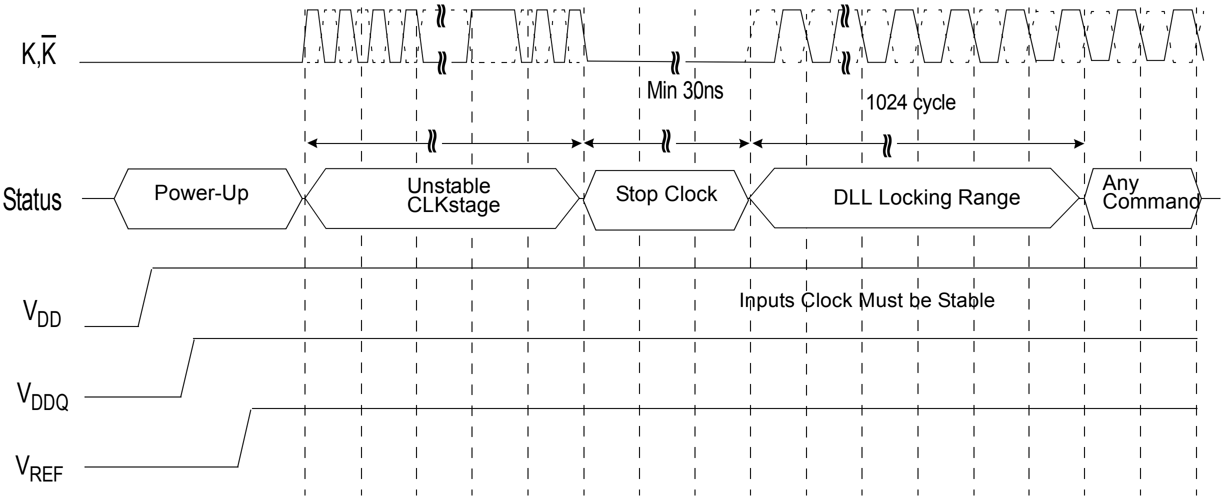
• DLL Constraints

1. DLL uses either K or C clock as its synchronizing input, the input should have low phase jitter which is specified as TKC var.
2. The lower end of the frequency at which the DLL can operate is 8.4ns.
3. If the incoming clock is unstable and the DLL is enabled, then the DLL may lock onto a wrong frequency and this may cause the failure in the initial stage.

Power up & Initialization Sequence ($\overline{\text{Doff}}$ pin controlled)



Power up & Initialization Sequence ($\overline{\text{Doff}}$ pin Fixed high, Clock controlled)



* **Notes**: When the operating frequency is changed, It is required to reset DLL again.
After reseting DLL, the minimum 1024 cycles of clock input is needed to lock the DLL.

Truth Tables

SYNCHRONOUS TRUTH TABLE

K	$\overline{R}$	$\overline{W}$	D		Q		Operation
			D(A0)	D(A1)	Q(A0)	Q(A1)	
Stopped	X	X	Previous state	Previous state	Previous state	Previous state	Clock Stop
↑	H	H	X	X	High-Z	High-Z	No Operation
↑	L	X	X	X	DOUT at $\overline{C}$(t+1)	DOUT at C(t+2)	Read
↑	X	L	Din at K(t)	Din at $\overline{K}$(t)	X	X	Write

Notes: 1. X means “Don′t Care”.
2. The rising edge of clock is symbolized by (↑).
3. Before enter into clock stop status, all pending read and write operations will be completed.

WRITE TRUTH TABLE(x18)

K	$\overline{K}$	$\overline{BW_0}$	$\overline{BW_1}$	Operation
↑		L	L	WRITE ALL BYTEs (K↑)
	↑	L	L	WRITE ALL BYTEs ($\overline{K}$↑)
↑		L	H	WRITE BYTE 0 (K↑)
	↑	L	H	WRITE BYTE 0 ($\overline{K}$↑)
↑		H	L	WRITE BYTE 1 (K↑)
	↑	H	L	WRITE BYTE 1 ($\overline{K}$↑)
↑		H	H	WRITE NOTHING (K↑)
	↑	H	H	WRITE NOTHING ($\overline{K}$↑)

Notes: 1. X means “Don′t Care”.
2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{K}$ (↑).
3. Assumes a WRITE cycle was initiated.
4. This table illustrates operation for x18 devices. x9 device operation is similar except that $\overline{BW}$ controls D0:D8.

WRITE TRUTH TABLE(x36)

K	$\overline{K}$	$\overline{BW_0}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	Operation
↑		L	L	L	L	WRITE ALL BYTEs (K↑)
	↑	L	L	L	L	WRITE ALL BYTEs ($\overline{K}$↑)
↑		L	H	H	H	WRITE BYTE 0 (K↑)
	↑	L	H	H	H	WRITE BYTE 0 ($\overline{K}$↑)
↑		H	L	H	H	WRITE BYTE 1 (K↑)
	↑	H	L	H	H	WRITE BYTE 1 ($\overline{K}$↑)
↑		H	H	L	L	WRITE BYTE 2 and BYTE 3 (K↑)
	↑	H	H	L	L	WRITE BYTE 2 and BYTE 3 ($\overline{K}$↑)
↑		H	H	H	H	WRITE NOTHING (K↑)
	↑	H	H	H	H	WRITE NOTHING ($\overline{K}$↑)

Notes: 1. X means “Don′t Care”.
2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{K}$ (↑).
3. Assumes a WRITE cycle was initiated.

Absolute Maximum Ratings*

Parameter		Symbol	Rating	Unit
Voltage on VDD Supply Relative to VSS		VDD	-0.5 to 2.9	V
Voltage on VDDQ Supply Relative to VSS		VDDQ	-0.5 to VDD	V
Voltage on Input Pin Relative to VSS		VIN	-0.5 to VDD+0.3	V
Storage Temperature		TSTG	-65 to 150	°C
Operating Temperature	Commercial / Industrial	TOPR	0 to 70 / -40 to 85	°C
Storage Temperature Range Under Bias		TBIAS	-10 to 85	°C

***Note:** 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. VDDQ must not exceed VDD during normal operation.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VDD	1.7	1.9	V
	VDDQ	1.4	1.9	V
Reference Voltage	VREF	0.68	0.95	V

DC Electrical Characteristics

Parameter	Symbol	test Conditions		Min	Max	Unit	Notes
Input Leakage Current	IIL	VDD=Max; VIN=VSS to VDDQ		-2	+2	μA	
Output Leakage Current	IOL	Output Disabled,		-2	+2	μA	
Operating Current (x36)	ICC	VDD=Max, IOUT=0mA Cycle Time ≥ tKHKH Min	-33	-	950	mA	1,5
			-30	-	890		
			-25	-	740		
Operating Current (x18)	ICC	VDD=Max, IOUT=0mA Cycle Time ≥ tKHKH Min	-33	-	820	mA	1,5
			-30	-	770		
			-25	-	670		
Operating Current (x9)	ICC	VDD=Max, IOUT=0mA Cycle Time ≥ tKHKH Min	-33	-	780	mA	1,5
			-30	-	740		
			-25	-	640		
Standby Current (NOP)	ISB1	Device deselected, IOUT=0mA, f=Max, All Inputs≤0.2V or ≥ VDD-0.2V	-33	-	370	mA	1,6
			-30	-	360		
			-25	-	340		
Output High Voltage	VOH1			VDDQ/2-0.12	VDDQ/2+0.12	V	2,7
Output Low Voltage	VOL1			VDDQ/2-0.12	VDDQ/2+0.12	V	3,7
Output High Voltage	VOH2	IOH=-1.0mA		VDDQ-0.2	VDDQ	V	4
Output Low Voltage	VOL2	IOL=1.0mA		VSS	0.2	V	4
Input Low Voltage	VIL			-0.3	VREF-0.1	V	8,9
Input High Voltage	VIH			VREF+0.1	VDDQ+0.3	V	8,10

Notes: 1. Minimum cycle. IOUT=0mA.
2. |IOH|=(VDDQ/2)/(RQ/5) for 175Ω ≤ RQ ≤ 350Ω.
3. |IOL|=(VDDQ/2)/(RQ/5) for 175Ω ≤ RQ ≤ 350Ω.
4. Minimum Impedance Mode when ZQ pin is connected to VDD.
5. Operating current is calculated with 50% read cycles and 50% write cycles.
6. Standby Current is only after all pending read and write burst operations are completed.
7. Programmable Impedance Mode.
8. These are DC test criteria. DC design criteria is VREF±50mV. The AC VIH/VIL levels are defined separately for measuring timing parameters.
9. VIL (Min.) DC=-0.3V, VIL (Min)AC=-1.5V(pulse width ≤ 3ns).
10. VIH (Max)DC=VDDQ+0.3, VIH (Max)AC=VDDQ+0.85V(pulse width ≤ 3ns).

AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input High Voltage	V_{IH} (AC)	VREF + 0.2	-	V	1,2
Input Low Voltage	V_{IL} (AC)	-	VREF - 0.2	V	1,2

Notes: 1. This condition is for AC function test only, not for AC parameter test.
2. To maintain a valid level, the transition edge of the input must:
a) Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$
b) Reach at least the target AC level
c) After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$

AC Timing Characteristics

Parameter	Symbol	-33		-30		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock									
Clock Cycle Time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKH}	3.00	8.40	3.30	8.40	4.00	8.40	ns	
Clock Phase Jitter (K, $\overline{K}$, C, $\overline{C}$)	$t_{KC\ var}$		0.20		0.20		0.20	ns	5
Clock High Time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKL}	1.2		1.32		1.60		ns	
Clock Low Time (K, $\overline{K}$, C, $\overline{C}$)	t_{KLKH}	1.2		1.32		1.60		ns	
Clock to $\overline{\text{Clock}}$ ($K\uparrow \rightarrow \overline{K}\uparrow$, $C\uparrow \rightarrow \overline{C}\uparrow$)	$t_{KH\overline{K}H}$	1.35		1.49		1.80		ns	
Clock to data clock ($K\uparrow \rightarrow C\uparrow$, $\overline{K}\uparrow \rightarrow \overline{C}\uparrow$)	t_{KHCH}	0.00	1.30	0.00	1.45	0.00	1.80	ns	
DLL Lock Time (K, C)	$t_{KC\ lock}$	1024		1024		1024		cycle	6
K Static to DLL reset	$t_{KC\ reset}$	30		30		30		ns	
Output Times									
C, $\overline{C}$ High to Output Valid	t_{CHQV}		0.45		0.45		0.45	ns	3
C, $\overline{C}$ High to Output Hold	t_{CHQX}	-0.45		-0.45		-0.45		ns	3
C, $\overline{C}$ High to Echo Clock Valid	t_{CHCQV}		0.45		0.45		0.45	ns	
C, $\overline{C}$ High to Echo Clock Hold	t_{CHCQX}	-0.45		-0.45		-0.45		ns	
CQ, $\overline{CQ}$ High to Output Valid	t_{CQHQV}		0.25		0.27		0.30	ns	7
CQ, $\overline{CQ}$ High to Output Hold	t_{CQHQX}	-0.25		-0.27		-0.30		ns	7
$\overline{C}$, High to Output High-Z	t_{CHQZ}		0.45		0.45		0.45	ns	3
$\overline{C}$, High to Output Low-Z	t_{CHQX1}	-0.45		-0.45		-0.45		ns	3
Setup Times									
Address valid to K rising edge	t_{AVKH}	0.28		0.30		0.35		ns	
Control inputs valid to K rising edge	t_{IVKH}	0.28		0.30		0.35		ns	2
Data-in valid to K, $\overline{K}$ rising edge	t_{DVKH}	0.28		0.30		0.35		ns	
Hold Times									
K rising edge to address hold	t_{KHAX}	0.28		0.30		0.35		ns	
K rising edge to control inputs hold	t_{KHIX}	0.28		0.30		0.35		ns	
K, $\overline{K}$ rising edge to data-in hold	t_{KHDX}	0.28		0.30		0.35		ns	

Notes: 1. All address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control singles are $\overline{R}$, $\overline{W}$,BW_0,BW_1 and BW_2, BW_3, also for x36
3. If C,$\overline{C}$ are tied high, K,$\overline{K}$ become the references for C,$\overline{C}$ timing parameters.
4. To avoid bus contention, at a given voltage and temperature $tCHQX_1$ is bigger than tCHQZ.
The specs as shown do not imply bus contention because $tCHQX_1$ is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9V) than tCHQZ, which is a MAX parameter (worst case at 70°C, 1.7V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6. Vdd slew rate must be less than 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once Vdd and input clock are stable.
7. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ± 0.1 ns variation from echo clock to data.
The data sheet parameters reflect tester guardbands and test setup variations.

Thermal Resistance

Parameter	Symbol	Typical	Unit	Notes
Junction to Ambient	θ_{JA}	20.2	°C/W	
Junction to Case	θ_{JC}	2.1	°C/W	

Note: Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. $T_J=T_A + P_D$ x θ_{JA}

Pin Capacitance

Parameter	Symbol	Test Condition	Typ	Max	Unit	Notes
Address Control Input Capacitance	CIN	VIN=0V	3.5	4	pF	
Input and Output Capacitance	COUT	VOUT=0V	4	5	pF	
Clock Capacitance	CCLK	-	3	4	pF	

Note: 1. Parameters are tested with RQ=250Ω and VDDQ=1.5V.

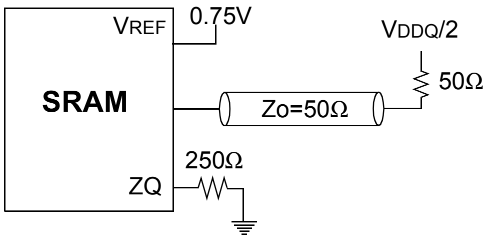
2. Periodically sampled and not 100% tested.

AC Test Conditions

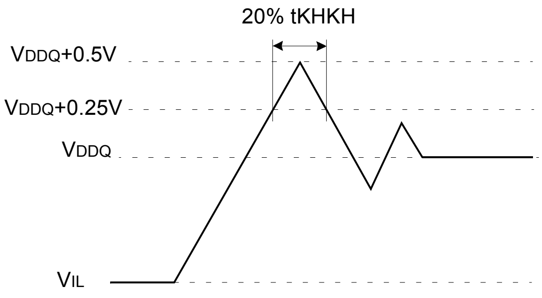
Parameter	Symbol	Value	Unit
Core Power Supply Voltage	VDD	1.7~1.9	V
Output Power Supply Voltage	VDDQ	1.4~1.9	V
Input High/Low Level	VIH/VIL	1.25/0.25	V
Input Reference Level	VREF	0.75	V
Input Rise/Fall Time	TR/TF	0.3/0.3	ns
Output Timing Reference Level		VDDQ/2	V

Note: Parameters are tested with RQ=250Ω

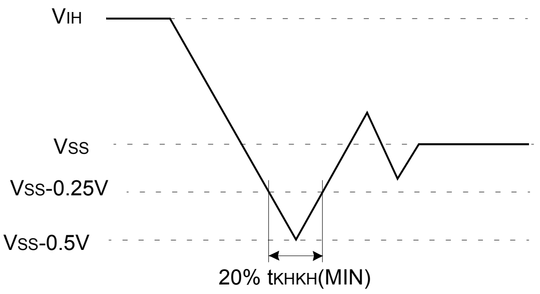
AC Test Output Load



Overershoot Timing

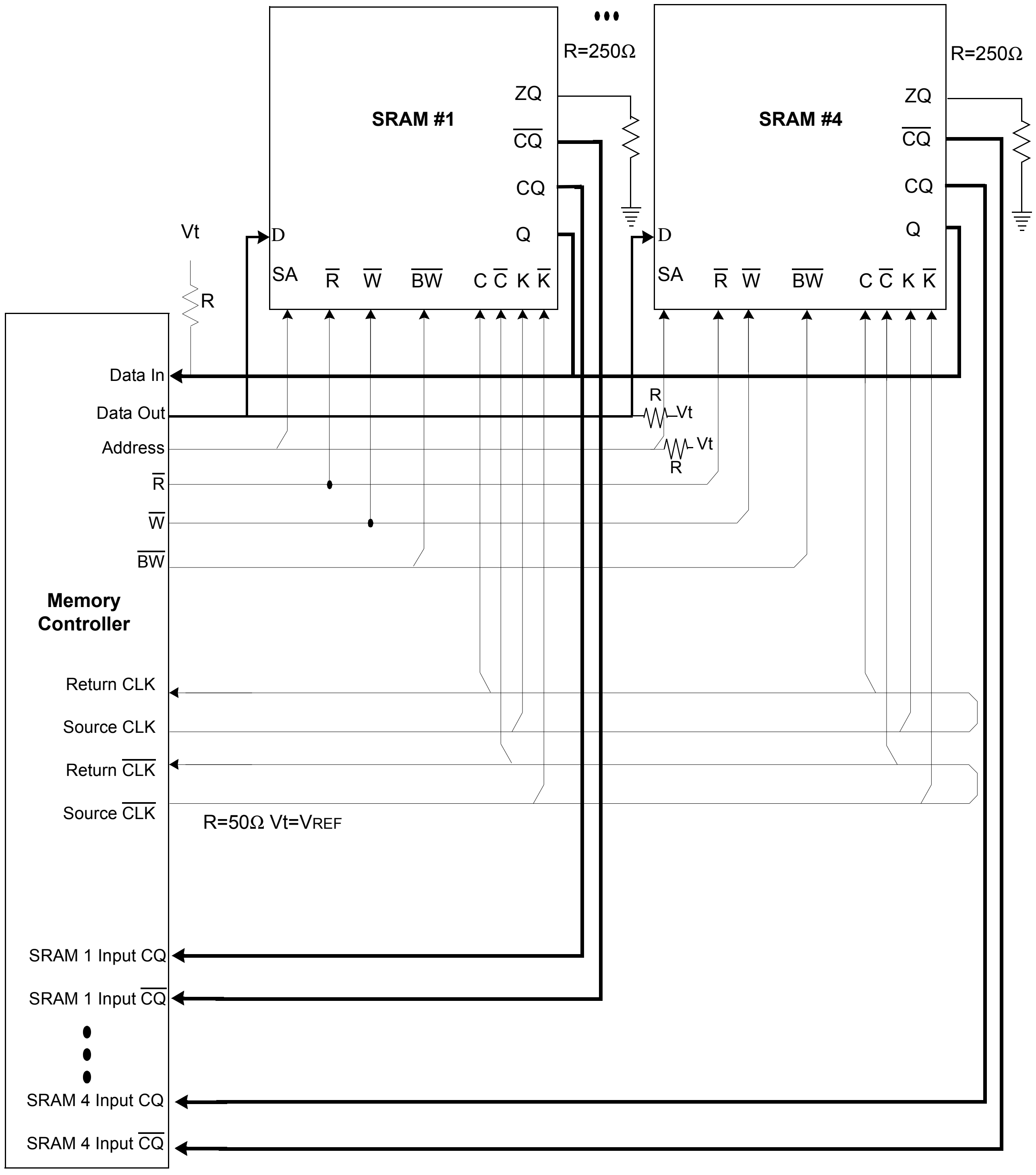


Undershoot Timing

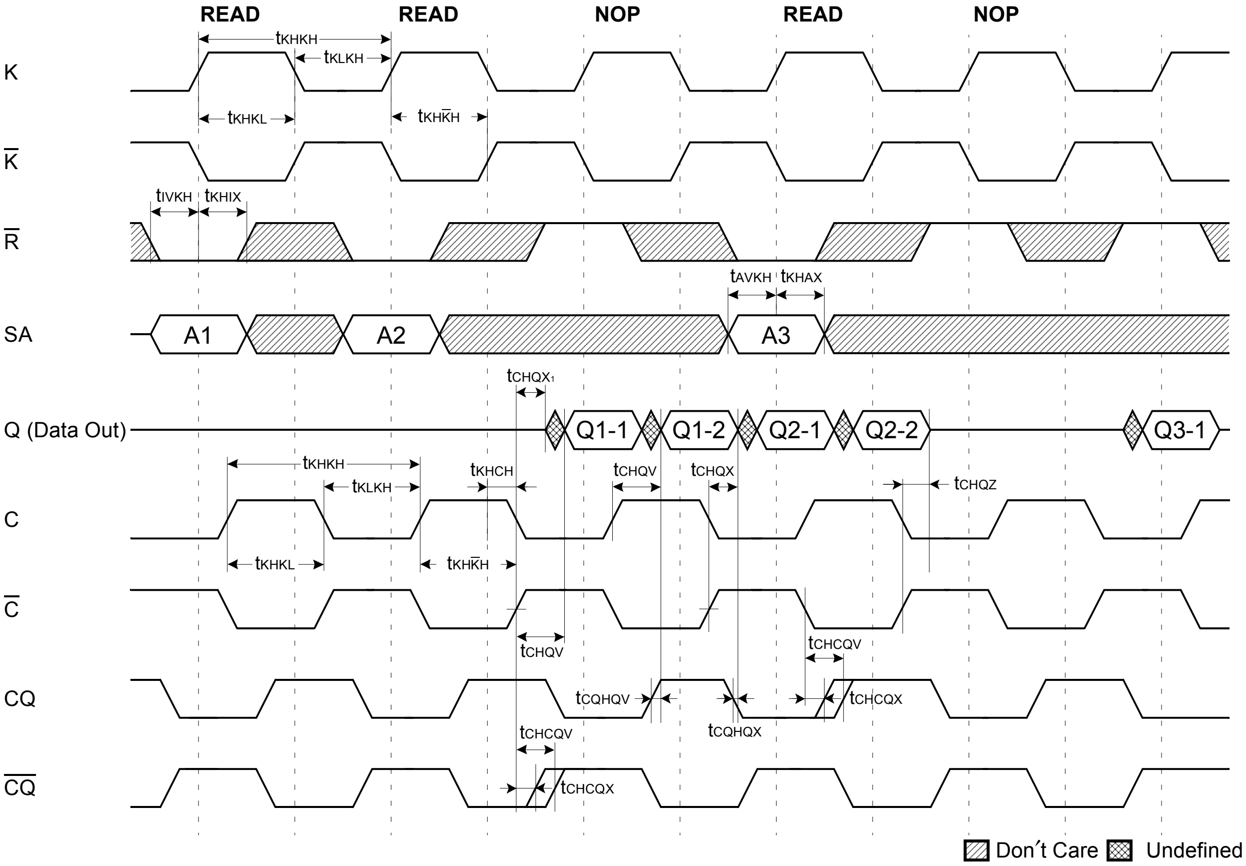


Note: For power-up, VIH ≤ VDDQ+0.3V and VDD ≤ 1.7V and VDDQ ≤ 1.4V t ≤ 200ms

Application Information



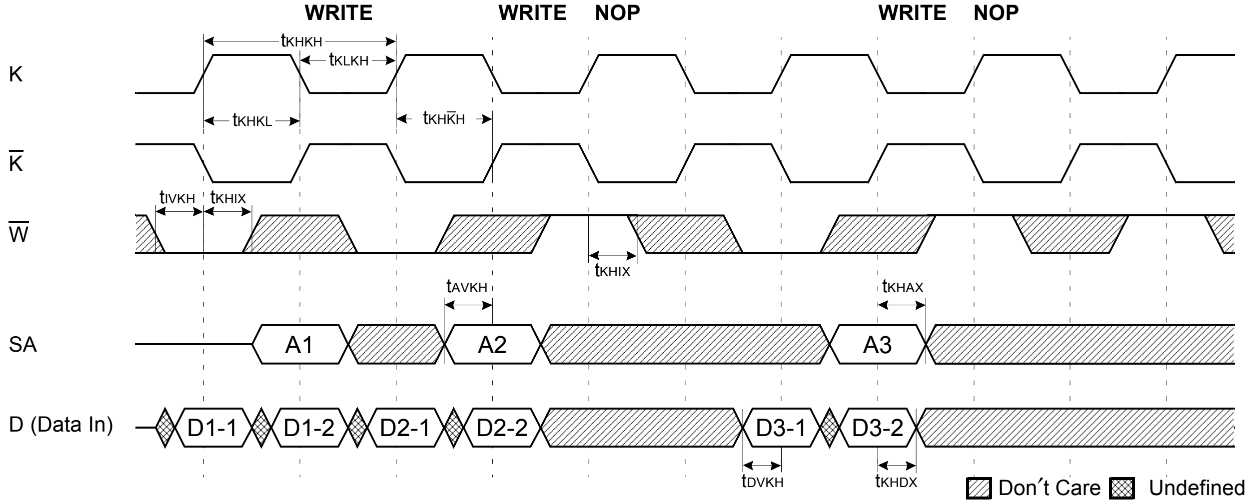
TIMING WAVE FORMS OF READ AND NOP



Note: 1. Q1-1 refers to output from address A1+0, Q1-2 refers to output from address A1+1 i.e. the next internal burst address following A1+0.

2. Outputs are disabled one cycle after a NOP.

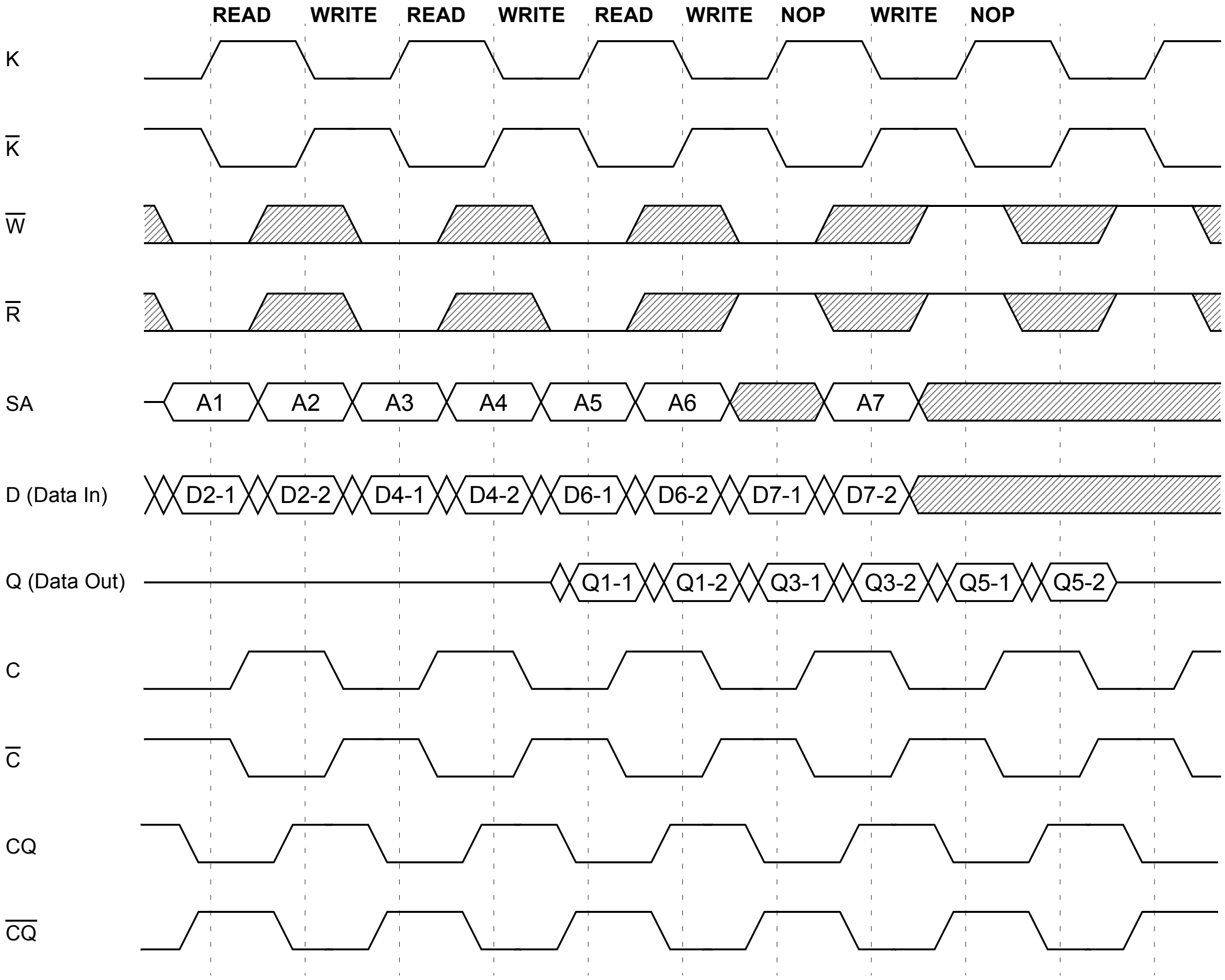
TIMING WAVE FORMS OF WRITE AND NOP



Note: 1.D1-1 refers to input to address A1+0, D1-2 refers to input to address A1+1, i.e the next internal burst address following A1+0.

2. $\overline{\text{BWx}}$ ($\overline{\text{NWx}}$) assumed active.

TIMING WAVE FORMS OF READ, WRITE AND NOP



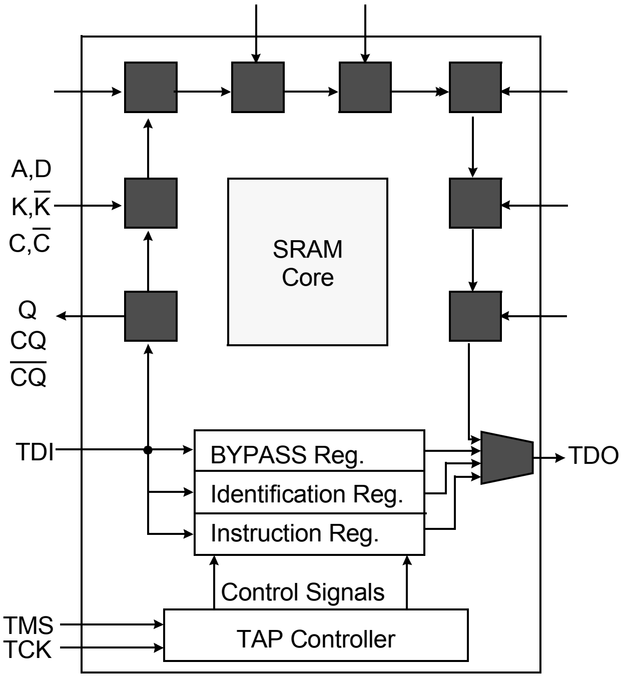
▨ Don't Care ▩ Undefined

Note: 1. If address A1=A2, data Q1-1=D2-1, data Q1-2=D2-2.
Write data is forwarded immediately as read results.
2.$\overline{BWx}$ ($\overline{NWx}$) assumed active.

IEEE 1149.1 Test Access Port and Boundary Scan-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP).The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to VSS to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



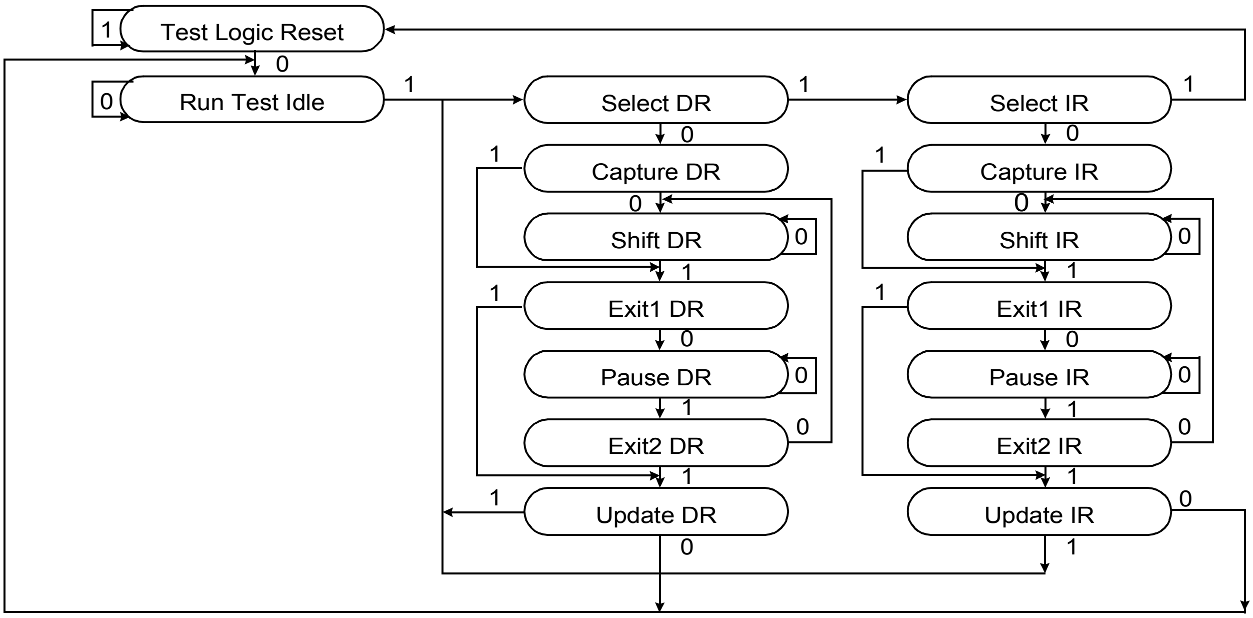
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	RESERVED	Do Not Use	6
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	RESERVED	Do Not Use	6
1	1	1	BYPASS	Bypass Register	4

NOTE:

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to VSS when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram



Scan Register Definition

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
2M x 36 4M x 18 8M x 9	3 bits	1 bit	32 bits	109 bits

ID Registration Definition

Part	Revision Number (31:29)	Part Configuration (28:12)	Netsol JEDEC Code (11: 1)	Start Bit(0)
2M x 36 4M x 18 8M x 9	000	00def0wx0t0q0b0s0	01111011001	1

Note: Part Configuration
/def=011 for 72Mb, /wx=11 for x36, 10 for x18, 00 for x9
/t=1 for DLL Ver., 0 for non-DLL Ver. /q=1 for Quadruple, 0 for DDR /b=1 for 4Bit Burst, 0 for 2Bit Burst /s=1 for Separate I/O, 0 for Common I/O

Boundary Scan Exit Order

Order	Pin ID
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E
37	10D
38	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	10A
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	2A
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1H
85	1J
86	2J
87	3K
88	3J
89	2K
90	1K
91	2L
92	3L
93	1M
94	1L
95	3N
96	3M
97	1N
98	2M
99	3P
100	2N
101	2P
102	1P
103	3R
104	4R
105	4P
106	5P
107	5N
108	5R
109	Internal

Note: 1. NC pins are read as "X" (i.e. don´t care.)

JTAG DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Input High Level	V_{IH}	1.3	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.5	V	
Output High Voltage (I_{OH}=-2mA)	V_{OH}	1.4	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.4	V	

Note: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC Test Conditions

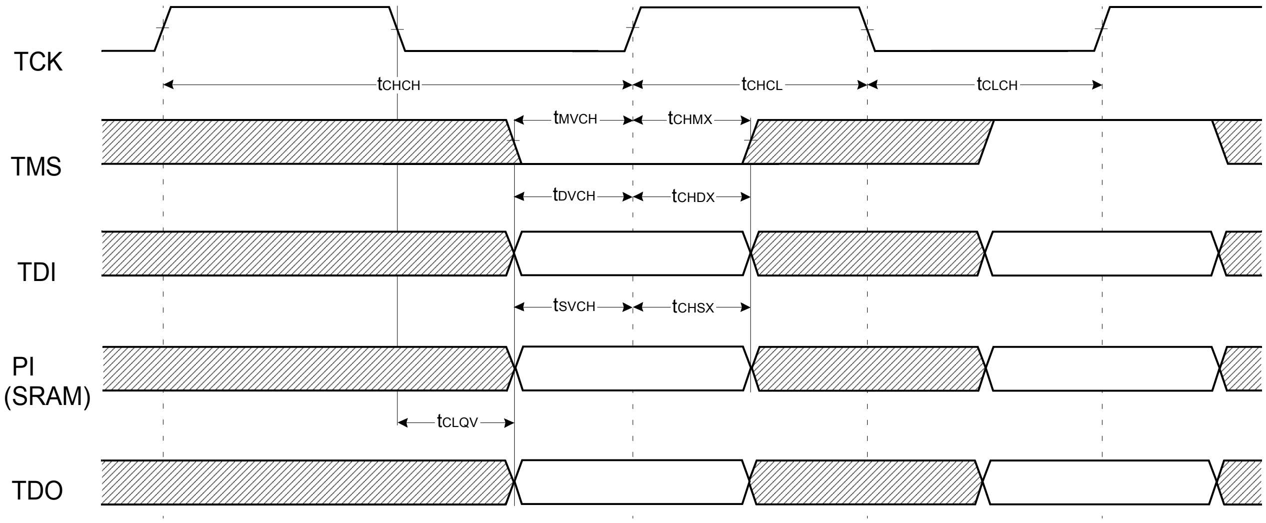
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.8/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	1

Note: 1. See SRAM AC test output load on page 11.

JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

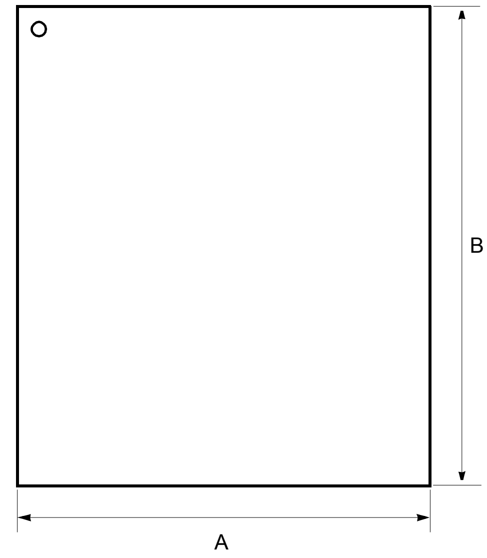
JTAG Timing Diagram



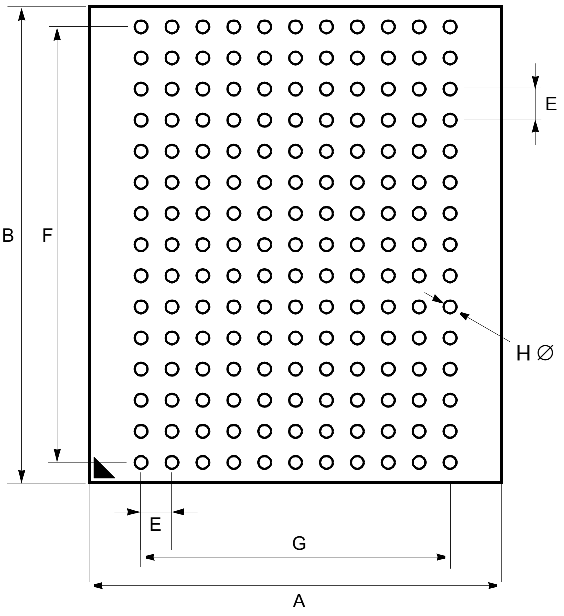
165 FBGA Package Dimensions - Lead & Lead Free

13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Grid Array

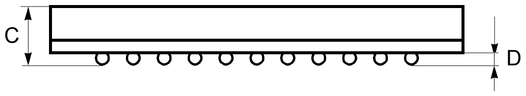
Top View



Bottom View



Side View



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	13 ± 0.1	mm		**E**	1.0	mm	
B	15 ± 0.1	mm		**F**	14.0	mm	
C	1.3 ± 0.1	mm		**G**	10.0	mm	
D	0.35 ± 0.05	mm		**H**	0.5 ± 0.05	mm	