36Mb Quadruple-II+ BL4 SRAM Specification

(2.0 Clock Read Latency)

165FBGA with Pb & Pb Free

(ROHS Compliant)

Document Title

1Mx36 & 2Mx18 & 4Mx9 - Bit Quadruple-II+ Burst Length of 4 SRAM
(2.0 Clock Read Latency)

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Sep. 2012	Preliminary
1.0	Final spec release Add current spec value	Feb. 2013	Final
1.1	Change Thermal Resistance θJA value from 20.8°C/W to 16.3°C/W	Apr. 2013	Final

1Mx36 & 2Mx18 & 4Mx9 - Bit Quadruple-II+ Burst Length of 4 SRAM (2.0 Clock Read Latency)

Features

- 1.8V+0.1V/-0.1V Power Supply.
- DLL circuitry for wide output data valid window and future frequency scaling.
- I/O Supply Voltage 1.5V+0.1V/-0.1V for 1.5V I/O, 1.8V+0.1V/-0.1V for 1.8V I/O.
- Separate independent read and write data ports with concurrent read and write operation
- HSTL I/O
- Full data coherency, providing most current data.
- Synchronous pipeline read with self timed late write
- Read latency : 2 clock cycles.
- Registered address, control and data input/output.
- DDR (Double Data Rate) Interface on read and write ports.
- Fixed 4-bit burst for both read and write operation.
- Clock-stop supports to reduce current.
- Two input clocks (K and $\overline{K}$) for accurate DDR timing at clock rising edges only.
- Two echo clocks (CQ and $\overline{CQ}$) to enhance output data traceability.
- Data Valid pin(QVLD) supported
- Single address bus.
- Byte write (x9, x18, x36) function.
- Separate read/write control pin ($\overline{R}$ and $\overline{W}$)
- Simple depth expansion with no data contention.
- Programmable output impedance(ZQ).
- JTAG 1149.1 compatible test access port.
- 165FBGA(11x15 ball array FBGA) with body size of 13x15mm & Lead Free

Key Parameters

Part Number	Org.	Freq. (MHz)	Cycle Time (ns)	Access Time (ns)	RoHS
S7S3236T4M-E(F)C(I)45	x36	450	2.2	0.45	O
S7S3236T4M-E(F)C(I)40		400	2.5	0.45	O
S7S3218T4M-E(F)C(I)45	x18	450	2.2	0.45	O
S7S3218T4M-E(F)C(I)40		400	2.5	0.45	O
S7S3209T4M-E(F)C(I)45	x9	450	2.2	0.45	O
S7S3209T4M-E(F)C(I)40		400	2.5	0.45	O

* -E(F)C(I)
E(F) [Package type]: E-Pb Free, F-Pb
C(I) [Operating Temperature]: C-Commercial, I-Industrial

GENERAL DESCRIPTION

The S7S3236T4M, S7S3218T4M and S7S3209T4M are 37,748,736-bits Quadruple Synchronous Pipelined Burst SRAMs. They are organized as 1,048,576 words by 36bits for S7S3236T4M, 2,097,152 words by 18bits for S7S3218T4M and 4,194,304 words by 9bits for S7S3209T4M.

The Quadruple operation is possible by supporting DDR read and write operations through separate data output and input ports with the same cycle. Memory bandwidth is maximized as data can be transferred into and out of SRAM on every rising edge of K and $\overline{K}$. And totally independent read and write ports eliminate the need for high speed bus turn around.

Address for read and write are latched on alternate rising edges of the input clock K. Data inputs and outputs, and all control signals are synchronized to the input clock (K or $\overline{K}$). Read data are referenced to echo clock (CQ or $\overline{CQ}$) outputs.

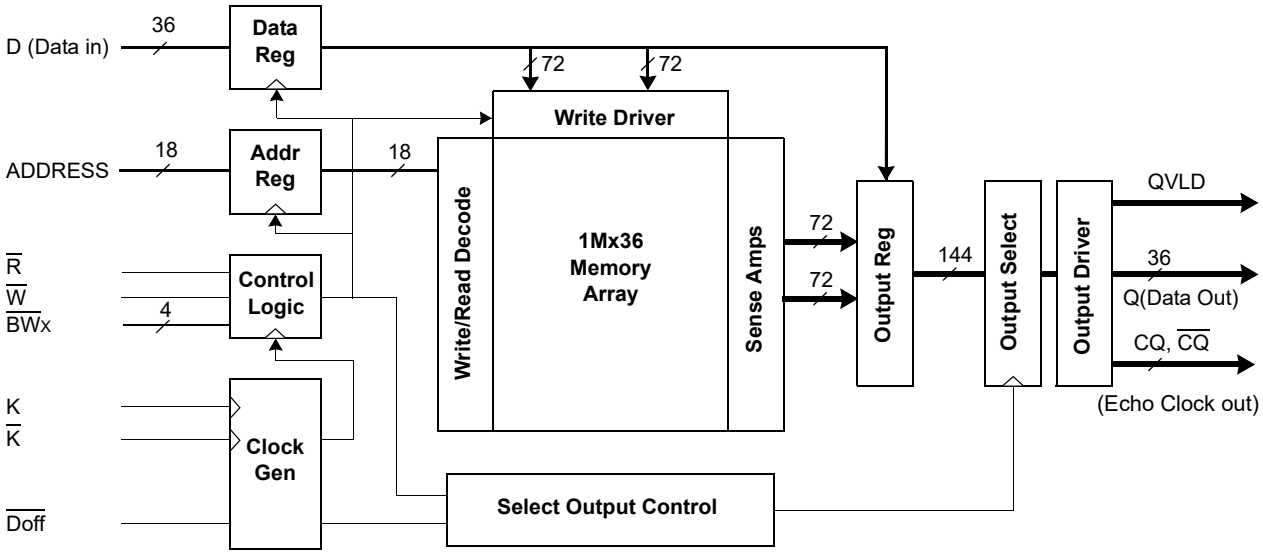
Common address bus is used to access address both for read and write operations. The internal burst counter is fixed to 4-bit sequential for both read and write operations requiring two full clock bus cycles. Any request that attempts to interrupt a burst operation in progress is ignored.

Synchronous pipeline read and late write enable high speed operations. Simple depth expansion is accomplished by using $\overline{R}$ and $\overline{W}$ for port selection. Byte write operation is supported with $\overline{BW}_0$ and $\overline{BW}_1$ ($\overline{BW}_2$ and $\overline{BW}_3$) pins for x18 (x36) device and only $\overline{BW}$ pin for x9 device.

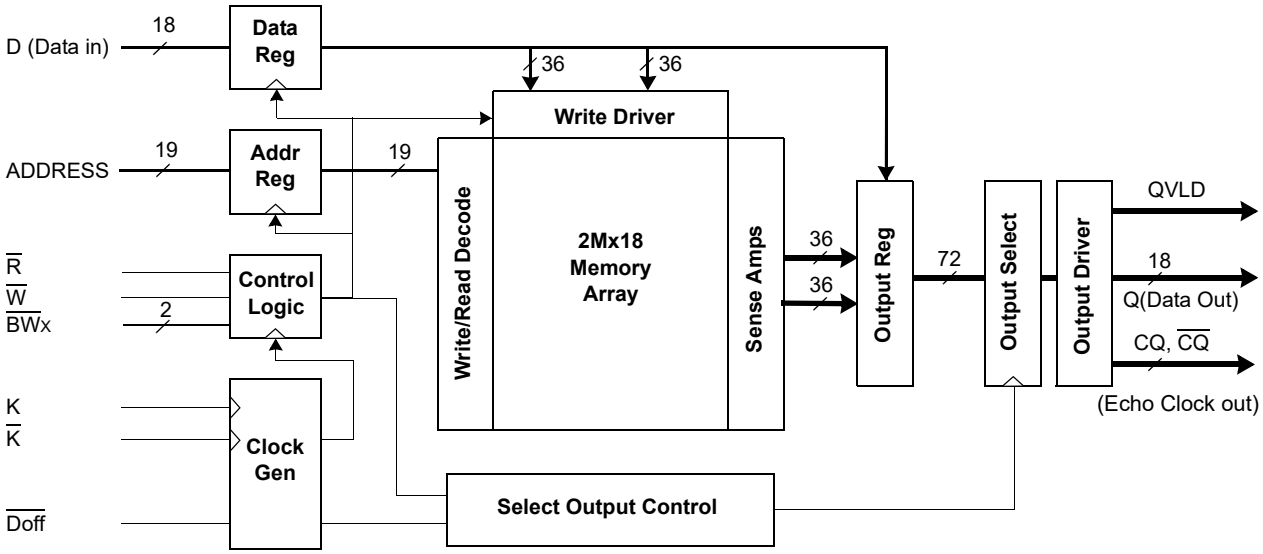
IEEE 1149.1 serial boundary scan (JTAG) simplifies monitoring package pads attachment status with system.

The S7S3236T4M, S7S3218T4M and S7S3209T4M are implemented with Netsol's high performance 6T CMOS technology and is available in 165pin FBGA packages. Multiple power and ground pins minimize ground bounce.

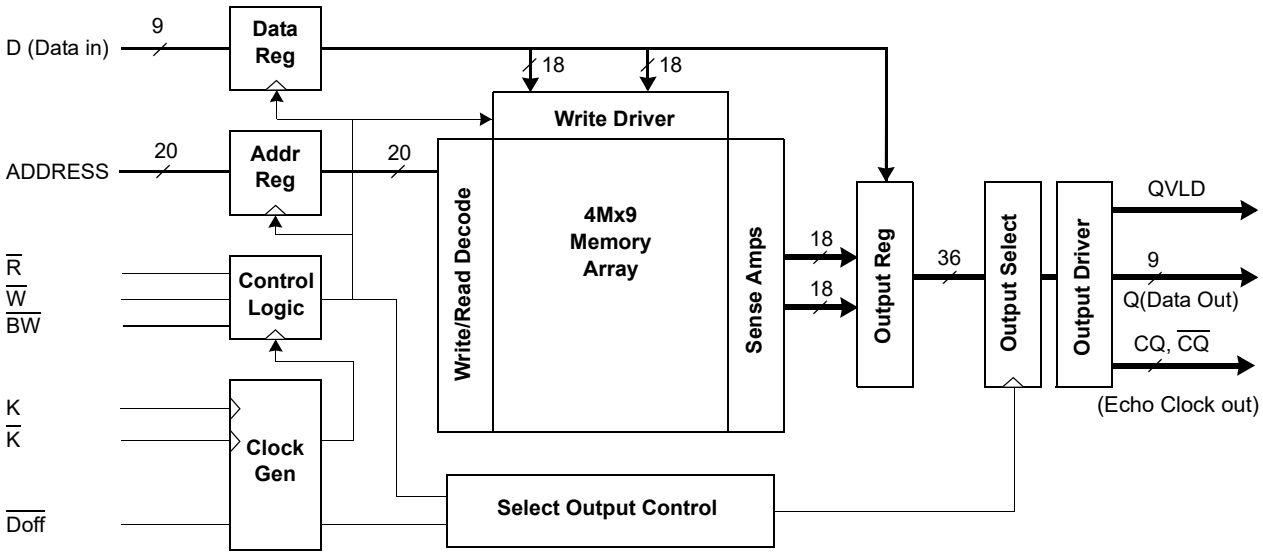
Logic Block Diagram - S7S3236T4M (1M x 36)



Logic Block Diagram - S7S3218T4M (2M x 18)



Logic Block Diagram - S7S3209T4M (4M x 9)



165FBGA PKG Pin Configurations - S7S3236T4M (1Mx36) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/SA*	NC/SA*	$\overline{W}$	$\overline{BW_2}$	$\overline{K}$	$\overline{BW_1}$	$\overline{R}$	SA	NC/SA*	CQ
B	Q27	Q18	D18	SA	$\overline{BW_3}$	K	$\overline{BW_0}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	NC	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	QVLD	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI

Notes: 1. * Checked No Connect (NC) or Vss pins are reserved for higher density address, i.e. 3A for 72Mb, 10A for 144Mb.
2. $\overline{BW_0}$ controls write to D0:D8, $\overline{BW_1}$ controls write to D9:D17, $\overline{BW_2}$ controls write to D18:D26 and $\overline{BW_3}$ controls write to D27:D35.

Pin Name

Symbol	Pin Numbers	Description	Note
K, $\overline{K}$	6B, 6A	Input Clock	1
QVLD	6P	Q Valid Output	
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA	9A,4B,8B,5C,7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-35	10P,11N,11M,10K,11J,11G,10E,11D,11C,10N,9M,9L 9J,10G,9F,10D,9C,9B,3B,3C,2D,3F,2G,3J,3L,3M,2N 1C,1D,2E,1G,1J,2K,1M,1N,2P	Data Inputs	
Q0-35	11P,10M,11L,11K,10J,11F,11E,10C,11B,9P,9N,10L 9K,9G,10F,9E,9D,10B,2B,3D,3E,2F,3G,3K,2L,3N 3P,1B,2C,1E,1F,2J,1K,1L,2M,1P	Data Outputs	
$\overline{W}$	4A	Write Control Pin, active when low	
$\overline{R}$	8A	Read Control Pin, active when low	
$\overline{BW_0}$, $\overline{BW_1}$,$\overline{BW_2}$, $\overline{BW_3}$	7B,7A,5A,5B	Block Write Control Pin, active when low	
V_{REF}	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
V_{DD}	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (1.8 V)	
V_{DDQ}	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
V_{SS}	4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M, 8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	2A,3A,10A,6C,6R	No Connect	3

Notes: 1. K or $\overline{K}$ cannot be set to V_{REF} voltage.
2. When ZQ pin is directly connected to V_{DD} output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

165FBGA PKG Pin Configurations - S7S3218T4M (2Mx18) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/SA*	SA	$\overline{W}$	$\overline{BW_1}$	$\overline{K}$	NC	$\overline{R}$	SA	NC/SA*	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW_0}$	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	NC	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	QVLD	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI

Notes: 1. * Checked No Connect(NC) pins are reserved for higher density address, i.e. 10A for 72Mb, 2A for 144Mb.
2. $\overline{BW_0}$ controls write to D0:D8 and $\overline{BW_1}$ controls write to D9:D17.

Pin Name

Symbol	Pin Numbers	Description	Note
K, $\overline{K}$	6B, 6A	Input Clock	1
QVLD	6P	Q Valid Output	
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA	3A,9A,4B,8B,5C,7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-17	10P,11N,11M,10K,11J,11G,10E,11D,11C,3B,3C,2D, 3F,2G,3J,3L,3M,2N	Data Inputs	
Q0-17	11P,10M,11L,11K,10J,11F,11E,10C,11B,2B,3D,3E, 2F,3G,3K,2L,3N,3P	Data Outputs	
$\overline{W}$	4A	Write Control Pin, active when low	
$\overline{R}$	8A	Read Control Pin, active when low	
$\overline{BW_0}$, $\overline{BW_1}$	7B, 5A	Block Write Control Pin, active when low	
V_{REF}	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
V_{DD}	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (1.8 V)	
V_{DDQ}	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
V_{SS}	4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	2A,7A,10A,1B,5B,9B,10B,1C,2C,6C,9C,1D,9D,10D,1E,2E,9E, 1F,9F,10F,1G,9G,10G,1J,2J,9J,1K,2K,9J,1L,9L,10L,1M,2M,9M, 1N,9N,10N,1P,2P,9P,6R	No Connect	3

Notes: 1. K or $\overline{K}$ cannot be set to V_{REF} voltage.
2. When ZQ pin is directly connected to V_{DD} output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

165FBGA PKG Pin Configurations - S7S3209T4M (4Mx9) - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/SA*	SA	$\overline{W}$	NC	$\overline{K}$	NC	$\overline{R}$	SA	SA	CQ
B	NC	NC	NC	SA	NC	K	$\overline{BW}$	SA	NC	NC	Q4
C	NC	NC	NC	V_{SS}	SA	NC	SA	V_{SS}	NC	NC	D4
D	NC	D5	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D3	Q3
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	D6	Q6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q2	D2
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	Q7	D7	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D1
N	NC	D8	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	Q8	SA	SA	QVLD	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI

Notes: 1. * Checked No Connect(NC) pins are reserved for higher density address, i.e. 2A for 72Mb, 7A for 144Mb.
2. $\overline{BW}$ controls write to D0:D8.

Pin Name

Symbol	Pin Numbers	Description	Note
K, $\overline{K}$	6B, 6A	Input Clock	1
QVLD	6P	Q Valid Output	
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA	3A,9A,10A,4B,8B,5C,7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
D0-8	11M,11J,10E,11C,2D,2G,3L,2N,10P	Data Inputs	
Q0-8	11L,10J,11E,11B,3E,3G,2L,3P,11P	Data Outputs	
$\overline{W}$	4A	Write Control Pin, active when low	
$\overline{R}$	8A	Read Control Pin, active when low	
$\overline{BW}$	7B	Block Write Control Pin, active when low	
V_{REF}	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
V_{DD}	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (1.8 V)	
V_{DDQ}	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
V_{SS}	4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	2A,5A,7A,1B,2B,3B,5B,9B,10B,1C,2C,3C,6C,9C,10,1D,3D, 9D,10D,11D,1E,2E,9E,1F,2F,3F,9F,10F,11F,1G,9G,10G,11G, 1J,2J,3J,9J,1K,2K,3K,9K,10K,11K,1L,9L,10L,1M,2M,3M,9M 10M,1N,3N,9N,10N,11N,1P,2P,9P,6R	No Connect	3

Notes: 1. K or $\overline{K}$ cannot be set to V_{REF} voltage.
2. When ZQ pin is directly connected to V_{DD} output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

Read Operations

Read cycles are initiated by activating $\overline{R}$ at the rising edge of the positive input clock K. Address is presented and stored in the read address register synchronized with K clock. For 4-bit burst DDR operation, it will access four 36-bit, 18-bit or 9-bit data words with each read command.

The first pipelined data is transferred out of the device triggered by K clock rising edge. Next burst data is triggered by the rising edge of following $\overline{K}$ clock rising edge. The process continues until all four data are transferred. Continuous read operations are initiated with K clock rising edge. And pipelined data are transferred out of device on every rising edge of both K and $\overline{K}$ clocks. Initial read data latency is 2 clock cycles when DLL is on.

When the $\overline{R}$ is disabled after a read operation, the S7S3236T4M, S7S3218T4M and S7S3209T4M will first complete burst read operation before entering into deselect mode at the next K clock rising edge. Then output drivers disabled automatically to high impedance state.

Write Operations

Write cycles are initiated by activating $\overline{W}$ at the rising edge of the positive input clock K. Address is presented and stored in the write address register synchronized with K clock. For 4-bit burst DDR operation, it will write four 36-bit, 18-bit or 9-bit data words with each write command.

The first “late” data is transferred and registered into the device synchronous with next K clock rising edge. Next burst data is transferred and registered synchronous with following $\overline{K}$ clock rising edge. The process continues until all four data are transferred and registered. Continuous write operations are initiated with K rising edge. And “late write” data is presented to the device on every rising edge of both K and $\overline{K}$ clocks.

The device disregards input data presented on the same cycle $\overline{W}$ disabled. When the $\overline{W}$ is disabled after a write operation, the S7S3236T4M, S7S3218T4M and S7S3209T4M will first complete burst write operation before entering into deselect mode at the next K clock rising edge.

The S7S3236T4M, S7S3218T4M and S7S3209T4M support byte write operations. With activating $\overline{BW_0}$ or $\overline{BW_1}$ ($\overline{BW_2}$ or $\overline{BW_3}$) in write cycle, only one byte of input data is presented. In S7S3218T4M, $\overline{BW_0}$ controls write operation to D0:D8, $\overline{BW_1}$ controls write operation to D9:D17. And in S7S3236T4M $\overline{BW_2}$ controls write operation to D18:D26, $\overline{BW_3}$ controls write operation to D27:D35. And in S7S3209T4M $\overline{BW}$ controls write operation to D0:D8.

Depth Expansion

Separate input and output ports enables easy depth expansion. Each port can be selected and deselected independently and read and write operation do not affect each other. Before chip deselected, all read and write pending operations are completed.

Programmable Impedance Output Buffer Operation

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to V_{SS} through a precision resistor (RQ). The allowable range of RQ is 175Ω and 350Ω. The value of RQ (within 15% tolerance) is five times the output impedance desired. For example, 250Ω resistor will give an output impedance of 50Ω. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles.

In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM.

To guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

Output Valid Pin (QVLD)

The Q Valid indicates valid output data. QVLD is actiated half cycle before the read data for the receiver to be ready for capturing the data. QVLD is edge aligned with CQ and $\overline{CQ}$

Echo clock operation

To assure the output traceability, the SRAM provides the output Echo clock, pair of compliment clock CQ and $\overline{CQ}$, which are synchronized with internal data output. Echo clocks run free during normal operation.

The Echo clock is triggered by internal output clock signal, and transferred to external through same structures as output driver.

Clock Consideration

S7S3236T4M,S7S3218T4M and S7S3209T4M utilizes internal DLL (Delay-Locked Loops) for maximum output data valid window. It can be placed into a stopped-clock state to minimize power with a modest restart time of 2048 clock cycles.
Circuitry automatically resets the DLL when absence of input clock is detected.

Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, then V_{IN}. V_{DD} and V_{DDQ} can be applied simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN}, V_{REF}, V_{DDQ}, V_{DD}, V_{SS}. V_{DD} and V_{DDQ} can be removed simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-down.

Detail Specification of Power-Up Sequence in Quadruple-II+ SRAM

Quadruple-II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

• Power-Up Sequence

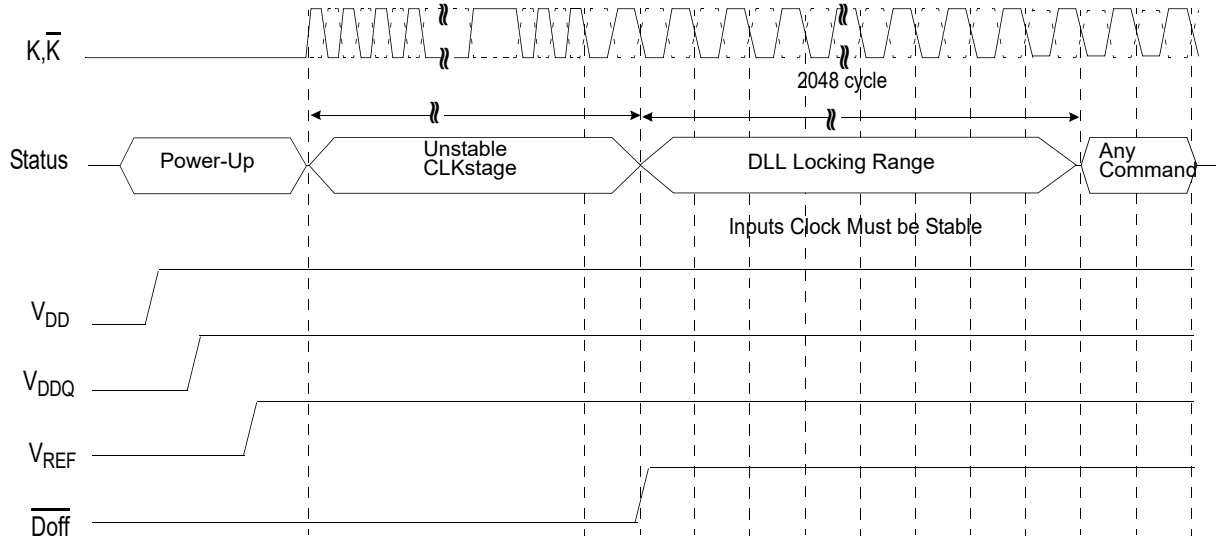
1. Apply power and keep $\overline{Doff}$ at low state (All other inputs may be undefined)
   - Apply VDD before VDDQ
   - Apply VDDQ before VREF or the same time with VREF
2. Just after the stable power and clock (K, $\overline{K}$), take $\overline{Doff}$ to be high.
3. The additional 2048 cycles of clock input is required to lock the DLL after enabling DLL

*** Notes**: If you want to tie up the $\overline{Doff}$ pin to High with unstable clock, then you must stop the clock for a few seconds (Min. 30ns) to reset the DLL after it become a stable clock status.

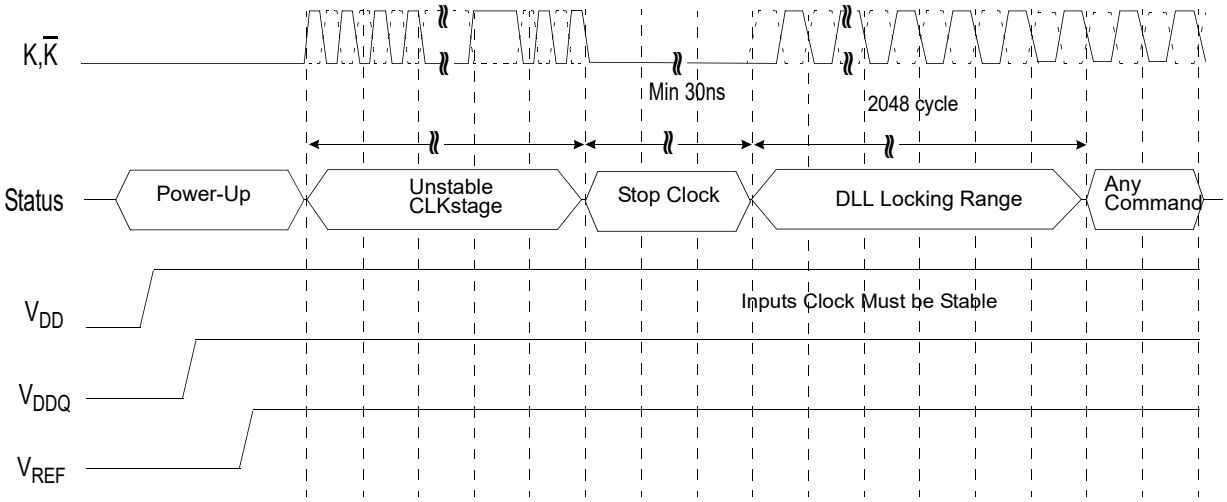
• DLL Constraints

1. DLL uses K clock as its synchronizing input, the input should have low phase jitter which is specified as TK var.
2. The lower end of the frequency at which the DLL can operate is 120MHz.
3. If the incoming clock is unstable and the DLL is enabled, then the DLL may lock onto a wrong frequency and this may cause the failure in the initial stage.

Power up & Initialization Sequence ($\overline{\text{Doff}}$ pin controlled)



Power up & Initialization Sequence ($\overline{\text{Doff}}$ pin Fixed high, Clock controlled)



*** Notes**: When the operating frequency is changed, It is required to reset DLL again.
After reseting DLL, the minimum 2048 cycles of clock input is needed to lock the DLL.

Truth Tables

SYNCHRONOUS TRUTH TABLE

K	$\overline{R}$	$\overline{W}$	D				Q				OPERATION
			D(A1)	D(A2)	D(A3)	D(A4)	Q(A1)	Q(A2)	Q(A3)	Q(A4)	
Stopped	X	X	Previous state	Previous state	Previous state	Previous state	Previous state	Previous state	Previous state	Previous state	Clock Stop
↑	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	No Operation
↑	L[4]	X	X	X	X	X	Q_{OUT} at K(t+2)	Q_{OUT} at $\overline{K}$(t+2)	Q_{OUT} at K(t+3)	Q_{OUT} at $\overline{K}$(t+3)	Read
↑	H[5]	L[4]	Din at K(t+1)	Din at $\overline{K}$(t+1)	Din at K(t+2)	Din at $\overline{K}$(t+2)	X	X	X	X	Write

Notes: 1. X means "Don't Care".
2. The rising edge of clock is symbolized by (↑).
3. Before enter into clock stop status, all pending read and write operations will be completed.
4. This signal was HIGH on previous K clock rising edge. Initiating consecutive READ or WRITE operations on consecutive K clock rising edges is not permitted. The device will ignore the second request.
5. If this signal was LOW to initiated the previous cycle, this signal becomes a don't care for this operation however it is strongly recommended that this signal is brought HIGH as shown in the truth table.

WRITE TRUTH TABLE(x18)

K	$\overline{K}$	$\overline{BW_0}$	$\overline{BW_1}$	Operation
↑		L	L	WRITE ALL BYTEs (K↑)
	↑	L	L	WRITE ALL BYTEs ($\overline{K}$↑)
↑		L	H	WRITE BYTE 0 (K↑)
	↑	L	H	WRITE BYTE 0 ($\overline{K}$↑)
↑		H	L	WRITE BYTE 1 (K↑)
	↑	H	L	WRITE BYTE 1 ($\overline{K}$↑)
↑		H	H	WRITE NOTHING (K↑)
	↑	H	H	WRITE NOTHING ($\overline{K}$↑)

Notes: 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{K}$ (↑).
3. Assumes a WRITE cycle was initiated.
4. This table illustrates operation for x18 devices. x9 device operation is similar except that $\overline{BW}$ controls D0:D8.

WRITE TRUTH TABLE(x36)

K	$\overline{K}$	$\overline{BW_0}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	Operation
↑		L	L	L	L	WRITE ALL BYTEs (K↑)
	↑	L	L	L	L	WRITE ALL BYTEs ($\overline{K}$↑)
↑		L	H	H	H	WRITE BYTE 0 (K↑)
	↑	L	H	H	H	WRITE BYTE 0 ($\overline{K}$↑)
↑		H	L	H	H	WRITE BYTE 1 (K↑)
	↑	H	L	H	H	WRITE BYTE 1 ($\overline{K}$↑)
↑		H	H	L	L	WRITE BYTE 2 and BYTE 3 (K↑)
	↑	H	H	L	L	WRITE BYTE 2 and BYTE 3 ($\overline{K}$↑)
↑		H	H	H	H	WRITE NOTHING (K↑)
	↑	H	H	H	H	WRITE NOTHING ($\overline{K}$↑)

Notes: 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{K}$ (↑).
3. Assumes a WRITE cycle was initiated.

Absolute Maximum Ratings*

Parameter		Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to V_{SS}		V_{DD}	-0.5 to 2.9	V
Voltage on V_{DDQ} Supply Relative to V_{SS}		V_{DDQ}	-0.5 to V_{DD}	V
Voltage on Input Pin Relative to V_{SS}		V_{IN}	-0.5 to V_{DD}+0.3	V
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial / Industrial	T_{OPR}	0 to 70 / -40 to 85	°C
Storage Temperature Range Under Bias		T_{BIAS}	-10 to 85	°C

***Note:** 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. V_{DDQ} must not exceed V_{DD} during normal operation.

OPERATING CONDITIONS ($0°C \le T_A \le 70°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
	V_{DDQ}	1.4	1.5	1.9	V
Reference Voltage	V_{REF}	0.7	0.75	0.95	V
Input Low Voltage(DC) [2,3]	$V_{IL(DC)}$	-0.3	-	V_{REF} - 0.1	V
Input High Voltage(DC) [2,4]	$V_{IH(DC)}$	V_{REF} + 0.1	-	V_{DDQ} + 0.3	V
Input Low Voltage(AC) [6,7]	$V_{IL(AC)}$	-	-	V_{REF} - 0.2	V
Input High Voltage(AC) [6,7]	$V_{IH(AC)}$	V_{REF} + 0.2	-	-	V

Note: 1. V_{DDQ} must not exceed V_{DD} during normal operation.

2. These are DC test criteria. DC design criteria is $V_{REF} \pm 50mV$. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.

3. V_{IL} (Min)DC=-0.3V, V_{IL} (Min)AC=-1.5V(pulse width ≤ 3ns).

4. V_{IH} (Max)DC=V_{DDQ}+0.3V, V_{IH} (Max)AC=V_{DDQ}+0.85V(pulse width ≤ 3ns).

5. Overshoot : V_{IH} (AC) ≤ V_{DDQ}+0.5V for t ≤ 50% t_{KHKH}(MIN).
Undershoot: V_{IL} (AC) ≤ V_{SS}-0.5V for t ≤ 50% t_{KHKH}(MIN).

6. This condition is for AC function test only, not for AC parameter test.

7. To maintain a valid level, the transiting edge of the input must:
a) Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$
b) Reach at least the target AC level
c) After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$

DC Electrical Characteristics

Parameter	Symbol	test Conditions		Min	Max	Unit	Notes
Input Leakage Current	I_{IL}	V_{DD}=Max; V_{IN}=V_{SS} to V_{DDQ}		-2	+2	μA	
Output Leakage Current	I_{OL}	Output Disabled,		-2	+2	μA	
Operating Current (x36)	I_{CC}	V_{DD}=Max, I_{OUT}=0mA Cycle Time ≥ t_{KHKH} Min	-45		760	mA	1,4
			-40	-	690		
Operating Current (x18)	I_{CC}	V_{DD}=Max, I_{OUT}=0mA Cycle Time ≥ t_{KHKH} Min	-45		640	mA	1,4
			-40	-	580		
Operating Current (x9)	I_{CC}	V_{DD}=Max, I_{OUT}=0mA Cycle Time ≥ t_{KHKH} Min	-45		625	mA	1,4
			-40	-	570		
Standby Current (NOP)	I_{SB1}	Device deselected, I_{OUT}=0mA, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-45		300	mA	1,5
			-40	-	280		
Output High Voltage	V_{OH1}			V_{DDQ}/2-0.12	V_{DDQ}/2+0.12	V	2,6
Output Low Voltage	V_{OL1}			V_{DDQ}/2-0.12	V_{DDQ}/2+0.12	V	2,6
Output High Voltage	V_{OH2}	I_{OH}=-1.0mA		V_{DDQ}-0.2	V_{DDQ}	V	3
Output Low Voltage	V_{OL2}	I_{OL}=1.0mA		V_{SS}	0.2	V	3

Notes: 1. Minimum cycle. I_{OUT}=0mA.
2. $|I_{OH}|=(V_{DDQ}/2)/(RQ/5)$ for $175\Omega \le RQ \le 350\Omega$. $|I_{OL}|=(V_{DDQ}/2)/(RQ/5)$ for $175\Omega \le RQ \le 350\Omega$.
3. Minimum Impedance Mode when ZQ pin is connected to V_{DD}.
4. Operating current is calculated with 50% read cycles and 50% write cycles.
5. Standby Current is only after all pending read and write burst operations are completed.
6. Programmable Impedance Mode.

AC Timing Characteristics (V_{DD}=1.8V±0.1V, T_A=0°C to +70°C)

Parameter	Symbol	-45		-40		Unit	Notes
		Min	Max	Min	Max		
Clock							
Clock Cycle Time (K, $\overline{K}$)	t_{KHKH}	2.22	8.40	2.50	8.40	ns	
Clock Phase Jitter (K, $\overline{K}$)	$t_{KC\ var}$		0.15		0.20	ns	4
Clock High Time (K, $\overline{K}$)	t_{KHKL}	0.4		0.4		ns	
Clock Low Time (K, $\overline{K}$)	t_{KLKH}	0.4		0.4		ns	
Clock to $\overline{Clock}$ (K↑ → $\overline{K}$↑)	$t_{KH\overline{K}H}$	0.94		1.06		ns	
DLL Lock Time (K, C)	$t_{KC\ lock}$	2048		2048		cycle	5
K Static to DLL reset	$t_{KC\ reset}$	30		30		ns	
Output Times							
K, $\overline{K}$ High to Output Valid	t_{KHQV}		0.45		0.45	ns	
K, $\overline{K}$ High to Output Hold	t_{KHQX}	-0.45		-0.45		ns	
K, $\overline{K}$ High to Echo Clock Valid	t_{KHCQV}		0.45		0.45	ns	
K, $\overline{K}$ High to Echo Clock Hold	t_{KHCQX}	-0.45		-0.45		ns	
CQ, $\overline{CQ}$ High to Output Valid	t_{CQHQV}		0.15		0.20	ns	
CQ, $\overline{CQ}$ High to Output Hold	t_{CQHQX}	-0.15		-0.20		ns	
CQ High to $\overline{CQ}$ High	$t_{CQH\overline{CQ}H}$	0.85		1.0			6
K, $\overline{K}$ High to Output High-Z	t_{KHZ}		0.45		0.45	ns	
K, $\overline{K}$ High to Output Low-Z	t_{KLZ}	-0.45		-0.45		ns	
CQ, CQ High to QVLD Valid	t_{QVLD}	-0.15	0.15	-0.2	0.2	ns	
Setup Times							
Address valid to K rising edge	t_{AVKH}	0.275		0.40		ns	
Control inputs valid to K rising edge	t_{IVKH}	0.275		0.40		ns	2
Data-in valid to K, $\overline{K}$ rising edge	t_{DVKH}	0.22		0.28		ns	
Hold Times							
K rising edge to address hold	t_{KHAX}	0.275		0.40		ns	
K rising edge to control inputs hold	t_{KHIX}	0.275		0.40		ns	
K, $\overline{K}$ rising edge to data-in hold	t_{KHDX}	0.22		0.28		ns	

Notes: 1. All address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control singles are $\overline{R}$, $\overline{W}$. $\overline{BW}_x$ does not apply to this parameters
However $\overline{BW}_x$ signals obey the data setup and hold times.
3. To avoid bus contention, at a given voltage and temperature tKLZ is bigger than tKHZ.
The specs as shown do not imply bus contention because tKLZ is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9V) than tKHZ, which is a MAX parameter (worst case at 70°C, 1.7V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
4. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
5. Vdd slew rate must be less than 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once Vdd and input clock are stable.
6. This parameter is extrapolated from the input timing parameters (tKH$\overline{K}$H - 200ps is the internal jitter.) this parameter is only guaranteed by design and not tested in production

Thermal Resistance

Parameter	Symbol	Typical	Unit	Notes
Junction to Ambient	θ_{JA}	16.3	°C/W	
Junction to Case	θ_{JC}	2.3	°C/W	
Junction to Pins	θ_{JB}	4.3	°C/W	

Note: Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. $T_J = T_A + P_D \times \theta_{JA}$

Pin Capacitance

Parameter	Symbol	Test Condition	Typ	Max	Unit	Notes
Address Control Input Capacitance	C_{IN}	V_{IN}=0V	3.5	4	pF	
Input and Output Capacitance	C_{OUT}	V_{OUT}=0V	4	5	pF	
Clock Capacitance	C_{CLK}	-	3	4	pF	

Note: 1. Parameters are tested with RQ=250Ω and V_{DDQ}=1.5V.

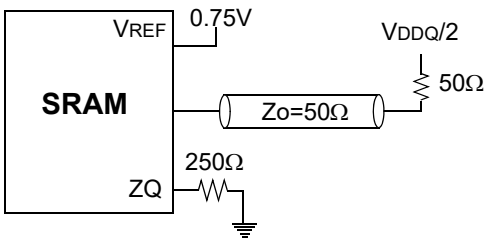
2. Periodically sampled and not 100% tested.

AC Test Conditions

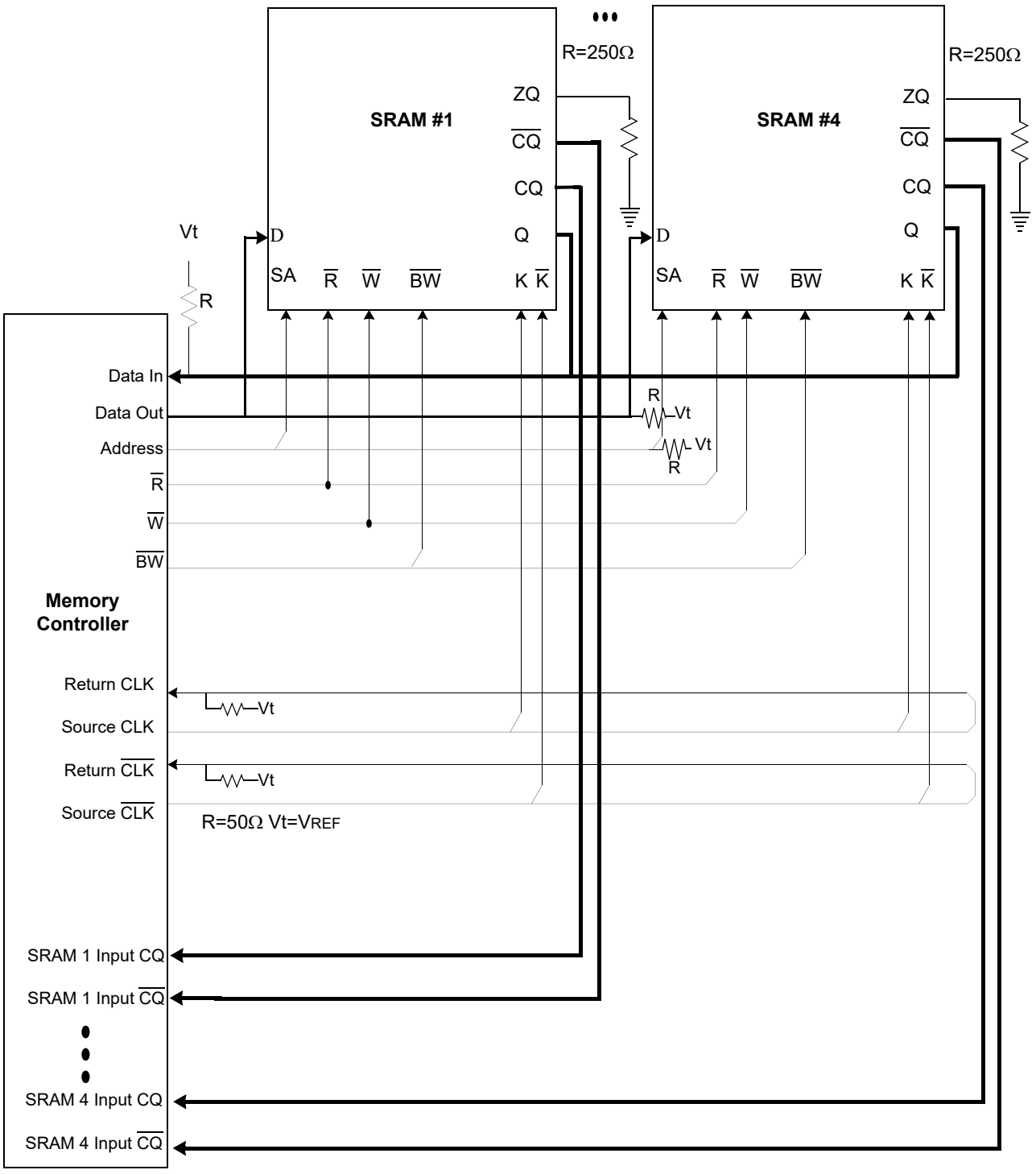
Parameter	Symbol	Value	Unit
Core Power Supply Voltage	V_{DD}	1.7~1.9	V
Output Power Supply Voltage	V_{DDQ}	1.4~1.9	V
Input High/Low Level	V_{IH}/V_{IL}	1.25/0.25	V
Input Reference Level	V_{REF}	0.75	V
Input Rise/Fall Time	T_R/T_F	0.3/0.3	ns
Output Timing Reference Level		$V_{DDQ}/2$	V

Note: Parameters are tested with RQ=250Ω

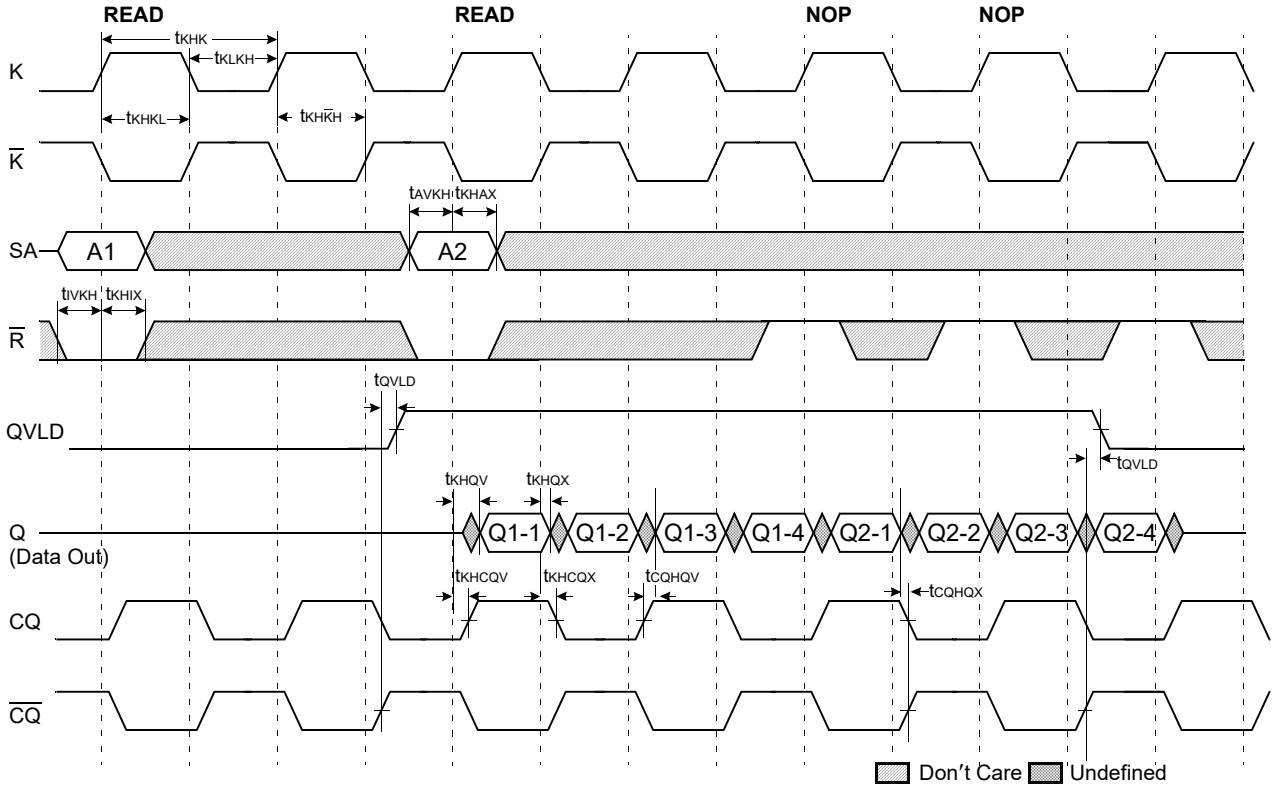
AC Test Output Load



Application Information

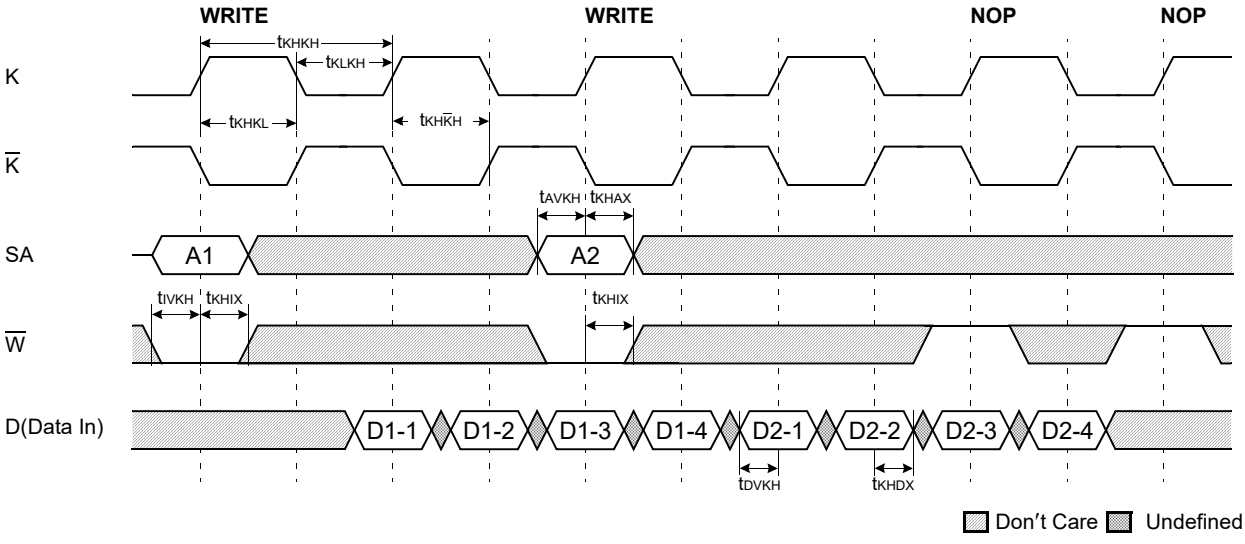


TIMING WAVE FORMS OF READ AND NOP



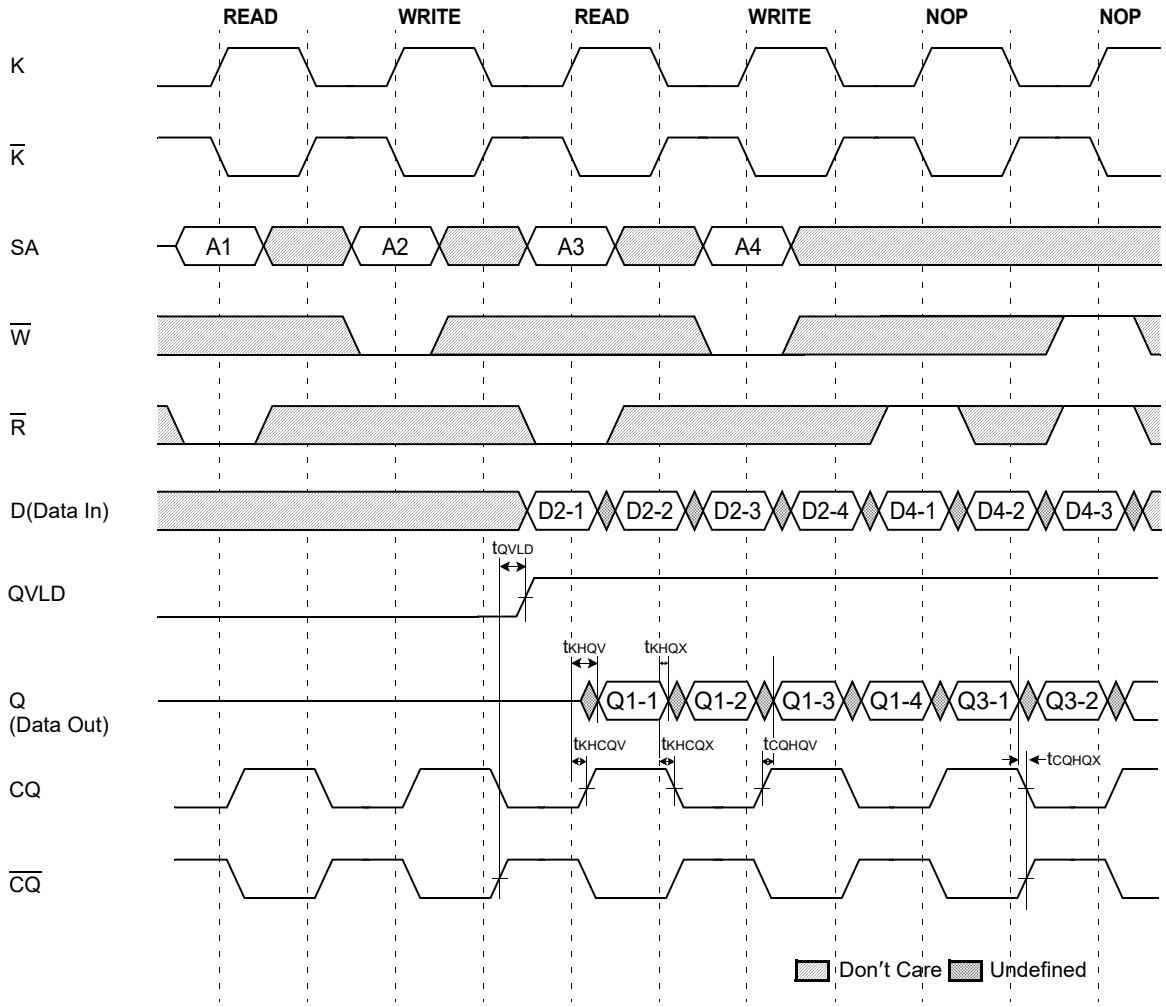
Note: 1. Q1-1 refers to output from address A1+0, Q1-2 refers to output from address A1+1 i.e. the next internal burst address following A1+0.
2. Outputs are disabled one cycle after a NOP.

TIMING WAVE FORMS OF WRITE AND NOP



Note: 1. D1-1 refers to input to address A1+0, D1-2 refers to input to address A1+1, i.e the next internal burst address following A1+0.
2. $\overline{BWx}$ assumed active.

TIMING WAVE FORMS OF READ, WRITE AND NOP

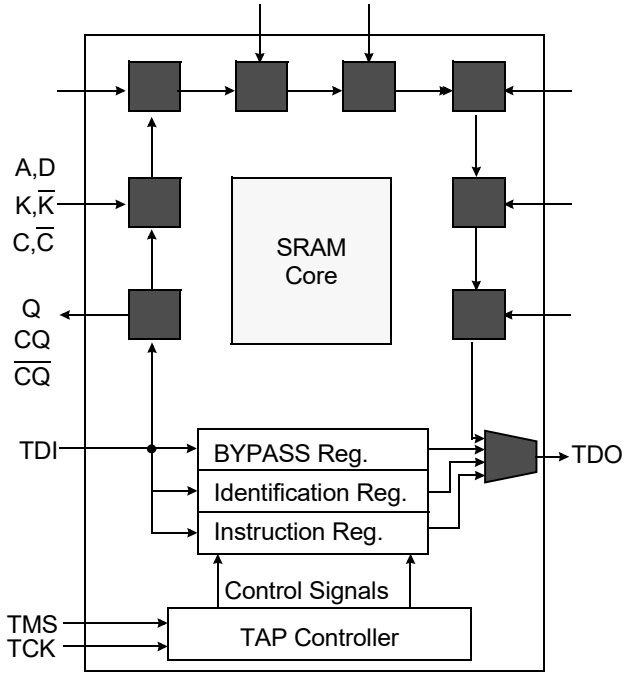


Note: 1. If address A3=A2, data Q3-1=D2-1, data Q3-2=D2-2, data Q3-3=D2-3, data Q3-4=D2-4
Write data is forwarded immediately as read results.
2.$\overline{BWx}$ assumed active.

IEEE 1149.1 Test Access Port and Boundary Scan-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP).The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



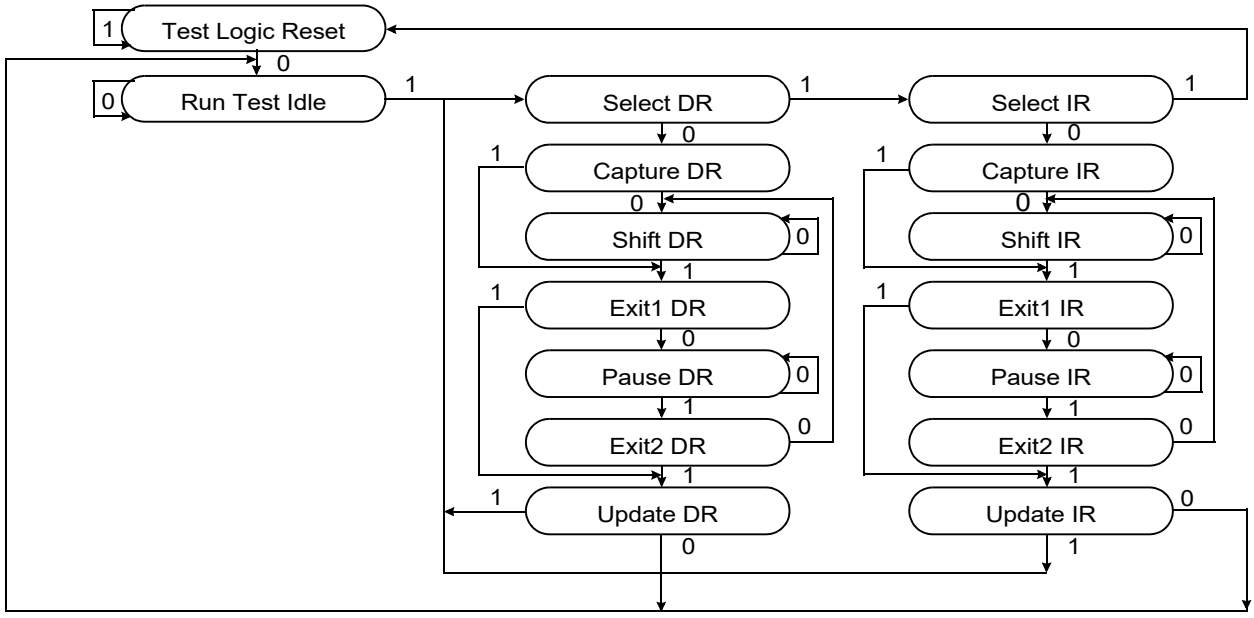
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	RESERVED	Do Not Use	6
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	RESERVED	Do Not Use	6
1	1	1	BYPASS	Bypass Register	4

NOTE:

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram



Scan Register Definition

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1M x 36 2M x 18 4M x 9	3 bits	1 bit	32 bits	109 bits

ID Registration Definition

Part	Revision Number (31:29)	Part Configuration (28:12)	Netsol JEDEC Code (11: 1)	Start Bit(0)
1M x 36 2M x 18 4M x 9	000	00def0wx0tpqlb0s0	01111011001	1

Note: Part Configuration
/def=010 for 36Mb, /wx=11 for x36, 10 for x18, 00 for x9
/t=1 for DLL Ver., 0 for non-DLL Ver. /p=1 for Quadruple-II+ or DDR-II+, 0 for Quadruple-II or DDR-II
/q=1 for Quadruple, 0 for DDR /l=1 for 2.5 read latency, 0 for 2.0 read latency (applicable only to Quadruple-II+ and DDR-II+)
/b=1 for 4Bit Burst, 0 for 2Bit Burst /s=1 for Separate I/O, 0 for Common I/O

Boundary Scan Exit Order

Order	Pin ID	Order	Pin ID	Order	Pin ID
1	6R	37	10D	73	2C
2	6P	38	9E	74	3E
3	6N	39	10C	75	2D
4	7P	40	11D	76	2E
5	7N	41	9C	77	1E
6	7R	42	9D	78	2F
7	8R	43	11B	79	3F
8	8P	44	11C	80	1G
9	9R	45	9B	81	1F
10	11P	46	10B	82	3G
11	10P	47	11A	83	2G
12	10N	48	10A	84	1H
13	9P	49	9A	85	1J
14	10M	50	8B	86	2J
15	11N	51	7C	87	3K
16	9M	52	6C	88	3J
17	9N	53	8A	89	2K
18	11L	54	7A	90	1K
19	11M	55	7B	91	2L
20	9L	56	6B	92	3L
21	10L	57	6A	93	1M
22	11K	58	5B	94	1L
23	10K	59	5A	95	3N
24	9J	60	4A	96	3M
25	9K	61	5C	97	1N
26	10J	62	4B	98	2M
27	11J	63	3A	99	3P
28	11H	64	2A	100	2N
29	10G	65	1A	101	2P
30	9G	66	2B	102	1P
31	11F	67	3B	103	3R
32	11G	68	1C	104	4R
33	9F	69	1B	105	4P
34	10F	70	3D	106	5P
35	11E	71	3C	107	5N
36	10E	72	1D	108	5R
				109	Internal

Note: 1. NC pins are read as "X" (i.e. don't care.)

JTAG DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Input High Level	V_{IH}	1.3	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.5	V	
Output High Voltage (I_{OH}=-2mA)	V_{OH}	1.4	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.4	V	

Note: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC Test Conditions

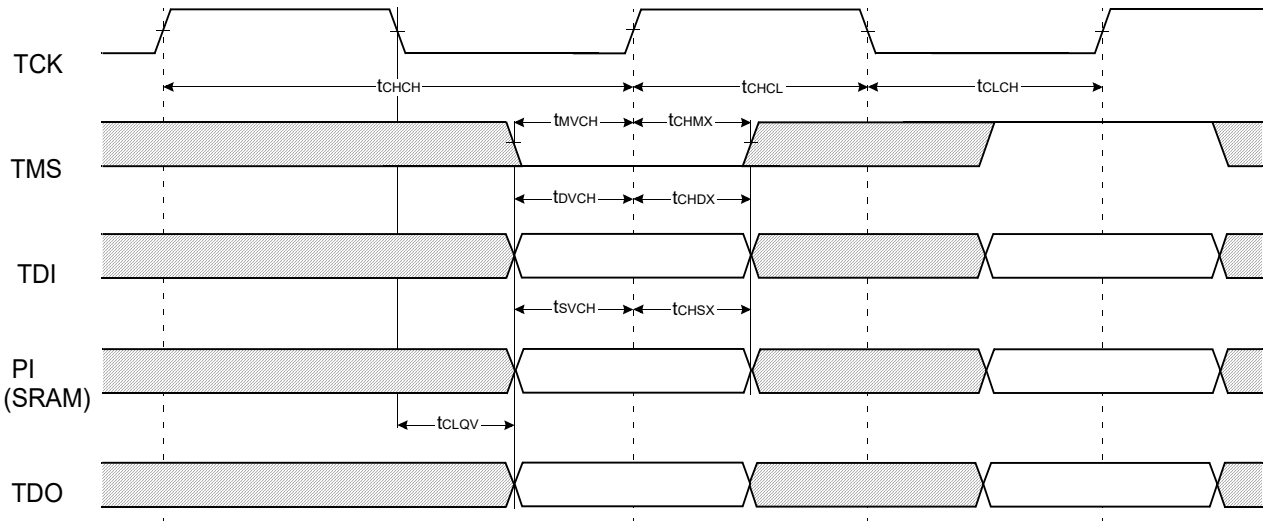
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.8/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	1

Note: 1. See SRAM AC test output load on page 11.

JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

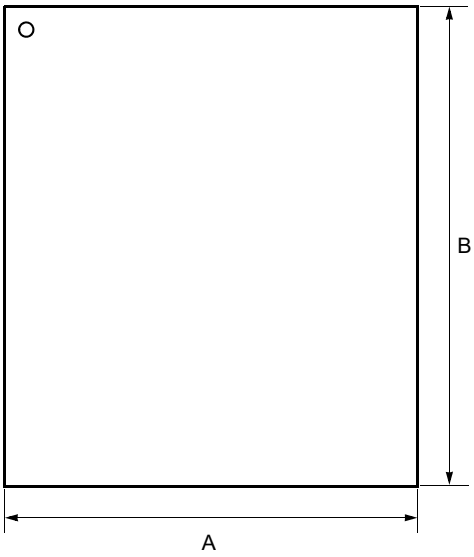
JTAG Timing Diagram



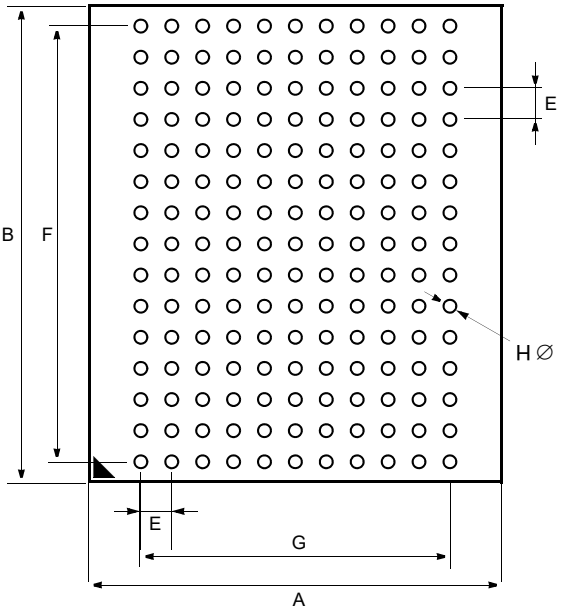
165 FBGA Package Dimensions - Lead & Lead Free

13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Grid Array

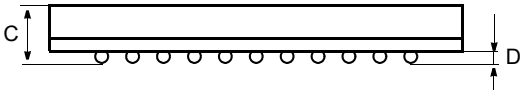
Top View



Bottom View



Side View



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	13 ± 0.1	mm		**E**	1.0	mm	
B	15 ± 0.1	mm		**F**	14.0	mm	
C	1.3 ± 0.1	mm		**G**	10.0	mm	
D	0.35 ± 0.05	mm		**H**	0.5 ± 0.05	mm	