S905

Datasheet

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Amlogic, Inc.

REVISION HISTORY

Revision Number	Revision Date	Changes
0.5	2015/7/18	Initial version release
1.0	2016/3/11	Add Information about crypto, video path, audio path, mermory interface, DDR, Nand, PLLs, JTAG, temperature sensor, Int 32K osc and PerfMon information
1.1.4	2016/6/1	Add SHA-2 hash functions (SHA-224/SHA-256) supported in 3.3

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Section I About This Documentation

1. Documentation Overview

This documentation is an overall Description of Amlogic advanced quad-core OTT/IP Set Top Box(STB) application processor S905, providing programmers instructions from the following aspects: system, video path, audio path, memory interfaces, I/O interfaces and system interfaces.

2. Acronyms and Abbreviations

Table I.2.1 Acronyms and Abbreviations

A		
AHB	AMBA High-speed Bus	A bus protocal designed for the connection and management of functional blocks in system-on-a-chip (SoC) designs
APB	Advanced Peripheral Bus	A bus protocal designed for low bandwidth control accesses
D		
DMAC	Direct Memory Access Controller	An engine connected to the DDR controller for the purposes of moving data to/from DDR memory.
DMC	DDR memory controller	An engine controls DDR
E		
eMMC	Embedded multimedia card	An architecture consisting of an embedded stortage solution with MMC interface, flash memory and controler
H		
HDMI	High-Definition Multimedian Interface	A compact audio/video interface used for transmitting uncompressed digital data
I		
I2C	Inter-Integrated Circuit	An multi-master, multi-slave, single-ended, serial computer bus used for attaching lower-speed peripheral ICs to processors and microcontrollers.
I2S	Inter IC sound	An electrical serial bus interface stand used for connnecting digital audio device together
P		
PCM	Pulse Code Modulation	A method used to digitally represent sampled analog signals
PDM	Pulse Density Modulation	A mothed used to represent an analog signal with digital signal
S		

SPI	Synchronous Peripheral Interface	A synchronous serial data link standard operating in sull duplex mode, devices communicate in master/slave mode where the master device initiates the date frame

Section II General Information

S905 is an advanced application processor designed for OTT/IP Set Top Box(STB), smart projector and high-end media box applications. It integrates a powerful CPU/GPU subsystem, and a secured UHD video CODEC engine with all major peripherals to form the ultimate low power multimedia AP.

The main system CPU is a quad-core ARM Cortex-A53 CPU with 32KB L1 instruction and 32KB data cache for each core and a large 512KB L2 unified cache to improve system performance. In addition, the Cortex-A53 CPU includes the NEON SIMD co-processor to improve software media processing capability. The quad-core ARM Cortex-A53 CPU can be overdriven to 2.0GHz and has a wide bus connecting to the memory sub-system.

The graphic subsystem consists of two graphic engines and a flexible video/graphic output pipeline. The five core ARM Mali-450 GPU including dual geometry processors (GP) and triple pixel processors (PP) handles all OpenGL ES 1.1/2.0 and OpenVG graphics programs, while the 2.5D graphics processor handles additional scaling, alpha, rotation and color space conversion operations. The video output pipeline can perform advanced video post-processing and enhancements. Together, the CPU and GPU handle all operating system, networking, user-interface and gaming related tasks.

Amlogic Video Engine (AVE) offloads the CPU by handling all video CODEC processing. It includes dedicated hardware video decoder and encoder. AVE is capable of decoding 4K2K resolution video at 60fps with complete Trusted Video Path (TVP) for secure applications and supports full formats including MVC, MPEG-1/2/4, VC-1/WMV, AVS, AVS+, RealVideo, MJPEG streams, H.264, H265-10 and also JPEG pictures with no size limitation. The independent encoder is able to encode in JPEG and H.264 up to 1080p at 60fps.

S905 integrates all standard audio/video input/output interfaces including a HDMI2.0 transmitter with 3D, CEC and HDCP 2.2 support, a CVBS output, I2S and SPDIF digital audio input/output interfaces, a PCM audio interface, two-channel PDM digital MIC inputs and dual DVP camera interfaces.

S905 also integrates a set of functional blocks for digital TV broadcasting streams. The built-in two demux can process the TV streams from the serial and parallel transport stream input interface, which can connect to external tuner/demodulator. An ISO7816 smart card interface and a crypto-processor are built in to help handling encrypted traffic and media streams.
The processor has rich advanced network and peripheral interfaces, including a Gigabit Ethernet MAC with RMII/RGMII interface, dual USB 2.0 high-speed ports (one OTG and one HOST) and multiple SDIO/SD card controllers, UART, I2C, high-speed SPI and PWMs.

Standard development environment utilizing GNU/GCC Android tool chain is supported. Please contact your AMLOGIC sales representative for more information.

3. Features

3.1 CPU Architecture

- Quad core ARM Cortex-A53 CPU up to 2.0GHz (DVFS)
- ARMv8-A architecture with Neon
- 8-stage in-order full dual issue pipeline
- 32KB instruction cache and 32KB data cache
- 512KB Unified L2 cache
- Advanced TrustZone security system
- Application based traffic optimization using internal QoS-based switching fabrics

3.2 GPU Architecture

- Penta-core ARM Mali-450 GPU up to 750MHz+ (DVFS)
- Dual Geometry Processors with 32KB L2 cache
- Triple Pixel Processors with 128KB L2 caches
- Concurrent multi-core processing
- 2250Mpix/sec and 165Mtri/sec
- Full scene over-sampled 4X anti-aliasing engine with no additional bandwidth usage
- OpenGL ES 1.1/2.0 and OpenVG 1.1 support
- Fast bitblt engine with dual inputs and single output
- Programmable raster operations (ROP)
- Programmable polyphase scaling filter
- Supports multiple video formats 4:2:0, 4:2:2 and 4:4:4 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Fast color space conversion
- Advanced anti-flickering filter

3.3 Crypto Engine

- AES block cipher with 128/192/256 bits keys, standard 16 bytes block size and streaming ECB, CBC and CTR modes
- DES/TDES block cipher with ECB and CBC modes supporting 64 bits key for DES and 192 bits key for 3DES
- Hardware key-ladder operation and DVB-CSA for transport stream encryption
- Built-in hardware True Random Number Generator (TRNG), CRC and SHA-1/SHA-2 (SHA-224/SHA-256) engine

3.4 Video Path

- Amlogic Video Engine (AVE) with dedicated hardware decoders and encoders
- Supports multiple "secured" video decoding sessions and simultaneous decoding and encoding
- Video/Picture Decoding
  - H.265 HEVC MP-10@L5.1 up to 4Kx2K@60fps
  - H.264 AVC HP@L5.1 up to 4Kx2K@30fps
  - H.264 MVC up to 1080p @60fps
  - MPEG-4 ASP@L5 up to 1080P@60fps (ISO-14496)
  - WMV/VC-1 SP/MP/AP up to 1080P@60fps
  - AVS-P16(AVS+) /AVS-P2 JiZhun Profile up to 1080P@60fps
  - MPEG-2 MP/HL up to 1080P@60fps (ISO-13818)
  - MPEG-1 MP/HL up to 1080P@60fps (ISO-11172)
  - RealVideo 8/9/10 up to 1080P
  - WebM up to VGA
  - Multiple language and multiple format sub-title video support
  - MJPEG and JPEG unlimited pixel resolution decoding (ISO/IEC-10918)
  - Supports JPEG thumbnail, scaling, rotation and transition effects
  - Supports *.mkv,*.wmv,*.mpg, *.mpeg, *.dat, *.avi, *.mov, *.iso, *.mp4, *.rm and *.jpg file formats

- Video/Picture Encoding
  - Independent JPEG and H.264 encoder with configurable performance/bits-rate
  - JPEG image encoding
  - H.264 video encoding up to 1080P@60fps with low latency
- Built-in HDMI 2.0 transmitter including both controller and PHY with CEC and HDCP 2,2, 4Kx2K@60 max resolution output
- CVBS 480i/576i standard definition output
- Supports all standard SD/HD/FHD video output formats: 480i/p, 576i/p, 720p, 1080i/p and 4Kx2K

3.5 Audio Path

- Supports MP3, AAC, WMA, RM, FLAC, Ogg and programmable with 7.1/5.1 down-mixing
- I2S audio interface supporting 8-channel (7.1) input and output
- Built-in serial digital audio SPDIF/IEC958 output and PCM input/output
- Dual-channel digital microphone PDM input
- Supports concurrent dual audio stereo channel output with combination of I2S+PCM

3.6 Memory

- 16/32-bit SDRAM memory interface running up to DDR2133
- Supports up to 2GB DDR3, DDR3L, LPDDR2, LPDDR3 with dual ranks
- Supports SLC/MLC/TLC NAND Flash with 60-bit ECC, compatible to Toshiba toggle mode in addition to ONFI 2.2
- SDSC/SDHC/SDXC card and SDIO interface with 1-bit and 4-bit data bus width supporting spec version 2.x/3.x/4.x DS/HS modes up to UHS-I SDR104
- eMMC and MMC card interface with 1/4/8-bit data bus width fully supporting spec version 5.0 HS400
- Supports serial 1, 2 or 4-bit NOR Flash via SPI interface
- Built-in 4k bits One-Time-Programming memory for key storage

3.7 I/O Interfaces

- Network
  - ıntegrated IEEE 802.3 10/100/1000 Gigabit Ethernet controller with RMII/RGMII interface
  - Supports Energy Efficiency Ethernet (EEE) mode
  - Optional 50MHz and 125MHz clock output to Ethernet PHY
  - WiFi/IEEE802.11 & Bluetooth supporting via SDIO/USB/UART/PCM
  - Network interface optimized for mixed WIFI and BT traffic
- Digital Television Interface
  - Transport stream (TS) input interface with built-in demux processor for connecting to external digital TV tuner/demodulator
  - Built-in PWM, I2C and SPI interfaces to control tuner and demodulator
  - Integrated ISO 7816 smart card controller
- Integrated I/O Controllers and Interfaces
  - Dual USB 2.0 high-speed USB I/O, one USB Host and one USB OTG
  - Multiple UART, I2C and SPI interface with slave select
  - Multiple PWMs
  - Programmable IR remote input/output controllers
  - Built-in 10bit SAR ADC with 2 input channels
  - A set of General Purpose IOs with built-in pull up and pull down

3.8 System Interface

- Integrated general purpose timers, counters, DMA controllers
- 24 MHz crystal input and internal 32KHz oscillator
- Embedded debug interface using ICE/JTAG

3.9 Power Management

- Multiple external power domains controlled by PMIC
- Multiple internal power domains controlled by software
- Multiple sleep modes for CPU, system, DRAM, etc.
- Multiple internal PLLs for DVFS operation
- Multi-voltage I/O design for 1.8V and 3.3V
- Power management auxiliary processor in a dedicated always-on (AO) power domain that can communicate with an external PMIC

3.10 Security

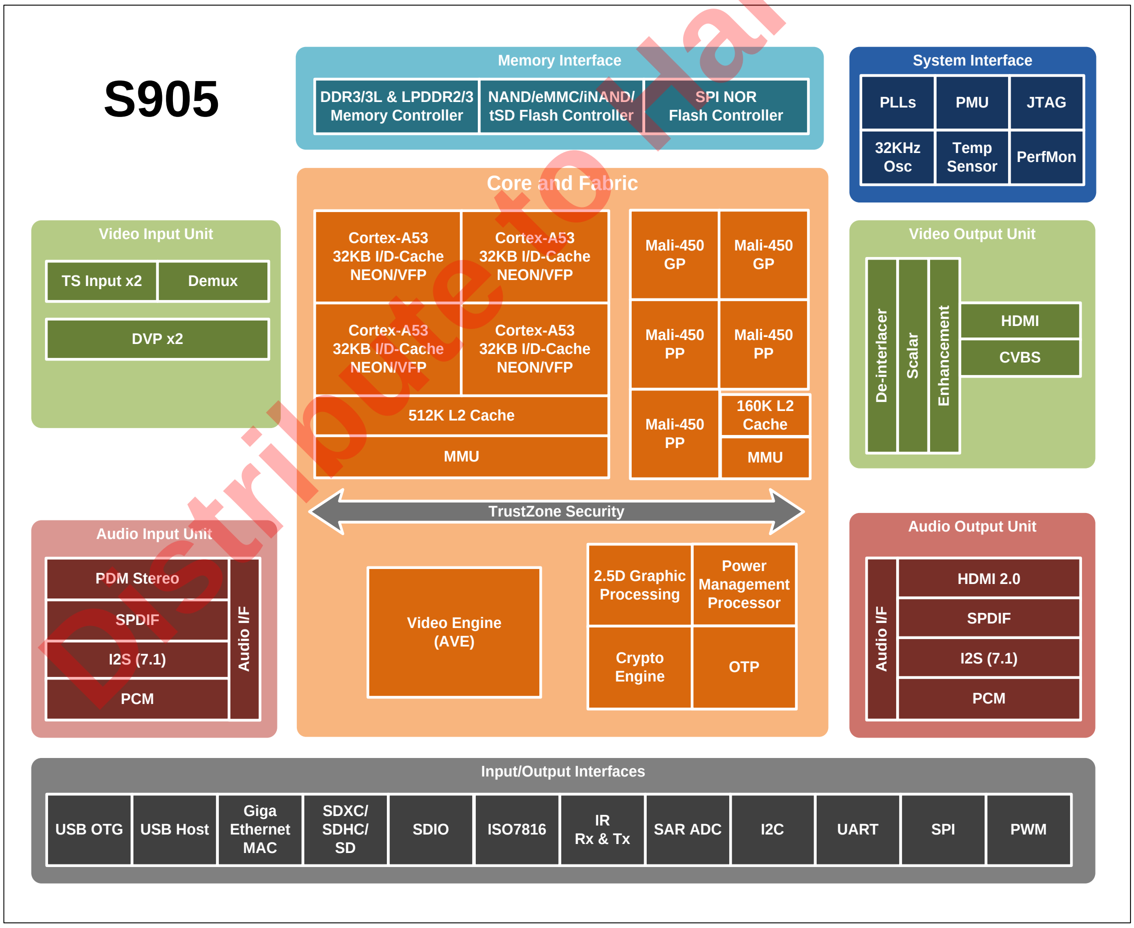
- Trustzone based Trusted Execution Environment (TEE)
- Secured boot, obfuscated OTP, internal control buses and storage
- Protected memory regions and electric fence data partition
- Hardware based Trusted Video Path (TVP) and secured contents (needs SecureOS software)

4. System Block Diagram

Fig II.4.1 shows the structure of S905.

Fig II.4.1 Block Diagram of S905

ADVANCED CONNECTED MULTIMEDIA PROCESSOR



5. Pin-Out Diagram (Top view)

Below is the pin-out diagram of S905.

FigII.5.1 S905 Pin-out Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	GPIOY_12	GPIOY_9	GPIOY_6	GPIOY_5	GPIOY_1	BOOT_15	BOOT_11	BOOT_7	BOOT_5	BOOT_2	sys_osc_in	OSC_BUF_OUT	USBA_ID	USBB_DP	USB_TXRTUNE	CVBS_COMP	HDMITX_2P	HDMITX_2N	HDMITX_1P	A
B	GPIOY_13	GPIOY_10	GPIOY_7	GPIOY_4	GPIOY_0	BOOT_14	BOOT_10	BOOT_6	BOOT_4	BOOT_1	sys_osc_out	EXTC_DPLL	USBA_VBUS	USBB_DM	CVBS_IOUT	CVBS_VREF	GPIOH_3	HDMITX_AVSS	HDMITX_1N	B
C	GPIOY_14	GPIOY_11	GPIOY_8	GPIOY_3	.	BOOT_13	BOOT_9	.	BOOT_3	BOOT_0	GPIOCLK_0	.	USBA_DP	USBA_DM	.	CVBS_RSET	GPIOH_2	HDMITX_0P	.	C
D	GPIOX_2	GPIOY_15	GPIOY_16	GPIOY_2	VDDIO_Y	BOOT_12	VDDIO_BOOT	BOOT_8	IOVREF_1p8v	GPIOCLK_1	SARADC_CH1	SARADC_CH0	AVDD18_USB_ADC	AVDD18_CVBS_EFUSE	GPIOH_0	GPIOH_1	HDMI_REXT	HDMITX_0N	HDMITX_CKP	D
E	GPIOX_4	GPIOX_3	.	VDDIO_X	VDDCPU	VDDCPU	VDDCPU	VDDCPU	VDDCPU	VDDEE_0V9	VDD18_XTAL_CLK	AVDD18_DPLL	VDDEE_0V9	USB33_VDDIOH	HDMITX_AVDD33	HDMI_AVDD18	.	HDMITX_AVSS	HDMITX_CKN	E
F	GPIOX_6	GPIOX_5	GPIOX_1	GPIOX_0	VDDCPU	DVSS	DVSS	DVSS	DVSS	DVSS	AVSS_DPLL	CVBS_AVSS	DVSS	HDMITX_VDD0P9	HDMITX_AVSS	HDMI_AVDD18	HPLL_CEXT	GPIOZ_15	HDMI_CEXT	F
G	GPIOX_9	GPIOX_8	GPIOX_7	VDDCPU	.	DVSS	.	VDDCPU	DVSS	.	DVSS	DVSS	.	DVSS	HDMITX_AVSS	HDMITX_AVDD33	HPLL_AVDD18	GPIOZ_14	GPIOZ_13	G
H	GPIOX_12	GPIOX_11	.	GPIOX_10	VDDCPU	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	VDDEE_0V9	DVSS	HPLL_AVSS	GPIOZ_12	.	GPIOZ_11	GPIOZ_10	H
J	GPIOX_19	GPIOX_15	GPIOX_14	GPIOX_13	VDDCPU	DVSS	VDDCPU	DVSS	DVSS	DVSS	DVSS	.	DVSS	DVSS	VDDEE_0V9	GPIOZ_6	GPIOZ_7	GPIOZ_9	GPIOZ_8	J
K	GPIOX_21	CKE0	GPIOX_20	VDDEE_0V9	DVSS	DVSS	DVSS	.	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	VDDEE_0V9	GPIOZ_4	GPIOZ_5	CARD_1	CARD_0	K
L	CKE1	A10	BA1	A4	DVSS	VDDEE_0V9	DVSS	DVSS	DVSS	DVSS	DVSS	VDDEE_0V9	DVSS	DVSS	VDDIO_Z	GPIOZ_1	GPIOZ_2	CARD_3	CARD_2	L
M	A15	A8	.	VDDQ	DVSS	DVSS	.	VDDEE_0V9	DVSS	.	DVSS	DVSS	.	DVSS	VDDIO_CARD	GPIOZ_3	.	CARD_5	CARD_4	M
N	DVSS	A6	A11	A14	VDDQ	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	VDDEE_0V9	GPIOZ_0	GPIODV_29	GPIODV_28	CARD_6	N
P	A1	A12	BA2	A0	.	DVSS	VDDEE_0V9	PLL_VDD	VDDQ	VDDQ	VDDEE_0V9	VDDAO_0V9	VDDIO_AO	VDDEE_0V9	VDDIO_DV	GPIODV_24	GPIODV_25	GPIODV_27	GPIODV_26	P
R	A2	A9	.	BA0	WE_N	VDDQ	VDDQ	DQ3	DQ1	VDDQ	DQ18	DQS2_P	DQ19	VDDQ	RESET_N	GPIOAO_2	.	GPIOAO_0	GPIOAO_1	R
T	A13	A7	CS1_N	RAS_N	DQ6	DQ2	DQS0_N	DQM0	DQ5	DQ22	DQ16	DQS2_N	DQ17	DQ21	TEST_N	GPIOAO_12	GPIOAO_4	GPIOAO_3	GPIOAO_7	T
U	DVSS	A5	CS0_N	DDR_RST	DQ4	.	DQS0_P	DQ7	DVSS	DQ20	.	DQM2	.	DQ23	DVSS	GPIOAO_13	GPIOAO_5	GPIOAO_6	GPIOAO_8	U
V	A3	ODT0	PZQ	CLKN	DQ0	DVSS	DQ15	DQM1	DQS1_N	DQ14	DQ8	DQ27	DQ31	DQM3	DQS3_N	DQ28	DQ30	GPIOAO_10	GPIOAO_9	V
W	CAS_N	ODT1	PVREF	CLKP	DQ11	DQ13	DQ9	DQS1_P	.	DQ12	DQ10	DQ29	DVSS	DQ25	DQS3_P	DVSS	DQ26	DQ24	GPIOAO_11	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

6. Pin Description

Table II.6.1 gives the pin Description of S905.

Table II.6.1 Pin Description

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
GPIOX - Refer to Table II.7.1 for functional multiplex information.						
F4	GPIOX_0	DIO_4mA	UP	General purpose input/output bank X signal 0	VDDIO_X	-
F3	GPIOX_1	DIO_4mA	UP	General purpose input/output bank X signal 1	VDDIO_X	-
D1	GPIOX_2	DIO_4mA	UP	General purpose input/output bank X signal 2	VDDIO_X	-
E2	GPIOX_3	DIO_4mA	UP	General purpose input/output bank X signal 3	VDDIO_X	-
E1	GPIOX_4	DIO_4mA	UP	General purpose input/output bank X signal 4	VDDIO_X	-
F2	GPIOX_5	DIO_4mA	UP	General purpose input/output bank X signal 5	VDDIO_X	-
F1	GPIOX_6	DIO_3mA	DOWN	General purpose input/output bank X signal 6	VDDIO_X	-
G3	GPIOX_7	DIO_3mA	UP	General purpose input/output bank X signal 7	VDDIO_X	-
G2	GPIOX_8	DIO_3mA	UP	General purpose input/output bank X signal 8	VDDIO_X	-
G1	GPIOX_9	DIO_3mA	UP	General purpose input/output bank X signal 9	VDDIO_X	-
H4	GPIOX_10	DIO_3mA	UP	General purpose input/output bank X signal 10	VDDIO_X	-
H2	GPIOX_11	DIO_3mA	UP	General purpose input/output bank X signal 11	VDDIO_X	-
H1	GPIOX_12	DIO_3mA	UP	General purpose input/output bank X signal 12	VDDIO_X	-
J4	GPIOX_13	DIO_3mA	UP	General purpose input/output bank X signal 13	VDDIO_X	-
J3	GPIOX_14	DIO_3mA	UP	General purpose input/output bank X signal 14	VDDIO_X	-
J2	GPIOX_15	DIO_3mA	UP	General purpose input/output bank X signal 15	VDDIO_X	-
J1	GPIOX_19	DIO_3mA	UP	General purpose input/output bank X signal 19	VDDIO_X	-
K3	GPIOX_20	DIO_3mA	DOWN	General purpose input/output bank X signal 20	VDDIO_X	-
K1	GPIOX_21	DIO_3mA	Up	General purpose input/output bank X signal 21	VDDIO_X	-
E4	VDDIO_X	P	-	Power supply for GPIO bank X	-	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
GPIOY - Refer to Table II.7.2 for functional multiplex information.						
B5	GPIOY_0	DIO_3mA	UP	General purpose input/output bank Y signal 0	VDDIO_Y	-
A5	GPIOY_1	DIO_3mA	UP	General purpose input/output bank Y signal 1	VDDIO_Y	-
D4	GPIOY_2	DIO_3mA	UP	General purpose input/output bank Y signal 2	VDDIO_Y	-
C4	GPIOY_3	DIO_3mA	UP	General purpose input/output bank Y signal 3	VDDIO_Y	-
B4	GPIOY_4	DIO_3mA	UP	General purpose input/output bank Y signal 4	VDDIO_Y	-
A4	GPIOY_5	DIO_3mA	UP	General purpose input/output bank Y signal 5	VDDIO_Y	-
A3	GPIOY_6	DIO_3mA	UP	General purpose input/output bank Y signal 6	VDDIO_Y	-
B3	GPIOY_7	DIO_3mA	UP	General purpose input/output bank Y signal 7	VDDIO_Y	-
C3	GPIOY_8	DIO_3mA	UP	General purpose input/output bank Y signal 8	VDDIO_Y	-
A2	GPIOY_9	DIO_3mA	UP	General purpose input/output bank Y signal 9	VDDIO_Y	-
B2	GPIOY_10	DIO_3mA	UP	General purpose input/output bank Y signal 10	VDDIO_Y	-
C2	GPIOY_11	DIO_3mA	UP	General purpose input/output bank Y signal 11	VDDIO_Y	-
A1	GPIOY_12	DIO_3mA	UP	General purpose input/output bank Y signal 12	VDDIO_Y	-
B1	GPIOY_13	DIO_3mA	UP	General purpose input/output bank Y signal 13	VDDIO_Y	-
C1	GPIOY_14	DIO_3mA	DOWN	General purpose input/output bank Y signal 14	VDDIO_Y	-
D2	GPIOY_15	DIO_3mA	DOWN	General purpose input/output bank Y signal 15	VDDIO_Y	-
D3	GPIOY_16	DIO_3mA	DOWN	General purpose input/output bank Y signal 16	VDDIO_Y	-
D5	VDDIO_Y	P	-	Power supply for GPIO bank Y	-	-
GPIODV - Refer to Table II.7.3 for functional multiplex information.						
P16	GPIODV_24	DIO_3mA	Z	General purpose input/output bank DV signal 24	GPIO_DV	-
P17	GPIODV_25	DIO_3mA	Z	General purpose input/output bank DV signal 25	GPIO_DV	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
P19	GPIODV_26	DIO_4mA	Z	General purpose input/output bank DV signal 26	GPIO_DV	-
P18	GPIODV_27	DIO_3mA	Z	General purpose input/output bank DV signal 27	GPIO_DV	-
N18	GPIODV_28	DIO_3mA	Z	General purpose input/output bank DV signal 28	GPIO_DV	-
N17	GPIODV_29	DIO_3mA	Z	General purpose input/output bank DV signal 29	GPIO_DV	-
P15	VDDIO_DV	P	-	Power supply for GPIO bank DV	-	-
CARD - Refer to Table II.7.4 for functional multiplex information.						
K19	CARD_0	DIO_4mA	UP	General purpose input/output bank CARD signal 0	VDDIO_CARD	-
K18	CARD_1	DIO_4mA	UP	General purpose input/output bank CARD signal 1	VDDIO_CARD	-
L19	CARD_2	DIO_4mA	UP	General purpose input/output bank CARD signal 2	VDDIO_CARD	-
L18	CARD_3	DIO_4mA	UP	General purpose input/output bank CARD signal 3	VDDIO_CARD	-
M19	CARD_4	DIO_4mA	UP	General purpose input/output bank CARD signal 4	VDDIO_CARD	-
M18	CARD_5	DIO_4mA	UP	General purpose input/output bank CARD signal 5	VDDIO_CARD	-
N19	CARD_6	DIO_2mA	UP	General purpose input/output bank CARD signal 6	VDDIO_CARD	-
M15	VDDIO_CARD	P	-	Power supply for GPIO bank CARD	-	-
BOOT - Refer to Table II.7.5 for functional multiplex information.						
C10	BOOT_0	DIO_4mA	UP	General purpose input/output bank BOOT signal 0	VDDIO_BOOT	-
B10	BOOT_1	DIO_4mA	UP	General purpose input/output bank BOOT signal 1	VDDIO_BOOT	-
A10	BOOT_2	DIO_4mA	UP	General purpose input/output bank BOOT signal 2	VDDIO_BOOT	-
C9	BOOT_3	DIO_4mA	UP	General purpose input/output bank BOOT signal 3	VDDIO_BOOT	-
B9	BOOT_4	DIO_4mA	UP	General purpose input/output bank BOOT signal 4	VDDIO_BOOT	-
A9	BOOT_5	DIO_4mA	UP	General purpose input/output bank BOOT signal 5	VDDIO_BOOT	-
B8	BOOT_6	DIO_4mA	UP	General purpose input/output bank BOOT signal 6	VDDIO_BOOT	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
A8	BOOT_7	DIO_4mA	UP	General purpose input/output bank BOOT signal 7	VDDIO_BOOT	-
D8	BOOT_8	DIO_4mA	UP	General purpose input/output bank BOOT signal 8	VDDIO_BOOT	-
C7	BOOT_9	DIO_4mA	UP	General purpose input/output bank BOOT signal 9	VDDIO_BOOT	-
B7	BOOT_10	DIO_4mA	UP	General purpose input/output bank BOOT signal 10	VDDIO_BOOT	-
A7	BOOT_11	DIO_4mA	UP	General purpose input/output bank BOOT signal 11	VDDIO_BOOT	-
D6	BOOT_12	DIO_4mA	UP	General purpose input/output bank BOOT signal 12	VDDIO_BOOT	-
C6	BOOT_13	DIO_4mA	UP	General purpose input/output bank BOOT signal 13	VDDIO_BOOT	-
B6	BOOT_14	DIO_4mA	UP	General purpose input/output bank BOOT signal 14	VDDIO_BOOT	-
A6	BOOT_15	DIO_4mA	UP	General purpose input/output bank BOOT signal 15	VDDIO_BOOT	-
D7	VDDIO_BOOT	P	-	Power supply for GPIO bank BOOT	-	-
GPIOH - Refer to Table II.7.6 for functional multiplex information.						
D15	GPIOH_0	DIO_OD	Z	General purpose input/output bank H signal 0	USB33_VDDIOH	-
D16	GPIOH_1	DIO_OD	Z	General purpose input/output bank H signal 1	USB33_VDDIOH	-
C17	GPIOH_2	DIO_OD	Z	General purpose input/output bank H signal 2	USB33_VDDIOH	-
B17	GPIOH_3	DIO_2mA	DOWN	General purpose input/output bank H signal 3	USB33_VDDIOH	-
E14	USB33_VDDIOH	P	-	Power supply for GPIO bank H and USB	-	-
GPIOZ - Refer to Table II.7.7 for functional multiplex information.						
N16	GPIOZ_0	DIO_4mA	UP	General purpose input/output bank H signal 0	VDDIO_Z	-
L16	GPIOZ_1	DIO_4mA	UP	General purpose input/output bank H signal 1	VDDIO_Z	-
L17	GPIOZ_2	DIO_4mA	UP	General purpose input/output bank H signal 2	VDDIO_Z	-
M16	GPIOZ_3	DIO_4mA	UP	General purpose input/output bank H signal 3	VDDIO_Z	-
K16	GPIOZ_4	DIO_4mA	UP	General purpose input/output bank H signal 4	VDDIO_Z	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
K17	GPIOZ_5	DIO_4mA	UP	General purpose input/output bank H signal 5	VDDIO_Z	-
J16	GPIOZ_6	DIO_4mA	UP	General purpose input/output bank H signal 6	VDDIO_Z	-
J17	GPIOZ_7	DIO_4mA	UP	General purpose input/output bank H signal 7	VDDIO_Z	-
J19	GPIOZ_8	DIO_4mA	UP	General purpose input/output bank H signal 8	VDDIO_Z	-
J18	GPIOZ_9	DIO_4mA	UP	General purpose input/output bank H signal 9	VDDIO_Z	-
H19	GPIOZ_10	DIO_4mA	UP	General purpose input/output bank H signal 10	VDDIO_Z	-
H18	GPIOZ_11	DIO_4mA	UP	General purpose input/output bank H signal 11	VDDIO_Z	-
H16	GPIOZ_12	DIO_4mA	UP	General purpose input/output bank H signal 12	VDDIO_Z	-
G19	GPIOZ_13	DIO_4mA	UP	General purpose input/output bank H signal 13	VDDIO_Z	-
G18	GPIOZ_14	DIO_4mA	DOWN	General purpose input/output bank H signal 14	VDDIO_Z	-
F18	GPIOZ_15	DIO_4mA	UP	General purpose input/output bank H signal 15	VDDIO_Z	-
L15	VDDIO_Z	P	-	Power supply for GPIO bank Z	-	-
GPIOAO - Refer to Table II.7.8 for functional multiplex information.						
R18	GPIOAO_0	DIO_2mA	UP	General purpose input/output bank AO signal 0	VDDIO_AO	-
R19	GPIOAO_1	DIO_2mA	UP	General purpose input/output bank AO signal 1	VDDIO_AO	-
R16	GPIOAO_2	DIO_2mA	UP	General purpose input/output bank AO signal 2	VDDIO_AO	-
T18	GPIOAO_3	DIO_2mA	UP	General purpose input/output bank AO signal 3	VDDIO_AO	-
T17	GPIOAO_4	DIO_2mA	UP	General purpose input/output bank AO signal 4	VDDIO_AO	-
U17	GPIOAO_5	DIO_2mA	UP	General purpose input/output bank AO signal 5	VDDIO_AO	-
U18	GPIOAO_6	DIO_2mA	UP	General purpose input/output bank AO signal 6	VDDIO_AO	-
T19	GPIOAO_7	DIO_2mA	UP	General purpose input/output bank AO signal 7	VDDIO_AO	-
U19	GPIOAO_8	DIO_2mA	UP	General purpose input/output bank AO signal 8	VDDIO_AO	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
V19	GPIOAO_9	DIO_2mA	UP	General purpose input/output bank AO signal 9	VDDIO_AO	-
V18	GPIOAO_10	DIO_2mA	UP	General purpose input/output bank AO signal 10	VDDIO_AO	-
W19	GPIOAO_11	DIO_2mA	UP	General purpose input/output bank AO signal 11	VDDIO_AO	-
T16	GPIOAO_12	DIO_OD	Z	General purpose input/output bank AO signal 12	VDDIO_AO	-
U16	GPIOAO_13	DIO_3mA	UP	General purpose input/output bank AO signal 13	VDDIO_AO	-
T15	TEST_N	DIO_2mA	Up	General purpose input/output bank AO signal 14. Should be pulled up during normal operation.	VDDIO_AO	-
R15	RESET_N	DI	DOWN	System reset input	VDDIO_AO	-
P13	VDDIO_AO	P	-	Power supply for GPIO bank AO	-	-
GPIOCLK - Refer to Table II.7.9 for functional multiplex information.						
C11	GPIOCLK_0	DIO_3mA	UP	General purpose input/output bank CLK signal 0	VDD18_XTAL_CLK	-
D10	GPIOCLK_1	DIO_3mA	UP	General purpose input/output bank CLK signal 1	VDD18_XTAL_CLK	-
E11	VDD18_XTAL_CLK	P	-	Power supply for GPIO bank CLK and crystal	-	-
SARADC						
D11	SARADC_CH0	AI	-	ADC channel 0 input	AVDD18_USB_ADC	-
D12	SARADC_CH1	AI	-	ADC channel 1 input	AVDD18_USB_ADC	-
A12	OSC_BUF_OUT	AO	-	Buffered 24MHz XTAL output	AVDD18_USB_ADC	-
D13	AVDD18_USB_ADC	AP	-	Analog power supply for SARADC and USB	-	-
CVBS						
A16	CVBS_COMP	A	-	CVBS external compensation capacitor connection	AVDD18_CVBS_EFUSE	NC
C16	CVBS_RSET	A	-	CVBS output strength setting resistor	AVDD18_CVBS_EFUSE	NC
B16	CVBS_VREF	A	-	CVBS reference voltage filter cap	AVDD18_CVBS_EFUSE	NC
B15	CVBS_IOUT	AO	-	CVBS output	AVDD18_CVBS_EFUSE	NC

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
D14	AVDD18_CVBS_EFUSE	P	-	Analog power supply for CVBS and eFuse	-	To 1.8V
F12	CVBS_AVSS	P	-	Analog power ground for CVBS	-	To VSS
HDMI						
C18	HDMITX_0P	AO	-	HDMI TMDS data0 positive output	HDMITX_AVDD33	NC
D18	HDMITX_0N	AO	-	HDMI TMDS data0 negative output	HDMITX_AVDD33	NC
A19	HDMITX_1P	AO	-	HDMI TMDS data1 positive output	HDMITX_AVDD33	NC
B19	HDMITX_1N	AO	-	HDMI TMDS data1 negative output	HDMITX_AVDD33	NC
A17	HDMITX_2P	AO	-	HDMI TMDS data1 positive output	HDMITX_AVDD33	NC
A18	HDMITX_2N	AO	-	HDMI TMDS data1 negative output	HDMITX_AVDD33	NC
D19	HDMITX_CKP	AO	-	HDMI TMDS clock positive output	HDMITX_AVDD33	NC
E19	HDMITX_CKN	AO	-	HDMI TMDS clock negative output	HDMITX_AVDD33	NC
D17	HDMI_REXT	A	-	HDMI output strength setting resistor	HDMI_AVDD18	NC
F19	HDMI_CEXT	A	-	HDMI TX external filter cap	HDMI_AVDD18	NC
G16,E15	HDMITX_AVDD33	P	-	Analog power supply 3.3V for HDMI	-	To 3.3V
E16,F16	HDMITX_AVDD18	P	-	Analog power supply 1.8V for HDMI	-	To 1.8V
F14	HDMITX_VDD0P9	P	-	Power supply 0.9V for HDMI	-	To 0.9V
B18,E18,F15,G15	HDMITX_AVSS	P	-	Analog power ground for HDMI	-	To VSS
DRAM						
P4	A0	DO	-	DRAM address bus bit 0	VDDQ	-
P1	A1	DO	-	DRAM address bus bit 1	VDDQ	-
R1	A2	DO	-	DRAM address bus bit 2	VDDQ	-
V1	A3	DO	-	DRAM address bus bit 3	VDDQ	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
L4	A4	DO	-	DRAM address bus bit 4	VDDQ	-
U2	A5	DO	-	DRAM address bus bit 5	VDDQ	-
N2	A6	DO	-	DRAM address bus bit 6	VDDQ	-
T2	A7	DO	-	DRAM address bus bit 7	VDDQ	-
M2	A8	DO	-	DRAM address bus bit 8	VDDQ	-
R2	A9	DO	-	DRAM address bus bit 9	VDDQ	-
L2	A10	DO	-	DRAM address bus bit 10	VDDQ	-
N3	A11	DO	-	DRAM address bus bit 11	VDDQ	-
P2	A12	DO	-	DRAM address bus bit 12	VDDQ	-
T1	A13	DO	-	DRAM address bus bit 13	VDDQ	-
N4	A14	DO	-	DRAM address bus bit 14	VDDQ	-
M1	A15	DO	-	DRAM address bus bit 15	VDDQ	-
R4	BA_0	DO	-	DRAM bank address bus bit 0	VDDQ	-
L3	BA_1	DO	-	DRAM bank address bus bit 1	VDDQ	-
P3	BA_2	DO	-	DRAM bank address bus bit 2	VDDQ	-
W1	CAS_N	DO	-	DRAM column address strobe	VDDQ	-
W4	CLKP	DO	-	DRAM clock positive output	VDDQ	-
V4	CLKN	DO	-	DRAM clock negative output	VDDQ	-
K2	CKE0	DO	-	DRAM clock enable output 0	VDDQ	-
L1	CKE1	DO	-	DRAM clock enable output 1	VDDQ	-
U3	CS0_N	DO	-	DRAM chip select output 0	VDDQ	-
T3	CS1_N	DO	-	DRAM chip select output 1	VDDQ	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
V2	ODT0	DO	-	DRAM on-die termination 0	VDDQ	-
W2	ODT1	DO	-	DRAM on-die termination 1	VDDQ	-
T4	RAS_N	DO	-	DRAM row address strobe	VDDQ	-
R5	WE_N	DO	-	DRAM write enable	VDDQ	-
U4	DDR_RST	DO	-	DRAM reset	VDDQ	-
V5	DQ0	DIO	-	DRAM data bus bit 0	VDDQ	-
R9	DQ1	DIO	-	DRAM data bus bit 1	VDDQ	-
T6	DQ2	DIO	-	DRAM data bus bit 2	VDDQ	-
R8	DQ3	DIO	-	DRAM data bus bit 3	VDDQ	-
U5	DQ4	DIO	-	DRAM data bus bit 4	VDDQ	-
T9	DQ5	DIO	-	DRAM data bus bit 5	VDDQ	-
T5	DQ6	DIO	-	DRAM data bus bit 6	VDDQ	-
U8	DQ7	DIO	-	DRAM data bus bit 7	VDDQ	-
V11	DQ8	DIO	-	DRAM data bus bit 8	VDDQ	-
W7	DQ9	DIO	-	DRAM data bus bit 9	VDDQ	-
W11	DQ10	DIO	-	DRAM data bus bit 10	VDDQ	-
W5	DQ11	DIO	-	DRAM data bus bit 11	VDDQ	-
W10	DQ12	DIO	-	DRAM data bus bit 12	VDDQ	-
W6	DQ13	DIO	-	DRAM data bus bit 13	VDDQ	-
V10	DQ14	DIO	-	DRAM data bus bit 14	VDDQ	-
V7	DQ15	DIO	-	DRAM data bus bit 15	VDDQ	-
T11	DQ16	DIO	-	DRAM data bus bit 16	VDDQ	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
T13	DQ17	DIO	-	DRAM data bus bit 17	VDDQ	-
R11	DQ18	DIO	-	DRAM data bus bit 18	VDDQ	-
R13	DQ19	DIO	-	DRAM data bus bit 19	VDDQ	-
U10	DQ20	DIO	-	DRAM data bus bit 20	VDDQ	-
T14	DQ21	DIO	-	DRAM data bus bit 21	VDDQ	-
T10	DQ22	DIO	-	DRAM data bus bit 22	VDDQ	-
U14	DQ23	DIO	-	DRAM data bus bit 23	VDDQ	-
W18	DQ24	DIO	-	DRAM data bus bit 24	VDDQ	-
W14	DQ25	DIO	-	DRAM data bus bit 25	VDDQ	-
W17	DQ26	DIO	-	DRAM data bus bit 26	VDDQ	-
V12	DQ27	DIO	-	DRAM data bus bit 27	VDDQ	-
V16	DQ28	DIO	-	DRAM data bus bit 28	VDDQ	-
W12	DQ29	DIO	-	DRAM data bus bit 29	VDDQ	-
V17	DQ30	DIO	-	DRAM data bus bit 30	VDDQ	-
V13	DQ31	DIO	-	DRAM data bus bit 31	VDDQ	-
T8	DQM0	DO	-	DRAM data mask 0	VDDQ	-
V8	DQM1	DO	-	DRAM data mask 1	VDDQ	-
U12	DQM2	DO	-	DRAM data mask 2	VDDQ	-
V14	DQM3	DO	-	DRAM data mask 3	VDDQ	-
U7	DQS0_P	DIO	-	DRAM data strobe 0	VDDQ	-
T7	DQS0_N	DIO	-	DRAM data strobe 0 complementary	VDDQ	-
W8	DQS1_P	DIO	-	DRAM data strobe 1	VDDQ	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
V9	DQS1_N	DIO	-	DRAM data strobe 1 complementary	VDDQ	-
R12	DQS2_P	DIO	-	DRAM data strobe 2	VDDQ	-
T12	DQS2_N	DIO	-	DRAM data strobe 2 complementary	VDDQ	-
W15	DQS3_P	DIO	-	DRAM data strobe 3	VDDQ	-
V15	DQS3_N	DIO	-	DRAM data strobe 3 complementary	VDDQ	-
W3	PVREF	A	-	DRAM reference voltage	VDDQ	-
V3	PZQ	A	-	DRAM reference pin for ZQ calibration	VDDQ	-
USB						
C13	USBA_DP	AIO	-	USB OTG positive data signal	USB33_VDDIOH	NC
C14	USBA_DM	AIO	-	USB OTG negative data signal	USB33_VDDIOH	NC
B13	USBA_VBUS	AI	-	USB OTG cable power detection (5V tolerance)	AVDD18_USB_ADC	NC
A13	USBA_ID	DI	-	USB OTG mini-receptacle identifier (Internal 10KΩ pull-up resistor to AVDD18)	AVDD18_USB_ADC	NC
A14	USBB_DP	AIO	-	USB host positive data signal	USB33_VDDIOH	NC
B14	USBB_DM	AIO	-	USB host negative data signal	USB33_VDDIOH	NC
A15	USB_TXRTUNE	AIO	-	USB output strength setting resistor	AVDD18_USB_ADC	NC[1]
System Clock & PLL						
A11	sys_osc_in	AI	-	24MHz crystal oscillator input	VDD18_XTAL_CLK	-
B11	sys_osc_out	AO	-	24MHz crystal oscillator output	VDD18_XTAL_CLK	-
B12	EXTC_DPLL	A	-	DPLL external filter cap	AVDD18_DPLL	-
E12	AVDD18_DPLL	P	-	Analog power supply 1.8V for DPLL	-	-
F11	AVSS_DPLL	P	-	Analog power ground for DPLL	-	-
G17	HPLL_AVDD18	P	-	Analog 1.8V power supply for HPLL	-	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
H15	HPLL_AVSS	P	-	Analog power ground for HPLL	-	-
F17	HPLL_CEXT	A	-	HPLL external filter cap	HPLL_AVDD18	-
P8	PLL_VDD	P	-	Power supply for PLL	-	-
Digital Power						
J5,J7,E5,E6,E7,E8,E9,F5,G4,G8,H5	VDDCPU	P	-	Power supply for CPU (Cortex A5)	-	-
M4,N5,P9,P10,R6,R7,R10,R14	VDDQ	P	-	Power supply for DDR	-	-
H13,J15,K4,K15,E10,E13,L6,L12,M8,N15,P7,P11,P14	VDDEE_0V9	P	-	Power Supply for GPU and core logic	-	-
P12	VDDAO_0V9	P	-	Power supply 0.9V for AO domain	-	-
D9	IOVREF_1V8	P	-	1.8V Power supply for IOVREF	-	-
Digital Ground						
H9,H10,H11,H12,H14,J6,J8,J9,J10,J11,J13,J14,K5,K6,K7,K9,K10,K11,K12,K13,K14,U1,U9,L5,L7,L8,L9,L10,L11,L13,L14,M5,M6,M9,M11,M12,M14,N1,N6,N7,N8,N9,N10,N11,N12	DVSS	P	-	Digital power ground	-	-

Ball#	Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
,N13,U15,V6,F6,F7,F8,F9,F10,F13,G6,G9,G11,G12,G14,H6,H7,H8,N14,P6,W13,W16						

Note 1: USB_TXRTUNE can only be NC when both USBA/USBB are not used.

Abbreviations:

- DI = Digital input pin
- DO = Digital output pin
- DIO = Digital input/output pin
- DIO_OD = 5V input tolerant open drain (OD) output pin, need external pull up
- A = Analog setting or filtering pin
- AI = Analog input pin
- AO = Analog output pin
- AIO = Analog input/output pin
- P = Power pin
- AP = Analog power pin
- NC = No connection
- UP = Pull-Up
- DOWN = Pull-down
- Z = Tri-State

7. Pin Multiplexing

Multiple usage pins are used to conserve pin consumption for different features. The S905 devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be used as a GPIO pin as well.

Table II.7.1 GPIOX_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOX_0			SDIO_D0	
GPIOX_1			SDIO_D1	
GPIOX_2			SDIO_D2	
GPIOX_3			SDIO_D3	
GPIOX_4			SDIO_CLK	
GPIOX_5			SDIO_CMD	
GPIOX_6	TSIN_D_VALID_B	PWM_A		
GPIOX_7	TSIN_SOP_B	PWM_F	SDIO_IRQ	
GPIOX_8	TSIN_CLK_B		ISO7816_CLK	PCM_OUT_A
GPIOX_9	TSIN_D0_B		ISO7816_DATA	PCM_IN_A
GPIOX_10				PCM_FS_A
GPIOX_11				PCM_CLK_A
GPIOX_12		UART_TX_A	SLIP_UART_TX	
GPIOX_13		UART_RX_A	SLIP_UART_RX	
GPIOX_14		UART_CTS_A	SLIP_UART_CTS	
GPIOX_15		UART_RTS_A	SLIP_UART_RTS	
GPIOX_19		UART_RTS_B	PWM_E	
GPIOX_20				
GPIOX_21				

Table II.7.2 GPIOY_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4	Func5
GPIOY_0	TSin_D_VALID_A	DVP_HS_A			I2S_AO_CLK_IN
GPIOY_1	TSin_SOP_A	DVP_VS_A			I2S_LR_CLK_IN
GPIOY_2	TSin_CLK_A	DVP_CLK_A			
GPIOY_3	TSin_D0_A	DVP_D2_A			I2SIN_CH67
GPIOY_4	TSin_D1_A	DVP_D3_A		ISO7816_CLK	
GPIOY_5	TSin_D2_A	DVP_D4_A		ISO7816_DATA	
GPIOY_6	TSin_D3_A	DVP_D5_A			I2SIN_CH45
GPIOY_7	TSin_D4_A	DVP_D6_A			I2SIN_CH23
GPIOY_8	TSin_D5_A	DVP_D7_A			I2SOUT_CH23
GPIOY_9	Tsin_D6_A	DVP_D8_A			I2SOUT_CH45
GPIOY_10	TSin_D7_A	DVP_D9_A			I2SOUT_CH67
GPIOY_11	TSin_FAIL_A		SPDIF_IN	UART_CTS_C	
GPIOY_12			SPDIF_OUT	UART_RTS_C	
GPIOY_13			DMIC_IN	UART_TX_C	
GPIOY_14			DMIC_CLK_OUT	UART_RX_C	
GPIOY_15		DVP_D0_A		CLKOUT	PWM_F
GPIOY_16		DVP_D1_A			PWM_A

Table II.7.3 GPIODV_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
GPIODV_24	UART_TX_B	I2C_SDA_A	
GPIODV_25	UART_RX_B	I2C_SCK_A	
GPIODV_26	UART_CTS_B	I2C_SDA_B	
GPIODV_27	UART_RTS_B	I2C_SCK_B	
GPIODV_28		I2C_SDA_C	PWM_D
GPIODV_29		I2C_SCK_C	PWM_B

Table II.7.4 CARD_x Multi-Function Pin

Pin Name	Func1	Func2
CARD_0	SDCARD_D1	JTAG_TDI
CARD_1	SDCARD_D0	JTAG_TDO
CARD_2	SDCARD_CLK	JTAG_CLK
CARD_3	SDCARD_CMD	JTAG_TMS
CARD_4	SDCARD_D3	UART_TX_AO_A
CARD_5	SDCARD_D2	UART_RX_AO_A
CARD_6		

Table II.7.5 BOOT_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
BOOT_0	EMMC_NAND_D0		
BOOT_1	EMMC_NAND_D1		
BOOT_2	EMMC_NAND_D2		
BOOT_3	EMMC_NAND_D3		
BOOT_4	EMMC_NAND_D4		
BOOT_5	EMMC_NAND_D5		
BOOT_6	EMMC_NAND_D6		
BOOT_7	EMMC_NAND_D7		
BOOT_8	NAND_CE0		EMMC_CLK
BOOT_9	NAND_CE1		
BOOT_10	NAND_RB0		EMMC_CMD
BOOT_11	NAND_ALE	NOR_D	
BOOT_12	NAND_CLE	NOR_Q	
BOOT_13	NAND_WEN_CLK	NOR_C	
BOOT_14	NAND_REN_WR		
BOOT_15	NAND_DQS	NOR_CS	EMMC_DS

Table II.7.6 GPIOH_x Multi-Function Pin

Pin Name	Func1
GPIOH_0	HDMI_HPD (5V)
GPIOH_1	HDMI_SDA (5V)
GPIOH_2	HDMI_SCL (5V)
GPIOH_3	

Table II.7.7 GPIOZ_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOZ_0	ETH_MDIO	DVP_VS_B		
GPIOZ_1	ETH_MDC	DVP_HS_B		
GPIOZ_2	ETH_CLK_RMII_50M_IN/ ETH_RGMII_RX_CLK			
GPIOZ_3	ETH_RX_DV	DVP_CLK_B		
GPIOZ_4	ETH_RXD0	DVP_D2_B		
GPIOZ_5	ETH_RXD1	DVP_D3_B		
GPIOZ_6	ETH_RXD2	DVP_D4_B	SPI_SCLK	ISO7816_CLK
GPIOZ_7	ETH_RXD3	DVP_D5_B	SPI_SS0	ISO7816_Data
GPIOZ_8	ETH_RGMII_TX_CLK	DVP_D6_B		
GPIOZ_9	ETH_TX_EN	DVP_D7_B		
GPIOZ_10	ETH_TXD0	DVP_D8_B		
GPIOZ_11	ETH_TXD1	DVP_D9_B		
GPIOZ_12	ETH_TXD2		SPI_MISO	
GPIOZ_13	ETH_TXD3		SPI_MOSI	
GPIOZ_14				
GPIOZ_15		CLKOUT		

Table II.7.8 GPIOAO_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOAO_0	UART_TX_AO_A	UART_TX_AO_B		
GPIOAO_1	UART_RX_AO_A	UART_RX_AO_B		
GPIOAO_2	UART_CTS_AO_A	UART_CTS_AO_B		
GPIOAO_3	UART_RTS_AO_A	UART_RTS_AO_B		PWM_AO_A
GPIOAO_4	I2C_SCK_AO/ I2C_SLAVE_SCK_AO	UART_TX_AO_B		
GPIOAO_5	I2C_SDA_AO/ I2C_SLAVE_SDA_AO	UART_RX_AO_B		
GPIOAO_6	I2S_IN_01 (default)	SPDIF_OUT	CLK_32K_IN	PWM_AO_A
GPIOAO_7		REMOTE_INPUT/ REMOTE_OUTPUT		
GPIOAO_8	I2S_AM_CLK			JTAG_TCK
GPIOAO_9	I2S_AO_CLK_OUT		I2S_AO_CLK_IN	JTAG_TMS
GPIOAO_10	I2S_LR_CLK_OUT		I2S_LR_CLK_IN	JTAG_TDI
GPIOAO_11	I2SOUT_CH01			JTAG_TDO
GPIOAO_12		AO_CEC	EE_CEC	
GPIOAO_13	I2SOUT_CH45	REMOTE_OUTPUT	SPDIF_OUT	PWM_AO_B
TEST_N			WD_RESET_OUT	PWM_F
RESET_N	RESET_N			

Table II.7.9 GPIOCLK_x Multi-Function Pin

Pin Name	Func1	Func2
GPIOCLK_0	CLK24	CLK12(wifi)
GPIOCLK_1	CLK25	pwm_F

8. Signal Description

Table II.8.1~Table II.8. 21 give the Description of signals.

Table II. 8.1 SDIO Interface Signal Description

Signal Name	Type	Description
SDIO_D0	DIO	SDIO data bus bit 0 signal
SDIO_D1	DIO	SDIO data bus bit 1 signal
SDIO_D2	DIO	SDIO data bus bit 2 signal
SDIO_D3	DIO	SDIO data bus bit 3 signal
SDIO_CLK	DO	SDIO clock signal

Signal Name	Type	Description
SDIO_CMD	DIO	SDIO command signal
SDIO_IRQ	DIO	SDIO interrupt request signal

Table II.8.2 SDCARD Interface Signal Description

Signal Name	Type	Description
SDCARD_D0	DIO	SD Card data bus bit 0 signal
SDCARD_D1	DIO	SD Card data bus bit 1 signal
SDCARD_D2	DIO	SD Card data bus bit 2 signal
SDCARD_D3	DIO	SD Card data bus bit 3 signal
SDCARD_CLK	DO	SD Card clock signal
SDCARD_CMD	DIO	SD Card command signal

Table II.8.3 Clock Interface Signal Description

Signal Name	Type	Description
CLK12	DO	12MHz XTAL oscillator output
CLK24	DO	24MHz XTAL oscillator output
CLK25	DO	25MHz clock output
CLKOUT	DO	Configurable clock output

Table II.8.4 UART Interface Signal Description

Signal Name	Type	Description
UART_TX_A	DO	UART Port A data output
UART_RX_A	DI	UART Port A data input
UART_CTS_A	DI	UART Port A Clear To Send Signal
UART_RTS_A	DO	UART Port A Ready To Send Signal
UART_TX_B	DO	UART Port B data output
UART_RX_B	DI	UART Port B data input
UART_CTS_B	DI	UART Port B Clear To Send Signal
UART_RTS_B	DO	UART Port B Ready To Send Signal
UART_TX_C	DO	UART Port C data output
UART_RX_C	DI	UART Port C data input
UART_CTS_C	DI	UART Port C Clear To Send Signal
UART_RTS_C	DO	UART Port C Ready To Send Signal
SLIP_UART_TX	DO	UART Port SLIP data output
SLIP_UART_RX	DI	UART Port SLIP data input
SLIP_UART_CTS	DI	UART Port SLIP Clear To Send Signal
SLIP_UART_RTS	DO	UART Port SLIP Ready To Send Signal
UART_TX_AO_A	DO	UART Port AO_A data output
UART_RX_AO_A	DI	UART Port AO_A data input
UART_CTS_AO_A	DI	UART Port AO_A Clear To Send Signal
UART_RTS_AO_A	DO	UART Port AO_A Ready To Send Signal
UART_TX_AO_B	DO	UART Port AO_B data output
UART_RX_AO_B	DI	UART Port AO_B data input
UART_CTS_AO_B	DI	UART Port AO_B Clear To Send Signal
UART_RTS_AO_B	DO	UART Port AO_B Ready To Send Signal

Table II.8.5 PCM Interface Signal Description

Signal Name	Type	Description
PCM_OUT_A	DO	PCM port A output data stream
PCM_IN_A	DI	PCM port A input data stream

Signal Name	Type	Description
PCM_FS_A	DO	PCM port A frame synchronization
PCM_CLK_A	DO	PCM port A master clock input

Table II.8.6 TS In Interface Signal Description

Signal Name	Type	Description
TSin_D0_A	DI	TS input port A data bus bit 0 (LSB)
TSin_D1_A	DI	TS input port A data bus bit 1
TSin_D2_A	DI	TS input port A data bus bit 2
TSin_D3_A	DI	TS input port A data bus bit 3
TSin_D4_A	DI	TS input port A data bus bit 4
TSin_D5_A	DI	TS input port A data bus bit 5
TSin_D6_A	DI	TS input port A data bus bit 6
TSin_D7_A	DI	TS input port A data bus bit 7 (MSB)
TSin_CLK_A	DI	TS input port A clock
TSin_SOP_A	DI	TS input port A start of stream signal
TSin_D_VALID_A	DI	TS input port A date valid signal
TSin_FAIL_A	DI	TS input port A data failure signal
TSin_D0_B	DI	TS input port B data bus bit 0 (LSB)
TSin_CLK_B	DI	TS input port B clock
TSin_SOP_B	DI	TS input port B start of stream signal
TSin_D_VALID_B	DI	TS input port B date valid signal

Table II.8.7 DVP Interface Signal Description

Signal Name	Type	Description
DVP_D0_A	DI	DVP Port A input data bus bit 0 (LSB)
DVP_D1_A	DI	DVP Port A input data bus bit 1
DVP_D2_A	DI	DVP Port A input data bus bit 2
DVP_D3_A	DI	DVP Port A input data bus bit 3
DVP_D4_A	DI	DVP Port A input data bus bit 4
DVP_D5_A	DI	DVP Port A input data bus bit 5
DVP_D6_A	DI	DVP Port A input data bus bit 6
DVP_D7_A	DI	DVP Port A input data bus bit 7
DVP_D8_A	DI	DVP Port A input data bus bit 8
DVP_D9_A	DI	DVP Port A input data bus bit 9
DVP_CLK_A	DI	DVP Port A input master Clock
DVP_HS_A	DI	DVP Port A input HSYNC Signal
DVP_VS_A	DI	DVP Port A input VSYNC Signal
DVP_D2_B	DI	DVP Port B input data bus bit 2 (LSB)
DVP_D3_B	DI	DVP Port B input data bus bit 3
DVP_D4_B	DI	DVP Port B input data bus bit 4
DVP_D5_B	DI	DVP Port B input data bus bit 5
DVP_D6_B	DI	DVP Port B input data bus bit 6
DVP_D7_B	DI	DVP Port B input data bus bit 7
DVP_D8_B	DI	DVP Port B input data bus bit 8
DVP_D9_B	DI	DVP Port B input data bus bit 9
DVP_CLK_B	DI	DVP Port B input master Clock
DVP_HS_B	DI	DVP Port B input HSYNC Signal
DVP_VS_B	DI	DVP Port B input VSYNC Signal

Table II.8.8 PWM Interface Signal Description

Signal Name	Type	Description
PWM_A	DO	PWM channel A output signal
PWM_B	DO	PWM channel B output signal
PWM_C	DO	PWM channel C output signal
PWM_D	DO	PWM channel D output signal
PWM_E	DO	PWM channel E output signal
PWM_F	DO	PWM channel F output signal
PWM_AO_A	DO	PWM channel AO_A output signal
PWM_AO_B	DO	PWM channel AO_B output signal
PWM_VS	DO	PWM VSYNC output signal

Table II.8.9 I2C Interface Signal Description

Signal Name	Type	Description
I2C_SDA_A	DIO	I2C bus port A data input/output, Master or Slave
I2C_SCK_A	DIO	I2C bus port A clock input/output, Master or Slave
I2C_SDA_B	DIO	I2C bus port B data input/output, Master or Slave
I2C_SCK_B	DIO	I2C bus port B clock input/output, Master or Slave
I2C_SDA_C	DIO	I2C bus port C data input/output, Master or Slave
I2C_SCK_C	DIO	I2C bus port C clock input/output, Master or Slave
I2C_SDA_AO	DIO	Always-on I2C bus data input/output, Master or Slave
I2C_SCK_AO	DIO	Always-on I2C bus port A clock input/output, Master or Slave

Table II.8.10 I2S Interface Signal Description

Signal Name	Type	Description
I2S_OUT_01	DO	I2S Audio Data Output channel 0 and 1
I2S_OUT_23	DO	I2S Audio Data Output channel 2 and 3
I2S_OUT_45	DO	I2S Audio Data Output channel 4 and 5
I2S_OUT_67	DO	I2S Audio Data Output channel 6 and 7
I2S_LR_CLK_OUT	DO	I2S Left/Right Clock output
I2S_AO_CLK_OUT	DO	I2S data clock output
I2S_IN_CH01	DI	I2S Audio Data Input channel 0 and 1
I2S_IN_CH23	DI	I2S Audio Data Input channel 2 and 3
I2S_IN_CH45	DI	I2S Audio Data Input channel 4 and 5
I2S_IN_CH67	DI	I2S Audio Data Input channel 6 and 7
I2S_AO_CLK_IN	DI	I2S data clock input
I2S_LR_CLK_IN	DI	I2S Left/Right clock input
I2S_AM_CLK	DO	I2S master clock output

Table II.8.11 TCON Interface Signal Description

Signal Name	Type	Description
TCON_OEV	DO	TCON output enable input for scan driver
TCON_OEH	DO	TCON output enable input for data driver /DE
TCON_VCOM	DO	TCON common electrode driving signal
TCON_CPV	DO	TCON shift clock input for scan driver
TCON_STV1	DO	TCON vertical start pulse / VSYNC
TCON_STH1	DO	TCON horizontal start pulse / HYSNC
TCON_CPH	DO	TCON sampling and shifting clock pulse for data driver / PCLK

Table II.8.12 EMMC/NAND Interface Signal Description

Signal Name	Type	Description
EMMC_NAND_D0	DIO	eMMC/NAND data bus bit 0
EMMC_NAND_D1	DIO	eMMC/NAND data bus bit 1
EMMC_NAND_D2	DIO	eMMC/NAND data bus bit 2
EMMC_NAND_D3	DIO	eMMC/NAND data bus bit 3
EMMC_NAND_D4	DIO	eMMC/NAND data bus bit 4
EMMC_NAND_D5	DIO	eMMC/NAND data bus bit 5
EMMC_NAND_D6	DIO	eMMC/NAND data bus bit 6
EMMC_NAND_D7	DIO	eMMC/NAND data bus bit 7
NAND_CE0	DO	NAND chip enable 0
NAND_CE1	DO	NAND chip enable 1
NAND_CE2	DO	NAND chip enable 2
NAND_CE3	DO	NAND chip enable 3
NAND_RB0	DI	NAND ready/busy
NAND_ALE	DO	NAND address latch enable:
NAND_CLE	DO	NAND command latch enable:
NAND_WEN_CLK	DO	NAND write enable and clock:
NAND_REN_WR	DO	NAND read enable and write/read:
NAND_DQS	DIO	NAND data strobe
EMMC_CLK	DO	eMMC clock output
EMMC_CMD	DIO	eMMC command signal
EMMC_DS	DI	eMMC data strobe

Table II.8.13 NOR Interface Signal Description

Signal Name	Type	Description
NOR_D	DO	SPI NOR Master Output
NOR_Q	DI	SPI NOR Master Input
NOR_C	DO	SPI NOR Serial Clock
NOR_CS	DO	SPI NOR chip select

Table II.8.14 SPI Interface Signal Description

Signal Name	Type	Description
SPI_MOSI	DIO	SPI master output, slave input
SPI_MISO	DIO	SPI master input, slave output
SPI_SCLK	DO	SPI serial clock
SPI_SS0	DO	SPI slave select 0
SPI_SS1	DO	SPI slave select 1
SPI_SS2	DO	SPI slave select 2

Table II.8.15 Remote Interface Signal Description

Signal Name	Type	Description
IR_REMOTE_INPUT	DI	IR remote control input
IR_REMOTE_OUTPUT	DO	IR remote control output

Table II.8.16 JTAG Interface Signal Description

Signal Name	Type	Description
JTAG_TDO	DO	JTAG data output
JTAG_TDI	DI	JTAG data input
JTAG_TMS	DI	JTAG Test mode select input
JTAG_TCK	DI	JTAG Test clock input

Table II.8.17 HDMI Interface Signal Description

Signal Name	Type	Description
HDMI_HPD	DI	HDMI hot plug in detection signal input
HDMI_SDA	DIO	HDMI I2C control interface data signal
HDMI_SCL	DO	HDMI I2C control interface clock signal
EE_CEC	DIO	HDMI EE CEC (Consumer electronics control)
AO_CEC	DIO	HDMI AO CEC (Consumer electronics control)

Table II.8.18 RMII/RGMII Interface Signal Description

Signal Name	Type	Description
ETH_CLK_RMII_50M_IN	DI	Ethernet RMII interface reference clock input
ETH_RGMII_RX_CLK	DI	Ethernet RGMII interface receive clock input
ETH_RGMII_TX_CLK	DO	Ethernet RGMII transmit clock
ETH_TX_EN	DO	Ethernet RMII/RGMII Interface transmit enable
ETH_TXD3	DO	Ethernet RGMII interface transmit data 3
ETH_TXD2	DO	Ethernet RGMII interface transmit data 2
ETH_TXD1	DO	Ethernet RMII/RGMII interface transmit data 1
ETH_TXD0	DO	Ethernet RMII/RGMII interface transmit data 0
ETH_RX_CLK	DI	Ethernet RMII/RGMII receive clock
ETH_RX_DV	DI	Ethernet RMII/RGMII interface receive data valid signal
ETH_RXD3	DI	Ethernet RGMII interface receive data 3
ETH_RXD2	DI	Ethernet RGMII interface receive data 2
ETH_RXD1	DI	Ethernet RMII/RGMII interface receive data 1
ETH_RXD0	DI	Ethernet RMII/RGMII interface receive data 0
ETH_MDIO	DIO	Ethernet RMII/RGMII interface management data input/output
ETH_MDC	DO	Ethernet RMII/RGMII interface management data clock

Table II.8.19 SPDIF Interface Signal Description

Signal Name	Type	Description
SPDIF_IN	DI	SPDIF input signal
SPDIF_OUT	DO	SPDIF output signal

Table II.8.20 Digital MIC Interface Signal Description

Signal Name	Type	Description
DMIC_IN	DI	Digital MIC input signal
DMIC_CLK_OUT	DO	Digital MIC clock output signal

Table II.8.21 ISO7816 Interface Signal Description

Signal Name	Type	Description
ISO7816_CLK	DO	ISO7816 clock signal
ISO7816_DATA	DIO	ISO7816 serial data signal

9. Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Table II.9.1 Absolute Maximum Rating

Characteristic	Value	Unit
VDD_CPU Supply Voltage	1.3	V
VDD_EE Supply Voltage	1.3	V
VDDQ Supply Voltage	1.75	V
1.8V Supply Voltage	1.98	V
3.3V Supply Voltage	3.63	V
Input voltage, V_I	-0.3 ~ VDDIO+0.3	V
Junction Temperature	125	°C

10. Recommended Operating Conditions

The table below gives the recommended operating conditions of S905. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Table II.10.1 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDCPU	Voltage for Cortex A53 CPU	0.77[1]	1.0	1.19[2]	V
VDDEE_0V9	Voltage for GPU & core logic	0.77[1]	1.0	1.19[2]	V
VDDAO_0V9	Voltage for AO core logic	0.77[1]	1.0	1.19[2]	V
VDDQ	DDR3/LPDDR2/LPDDR3 IO Supply Voltage	1.15		1.6	V
AVDD18	1.8V AVDD for VDD18_XTAL_CLK, AVDD18_DPLL, AVDD18_USB_ADC, AVDD18_CVBS_EFUSE, PLL_VDD, HDMI_AVDD18, HPLL_AVDD18	1.71	1.80	1.89	V
USB33_VDDIOH	3.3V AVDD for USB and 3.3V VDDIO for GPIO_H	3.15	3.3	3.45	V
VDDIO	LV mode	1.71	1.80	1.89	V
	HV mode	2.8/3.0[3]	3.3	3.45	V
IOVREF_1V8	Voltage for IOVREF	1.71	1.80	1.89	V
T_J	Junction Temperature	0		125[4]	°C
T_A	Operating Temperature	0		70	°C

Note:

1) Minimal VDD_CPU/VDD_EE voltage is for sleep mode while system runs at 32.768KHz. Higher clock will need higher voltage. Considering the power supply may have 3% deviation, the minimal voltage in actual application should not be set to lower than 0.8V.
2) Likewise, this maximum VDD_CPU/VDD_EE voltage in actual application should not be higher than 1.1V. Voltage of VDD_CPU will affect CPU speed. Use lower voltage when CPU runs on lower speed to save power.
3) GPIO output driving strength will be weaker when VDDIO < 3.0V in HV mode. Signal ramp-up speed and max operation speed are lower than VDDIO at 3.3V.
4) For operating temperature, good heat sink may be needed to guarantee Tj < 125°C.

11. Ripple Voltage Specifications

Table II.11.1 below gives the ripple voltage of S905.

Table II.11.1 Ripple Voltage Specifications

Parameter	Recommended Voltage	Max Ripple	Unit
VDD_EE	1.0V	50	mV
VDDIO_AO18	1.8V	55	mV
VCCK	1.05V	50	mV
VDDIO_AO	3.3V	100	mV
VCC1.8V	1.8V	55	mV
DDR3_1.5V	1.5V	50	mV
MDDR3_VREF0	0.75V	50	mV
VDDIO_BOOT	1.8V/3.3V	55/100	mV
HDMI_AVDD18	1.8V	55	mV
HDMI_VDD09	1.05V	50	mV
VCC3.3V	3.3V	100	mV

12. Thermal Operating Specifications

The table below gives the thermal operation specification.

Table II.12.1 Thermal Operation Specification

Symbol	Parameter	Value.	Unit
Θjc	Package junction-to-case thermal resistance in nature convection	9.42	°C/Watt

13. DC Electrical Characteristics

13.1 Normal GPIO Specifications (For DIO_xmA)

Table II.13.1 gives the normal GPIO specifications.

Table II.13.1 Normal GPIO Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{iH}	High-level input voltage	IOVREF/2+0.3		VDDIO+0.3	V
V_{iL}	Low-level input voltage	-0.3		IOVREF/2-0.3	V
$R_{PU/PD}$	Built-in pull up/down resistor		60K		ohm
DIO_2mA	2mA IO driving capability	2[1]		3[2]	mA
DIO_3mA	3mA IO driving capability	3[1]		4.5[2]	mA
DIO_4mA	4mA IO driving capability	4[1]		6[2]	mA

Note:

1) Minimal driving capability applies when VDDIO LV 1.71V, or VDDIO HV 3.0V, VOL<0.4V.
2) Maximal driving capability only applies to applications such as driving LED when VOL<0.6V.

13.2 Open Drain GPIO Specifications (For DIO_OD)

Table II.13.2 shows the open drain GPIO Specifications.

Table II.13.2 Open Drain GPIO Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{iH}	High-level input voltage	2.2		5.5	V
V_{iL}	Low-level input voltage	-0.3		0.8	V
$R_{PU/PD}$	No built-in pull up/down resistor on OD IO		N/A		ohm
Iol	OD IO driving low capability		6		mA

13.3 DDR3/LPDDR2/LPDDR3 SDRAM Specifications

Table II.13.3~Table II.13.6 show the recommended operating conditions of DDR/SDRAM, DDR3/DDR3L/DDR3U LPDDR2 and LPDDR3 module respectively.

Table II.13.3 Recommended Operating Conditions of DDR/SDRAM Module

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDQ	IO supply voltage(DDR3)	1.46	1.50	1.57	V
VDDQ	IO supply voltage(DDR3L)	1.31	1.35	1.45	V
VDDQ	IO supply voltage(DDR3U)	1.21	1.25	1.31	V
VDDQ	IO supply voltage(LPDDR2/LPDDR3)	1.16	1.20	1.30	V

Vref	Input reference supply voltage	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V

Note: The minimal VDDQ voltage in sleep mode is defined by memory.

Table II.13.4 DC specifications - DDR3/DDR3L/DDR3U mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.100		VDDQ	V
VIL	DC input voltage low	VSSQ		Vref-0.100	V
VOH	DC output logic high	0.8*VDDQ			V
VOL	DC output logic low			0.2*VDDQ	V
RTT	Input termination resistance to VDDQ/2	100 54 36	120 60 40	140 66 44	ohm

Table II.13.5 DC Specifications – LPDDR2 mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.13		VDDQ	V
VIL	DC input voltage low	VSSQ		Vref-0.13	V
VOH	DC output logic high	0.9*VDDQ			V
VOL	DC output logic low			0.1*VDDQ	V

Table II.13.6 DC Specifications – LPDDR3 mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.100		VDDQ	V
VIL	DC input voltage low	VSSQ		Vref-0.100	V
VOH	DC output logic high	0.9*VDDQ			V
VOL	DC output logic low			0.1*VDDQ	V
RTT	Input termination resistance to VDDQ	100 200	120 240	140 280	ohm

13.4 Recommended Oscillator Electrical Characteristics

S905 requires the 24MHz oscillator for generating the main clock source.

Table II.13.7 24MHz Oscillator Specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_0	Nominal Frequency		24		MHz	
$\Delta f/f_0$	Frequency Tolerance	-30		+30	ppm	At 25 ℃
		-50		+50	ppm	At -20~85 ℃
C_L	Load Capacitance	8	12	20	pF	
ESR	Equivalent Series Resistance			80	oHm	

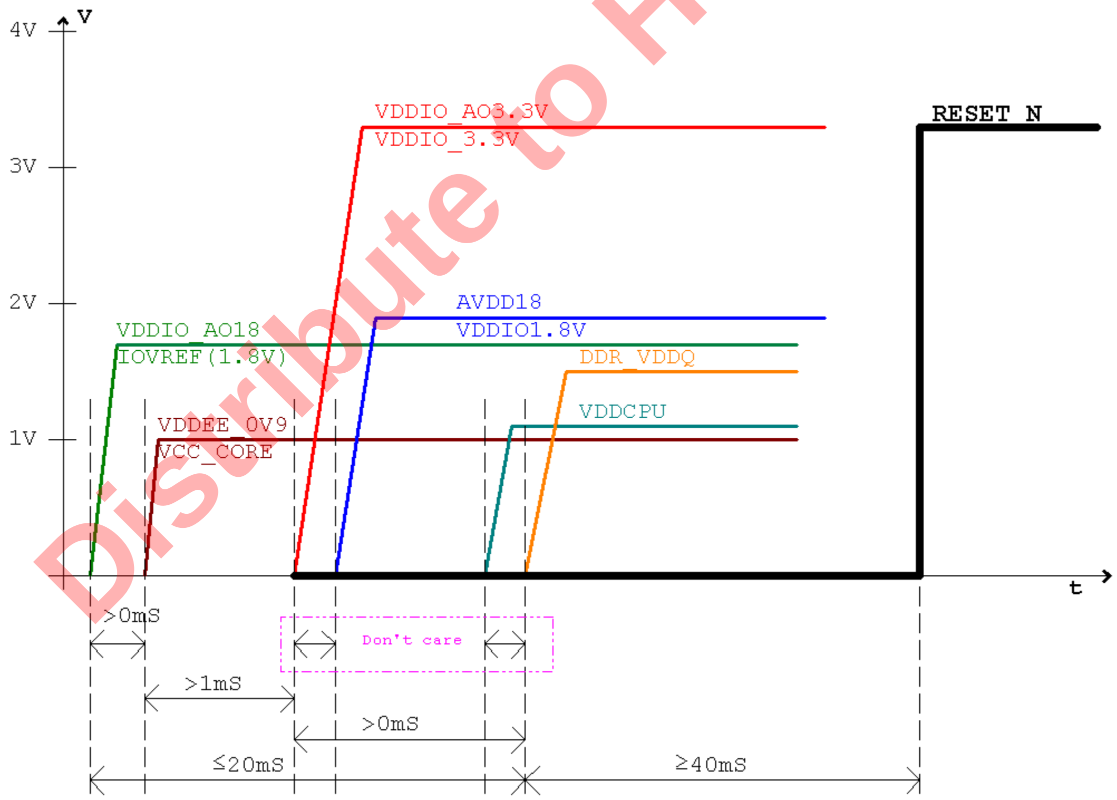
Note: 10ppm Tolerance is preferred if 24MHz XTAL is also driving WIFI module.

14. Recommended Power on sequence

Example power on sequence is shown in Fig II.14.1：

VDDIO_AO18&IOVREF->VDDEE_0V9->VDDIO_AO3.3V&VDDIO_3.3V&AVDD18& VDDIO1.8V ->VDDCPU&VDDQ

Fig II.14.1 Recommended Power on Sequence



Note:

1) No sequence requirement between power domains which are grouped as showing in the example sequence above.
2) Step delay should be 0-4ms. VDDIO_AO3.3V&VDDIO_3.3V is recommended to ramp up at least 1ms later than VDDEE.

3) VCC_CORE is the power Name if VDDEE and VDDCPU are merged.
4) VDDQ can be off and enabled by software.
5) VDDIO3.3V should never exceed IOVREF_1V8 + 2V.
6) Reset should be low before power up & kept low > 40ms after all power is on (except VDDQ).
7) VDDIO_AO18 is for some GPIOs such as WiFi IO.

Please refer to reference schematics.

15. Power Consumption

Note：Value listed here is typical max value tested. Enough margin in circuit needs to be reserved.

Table II. 15.1 System Power Consumption

Symbol	Maximum Current	Note
VDDCPU	2A	
VDDEE_0V9	2A	
VDDQ	1A	Total power of controller and DDR3 memory

Table II.15.2 Module Power Consumption

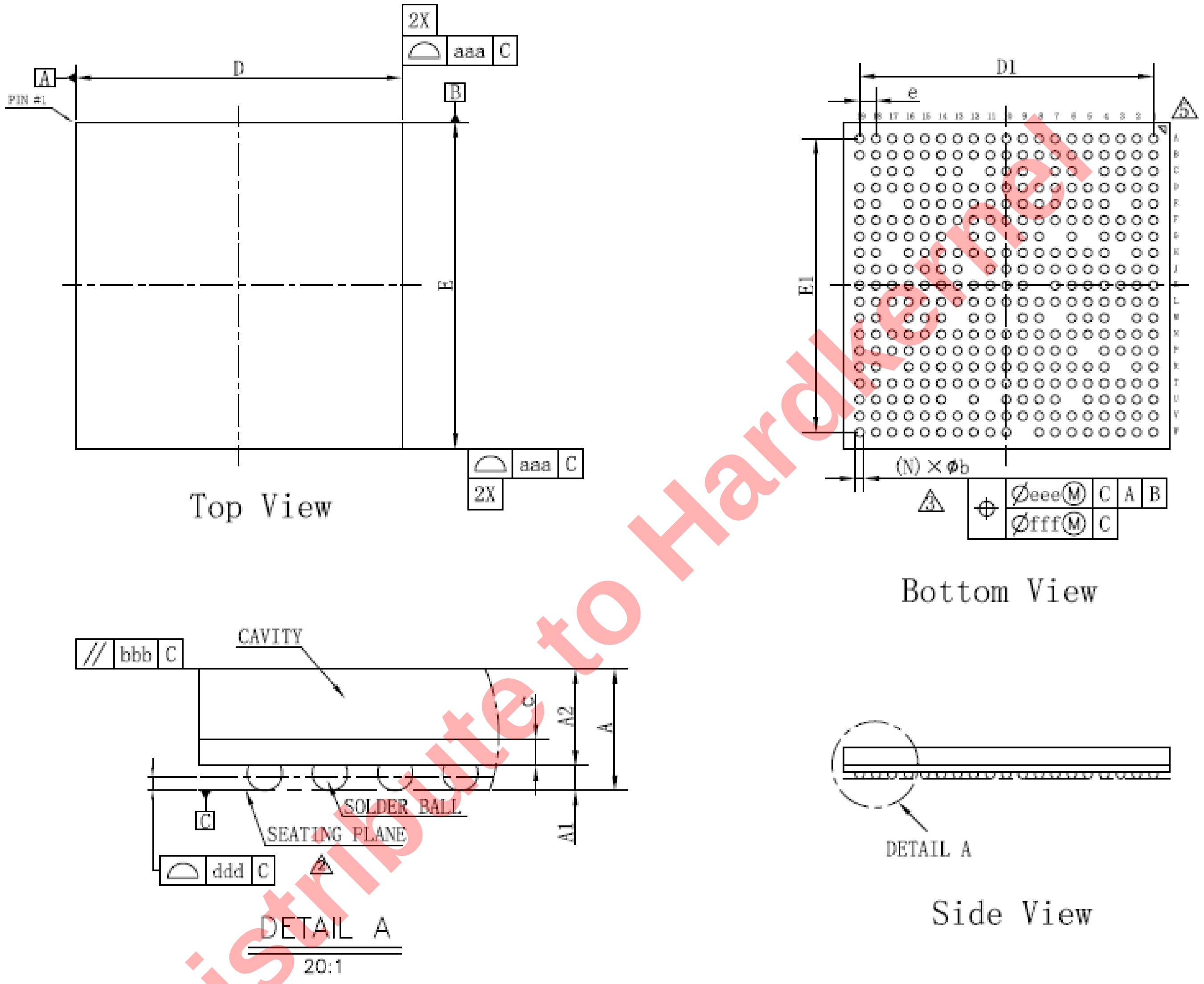
Symbol	Typical current	Maximum current	Note
HDMITX_AVDD33	80mA	-	At 6Gbps mode
USB33_VDDIOH	32mA	-	USB: 16mA Per channel, full/low speed mode, total 2 channel VDDIOH: normally 0mA, will be higher if there's pull low loading.
HDMI_AVDD18	80mA	-	At 6Gbps mode
HPLL_AVDD18	9mA	-	
AVDD18_DPLL	7mA	-	
PLL_VDD	35mA	-	Typical value when DDR3 controller is enabled
VDD18_XTAL_CLK	0.4mA	-	Typical value 0.4mA when XTAL is oscillating
AVDD18_USB_ADC	-	40mA	USB: 19mA per channel at high speed ode , total 2 channel ADC: 1.2mA During sampling
AVDD18_CVBS_EFUSE	38mA	-	EFUSE: Max 100mA when programing EFUSE. Normally 0mA CVBS: 38mA typically when CVBS output enabled.
IOVREF_1V8	0mA	20mA	Max 20mA when all GPIO powered with 3.3V & switch at 75MHz. Normally 0mA

16. Mechanical Dimension

The S905 processor comes in a 19x19 ball matrix LFBGA RoHS package. The mechanical dimensions are given in millimeters as below.

Note the following positions have null balls: C5, C8, C12, C15, C19, E3, E17, G5, G7, G10, G13, H3, H17, J12, K8, M3, M7, M10, M13, M17, P5, R3, R17, U6, U11, U13, W9.

Fig II.16.1 Mechanical Dimension of S905



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.310	—	—	0.052
A1	0.200	0.250	0.300	0.008	0.010	0.012
A2	0.910	0.960	1.010	0.036	0.038	0.040
c	0.220	0.260	0.300	0.009	0.010	0.012
D	12.900	13.000	13.100	0.508	0.512	0.516
E	12.900	13.000	13.100	0.508	0.512	0.516
D1	—	11.700	—	—	0.461	—
E1	—	11.700	—	—	0.461	—
e	—	0.650	—	—	0.026	—
b	0.300	0.350	0.400	0.012	0.014	0.016
aaa	0.150			0.006		
bbb	0.200			0.008		
ddd	0.100			0.004		
eee	0.150			0.006		
fff	0.080			0.003		
N	334			334		
MD/ME	19/19			19/19		

Section III System

This part describes the S905 system architecture from the following aspects:

- MEMORY MAP
- POWER DOMAIN
- CPU and GPU SUBSYSTEM
- CLOCK AND RESET UNIT
- SYSTEM BOOT
- GENERAL PURPOSE INPUT/OUTPUT (GPIO)
- INTERRUPT CONTROLLER
- DIRECT MEMORY ACCESS CONTROLLER (DMAC)
- TIMER
- Crypto

17. Memory Map

S905's memory map is listed as following in Table III.17.1.

Table III.17.1 S905 Memory Map

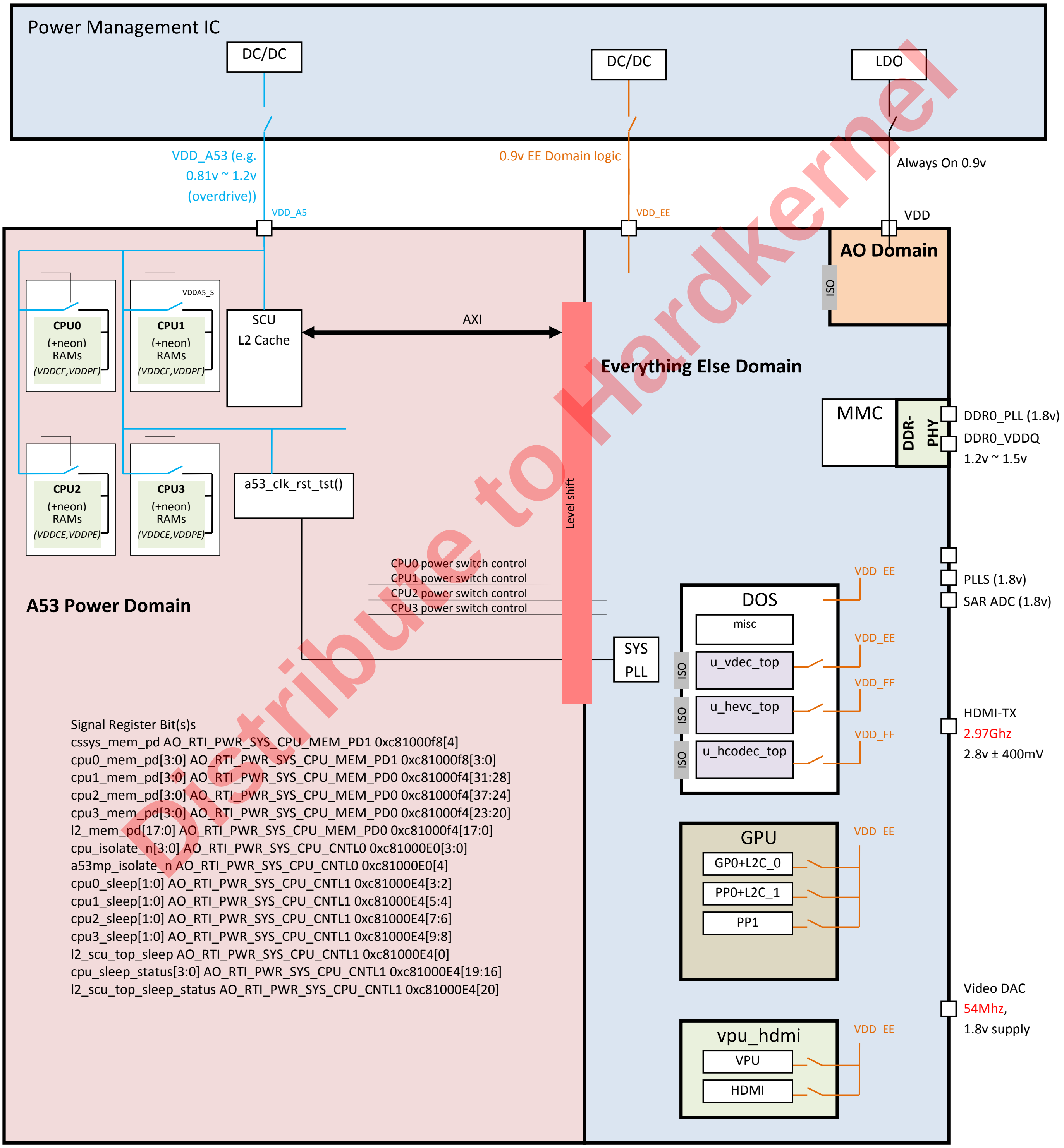
Start	End	Region (Normal)	NIC Arbitor
0x00000000	0xBFFFFFFF	DDR	**DDR**
0xC0000000	0xC01FFFFF	USB	
0xC0200000	0xC03FFFFF	DAP	
0xC0400000	0xC07FFFFF	CSSYS	
0xC0800000	0xC08043FF		
0xC0804400	0xC08044FF	RESET	
0XC0804500	0xC08047FF		
0xC0804800	0xC08048FF	VDIN	
0xC0804900	0xC08053FF		
0xC0805400	0xC08054FF	AIU	
0xC0805500	0xC08057FF		
0xC0805800	0xC08058FF	STB	
0xC0805900	0xC0807BFF		**CAPB3**
0xC0807C00	0xC0807CFF	ASSIST	
0xC0807D00	0xC08083FF		
0xC0808400	0xC08084FF	PERIPHS	
0xC0808500	0xC0808BFF		
0xC0808C00	0xC0808CFF	PERIPHS	
0xC0808D00	0xC08097FF		
0xC0809800	0xC08098FF	ISA	
0xC0809900	0xC080BFFF		
0xC080A000	0xC080A0FF	AUDIN	
0xC080A100	0xC080A3FF		
0xC080A400	0xC080A4FF	PARSER	
0xC080A500	0xC12FFFFF		
0xC1300000	0xC42FFFFF		
0xC4300000	0xC4307FFF	GIC	**GIC**
0xC4308FFF	0xC7FFFFFF		
0xC8000000	0xC8013FFF		
0xC8014000	0xC80FFFFF		
0xC8100000	0xC81FFFFF	RTI	
0xC8200000	0xC881FFFF		**SYS AHB**
0xC8820000	0xC882FFFF	DOS	
0xC8830000	0xC8831FFF		
0xC8832000	0xC8833FFF	BLKMV	

Start	End	Region (Normal)	NIC Arbitor
0xC8834000	0xC8835FFF	PERIPHS	
0xC8836000	0xC8837FFF	DDR TOP	
0xC8838000	0xC8839FFF	DMC	
0xC883A000	0xC883BFFF	HDMITX	
0xC883C000	0xC883DFFF	HIU	
0xC883E000	0xC8FFFFFF		
0xC9000000	0xC90FFFFF	USB0	
0xC9100000	0xC91FFFFF	USB1	
0xC9200000	0xC940FFFF	-	
0xC9410000	0xC941FFFF	ETHERNET	
0xCC000000	0xCFFFFFFF	SPI	
0xD0000000	0xD0041FFF		CAPB3
0xD0042000	0xD0043FFF	PDM	
0xD0044000	0xD00440FF	HDCP22	
0xD0044100	0xD0047FFF		
0xD0048000	0xD004FFFF	BT656	
0xD0050000	0xD005FFFF	BT656_2	
0xD0060000	0xD006FFFF		
0xD0070000	0xD0071FFF	SD_EMMC_A	
0xD0072000	0xD0073FFF	SD_EMMC_B	
0xD0074000	0xD0075FFF	SD_EMMC_C	
0xD0076000	0xD00BFFFF		
0xD00C0000	0xD00FFFFF	MALI APB	
0xD0100000	0xD013FFFF	VPU	VAPB3
0xD0150000	0xD015FFFF		
0xD0160000	0xD016FFFF	GE2D	
0xD0170000	0xD01FFFFF		
0xE0000000	0xFFFFFFFF		

18. Power Domain

Fig III.18.1 shows the power domain of S905.

Fig III.18.1 Power Domain



18.1 Top Level Power Domains

The power supplies for the different domains must follow a specific power supply order: The A53 can't be powered without the EE domain. The EE domain can't be powered up without the AO domain. If you read the Table III.18.1 left to right then right to left, that's essentially the power up/down sequence for the entire chip.

Table III.18.1 Power on Sequence of Different Power Domains

	Always On	**EE Domain**		**A53 domain**				
	Logic	EE Logic	Mali and DOS and VPU	A53 (SCU/L2)	L2 Cache	CPU0	CPU1	CPU2/3
STATE 0 All off	Off	The EE domain must be OFF if the AO domain is off		The A53 domain must be off if the EE domain is OFF				
STATE 1 Hibernate: Only the Always on Domain is powered	On	Off	The Mali must be OFF is if the EE domain is off	The A53 domain must be off if the EE domain is OFF				
STATE 2 Always On/EE only (for example audio applications or simple video applications that don't need the A53)	On	On	On or off as needed	Off	Off	Off	Off	Off
STATE 3 Single CPU	On	On	On or off as needed	All three must be enabled			Off	Off
STATE 4 2 CPU's	On	On	On or off as needed	All three must be enabled			On	Off
STATE 5 4 CPUs	On	On	On or off as needed	All three must be enabled			On	On

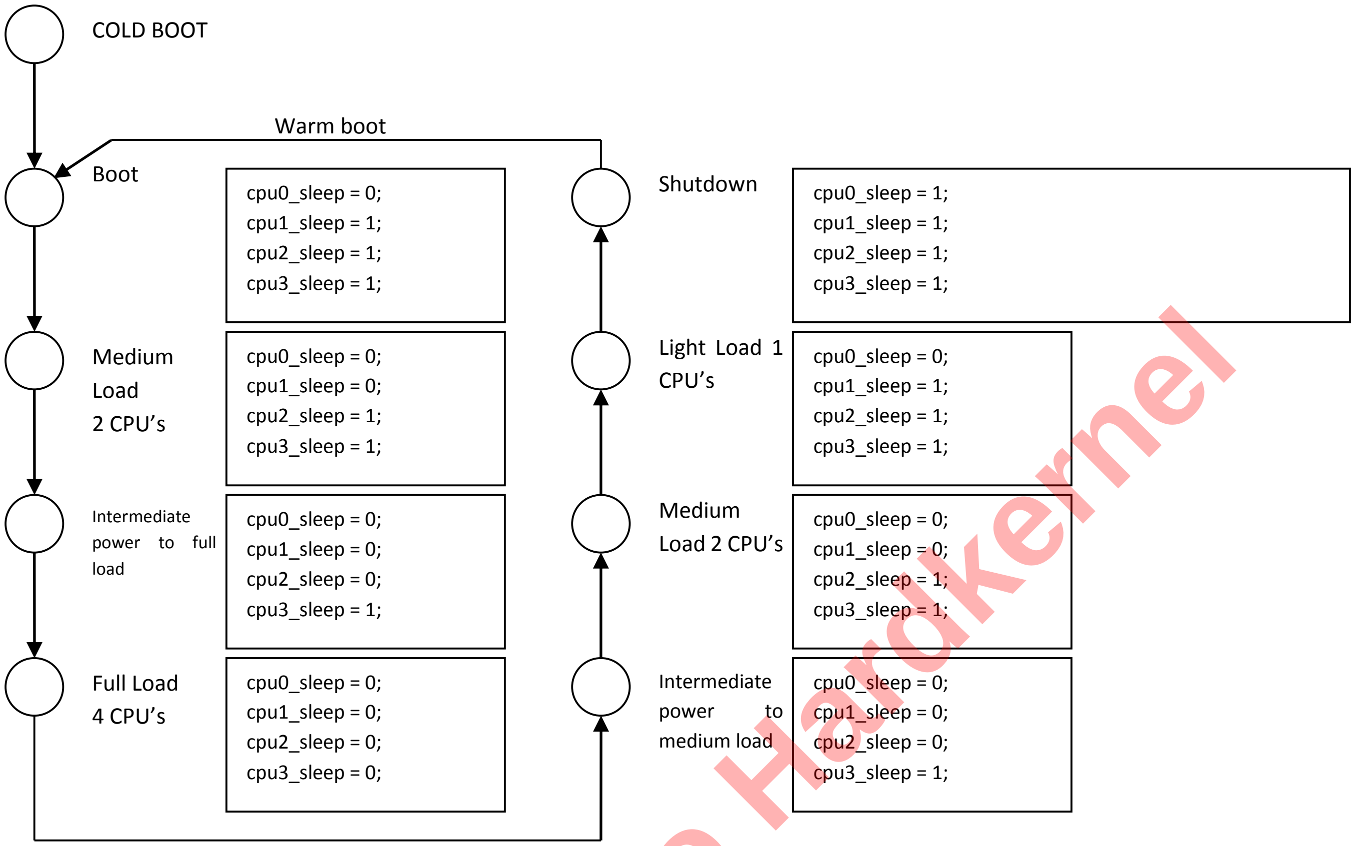
18.2 A53 Power Modes

The A53 domain is the last to power up and the first to power down. The A53 domain itself consists of a quad (4) CPU, an L2 cache controller and an SCU. The A53 CPU boots with the SCU/L2 powered and CPU0 powered. After CPU0 boots, subsequent CPU's can be enabled and disabled independently of one another using the control bits described below. The most likely scenario would be for the CPU0 to be used for low load conditions, CPU0 and CPU1 to be used for medium load conditions and CPU0,1,2 and CPU3 to all be used for heavy load conditions. It's unlikely we will run a 3 CPU configuration (although it's not precluded by the hardware). The flow-diagram below illustrates the transition to each legal state.

Table III.18.2 Power On Sequence of A53

	CPU0	**CPU1**	**CPU2**	**CPU3**
Domain Power Sleep bit (1 = power off)	Bit[2] of 0xC81000E4	Bit[4] of 0xC81000E4	Bit[6] of 0xC81000E4	Bit[8] of 0xC81000E4
Domain Power Acknowledge bit	Bit[16] of 0xC81000E4	Bit[17] of 0xC81000E4	Bit[18] of 0xC81000E4	Bit[19] of 0xC81000E4
Input Signal isolation bit (1 = isolated)	Bit[0] of 0xC81000E0	Bit[1] of 0xC81000E0	Bit[2] of 0xC81000E0	Bit[3] of 0xC81000E0
Output signal isolation bit (1 = isolated)	Bit[0] of 0xC81000E0	Bit[1] of 0xC81000E0	Bit[2] of 0xC81000E0	Bit[3] of 0xC81000E0

Fig III.18.2 Power Seuquence of A53



18.3 EE Top Level Power Modes

EE domain is powered off by DC-DC. VDD_EE also share the same VDD with VDDCE of A53 memory arrays. So if EE domains is shut off, A53 memory is also shut off. That does not matter. Before EE power domain is shut off, A53 should be shut off at first.

Table III.18.3 Power Sequence of EE Domain

	Register/Bit(s)
Ethernet Memory PD	Bits[3:2] of 0xC883C100 (HI_MEM_PD_REG0) 0x3 = power off, 0x0 = normal operation
HDMI Memory PD	Bits[15:8] of 0xC883C100 (HI_MEM_PD_REG0) 0xFF = power off, 0x0 = normal operation
VPU memory PD	Bit[31:0] of 0xC883C104/ 0xC883C108 0xFFFFFFFF = power off, 0x0 = normal operation

18.4 Mali Power Modes

The Mali block sits within the EE domain and the Mali module itself has 3 distinct power domains:

- GP + L2C_0
- PP0 + L2C_1
- PP12

We will power these up in sequence so as to reduce the surge currents. The following combinations are possible.

Table II.18.4 Power Sequence of Mali Module

Mali AXI Cores	1PP Power up/down	3PP Power up/down
GP + L2C_0	1st / last	1st / last
PP0 + L2C_1	2nd / 1st	2nd / 2nd
PP12		3rd / 1st

18.5 Power/Isolation/Memory Power Down Register Summary

Below lists the registers related to A53.

A53 Isolation 0xc81000e0

Bit(s)	R/W	Default	Description
31~30	R	-	CPU3 CTRL_MODE set by the CPU
29~28	R	-	CPU3 CTRL_MODE set by the CPU
27~26	R	-	CPU3 CTRL_MODE set by the CPU
25~24	R	-	CPU3 CTRL_MODE set by the CPU
23~22	R/W	11	CPU3 CTRL_MODE
21~20	R/W	11	CPU2 CTRL_MODE
19~18	R/W	11	CPU1 CTRL_MODE
17~16	R/W	00	CPU0 CTRL_MODE (set to tell the CPU which mode to enter)
15~14	R/W	0	Reserved
13	R/W	0	A53 Pwr top level clamp
12	R/W	0	SCURAM Clamp
11~8	R/W	0xE	NEON[3:0] Clamp
7~4	R/W	0xE	CPURAM[3:0] clamp
3~0	R/W	0xE	CPU[3:0] clamp

A53 Power 0xc81000e4

Bit(s)	R/W	Default	Description
31~20	R	0	Reserved
19	R	-	CPU3 Sleep status: 1 = powered down
18	R	-	CPU2 Sleep status: 1 = powered down
17	R	-	CPU1 Sleep status: 1 = powered down
16	R	-	CPU0 Sleep status: 1 = powered down
15~10	R/W	00	Reserved
9~8	R/W	11	CPU3 sleep: 1 = powered down
7~6	R/W	11	CPU2 sleep: 1 = powered down
5~4	R/W	11	CPU1 sleep: 1 = powered down
3~2	R/W	00	CPU0 sleep: 1 = powered down
1-0	R/W	10	Reserved

A53 RAM Power Down Control 0xc81000f4

Bit(s)	R/W	Default	Description
31-28	R/W	0xF	CPU1 RAM power down (Each Bit controls different RAMs): 1 = powered down
27-24	R/W	0xF	CPU2 RAM power down (Each Bit controls different RAMs): 1 = powered down
23-20	R/W	0xF	CPU3 RAM power down (Each Bit controls different RAMs): 1 = powered down
19-18	-	0	Reserved
17~0	R/W	0x00000	L2 RAM power down (Each Bit controls different RAMs): 1 = powered down

A53 RAM Power Down Control (cont.) 0xc81000f8

Bit(s)	R/W	Default	Description
31-4	-	0	Reserved
3~0	R/W	0x0	CPU0 RAM power down (Each Bit controls different RAMs): 1 = powered down

A53 SYS PLL 0xc1104300

PLL Enable = Bit[30]: 1 = pll enabled, 0 = pll disabled

Always On domain PWR_CNTL1 0xc810000c

Bit(s)	R/W	Default	Description
31~4	R/W	0	Reserved
3	R/W	0	DDR1PHYIO_RET_EN
2	R/W	0	DDR1PHYIO_REG_EN_N
1	R/W	0	DDR0PHYIO_RET_EN
0	R/W	0	DDR0PHYIO_REG_EN_N

Always On domain PWR_CNTL0 0xc8100010

Bit(s)	R/W	Default	Description
31~28	R/W	0	Reserved
27~22	R/W	0	reserved
21~20	R/W	0	AHB SRAM Memory power down: 00 = normal operation, 10 = power down. Other conditions reserved
19~16	R/W	0	Reserved
15~14	R/W	0	Reserved
13~12	R/W	0	32khz DS:
11~10	R/W	0	Alternate 32khz input clock select from GPIO pad
9	R/W	1	Reset to the EE domain. 0 = reset, 1 = normal operation
8	R/W	0	RTC oscillator input select: 1 = use RTC clock as clock. 0= used clk81 as the clock
7~5	R/W	0	reserved
4	R/W	0	EE domain isolation In
3	R/W	0	EE domain Isolation out
2	R/W	0	Reserved
1	R/W	0	Always on RESET isolation: 1 = isolated
0	R/W	0	Reserved

General Power gen_pwr_sleep_cntl0 0xc81000e8

Bit(s)	R/W	Default	Description
31~10	R/W	0	Reserved
9	R/W	0	VPU/HDMI Isolation
8	R/W	0	VPU/HDMI power: 1 = powered off
7~6	R/W	0	Reserved
5	R/W	1	Reserved
4	R/W	1	Reserved
3	R/W	1	Reserved
2	R/W	1	Reserved
1	R/W	1	Reserved
0	R/W	1	Reserved

General Isolation gen_pwr_iso_cntl0 0xc81000ec

Bit(s)	Description
31~10	Reserved
9	Reserved
8	Reserved
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	GPU ISO OUT
2	GPU ISO IN
1~0	reserved

General Acknowledge gen_pwr_sleep_ack0 0xc81000f0

Bit(s)	Description
31~9	Reserved
8	Reserved
7	MALI_PWRUP_ACK: PP456 acknowledge: 1 = powered off
6	MALI_PWRUP_ACK: PP12 acknowledge: 1 = powered off
5	MALI_PWRUP_ACK: PP0 acknowledge: 1 = powered off
4	MALI_PWRUP_ACK: GP acknowledge: 1 = powered off
3	Reserved
2	Reserved
1	Reserved
0	Reserved

Mali Power UP (domains_npwr_up) 0xd00c2000

Bit(s)	Description
31~3	Reserved
3	MALI PP456 power up: Write a 1 to power up
2	MALI PP12 power up
1	MALI PP0 power up
0	MALI GP power up

Mali Power Down (domains_npwr_up) 0xd00c2004

Bit(s)	Description
31~3	Reserved
3	MALI PP456 power down: Write a 1 to power down
2	MALI PP12 power down
1	MALI PP0 power down
0	MALI GP power down

19. System Booting

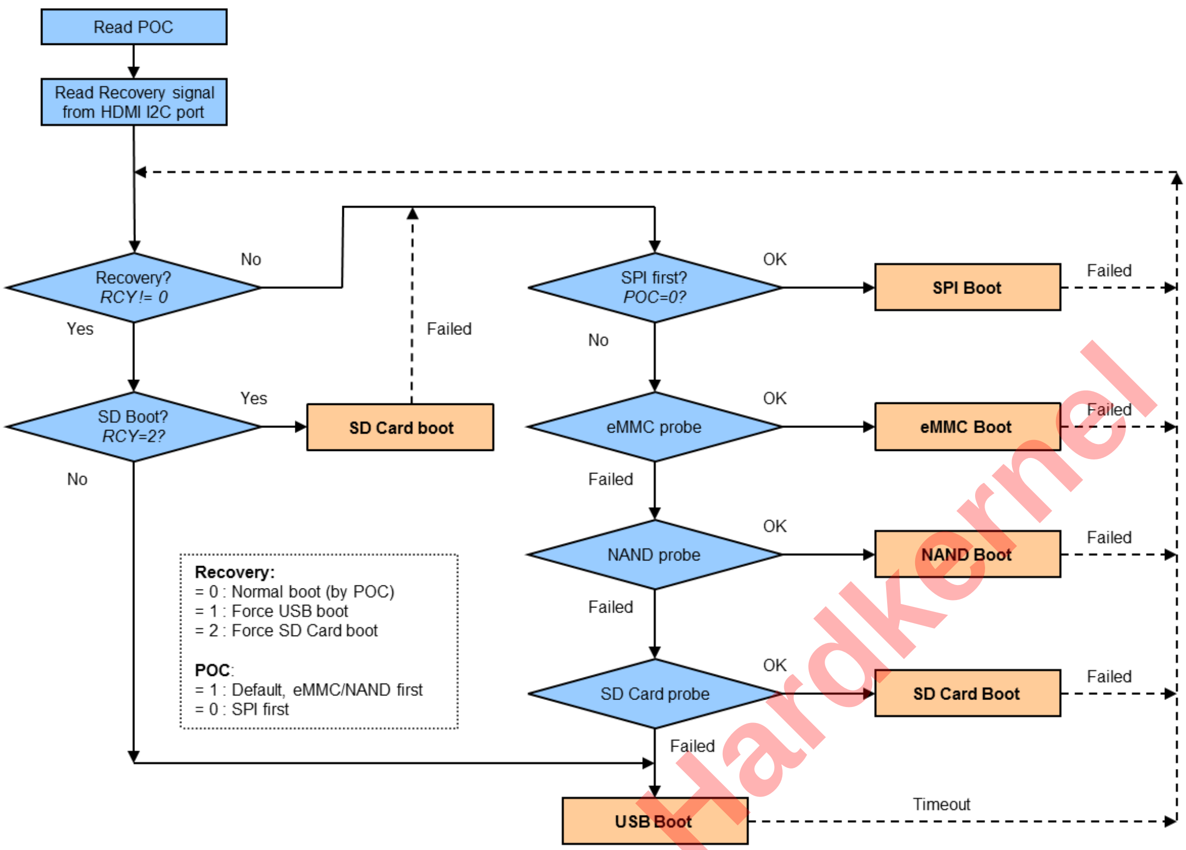
19.1 Overview

The part describes the power–on mode configuration of S905, which include two portions: Cortex-M3 for security control and A53 for others.

19.2 Power-on Flow Chart

Fig22.1 illustrates S905's power on sequence.

Fig III.19.1 Power-on Flow Chart



20. CPU

20.1 Overview

The Cortex™-A53 MP subsystem of the chip is a high-performance, low-power, ARM macrocell with an L1 cache subsystem and an L2 cache subsystem that provide full virtual memory capabilities. The Cortex-A53 processor implements the ARMv8 architecture and runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions and 64 bit ARMv8 instructions. The developers can follow the ARM official reference documents for programming details.

The Cortex-A53 processor features are:

- in-order pipeline with dynamic branch prediction
- ARM, Thumb, and ThumbEE instruction set support
- TrustZone security extensions
- Harvard level 1 memory system with a Memory Management Unit (MMU)
- 128-bit AXI master interface
- ARM CoreSight debug architecture
- trace support through an Embedded Trace Macrocell (ETMv4) interface
- Intelligent Energy Manager (IEM) support with
  - asynchronous AXI wrappers
  - two voltage domains
- Media Processing Engine (MPE) with NEON technology
- Surpports FPU
- Surpports Hardware Virtualization

21. GPU

The Mali-450 MP GPU is a hardware accelerator for 2D and 3D graphics system which compatible with the following graphics standards: OpenGL ES 2.0, OpenGL ES 1.1, OpenVG 1.1, EGL 1.5. The developers can follow the ARM and Khronos official reference documents for programming details.

22. Clock and Reset

22.1 Overview

The clock and reset unit is an APB slave module that is designed for generating all of the internal and system clocks, resets of chip.

22.2 Clock Trees

FigIII. 22.1 shows the PLLs of S905.

FigureIII.22.1 PLLs

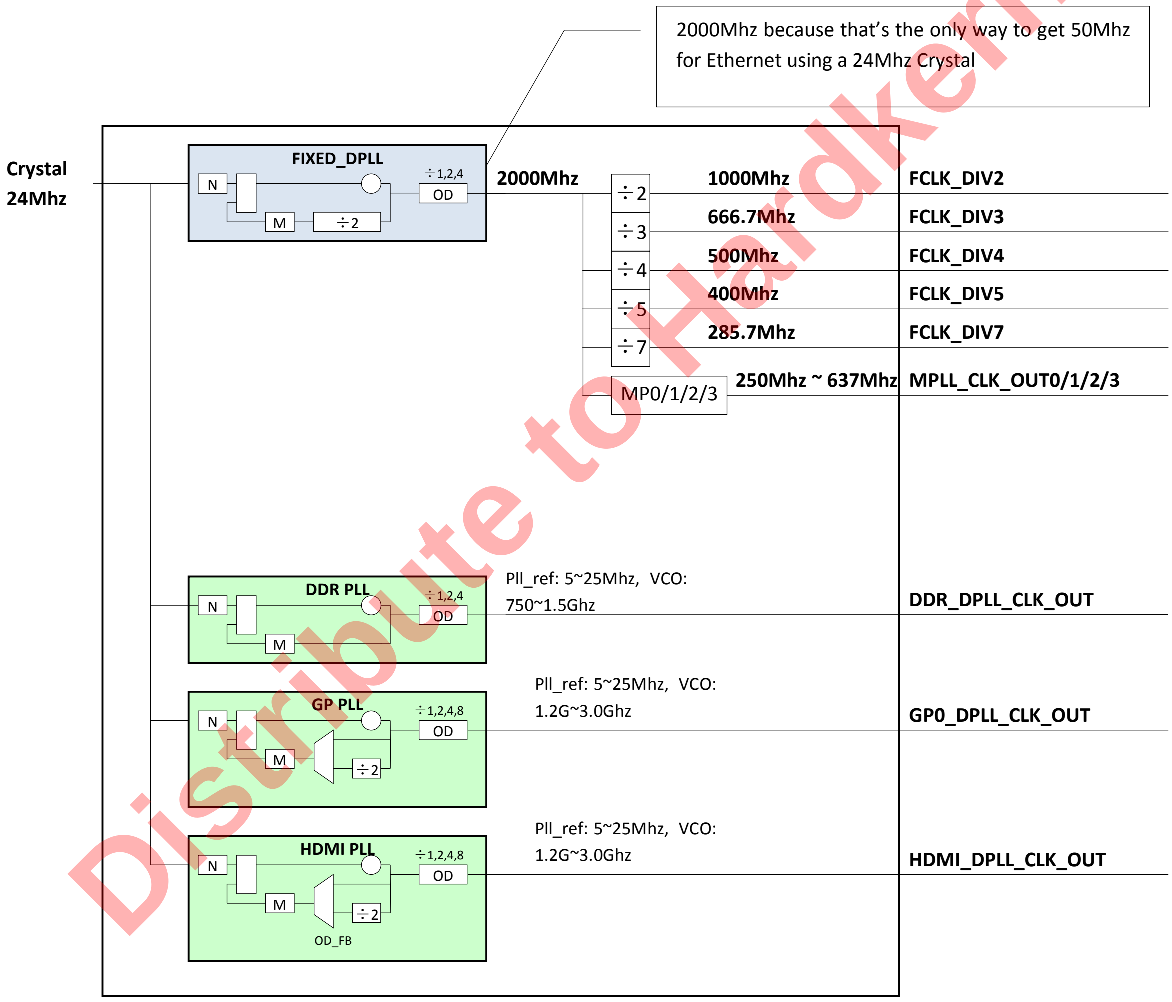


Table III.22.1 Integer PLL Parameters

Integer PLL	F-Ref Min (XTAL/N)	F-Ref Max (XTAL/N)	N-bits	M-bits	OD Bits	VCO MIN	VCO MAX	OD divider
DDR_DPLL	5 Mhz	30 Mhz	5	9	2	750Mhz	1.5Ghz	2-bits: ÷1, ÷2, ÷4
VID_DPLL	5 Mhz	30 Mhz	5	9	2	1.2Ghz	3.0Ghz	2-bits: ÷1, ÷2, ÷4, ÷8
HDMI_DPLL (VIID_DPLL)	5 Mhz	30 Mhz	5	9	2	1.2Ghz	3.0Ghz	OD: ÷1, ÷2, ÷4, ÷8 FB: ÷1, ÷2 LVDS: ÷1, ÷2, ÷4, ÷8
FIXED_DPLL	5 Mhz	30 Mhz	5	9	1	1Ghz	2Ghz	

Fig III.22.2 Mutil Phase PLLS

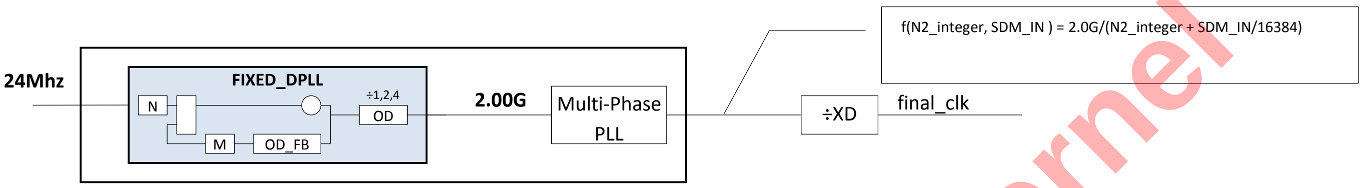


Table III.22.2 Multi-Phase PLL Parameters

Multi-Phase	N2_integer [Min]	N2_integer [Max]	SDM_IN [Min]	SDM_IN [Max]	Fout [Min]	Fout [Max]
MP0_DPLL	4	127	1	16383	5 Mhz	500Mhz
MP1_DPLL	4	127	1	16383	5 Mhz	500Mhz
MP2_DPLL	4	127	1	16383	5 Mhz	500Mhz

Table III.22.3 Direct Divide Frequencies (assuming 2.000 GHz fixed source clock)

Target Frequency	Effective Divider from 2.550Ghz	PLL_DIV3 850Mhz	PLL_DIV4 637.5	PLL_DIV5 510	PLL_DIV7 364Mhz
666.6667	3	÷1			
500	4		÷1		
400	5			÷1	
333.3333	6	÷2			
285.7143	7				÷1
250	8		÷2		
222.2222	9	÷3			
200	10			÷2	
166.6667	12	÷4	÷3		
142.8571	14				÷2
133.3333	15	÷5		÷3	
125	16		÷4		
111.1111	18	÷6			
100	20		÷5	÷4	
95.2381	21	÷7			÷3
83.33333	24	÷8	÷6		
80	25			÷5	
74.07407	27	÷9			
71.42857	28		÷7		÷4
66.66667	30	÷10		÷6	
62.5	32		÷8		
60.60606	33	÷11			
57.14286	35			÷7	÷5
55.55556	36	÷12	÷9		
51.28205	39	÷13			
50	40		÷10	÷8	÷6
47.61905	42	÷14			
45.45455	44		÷11		

44.44444	45	÷15		÷9	
41.66667	48	÷16	÷12		
40.81633	49				÷7
40	50			÷10	
39.21569	51	÷17			

Table III.22.4 Audio Frequencies (using Multi-phase PLL)

Sampling Frequency	Over Sampling	Target freq [Mhz]	N2_integer	SDM_IN	Divider in clk_rst_tst	final_clk [Mhz]	Error
7875 Hz	256	2.016	7	13296	127	2.016	0.00%
7875 Hz	384	3.024	8	9655	77	3.024	0.00%
8000 Hz	256	2.048	7	13312	125	2.048	0.00%
8000 Hz	384	3.072	7	9343	86	3.072	0.00%
11025 Hz	256	2.8224	8	2376	87	2.822	0.00%
11025 Hz	384	4.2336	7	12197	61	4.234	0.00%
12000 Hz	256	3.072	7	9343	86	3.072	0.00%
12000 Hz	384	4.608	6	7832	67	4.608	0.00%
16000 Hz	256	4.096	4	14464	100	4.096	0.00%
16000 Hz	384	6.144	7	9343	43	6.144	0.00%
22050 Hz	256	5.6448	4	1188	87	5.645	0.00%
22050 Hz	384	8.4672	4	1188	58	8.467	0.00%
24000 Hz	256	6.144	7	9343	43	6.144	0.00%
24000 Hz	384	9.216	4	1550	53	9.216	0.00%
32000 Hz	256	8.192	4	14464	50	8.192	0.00%
32000 Hz	384	12.288	7	1254	23	12.288	0.00%
44100 Hz	256	11.2896	4	3571	42	11.290	0.00%
44100 Hz	384	16.9344	4	1188	29	16.934	0.00%
48000 Hz	256	12.288	7	1254	23	12.288	0.00%
48000 Hz	384	18.432	4	2840	26	18.432	0.00%
96000 Hz	256	24.576	6	4260	13	24.576	0.00%
96000 Hz	384	36.864	4	2840	13	36.864	0.00%
192000 Hz	256	49.152	4	8538	9	49.152	0.00%
192000 Hz	384	73.728	4	8538	6	73.728	0.00%

Ethernet Frequencies:

- 10/100 Ethernet: 50Mhz
- 10/100/1000 Ethernet: 125Mhz and 25Mhz

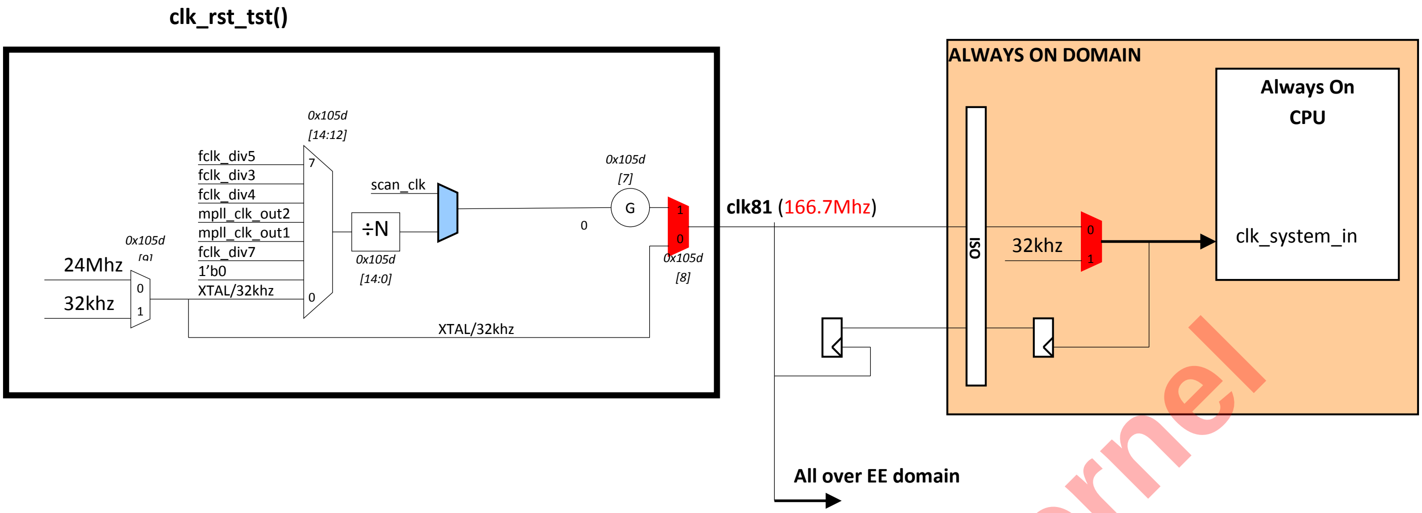
USB Frequencies:

- 19.2, 20, 24, 50Mhz

HDMI Frequencies:

- Min: 250Mhz (at the PHY) 25Mhz to the logic
- Max: 5.94Ghz at the PHY (4k2k)

Fig III.22.3 N Frenquency Divider Diagram



22.3 Clock Gating

Modules and sub-modules within the chip can be disabled by shutting off the clock. The control for these clocks comes from six CBUS registers that collectively make up a 64-bit register that controls the MPEG_DOMAIN and a32-bit register that controls the OTHER_ DOMAIN. The table below indicates the Bits associated with either the MPEG_DOMAIN and OTHER_DOMAIN gated clock enables. The table is organized by function rather than by bit order because it makes it easier to determine how to turn on/off a particular function within the chip. If a bit is set high, the clock is enabled. If a bit is set low, the clock is turned off and the module is disabled.

Table III. 22.5 AO Domain Clock Gating

Final address = 0xc8834400 + offset * 4

Module	address	Bit(s)	Module Description
CBUS	0x55	31-5	Unused
		4	Ao_i2c
		3	Always on Registers, timers,…
		2	AHB bus in the always on domain
		1	AHB SRAM
		0	AO CPU

Table III.22.6 EE Domain Clock Gating

Final address = 0xc8834400 + offset * 4

Module	address	Bit(s)	Module Description
	0x50	31	Reserved
PERIPHS		30	SPI Interface
		29	Reserved
		28	Reserved
		27	Reserved
		26	Reserved
		25	Reserved
		24	Reserved
ASSIST		23	ASSIST_MISC
		22	Reserved

Module	address	Bit(s)	Module Description
		21	Reserved
		20	Reserved
HIU		19	HIU Registers
ABUF		18	Audio Buffer u_abuf_top.HCLK
PERIPHS		17	SDIO
PERIPHS		16	ASYNC_FIFO
PERIPHS		15	STREAM Interface
PERIPHS		14	SDHC
PERIPHS		13	UART0
PERIPHS		12	Random Number generator
PERIPHS		11	Smart Card
PERIPHS		10	SAR ADC
PERIPHS		9	I2C Master / I2C SLAVE
PERIPHS		8	SPICC
PERIPHS		7	PERIPHS module top level (there are separate register Bits for internal blocks)
DDR		6	PL301 (AXI Matrix) to CBUS
ISA		5	ISA module
		4	Reserved
		3	Reserved
		2	Reserved
DOS (MDEC)		1	u_dos_top()
DDR		0	DDR Interfaces and bridges
MISC	0x51	31	ROM BOOT ROM clock
MISC		30	EFUSE logic
MISC		29	AHB ARB0
VIU		28	VDIN1
		27	
USB		26	USB General
DOS		25	U_parser_top()
PERIPHS		24	NAND Interface
MISC		23	RESET
USB		22	USB 1
USB		21	USB 0
GE2D		20	General 2D Graphics Engine
		19	Reserved
		18	Reserved
		17	Reserved
PERIPHS		16	UART1
AIU		15	AIU Top level (there is internal gating shown below)
BLKMV		14	Block move core logic
AIU		13	ADC

Module	address	Bit(s)	Module Description
AIU		12	Mixer Registers: u_ai_top.u_mixer_reg.clk
AIU		11	Mixer: u_ai_top.u_aud_mixer.clk
AIU		10	AIFIFO2: u_ai_top.u_aififo2.clk
AIU		9	AMCLK measurement circuit
AIU		8	I2S Out: This bit controls the clock to the logic between the DRAM control unit and the FIFO's that transfer data to the audio clock domain. (u_ai_top.I2S_fast.clk)
AIU		7	IEC958: iec958_fast()
AIU		6	AIU – ai_top_glue u_ai_top.ai_top_glue.clk u_ai_top.fifo_async_fast_I2S.clk u_ai_top.fifo_async_fast_958.clk
		5	
DEMUX		4	Set top box demux moduleu_stb_top.clk
ETHERNET		3	Ethernet core logic
AUDIN		2	I2S / SPDIF Input
		1	Reserved
		0	Reserved
	0x52	31	Reserved
		30	Reserved
MISC		29	CLK81 to the A53 domain
		28	Reserved
		27	Reserved
AHB		26	Secure AHB to APB3 Bridge
VPU		25	VPU Interrupt
		24	Reserved
		23	Reserved
PERIPHS		22	SANA
		21	Reserved
		20	Reserved
		19	Reserved
		18	Reserved
		17	Reserved
		16	Reserved
PERIPHS		15	UART 2
		13	Reserved
MISC		12	DVIN
DDR		11	MMC PCLK
		10	Reserved
USB		9	USB0 to DDR bridge
USB		8	USB1 to DDR bridge
		7	Reserved

Module	address	Bit(s)	Module Description
		6	Reserved
		5	Reserved
HDMI		4	HDMI PCLK
HDMI		3	HDMI interrupt synchronization
MISC		2	AHB control bus
MISC		1	AHB data bus
		0	Reserved
EDP	0x54	31	Video clock enable
		30	Reserved
		29	Reserved
		28	Reserved
		27	Reserved
VENC		26	VCLK2_OTHER
VENC		25	VCLK2_VENCL
VENC		24	VCLK2_VENCLMMC Clock All
		23	Reserved
VENC		22	gclk_vencl_int
PERIPH		21	Random Number Generator
VENC		20	ENC480P
		19	Reserved
		18	Reserved
		17	Reserved
AIU		16	IEC958_GATE
		15	Reserved
AIU		14	AOCLK_GATE
		13	Reserved
		12	Reserved
		11	Reserved
VENC		10	DAC_CLK
VENC		9	gclk_vencp_int
VENC		8	gclk_venci_int
		7	Reserved
		6	Reserved
		5	Reserved
VENC		4	VCLK2_VENCP
VENC		3	VCLK2_VENCP
VENC		2	VCLK2_VENCI for venc_i_top other normal function
VENC		1	VCLK2_VENCI for venc_i_top BIST function
		0	Reserved

22.4 Register Description

Each register's final address = 0xC883C000 + offset * 4

SCR System Clock Reference 0x0B

Bit(s)	R/W	Default	Description
31-0	R/W	0	System clock reference high: Bits 31:16

TIMEOUT_VALUE: Program timer 0x0F

Bit(s)	R/W	Default	Description
15-12	R	0	Unused
11-0	R/W	0	Program timer

Increased by 1 every 900 cycles. Triggers timer interrupt to CPU when it expires.

HHI_GP0_PLL_CNTL 0x10

Bit(s)	R/W	Default	Description
31	R	0	LOCK
30	R/W	0	ENABLE
29	R/W	0	RESET
28~18	R/W	0	Reserved
17~16	R/W	0	OD
15~14	R/W	0	Reserved
13~9	R/W	0	N
8~0	R/W	0	M

HHI_GP0_PLL_CNTL2 0x11

Bit(s)	R/W	Default	Description
31~28	R/W	0	DPLL_LM_W
27~22	R/W	0	DPLL_LM_S
21	R/W	0	DPLL_DPFD_LMODE
20~19	R/W	0	DC_VC_IN
18~17	R/W	0	DCO_SDMCK_SEL
16	R/W	0	DCO_M_EN
15	R/W	0	Reserved
14	R/W	0	Reserved
13	R/W	0	AFC_DSEL_BYPASS
12	R/W	0	AFC_DSEL_IN
11~0	R/W	0	Reserved

HHI_GP0_PLL_CNTL3 0x12

Bit(s)	R/W	Default	Description
31~30	R/W	0	Reserved
29~26	R/W	0	FILTER_PVT2
25~22	R/W	0	FILTER_PVT1
21~11	R/W	0	FILTER_ACQ2
10~0	R/W	0	FILTER_ACQ1

HHI_GP0_PLL_CNTL4 0x13

Bit(s)	R/W	Default	Description
31~26	R/W	0	Reserved
25~24	R/W	0	DCO_IUP
23~16	R/W	0	TDC_BUF
15~4	R/W	0	REVE
3	R/W	0	PVT_FIX_EN
2	R/W	0	DCO_SDM_EN
1	R/W	0	IIR_BYPASS_N
0	R/W	0	TDC_EN

HHI_XTAL_DIVN_CNTL 0x2f

Bit(s)	R/W	Default	Description
31~20	R/W	0	reserved
19	R/W	0	gpioCLK_3_xtal
18	R/W	0	gpioCLK_3_xtal_2
17	R/W	0	reserved
16	R/W	0	reserved
15	R/W	0	gpioCLK_2_xtal_2
14	R/W	0	gpioCLK_2_xtal
13	R/W	0	reserved
12	R/W	0	gpioCLK_1_fclk_div2
11	R/W	0	gpioCLK_1_xtal_2
10	R/W	0	gpioCLK_1_xtal
9	R/W	0	reserved
8	R/W	0	Fclk_div2_gclk_en
7~0	R/W	0	Fclk_div2_tcnt

HHI_TIMER90K 0x3B

Bit(s)	R/W	Default	Description
31-16	R/W	0	Unused
15-0	R/W	0x384	90khz divider

HHI_MEM_PD_REG0 0x40

Bit(s)	R/W	Default	Description
31~16	R/W	0xFFFFFFFF	Reserved
15~8	R/W	0xFF	HDMI memory PD
7~4	R/W	0xF	Reserved
3~2	R/W	0x3	Ethernet memory PD
1~0	R/W	0x3	Reserved

HHI_VPU_MEM_PD_REG0: 0x41

Bit(s)	R/W	Default	Description
31~30	R/W	0x3	Reserved
29~28	R/W	0x3	Deinterlacer – di_post: 11 = power down. 00 = normal operation
27~26	R/W	0x3	Deinterlacer – di_pre
25~24	R/W	0x3	Picture rotation3
23~22	R/W	0x3	Picture rotation2
21~20	R/W	0x3	Picture rotation1
19~18	R/W	0x3	Vdin1 memory
17~16	R/W	0x3	Vdin0 memory
15~14	R/W	0x3	Osd_scaler
13~12	R/W	0x3	Scaler memory
11~10	R/W	0x3	Vpp output fifo
9~8	R/W	0x3	Color management module
7~6	R/W	0x3	Vd2 memory
5~4	R/W	0x3	Vd1 memory
3~2	R/W	0x3	Osd2 memory
1~0	R/W	0x3	Osd1 memory

HHI_VPU_MEM_PD_REG1: 0x42

Bit(s)	R/W	Default	Description
31~30	R/W	0x3	Reserved
29~28	R/W	0x3	Reserved
27~26	R/W	0x3	ISP memory: 11 = power down. 00 = normal operation
25~24	R/W	0x3	CVBS inci interface
23~22	R/W	0x3	Panel encl top

Bit(s)	R/W	Default	Description
21~20	R/W	0x3	Hdmi encp interface
19~18	R/W	0x3	Reserved
17~16	R/W	0x3	Reserved
15~14	R/W	0x3	Reserved
13~12	R/W	0x3	VIU2 OSD scaler
11~10	R/W	0x3	VIU2 scaler
9~8	R/W	0x3	VIU2 VPP
7~6	R/W	0x3	VIU2 color management
5~4	R/W	0x3	VIU2 VD1
3~2	R/W	0x3	VIU2 OSD2
1~0	R/W	0x3	VIU2 OSD1

HHI_VIID_CLK_DIV 0x4a

Bit(s)	R/W	Default	Description
31-28	R/W	0	DAC0_CLK_SEL
27-24	R/W	0	DAC1_CLK_SEL
23-20	R/W	0	DAC2_CLK_SEL
19	R/W	0	Select adc_pll_clk_b2 to be cts_clk_vdac
18	R/W	0	Unused
17	R/W	0	V2_cntl_clk_div_reset
16	R/W	0	V2_cntl_clk_div_en
15-12	R/W	0	Encl_clk_sel
14-8	R/W	0	Unused
7-0	R/W	0	V2_cntl_xd0

HHI_VIID_CLK_CNTL 0x4b

Bit(s)	R/W	Default	Description
31-20	R/W	0	Unused
19	R/W	0	V2_cntl_clk_en0
18-16	R/W	0	V2_cntl_clk_in_sel
15	R/W	0	V2_cntl_soft_reset
14-5	R/W	0	Unused
4	R/W	0	V2_cntl_div12_en
3	R/W	0	V2_cntl_div6_en
2	R/W	0	V2_cntl_div4_en
1	R/W	0	V2_cntl_div2_en
0	R/W	0	V2_cntl_div1_en

HHI_GCLK_MPEG0 0x50

Bit(s)	R/W	Default	Description
31-0	R/W	0	Bits [31:0] of the composite MPEG clock gating register

HHI_GCLK_MPEG1 0x51

Bit(s)	R/W	Default	Description
31-0	R/W	0	Bits [63:32] of the composite MPEG clock gating register

HHI_GCLK_MPEG2 0x52

Bit(s)	R/W	Default	Description
31-0	R/W	0	Bits [63:32] of the composite MPEG clock gating register

HHI_GCLK_OTHER 0x54

Bit(s)	R/W	Default	Description
31-0	R/W	0	Bits [31:0] of the composite Other clock gating register

HHI_GCLK_AO 0x55

Bit(s)	R/W	Default	Description
31-8	R	0	Unused
7-5	R/W	0x7	unused
4	R/W	1	i2c
3	R/W	1	Always On Register logic
2	R/W	1	Always on general clock in the always on domain
1	R/W	1	AHB SRAM
0	R/W	1	AO CPU

HHI_SYS_OSCIN_CNTL 0x56

Bit(s)	R/W	Default	Description
31-16	R	0	Unused
15	R/W	1	Padu_sys_osc_en
14-0	R/W	0x7FFF	Xtal_source_en[14:0]

HHI_SYS_CPU_CLK_CNTL1 0x57

Bit(s)	R/W	Default	Description
31-24	R/W	0	Reserved
23	R/W	0	A53_trace_clk _DIS: Set to 1 to manually disable the A53_trace_clk when changing the mux selection. Typically This bit is set to 0 since the clock muxes can switch without glithces. This is a “just in case” bit
22:20	R/W	0	A53_trace_clk: 1. A53 clock divided by 2 2. A53 clock divided by 3 3. A53 clock divided by 4 4. A53 clock divided by 5 5. A53 clock divided by 6 6. A53 clock divided by 7 7. A53 clock divided by 8
19	R/W	0	
18	R/W	0	AXI_CLK_DIS: Set to 1 to manually disable the AXI clock when changing the mux selection. Typically This bit is set to 0 since the clock muxes can switch without glithces. This is a “just in case” bit
17	R/W	0	
16	R/W	0	APB_CLK_DIS: Set to 1 to manually disable the APB clock when changing the mux selection. Typically This bit is set to 0 since the clock muxes can switch without glithces. This is a “just in case” bit
15	R/W	0	Reserved
14~12	R/W	0	Reserved
11~9	R/W	0	AXI_CLK _MUX: 8. A53 clock divided by 2 9. A53 clock divided by 3 10. A53 clock divided by 4 11. A53 clock divided by 5 12. A53 clock divided by 6 13. A53 clock divided by 7 14. A53 clock divided by 8
8~6	R/W	0	Reserved
5~3	R/W	0	APB_CLK _MUX: 1. A53 clock divided by 2 2. A53 clock divided by 3 3. A53 clock divided by 4 4. A53 clock divided by 5 5. A53 clock divided by 6 6. A53 clock divided by 7 7. A53 clock divided by 8
2	R/W	0	Soft_reset
1	R/W	0	Div16_en
0	R/W	0	Pclk_en_dbg

HHI_SYS_CPU_RESET_CNTL 0x58

Bit(s)	R/W	Default	Description
31-11	R/W	0	Reserved
10	R/W	0	Cpu_axi_reset
9	R/W	0	nPRESETDBG

Bit(s)	R/W	Default	Description
8	R/W	0	nL2RESET
7-4	R/W	0	nCORERESET[3:0]
3-0	R/W	0	Cpu_soft_reset[3:0]

HHI_VID_CLK_DIV 0x59

Bit(s)	R/W	Default	Description
31-28	R/W	0	ENCI_CLK_SEL
27-24	R/W	0	ENCP_CLK_SEL
23-20	R/W	0	ENCT_CLK_SEL
19-18	R/W	0	UNUSED
17	R/W	0	CLK_DIV_RESET
16	R/W	0	CLK_DIV_EN
15-8	R/W	0	XD1
7-0	R/W	0	XD0

HHI_MPEG_CLK_CNTL 0x5d

Bit(s)	R/W	Default	Description
31	R/W	0	NEW_DIV_EN: If This bit is set to 1, then Bits[30:16] make up the clk81 divider. If This bit is 0, then Bits[6:0] dictate the divider value. This is a new feature that allows clk81 to be divided down to a very slow frequency.
30~16	R/W	0	NEW_DIV: New divider value if Bit[31] = 1
15	R/W	0	Production clock enable
14-12	R.W	6	MPEG_CLK_SEL (See clock document)
11-10	R/W	0	unused
9	R.W	0	RTC Oscillator Enable: Set This bit to 1 to connect the RTC 32khz oscillator output as the XTAL input for the divider above
8	R/W	0	Divider Mux: 0 = the ao cpu clock and the MPEG system clock are connected to the 27Mhz crystal. 1 = the ao cpu clock and the MPEG system clock are connected to the MPEG PLL divider
7	R/W	1	PLL Mux: 0 = all circuits associated with the MPEG PLL are connected to 27Mhz. 1 = all circuits associated with the MPEG PLL are connected to the MPEG PLL
6-0	R/W	0	PLL Output divider. The MPEG System clock equals the video PLL clock frequency divided by (N+1). Note: N must be odd (1,3,5,….) so that the MPEG clock is divided by an even number to generate a 50% duty cycle.

HHI_AUD_CLK_CNTL 0x5e

Bit(s)	R/W	Default	Description
31-26	R/W	0	Unused
25-24	R/W	0	Audio DAC clock select (See clock document)
23	R/W	0	Audio DAC Clock enable
22-16	R/W	0	Audio DAC Clock divider
15-11	R/W	0	Unused
10-9	R/W	0	AMCLK_SRC_SEL: (see clock tree document)
8	R/W	0	PLL Clock Enable. Set This bit to 1 to enable the PLL to the rest of the logic. To avoid glitching state machines inside the chip please change the PLL using the following sequence: • Set Bit[8] = 0 to block the logic from the PLL • set the PLL using register 0x15b and wait for the PLL to settle (1mS) • Set Bit[8] = 1 to enable the PLL driving all of the logic
7-0	R/W	1	PLL Output divider. The Audio System clock equals the video PLL clock frequency divided by (N+1).

HHI_VID_CLK_CNTL 0x5f

Bit(s)	R/W	Default	Description
31-21	R/W	0	TCON_CLK0_CTRL
20	R/W	0	CLK_EN1
19	R/W	0	CLK_EN0
18-16	R/W	0	CLK_IN_SEL
15	R/W	0	SOFT_RESET
14	R/W	0	PH23_ENABLE
13	R/W	0	DIV12_PH23

Bit(s)	R/W	Default	Description
12-5	R/W	0	UNUSED
4	R/W	0	DIV12_EN
3	R/W	0	DIV6_EN
2	R/W	0	DIV4_EN
1	R/W	0	DIV2_EN
0	R/W	0	DIV1_EN

HHI_AUD_CLK_CNTL2 0x64

Bit(s)	R/W	Default	Description
31-28	R/W	0	Unused
27	R/W	0	IEC958_USE_CNTL: If This bit is set to 1, then Bits[26;16] are used as the IEC958 clock divider
26-25	R/W	0	IEC958_CLK_SRC_SEL. See the clock tree document
23-16	R/W	0	IEC958_CLK_DIV.
15-0	R/W	0	Reserved

HHI_VID_CLK_CNTL2 0x65

Bit(s)	R/W	Default	Description
31-16	R	0	
15-9	R/W	0	Reserved
8	R/W	0	Atv demod vdac gated clock control
7	R/W	1	LCD_AN_CLK_PHY2 gated clock control. 1 = enable
6	R/W	1	LCD_AN_CLK_PH3 gated clock control
5	R/W	1	HDMI_TX_PIXEL_CLK gated clock control
4	R/W	1	VDAC_clk gated clock control
3	R/W	1	ENCL gated clock control
2	R/W	1	ENCP gated clock control
1	R/W	1	ENCT gated clock control
0	R/W	1	ENCI gated clock control

HHI_SYS_CPU_CLK_CNTL0 0x67

Bit(s)	R/W	Default	Description
31	R	0	Final_mux_sel
30	R	0	Final_dyn_mux_sel
29	R	0	Busy_cnt
28	R	0	busy
26	R/W	0	Dyn_enable
25-20	R/W	0	Mux1_divn_tcnt
18	R/W	0	Postmux1
17-16	R/W	0	Premux1
15	R/W	0	Manual_mux_mode
14	R/W	0	Manual_mode_post
13	R/W	0	Manual_mode_pre
12	R/W	0	Force_update_t
11	R/W	0	Final_mux_sel
10	R/W	0	Final_dyn_mux_sel
9-4	R/W	0	mux0_divn_tcnt
3	R/W	0	Rev
2	R/W	0	Postmux0
1-0	R/W	0	Premux0

HHI_VID_PLL_CLK_DIV 0x68

Bit(s)	R/W	Default	Description
31~24	R	0	RESERVED
23~20	R/W	0	Reserved
19	R/W	0	CLK_FINAL_EN
18	R/W	0	CLK_DIV1
17~16	R/W	0	CLK_SEL

Bit(s)	R/W	Default	Description
15	R/W	0	SET_PRESET
14-0	R/W	0	SHIFT_PRESET

HHI_AUD_CLK_CNTL3 0x69

Bit(s)	R/W	Default	Description
31-29	R/W	0	Unused
18:17	R/W	0	Pdm_clk_src_sel: 0:cts_amclk 1:mp0_clk_out 2:mp1_clk_out 3:mp2_clk_out
16	R/W	0	Pdm_clk_en
15-0	R/W	0	Pdm_clk_div

HHI_MALI_CLK_CNTL 0x6c

Bit(s)	R/W	Default	Description
31-28	R/W	0	Reserved
27~25	R/W	0	CLK_SEL: See the Clock Tree document for information related to cts_mali _clk
24	R/W	0	CLK_EN: See the Clock Tree document for information related to cts_ mali _clk
23	R/W	0	Reserved
22~16	R/W	0	CLK_DIV: See the Clock Tree document for information related to cts_ mali _clk
15~12			
11~9	R/W	0	CLK_SEL: See the Clock Tree document for information related to cts_mali _clk
8	R/W	0	CLK_EN: See the Clock Tree document for information related to cts_ mali _clk
7	R/W	0	Reserved
6-0	R/W	0	CLK_DIV: See the Clock Tree document for information related to cts_ mali _clk

HHI_VPU_CLK_CNTL 0x6f

Bit(s)	R/W	Default	Description
31	R/W	0	Final mux sel
30-29	R/W	0	Reserved
28	R/W	0	TVFE MCLK EN
27~25	R/W	0	CLK_SEL: See the Clock Tree document for information related to cts_vpu_clk
24	R/W	0	CLK_EN: See the Clock Tree document for information related to cts_vpu_clk
23	R/W	0	Reserved
22~16	R/W	0	CLK_DIV: See the Clock Tree document for information related to cts_vpu_clk
15~12			
11~9	R/W	0	CLK_SEL: See the Clock Tree document for information related to cts_vpu_clk
8	R/W	0	CLK_EN: See the Clock Tree document for information related to cts_vpu_clk
7	R/W	0	Reserved
6-0	R/W	0	CLK_DIV: See the Clock Tree document for information related to cts_vpu_clk

HHI_HDMI_CLK_CNTL 0x73

Bit(s)	R/W	Default	Description
31-20	R/W	0	Reserved
19~16	R/W	0	crt_hdmi_pixel_clk_sel
15~11	R/W	0	Reserved
10~9	R/W	0	CLK_SEL: See the Clock Tree document for information related to cts_hdmi_sys_clk
8	R/W	0	CLK_EN: See the Clock Tree document for information related to cts_hdmi_sys_clk
7	R/W	0	Reserved
6-0	R/W	0	CLK_DIV: See the Clock Tree document for information related to cts_hdmi_sys_clk

HHI_VDEC_CLK_CNTL 0x78

Bit(s)	R/W	Default	Description
31-28	R/W	0	Reserved
27~25	R/W	0	CLK_SEL: See the Clock Tree document for information related to cts_hcodec_clk

Bit(s)	R/W	Default	Description
24	R/W	0	CLK_EN: See the Clock Tree document for information related to cts_hcodec_clk
23	R/W	0	Reserved
22~16	R/W	0	CLK_DIV: See the Clock Tree document for information related to ctshcodec_clk
15~12	R/W	0	Reserved
11~9	R/W	0	CLK_SEL: See the Clock Tree document for information related to cts_vdec_clk
8	R/W	0	CLK_EN: See the Clock Tree document for information related to cts_vdec_clk
7	R/W	0	Reserved
6-0	R/W	0	CLK_DIV: See the Clock Tree document for information related to cts_vdec_clk

HHI_VDEC2_CLK_CNTL 0x79

Bit(s)	R/W	Default	Description
31-28	R/W	0	Reserved
27~25	R/W	0	HEVC_CLK_SEL: See the Clock Tree document for information related to cts_vdec2_clk
24	R/W	0	HEVC_CLK_EN: See the Clock Tree document for information related to cts_vdec2_clk
23	R/W	0	Reserved
22~16	R/W	0	HEVC_CLK_DIV: See the Clock Tree document for information related to cts_vdec2_clk
15~12			
11~9	R/W	0	VDEC2_CLK_SEL: See the Clock Tree document for information related to cts_vdec2_clk
8	R/W	0	VDEC2_CLK_EN: See the Clock Tree document for information related to cts_vdec2_clk
7	R/W	0	Reserved
6-0	R/W	0	VDEC2_CLK_DIV: See the Clock Tree document for information related to cts_vdec2_clk

HHI_VDEC3_CLK_CNTL 0x7a

Bit(s)	R/W	Default	Description
31~0	R/W	0	See the clock tree document. This register controls the Alternate clock for cts_vdec_clk and cts_hcodec_clk

HHI_VDEC4_CLK_CNTL 0x7b

Bit(s)	R/W	Default	Description
31-0	R/W	0	See the clock tree document. This register controls the Alternate clock for cts_vdec2_clk and cts_hevc_clk

HHI_HDCP22_CLK_CNTL 0x7c

Bit(s)	R/W	Default	Description
31-0	R/W	0	Reserved
26-25	R/W	0	Clk_sel: 0:cts_oscin_clk 1:fclk_div4 2:fclk_div3 3:fclk_div5
24	R/W	0	Clk_en
23-0	R/W	0	Clk_div

HHI_VAPBCLK_CNTL 0x7d

Bit(s)	R/W	Default	Description
31	R/W	0	Final_mux_sel
30	R/W	0	Enable
29-28	R/W	0	Reserved
27-25	R/W	0	Mux1_sel: 0:fclk_div4 1:fclk_div3 2:fclk_div5 3:fclk_div7 4:mp1_clk_out 5:vid_pll_clk 6:mp2_clk_out 7:gp0_pll_clk
24	R/W	0	Mux1_en
23	R/W	0	Reserved

Bit(s)	R/W	Default	Description
22-16	R/W	0	Mux1_div
15-12	R/W	0	Reserved
11-9	R/W	0	Mux0_sel,as mux1_sel
8	R/W	0	Mux0_en
7	R/W	0	Reserved
6-0	R/W	0	Mux0_div

HHI_VPU_CLKB_CNTL 0x83

Bit(s)	R/W	Default	Description
31-9	R/W	0	Reserved
8	R/W	0	Vpu_clkb_en
7-0	R/W	0	Vpu_clkb_div

HHI_USB_CLK_CNTL0x88

Bit(s)	R/W	Default	Description
31-0	R/W	0	Reserved
11-10	R/W	0	Usb_clk_sel: 0:cts_oscin_clk 1:rtc_oscin_i
9	R/W	0	Usb_clk_en
8-0	R/W	0	Usb_clk_div

HHI_32K_CLK_CNTL 0x89

Bit(s)	R/W	Default	Description
31-0	R/W	0	Reserved
17-16	R/W	0	Hi_32k_clk_sel: 0:cts_oscin_clk 1:cts_slow_oscin_clk 2:fclk_div3 3:fclk_div5
15	R/W	0	Hi_32k_clk_en
14	R/W	0	Reserved
13-0	R/W	0	Hi_32k_clk_div

HHI_GEN_CLK_CNTL 0x8a

Bit(s)	R/W	Default	Description
31-17	R/W	0	Reserved
16	R/W	0	OSCIN GATE CLK ENABLE
15~12	R/W	0	CLK_SEL: 0:cts_oscin_clk 1:rtc_oscin_i 2:sys_cpu_clk_div16 3:ddr_dpll_pt_clk 4:vid_pll_clk 5:vid2_pll_clk 6:mp0_clk_out 7:mp1_clk_out 8:mp2_clk_out 9:fclk_div4 10:fclk_div3 11:fclk_div5 12:cts_msr_clk 13:fclk_div7 14:gp0_pll_clk
11	R/W	0	CLK_EN: See the Clock Tree document for information related to gen_clk_out
10~0	R/W	0	CLK_DIV: See the Clock Tree document for information related to gen_clk_out

HHI_PCM_CLK_CNTL 0x96

Clock control for cts_pcm_mclk and cts_pcm_sclk

Bit(s)	R/W	Default	Description
31-23	R/W	0	unused
22	R/W	0	CLK_EN: See the Clock Tree document for information related to cts_pcm_sclk
21-16	R/W	0	CLK_DIV: See the Clock Tree document for information related to cts_pcm_sclk
15-12	R/W	0	Unused
11-10	R/W	0	CLK_SEL: See the Clock Tree document for information related to cts_pcm_mclk
9	R/W	0	CLK_EN: See the Clock Tree document for information related to cts_pcm_mclk
8-0	R/W	48	CLK_DIV: See the Clock Tree document for information related to cts_pcm_mclk

HHI_NAND_CLK_CNTL 0x97

Clock control for cts_pcm_mclk and cts_pcm_sclk

Bit(s)	R/W	Default	Description
31-12	R/W	0	unused
11-9	R/W	0	CLK_SEL: 0:cts_oscin_clk 1:fclk_div2 2:fclk_div3 3:fclk_div5 4:fclk_div7 5:mp2_clk_out 6:mp3_clk_out 7:gp0_pll_clk
8			Reserved
7	R/W	0	CLK_EN:
6-0	R/W	48	CLK_DIV

HHI_SD_EMMC_CLK_CNTL 0x99

Bit(s)	R/W	Default	Description
31-28	R/W	0	unused
27-25	R/W	0	Sd_emmc_B_CLK_SEL: 0:cts_oscin_clk 1:fclk_div2 2:fclk_div3 3:fclk_div5 4:fclk_div7 5:mp2_clk_out 6:mp3_clk_out 7:gp0_pll_clk
24			Reserved
23	R/W	0	Sd_emmc_B_CLK_EN:
22-16	R/W	48	Sd_emmc_B_CLK_DIV
15-12	R/W	0	Reserved
11-9	R/W	0	Sd_emmc_A_CLK_SEL: 0:cts_oscin_clk 1:fclk_div2 2:fclk_div3 3:fclk_div5 4:fclk_div7 5:mp2_clk_out 6:mp3_clk_out 7:gp0_pll_clk
8			Reserved
7	R/W	0	Sd_emmc_A_CLK_EN:
6-0	R/W	48	Sd_emmc_A_CLK_DIV

HHI_MPLL_CNTL 0xa0

Bit(s)	R/W	Default	Description
31	R	-	MPLL_LOCK
30	R/W	0	MPLL_ENABLE. 1 = enable
29	R/W	0	MPLL_RESET
28~18	R/W	0	Reserved
28-26	R/W	0	DDS0_P_SET
25	R/W	0	DDS0_SSEN
24-20	R/W	0	DDS0_F_SET
19~18	R/W	0	Reserved
17-16	R/W	0	MPLL_OD
15-14	R/W	0	Unused
13-9	R/W	0	MPLL_N
8-0	R/W	0	MPLL_M

HHI_MPLL_CNTL2 0xa1

Bit(s)	R/W	Default	Description
31-28	R/W	0	LM_W
27~22	R/W	0	LM_S
21	R/W	0	DPFD_LMODE
20~19	R/W	0	VC_IN
18~17	R/W	0	SDMCK_SEL
16	R/W	0	DCO_M_EN
15	R/W	0	SDM_PR_EN
14	R/W	0	DIV_MODE
13	R/W	0	AFC_DSEL_BYPASS
12	R/W	0	AFC_DSEL_IN
11-0	R/W	0	DPLL_DIV_FRAC

HHI_MPLL_CNTL3 0xa2

Bit(s)	R/W	Default	Description
31~30	R/W	0	RESERVED
29~26	R/W	0	FILTER_PVT2
25~22	R/W	0	FILTER_PVT1
21~11	R/W	0	FILTER_ACQ2
10~0	R/W	0	FILTER_ACQ1

HHI_MPLL_CNTL4 0xa3

Bit(s)	R/W	Default	Description
31~24	R/W	0	REVE
23~16	R/W	0	TDC_BUF
15	R/W	0	TDC_CAL_EN
14	R/W	0	PVT_FIX_EN
13~12	R/W	0	DCO_IUP
11~8	R/W	0	SS_AMP
7~4	R/W	0	SS_CLK
3	R/W	0	SSEN
2	R/W	0	DCO_SDM_EN
1	R/W	0	IIR_BYPASS_EN
0	R/W	0	TDC_EN

HHI_MPLL_CNTL5 0xa4

Bit(s)	R/W	Default	Description
31~28	R/W	0	DPLL_BGP_C
27~26	R/W	0	VR_FB2
25~24	R/W	0	VR_FB1
23~22	R/W	0	DDS_VC_VDD

Bit(s)	R/W	Default	Description
21	R/W	0	DDS_LDO_RUPSEL
20	R/W	0	DDS_ENLDO
19~17	R/W	0	TEST_C
16~14	R/W	0	RESERVED
13	R/W	0	IRSEL
12	R/W	0	MP_OD
11~10	R/W	0	TDC_OFF_C
9~8	R/W	0	TDO_NC_SEL
7	R/W	0	TDO_CLK_SEL
6~5	R/W	0	TDC_CAL_PG
4~2	R/W	0	TDC_CAL_OFF
1-0	R/W	0	TDC_CAL_IG

HHI_MPLL_CNTL6 0xa5

Bit(s)	R/W	Default	Description
31~28	R/W	0	CKEN[3:0]
27	R/W	0	CKEN[4]
26	R/W	0	SYS_DPLL_BGP_EN
25~24	R/W	0	SYS_DPLL_EXLDO
23~20	R/W	0	VREF_CS2
19~16	R/W	0	VREF_CF2
15~12	R/W	0	VREF_CS1
11~8	R/W	0	VREF_CF1
7~4	R/W	0	VREF_CS0
3~0	R/W	0	VREF_CF0

HHI_MPLL_CNTL7 (MP0) 0xa6

Bit(s)	R/W	Default	Description
31	R/W	0	IR_BYPASS0
30	R/W	0	MODLSEL0
29~26	R/W	0	IR_BYIN0
25	R/W	0	LP_EN0
24~16	R/W	0	N_IN0
15	R/W	0	SDM_EN0
14	R/W	0	EN_DDS0
13~0	R/W	0	SDM_IN0

HHI_MPLL_CNTL8 (MP1) 0xa7

Bit(s)	R/W	Default	Description
31	R/W	0	IR_BYPASS1
30	R/W	0	MODLSEL1
29~26	R/W	0	IR_BYIN1
25	R/W	0	LP_EN1
24~16	R/W	0	N_IN1
15	R/W	0	SDM_EN1
14	R/W	0	EN_DDS1
13~0	R/W	0	SDM_IN1

HHI_MPLL_CNTL9 (MP2) 0xa8

Bit(s)	R/W	Default	Description
31	R/W	0	IR_BYPASS2
30	R/W	0	MODLSEL2
29~26	R/W	0	IR_BYIN2
25	R/W	0	LP_EN2
24~16	R/W	0	N_IN2
15	R/W	0	SDM_EN2
14	R/W	0	EN_DDS2

Bit(s)	R/W	Default	Description
13~0	R/W	0	SDM_IN2

HHI_MPLL_CNTL10 (MP2) 0xa9

Bit(s)	R/W	Default	Description
31-13	R/W	0	Reserved
12	R/W	0	Mpll_clk25M_en
11-8	R/W	0	Mpll_clk_out_div3_en
7~0	R/W	0	Mpll_clk_out_div2_en

HHI_MPLL3_CNTL0 0xb8

Bit(s)	R/W	Default	Description
31-28	R/W	0	MPLL_IR_BYIN3
25-12	R/W	0	MPLL_SDM_IN3
11	R/W	0	MPLL_SDM_EN3
10~2	R/W	0	MPLL_N_IN3
1	R/W	0	MPLL_MODELSEL3
0	R/W	0	MPLL_EN_DDS3

HHI_MPLL3_CNTL1 0xb9

Bit(s)	R/W	Default	Description
31~10	R/W	0	Reserved
9	R/W	0	MPLL_LP_EN3
8	R/W	0	MPLL_IR_BYPASS3
7-4	R/W	0	MPLL_VREF_CS3
3-0	R/W	0	MPLL_VREF_CF3

HHI_VDAC_CNTL0 0xbd

Bit(s)	R/W	Default	Description
27	R/W	0	CDAC_BIAS_C
26	R/W	0	CDAC_EXT_VREF_EN
25	R/W	0	CDAC_DRIVER_ADJ
24	R/W	0	CDAC_CLK_PHASE_SEL
23~21	R/W	0	CDAC_RL_ADJ
20~16	R/W	0	CDAC_VREF_ADJ
15~8	R/W	0	CDAC_CTRL_RESV2
7~0	R/W	0	CDAC_CTRL_RESV1

HHI_VDAC_CNTL1 0xbe

Bit(s)	R/W	Default	Description
23~16	R	0	CDAC_DIG_OUT_RESV
15~4	R	0	Reserved
3	R/W	0	Cdac_pwd
2~0	R/W	0	CDAC_GSW

HHI_DPLL_TOP_I 0xc6

Bit(s)	R/W	Default	Description
31-22	R	0	RESERVED
21	R	-	GP1_AFC_DONE
20	R	-	Reserved
19	R	-	GP0_AFC_DONE
18	R	-	MPLL_IR_DONE2
17	R	-	MPLL_IR_DONE1
16	R	-	MPLL_IR_DONE0
15~12	R	-	MPLL_IR_OUT2
11~8	R	-	MPLL_IR_OUT1
7~4	R	-	MPLL_IR_OUT0

Bit(s)	R/W	Default	Description
3	R	0	RESERVED
2	R	-	MPLL_TDC_CAL_DONE
1	R	-	SYS_TDC_CAL_DONE
0	R	-	SYS_AFC_DONE

HHI_DPLL_TOP2_I 0xc7

Bit(s)	R/W	Default	Description
31-24	R	0	MPLL_DPLL_OUT_RSV
23-16	R		SYS_DPLL_OUT_RSV
15-13	R	-	Reserved
12	R	-	MPLL_IR_DONE3
11-8	R		MPLL_IR_OUT3
7~0	R	-	GP0_DPLL_OUT_RSV

HHI_HDMI_PLL_CNTL 0xc8

There is some internal muxing controlled by “VLOCK_CNTL_EN” Bit[20] of HHI_HDMI_PLL_CNTL6.

Bit(s)	R/W	Default	Description
31	R/W	0	Lock
30	R/W	0	Enable
29	R/W	0	Reserved
28	R/W	0	RESET
27~14	R/W	0	Reserved
13~9	R/W	0	N
8~0	R/W	0	M = VLOCK_CNTL_EN ? vpu_hdmi_top.m_int_pll : (this register)

HHI_HDMI_PLL_CNTL2 0xc9

There is some internal muxing controlled by “VLOCK_CNTL_EN” Bit[20] of HHI_HDMI_PLL_CNTL6.

Bit(s)	R/W	Default	Description
31	R/W	0	DSEL_IN
30	R/W	0	DSEL_BYPASS
29~24	R/W	0	Reserved
23~22	R/W	0	OD[3:2]
21~20	R/W	0	Reserved
19~18	R/W	0	OD2
17~16	R/W	0	OD[1:0]
15	R/W	0	Reserved
14	R/W	0	DIV_MODE
13~12	R/W	0	Reserved
11~0	R/W	0	DIV_FRAC = VLOCK_CNTL_EN ? vpu_hdmi_top.m_frac_pll : (this register)

HHI_HDMI_PLL_CNTL3 0xca

Bit(s)	R/W	Default	Description
31-29	R/W	0	Reserved
28~18	R/W	0	FILTER_ACQ2
17~7	R/W	0	FILTER_ACQ1
6	R/W	0	DPFD_LMODE
5~4	R/W	0	DC_VC_IN
3~2	R/W	0	DCO_SDMCK_SEL
1	R/W	0	DCO_M_EN
0	R/W	0	SDM_PR_EN

HHI_HDMI_PLL_CNTL4 0xcb

Bit(s)	R/W	Default	Description
31~30	R/W	0	DCO_IUP
29~26	R/W	0	SS_AMP
25~22	R/W	0	SS_CLK
21	R/W	0	SSEN
20	R/W	0	DCO_SDM_EN
19	R/W	0	IIR_BYPASS
18	R/W	0	TDC_EN
17~14	R/W	0	LM_W
13~8	R/W	0	LM_S
7~4	R/W	0	FILTER_PVT2
3~0	R/W	0	FILTER_PVT1

HHI_HDMI_PLL_CNTL5 0xcc

Bit(s)	R/W	Default	Description
31	R/W	0	Reserved
30	R/W	0	VID2_DPLL_BGP_EN
29~22	R/W	0	REVE
21~20	R/W	0	TDC_OFF_C
19~18	R/W	0	TDC_NC_SEL
17	R/W	0	TDC_CLK_SEL
16~15	R/W	0	TDC_CAL_PG
14~12	R/W	0	TDC_CAL_OFF
11~10	R/W	0	TDC_CAL_IG
9	R/W	0	TDC_CAL_EN
8	R/W	0	PVT_FIX_EN
7~0	R/W	0	TDC_BUF

HHI_HDMI_PLL_CNTL6 0xcd

Bit(s)	R/W	Default	Description
31-28	R	0	Reserved
27~21	R/W	0	Reserved
20	R/W	0	VLOCK_CNTL_EN: See HHI_HDMI_PLL_CNTL above,1: have VPU_VLOCK module to control the M/N setting of PLL
19~12	R/W	0	CNEW
11~10	R/W	0	OUT_GATE_CTRL
9-4	R/W	0	Reserved
3~0	R/W	0	HDMI_DPLL_BGP_C

HHI_HDMI_PLL_CNTL_I 0xce

Bit(s)	R/W	Default	Description
31-12	R	0	Reserved
11~4	R		DPLL_OUT_RSV
3~1	R	0	Reserved
0	R	0	AFC_DONE

HHI_HDMI_PLL_CNTL7 0xcf

Bit(s)	R/W	Default	Description
31-18	R	0	Reserved
17-16	R	0	HDMI_DPLL_EXLDO
15-0	R	0	HDMI_DPLL_RSV

HHI_HDMI_PHY_CNTL0 0xe8

Bit(s)	R/W	Default	Description
31~16	R/W	0	HDMI_CTL1
15~0	R/W	0	HDMI_CTL0

HHI_HDMI_PHY_CNTL1 0xe9

Bit(s)	R/W	Default	Description
31~18	R/W	0	Reserved
17	R/W	0	BIT_INVERT
16	R/W	0	MSB_LSB_SWAP
15	R/W	0	Reserved
14	R/W	0	CAPTURE_CLK_GATE_EN
13	R/W	0	HDMI_TX_PRBS_EN: Set to 1 to enable the PRBS engine
12	R/W	0	HDMI_TX_PRBS_ERR_EN: Set to 1 to enable the error flag detector. Set to 0 to reset the error detection logic
11~8	R/W	0	HDMI_TX_SET_HIGH: Set Each Bit to 1 to set the HDMI pin high
7~4	R/W	0	HDMI_TX_SET_LOW: Set Each Bit to 0 to set the HDMI Pins low
3	R/W	0	HDMI_FIFO_WR_ENALBE
2	R/W	0	HDMI_FIFO_ENABLE
1	R/W	0	HDMI_TX_PHY_CLK_EN: Set to 1 to enable the HDMI TX PHY
0	R/W	0	HDMI_TX_PHY_SOFT_RESET: Set to 1 to reset the HDMI TX PHY

HHI_HDMI_PHY_CNTL2 0xea

Bit(s)	R/W	Default	Description
31~9	R	0	Reserved
8	R	0	Test error
7~0	R	0	HDMI_REGRD

HHI_HDMI_PHY_CNTL3 0xeb

Bit(s)	R/W	Default	Description
31~0	R/W	0	RSV

HHI_VID_LOCK_CLK_CNTL 0xf2

Bit(s)	R/W	Default	Description
31~10	R/W	0	reserved
9-8	R/W	0	Clk_sel: 0:cts_oscin_clk 1:cts_encl_clk 2:cts_enci_clk 3:cts_encp_clk
7	R/W	0	Clk_en
6-0	R/W	0	Clk_div

HHI_BT656_CLK_CNTL 0xf5

Bit(s)	R/W	Default	Description
31~27	R/W	0	Reserved
26-25	R/W	0	Bt656_2_clk_sel, the same as bt656_1_clk_sel
24	R/W	0	Reserved
23	R/W	0	Bt656_2_clk_en
22-16	R/W	0	Bt656_2_clk_div
15-11	R/W	0	Reserved
10-9	R/W	0	Bt656_1_clk_sel 0:fclk_div2 1:fclk_div3 2:fclk_div5 3:fclk_div7
8	R/W	0	Reserved
7	R/W	0	Bt656_1_clk_en
6-0	R/W	0	Bt656_1_clk_div

HHI_SAR_CLK_CNTL 0xf6

Bit(s)	R/W	Default	Description
31~11	R/W	0	Reserved
10-9	R/W	0	Clk_sel: 0:cts_oscin_clk

Bit(s)	R/W	Default	Description
			1:clk81
8	R/W	0	Clk_en
7-0	R/W	0	Clk_div

RESET_REGISTER 0xc11004404

Bit(s)	R/W	Default	Description
31-28	R/W	0	MIPI
27	R/W	0	mmc
26	R/W	0	Vcbus_clk81
25	R/W	0	Ahb_data
24	R/W	0	Ahb_cntl
23	R/W	0	Cbus_capb3
22	R/W	0	Sys_cpu_capb3
21	R/W	0	Dos_capb3
20	R/W	0	Mali_capb3
19	R/W	0	Hdmitx_capb3
18	R/W	0	Nand_capb3
17	R/W	0	Capb3_decode
16	R/W	0	Gic
15	R/W	0	Reserved
14	R/W	0	Reserved
13	R/W	0	vcbus
12	R/W	0	AFIFO2
11	R/W	0	ASSIST
10	R/W	0	VENC
9	R/W	0	PMUX
8	R/W	0	Reserved
7	R/W	0	Vid_pll_div
6	R/W	0	AIU
5	R/W	0	VIU
4	R/W	0	DCU_RESET
3	R/W	0	DDR_TOP
2	R/W	0	DOS_RESET
1	R/W	0	Reserved
0	R/W	0	HIU

RESET1_REGISTER 0xc11004408

Bit(s)	R/W	Default	Description
31-29	R/W	0	Reserved
28	R/W	0	Sys_cpu_mbist
27	R/W	0	Sys_cpu_p
26	R/W	0	Sys_cpu_l2
25	R/W	0	Sys_cpu_axi
24	R/W	0	Sys_pll_div
23-20	R/W	0	Sys_cpu_core[3:0]
19-16	R/W	0	Sys_cpu[3:0]
15	R/W	0	Rom_boot
14	R/W	0	Sd_emmc_c
13	R/W	0	Sd_emmc_b
12	R/W	0	Sd_emmc_a
11	R/W	0	Ethernet
10	R/W	0	ISA
9	R/W	0	BLKMV (NDMA)
8	R/W	0	PARSER
7	R/W	0	Reserved
6	R/W	0	AHB_SRAM
5	R/W	0	BT656
4	R/W	0	AO Reset
3	R/W	0	DDR
2	R/W	0	USB_OTG
1	R/W	0	DEMUX
0	R/W	0	Cppm

RESET2_REGISTER 0xc110440c

Bit(s)	R/W	Default	Description
15	R/W	0	Hdmi system reset
14	R/W	0	MALI
13	R/W	0	AO CPU RESET
12	R/W	0	Reserved
11	R/W	0	Reserved
10	R/W	0	parser_top
9	R/W	0	parser_ctl
8	R/W	0	Paser_fetch
7	R/W	0	Parser_reg
6	R/W	0	GE2D
5	R/W	0	Reserved
4	R/W	0	Reserved
3	R/W	0	Reserved
2	R/W	0	HDMI_TX
1	R/W	0	AUDIN
0	R/W	0	VD_RMEM

RESET3_REGISTER 0xc11004410

Bit(s)	R/W	Default	Description
15	R/W	0	Demux reset 2
14	R/W	0	Demux reset 1
13	R/W	0	Demux reset 0
12	R/W	0	Demux S2P 1
11	R/W	0	Demux S2p 0
10	R/W	0	Demux DES
9	R/W	0	Demux top
8	R/W	0	Audio DAC
7	R/W	0	Reserved
6	R/W	0	AHB BRIDGE CNTL

Bit(s)	R/W	Default	Description
5	R/W	0	tvfe
4	R/W	0	AIFIFO
3	R/W	0	Sys_cpu_bvci
2	R/W	0	EFUSE
1	R/W	0	SYS CPU
0	R/W	0	Ring oscillator

RESET4_REGISTER 0xc11004414

Bit(s)	R/W	Default	Description
15	R/W	0	I2C_Master 1
14	R/W	0	I2C_Master 2
13	R/W	0	VENCL
12	R/W	0	VDI6
11	R/W	0	Reserved
10	R/W	0	RTC
9	R/W	0	VDAC
8	R/W	0	Reserved
7	R/W	0	VENCP
6	R/W	0	VENCI
5	R/W	0	RDMA
4	R/W	0	DVIN_RESET
3	R/W	0	Reserved
2	R/W	0	Reserved
1	R/W	0	Reserved
0	R/W	0	Reserved
1	R/W	0	MISC PLL
0	R/W	0	DDR PLL

RESET6_REGISTER 0xc1100441c

Bit(s)	R/W	Default	Description
15	R/W	0	Uart_slip
14	R/W	0	PERIPHS: SDHC
13	R/W	0	PERIPHS: SPI 0
12	R/W	0	PERIPHS: Async 1
11	R/W	0	PERIPHS: Async 0
10	R/W	0	PERIPHS: UART 1, 2
9	R/W	0	PERIPHS: UART 0
8	R/W	0	PERIPHS: SDIO
7	R/W	0	PERIPHS: Stream Interface
6	R/W	0	
5	R/W	0	SANA
4	R/W	0	PERIPHS: I2C Master 0
3	R/W	0	PERIPHS: SAR ADC
2	R/W	0	PERIPHS: Smart Card
1	R/W	0	PERIPHS: SPICC
0	R/W	0	PERIPHS: General

RESET6_REGISTER 0xc11004420

Bit(s)	R/W	Default	Description
15	R/W	0	Reserved
14	R/W	0	Reserved
13	R/W	0	Reserved
12	R/W	0	Reserved
11	R/W	0	Reserved
10	R/W	0	Reserved
9	R/W	0	Reserved
8	R/W	0	A9_dmc_pipel

Bit(s)	R/W	Default	Description
7	R/W	0	vid_lock
6	R/W	0	Reserved
5	R/W	0	Device_mmc_arb
4	R/W	0	Reserved
3~0	R/W	0	Usb_ddr[3:0]

RESET0_MASK 0xc11004440

The Bits of this register correspond to the RESET[n] REGISTERs above. If a bit is set in this register, then when the watchdog timer fires, that particular module will NOT be reset.

RESET1_MASK 0xc11004444

The Bits of this register correspond to the RESET[n] REGISTERs above. If a bit is set in this register, then when the watchdog timer fires, that particular module will NOT be reset.

RESET2_MASK 0xc11004448

The Bits of this register correspond to the RESET[n] REGISTERs above. If a bit is set in this register, then when the watchdog timer fires, that particular module will NOT be reset.

RESET3_MASK 0xc1100444c

The Bits of this register correspond to the RESET[n] REGISTERs above. If a bit is set in this register, then when the watchdog timer fires, that particular module will NOT be reset.

RESET4_MASK 0xc11004450

The Bits of this register correspond to the RESET[n] REGISTERs above. If a bit is set in this register, then when the watchdog timer fires, that particular module will NOT be reset.

RESET5_MASK 0xc11004454

The Bits of this register correspond to the RESET[n] REGISTERs above. If a bit is set in this register, then when the watchdog timer fires, that particular module will NOT be reset.

RESET6_MASK 0xc11004458

The Bits of this register correspond to the RESET[n] REGISTERs above. If a bit is set in this register, then when the watchdog timer fires, that particular module will NOT be reset.

RESET7_MASK 0xc1100445c

The Bits of this register correspond to the RESET[n] REGISTERs above. If a bit is set in this register, then when the watchdog timer fires, that particular module will NOT be reset.

AO_RTI_GEN_CTNL_REG0 0xC8100040

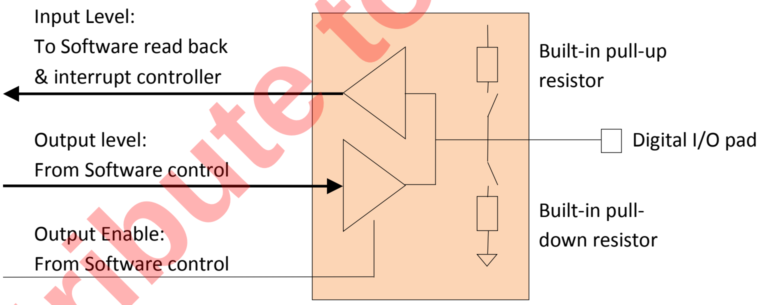
Bit(s)	R/W	Default	Description
31-24	R/W	0	Reserved
23	R/W	0	IR_BLASTER_RESET
22	R/W	0	UART2_RESET
21:20	R/W	0	Reserved
19	R/W	0	I2C_SLAVE_RESET: Set to 1 to reset
18	R/W	0	I2C_MASTER_RESET: Set to 1 to reset
17	R/W	0	UART_MODULE_RESET: Set to 1 to reset
16	R/W	0	IR_MODULE_RESET: Set to 1 to reset
15-8	R/W	0xFF	Reserved
7	R/W	1	Reserved
6	R/W	1	IR_BLASTER clock gate: 1 = clock enabled
5	R/W	1	UART2 module clock gate
4	R/W	1	Reserved
3	R/W	1	UART module clock gate
2	R/W	1	I2C slave module clock gate
1	R/W	1	I2C master module clock gate
0	R/W	1	IR remote decoder clock gate

23. GPIO

23.1 Overview

The SOC has a number of multi-function digital I/O pads that can be multiplexed to a number of internal resources (e.g. PWM generators, SDIO controllers …). When a digital I/O is not being used for any specific purpose, it is converted to a general purpose GPIO pin. A GPIO pin can be statically set to high/low logical levels. The structure of a GPIO is given below.

Figure III.23.1. GPIO Structure



Each GPIO pin has an individual control bitthat can be used to set the output level, output enable of the I/O pad (0 = output, 1 = input). Additionally all digital I/O pads have built-in pull-up and pull-down resistors. The input from the digital I/O pad can be read back in software and is also connected to an interrupt controller. The interrupt controller allows up to 8 GPIO pins to be used as active high, active low, rising edge or falling edge interrupts.

Finally, the GPIO's are grouped into voltage domains. Some GPIOs (depending on the PCB design) can be configured to operate between 0 and 1.8v while others may operate between 0.0v and 3.3v.

23.2 GPIO Multiplex Function

The GPIO multiplex functions are shown in the sections below, where the RegNN[MM] corresponds to CBUS registers defined in Table III. 23.1

Table III.23.1 Pin Mux Registers

Pin Mux Registers	Abbreviation	Offset	Default Value after power-on/Reset

PERIPHS_PIN_MUX_0	REG0	0xc88344b0	0x0000
PERIPHS_PIN_MUX_1	REG1	0xc88344b4	0x0000
PERIPHS_PIN_MUX_2	REG2	0xc88344b8	0x0000
PERIPHS_PIN_MUX_3	REG3	0xc88344bc	0x0000
PERIPHS_PIN_MUX_4	REG4	0xc88344c0	0x0000
PERIPHS_PIN_MUX_5	REG5	0xc88344c4	0x0000
PERIPHS_PIN_MUX_6	REG6	0xc88344c8	0x0000
PERIPHS_PIN_MUX_7	REG7	0xc88344cc	0x0000
PERIPHS_PIN_MUX_8	REG8	0xc88344d0	0x0000
PERIPHS_PIN_MUX_9	REG9	0xc88344d4	0x0000
AO_RTI_PIN_MUX_REG	AO_REG	0xc8100014	0x0000
AO_RTI_PIN_MUX_REG2	AO_REG2	0xc8100018	0x0000

Table III.23.2 GPIOX Pin Multiplexing Table

Package Name	Func1	Func2	Func3	Func4	Func5
GPIOX_0	SDIO_D0 Reg8[5]				
GPIOX_1	SDIO_D1 Reg8[4]				
GPIOX_2	SDIO_D2 Reg8[3]				
GPIOX_3	SDIO_D3 Reg8[2]				
GPIOX_4	SDIO_CLK Reg8[1]				
GPIOX_5	SDIO_CMD Reg8[0]				
GPIOX_6				TSin_D_VALID_B reg3[9]	PWM_A reg3[17]
GPIOX_7	SDIO_IRQ Reg8[11]			TSin_SOP_B reg3[8]	PWM_F reg3[18]
GPIOX_8	ISO7816_CLK reg4[7]		PCM_OUT_A Reg3[30]	TSin_CLK_B reg3[10]	
GPIOX_9	ISO7816_DATA reg4[6]		PCM_IN_A Reg3[29]	TSin_D0_B reg3[7]	
GPIOX_10			PCM_FS_A Reg3[28]		
GPIOX_11			PCM_CLK_A Reg3[27]		
GPIOX_12		UART_TX_A Reg4[13]	SLIP_UART_TX reg4[17]		
GPIOX_13		UART_RX_A Reg4[12]	SLIP_UART_RX reg4[16]		
GPIOX_14		UART_CTS_A Reg4[11]	SLIP_UART_CTS reg4[15]		
GPIOX_15		UART_RTS_A Reg4[10]	SLIP_UART_RTS reg4[14]		
GPIOX_19		UART_RTS_B Reg2[22]			PWM_E reg2[30
GPIOX_20					
GPIOX_21					

Table III.23.3 GPIOY Pin Multiplexing Table

Package Name	Func1	Func2	Func3	Func4	Func5
GPIOY_0	DVP_HS_A reg2[19]	TSin_D_VALID_A reg3[2]			I2S_AO_CLK_IN reg1[0]
GPIOY_1	DVP_VS_A reg2[18]	TSin_SOP_A reg3[1]			I2S_LR_CLK_IN reg1[1]
GPIOY_2	DVP_CLK_A reg2[17]	TSin_CLK_A reg3[0]			
GPIOY_3	DVP_D2_A reg2[16]	TSin_D0_A reg3[4]			I2SIN_CH67 reg1[2]
GPIOY_4	DVP_D3_A reg2[16]	TSin_D1_A reg3[5]		ISO7816_CLK reg1[12]	
GPIOY_5	DVP_D4_A reg2[16]	TSin_D2_A reg3[5]		ISO7816_DATA reg1[13]	
GPIOY_6	DVP_D5_A reg2[16]	TSin_D3_A reg3[5]			I2SIN_CH45 reg1[3]
GPIOY_7	DVP_D6_A reg2[16]	TSin_D4_A reg3[5]			I2SIN_CH23 reg1[4]
GPIOY_8	DVP_D7_A reg2[16]	TSin_D5_A reg3[5]			I2SOUT_CH23 reg1[5]
GPIOY_9	DVP_D8_A reg2[16]	Tsin_D6_A reg3[5]			I2SOUT_CH45 reg1[6]
GPIOY_10	DVP_D9_A reg2[16]	TSin_D7_A reg3[5]			I2SOUT_CH67 reg1[7]
GPIOY_11		TSin_FAIL_A reg3[3]	UART_CTS_C reg1[19]		SPDIF_IN reg1[8]
GPIOY_12			UART_RTS_C reg1[18]		SPDIF_OUT reg1[9]
GPIOY_13			UART_TX_C reg1[17]		DMIC_IN reg1[10]

Package Name	Func1	Func2	Func3	Func4	Func5
GPIOY_14			UART_RX_C reg1[16]		DMIC_CLK_OUT reg1[11]
GPIOY_15	DVP_D0_A reg2[20]			PWM_F reg1[20]	CLKOUT reg1[22]
GPIOY_16	DVP_D1_A reg2[21]			PWM_A reg1[21]	

Table III.23.4. GPIOZ Pin Multiplexing Table

Package Name	Func1	Func2	Func3	Func4
GPIOZ_0	ETH_MDIO reg6[1]	DVP_VS_B reg5[5]		
GPIOZ_1	ETH_MDC reg6[0]	DVP_HS_B reg5[6]		
GPIOZ_2	ETH_CLK_RX_CLK reg6[13]			
GPIOZ_3	ETH_RX_DV reg6[12]	DVP_CLK_B reg5[7]		
GPIOZ_4	ETH_RXD0 reg6[11]	DVP_D2_B reg5[4]		
GPIOZ_5	ETH_RXD1 reg6[10]	DVP_D3_B reg5[4]		
GPIOZ_6	ETH_RXD2 reg6[9]	DVP_D4_B reg5[4]	SPI_SCLK reg5[27]	ISO7816_CLK reg4[9]
GPIOZ_7	ETH_RXD3 reg6[8]	DVP_D5_B reg5[4]	SPI_SS0 reg5[26]	ISO7816_Data reg4[8]
GPIOZ_8	ETH_RGMII_TX_CLK reg6[7]	DVP_D6_B reg5[4]		
GPIOZ_9	ETH_TX_EN reg6[6]	DVP_D7_B reg5[4]		
GPIOZ_10	ETH_TXD0 reg6[5]	DVP_D8_B reg5[4]		
GPIOZ_11	ETH_TXD1 reg6[4]	DVP_D9_B reg5[4]		
GPIOZ_12	ETH_TXD2 reg6[3]		SPI_MISO reg5[28]	
GPIOZ_13	ETH_TXD3 reg6[2]		SPI_MOSI reg5[29]	
GPIOZ_14				
GPIOZ_15		GEN_CLK_OUT reg6[15]		

Table III.23.5 GPIO Bank DV Pin Multiplexing Table

Package Name	Func1	Func2	Func3	Func4	Func5	Func6
GPIODV_24	LCD_VS reg0[7]	DVIN_VS reg0[12]	TCON_STV1 reg5[12]		UART_TX_B reg2[29]	I2C_SDA_A reg7[26]
GPIODV_25	LCD_HS reg0[6]	DVIN_HS reg0[11]	TCON_STH1 reg5[11]		UART_RX_B reg2[28]	I2C_SCK_A reg7[27]
GPIODV_26		DVIN_CLK reg0[10]	TCON_CPH reg5[10]		UART_CTS_B reg2[27]	I2C_SDA_B reg7[24]
GPIODV_27		DVIN_DE reg0[9]	TCON_OEH reg5[9]	TCON_VCOM reg5[8]	UART_RTS_B reg2[26]	I2C_SCK_B reg7[25]
GPIODV_28					PWM_D reg3[20]	I2C_SDA_C reg7[22]
GPIODV_29				PWM_VS reg3[22]	PWM_B reg3[21]	I2C_SCK_C reg7[23]

Table III.23.6 GPIO Bank H Pin Multiplexing Table

Package Name	Func1
GPIOH_0	HDMI_HPD reg1[26]
GPIOH_1	HDMI_SDA reg1[25]
GPIOH_2	HDMI_SCL reg1[24]
GPIOH_3	

Table III.23.7 GPIO Bank CLK Pin Multiplexing Table

Package Name	Func1	Func2
GPIOCLK_0	CLK24	CLK12(wifi)
GPIOCLK_1	CLK25	pwm_F

Table III.23.8. GPIO Bank AO Pin Multiplexing Table

Package Name	Func1	Func2	Func3	Func4
GPIOAO_0	UART_TX_AO_A ao_reg[12]	UART_TX_AO_B ao_reg[26]		
GPIOAO_1	UART_RX_AO_A ao_reg[11]	UART_RX_AO_B ao_reg[25]		
GPIOAO_2	UART_CTS_AO_A ao_reg[10]	UART_CTS_AO_B ao_reg[8]		
GPIOAO_3	UART_RTS_AO_A ao_reg[9]	UART_RTS_AO_B ao_reg[7]	PWM_AO_A ao_reg[22]	
GPIOAO_4		UART_TX_AO_B ao_reg[24]	I2C_SCK_AO ao_reg[6]	I2C_SLAVE_SCK_AO ao_reg[2]
GPIOAO_5		UART_RX_AO_B ao_reg[25]	I2C_SDA_AO ao_reg[5]	I2C_SLAVE_SDA_AO ao_reg[1]
GPIOAO_6		I2S_IN_01 default	PWM_AO_A ao_reg[18]	SPDIF_OUT ao_reg[16]
GPIOAO_7	REMOTE_INPUT ao_reg[0]	REMOTE_OUTPUT ao_reg[21]		
GPIOAO_8			JTAG_TCK See *1-jtag_sel	I2S_AM_CLK ao_reg[30]
GPIOAO_9		I2S_AO_CLK_IN default	JTAG_TMS See *1-jtag_sel	I2S_AO_CLK_OUT ao_reg[29]
GPIOAO_10		I2S_LR_CLK_IN default	JTAG_TDI See *1-jtag_sel	I2S_LR_CLK_OUT ao_reg[28]
GPIOAO_11			JTAG_TDO See *1-jtag_sel	I2SOUT_CH01 ao_reg[27]
GPOAO_12	AO_CEC ao_reg[15]	EE_CEC ao_reg[14]	PWM_AO_A ao_reg[17]	I2SOUT_CH23 ao_reg2[0]
GPIOAO_13	REMOTE_OUTPUT ao_reg[31]	SPDIF_OUT ao_reg[4]	PWM_AO_B ao_reg[3]	I2SOUT_CH45 ao_reg2[1]
TEST_N			PWM_F ao_reg[19]	I2SOUT_CH67 ao_reg2[2]
RESET_N	RESET_N			

Table III.23.9 GPIO Bank BOOT Pin Multiplexing Table

Package Name	Func1	Func2	Func3
BOOT_0		EMMC_NAND_D0 reg4[30]	
BOOT_1		EMMC_NAND_D1 reg4[30]	
BOOT_2		EMMC_NAND_D2 reg4[30]	
BOOT_3		EMMC_NAND_D3 reg4[30]	
BOOT_4		EMMC_NAND_D4 reg4[30]	
BOOT_5		EMMC_NAND_D5 reg4[30]	
BOOT_6		EMMC_NAND_D6 reg4[30]	
BOOT_7		EMMC_NAND_D7 reg4[30]	
BOOT_8	NAND_CE0 reg4[26]	EMMC_CLK reg4[18]	
BOOT_9	NAND_CE1 reg4[27]		
BOOT_10	NAND_RB0 reg4[25]	EMMC_CMD reg4[19]	
BOOT_11	NAND_ALE reg4[24]		NOR_D reg5[1]
BOOT_12	NAND_CLE reg4[23]		NOR_Q reg5[3]

Package Name	Func1	Func2	Func3
BOOT_13	NAND_WEN_CLK reg4[22]		NOR_C reg5[2]
BOOT_14	NAND_REN_WR reg4[21]		
BOOT_15	NAND_DQS reg4[20]	EMMC_DS reg4[31]	NOR_CS reg5[0]

Table III.23.10 GPIO Bank CARD Pin Multiplexing Table

Package Name	Func1	Func2	Func3	Func4
CARD_0	SDCARD_D1 reg2[14]			JTAG_TDI See *1-jtag_sel
CARD_1	SDCARD_D0 reg2[15]			JTAG_TDO See *1-jtag_sel
CARD_2	SDCARD_CLK reg2[11]			JTAG_CLK See *1-jtag_sel
CARD_3	SDCARD_CMD reg2[10]			JTAG_TMS See *1-jtag_sel
CARD_4	SDCARD_D3 reg2[12]	UART_TX_AO_A reg8[10]	UART_RX_AO_A reg8[18]	
CARD_5	SDCARD_D2 reg2[13]	UART_RX_AO_A reg8[17]	UART_TX_AO_A reg8[9]	
CARD_6				

23.3 GPIO Interrupt

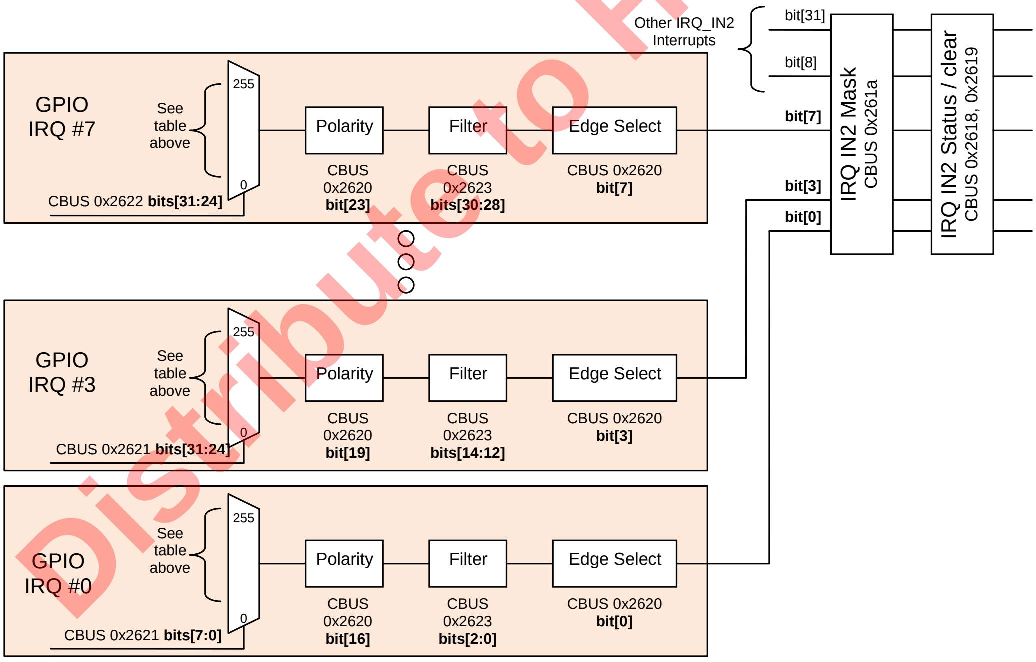
There are 8 independent filtered GPIO interrupt modules that can be programmed to use any of the GPIOs in the chip as an interrupt source (listed in the table below). For example, to select boot_3 as the source for GPIO IRQ #0, then CBUS 0x2621 Bits[7:0] = 27 (according to the table below).

Table III.23.11 GPIO Interrupt Sources

Input Mux Location CBUS registers 0x2621 and 0x2622	Description
255~133	Undefined (no interrupt)
132~129	gpioCLK[3:0]
128~106	gpioX[22:0]
105~89	gpioY[16:0]
88~59	gpioDV[29:0]
58~52	Card[6:0]
51~34	Boot[17:0]
33~30	gpioH[3:0]
29~14	gpioZ[15:0]
13 ~ 0	gpioAO[13:0]

The diagram below illustrates the path a GPIO takes to become an interrupt. The eight GPIO interrupts respond to the MASK, STATUS and STATUS/CLEAR registers just like any other interrupt in the chip. The difference for the GPIO interrupts is that they can be filtered and conditioned. Filtering can either be bypassed or enabled so that a GPIO must be high or low for [3n] * 125nS, where n = 1, 2, …, 7.

Fig III.23.2 GPIO Interrupt Path



NOTE: The input for the GPIO interrupt module (the input into the 256:1 mux) comes directly from the I/O pad of the chip. Therefore if a pad (say card_6) is configured as a UART TX pin, then in theory, the UART TX pin can be a GPIO interrupt since the TX pin will drive card_6 which in turn can drive the GPIO interrupt module.

23.4 Register Description

Table III.23.11 and Table III.23.12 shows the information of GPIO related registers.

Table III.23.11 GPIO Register Infromation I

Final address = 0xc8834400 + offset * 4

Package Name	OEN (Read Write)	OUT (Write Only)	IN (Read Only)	PU/PD-EN (Read Write)	PU/PD (Read Write)	IO Type
GPIOX_22~0	0x18 Bit[22:0]	0x19 Bit[22:0]	0x1a Bit[22:0]	0x4c Bit[22:0]	0x3e Bit[22:0]	Tri-State
GPIOY_16~0	0x0F Bit[16:0]	0x10 Bit[16:0]	0x11 Bit[16:0]	0x49 Bit[16:0]	0x3b Bit[16:0]	Tri-State
GPIODV_29~0	0x0C Bit[29:0]	0x0D Bit[29:0]	0x0E Bit[29:0]	0x48 Bit[29:0]	0x3a Bit[29:0]	Tri-State
GPIOH_3~0	0x0F Bit[23:20]	0x10 Bit[23:20]	0x11 Bit[23:20]	0x49 Bit[23:20]]	0x3b Bit[23:20]	Tri-State
BOOT_17~0	0x12 Bit[17:0]	0x13 Bit[17:0]	0x14 Bit[17:0]	0x4a Bit[17:0]	0x3c Bit[17:0]	Tri-State
CARD_6~0	0x12 Bit[26:20]	0x13 Bit[26:20]	0x14 Bit[26:20]	0x4a Bit[26:20]	0x3c Bit[26:20]	Tri-State
CLK_3~0	0x15 Bit[31:28]	0x16 Bit[31:28]	0x17 Bit[31:28]	0x4b Bit[31:28]	0x3d Bit[31:28]	Tri-State

Table III.23.12 GPIO Register Information II

Final address = 0xc8100000 + offset * 4

Package Name	OEN (Read Write)	OUT (Write Only)	IN (Read Only)	PU/PD-EN (Read Write)	PU/PD (Read Write)	IO Type
GPIOAO_13~0	0x09 Bit[13:0]	0x09 Bit[29:16]	0x0a Bit[13:0]	0x0b Bit[13:0]	0x0b Bit[29:16]	Tri-State

24. Interrupt Control

24.1 Overview

Generic Interrupt Controller (GIC) is a centralized resource that supports and manages interrupts in a system. For more details about GIC, please refer to the ARM GIC Architecture Specification V2.0.

24.2 Interrupt Source

There are 224 interrupt sources in the chip. All of the interrupts are connected to the integrated GIC in Cortex-A53 while the AO-CPU see a sub-set of the interrupts. The control Bits of AO-CPU interrupt are listed in the following table.

Table III.24.1 EE Interrupt Source

A53 GIC Bit	Interrupt sources	Description
255	1'b0	unused
254	1'b0	unused
253	1'b0	unused
252	1'b0	unused
251	1'b0	unused
250	sd_emmc_C_irq	
249	sd_emmc_B_irq	
248	sd_emmc_A_irq	
247	m_i2c_2_irq	
246	m_i2c_1_irq	
245	mbox_irq_send5	
244	mbox_irq_send4	
243	mbox_irq_send3	
242	mbox_irq_receiv2	
241	mbox_irq_receiv1	
240	mbox_irq_receiv0	
239	1'b0	unused
238	ao_timerA_irq	
237	1'b0	unused
236	ao_watchdog_irq	
235	ao_jtag_pwd_fast_irq	
234	1'b0	unused
233	ao_gpio_irq1	
232	ao_gpio_irq0	
231	ao_cec_irq	
230	ao_ir_blaster_irq	
229	ao_uart2_irq	
228	ao_ir_dec_irq	
227	ao_i2c_m_irq	
226	ao_i2c_s_irq	
225	ao_uart_irq	
224	1'b0	unused
223	1'b0	unused
222	1'b0	unused
221	1'b0	unused
220	1'b0	unused
219	1'b0	unused

A53 GIC Bit	Interrupt sources	Description
218	vp9dec_irq	unused
217	1'b0	unused
216	1'b0	unused
215	1'b0	unused
214	1'b0	unused
213	1'b0	unused
212	1'b0	unused
~~211~~	~~mali_irq_ppmmu7~~	
~~210~~	~~mali_irq_pp7~~	
~~209~~	~~mali_irq_ppmmu6~~	
~~208~~	~~mali_irq_pp6~~	
~~207~~	~~mali_irq_ppmmu5~~	
~~206~~	~~mali_irq_pp5~~	
~~205~~	~~mali_irq_ppmmu4~~	
~~204~~	~~mali_irq_pp4~~	
~~203~~	~~mali_irq_ppmmu3~~	
~~202~~	~~mali_irq_pp3~~	
201	mali_irq_ppmmu2	
200	mali_irq_pp2	
199	mali_irq_ppmmu1	
198	mali_irq_pp1	
197	mali_irq_ppmmu0	
196	mali_irq_pp0	
195	mali_irq_pmu	
194	mali_irq_pp	
193	mali_irq_gpmmu	
192	mali_irq_gp	
191		
190	EXTERRIRQ	
189	COMMIRQ3	
188	COMMIRQ2	
187	COMMIRQ1	
186	COMMIRQ0	
185	PMUIRQ3	
184	PMUIRQ2	
183	viu1_line_n_irq	
182	1'b0	
181	ge2d_irq	
180	cusad_irq	
179	asssit_mbox_irq3	
178	asssit_mbox_irq2	
177	asssit_mbox_irq1	
176	asssit_mbox_irq0	
175	det3d_int	
174	1'b0	
173	VCPUMNTIRQ3	
172	VCPUMNTIRQ2	
171	VCPUMNTIRQ1	

A53 GIC Bit	Interrupt sources	Description
170	VCPUMNTIRQ0	
169	PMUIRQ1	
168	PMUIRQ0	
167	1'b0	
166	1'b0	
165	1'b0	
164	1'b0	
163	1'b0	
162	ctiirq3	
161	ctiirq2	
160	ctiirq1	
127	ctiirq0	
126		
125	1'b0	unused
124	uart3_slip_irq	UART slip
123	uart2_irq	UART 2
122	1'b0	unused
121	1'b0	unused
120	1'b0	unused
119	rdma_done_int	RDMA
118	I2S_cbus_ddr_irq	Audio I2S CBUS IRQ
117	1'b0	unused
116	vid1_wr_irq	
115	vdin1_vsync_int	
114	vdin1_hsync_int	
113	vdin0_vsync_int	
112	vdin0_hsync_int	
111	spi2_int	
110	spi_int	
109	vid0_wr_irq	
108	1'b0	unused
107	1'b0	unused
106	1'b0	unused
105	uart1_irq	
104	1'b0	unused
103	sar_adc_irq	SAR ADC
102	1'b0	unused
101	gpio_irq[7]	GPIO Interrupt
100	gpio_irq[6]	GPIO Interrupt
99	gpio_irq[5]	GPIO Interrupt
98	gpio_irq[4]	GPIO Interrupt
97	gpio_irq[3]	GPIO Interrupt
96	gpio_irq[2]	GPIO Interrupt
95	gpio_irq[1]	GPIO Interrupt
94	gpio_irq[0]	GPIO Interrupt
93		
92	TimerI	TimerI
91	TimerH	TimerH

A53 GIC Bit	Interrupt sources	Description
90	TimerG	TimerG
89	TimerF	TimerF
88	1'b0	unused
87	hdcp22_irq	
86	hdmi_tx_interrupt	
85	1'b0	unused
84	hdmi_cec_interrupt	
83	1'b0	unused
82	demux_int_2	
81	dmc_irq	
80	dmc_sec_irq	
79	ai_iec958_int	IEC958 interrupt
78	iec958_ddr_irq	IEC958 DDR interrupt
77	I2S_irq	I2S DDR Interrupt
76	crc_done	From AIU CRC done
75	deint_irq	Reserved for Deinterlacer
74	dos_mbox_slow_irq[2]	DOS Mailbox 2
73	dos_mbox_slow_irq[1]	DOS Mailbox 1
72	dos_mbox_slow_irq[0]	DOS Mailbox 0
71	1'b0	unused
70	1'b0	unused
69	1'b0	unused
68	m_i2c_3_irq	I2C Master #3
67	1'b0	unused
66	smartcard_irq	
65	ndma_irq	Block Move
64	spdif_irq	
63	nand_irq	
62	viff_empty_int_cpu	
61	parser_int_cpu	
60		
59	U2d_interrupt	USB
58	U3h_interrupt	USB
57	Timer D	Timer D
56	bus_mon1_fast_irq	
55	bus_mon0_fast_irq	
54	uart0_irq	
53	async_fifo2_flush_irq	
52	async_fifo2_fill_irq	
51	demux_int	
50	encif_irq	
49	m_i2c_0_irq	
48	bt656_irq	
47	async_fifo_flush_irq	
46	async_fifo_fill_irq	
45	bt656_2_rq	bt656_B
44	1'b0	unused
43	1'b0	unused

A53 GIC Bit	Interrupt sources	Description
42	eth_lip_intro_o	
41	1'b0	unused
40	1'b0	unused
39	Timer B	Timer B
38	Timer A	Timer A
37	1'b0	unused
36	eth_gmac_int	
35	audin_irq	
34	Timer C	Timer C
33	demux_int_1	
32	eth_pmt_intr_o	

24.3 Register Description

Each register's final address = 0xC1100000 + offset * 4

GPIO Interrupt EDGE and Polarity: 0x2620

This register controls the polarity of the GPIO interrupts and whether or not the interrupts are level or edge triggered. There are 8 GPIO interrupts. These 8 GPIO interrupts can be assigned to any one of up to 256 pins on the chip.

Bit(s)	R/W	Default	Description
31-24	R	0	unused
23			GPIO_POLARITY_PATH_7: If a bitin this field is 1, then the GPIO signal for GPIO interrupt path 7 is inverted.
22			GPIO_POLARITY_PATH_6:
21			GPIO_POLARITY_PATH_5:
20			GPIO_POLARITY_PATH_4:
19			GPIO_POLARITY_PATH_3:
18			GPIO_POLARITY_PATH_2:
17			GPIO_POLARITY_PATH_1:
16	R/W	0	GPIO_POLARITY_PATH_0:
15-8	R	0	Unused
7	R/W		GPIO_EDGE_SEL_PATH_7: If a bit is set to 1, then the GPIO interrupt for GPIO path 7 is configured to be an edge generated interrupt. If the polarity (above) is 0, then the interrupt is generated on the rising edge. If the polarity is 1, then the interrupt is generated on the falling edge of the GPIO. If a bit is this field is 0, then the GPIO is a level interrupt.
6	R/W		GPIO_EDGE_SEL_PATH_6
5	R/W		GPIO_EDGE_SEL_PATH_5
4	R/W		GPIO_EDGE_SEL_PATH_4
3	R/W		GPIO_EDGE_SEL_PATH_3
2	R/W		GPIO_EDGE_SEL_PATH_2
1	R/W		GPIO_EDGE_SEL_PATH_1
0	R/W	0	GPIO_EDGE_SEL_PATH_0

GPIO 0 ~ 3 Pin Select: 0x2621

Each GPIO interrupt can select from any number of up to 256 GPIO pins on the chip. The Bits below control the pin selection for GPIO interrupts 0 ~3.

Bit(s)	R/W	Default	Description
31-24	R/W	0	GPIO_PIN_SEL3: This value select which of up to 256 pins on the chip can be mapped to GPIO interrupt 3
23-16	R/W	0	GPIO_PIN_SEL2: This value select which of up to 256 pins on the chip can be mapped to GPIO interrupt 2
15-8	R/W	0	GPIO_PIN_SEL1: This value select which of up to 256 pins on the chip can be mapped to GPIO interrupt 1

Bit(s)	R/W	Default	Description
7-0	R/W	0	GPIO_PIN_SEL0: This value select which of up to 256 pins on the chip can be mapped to GPIO interrupt 0

GPIO 4 ~ 7 Pin Select: 0x2622

Bit(s)	R/W	Default	Description
31-24	R/W	0	GPIO_PIN_SEL7: This value select which of up to 256 pins on the chip can be mapped to GPIO interrupt 7
23-16	R/W	0	GPIO_PIN_SEL6: This value select which of up to 256 pins on the chip can be mapped to GPIO interrupt 6
15-8	R/W	0	GPIO_PIN_SEL5: This value select which of up to 256 pins on the chip can be mapped to GPIO interrupt 5
7-0	R/W	0	GPIO_PIN_SEL4: This value select which of up to 256 pins on the chip can be mapped to GPIO interrupt 4

GPIO Filter Select (interrupts 0~7): 0x2623

Bit(s)	R/W	Default	Description
31	R/W	0	unused
30-28	R/W	0	FILTER_SEL7: (see FILTER_SEL0)
27	R/W	0	Unused
26-24	R/W	0	FILTER_SEL6: (see FILTER_SEL0)
23	R/W	0	Unused
22-20	R/W	0	FILTER_SEL5: (see FILTER_SEL0)
19	R/W	0	Unused
18-16	R/W	0	FILTER_SEL4: (see FILTER_SEL0)
15	R/W	0	Unused
14-12	R/W	0	FILTER_SEL3: (see FILTER_SEL0)
11	R/W	0	Unused
10-8	R/W	0	FILTER_SEL2: (see FILTER_SEL0)
7	R/W	0	Unused
6-4	R/W	0	FILTER_SEL1: (see FILTER_SEL0)
3	R/W	0	unused
2-0	R/W	0	FILTER_SEL0: This value sets the filter selection for GPIO interrupt 0. A value of 0 = no filtering. A value of 7 corresponds to 7 x 3 x (111nS) of filtering.

25. DIRECT MEMORY ACCESS CONTROLLER (DMAC)

25.1 Overview

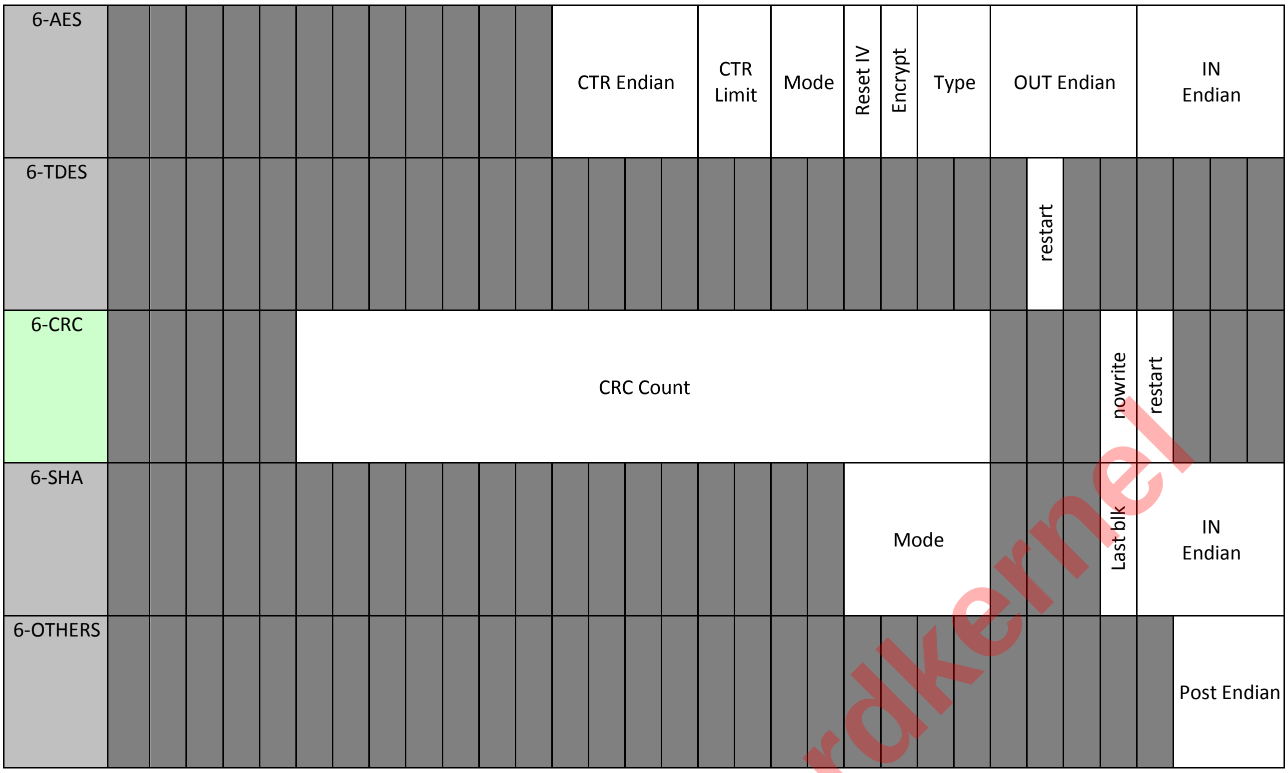
The DMA controller is an engine connected to the DDR controller for the purposes of moving data to/from DDR memory. The DMA controller supports 4 independent threads. Each thread is driven by DMA table descriptors placed in DDR memory. Each DMA descriptor consists of 8 entries that describe the source/destination location as well as the stride and burst. Inline processing is also supported to allow data from DDR to be processed using an AES, Triple-DES, CRC, or SHA module before being placed back into DDR memory.

25.2 Descriptor Table

Below is the descriptor Table.

Table III.25.1 Descriptor Table

<table>
<tr><th>Entry</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td colspan="2">Owner ID (01=system, 10=DMA engine, 00=no woner)</td><td colspan="3">Dmatab Pre Endian</td><td>Source Hold</td><td>Dest Hold</td><td colspan="3">INLINE Type</td><td>IRQ</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>NO Break</td><td colspan="8">Thread Slice Count (0 = use default slice) Number of 256-byte blocks to allocate to this thread</td></tr>
<tr><td>1</td><td colspan="32">SP: Source Pointer (AHB address)</td></tr>
<tr><td>2</td><td colspan="32">DP: Destination Pointer (AHB address) (0xFFFFFFFF = send data to the parser)</td></tr>
<tr><td>3</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="25">Byte transfer count</td></tr>
<tr><td>4</td><td colspan="16">Source Skip</td><td colspan="16">Source Burst Count</td></tr>
<tr><td>5</td><td colspan="16">Destination Skip</td><td colspan="16">Destination Burst Count</td></tr>
</table>



25.3 Register Description

The following registers' final address = 0xda832000 + offset*4

SEC_BLKMV_GEN_REG0 0x24

Bit(s)	R/W	Default	Description
31-20	R/W	'h0	ddr_secure_id
19-18	R/W	'h0	ddr_non_sec_val
17-16	R/W	'h0	ddr_sec_val1
15-14	R/W	'h0	ddr_sec_val0
13-12	R/W	'h0	sec_read_sel
11-8	R/W	'hF	non_sec_mask: 1 = a thread is non-secure
7-4	R/W	'h0	sec_ddr_sec_id_en: Even though a thread is secure, we may not want it to use the DDR secure ID (JIC)
3-0	R/W	'h0	ddr_thread_id[5:2]: 2-bit below used for security

SEC_BLKMV_AES_REG0 0x00

Bit(s)	R/W	Default	Description
31	R	-	aes_key_valid: read-back signal of aes_key_valid
30	R/W	'h0	Reserved
29-28	R/W	'h0	aes_pio_ctr_limit: pio mode CTR limit: Counter set up of counter mode (CTR): 00 = 128-bit Counter in CTR mode, 01 = 32 bit counter, 10 = 64-bit counter. 11 = 128-bit counter
27-24	R/W	'h0	aes_pio_ctr_endian: pio mode CTR endian: Endian set up of counter mode (CTR)
23-20	R/W	'hF	Reserved
19-18	R/W	'h0	aes_pio_type: pio mode aes type: 00 = 128, 01 = 192, 10 = 256, 11 = reserved
17-16	R/W	'h0	aes_pio_mode: pio mode aes mode: 00 = ECB mode, 01 = CBC mode, 10 = CTR mode, 11 = reserved
15-12	R/W	'h0	aes_pio_out_endian: pio mode aes out endian: Endian control of the outgoing message
11-8	R/W	'h0	aes_pio_in_endian: pio mode aes in endian: Endian control of the incoming message
7	R/W	'h0	aes_pio_encrypt: pio mode aes encrypt sel: 0 = decrypt, 1 = encrypt
6	R/W	'h0	aes_get_key_sim: Paused for simulation checking only
5-4	R/W	'h0	aes_key_iv_thread:
3	R/W	'h0	aes_use_sec_thread: used for woftware simulation/debug and PIO mode
2	R/W	'h0	Reserved
1	R/W	'h0	aes_pio_init_IV: (manual mode). Write with a 1 then a 0 to manually initialize the IV when running in PIO mode.
0	R/W	'h0	aes_clk_en_jic: backup enable and also used when the CPU needs to load keys/IV values into the save/restore engine

SEC_BLKMV_TDES_KEY_LO 0x08

The Triple DES engine maintains up to 4 IV keys used for CBC processing. The following three registers are used to setup and write the IV keys to an internal memory. Because each IV key is 64 Bits, the key must be written to an internal register before a 3rd register write is used to push the stored IV key into the internal RAM.

Writing this register sets the IV key Bits [31:0] of the register to be written to the RAM. Reading this register returns the current IV value for processing. This is useful if Cipher Block Chaining must be interrupted. Software can read the current IV key and restore it later to continue processing.

Bit(s)	R/W	Default	Description
31-0	W	'h0	sec_sr_tdes_key_IV_in[31:0]: secure lower 32 bits of tdes_sr_key_IV_in (key_IV_in)

SEC_BLKMV_TDES_KEY_HI 0x09

The register represents the 2nd32-bit component of the 64-bit IV key. Writing this register sets the IV key Bits [63:32] of the register to be written to the RAM. Reading this register returns the current IV value for processing. This is useful if Cipher Block Chaining must be interrupted. Software can read the current IV key and restore it later to continue processing.

Bit(s)	R/W	Default	Description
31-0	W	'h0	sec_sr_tdes_key_IV_in[63:32]: secure upper 32 bits of tdes_sr_key_IV_in (key_IV_in)

SEC_BLKMV_TDES_CONTROL 0x0a

In addition to the 4 IV keys, the Triple DES engine also maintains 4 structures that dictate the individual DES modes, CBC enable, and whether or not we're encrypting or decrypting.

Once the 64-bit IV Key has been established and the MODE, CBC_EN and DECRYPT_EN Bits have been set below, write this register again setting Bits 30 and 31. This pushes the 64-bit IV key and MODE, CBC_EN and DECRYPT_EN Bits into internal RAM. The processing engine will look up these values later using the 2-bit index (TDES_INDEX) supplied in the DMA table entry.

Bit(s)	R/W	Default	Description
31	R/W	'h0	sec_sr_tdes_key_IV_wr: TDES key_IV_wr control signal
30	R/W	'h0	sec_sr_tdes_mode_wr: the write control signal of mode of TDES
29-25	R/W	'h0	Reserved
24-22	R/W	'h0	sec_sr_des_modes: set to '101' for TDES decryption, '010 for DES Encryption
21	R/W	'h0	sec_sr_tdes_cbc: 0 = ECB mode, 1= CBC mode.
20	R/W	'h0	sec_sr_tdes_decrypt: set to 1 to decrypt, set to 0 to encrypt
19-18	R/W	'h0	sec_sr_tdes_wr_thread: CPU thread
17-16	R/W	'h0	sec_sr_tdes_key_IV_in_addr: 0 = key0, 1 = key1, 2 = key2, 3 = IV
15	R	-	tdes_pio_key_busy: TDES key busy read back signal
14	R	-	tdes_pio_busy: TDES busy read back signal
13-7	R/W	'h0	Reserved
6-4	R/W	'h0	des_pio_modes: Mode for the 3 DES engines: [0] = first DES engine, …, [2] = last DES core. // 0=encrypt, 1=decrypt
3	R/W	'h0	Reserved
2	R/W	'h0	tdes_pio_key_compute: set true for one clock to start key computation
1	R/W	'h0	tdes_pio_decrypt
0	R/W	'h0	tdes_pio_start: set true for one clock to process this message (msg_in)

SEC_BLKMV_SHA_CONTROL 0x32

Bit(s)	R/W	Default	Description
31	R	-	sha_busy: sha engine busy read-back signal
30-23	R/W	'h0	Reserved
22	R/W	'h0	sha_pio_fb: sha pio mode feedback sel. 1: sha_msg_in = sha_msg_out, 0: sha_msg_in = sha_pio_msg_in
21	R/W	'h0	sha_pio_last_wdata: last wdata signal for sha_pio_data_wrtire interface: CPU (PIO mode) to SHA engine
20	R/W	'h0	sha_pio_last_block: last block signal for sha_pio_data_wrtire interface: CPU (PIO mode) to SHA engine
19-18	R/W	'h0	sha_pio_wdata_byte_cnt: byte cnt signal for sha_pio_data_wrtire interface: CPU (PIO mode) to SHA engine
17-16	R/W	'h0	sec_sha_pio_mode: pio mode cntl of sha mode: 1:sha1, 2:sha2-256, 3:sha2-224
15-10	R/W	'h0	Reserved
9-8	R/W	'h0	sec_sha_rd_thread: sha message read out thread sel
7	R/W	'h0	Reserved
6	R/W	'h0	sec_sha_ cpu_save_init: pulsed. Reset the internal address counters for CPU writes
5-4	R/W	'h0	sec_sha_wr_thread: sha message write thread sel
3	R/W	'h0	sec_sha_dma_enable: sha enable signal
2	R/W	'h0	sec_sha_clk_en_jic: just in case sha gclk enable signal.
1	R/W	'h0	Reserved
0	R/W	'h0	sec_sha_pio_enable: pio mode sha enable signal

SEC_BLKMV_PIO_CNTL0 0x25

Bit(s)	R/W	Default	Description
31	R	-	pio_granted: pio grant signal (of pio_request) read-back
30-6	R/W	'h0	Reserved
5	R/W	'h0	pio_hold_all: set to 1 to block all in-line processing regardless of the PIO being used
4	R/W	'h0	pio_request: pio mode request signal
3	R/W	'h0	Reserved
2-0	R/W	'h0	pio_inline_type: 0: Normal 1D or 2D move, 1: Triple-DES (TDES) processing, 2: Rijndael (DIVX) processing, 3: CRC processing, 4: AES processing, 5: SHA processing

The following registers' final address = 0xc8832000 + offset*4

NDMA_CNTL_REG0 0x70

Bit(s)	R/W	Default	Description
31	R/W	1	IN-LINE processing clock gating mode: If This bit is set to 0, then the clocks to the DMA engine are always on. If This bit is set to 1, then the DMA engine operates in auto-power down mode. That is, the internal clocks are shut down dynamically to save power.
30	R/W	1	CRC_GATED_CLK_MODE: If This bit is set to 0, then the clocks to the CRC engine are always enabled. If This bit is set to 1, then the CRC block operates in auto-power down mode which will save power when the CRC module is not being used.
29	R/W	1	RIJNDAEL_GATED_CLK_MODE: If This bit is set to 0, then the clocks to the RIJNDAEL engine are always enabled. If This bit is set to 1, then the RIJNDAEL block operates in auto-power down mode which will save power when the RIJNDAEL module is not being used.
28	R/W	1	TDES_GATED_CLK_MODE: If This bit is set to 0, then the clocks to the TDES engine are always enabled. If This bit is set to 1, then the TDES block operates in auto-power down mode which will save power when the TDES module is not being used.
27	R/W	1	DMA_GATED_CLK_MODE: If This bit is set to 0, then the clocks to the general DMA engine are always enabled. If This bit is set to 1, then the general DMA block operates in auto-power down mode which will save power when the general DMA module is not being used.
26	R	-	Status: '1' indicates the DMA engine is processing a descriptor. '0' indicates that all descriptors have been processed
25-16	R/W	0x63	Periodic Interrupt Delay: This value dictates the rate at which periodic interrupts are generated if Bit 15 is set below. Note: If you change this value, then disable the periodic interrupt (Bit 15 below) and then re-enable the period interrupt to reset the internal periodic counter.
15	R/W	0	Periodic Interrupt Enable: If This bit is set to '1', then the DMA engine will generate an interrupt every N+1 uS where N is described above as the Periodic Interrupt Delay.
14	R/W	0	DMA Engine Enable: Set This bit to '1' to enable the DMA Engine. Note, the DMA engine will not do anything until a descriptor has been placed into memory and the NEW_DMA_ADD_DESCRIPTOR register has been written. Set This bit to '0' to abort the current DMA and return the DMA engine to an idle state. Note: If you abort a transfer you should also clear the internal descriptor count by writing 0x2271 with 0x00000001.
13	R/W	0	AES_GATED_CLK_MODE: If This bit is set to 0, then the clocks to the AES engine are always enabled. If This bit is set to 1, then the AES block operates in auto-power down mode which will save power when the AES module is not being used.
12	R	-	AES STATUS: 1 = AES decryption/encryption engine is busy.
11	R/W	0	Use std crc: 1: use standard crc32. 0: use mpeg2 crc32
10-0	R/W	0x00	Reserved

NDMA_TABLE_ADD_REG 0x72

Bit(s)	R/W	Default	Description
31:24	R	-	Blkmv (DME engine) descriptor_cnt[3] read_out
23-16	R	-	Blkmv (DME engine) descriptor_cnt[2] read_out
15-8	R	-	Blkmv (DME engine) descriptor_cnt[1] read_out
7-0	R	-	Blkmv (DME engine) descriptor_cnt[0] read_out

NDMA_TDES_IV_KEY_LO 0x73

The Triple DES engine maintains up to 4 IV keys used for CBC processing. The following three registers are used to setup and write the IV keys to an internal memory. Because each IV key is 64 Bits, the key must be written to an internal register before a 3rd register write is used to push the stored IV key into the internal RAM.

Writing this register sets the IV key Bits [31:0] of the register to be written to the RAM. Reading this register returns the current IV value for processing. This is useful if Cipher Block Chaining must be interrupted. Software can read the current IV key and restore it later to continue processing.

Bit(s)	R/W	Default	Description
31-0	W	0	Non-secure IV Key Bits[31:0]: Write Only

NDMA_TDES_IV_KEY_HI 0x74

The register represents the 2nd32-bit component of the 64-bit IV key. Writing this register sets the IV key Bits [63:32] of the register to be written to the RAM. Reading this register returns the current IV value for processing. This is useful if Cipher Block Chaining must be interrupted. Software can read the current IV key and restore it later to continue processing.

Bit(s)	R/W	Default	Description
31-0	W	0	Non-secure IV Key Bits[63:32] Write Only

NDMA_TDES_CONTROL 0x75

In addition to the 4 IV keys, the Triple DES engine also maintains 4 structures that dictate the individual DES modes, CBC enable, and whether or not we're encrypting or decrypting.

Once the 64-bit IV Key has been established and the MODE, CBC_EN and DECRYPT_EN Bits have been set below, write this register again setting Bits 30 and 31. This pushes the 64-bit IV key and MODE, CBC_EN and DECRYPT_EN Bits into internal RAM. The processing engine will look up these values later using the 2-bit index (TDES_INDEX) supplied in the DMA table entry.

Bit(s)	R/W	Default	Description
31	W	0	This bit is a write only bit. Writing This bit pushes the IV key stored in registers (0x2273 & 0x2274) into the IV key internal RAM. The RAM index is supplied by Bits [3:0] below.
30	W	0	This bit is a write only bit. Writing This bit pushes the DES_MODES, CBC_EN and DECRYPT_EN Bits into an internal RAM. The RAM index is supplied by Bits [3:0] below.
29-9	R	0	Reserved
8-6	R/W	0	MODE: Set to 0x5 for Triple DES decryption and 0x2 for Triple DES Encryption. Note this value is simply shadowed in this register. This bit should be written first before setting Bits 30/31 above to push this value into the internal MODE RAM.
5	R/W	0	CBC_EN: 0 = ECB mode, 1 = CBC mode. Note This bit is simply shadowed in this register. This bit should be written first before setting Bits 30/31 above to push this value into the internal MODE RAM.
4	R/W	0	DECRYPT_EN: Set This bit to 1 to decrypt, 0 to encrypt using triple DES. Note This bit is simply shadowed in this register. This bit should be written first before setting Bits 30/31 above to push this value into the internal MODE RAM.
3-2	R/W	0	IV KEY and Modes Address. These 2 Bits are used to index the 4 locations in the IV KEY RAM and the MODE RAM. These 2 Bits should be set before writing Bits 30 and 31 above.
1-0	R/W	0	TDES KEY IV IN ADDR: 0 = key0, 1 = key1, 2 = key2, 3 = IV

NDMA_RIJNDAEL_CONTROL 0x76

This register directs DIVX processing.

Bit(s)	R/W	Default	Description
31	W	0	This bit is a write only bit. If This bit is set when writing, the RK fifo write pointer is reset.
30-4	R	0	Reserved
3-0	R/W	0	NR Value: 10,12 or 14

NDMA_RIJNDAEL_RK_FIFO 0x77

Bit(s)	R/W	Default	Description
31-0	R/W	0	Writing this register writes the RK FIFO for DIVX Decryption

NDMA_THREAD_REG 0x79

Bit(s)	R/W	Default	Description
31-28	R/W	0	Reserved
27-24	R/W	0	THREAD_INIT: Each Bit is used to initialize a particular thread.
23-16	R/W	0	Reserved
15	R	0	CORE_BUSY: This bit indicates that the thread state-machine is busy
14	R/W	0	Reserved
13-12	R	-	CURR_THREAD_NUM: This value represents the current thread ID being processed by the DMA state-machine
11-8	R/W	0	THREAD_ENABLE: There are 4 threads that can be enabled/disabled corresponding to Bits[11:8]
7-0	R/W	1	DEFAULT_SLICE_CNT: The DMA engine will move from one thread to another after [n] * 256 byte transfers. If a slice count is not provided in the descriptor table, the default value is applied to that thread's descriptor

NDMA_SHA_CONTROL 0x9f

Bit(s)	R/W	Default	Description
31-8	R	0	Reserved
7-6	R/W	0	Reserved
5-4	R/W	0	non_sec_sha_rd_thread: the non_secure SHA msg_out/datalen_out read out thread selection
3	R/W	0	Reserved

Bit(s)	R/W	Default	Description
2	R/W	0	non_sec_sha_cpu_save_init: control of sha_save_restore CPU init signal: reset the internal address counters for cpu writes
1-0	R/W	0	non_sec_sha_wr_thread: the non_secure SHA msg_wr/datalen_wr write thread selection

NDMA_AES_REG0 0x9c

Bit(s)	R/W	Default	Description
31-25	R	0	Reserved
24-20	R	-	mem_st_dbg[4:0]: debug (monitor) of mem_st signal: 0 = MEM_ST_IDLE; 1 = MEM_ST_CHECK_PIO 2 = MEM_ST_INIT; 3 = MEM_ST_READY 4 = MEM_ST_TDES_WAIT; 5 = MEM_ST_TDES_WR_MODULE 6 = MEM_ST_TDES_WR_FIFO; 7 = MEM_ST_RIJNDAEL_WRITE 8 = MEM_ST_RIJNDAEL_WAIT; 9 = MEM_ST_RIJNDAEL_READ 10 = MEM_ST_CRC_PROCESS; 11 = MEM_ST_CRC_NEXT 12 = MEM_ST_AES_WRITE; 13 = MEM_ST_AES_WAIT 14 = MEM_ST_AES_READ; 15 = MEM_ST_SHA_WRITE 16 = MEM_ST_SHA_WAIT; 17 = MEM_ST_SHA_SAVE
		-	cache_st_dbg[1:0]: debug (monitor) of cache_st signal (of new_blkmv_top): 0 = CACHE_ST_IDLE; 1 = CACHE_ST_STORE_TABLE 2 = CACHE_ST_STORE_THREAD; 3 = CACHE_ST_READ_THREAD
17-14	R	-	dma_st_dbg[3:0]: debug (monitor) of dma_st signal (of new_blkmv_top): 0 = DMA_ST_IDLE; 1 = DMA_ST_RD_TABLE_PRE; 2 = DMA_ST_RD_TABLE_REQ; 3 = DMA_ST_RD_TABLE_WAIT; 4 = DMA_ST_RD_TABLE_TAG_OWN; 5 = DMA_ST_RD_TABLE_TAG_DONE; 6 = DMA_ST_CHECK_THREAD_STATUS; 7 = DMA_ST_CACHE_TABLE; 8 = DMA_ST_PROCESS; 9 = DMA_ST_CACHE_THREAD; 10 = DMA_ST_ABORT; 11 = DMA_ST_GET_THREAD_DATA; 12 = DMA_ST_PROCESS_UNPAUSE;
13-10	R	0	Reserved
9-8	R/W	0	non_sec_aes_key_iv_thread: non secure aes key / IV write thread select
7-0	R/W	0	Reserved

NDMA_CNTL_REG1 0x8c

Bit(s)	R/W	Default	Description
31-16	R	-	debug (monitor) of xfer_st signal (of new_blkmv_core): XFER_ST_IDLE = 16'h0001; XFER_ST_RD_START = 16'h0002 XFER_ST_RD_DDR_REQUEST = 16'h0004; XFER_ST_RD_DDR_WAIT = 16'h0008 XFER_ST_INLINE = 16'h0010; XFER_ST_WR_AHB_PROCESS = 16'h0040 XFER_ST_PARSER_PRE = 16'h0080; XFER_ST_PARSER_XFER = 16'h0100 XFER_ST_CHECK = 16'h0200; XFER_ST_RD_START_FNL = 16'h0400 XFER_ST_WR_DDR_PREP0 = 16'h0800; XFER_ST_WR_DDR_PREP1 = 16'h1000
15-10	R/W	0	ddr_burst_num: burst_num_blkmv output to DDR
9-4	R/W	6'h3f	Reserved
3	R/W	0	Reserved
2	R/W	0	thread_speed_up: thread speed up control of BLKMV DMA_ST_PROCESS
1	R/W	0	A_urgent: DDR Urgent bit
0	R/W	'h1	cntl_wr_avail_en: write available enable (jic) signal: Write available forces the DMA state-machines to wait until all data is sent to the DDR memory before moving to the next task. NOTE: This only applies to the very last byte of data for a block to minimize transfer delays. This feature ensures data is actually in the DDR memory before issuing an interrupt to the CPU subsequently forcing a "sync" operation.

26. TIMER

26.1 Overview

The SOC contains 11 general purpose timers and 2 watchdog timers.

26.2 General-Purpose Timer

The SOC contains a number of general-purpose timers that can be used as general counters or interrupt generators. Each counter (except TIMER E) can be configured as a periodic counter (for generating periodic interrupts) or a simple count-down and stop counter. Additionally, the timers have a programmable count rate ranging from 1uS to 1mS. The table below outlines the general-purpose timers available in the chip.

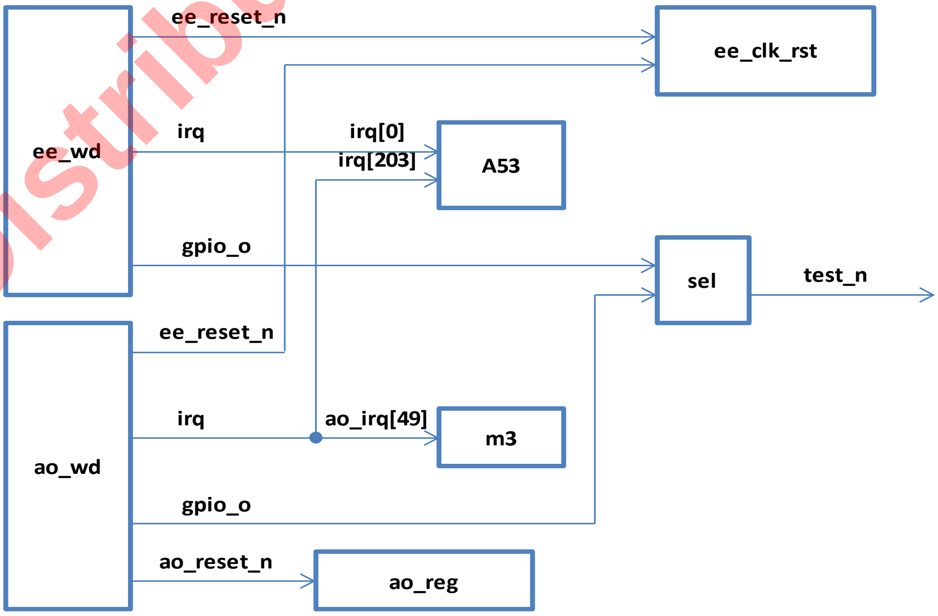
Table III. 26.1. General-Purpose Timer

Timer	Timebase Options	Counter size	Comment
Timer A	1uS, 10uS, 100uS, 1mS	16-bits	The 16-bit counter allows the timer to generate interrupts as infrequent as every 65.535 Seconds
Timer B	1uS, 10uS, 100uS, 1mS	16-bits	
Timer C	1uS, 10uS, 100uS, 1mS	16-bits	
Timer D	1uS, 10uS, 100uS, 1mS	16-bits	
Timer E	System clock, 1uS, 10uS, 100uS, 1mS	64-bits	Doesn't generate an interrupt. This is a count up counter that counts from 0 to 0xFFFFFFFF. The counter can be written at any time to reset the value to 0.
Timer F	1uS, 10uS, 100uS, 1mS	16-bits	
Timer G	1uS, 10uS, 100uS, 1mS	16-bits	
Timer H	1uS, 10uS, 100uS, 1mS	16-bits	
Timer I	1uS, 10uS, 100uS, 1mS	16-bits	
Timer A-AO	System clock, 1uS, 10uS, 100uS	16-bits	Used in the Always On domain to generate interrupts for the AO-CPU
Timer E-AO	System clock	32-bits	This Always On counter doesn't generate an interrupt. Instead it simply counts up from 0 to 0xFFFFFFFF. The counter can be written at any time to reset the value to 0.

26.3 Watchdog Timer

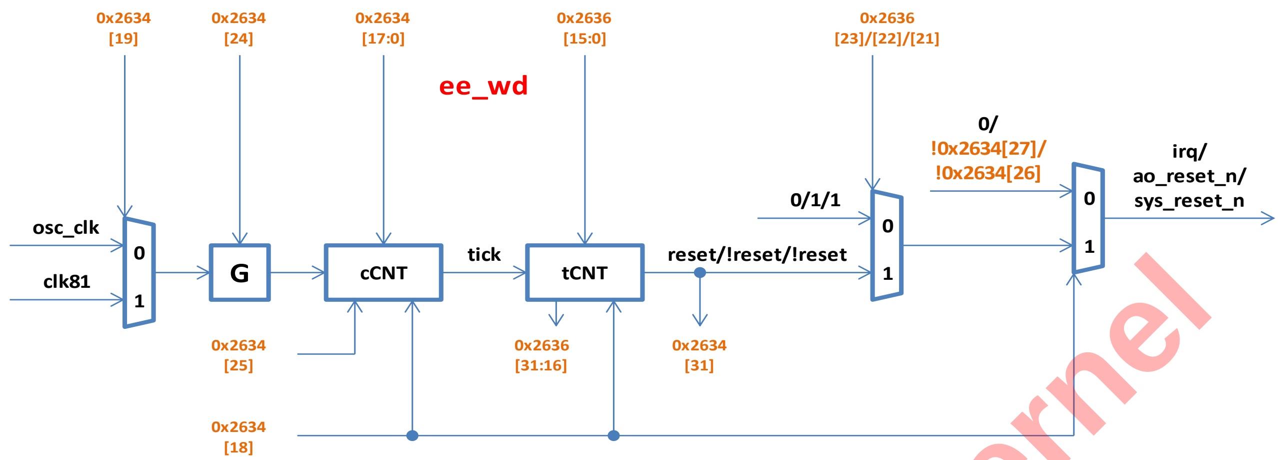
There are two watchdog timers, one in AO and the other in EE domain, illustrated as following:

Figure 26.1 Watchdog Timer



AO domain watchdog timer and EE domain watchdog timer have the same design, as illustrated in the folloing figure:

Figure 26.2 EE domain Watchdog Timer degisn



The AO Domain watchdog timer is driven from the system clock (typically 157Mhz). It is a 16-bit counter that is periodically reset by either the AO CPU or the System CPU (A53). This AO-watchdog timer can be used to generate an interrupt of the AO domain. Additionally, the AO-watchdog timer can be used to "enable" a delay generator that can toggle a GPIO pin (currently the TEST_n I/O pad). The "delay generator" allows an interrupt to first be acknowledged by the AO-CPU before the TEST_N pad is toggled. The "delay generator" is programmable from 1 to 65535 system clocks (typically 417uS).

It should be noted that the AO watchdog timer can also be used to reset the AO domain but this feature is only used when operating in a suspend mode (only the AO-domain is powered). As long as the system periodically resets the AO-watchdog timer the WD_GPIO_CNT (delay generator) will not be enabled and the I/O pad will not toggle.

NOTE: The maximum delay between two AO-watchdog periodic resets is about 100mS (assuming a 157Mhz system clock).

The EE Domain watchdog timer is driven by the 24Mhz crystal clock and can be used to generate an interrupt to the system CPU (the A53) or optionally, the watchdog timer can completely reset the chip (causing a cold boot). There are a few registers that are not affected by watchdog timer. These registers are only reset by the external RESET_n I/O pad and can be used to store information related to a possible watchdog event. As long as the system CPU periodically resets the EE-watchdog timer, it will never timeout and cause an interrupt or system reset.

NOTE: The maximum delay between two EE-watchdog periodic resets is about 8.3 Seconds. This time is independent of the system clocks and is driven by the external 24Mhz crystal.

26.4 Register Definitions

Each register final address = 0xC1100000 + offset * 4

ISA_TIMER_MUX 0x2650

Bit(s)	R/W	Default	Description
31-20	R	0	unused
19	R/W	1	TIMERD_ EN: Set to 1 to enable Timer D

Bit(s)	R/W	Default	Description
18	R/W	1	TIMERC_ EN: Set to 1 to enable Timer C
17	R/W	1	TIMERB_ EN: Set to 1 to enable Timer B
16	R/W	1	TIMERA_EN: Set to 1 to enable Timer A
15	R/W	0	TIMERD_MODE: If This bit is set to 1, then timerD is a periodic . 0 = one-shot timer
14	R/W	0	TIMERC_MODE: If This bit is set to 1, then timerC is a periodic . 0 = one-shot timer
13	R/W	1	TIMERB_MODE: If This bit is set to 1, then timerB is a periodic . 0 = one-shot timer
12	R/W	1	TIMERA_MODE: If This bit is set to 1, then timerA is a periodic . 0 = one-shot timer
11	R	0	unused
10-8	R/W	0x1	TIMER E input clock selection: 000: System clock 001: 1uS Timebase resolution 010: 10uS Timebase resolution 011: 100uS Timebase resolution 100: 1mS timebase NOTE: The mux selection for Timer E is different from timer A, B, C and D
7-6	R/W	0x0	TIMER D input clock selection: See TIMER A below
5-4	R/W	0x0	TIMER C input clock selection: See TIMER A below
2-3	R/W	0x0	TIMER B input clock selection: See TIMER A below
1-0	R/W	0x0	TIMER A Input clock selection: These Bits select the input timebase for the counters for TimerA 00: 1uS Timebase resolution 01: 10uS Timebase resolution 10: 100uS Timebase resolution 11: 1mS Timebase resolution

ISA_TIMERA 0x2651

Timer A is a 16 bit count DOWN counter driven by the clock selected in register 0x01000530. TIMER A will count down from some value to zero, generate an interrupt and then re-load the original start count value. This timer can be used to generate a periodic interrupt (e.g. interrupt every 22 uS).

Bit(s)	R/W	Default	Description
31-16	R	-	Current Count value
15-0	R/W	0x0	Starting count value. Write this value to start TIMER A.

ISA_TIMERB 0x2652

Timer B is just like Timer A.

Bit(s)	R/W	Default	Description
31-16	R	-	Current Count value
15-0	R/W	0x0	Starting count value. Write this value to start TIMER B

ISA_TIMERC 0x2653

Timer C is just like Timer A.

Bit(s)	R/W	Default	Description
31-16	R	0	unused
15-0	R/W	0x0	Starting count value. Write this value to start TIMER C

ISA_TIMERD 0x2654

Timer D is identical to Timer A.

Bit(s)	R/W	Default	Description
31-16	R	0	unused
15-0	R/W	0x0	Starting count value. Write this value to start TIMER D

ISA_TIMERE 0x2662

Timer E is simply a 64-bit counter that increments at a rate set by register 0x2650. To reset the counter to zero, simply write this register with any value. The value below is a read-only value that reflects the current count of the internal counter. This register can be used by software to simply provide a polling delay loop based on a programmable timebase.

Bit(s)	R/W	Default	Description
31-0	R	-	Current value of Timer E. Write this register with any value to clear the counter.

ISA_TIMERE_HI 0x2663

Bit(s)	R/W	Default	Description
31-0	R	-	Current value of Timer E[63:32]. Need read ISA_TIMERE first.

ISA_TIMER_MUX1 0x2664

Bit(s)	R/W	Default	Description
31-20	R	0	unused
19	R/W	1	TIMERD_ EN: Set to 1 to enable Timer D
18	R/W	1	TIMERC_ EN: Set to 1 to enable Timer C
17	R/W	1	TIMERB_ EN: Set to 1 to enable Timer B
16	R/W	1	TIMERA_EN: Set to 1 to enable Timer A
15	R/W	0	TIMERD_MODE: If This bit is set to 1, then timerD is a periodic . 0 = one-shot timer
14	R/W	0	TIMERC_MODE: If This bit is set to 1, then timerC is a periodic . 0 = one-shot timer
13	R/W	1	TIMERB_MODE: If This bit is set to 1, then timerB is a periodic. 0 = one-shot timer
12	R/W	1	TIMERA_MODE: If This bit is set to 1, then timerA is a periodic. 0 = one-shot timer
11	R	0	unused
10-8	R/W	0x1	TIMER E input clock selection: 000: System clock 001: 1uS Timebase resolution 010: 10uS Timebase resolution 011: 100uS Timebase resolution 100: 1mS timebase NOTE: The mux selection for Timer E is different from timer A, B, C and D
7-6	R/W	0x0	TIMER D input clock selection: See TIMER A below
5-4	R/W	0x0	TIMER C input clock selection: See TIMER A below
2-3	R/W	0x0	TIMER B input clock selection: See TIMER A below
1-0	R/W	0x0	TIMER A Input clock selection: These Bits select the input timebase for the counters for TimerA 00: 1uS Timebase resolution 01: 10uS Timebase resolution 10: 100uS Timebase resolution 11: 1mS Timebase resolution

ISA_TIMERF0x2665

Timer F is a 16 bit count DOWN counter driven by the clock selected in register 0x01000530. TIMER A will count down from some value to zero, generate an interrupt and then re-load the original start count value. This timer can be used to generate a periodic interrupt (e.g. interrupt every 22 uS).

Bit(s)	R/W	Default	Description
31-16	R	-	Current Count value
15-0	R/W	0x0	Starting count value. Write this value to start TIMER A.

ISA_TIMERG 0x2666

Timer G is just like Timer F.

Bit(s)	R/W	Default	Description
31-16	R	-	Current Count value
15-0	R/W	0x0	Starting count value. Write this value to start TIMER B

ISA_TIMER_H 0x2667

Timer H is just like Timer F.

Bit(s)	R/W	Default	Description
31-16	R	0	unused
15-0	R/W	0x0	Starting count value. Write this value to start TIMER C

WATCHDOG_CNTL 0x2634

Bit(s)	R/W	Default	Description
31	R	0	Watchdog_reset
30-28	R/W	0	Reserved
27	R/W	0	Ao_reset_n_now, if watchdog_en =0, output ao_reset_n = ! ao_reset_n_now
26	R/W	0	Sys_reset_n_now, if watch_dog_en = 1, output sys_reset_n = !sys_reset_n_now.
25	R/W	0	Clk_div_en: 0: no tick; 1: generate tick;

Bit(s)	R/W	Default	Description
24	R/W	0	Clk_en: 0: no clk; 1: clk work;
23	R/W	0	Interrupt_en: 0: no irq out; 1: irq = watchdog_reset;
22	R/W	0	Ao_reset_n_en: 0: output ao_reset_n = 1; 1: output ao_reset_n = ! watchdog_reset;
21	R/W	0	Sys_reset_n_en 0: output sys_reset_n = 1; 1: output sys_reset_n = ! watchdog_reset;
20	R/W	0	Reserved
19	R/W	0	Clk_sel： 0:osc_clk; 1:clk_81
18	R/W	0	Watchdog_en 0: no watchdog reset 1: gen watchdog reset
17-0	R/W	0	Clk_div_tcnt, when clk_div_en is 1, generate a tick each tcnt clock

WATCHDOG_CNTL1 0x2635

Bit(s)	R/W	Default	Description
31-18	R	0	Reserved
17	R/W	0	Gpio_pulse 0:level reset 1:pulse reset
16	R/W	0	Gpio_polarity 0: 1 is reset; 1: 0 is reset.
15-0	R/W	0	Gpio_pulse_tcnt If gpio_pulse is 1, level reset will hold tcnt clock.

WATCHDOG_TCNT 0x2636

Bit(s)	R/W	Default	Description
31-16	R	0	The cnt of tick.
15-0	R/W	5000	If watchdog_en is 1, when tick cnt reached “5000”, generate watchdog_reset.

WATCHDOG_RESET 0x2637

Bit(s)	R/W	Default	Description
31-0	W	0	When write any value(include 0), watchdog module will be reset.

AO_TIMER_REG 0xc810004c

Timer controls.

Bit(s)	R/W	Default	Description
31-5	R/W	0	Unused

4	R/W	0	TIMER_E_EN
3	R/W	0	TIMER_A_EN
2	R/W	0	TIMER_A_MODE: 1 = periodic, 0 = one-shot
1-0	R/W	0	TIMER_CLK_MUX: 00 = TimerA clock = AO CPU clock 01 = Timer A clock = 1uS ticks 10 = Timer A clock = 10uS ticks 11 = Timer A clock = 100uS ticks

AO_TIMERA_REG 0xc8100050

Timer A starts at a non-zero value and decrements to 0. When timer A reaches a count of 0 it will re-load with the TIMER_A_TCNT value.

Bit(s)	R/W	Default	Description
31-16	R	0	TIMER A current count.
15-0	R/W	0	TIMER_A_TCNT: Timer A Terminal count

AO_TIMERE_REG 0 0xc8100054

If this register is written (with any value), then Timer E is reset to 0. Immediately after being cleared, timer E will start incrementing at a clock rate equal to the clock used for the AO CPU.

Bit(s)	R/W	Default	Description
31-0	R/W	0	TIMER E current Count

27. Crypto

27.1 Overview

The crypto engine is one encrypt/decrypt function accelerator. It supports both encryption/decryption and signature/verification. Crypto engine supports 4 different modes, i.e. A53 secure, A53 non secure, M3 secure and M3 non secure. The crypto engine has special internal DMA controller to transfer data.

It has the following features:

- AES block cipher with 128/192/256 Bits keys, standard 16 bytes block size and streaming ECB, CBC and CTR modes
- DES/TDES block cipher with ECB and CBC modes supporting 64 Bits key for DES and 192 Bits key for 3DES
- Hardware key-ladder operation and DVB-CSA for transport stream encryption
- Built-in hardware True Random Number Generator (TRNG), CRC and SHA-1/SHA-2 (SHA-224/SHA-256) engine

27.2 Key Ladder

The Key Ladder is a series of TDES / AES crypto processes that iterates on different user supplied and OTP keys. The key ladder module uses a single AES / TDES crypto module and iterates using internal storage to hold temporary states.

27.3 RNG

Functionality the Random Number Generator (RNG) contains two main modules: True Random Number Generator (TRNG) and Deterministic Random Number Generator (DRNG).
True Random Number Generator (TRNG): this TRNG is realized by using metastability and jitter for random bit generation based on four free running ring oscillator
Deterministic Random Number Generator (DRNG): this DRNG, which has32-bit random number generator, is mainly designed to increase the throughput and do post-processing of the Digital TRNG, which will need hundreds cycles to collect entropy.

27.4 EFUSE

The EFUSE consists of a 4kbit One Time Programmable (OTP) memory that is broken up into 32, 128-bit blocks. Data is always read/written in 128-bit blocks using the APB bus (software) or by the Key-ladder which is integrated with EFUSE block.

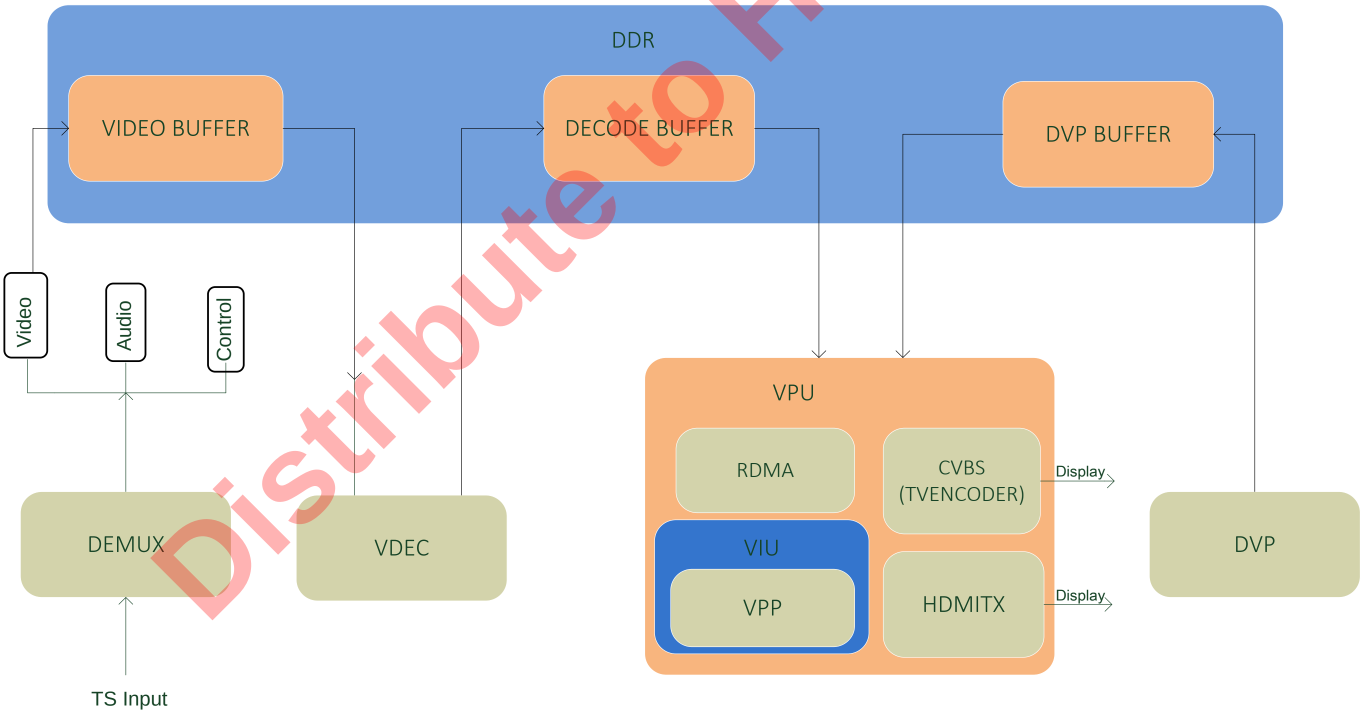
Section IV Video Path

The data path of the video path module is shown in the Fig IV.1 below:
The working flow of S905 video path module is as following:
For TS input, it will go to DEMUX, which will separate the data in to video data, audio data and control data, and will write video data in to DDR, the VDEC module will read this data from DDR and decode it, and then write it back to DDR, which will be sent to VPU module and display in either HDMI format or CVBS format.
For DVP input, DVP module will write it directly to DDR, and VPU module read it and display it in either HDMI or CVBS format.

This section describe S905 video path from the following aspects:

- Video Input
  - -TS input
  - -DEMUX
  - -DVP
- Video Output
  - -RDMA
  - -VPP(VIU/VPP)
  - -HDMI
  - -DVBS

Fig IV.1 Data Path of Video Path



28. Video Input

28.1 Overview

This part describes the video input module of S905, including TS input, Demux and DVP submodules.

28.2 Demux

Demux submodule of S905 is designed for connecting to external digital TV tuner/demodular and de-mux the input signal. It decomposes the TS input signal into video signal, audio signal, and clock signal, the video signal will be first writen in to DDR, then decoded by the video decoder(VDEC). S905 use external demudulator to demulate received signal in to TS (Transport Stream) signal. TS signals contains one or more program of coded data. S905 TS abide by H.222.0, for more detail, please check H.222.0 files. TS uses GPIO ports for input, check 23. GPIO for more information about registers.

28.3 DVP

DVP is an interface designed for camera input. S905's DVP supports ITU656 and ITU601 format. S905 has 2-channle DVP interface, the data recoded by digital camera will be written directly in to DDR, and VPU will read this data and display it in either HDMI format or CVBS format.

28.4 Register Definition

Demux Register

Demux Common Register

Final address = 0xc1105800 + offset * 4

STB_TOP_CONFIG 0xf0

Bit(s)	R/W	Default	Description
30:28	RW	0	ciplus_o_sel
27:26	RW	0	ciplus_i_sel
25	RW	0	use FAIL from TS2
24	RW	0	use FAIL from TS1
23	RW	0	use FAIL from TS0
22	RW	0	invert fec_error for S2P1
21	RW	0	invert fec_data for S2P1
20	RW	0	invert fec_sync for S2P1
19	RW	0	invert fec_valid for S2P1
18	RW	0	invert fec_clk for S2P1
17:16	RW	0	fec_s_sel for S2P1 00 - select TS0, 01 -- select TS1, 10 -- select TS2, 11 - reserved
15	RW	0	enable_des_pl_clk
14:13	RW	0	reserved
12:10	RW	0	ts_out_select, 0-TS0, 1-TS1, 2-TS2, 3,4-Reserved, 5-S2P1, 6-S2P0, 7-File
9:8	RW	0	des_i_sel 00 -- select_fec_0, 01 -- select_fec_1, 10 -- select_fec_2, 11 - reserved
7	RW	0	enable_des_pl
6	RW	0	invert fec_error for S2P0
5	RW	0	invert fec_data for S2P0
4	RW	0	invert fec_sync for S2P0
3	RW	0	invert fec_valid for S2P0
2	RW	0	invert fec_clk for S2P0
1:0	RW	0	fec_s_sel for S2P0 00 - select TS0, 01 -- select TS1, 10 -- select TS2, 11 - reserved

TS_TOP_CONFIG 0xf1

Bit(s)	R/W	Default	Description
31:28	RW	7	s2p1_clk_div
27:24	RW	7	s2p0_clk_div
23	RW	0	s2p1_disable
22	RW	0	s2p0_disable
21	RW	0	Reserved
20	RW	0	TS_OUT_error_INVERT
19	RW	0	TS_OUT_data_INVERT
18	RW	0	TS_OUT_sync_INVERT
17	RW	0	TS_OUT_valid_INVERT
16	RW	0	TS_OUT_clk_INVERT
15:8	RW	187	TS_package_length_sub_1 (default : 187)
7:0	RW	0x47	fec_sync_byte (default : 0x47)

TS_FILE_CONFIG 0xf2

Bit(s)	R/W	Default	Description
25:24	RW	3	transport_scrambling_control_odd_2 // should be 3
23:16	RW	0	file_m2ts_skip_bytes
15:8	RW	0	des_out_dly
7:6	RW	3	transport_scrambling_control_odd // should be 3
5	RW	0	ts_hiu_enable
4:0	RW	4	fec_clk_div

TS_PL_PID_INDEX 0xf3

Bit(s)	R/W	Default	Description
19:14	R	0	des_2 ts pl state -- Read Only
13:8	R	0	des ts pl state -- Read Only
3:0	RW	0	PID index to 8 PID to get key-set auto increse after TS_PL_PID_DATA read/write

TS_PL_PID_DATA 0xf4

Bit(s)	R/W	Default	Description
29	RW	0	PID #INDEX +1 match disble
28:16	RW	0	PID #INDEX+1
13	RW	0	PID #INDEX match disble
12:0	RW	0	PID #INDEX

COMM_DESC_KEY0 0xf5

Bit(s)	R/W	Default	Description
31:0	RW	0	Common descrambler key (key Bits[63:32])

COMM_DESC_KEY1 0xf6

Bit(s)	R/W	Default	Description
31:0	RW	0	Common descrambler key (key Bits[31:0])

COMM_DESC_KEY_RW 0xf7

Bit(s)	R/W	Default	Description
7	RW	0	Key endian;

Bit(s)	R/W	Default	Description
6	RW	0	Write key ladder cw [127:64] to key;
5	RW	0	Write key ladder cw [63:0] to key;
4	RW	0	0: write to descramble 1; 1: write to descramble 2;
3:0	RW	0	The address of key

CIPLUS_KEY0 0xf8

Bit(s)	R/W	Default	Description
31:0	RW	0	CI+ Register defines Bits[31:0] of the key

CIPLUS_KEY1 0xf9

Bit(s)	R/W	Default	Description
31:0	RW	0	CI+ Register defines Bits[63:32] of the key

CIPLUS_KEY2 0xfa

Bit(s)	R/W	Default	Description
31:0	RW	0	CI+ Register defines Bits[95:64] of the key

CIPLUS_KEY3 0xfb

Bit(s)	R/W	Default	Description
31:0	RW	0	CI+ Register defines Bits[127:96] of the key

CIPLUS_KEY_WR 0xfc

Bit(s)	R/W	Default	Description
5	RW	0	write AES IV B value
4	RW	0	write AES IV A value
3	RW	0	write AES B key
2	RW	0	write AES A key
1	RW	0	write DES B key
0	RW	0	write DES A key

CIPLUS_CONFIG 0xfd

Bit(s)	R/W	Default	Description
15:8	RW	0	TS out delay. This controls the rate at which the CIplus module drives TS out
3	RW	0	General enable for the ciplus module
2	RW	0	AES CBC disable (default should be 0 to enable AES CBC)
1	RW	0	AES Enable
0	RW	0	DES Eanble

CIPLUS_ENDIAN 0xfe

Bit(s)	R/W	Default	Description
31:28	RW	0	AES IV endian
27:24	RW	0	AES message out endian
23:20	RW	0	AES message in endian
19:16	RW	0	AES key endian
15:11	RW	0	unused
10:8	RW	0	DES message out endian
6:4	RW	0	DES message in endian
2:0	RW	0	DES key endian

COMM_DESC_2_CTL 0xff

Bit(s)	R/W	Default	Description
15:8	RW	0	des_out_dly_2
7	RW	0	reserved
6	RW	0	enable_des_pl_clk_2
5	RW	0	enable_des_pl_2
4:2	RW	0	use_des_2 Bit[2] -- demux0, Bit[3] -- demux1, Bit[4] -- demux2
1:0	RW	0	des_i_sel_2 00 -- select_fec_0, 01 -- select_fec_1, 10 -- select_fec_2, 11 - reserved

demux core register

demux core 0 Final address = 0xc1105800 + offset * 4

demux core 1 Final address = 0xc1105940 + offset * 4

demux core 2 Final address = 0xc1105a80 + offset * 4

STB_VERSION_O 0x00

Bit(s)	R/W	Default	Description
31:0	R	0x30003	The version of stb

STB_TEST_REG_O 0x01

Bit(s)	R/W	Default	Description
31:0	RW	0xfe015aa5	Test register.

FEC_INPUT_CONTROL_O 0x02

Bit(s)	R/W	Default	Description
15	RW	0	fec_core_select 1 - select descramble output
14:12	RW	0	fec_select 0-TS0, 1-TS1, 2-TS2, 3,4-Reserved, 5-S2P1, 6-S2P0, 7-File
11	RW	0	FEC_CLK
10	RW	0	SOP
9	RW	0	D_VALID
8	RW	0	D_FAIL
7:0	RW	0	D_DATA 7:0

FEC_INPUT_DATA_O 0x03

Bit(s)	R/W	Default	Description
11	R	0	FEC_CLK
20	R	0	SOP
9	R	0	VALID
8	R	0	FAIL
7:0	R	0	FEC DATAIN

DEMUX_CONTROL_O 0x04

Bit(s)	R/W	Default	Description
31	RW	0	enable_free_clk_fec_data_valid
30	RW	0	enable_free_clk_stb_reg
29	RW	0	always_use_pes_package_length
28	RW	0	disable_pre_incomplete_section_fix
27	RW	0	pointer_field_multi_pre_en
26	RW	0	ignore_pre_incomplete_section
25	RW	0	video2_enable
24:22	RW	0	video2_type

Bit(s)	R/W	Default	Description
21	RW	0	do_not_trust_pes_package_length
20 (bit4)	RW	0	Bypass use recoder path
19 (bit3)	RW	0	clear_PID_continuity_counter_valid
18 (bit2)	RW	0	Disable Splicing
17 (bit1)	RW	0	Insert PES_STRONG_SYNC in Audio PES
16 (bit0)	RW	0	Insert PES_STRONG_SYNC in Video PES
15	RW	0	do not trust section length
14	RW	0	om cmd push even zero
13	RW	0	set_buff_ready_even_not_busy
12	RW	0	SUB, OTHER PES interrupt at beginning of PES
11	RW	0	discard_av_package -- for ts_recorder use only
10	RW	0	ts_recorder_select 0:after PID filter 1:before PID filter
9	RW	0	ts_recorder_enable
8	RW	0	(table_id == 0xff) means section_end
7	RW	0	do not send uncomplete section
6	RW	0	do not discard duplicate package
5	RW	0	search SOP when trasport_error_indicator
4	RW	0	stb demux enable
3	RW	0	do not reset state machine on SOP
2	RW	0	search SOP when error happened (when ignore_fail_n_sop, will have this case)
1	RW	0	do not use SOP input (check FEC sync byte instead)
0	RW	0	ignore fec_error bit when non sop (check error on SOP only)

FEC_SYNC_BYTE_O 0x05

Bit(s)	R/W	Default	Description
15:8	RW	187	demux package length - 1 (default : 187)
7:0	RW	0	default is 0x47

FM_WR_DATA_O 0x06

Bit(s)	R/W	Default	Description
31:16	RW	0	filter memory write data hi[31:16]
15:0	RW	0	filter memory write data low [15:0]

FM_WR_ADDR_O 0x07

Bit(s)	R/W	Default	Description
31:24	RW	0	advanced setting hi
23:16	RW	0	advanced setting low
15	R	0	filter memory write data request
7:0	R	0	filter memory write addr

MAX_FM_COMP_ADDR_O 0x08

Bit(s)	R/W	Default	Description
13:8	R	0	demux state -- read only
7:4	RW	0	maxnum section filter compare address
3:0	RW	0	maxnum PID filter compare address

TS_HEAD_0_O 0x09

Bit(s)	R/W	Default	Description

15	RW	0	transport_error_indicator
14	RW	0	payload_unit_start_indicator
13	RW	0	transport_priority
12:0	RW	0	PID

TS_HEAD_1_O 0x0a

Bit(s)	R/W	Default	Description
7:6	R	0	transport_scrambling_control
5:4	R	0	adaptation_field_control
3:0	R	0	continuity_counter

OM_CMD_STATUS_O 0x0b

Bit(s)	R/W	Default	Description
15:12	R	0	om_cmd_count (read only)
11:9	R	0	overflow_count // bit 11:9 -- om_cmd_wr_ptr (read only)
8:6	R	0	om_overwrite_count // bit 8:6 -- om_cmd_rd_ptr (read only)
5:3	R	0	type_stb_om_w_rd (read only)
2	R	0	unit_start_stb_om_w_rd (read only)
1	R	0	om_cmd_overflow (read only)
0	R	0	om_cmd_pending (read)
0	R	0	om_cmd_read_finished (write)

OM_CMD_DATA_O 0x0c

Bit(s)	R/W	Default	Description
15:9	R	0	count_stb_om_w_rd (read only)
8:0	R	0	start_stb_om_wa_rd (read only)

OM_CMD_DATA2_O 0x0d

Bit(s)	R/W	Default	Description
11:0	R	0	offset for section data

SEC_BUFF_01_START_O 0x0e

Bit(s)	R/W	Default	Description
31:16	RW	0	base address for section buffer group 0 (*0x400 to get real address)
15:0	RW	0	base address for section buffer group 1 (*0x400 to get real address)

SEC_BUFF_23_START_O 0x0f

Bit(s)	R/W	Default	Description
31:16	RW	0	base address for section buffer group 2 (*0x400 to get real address)
15:0	RW	0	base address for section buffer group 3 (*0x400 to get real address)

SEC_BUFF_SIZE_O 0x10

Bit(s)	R/W	Default	Description
3:0	RW	0	section buffer size for group 0 (bitused, for example, 10 means 1K)
7:4	RW	0	section buffer size for group 1
11:8	RW	0	section buffer size for group 2
15:12	RW	0	section buffer size for group 3

SEC_BUFF_BUSY_O 0x11

Bit(s)	R/W	Default	Description
31:0	R	0	Section buffer busy status for buff 31:0 (Read Only)

SEC_BUFF_READY_O 0x12

Bit(s)	R/W	Default	Description
31:0	RW	0	section buffer write status for buff 31:0 -- Read clear buffer status (buff READY and BUSY) – write

SEC_BUFF_NUMBER_O 0x13

Bit(s)	R/W	Default	Description
4:0	RW	0	SEC_BUFFER_INDEX RW
12:8	RW	0	SEC_BUFFER_NUMBER for the INDEX buffer Read_Only
14	RW	0	output_section_buffer_valid
15	RW	0	section_reset_busy (Read Only)

ASSIGN_PID_NUMBER_O 0x14

Bit(s)	R/W	Default	Description
9:5	RW	0	BYPASS PID number
4:0	RW	0	PCR PID number

VIDEO_STREAM_ID_O 0x15

Bit(s)	R/W	Default	Description
31:16	RW	0	for video2
15:0	RW	0	stream_id filter Bit(s) enable

AUDIO_STREAM_ID_O 0x16

Bit(s)	R/W	Default	Description
15:0	RW	0	For audio

SUB_STREAM_ID_O 0x17

Bit(s)	R/W	Default	Description
15:0	RW	0	For sub

OTHER_STREAM_ID_O 0x18

Bit(s)	R/W	Default	Description
15:0	RW	0	For other

PCR90K_CTL_O 0x19

Bit(s)	R/W	Default	Description
12	RW	0	PCR_EN
11:0	RW	0	PCR90K_DIV

PCR_DEMUX_O 0x1a

Bit(s)	R/W	Default	Description
31:0	RW	0	PCR

VIDEO_PTS_DEMUX_O 0x1b

Bit(s)	R/W	Default	Description
31:0	RW	0	VPTS

VIDEO_DTS_DEMUX_O 0x1c

Bit(s)	R/W	Default	Description
31:0	RW	0	VDTS

AUDIO_PTS_DEMUX_O 0x1d

Bit(s)	R/W	Default	Description
31:0	RW	0	APTS

SUB_PTS_DEMUX_O 0x1e

Bit(s)	R/W	Default	Description
31:0	RW	0	SPTS

STB_PTS_DTS_STATUS_O 0x1f

Bit(s)	R/W	Default	Description
15	R	0	SUB_PTS[32]
14	R	0	AUDIO_PTS[32]
13	R	0	VIDEO_DTS[32]
12	R	0	VIDEO_PTS[32]
3	R	0	sub_pts_ready
2	R	0	audio_pts_ready
1	R	0	video_dts_ready
0	R	0	video_pts_ready

STB_DEBUG_INDEX_O 0x20

Bit(s)	R/W	Default	Description
3	RW	0	pes_ctr_byte[7:0], pes_flag_byte[7:0]
2	RW	0	pes_package_bytes_left[15:0]
1	RW	0	stream_id[7:0], pes_header_bytes_left[7:0]
0	RW	0	adaptation_field_length[7:0], adaption_field_byte_1[7:0]

STB_DEBUG_DATAOUT_O 0x21

Bit(s)	R/W	Default	Description
15:0	R	0	Debug data out[15:0]

STB_MOM_CTL_O 0x22

Bit(s)	R/W	Default	Description
31	RW	0	no_match_record_en
30:16	RW	0	reserved
15:9	RW	0	MAX OM DMA COUNT (default: 0x40)
8:0	RW	0	LAST ADDR OF OM ADDR (default: 127)

STB_INT_STATUS_O 0x23

Bit(s)	R/W	Default	Description
12	R	0	INPUT_TIME_OUT
11	R	0	PCR_ready
10	R	0	audio_splicing_point
9	R	0	video_splicing_point
8	R	0	other_PES_int
7	R	0	sub_PES_int

Bit(s)	R/W	Default	Description
6	R	0	discontinuity
5	R	0	duplicated_pack_found
4	R	0	New PDTS ready
3	R	0	om_cmd_buffer ready for access
2	R	0	section buffer ready
1	R	0	transport_error_indicator
0	R	0	TS ERROR PIN

DEMUX_ENDIAN_O 0x24

Bit(s)	R/W	Default	Description
23:21	RW	0	demux om write endian control for OTHER_PES_PACKET
20:18	RW	0	demux om write endian control for SCR_ONLY_PACKET
17:15	RW	0	demux om write endian control for SUB_PACKET
14:12	RW	0	demux om write endian control for AUDIO_PACKET
11:9	RW	0	demux om write endian control for VIDEO_PACKET
8:6	RW	0	demux om write endian control for else
5:3	RW	0	demux om write endian control for bypass
2:0	RW	0	demux om write endian control for section

TS_HIU_CTL_O 0x25

Bit(s)	R/W	Default	Description
15:8	RW	0	last_burst_threshold
7	RW	0	use hi_bsf interface
6:2	RW	0	fec_clk_div
1	RW	0	ts_source_sel
0	RW	0	Hiu TS generate enable

SEC_BUFF_BASE_O 0x26

Bit(s)	R/W	Default	Description
15:0	RW	0	base address for section buffer start (*0x10000 to get real base)

DEMUX_MEM_REQ_EN_O 0x27

Bit(s)	R/W	Default	Description
11	RW	0	mask bit for OTHER_PES_AHB_DMA_EN
10	RW	0	mask bit for SUB_AHB_DMA_EN
9	RW	0	mask bit for BYPASS_AHB_DMA_EN
8	RW	0	mask bit for SECTION_AHB_DMA_EN
7	RW	0	mask bit for recoder stream
6:0	RW	0	mask bit for each type

VIDEO_PDTS_WR_PTR_O 0x28

Bit(s)	R/W	Default	Description
31:0	RW	0	vb_wr_ptr for video PDTS

AUDIO_PDTS_WR_PTR_O 0x29

Bit(s)	R/W	Default	Description
31:0	RW	0	ab_wr_ptr for video PDTS

SUB_WR_PTR_O 0x2a

Bit(s)	R/W	Default	Description
20:0	RW	0	SB_WRITE_PTR (sb_wr_ptr << 3 == byte write position)

SB_START_O 0x2b

Bit(s)	R/W	Default	Description
19:0	RW	0	SB_START (sb_start << 12 == byte address);

SB_LAST_ADDR_O 0x2c

Bit(s)	R/W	Default	Description
20:0	RW	0	SB_SIZE (sb_size << 3 == byte size, 16M maximun)

SB_PES_WR_PTR_O 0x2d

Bit(s)	R/W	Default	Description
31:0	RW	0	sb_wr_ptr for sub PES

OTHER_WR_PTR_O 0x2e

Bit(s)	R/W	Default	Description
31:21	RW	0	ob_wr_ptr for other PES
20:0	RW	0	OB_WRITE_PTR (ob_wr_ptr << 3 == byte write position)

OB_START_O 0x2f

Bit(s)	R/W	Default	Description
19:0	RW	0	OB_START (ob_start << 12 == byte address);

OB_LAST_ADDR_O 0x30

Bit(s)	R/W	Default	Description
20:0	RW	0	OB_SIZE (ob_size << 3 == byte size, 16M maximun)

OB_PES_WR_PTR_O 0x31

Bit(s)	R/W	Default	Description
31:0	RW	0	ob_wr_ptr for sub PES

STB_INT_MASK_O 0x32

Bit(s)	R/W	Default	Description
9	RW	0	splicing_point
8	RW	0	other_PES_int
7	RW	0	sub_PES_int
6	RW	0	discontinuity
5	RW	0	duplicated_pack_found
4	RW	0	New PDTS ready
3	RW	0	om_cmd_buffer ready for access
2	RW	0	section buffer ready
1	RW	0	transport_error_indicator
0	RW	0	TS ERROR PIN

VIDEO_SPLICING_CTL_O 0x33

Bit(s)	R/W	Default	Description
15	RW	0	splicing VIDEO PID change enable

Bit(s)	R/W	Default	Description
14:10	RW	0	VIDEO PID FILTER ADDRESS
9	RW	0	PES splicing active (Read Only)
8	RW	0	splicing active (Read Only)
7:0	RW	0	splicing countdown (Read Only)

AUDIO_SPLICING_CTL_O 0x34

Bit(s)	R/W	Default	Description
15	RW	0	splicing AUDIO PID change enable
14:10	RW	0	AUDIO PID FILTER ADDRESS
9	RW	0	PES splicing active (Read Only)
8	RW	0	splicing active (Read Only)
7:0	RW	0	splicing countdown (Read Only)

TS_PACKAGE_BYTE_COUNT_O 0x35

Bit(s)	R/W	Default	Description
23:16	RW	0	M2TS_SKIP_BYTES
15:8	RW	0	LAST TS PACKAGE BYTE COUNT (Read Only)
7:0	RW	0	PACKAGE BYTE COUNT (Read Only)

PES_STRONG_SYNC_O 0x36

Bit(s)	R/W	Default	Description
15:0	RW	0	2 bytes strong sync add to PES

OM_DATA_RD_ADDR_O 0x37

Bit(s)	R/W	Default	Description
15	RW	0	stb_om_ren
14:11	RW	0	reserved
10:0	RW	0	OM_DATA_RD_ADDR

OM_DATA_RD_O 0x38

Bit(s)	R/W	Default	Description
15:0	RW	0	OM_DATA_RD

SECTION_AUTO_STOP_3_O 0x39

Bit(s)	R/W	Default	Description
31	RW	0	Auto stop count 31 Wr_en
30:28	RW	0	Auto stop count 31
27	RW	0	Auto stop count 30 Wr_en
26:24	RW	0	Auto stop count 30
23	RW	0	Auto stop count 29 Wr_en
22:20	RW	0	Auto stop count 29
19	RW	0	Auto stop count 28 Wr_en
18:16	RW	0	Auto stop count 28
15	RW	0	Auto stop count 27 Wr_en
14:12	RW	0	Auto stop count 27
11	RW	0	Auto stop count 26 Wr_en
10:8	RW	0	Auto stop count 26
7	RW	0	Auto stop count 25 Wr_en

Bit(s)	R/W	Default	Description
6:4	RW	0	Auto stop count 25
3	RW	0	Auto stop count 24 Wr_en
2:0	RW	0	Auto stop count 24

SECTION_AUTO_STOP_2_O   0x3a

Bit(s)	R/W	Default	Description
31	RW	0	Auto stop count 23 Wr_en
30:28	RW	0	Auto stop count 23
27	RW	0	Auto stop count 22 Wr_en
26:24	RW	0	Auto stop count 22
23	RW	0	Auto stop count 21 Wr_en
22:20	RW	0	Auto stop count 21
19	RW	0	Auto stop count 20 Wr_en
18:16	RW	0	Auto stop count 20
15	RW	0	Auto stop count 19 Wr_en
14:12	RW	0	Auto stop count 19
11	RW	0	Auto stop count 18 Wr_en
10:8	RW	0	Auto stop count 18
7	RW	0	Auto stop count 17 Wr_en
6:4	RW	0	Auto stop count 17
3	RW	0	Auto stop count 16 Wr_en
2:0	RW	0	Auto stop count 16

SECTION_AUTO_STOP_1_O 0x3b

Bit(s)	R/W	Default	Description
31	RW	0	Auto stop count 15 Wr_en
30:28	RW	0	Auto stop count 15
27	RW	0	Auto stop count 14 Wr_en
26:24	RW	0	Auto stop count 14
23	RW	0	Auto stop count 13 Wr_en
22:20	RW	0	Auto stop count 13
19	RW	0	Auto stop count 12 Wr_en
18:16	RW	0	Auto stop count 12
15	RW	0	Auto stop count 11 Wr_en
14:12	RW	0	Auto stop count 11
11	RW	0	Auto stop count 10 Wr_en
10:8	RW	0	Auto stop count 10
7	RW	0	Auto stop count 9 Wr_en
6:4	RW	0	Auto stop count 9
3	RW	0	Auto stop count 8 Wr_en
2:0	RW	0	Auto stop count 8

SECTION_AUTO_STOP_0_O 0x3c

Bit(s)	R/W	Default	Description
31	RW	0	Auto stop count 7 Wr_en
30:28	RW	0	Auto stop count 7
27	RW	0	Auto stop count 6 Wr_en
26:24	RW	0	Auto stop count 6

Bit(s)	R/W	Default	Description
23	RW	0	Auto stop count 5 Wr_en
22:20	RW	0	Auto stop count 5
19	RW	0	Auto stop count 4 Wr_en
18:16	RW	0	Auto stop count 4
15	RW	0	Auto stop count 3 Wr_en
14:12	RW	0	Auto stop count 3
11	RW	0	Auto stop count 2 Wr_en
10:8	RW	0	Auto stop count 2
7	RW	0	Auto stop count 1 Wr_en
6:4	RW	0	Auto stop count 1
3	RW	0	Auto stop count 0 Wr_en
2:0	RW	0	Auto stop count 0

DEMUX_CHANNEL_RESET_O 0x3d

Bit(s)	R/W	Default	Description
31:0	R	0	Bit 31:0 reset channel status - Each Bit reset each channel

DEMUX_SCRAMBLING_STATE_O 0x3e

Bit(s)	R/W	Default	Description
31:0	R	0	Scrambling state of each channel

DEMUX_CHANNEL_ACTIVITY_O 0x3f

Bit(s)	R/W	Default	Description
31:0	R	0	Channel activity of each channel

DEMUX_STAMP_CTL_O 0x40

Bit(s)	R/W	Default	Description
4	RW	0	video_stamp_use_dts
3	RW	0	audio_stamp_sync_1_en
2	RW	0	audio_stamp_insert_en
1	RW	0	video_stamp_sync_1_en
0	RW	0	video_stamp_insert_en

DEMUX_VIDEO_STAMP_SYNC_0_O 0x41

Bit(s)	R/W	Default	Description
31:0	RW	0	Video stamp sync [63:32]

DEMUX_VIDEO_STAMP_SYNC_1_O 0x42

Bit(s)	R/W	Default	Description
31:0	RW	0	Video stamp sync [31:0]

DEMUX_AUDIO_STAMP_SYNC_0_O 0x43

Bit(s)	R/W	Default	Description
31:0	RW	0	Aideo stamp sync [63:32]

DEMUX_AUDIO_STAMP_SYNC_1_O 0x44

Bit(s)	R/W	Default	Description
31:0	RW	0	Aideo stamp sync [31:0]

DEMUX_SECTION_RESET_O 0x45

Bit(s)	R/W	Default	Description
31:0	R	0	Write : Bit[4:0] secter filter number for reset Read : select according to output_section_buffer_valid: per bit per section buffer valid status or section_buffer_ignore

DEMUX_INPUT_TIMEOUT_C_O 0x46

Bit(s)	R/W	Default	Description
31:0	RW	0	channel_reset_timeout_disable

DEMUX_INPUT_TIMEOUT_O 0x47

Bit(s)	R/W	Default	Description
31	RW	0	no_match_reset_timeout_disable
30:0	RW	0	input_time_out_int_cnt (0 -- means disable) Wr-setting, Rd-count

DEMUX_PACKET_COUNT_O 0x48

Bit(s)	R/W	Default	Description
31:0	RW	0	channel_packet_count_disable

DEMUX_PACKET_COUNT_C_O 0x49

Bit(s)	R/W	Default	Description
31	RW	0	no_match_packet_count_disable
30:0	RW	0	input_packet_count

DEMUX_CHAN_RECORD_EN_O 0x4a

Bit(s)	R/W	Default	Description
31:0	RW	0xffffffff	channel_record_enable

DEMUX_CHAN_PROCESS_EN_O 0x4b

Bit(s)	R/W	Default	Description
31:0	RW	0xffffffff	channel_process_enable

DEMUX_SMALL_SEC_CTL_O 0x4c

Bit(s)	R/W	Default	Description
31:24	RW	0	small_sec_size ((n+1) * 256 Bytes)
23:16	RW	0	small_sec_rd_ptr
15:8	RW	0	small_sec_wr_ptr
7:2	RW	0	reserved
1	RW	0	small_sec_wr_ptr_wr_enable
0	RW	0	small_section_enable

DVP Register

Final Address = 0xd0048000 + offset *4
Write Register

CTRL 0x00

Bit(s)	Name	Description
31	Soft_reset	The reset of all bt656 module
30	syncfifo_soft_reset_n_sys	The reset of syncfifo output
29	syncfifo_soft_reset_n_bt	The reset of syncfifo input
28	Syncfifo_reset	The reset of syncfifo all
27	raw_isp	0: use 3 port send raw data; 1: use 1 port send raw data;
[26:25]	vs_to_viu_sel/ vs_to_isp_sel	0:sof;1:eof;2:vbi_start;3:vbi_end;
[24:23]	hs_to_viu_sel/ hs_to_isp_sel	0:eav;1:sav;2:eol;3:sol
22	camera_mode	Go to camera state.
[21:18]	Eol_delay	Eol =vdo_en's negedge[delay]
16	update_st_ctl	Update all status register by: 0:eof/1:sof.
15	color_repeat	Format select of YCbCr422 to YCbCr444.
14:13	video_mode	Input format and output format. 0:YCbCr;1:565RGB; 2:1byte raw
12	auto_fmt	Go to ntsc/pal state and auto check.
11	prog_mode	Go to DVP state.
10		
9	Sys_clk_en	Gate enable of sys_clk. need set 1 at first
8		
7	bt_clk_en	Gate enable of clkin need set 1 at first
6	clk27_phase	Reverse of clk27.
5	auto_cover_error	Reset after error occurs.
4		
3	Fmt_mode	Auto check for: 0:pal,1:ntsc
2	ref_mode	Use data or port control
1	Bt_mode	1: normal pasl/ntsc; 0: programe
0	bt_data_en	Enable of input

VBIST 0x01

Bit(s)	Name	Description
[12:0]	vbi0_start	The line number when vblanking started.

VBIEND 0x02

Bit(s)	Name	Description
[12:0]	vbi0_end	The line number when vblanking finished.

LINECTRL 0x04

Bit(s)	Name	Description
[31]	soft_video_active	0: control by vs/hs/field; 1: control by cnt and sw;
[30:16]	hend	The end of active pixel
[14:0]	hoffset	The start of active pixel

AVST 0x05

Bit(s)	Name	Description
[28:16]	video1_start	The start of active line, field1
[12:0]	video0_start	The start of active line, field0

AVEND 0x06

Bit(s)	Name	Description
[28:16]	video1_end	The end of active line, field1
[12:0]	video0_end	The end of active line, field0

PORT_CTRL 0x09

Bit(s)	Name	Description
[31:30]		
[29:28]	Pd_mem	Power down the memory
27	Vdo_rdy_bypass_eav	1: bypass eav for vdo_rdy
26	data_endian	0: afifo_wdata = {data1,data2} 1: afifo_wdata = {data2,data1}
25	clk_inv_sel	Reverse clk in
24	dual_edge_clk_en	Use dual edge clock
23	port_active_hmode	0: active data when hsync is low; 1: active data when hsync is high;
22	vref_fro_vs_only	0: use reference reverse vblank; 1： use vsync reverse vblank;
21	fid_hsvs_falling	For 601 format: 0: do not use falling edge of vsync 1:use falling edge of vsync
20	fid_hsvs_rising	For 601 format: 0: do not use rising edge of vsync 1:use rising edge of vsync
19	fid_hsvs_pcnt	For 601 format: 0： use hs/vs generate field； 1： use pixel cnt generate field;
9	bt_10bto8b	When use 8Bits data port: 0： [9:2]； 1： [9:2] + [1]；
8	bt_d8b	0： use 10Bits data port； 1： use 8Bits data port;
7	idq_phase	Reverse de port
6	idq_en	Enable de port
5	fid_hsvs	For 601 format: 0: use hs/vs generate fid; 1: use field port directly;
4	fid_phase	Reverse field port
[3:2]		
1	vsync_phase	Reverse vsync port
0	hsync_phase	Reverse hsync port

SWAP_CTRL 0x0a

Bit(s)	Name	Description
[14:12]	y1 sel	Y1 poistion
[10:8]	cr0 sel	Cr0 poistion
[6:4]	y0 sel	Y0 poistion
[2:0]	cb0 sel	Cb0 poistion

RAW_CTRL 0x13

Bit(s)	Name	Description
[11:9]	pixel_even,line_even	[r,g,b] output select
[8:6]	pixel_even,line_odd	[r,g,b] output select
[5:3]	pixel_odd,line_even	[r,g,b] output select
[2:0]	pixel_odd,line_odd	[r,g,b] output select

C601_CTRL0 0x0e

Bit(s)	Name	Description
[30:16]	even_field_cnt_max	
[14:0]	even_field_cnt_min	

C601_CTRL1 0x0f

Bit(s)	Name	Description
[30:16]	top_field_cnt_left_max	
[14:0]	top_field_cnt_left_min	

C601_CTRL2 0x10

Bit(s)	Name	Description
[21:16]	field_det_close_max	
[14:0]	top_field_cnt_right	

DELAY_CTRL 0x1d

Bit(s)	Name	Description
[30:28]	Vsync5	
[26:24]	Vsync4	
[22:20]	Fid	
[18:16]	Vsync3	
[14:12]	Vsync2	
[10:8]	Vsync1	
[6:4]	Hsync2	
[2:0]	Hsync1	

Interrupt Register

INTEN 0x15

Bit(s)	Name	Description
4	sof_int_en	Interrupt after sof
3	eof_int_en	Interrupt after eof
1	btin_ov_int_en	Interrupt after sync_fifo overflow
0	bt_error_int_en	Interrupt after error

ERRCNT 0x19

Bit(s)	Name	Description
[28:16]	max_line_cnt	When line number bigger than it, will generate an error
[14:0]	max_pix_cnt	When pixel number bigger than it, will generate an error

STATUS 0x14

Bit(s)	Name	Description
[31:15]		
14	fmt_st	Detect result of Pal/Ntsc mode
13	field_st	The field of current one
12	pre_field_st	The field of last one
11		
10		
9	sof_int_st	to 1 after interrupt occurs, to 0 after write This bit
8	eof_int_st	to 1 after interrupt occurs, to 0 after write This bit
7	btin_ov_st	to 1 after interrupt occurs, to 0 after write This bit
6	lcnt_error_st	to 1 after interrupt occurs, to 0 after write This bit
5	dcnt_error_st	to 1 after interrupt occurs, to 0 after write This bit
4	error_st	to 1 after interrupt occurs, to 0 after write This bit
[3:0]	bt_state	The state of fsm

Read Register

VLINE 0x17

Bit(s)	Name	Description
[12:0]	vline_num	Line number in one field

LUMA 0x12

Bit(s)	Name	Description
[31:0]	field_luma	Accumulated of Y

LCNT 0x1a

Bit(s)	Name	Description
[30:16]	dcnt_max	The maximum input counter in one line
[14:0]	dcnt_min	The minimum input counter in one line

PCNT 0x1c

Bit(s)	Name	Description
[30:16]	pcnt_max	The maximum pixel counter in one line
[14:0]	pcnt_min	The minimum pixel counter in one line

29. Video Output

this section ion describes S905's VPU sub-module, including CVBS sub-module.

29.1 CVBS

S905 supports CVBS 480i/576i standard definition output.

Register Definition

LCD Registers
L_Gamma Control

L_GAMMA_CNTL_PORT 0x1400

Bit(s)	Field Name	R/W	Default	Description
7	GAMMA_VCOM_POL	R/W	0	Reverse VCOM Polarity
6	GAMMA_RVS_OUT	R/W	0	GAMMA DATA REVERSE OUTPUT FOLLOWING VCOM
5	ADR_RDY	R	0	GAMMA ADDR PORT Is Ready for access
4	WR_RDY	R	0	GAMMA DATA PORT IS RDY to Write
3	RD_RDY	R	0	GAMMA DATA PORT IS RDY to Read
2	GAMMA_TR	R/W	0	RGB10-->RGB8 using Trancate or Round off
1	GAMMA_SET	R/W	0	Gamma turn on syncing with Vsync
0	GAMMA_EN	R/W	0	Gamma Enable

L_GAMMA_DATA_PORT 0x1401

Bit(s)	Field Name	R/W	Default	Description
15:0	GAMMA_DATA_PORT	-	0	GAMMA DATA PORT ADDR, all gamma data read/write operation is via this port

L_GAMMA_ADDR_PORT VCBUS: 0x1402

Bit(s)	Field Name	R/W	Default	Description
12	H-RD	R/W	0	GAMMA is READY for Host to read/write
11	H-AUTO_INC	R/W	0	BURST MODE *
10	H_SEL_R	R/W	0	GAMMA R Selected
9	H_SEL_G	R/W	0	GAMMA G Selected
8	H_SEL_B	R/W	0	GAMMA B Selected
7:0	HADR	W	0	GAMMA ADDR.

**NOTE:: When Programming the Gamma with Burst Mode, please turn off the IRQ service (Or make sure the IRQ service task have no Gamma programming operation)*

L_GAMMA_VCOM_HSWITCH_ADDR 0x1403

Bit(s)	Field Name	R/W	Default	Description
12:0	GAMMA_VCOM_HSWITCH_ADDR	R/W	0	Horizontal Switch Point for VCOM with Gamma

L_RGB_BASE_ADDR 0x1405

Bit(s)	Field Name	R/W	Default	Description
9:0	RGB_BASE_ADDR	R/W	0	RGB Converter OFFSET

L_RGB_COEFF_ADDR 0x1406

Bit(s)	Field Name	R/W	Default	Description
10:0	RGB_COEFF_ADDR	R/W	0	RGB Converter SCALE

L_POL_CNTL_ADDR 0x1407

Bit(s)	Field Name	R/W	Default	Description
15:14	DCLK_SEL	R/W	0	DCLK output
11	TCON_VSYNC_SEL_DVI	R/W	0	VSYNC generated by TCON for RGB format DVI output (support Digital LCD interface)
10	TCON_HSYNC_SEL_DVI	R/W	0	HSYNC generated by TCON for RGB format DVI output (support Digital LCD interface)
9	TCON_DE_SEL_DVI	R/W	0	DE generated by TCON for RGB format DVI output (support Digital LCD interface)
8	CPH3_POL	R/W	0	CPH3 Polarity Control
7	CPH2_POL	R/W	0	CPH2 Polarity Control
6	CPH1_POL	R/W	0	CPH1 Polarity Control
5	TCON_DE_SEL	R/W	0	DE Generate by TCON
4	TCON_VS_SEL	R/W	0	Vsync Generate by TCON
3	TCON_HS_SEL	R/W	0	Hsync Generate by TCON

Bit(s)	Field Name	R/W	Default	Description
2	DE_POL	R/W	0	De polarity control
1	VS_POL	R/W	0	Vsync polarity control
0	HS_POL	R/W	0	Hsync polarity control

L_DITH_CNTL_ADDR 0x1408

Bit(s)	Field Name	R/W	Default	Description
13	DITH_R5	R/W	0	1=use the current dithering to dither input 10-bit R down to 5-bit . Applicable only if both dith10_en & dith8_en = 1, otherwise no effect
12	DITH_G5	R/W	0	1=use the current dithering to dither input 10-bit G down to 5-bit . Applicable only if both dith10_en & dith8_en = 1, otherwise no effect
11	DITH_B5	R/W	0	1=use the current dithering to dither input 10-bit B down to 5-bit . Applicable only if both dith10_en & dith8_en = 1, otherwise no effect
10	DITH10_EN	R/W	0	10-bits Dithering to 8 Bits Enable
9	DITH8_EN	R/W	0	8-bits Dithering to 6 Bits Enable
8	DITH_MD	R/W	0	Dithering Mode select
7:4	DITH8_CNTL	R/W	0	8-bits Dithering control
3:0	DITH10_CNTL	R/W	0	10-bits Dithering control

L_GAMMA_PROBE_CTRL 0x1409

Bit(s)	Field Name	R/W	Default	Description
1	HIGHLIGHT_EN	R/W	0	
0	PROBE_EN	R/W	0	

L_GAMMA_PROBE_COLOR_L 0x140a

Bit(s)	Field Name	R/W	Default	Description
15:0	GAMMA_PROBE_COLOR_L	R	0	Probe_pix[15:0]

L_GAMMA_PROBE_COLOR_H 0x140b

Bit(s)	Field Name	R/W	Default	Description
15	PROBE_PIX_V	R	0	probe_pix_v
14	reserve	R	0	reserve
13:0	GAMMA_PROBE_COLOR_H	R	0	Probe_pix[29:16]

L_GAMMA_PROBE_HL_COLOR 0x140c

Bit(s)	Field Name	R/W	Default	Description
15:0	GAMMA_PROBE_HL_COLOR	R	0	5:6:5 color

L_GAMMA_PROBE_POS_X 0x140d

Bit(s)	Field Name	R/W	Default	Description
12:0	GAMMA_PROBE_POS_X	R/W	0	Pos_x

L_GAMMA_PROBE_POS_Y 0x140e

Bit(s)	Field Name	R/W	Default	Description
12:0	GAMMA_PROBE_POS_Y	R/W	0	Pos_y

L_TCON Control

L_STH1_HS_ADDR 0x1410

Bit(s)	Field Name	R/W	Default	Description
12:0	STH1_HS_ADDR	R/W	0	STH1 Horizontal Start

L_STH1_HE_ADDR 0x1411

Bit(s)	Field Name	R/W	Default	Description
12:0	STH1_HE_ADDR	R/W	0	STH1 Horizontal End

L_STH1_VS_ADDR 0x1412

Bit(s)	Field Name	R/W	Default	Description
12:0	STH1_VS_ADDR	R/W	0	STH1 Vertical Start

L_STH1_VE_ADDR 0x1413

Bit(s)	Field Name	R/W	Default	Description
12:0	STH1_VE_ADDR	R/W	0	STH1 Vertical End

L_STH2_HS_ADDR 0x1414

Bit(s)	Field Name	R/W	Default	Description
12:0	STH2_HS_ADDR	R/W	0	STH2 Horizontal Start

L_STH2_HE_ADDR 0x1415

Bit(s)	Field Name	R/W	Default	Description
12:0	STH2_HE_ADDR	R/W	0	STH2 Horizontal End

L_STH2_VS_ADDR 0x1416

Bit(s)	Field Name	R/W	Default	Description
12:0	STH2_VS_ADDR	R/W	0	STH2 Vertical Start

L_STH2_VE_ADDR 0x1417

Bit(s)	Field Name	R/W	Default	Description
12:0	STH2_VE_ADDR	R/W	0	STH2 Vertical End

L_OEH_HS_ADDR 0x1418

Bit(s)	Field Name	R/W	Default	Description
12:0	OEH_HS_ADDR	R/W	0	OEH Horizontal Start

L_OEH_HE_ADDR 0x1419

Bit(s)	Field Name	R/W	Default	Description
12:0	OEH_HE_ADDR	R/W	0	OEH Horizontal End

L_OEH_VS_ADDR 0x141a

Bit(s)	Field Name	R/W	Default	Description
12:0	OEH_VS_ADDR	R/W	0	OEH Vertical Start

L_OEH_VE_ADDR 0x141b

Bit(s)	Field Name	R/W	Default	Description
12:0	OEH_VE_ADDR	R/W	0	OEH Vertical End

L_VCOM_HSWITCH_ADDR 0x141c

Bit(s)	Field Name	R/W	Default	Description
12:0	VCOM_HSWITCH_ADDR	R/W	0	VCOM Horizontal Switch Point

L_VCOM_VS_ADDR 0x141d

Bit(s)	Field Name	R/W	Default	Description
12:0	VCOM_VS_ADDR	R/W	0	VCOM Vertical Start

L_VCOM_VE_ADDR 0x141e

Bit(s)	Field Name	R/W	Default	Description
12:0	VCOM_VE_ADDR	R/W	0	VCOM Vertical End

L_CPV1_HS_ADDR 0x141f

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV1_HS_ADDR	R/W	0	CPV1 Horizontal Start

L_CPV1_HE_ADDR 0x1420

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV1_HE_ADDR	R/W	0	CPV1 Horizontal End

L_CPV1_VS_ADDR 0x1421

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV1_VS_ADDR	R/W	0	CPV1 Vertical Start

L_CPV1_VE_ADDR 0x1422

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV1_VE_ADDR	R/W	0	CPV1 Vertical End

L_CPV2_HS_ADDR 0x1423

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV2_HS_ADDR	R/W	0	CPV2 Horizontal Start

L_CPV2_HE_ADDR 0x1424

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV2_HE_ADDR	R/W	0	CPV2 Horizontal End

L_CPV2_VS_ADDR 0x1425

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV2_VS_ADDR	R/W	0	CPV2 Vertical Start

L_CPV2_VE_ADDR 0x1426

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV2_VE_ADDR	R/W	0	CPV2 Vertical End

L_STV1_HS_ADDR 0x1427

Bit(s)	Field Name	R/W	Default	Description
12:0	STV1_HS_ADDR	R/W	0	STV1 Horizontal Start

L_STV1_HE_ADDR 0x1428

Bit(s)	Field Name	R/W	Default	Description
12:0	STV1_HE_ADDR	R/W	0	STV1 Horizontal End

L_STV1_VS_ADDR 0x1429

Bit(s)	Field Name	R/W	Default	Description
12:0	STV1_VS_ADDR	R/W	0	STV1 Vertical Start

L_STV1_VE_ADDR 0x142a

Bit(s)	Field Name	R/W	Default	Description
12:0	STV1_VE_ADDR	R/W	0	STV1 Vertical End

L_STV2_HS_ADDR 0x142b

Bit(s)	Field Name	R/W	Default	Description
12:0	STV2_HS_ADDR	R/W	0	STV2 Horizontal Start

L_STV2_HE_ADDR 0x142c

Bit(s)	Field Name	R/W	Default	Description
12:0	STV2_HE_ADDR	R/W	0	STV2 Horizontal End

L_STV2_VS_ADDR 0x142d

Bit(s)	Field Name	R/W	Default	Description
12:0	STV2_VS_ADDR	R/W	0	STV2 Vertical Start

L_STV2_VE_ADDR 0x142e

Bit(s)	Field Name	R/W	Default	Description
12:0	STV2_VE_ADDR	R/W	0	STV2 Vertical End

L_OEV1_HS_ADDR 0x142f

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV1_HS_ADDR	R/W	0	OEV1 Horizontal Start

L_OEV1_HE_ADDR 0x1430

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV1_HE_ADDR	R/W	0	OEV1 Horizontal End

L_OEV1_VS_ADDR 0x1431

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV1_VS_ADDR	R/W	0	OEV1 Vertical Start

L_OEV1_VE_ADDR 0x1432

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV1_VE_ADDR	R/W	0	OEV1 Vertical End

L_OEV2_HS_ADDR 0x1433

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV2_HS_ADDR	R/W	0	OEV2 Horizontal Start

L_OEV2_HE_ADDR 0x1434

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV2_HE_ADDR	R/W	0	OEV2 Horizontal End

L_OEV2_VS_ADDR 0x1435

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV2_VS_ADDR	R/W	0	OEV2 Vertical Start

L_OEV2_VE_ADDR 0x1436

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV2_VE_ADDR	R/W	0	OEV2 Vertical End

L_OEV3_HS_ADDR 0x1437

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV3_HS_ADDR	R/W	0	OEV3 Horizontal Start

L_OEV3_HE_ADDR 0x1438

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV3_HE_ADDR	R/W	0	OEV3 Horizontal End

L_OEV3_VS_ADDR 0x1439

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV3_VS_ADDR	R/W	0	OEV3 Vertical Start

L_OEV3_VE_ADDR 0x143a

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV3_VE_ADDR	R/W	0	OEV3 Vertical End

L_LCD_PWR_ADDR 0x143b (Unused)

Bit(s)	Field Name	R/W	Default	Description
5	LCD_VDD	R/W	0	LCD VDD control
4	LCD_VBL	R/W	0	LCD VBL control
3:0	LCD_GPIO	R/W	0	LCD GPIO control

L_LCD_PWM0_LO_ADDR 0x143c (Unused)

Bit(s)	Field Name	R/W	Default	Description
12:0	LCD_PWM0_LO_ADDR	R/W	0	LOW Count

L_LCD_PWM0_HI_ADDR 0x143d (Unused)

Bit(s)	Field Name	R/W	Default	Description
12:0	LCD_PWM0_HI_ADDR	R/W	0	High Count

L_LCD_PWM1_LO_ADDR 0x143e (Unused)

Bit(s)	Field Name	R/W	Default	Description
12:0	LCD_PWM0_LO_ADDR	R/W	0	LOW Count

L_LCD_PWM1_HI_ADDR 0x143f(Unused)

Bit(s)	Field Name	R/W	Default	Description
12:0	LCD_PWM0_HI_ADDR	R/W	0	High Count

L_INV_CNT_ADDR 0x1440

Bit(s)	Field Name	R/W	Default	Description
4	INV_EN	R/W	0	Invert data output Enable
3:0	INV_CNT	R/W	0	Invert data count define

L_TCON_MISC_SEL_ADDR 0x1441

Bit(s)	Field Name	R/W	Default	Description
12	STH2_SEL	R/W	0	STH2 is Line signal
11	STH1_SEL	R/W	0	STH1 is Line Signal
10	OEH_SEL	R/W	0	OEH is Line Signal
9	VCOM_SEL	R/W	0	VCOM is Line Signal
8	DB_LINE_SW	R/W	0	VCOM switched double lines
7	CPV2_SEL	R/W	0	CPV2 is Line Signal
6	CPV1_SEL	R/W	0	CPV1 is Line Signal
5	STV2_SEL	R/W	1	STV2 is frame Signal
4	STV1_SEL	R/W	1	STV1 is frame Signal
3	OEV_UNITE	R/W	1	OEV3/2/1 look like one signal
2	OEV3_SEL	R/W	0	OEV3 is Line Signal
1	OEV2_SEL	R/W	0	OEV2 is Line Signal
0	OEV1_SEL	R/W	0	OEV1 is Line Signal

L_DUAL_PORT_CNTL_ADDR 0x1442

Bit(s)	Field Name	R/W	Default	Description
15	OUTPUT_YUV	R/W	0	
14:12	IDF	R.W	0	
11:9	ISF	R/W	0	
8	LCD_ANALOG_SEL_CPH3	R/W	0	CPH3/INVT pin select
7	LCD_ANALOG_3PHI_CLK_SEL	R/W	0	CPH3/2/1 Output 3 phases
6	LCD_LVDS_SEL54	R/W	0	
5	LCD_LVDS_SEL27	R/W	0	
4	LCD_TTL_SEL	R/W	0	
3	DUAL_LVDS_EN	R/W	0	
2	PORT_SWP	R/W	0	
1	RGB_SWP	R/W	0	R/B Swapped in data path
0	BIT_SWP	R/W	0	Bit Swap in data path(7:0→0:7)

MLVDS_CLK_CTL1_HI 0x1443 (Unused in Athena)

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shi

MLVDS_CLK_CTL1_LO 0x1444 (Unused)

Bit(s)	R/W	Default	Description
31-30	R/W	0	Enable mlvds clocks
24	R/W	0	Mlvds_clk_half_delay
23:0	R/W	0	Mlvds_clk_pattern

L_TCON_DOUBLE_CTL 0x1449

Bit(s)	R/W	Default	Description
16	W	0	tcon_double_reset

Bit(s)	R/W	Default	Description
15:8	R/W	0	tcon_double_ini
7:0	R/w	0	tcon_double_inv

L_TCON_PATTERN_HI 0x144a

Bit(s)	R/W	Default	Description
15:0	R/W	0	tcon_pattern[31:16]

L_TCON_PATTERN_LO 0x144b

Bit(s)	R/W	Default	Description
15:0	R/W	0	tcon_pattern[15:0]

LDIM_BL_ADDR_PORT 0x144e

Bit(s)	Field Name	R/W	Default	Description
	LDIM_BL_ADDR_PORT	R/W	0	N/A

LDIM_BL_DATA_PORT 0x144f

Bit(s)	Field Name	R/W	Default	Description
	LDIM_BL_DATA_PORT	R/W	0	N/A

L_DE_HS_ADDR 0x1451

Bit(s)	Field Name	R/W	Default	Description
15:14	enable_tcon_double[7:6]	R/W	0	enable_tcon_double[7:6]
12:0	de_hs	R/W	0	DE Horizontal Start

L_DE_HE_ADDR 0x1452

Bit(s)	Field Name	R/W	Default	Description
15:14	enable_tcon_double[5:4]	R/W	0	enable_tcon_double[5:4]
12:0	DE_HE_ADDR	R/W	0	DE Horizontal End

L_DE_VS_ADDR 0x1453

Bit(s)	Field Name	R/W	Default	Description
15:14	enable_tcon_double[3:2]	R/W	0	enable_tcon_double[3:2]
12:0	DE_VS_ADDR	R/W	0	DE Vertical Start

L_DE_VE_ADDR 0x1454

Bit(s)	Field Name	R/W	Default	Description
15:14	enable_tcon_double[1:0]	R/W	0	enable_tcon_double[1:0]
12:0	DE_VE_ADDR	R/W	0	DE Vertical End

L_HSYNC_HS_ADDR 0x1455

Bit(s)	Field Name	R/W	Default	Description
12:0	HSYNC_HS_ADDR	R/W	0	HSYNC Horizontal Start

L_HSYNC_HE_ADDR 0x1456

Bit(s)	Field Name	R/W	Default	Description
12:0	HSYNC_HE_ADDR	R/W	0	HSYNC Horizontal End

L_HSYNC_VS_ADDR 0x1457

Bit(s)	Field Name	R/W	Default	Description
12:0	HSYNC_VS_ADDR	R/W	0	HSYNC Vertical Start

L_HSYNC_VE_ADDR 0x1458

Bit(s)	Field Name	R/W	Default	Description
12:0	HSYNC_VE_ADDR	R/W	0	HSYNC Vertical End

L_VSYNC_HS_ADDR 0x1459

Bit(s)	Field Name	R/W	Default	Description
12:0	VSYNC_HS_ADDR	R/W	0	VSYNC Horizontal Start

L_VSYNC_HE_ADDR 0x145a

Bit(s)	Field Name	R/W	Default	Description
12:0	VSYNC_HE_ADDR	R/W	0	VSYNC Horizontal End

L_VSYNC_VS_ADDR 0x145b

Bit(s)	Field Name	R/W	Default	Description
12:0	VSYNC_VS_ADDR	R/W	0	VSYNC Vertical Start

L_VSYNC_VE_ADDR 0x145c

Bit(s)	Field Name	R/W	Default	Description
12:0	VSYNC_VE_ADDR	R/W	0	VSYNC Vertical End

L_LCD_MCU_CTL 0x145d

Bit(s)	Field Name	R/W	Default	Description
11:10	MCU_SOURCE	R/W	0	mcu_source
9	DISABLE_GAMMA_10B	R/W	0	If true, disable GAMMA 10bit input resolution(8bit input)
8	VFIFO_MCU_ENABLE	R/W	0	Read data from viu vfifo output
7	HALT_VS_DE	R/W	0	0: after vsync, halt the encp venc 1: after vsync and DE, halt encp venc
6	R8G8B8_FORMAT	R/W	0	If true, RGB888
5	R6G6B6_FORMAT	R/W	0	If true RGB666
4	R5G6B5_FORMAT	R/W	0	If true RGB565
3	DAC_DITH_SEL	R/W	0	If true, dither result is selected to VDAC
2	LCD_MCU_ENABLE_DE	R	0	Read only
1	LCD_MCU_ENABLE_VSYNC	R	0	Read only
0	LCD_MCU_ENABLE	R/W	0	LCD MCU interface enable

Gamma Control

GAMMA_CNTL_PORT 0x1480

Bit(s)	Field Name	R/W	Default	Description
7	GAMMA_VCOM_POL	R/W	0	Reverse VCOM Polarity
6	GAMMA_RVS_OUT	R/W	0	GAMMA DATA REVERSE OUTPUT FOLLOWING VCOM
5	ADR_RDY	R	0	GAMMA ADDR PORT Is Ready for access
4	WR_RDY	R	0	GAMMA DATA PORT IS RDY to Write
3	RD_RDY	R	0	GAMMA DATA PORT IS RDY to Read
2	GAMMA_TR	R/W	0	RGB10-->RGB8 using Trancate or Round off
1	GAMMA_SET	R/W	0	Gamma turn on syncing with Vsync
0	GAMMA_EN	R/W	0	Gamma Enable

GAMMA_DATA_PORT 0x1481

Bit(s)	Field Name	R/W	Default	Description
15:0	GAMMA_DATA_PORT	-	0	GAMMA DATA PORT ADDR, all gamma data read/write operation is via this port

GAMMA_ADDR_PORT 0x1482

Bit(s)	Field Name	R/W	Default	Description
12	H-RD	R/W	0	GAMMA is READY for Host to read/write
11	H-AUTO_INC	R/W	0	BURST MODE *
10	H_SEL_R	R/W	0	GAMMA R Selected
9	H_SEL_G	R/W	0	GAMMA G Selected
8	H_SEL_B	R/W	0	GAMMA B Selected
7:0	HADR	W	0	GAMMA ADDR.

**NOTE:: When Programming the Gamma with Burst Mode, please turn off the IRQ service (Or make sure the IRQ service task have no Gamma programming operation)*

GAMMA_VCOM_HSWITCH_ADDR 0x1483

Bit(s)	Field Name	R/W	Default	Description
12:0	GAMMA_VCOM_HSWITCH_ADDR	R/W	0	Horizontal Switch Point for VCOM with Gamma

RGB_BASE_ADDR 0x1485

Bit(s)	Field Name	R/W	Default	Description
9:0	RGB_BASE_ADDR	R/W	0	RGB Converter OFFSET

RGB_COEFF_ADDR 0x1486

Bit(s)	Field Name	R/W	Default	Description
10:0	RGB_COEFF_ADDR	R/W	0	RGB Converter SCALE

POL_CNTL_ADDR 0x1487

Bit(s)	Field Name	R/W	Default	Description
15:14	DCLK_SEL	R/W	0	DCLK output
11	TCON_VSYNC_SEL_DVI	R/W	0	VSYNC generated by TCON for RGB format DVI output (support Digital LCD interface)
10	TCON_HSYNC_SEL_DVI	R/W	0	HSYNC generated by TCON for RGB format DVI output (support Digital LCD interface)
9	TCON_DE_SEL_DVI	R/W	0	DE generated by TCON for RGB format DVI output (support Digital LCD interface)
8	CPH3_POL	R/W	0	CPH3 Polarity Control
7	CPH2_POL	R/W	0	CPH2 Polarity Control
6	CPH1_POL	R/W	0	CPH1 Polarity Control

Bit(s)	Field Name	R/W	Default	Description
5	TCON_DE_SEL	R/W	0	DE Generate by TCON
4	TCON_VS_SEL	R/W	0	Vsync Generate by TCON
3	TCON_HS_SEL	R/W	0	Hsync Generate by TCON
2	DE_POL	R/W	0	De polarity control
1	VS_POL	R/W	0	Vsync polarity control
0	HS_POL	R/W	0	Hsync polarity control

DITH_CNTL_ADDR 0x1488

Bit(s)	Field Name	R/W	Default	Description
13	DITH_R5	R/W	0	1=use the current dithering to dither input 10-bit R down to 5-bit . Applicable only if both dith10_en & dith8_en = 1, otherwise no effect
12	DITH_G5	R/W	0	1=use the current dithering to dither input 10-bit G down to 5-bit . Applicable only if both dith10_en & dith8_en = 1, otherwise no effect
11	DITH_B5	R/W	0	1=use the current dithering to dither input 10-bit B down to 5-bit . Applicable only if both dith10_en & dith8_en = 1, otherwise no effect
10	DITH10_EN	R/W	0	10-bits Dithering to 8 Bits Enable
9	DITH8_EN	R/W	0	8-bits Dithering to 6 Bits Enable
8	DITH_MD	R/W	0	Dithering Mode select
7:4	DITH8_CNTL	R/W	0	8-bits Dithering control
3:0	DITH10_CNTL	R/W	0	10-bits Dithering control

GAMMA_PROBE_CTRL 0x1489

Bit(s)	Field Name	R/W	Default	Description
1	HIGHLIGHT_EN	R/W	0	
0	PROBE_EN	R/W	0	

GAMMA_PROBE_COLOR_L 0x148a

Bit(s)	Field Name	R/W	Default	Description
15:0	GAMMA_PROBE_COLOR_L	R	0	Probe_pix[15:0]

GAMMA_PROBE_COLOR_H 0x148b

Bit(s)	Field Name	R/W	Default	Description
15	PROBE_PIX_V	R	0	probe_pix_v
14	reserve	R	0	reserve
13:0	GAMMA_PROBE_COLOR_H	R	0	Probe_pix[29:16]

GAMMA_PROBE_HL_COLOR 0x148c

Bit(s)	Field Name	R/W	Default	Description
15:0	GAMMA_PROBE_HL_COLOR	R	0	5:6:5 color

GAMMA_PROBE_POS_X 0x148d

Bit(s)	Field Name	R/W	Default	Description
12:0	GAMMA_PROBE_POS_X	R/W	0	Pos_x

GAMMA_PROBE_POS_Y 0x148e

Bit(s)	Field Name	R/W	Default	Description
12:0	GAMMA_PROBE_POS_Y	R/W	0	Pos_y

TCON Control

STH1_HS_ADDR 0x1490

Bit(s)	Field Name	R/W	Default	Description
12:0	STH1_HS_ADDR	R/W	0	STH1 Horizontal Start

STH1_HE_ADDR 0x1491

Bit(s)	Field Name	R/W	Default	Description
12:0	STH1_HE_ADDR	R/W	0	STH1 Horizontal End

STH1_VS_ADDR 0x1492

Bit(s)	Field Name	R/W	Default	Description
12:0	STH1_VS_ADDR	R/W	0	STH1 Vertical Start

STH1_VE_ADDR 0x1493

Bit(s)	Field Name	R/W	Default	Description
12:0	STH1_VE_ADDR	R/W	0	STH1 Vertical End

STH2_HS_ADDR 0x1494

Bit(s)	Field Name	R/W	Default	Description
12:0	STH2_HS_ADDR	R/W	0	STH2 Horizontal Start

STH2_HE_ADDR 0x1495

Bit(s)	Field Name	R/W	Default	Description
12:0	STH2_HE_ADDR	R/W	0	STH2 Horizontal End

STH2_VS_ADDR 0x1496

Bit(s)	Field Name	R/W	Default	Description
12:0	STH2_VS_ADDR	R/W	0	STH2 Vertical Start

STH2_VE_ADDR 0x1497

Bit(s)	Field Name	R/W	Default	Description
12:0	STH2_VE_ADDR	R/W	0	STH2 Vertical End

OEH_HS_ADDR 0x1498

Bit(s)	Field Name	R/W	Default	Description
12:0	OEH_HS_ADDR	R/W	0	OEH Horizontal Start

OEH_HE_ADDR 0x1499

Bit(s)	Field Name	R/W	Default	Description
12:0	OEH_HE_ADDR	R/W	0	OEH Horizontal End

OEH_VS_ADDR 0x149a

Bit(s)	Field Name	R/W	Default	Description
12:0	OEH_VS_ADDR	R/W	0	OEH Vertical Start

OEH_VE_ADDR 0x149b

Bit(s)	Field Name	R/W	Default	Description
12:0	OEH_VE_ADDR	R/W	0	OEH Vertical End

VCOM_HSWITCH_ADDR 0x149c

Bit(s)	Field Name	R/W	Default	Description
12:0	VCOM_HSWITCH_ADDR	R/W	0	VCOM Horizontal Switch Point

VCOM_VS_ADDR 0x149d

Bit(s)	Field Name	R/W	Default	Description
12:0	VCOM_VS_ADDR	R/W	0	VCOM Vertical Start

VCOM_VE_ADDR 0x149e

Bit(s)	Field Name	R/W	Default	Description
12:0	VCOM_VE_ADDR	R/W	0	VCOM Vertical End

CPV1_HS_ADDR 0x149f

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV1_HS_ADDR	R/W	0	CPV1 Horizontal Start

CPV1_HE_ADDR 0x14a0

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV1_HE_ADDR	R/W	0	CPV1 Horizontal End

CPV1_VS_ADDR 0x14a1

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV1_VS_ADDR	R/W	0	CPV1 Vertical Start

CPV1_VE_ADDR 0x14a2

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV1_VE_ADDR	R/W	0	CPV1 Vertical End

CPV2_HS_ADDR 0x14a3

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV2_HS_ADDR	R/W	0	CPV2 Horizontal Start

CPV2_HE_ADDR 0x14a4

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV2_HE_ADDR	R/W	0	CPV2 Horizontal End

CPV2_VS_ADDR 0x14a5

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV2_VS_ADDR	R/W	0	CPV2 Vertical Start

CPV2_VE_ADDR 0x14a6

Bit(s)	Field Name	R/W	Default	Description
12:0	CPV2_VE_ADDR	R/W	0	CPV2 Vertical End

STV1_HS_ADDR 0x14a7

Bit(s)	Field Name	R/W	Default	Description
12:0	STV1_HS_ADDR	R/W	0	STV1 Horizontal Start

STV1_HE_ADDR 0x14a8

Bit(s)	Field Name	R/W	Default	Description
12:0	STV1_HE_ADDR	R/W	0	STV1 Horizontal End

STV1_VS_ADDR 0x14a9

Bit(s)	Field Name	R/W	Default	Description
12:0	STV1_VS_ADDR	R/W	0	STV1 Vertical Start

STV1_VE_ADDR 0x14aa

Bit(s)	Field Name	R/W	Default	Description
12:0	STV1_VE_ADDR	R/W	0	STV1 Vertical End

STV2_HS_ADDR 0x14ab

Bit(s)	Field Name	R/W	Default	Description
12:0	STV2_HS_ADDR	R/W	0	STV2 Horizontal Start

STV2_HE_ADDR 0x14ac

Bit(s)	Field Name	R/W	Default	Description
12:0	STV2_HE_ADDR	R/W	0	STV2 Horizontal End

STV2_VS_ADDR 0x14ad

Bit(s)	Field Name	R/W	Default	Description
12:0	STV2_VS_ADDR	R/W	0	STV2 Vertical Start

STV2_VE_ADDR 0x14ae

Bit(s)	Field Name	R/W	Default	Description
12:0	STV2_VE_ADDR	R/W	0	STV2 Vertical End

OEV1_HS_ADDR 0x14af

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV1_HS_ADDR	R/W	0	OEV1 Horizontal Start

OEV1_HE_ADDR 0x14b0

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV1_HE_ADDR	R/W	0	OEV1 Horizontal End

OEV1_VS_ADDR 0x14b1

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV1_VS_ADDR	R/W	0	OEV1 Vertical Start

OEV1_VE_ADDR 0x14b2

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV1_VE_ADDR	R/W	0	OEV1 Vertical End

OEV2_HS_ADDR 0x14b3

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV2_HS_ADDR	R/W	0	OEV2 Horizontal Start

OEV2_HE_ADDR 0x14b4

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV2_HE_ADDR	R/W	0	OEV2 Horizontal End

OEV2_VS_ADDR 0x14b5

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV2_VS_ADDR	R/W	0	OEV2 Vertical Start

OEV2_VE_ADDR 0x14b6

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV2_VE_ADDR	R/W	0	OEV2 Vertical End

OEV3_HS_ADDR 0x14b7

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV3_HS_ADDR	R/W	0	OEV3 Horizontal Start

OEV3_HE_ADDR 0x14b8

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV3_HE_ADDR	R/W	0	OEV3 Horizontal End

OEV3_VS_ADDR 0x14b9

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV3_VS_ADDR	R/W	0	OEV3 Vertical Start

OEV3_VE_ADDR 0x14ba

Bit(s)	Field Name	R/W	Default	Description
12:0	OEV3_VE_ADDR	R/W	0	OEV3 Vertical End

LCD_PWR_ADDR 0x14bb (Unused)

Bit(s)	Field Name	R/W	Default	Description
5	LCD_VDD	R/W	0	LCD VDD control
4	LCD_VBL	R/W	0	LCD VBL control
3:0	LCD_GPIO	R/W	0	LCD GPIO control

LCD_PWM0_LO_ADDR 0x14bc (Unused)

Bit(s)	Field Name	R/W	Default	Description
12:0	LCD_PWM0_LO_ADDR	R/W	0	LOW Count

LCD_PWM0_HI_ADDR 0x14bd (Unused)

Bit(s)	Field Name	R/W	Default	Description
12:0	LCD_PWM0_HI_ADDR	R/W	0	High Count

LCD_PWM1_LO_ADDR 0x14be (Unused)

Bit(s)	Field Name	R/W	Default	Description
12:0	LCD_PWM0_LO_ADDR	R/W	0	LOW Count

LCD_PWM1_HI_ADDR 0x14bf (Unused)

Bit(s)	Field Name	R/W	Default	Description
12:0	LCD_PWM0_HI_ADDR	R/W	0	High Count

INV_CNT_ADDR 0x14c0

Bit(s)	Field Name	R/W	Default	Description
4	INV_EN	R/W	0	Invert data output Enable
3:0	INV_CNT	R/W	0	Invert data count define

TCON_MISC_SEL_ADDR 0x14c1

Bit(s)	Field Name	R/W	Default	Description
12	STH2_SEL	R/W	0	STH2 is Line signal
11	STH1_SEL	R/W	0	STH1 is Line Signal
10	OEH_SEL	R/W	0	OEH is Line Signal
9	VCOM_SEL	R/W	0	VCOM is Line Signal
8	DB_LINE_SW	R/W	0	VCOM switched double lines
7	CPV2_SEL	R/W	0	CPV2 is Line Signal
6	CPV1_SEL	R/W	0	CPV1 is Line Signal
5	STV2_SEL	R/W	1	STV2 is frame Signal
4	STV1_SEL	R/W	1	STV1 is frame Signal
3	OEV_UNITE	R/W	1	OEV3/2/1 look like one signal
2	OEV3_SEL	R/W	0	OEV3 is Line Signal
1	OEV2_SEL	R/W	0	OEV2 is Line Signal
0	OEV1_SEL	R/W	0	OEV1 is Line Signal

DUAL_PORT_CNTL_ADDR 0x14c2

Bit(s)	Field Name	R/W	Default	Description
15	OUTPUT_YUV	R/W	0	
14:12	IDF	R.W	0	
11:9	ISF	R/W	0	
8	LCD_ANALOG_SEL_CPH3	R/W	0	CPH3/INVT pin select
7	LCD_ANALOG_3PHI_CLK_SEL	R/W	0	CPH3/2/1 Output 3 phases
6	LCD_LVDS_SEL54	R/W	0	
5	LCD_LVDS_SEL27	R/W	0	
4	LCD_TTL_SEL	R/W	0	
3	DUAL_LVDS_EN	R/W	0	
2	PORT_SWP	R/W	0	
1	RGB_SWP	R/W	0	R/B Swapped in data path
0	BIT_SWP	R/W	0	Bit Swap in data path(7:0→0:7)

LVDS_PACK_CNTL_ADDR 0x14d0

Bit(s)	Field Name	R/W	Default	Description
15:14	G_SELECT	R/W	0	0:R, 1:G, 2:B, 3:0
13:12	G_SELECT	R/W	0	0:R, 1:G, 2:B, 3:0
11:10	R_SELECT	R/W	0	0:R, 1:G, 2:B, 3:0
9:8	BIT_SIZE	R/W	0	0:10Bits, 1:8Bits, 2:6Bits, 3:4Bits
7	LVDS_USE_TCON	R/W	0	hs, vs, de controlled by tcon
6	LVDS_DUAL	R/W	0	dual port mapping
5	PN_SWP	R/W	0	pn_swp
4	LSB_FIRST	R/W	0	0:MSB first, 1:LSB first
3	LVDS_RESV	R/W	0	invert hs and vs

Bit(s)	Field Name	R/W	Default	Description
2	ODD_EVEN_SWP	R/W	0	0:normal, 1:swap
1:0	LVDS_rEPACK	R/W	0	0:normal, 1,2:repack

DE_HS_ADDR 0x14d1

Bit(s)	Field Name	R/W	Default	Description
12:0	DE_HS_ADDR	R/W	0	DE Horizontal Start

DE_HE_ADDR 0x14d2

Bit(s)	Field Name	R/W	Default	Description
12:0	DE_HE_ADDR	R/W	0	DE Horizontal End

DE_VS_ADDR 0x14d3

Bit(s)	Field Name	R/W	Default	Description
12:0	DE_VS_ADDR	R/W	0	DE Vertical Start

DE_VE_ADDR 0x14d4

Bit(s)	Field Name	R/W	Default	Description
12:0	DE_VE_ADDR	R/W	0	DE Vertical End

HSYNC_HS_ADDR 0x14d5

Bit(s)	Field Name	R/W	Default	Description
12:0	HSYNC_HS_ADDR	R/W	0	HSYNC Horizontal Start

HSYNC_HE_ADDR 0x14d6

Bit(s)	Field Name	R/W	Default	Description
12:0	HSYNC_HE_ADDR	R/W	0	HSYNC Horizontal End

HSYNC_VS_ADDR 0x14d7

Bit(s)	Field Name	R/W	Default	Description
12:0	HSYNC_VS_ADDR	R/W	0	HSYNC Vertical Start

HSYNC_VE_ADDR 0x14d8

Bit(s)	Field Name	R/W	Default	Description
12:0	HSYNC_VE_ADDR	R/W	0	HSYNC Vertical End

VSYNC_HS_ADDR 0x14d9

Bit(s)	Field Name	R/W	Default	Description
12:0	VSYNC_HS_ADDR	R/W	0	VSYNC Horizontal Start

VSYNC_HE_ADDR 0x14da

Bit(s)	Field Name	R/W	Default	Description
12:0	VSYNC_HE_ADDR	R/W	0	VSYNC Horizontal End

VSYNC_VS_ADDR 0x14db

Bit(s)	Field Name	R/W	Default	Description
12:0	VSYNC_VS_ADDR	R/W	0	VSYNC Vertical Start

VSYNC_VE_ADDR 0x14dc

Bit(s)	Field Name	R/W	Default	Description
12:0	VSYNC_VE_ADDR	R/W	0	VSYNC Vertical End

LCD_MCU_CTL 0x14dd

Bit(s)	Field Name	R/W	Default	Description
11:10	MCU_SOURCE	R/W	0	mcu_source
9	DISABLE_GAMMA_10B	R/W	0	If true, disable GAMMA 10bit input resolution(8bit input)
8	VFIFO_MCU_ENABLE	R/W	0	Read data from viu vfifo output
7	HALT_VS_DE	R/W	0	0: after vsync, halt the encp venc 1: after vsync and DE, halt encp venc
6	R8G8B8_FORMAT	R/W	0	If true, RGB888
5	R6G6B6_FORMAT	R/W	0	If true RGB666
4	R5G6B5_FORMAT	R/W	0	If true RGB565
3	DAC_DITH_SEL	R/W	0	If true, dither result is selected to VDAC
2	LCD_MCU_ENABLE_DE	R	0	Read only
1	LCD_MCU_ENABLE_VSYNC	R	0	Read only
0	LCD_MCU_ENABLE	R/W	0	LCD MCU interface enable

LCD_MCU_DATA_0 0x14de

Bit(s)	Field Name	R/W	Default	Description
15-0		R	0	If RGB565 mode 15:11 R, 10:5 G, 4:0 B Else If (RGB666 or RGB888) 15:8 G, 7:0 R Else 14:10 G[4:0], 9:0 R

LCD_MCU_DATA_1 0x14de

Bit(s)	Field Name	R/W	Default	Description

15-0		R	0	If (RGB666 or RGB888)
				15:8 G, 7:0 B
				Else
				14:10 G[9:5], 9:0 B

LVDS Registers

LVDS_GEN_CNTL 0x14e0

Bit(s)	R/W	Default	Description
15	R/W	0	Mini LVDS (Ask Chen Shi)
14-11	R/W	0	unused
10:6	R/W	0	LVDS_PHY_MODE,unused
5-4	R/W	0	LVDS_FIFO_CLK_SEL: 0 = PHY clock divided by 6 1 = PHY clock divided by 7 2 = PHY clock divided by 8
3	R/W	0	FIFO_WR_EN: Set to 1 to enable the LVDS FIFO
2	R/W	0	FIFO_WR_BIST_GATE: This bit is used during production test to enable the FIFO writes at a particular time to ensure the data sent is consistent from run to run
1-0	R/W	0	FIFO_WR_MODE: 0 = FIFO disabled 1 = FIFO enabled 2 = FIFO write = DCLK / 2 3 = FIFO write = signal control (preferred)

LVDS_PHY_CNTL0 0x14e1 (Unused)

Bit(s)	R/W	Default	Description
15-11	R/W	0	unused
10	R/W	0	LVDS_CLKSEL_CHCK
9	R/W	0	LVDS_CLKSEL_CH5
8	R/W	0	LVDS_CLKSEL_CH4
7	R/W	0	LVDS_CLKSEL_CH3
6	R/W	0	LVDS_CLKSEL_CH2
5	R/W	0	LVDS_CLKSEL_CH1
4	R/W	0	LVDS_CLKSEL_CH0
3-0	R/W	0	LVDS_CTL_REG

LVDS_PHY_CNTL1 0x14e2 (Unused)

Bit(s)	R/W	Default	Description
15	R/W	0	unused
14	R/W	0	LVDS_PDN_CHCK
13	R/W	0	LVDS_PDN_CH5
12	R/W	0	LVDS_PDN_CH4
11	R/W	0	LVDS_PDN_CH3
10	R/W	0	LVDS_PDN_CH2
9	R/W	0	LVDS_PDN_CH1
8	R/W	0	LVDS_PDN_CH0
7	R/W	0	Unused
6	R/W	0	LVDS_DININV_CHCK
5	R/W	0	LVDS_DININV_CH5
4	R/W	0	LVDS_DININV_CH4
3	R/W	0	LVDS_DININV_CH3
2	R/W	0	LVDS_DININV_CH2
1	R/W	0	LVDS_DININV_CH1
0	R/W	0	LVDS_DININV_CH0

LVDS_PHY_CNTL2 0x14e3 (Unused)

Bit(s)	R/W	Default	Description
15-0	R/W	0	unused

LVDS_PHY_CNTL3 0x14e4 (Unused)

Bit(s)	R/W	Default	Description
15-12	R/W	0	unused
11-0	R/W	0	LVDS_COMMON

LVDS_PHY_CNTL4 0x14e5) (Unused)

Bit(s)	R/W	Default	Description
15-7	R/W	0	unused
6-0	R/W	0	LVDS_MDR_PU

LVDS_PHY_CNTL5 0x14e6 (Unused)

Bit(s)	R/W	Default	Description
15-11	R/W	0	LVDS_REFCTL
10-8	R/W	0	LVDS_VCM_CTL
7-4	R/W	0	LVDS_SWING_CTL
3-0	R/W	0	LVDS_PREM_CTL

LVDS_SRG_TEST 0x14e8 (Unused)

Bit(s)		R/W	Default	Description
12-0		R	0	unused

LVDS_BIST_MUX0 0x14e9

Bit(s)	R/W	Default	Description
15-14	R/W	0	B2 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED2 (see below)
13-12	R/W	0	B1 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED1 (see below)
11-10	R/W	0	B0 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED0 (see below)
9-8	R/W	0	A4 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED0 (see below)
7-6	R/W	0	A3 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED3 (see below)
5-4	R/W	0	A2 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED2 (see below)
3-2	R/W	0	A1 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED1 (see below)
1-0	R/W	0	A0 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED0 (see below)

LVDS_BIST_MUX1 0x14ea

Bit(s)	R/W	Default	Description
15-8	R/W	0	unused
7-6	R/W	0	CLKB BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED3 (see below)
5-4	R/W	0	CLKA BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED2 (see below)
3-2	R/W	0	B4 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED0 (see below)
1-0	R/W	0	B3 BIST MUX 0 = pre-select random LFSR selection 1 = LFSR[8:1] 2 = LVDS_BIST_FIXED3 (see below)

LVDS_BIST_FIXED0 0x14eb

Bit(s)	R/W	Default	Description
15-8	R/W	0	LVDS_BIST_FIXED1
7-0	R/W	0	LVDS_BIST_FIXED0

LVDS_BIST_FIXED1 0x14ec

Bit(s)	R/W	Default	Description
15-8	R/W	0	LVDS_BIST_FIXED3
7-0	R/W	0	LVDS_BIST_FIXED2

LVDS_BIST_CNTL0 0x14ed

Bit(s)	R/W	Default	Description
15-7	R	0	unused
6	R/W	0	LVDS_BIST_DUAL_PIXEL
5-1	R/W	0	LVDS_BIST_TAP_SEL: This selects the LFSR polynomial
0	R/W	0	BIST_EN

LVDS_CLKB_CLKA 0x14ee

Bit(s)	R/W	Default	Description
15	R/W	0	0
14-8	R/W	0x63	CLKB LVDS value shifted out serially
7	R/W	0	0
6-0	R/W	0x63	CLKA LVDS value shifted out serially

LVDS_PHY_CLK_CNTL 0x14ef

Bit(s)	R/W	Default	Description
15	R/W	0	LVDS_DIV_RESET_N
14	R/W	0	LVDS_DIV_SOFT_RESET
13-0	R/W	0	unused

LVDS_SER_EN 0x14f0

Bit(s)	R/W	Default	Description
15-0	R/W	0	unusedn

LVDS_PHY_CNTL6 0x14f1

Bit(s)	R/W	Default	Description
15-0	R/W	0	unused

LVDS_PHY_CNTL7 0x14f2

Bit(s)	R/W	Default	Description
15-0	R/W	0	Unused

LVDS_PHY_CNTL8 0x14f3

Bit(s)	R/W	Default	Description
15-0	R/W	0	unused

MLVDS_CLK_CTL_HI 0x14f4

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shi

MLVDS_CLK_CTL_LO 0x14f5

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shi

MLVDS_DUAL_GATE_WR_START 0x14f6

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shi

MLVDS_DUAL_GATE_WR_END 0x14f7

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shi

MLVDS_DUAL_GATE_RD_START 0x14f8

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shi

MLVDS_DUAL_GATE_RD_END 0x14f9

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shi

MLVDS_SECOND_RESET_CTL 0x14fa

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shi

MLVDS_GATE_CTL_HI 0x14fb

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shi, mlvds_dual_gate_ctl[31:16]

MLVDS_GATE_CTL_LO 0x14fc

Bit(s)	R/W	Default	Description
15-0	R/W	0	Ask Chen Shii, mlvds_dual_gate_ctl[15:0]

Video Encoder Registers

ENCI_VIDEO_MODE 0x1b00

Bit(s)	Field Name	R/W	Default	Description
7	ENCI_VIDEO_MODE_PAL_LN309_AVON	R/W	0	Fix the bug pal video is not on some fields of ln309
6	ENCI_VIDEO_MODE_SQPX	R/W	0	Square pixel mode
5-4	ENCI_VIDEO_MODE_FSCSEL	R/W	0	0: Fc=3.5795M, 1:Fsc=4.4336M, 2: Fsc=3.5756M, 3:Fsc=3.582M.
3	ENCI_VIDEO_MODE_PED	R/W	0	0: No pedestal, 1: Pedestal enable
2	ENCI_VIDEO_MODE_PDRST	R/W	0	0: Phase reset every field, 1: Phase not reset
1	ENCI_VIDEO_MODE_PHALT	R/W	0	0: Phase alternate disable, 1: Phase alternate enable
0	ENCI_VIDEO_MODE_LNFMT	R/W	0	0: 525 lines, 1:625 lines

ENCI_VIDEO_MODE_ADV 0x1b01

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_VIDEO_MODE_EN_CSYNC_MACV	R/W	0	Enable macrovision signal on CSYNC
14	CFG_LUMA_FOR_CVBS_HIGH	R/W	0	Luma for CVBS high bandwidth
13	CFG_CHROMA_MOD_HIGH	R/W	0	Chroma modulation high bandwidth
12	CFG_LUMA_FOR_RGB_HIGH	R/W	0	Using high bandwidth luma for RGB
11-10	ENCI_VIDEO_MODE_ADV_HY_SYLPF_SEL	R/W	0	Low pass filter selection on sync of high bandwidth Luma signal. 0=Bypass LPF; 1=Use 3-tap LPF; 2=Use 5-tap LPF.
9 -8	ENCI_VIDEO_MODE_ADV_CMPT_BURST_WIN_SEL	R/W	0	
7 -6	ENCI_VIDEO_MODE_ADV_CBW	R/W	0	Chroma Filter bandwidth, 0:Low, 1:Medium, 2:Higher
5 -4	ENCI_VIDEO_MODE_ADV_YBW	R/W	0	Luma Filter bandwidth , 0:Medium, 1:Low, 2:High
2	ENCI_VIDEO_MODE_ADV_VBICTL	R/W	1	0: Blank line end at line6 1: Blank line end at line17/22
1 -0	ENCI_VIDEO_MODE_ADV_DMXMD	R/W	2'b10	Video input demux shifting mode, adjust this value When input video stream is shifted.

ENCI_VIDEO_FSC_ADJ 0x1b02

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VIDEO_FSC_ADJ	R/W	16'd0	FSC adjust , 16 bit value that can adjust FSC frequency (Add with setting value)

ENCI_VIDEO_BRIGHT 0x1b03

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_VIDEO_BRIGHT	R/W	8'd0	Brightness

ENCI_VIDEO_CONT 0x1b04

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_VIDEO_CONT	R/W	8'd0	Contrast

ENCI_VIDEO_SAT 0x1b05

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_VIDEO_SAT	R/W	8'd0	Saturation

ENCI_VIDEO_HUE 0x1b06

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_VIDEO_HUE	R/W	8'd0	Hue

ENCI_VIDEO_SCH 0x1b07

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_VIDEO_SCH	R/W	8'd0	Sch adjust, adjust the phase of the FSC

ENCI_SYNC_MODE 0x1b08

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_SYNC_MODE	R/W	8'd7	Video input Synchronization mode Define Field sync/Vertical Sync/Horizontal Sync source, 0: FFF All from fsi (Not used in T25) 1: FVH From FSI, VSI, HSI respectively 2: FVV From FSI, VSI, VSI respectively 3: 0VV No FSI, Vsync/Hsync from VSI, HSI respectively 4: FVH_EAV From CCIR601 stream directly 5: FFF_EAV From CCIR601 stream, but use Field sync only 6: FMVH field rst when vs is near around line start. 7: MASTER Master mode, free run, send HSO/VSO out

Notes: Suggest use Master mode only

ENCI_SYNC_HSO_BEGIN 0x1b09

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCI_SYNC_HSO_BEGIN	R/W	11'd3	HSO begin position

ENCI_SYNC_HSO_END 0x1b0a

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCI_SYNC_HSO_END	R/W	11'd5	HSO end postion

ENCI_SYNC_VSO_EVNLN 0x1b0b

Bit(s)	Field Name	R/W	Default	Description
15 -8	ENCI_SYNC_VSO_EVN_STRTLN	R/W	8	VSO output start line in even field
7 -0	ENCI_SYNC_VSO_EVN_ENDLN	R/W	8	VSO output end line in even field

ENCI_SYNC_VSO_ODDLN 0x1b0e

Bit(s)	Field Name	R/W	Default	Description
15 -8	ENCI_SYNC_VSO_ODD_STRTLN	R/W	9	VSO output start line in odd field

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_SYNC_VSO_ODD_ENDLN	R/W	9	VSO output end line in odd field

ENCI_SYNC_CTRL 0x1b0f

Bit(s)	Field Name	R/W	Default	Description
8	ENCI_SYNC_DE_V	R/W	0	
7	ENCI_SYNC_VSO_INACTIVE_MODE	R/W	0	
6	ENCI_SYNC_CTRL_VSOMD	R/W	0	VSO position in odd field, 0:Half line after VSO in Even field, 1:Same as Even Field
5	ENCI_SYNC_CTRL_FSOP	R/W	0	FSO polarity
4	ENCI_SYNC_CTRL_VSOP	R/W	0	VSO polarity
3	ENCI_SYNC_CTRL_HSOP	R/W	0	HSO polarity
2	ENCI_SYNC_CTRL_FSIP	R/W	1	FSI polarity
1	ENCI_SYNC_CTRL_VSIP	R/W	0	VSI polarity
0	ENCI_SYNC_CTRL_HSIP	R/W	0	HSI polarity

ENCI_SYNC_HOFFST 0x1b10

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCI_SYNC_HOFFST	R/W	2	Horizontal offset after HSI in slave mode

ENCI_SYNC_VOFFST 0x1b11

Bit(s)	Field Name	R/W	Default	Description
8 -0	ENCI_SYNC_VOFFST	R/W	0	Horizontal offset aftet VSI in slave mode

ENCI_SYNC_ADJ 0x1b12

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_SYNC_ADJ_EN	R/W	0	Analog Synchronization and color burst value adjust enable
14 -10	ENCI_SYNC_ADJ_BU_V	R/W	0	Analog V burst adjustment, Signed value
9 -5	ENCI_SYNC_ADJ_BU_U	R/W	0	Analog U burst adjustment, Signed value
4 -0	ENCI_SYNC_ADJ_SYNC	R/W	0	Analog sync adjustment, Signed value

ENCI_RGB_SETTING 0x1b13

Bit(s)	Field Name	R/W	Default	Description
12 -3	RESERVED	R/W	0	Resevered
2 -0	ENCI_RGB_SYNC	R/W	0	Analog RGB sync disable (1:Enable Sync, 0:Disable) , bit 2 for Blue, bit 1 for Green. Bit 0 for Red

ENCI_CMPN_MATRIX_CB 0x1b14

Bit(s)	Field Name	R/W	Default	Description
15:8	ENCP_VIDEO_MATRIX_MA	R/W	0	CbCr matrix parameter Ma (signed value)
7:0	ENCP_VIDEO_MATRIX_MB	R/W	0	CbCr matrix parameter Mb (signed value)

Note: These 2 register is for HUE adjustment. The formula is : Cb' = Cb*Ma + Cr*Mb, Cr' = Cb*Mc + Cr*Md (effective only when Enable HUE matrix by bit ENCI_VIDEO_MODE_ADV[11])

ENCI_CMPN_MATRIX_CR 0x1b15

Bit(s)	Field Name	R/W	Default	Description
15:8	ENCP_VIDEO_MATRIX_MC	R/W	0	CbCr matrix parameter Mc (signed value)
7:0	ENCP_VIDEO_MATRIX_MD	R/W	0	CbCr matrix parameter Md (signed value)

Note: See above.

ENCI_VBI_SETTING 0x1b20

Bit(s)	Field Name	R/W	Default	Description
13	ENCI_VBI_SETTING_CCCSTM	R/W	0	Close caption phase adjustment (Value is from TTXDT0)

Bit(s)	Field Name	R/W	Default	Description
12	ENCI_VBI_SETTING_TTX_ODD_EN	R/W	0	Teletext odd field enable
11	ENCI_VBI_SETTING_TTX_EVN_EN	R/W	0	Teletext even field enable
10 -8	ENCI_VBI_SETTING_TTX_FREQ	R/W	0	Teletext frequency selection
5	ENCI_VBI_SETTING_CGMS_ODD_EN	R/W	0	CGMS odd field enable
4	ENCI_VBI_SETTING_CGMS_EVN_EN	R/W	0	CGMS even field enable
3	ENCI_VBI_SETTING_WSS_ODD_EN	R/W	0	WSS odd field enable
2	ENCI_VBI_SETTING_WSS_EVN_EN	R/W	0	WSS Even Field enable
1	ENCI_VBI_SETTING_CC_ODD_EN	R/W	0	Close Caption Odd Field enable
0	ENCI_VBI_SETTING_CC_EVN_EN	R/W	0	Close Caption Even Field enable

ENCI_VBI_CCDT_EVN 0x1b21

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_CCDT_EVN	R/W	0	Close caption even field data

ENCI_VBI_CCDT_ODD 0x1b22

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_CCDT_ODD	R/W	0	Close caption even odd data

ENCI_VBI_CC525_LN 0x1b23

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_CC525_LN	R/W	16'h1211	Close caption line in 525 format

ENCI_VBI_CC625_LN 0x1b24

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_CC625_LN	R/W	16'h1615	Close caption line in 625 format

ENCI_VBI_WSSDT 0x1b25

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_WSSDT	R/W	16'h0	WSS data

ENCI_VBI_WSS_LN 0x1b26

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_WSS_LN	R/W	16'd22	WSS line

ENCI_VBI_CGMSDT_L 0x1b27

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_CGMSDT_L	R/W	16'h0	CGMS data low 16 Bits

ENCI_VBI_CGMSDT_H 0x1b28

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_VBI_CGMSDT_H	R/W	8'h0	CGMS data high 8 Bits

ENCI_VBI_CGMS_LN 0x1b29

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_CGMS_LN	R/W	16'h1110	CGMS line

ENCI_VBI_TTX_HTIME 0x1b2a

Bit(s)	Field Name	R/W	Default	Description
15 -10	ENCI_VBI_TTX_HTIME_TOTAL_BYTES	R/W	6'h2d	Teletext total bytes
9 -0	ENCI_VBI_TTX_HTIME_STRT_POS	R/W	11'h135	Teletext start postion

ENCI_VBI_TTX_LN 0x1b2b

Bit(s)	Field Name	R/W	Default	Description
15 -9	ENCI_VBI_TTX_STRT_LN	R/W	16'h1415	Teletext Start line
8 -0	ENCI_VBI_TTX_END_LN	R/W	16'h1415	Teletext End Line

ENCI_VBI_TTXDT0 0x1b2c

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_TTXDT0	R/W	16'h0	Teletext data0

ENCI_VBI_TTXDT1 0x1b2d

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_TTXDT1	R/W	16'h0	Teletext data1

ENCI_VBI_TTXDT2 0x1b2e

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_TTXDT2	R/W	16'h0	Teletext data2

ENCI_VBI_TTXDT3 0x1b2f

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_VBI_TTXDT3	R/W	16'h0	Teletext data3

ENCI_MACV_N0 0x1b30

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_MACV_N0	R/W	8'h00	Macrovision register N0

ENCI_MACV_N1 0x1b31

Bit(s)	Field Name	R/W	Default	Description
5 -0	ENCI_MACV_N1	R/W	6'h17	Macrovision register N1

ENCI_MACV_N2 0x1b32

Bit(s)	Field Name	R/W	Default	Description
5 -0	ENCI_MACV_N2	R/W	6'h15	Macrovision register N2

ENCI_MACV_N3 0x1b33

Bit(s)	Field Name	R/W	Default	Description
5 -0	ENCI_MACV_N3	R/W	6'h21	Macrovision register N3

ENCI_MACV_N4 0x1b34

Bit(s)	Field Name	R/W	Default	Description
5 -0	ENCI_MACV_N4	R/W	6'h15	Macrovision register N4

ENCI_MACV_N5 0x1b35

Bit(s)	Field Name	R/W	Default	Description
2 -0	ENCI_MACV_N5	R/W	3'h5	Macrovision register N5

ENCI_MACV_N6 0x1b36

Bit(s)	Field Name	R/W	Default	Description
2 -0	ENCI_MACV_N6	R/W	3'h5	Macrovision register N6

ENCI_MACV_N7 0x1b37

Bit(s)	Field Name	R/W	Default	Description
1 -0	ENCI_MACV_N7	R/W	2'h2	Macrovision register N7

ENCI_MACV_N8 0x1b38

Bit(s)	Field Name	R/W	Default	Description
5 -0	ENCI_MACV_N8	R/W	6'h1b	Macrovision register N8

ENCI_MACV_N9 0x1b39

Bit(s)	Field Name	R/W	Default	Description
5 -0	ENCI_MACV_N9	R/W	6'h1b	Macrovision register N9

ENCI_MACV_N10 0x1b3a

Bit(s)	Field Name	R/W	Default	Description
5 -0	ENCI_MACV_N10	R/W	6'h24	Macrovision register N10

ENCI_MACV_N11 0x1b3b

Bit(s)	Field Name	R/W	Default	Description
14 -0	ENCI_MACV_N11	R/W	15'h07f8	Macrovision register N11

ENCI_MACV_N12 0x1b3c

Bit(s)	Field Name	R/W	Default	Description
14 -0	ENCI_MACV_N12	R/W	15'h0	Macrovision register N12

ENCI_MACV_N13 0x1b3d

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_MACV_N13	R/W	8'h0f	Macrovision register N13

ENCI_MACV_N14 0x1b3e

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_MACV_N14	R/W	8'h0f	Macrovision register N14

ENCI_MACV_N15 0x1b3f

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCI_MACV_N15	R/W	8'h60	Macrovision register N15

ENCI_MACV_N16 0x1b40

Bit(s)	Field Name	R/W	Default	Description
0 -0	ENCI_MACV_N16	R/W	1'h1	Macrovision register N16

ENCI_MACV_N17 0x1b41

Bit(s)	Field Name	R/W	Default	Description
3 -0	ENCI_MACV_N17	R/W	4'ha	Macrovision register N17

ENCI_MACV_N18 0x1b42

Bit(s)	Field Name	R/W	Default	Description
3 -0	ENCI_MACV_N18	R/W	4'h0	Macrovision register N18

ENCI_MACV_N19 0x1b43

Bit(s)	Field Name	R/W	Default	Description
3 -0	ENCI_MACV_N19	R/W	4'h5	Macrovision register N19

ENCI_MACV_N20 0x1b44

Bit(s)	Field Name	R/W	Default	Description
2 -0	ENCI_MACV_N20	R/W	3'h4	Macrovision register N20

ENCI_MACV_N21 0x1b45

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCI_MACV_N21	R/W	10'h3ff	Macrovision register N21

ENCI_MACV_N22 0x1b46

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCI_MACV_N22	R/W	16'h0	Macrovision register N22

ENCI_DBG_PX_RST 0x1b48

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_DBG_PX_RST_EN	R/W	1	1:Reset enable (Interlaced TV encoder is disabled), 0:Normal
10 -0	ENCI_DBG_PX_RST_VAL	R/W	0	Pixel value after reset

ENCI_DBG_FLDLN_RST 0x1b49

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_DBG_LN_RST_EN	R/W	0	Line reset enable
14	ENCI_DBG_FLD_RST_EN	R/W	0	Field reset enable
11 -9	ENCI_DBG_FLD_RST_VAL	R/W	0	Field reset value
8 -0	ENCI_DBG_LN_RST_VAL	R/W	0	Line reset value

ENCI_DBG_PX_INT 0x1b4a

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_DBG_PX_INT_EN	R/W	0	Pixel Interrupt enable
10 -0	ENCI_DBG_PX_INT_VAL	R/W	0	Pixel value that trig the interrupt

ENCI_DBG_FLDLN_INT 0x1b4b

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_DBG_FLD_INT_EN	R/W	0	Field interrupt enable
11	ENCI_DBG_LN_INT_EN	R/W	0	Line interrupt enable
14 -12	ENCI_DBG_FLD_INT_VAL	R/W	0	Field value that trig the interrupt
8 -0	ENCI_DBG_LN_INT_VAL	R/W	0	Line value that trig the interrupt

ENCI_DBG_MAXPX 0x1b4c

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_DBG_MAXPX_EN	R/W	0	Debug mode, change the max pixel.
10 -0	ENCI_DBG_MAXPX_CHGVAL	R/W	0	The value of max pixel

ENCI_DBG_MAXLN 0x1b4d

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_DBG_MAXLN_EN	R/W	0	Debug mode, change the max line counter
8 -0	ENCI_DBG_MAXLN_CHGVAL	R/W	0	The value want to change

ENCI_MACV_MAX_AMP 0x1b50

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_MACV_MAX_AMP_EN	R/W	0	Macrovision max amplitude change enable
10 -0	ENCI_MACV_MAX_AMP_VAL	R/W	0	The value want to change

ENCI_MACV_PULSE_LO 0x1b51

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_MACV_PULSE_LO_EN	R/W	0	Macrovision low pulse change enable.
10 -0	ENCI_MACV_PULSE_LO_VAL	R/W	0	The value want to change

ENCI_MACV_PULSE_HI 0x1b52

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_MACV_PULSE_HI_EN	R/W	0	Macrovision high pulse change enable.
10 -0	ENCI_MACV_PULSE_HI_VAL	R/W	0	The value want to change

ENCI_MACV_BKP_MAX 0x1b53

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_MACV_BKP_MAX_EN	R/W	0	Macrovision back porch max value change enable.
9 -0	ENCI_MACV_BKP_MAX_VAL	R/W	0	The value want to change

ENCI_CFILT_CTRL 0x1b54

Bit(s)	Field Name	R/W	Default	Description
12	ENCI_CFILT_CMPT_SMOOTH_FLT	R/W	1	Component Cb/Cr smooth filter
11-10	ENCI_CFILT_CMPT_SEL	R/W	0	Filter component bandwith Cb/Cr sel 0: High, 1: Medium 2: Low
1	ENCI_CFILT_CMPT_SEL	R/W	1	Filter component CbCr bandwith sel (1:high, 0:low)
0	ENCI_CFILT_CVBS_SEL	R/W	0	Filter CVBS CbCr bandwith sel (1:high, 0:low)

ENCI_CFILT7 0x1b55

Bit(s)	Field Name	R/W	Default	Description
14-0	ENCI_CFILT7	R/W	15'h4d53	Filter7 parameters

ENCI_YC_DELAY 0x1b56

Bit(s)	Field Name	R/W	Default	Description
9-8	ENCI_COMPY_DELAY	R/W	0	Component Y delay
7-4	ENCI_Y_DELAY	R/W	4'h2	Interlace Y delay
3-0	ENCI_C_DELAY	R/W	4'h0	Interlace C delay

ENCI_VIDEO_EN 0x1b57

Bit(s)	Field Name	R/W	Default	Description
0	ENCI_VIDEO_EN	R/W	0	Interlace video enable

ENCP_VFIFO2VD_CTL 0x1b58

Bit(s)	Field Name	R/W	Default	Description
15-8	VFIFO2VD_VD_SEL	R/W	0	vfifo2vd_vd_sel
7	VFIFO2VD_DROP	R/W	0	vfifo2vd_drop
6-1	VFIFO2VD_DELAY	R/W	0	vfifo2vd_delay
0	VFIFO2VD_EN	R/W	0	vfifo2vd_en

ENCP_VFIFO2VD_PIXEL_START 0x1b59

Bit(s)	Field Name	R/W	Default	Description
12-0	VFIFO2VD_PIXEL_START	R/W	0	Pixel start

ENCP_VFIFO2VD_PIXEL_END 0x1b5a

Bit(s)	Field Name	R/W	Default	Description
15	VFIFO2VD_YC_USE_FIRST_VFIFO_REQ	R/W	0	0=Keep as previous version; 1=On the very first pixel since VFIFO is enabled, YC pipeline values take from default setting, rather than from values stored in the pipeline.
12-0	VFIFO2VD_PIXEL_END	R/W	0	Pixel end

ENCP_VFIFO2VD_LINE_TOP_START 0x1b5b

Bit(s)	Field Name	R/W	Default	Description
10-0	VFIFO2VD_LINE_TOP_START	R/W	0	Top field line end

ENCP_VFIFO2VD_LINE_TOP_END 0x1b5c

Bit(s)	Field Name	R/W	Default	Description
10-0	VFIFO2VD_LINE_TOP_END	R/W	0	Top field line end

ENCP_VFIFO2VD_LINE_BOT_START 0x1b5d

Bit(s)	Field Name	R/W	Default	Description
10-0	VFIFO2VD_LINE_BOT_START	R/W	0	Bottom field line end

ENCP_VFIFO2VD_LINE_BOT_END 0x1b5e

Bit(s)	Field Name	R/W	Default	Description
10-0	VFIFO2VD_LINE_BOT_END	R/W	0	Bottom field line end

VENC_SYNC_ROUTE 0x1b60

Bit(s)	Field Name	R/W	Default	Description
2	VENC_SYNC_ROUTE	R/W	0	Internal Vencoder hsync/vsync source (0-VIU, 1-External Venc)
1	VIU_SYNC_ROUTE	R/W	0	VIU hsync/vsync input source (0-Venc, 1-External Venc)
0	VPINS_SYNC_ROUTE	R/W	1	External Vencoder hsync/vsync source (0-Internal Venc, 1-VIU)

VENC_VIDEO_EXSRC 0x1b61

Bit(s)	Field Name	R/W	Default	Description
0	VENC_VIDEO_EXSRC	R/W	1	External Video Source enable, get video data from external pins.

Notes: This is not supported by T25, clear this when init.

VENC_DVI_SETTING 0x1b62

Bit(s)	Field Name	R/W	Default	Description
15	VENC_DVI_SEL_DVI	R/W	0	1=use programmable vs/hs/de whose only connection is to DVI/HDMI.
14	VENC_DVI_SEL_INTL_DE	R/W	0	For interlace mode only. 1=use intl_de for DE.
13	VENC_DVI_GAMMA_EN	R/W	0	0=Send to DVI/HDMI interface with data NOT from Gamma table. 1=Send to DVI/HDMI interface with data from Gamma table.
12	VENC_DVI_DDR_DESEL	R/W	0	For external DVI device only.
11	VENC_DVI_DDR_CKSEL	R/W	0	For external DVI device only.
10	VENC_DVI_DDR_CKPHI	R/W	0	For external DVI device only.
9	VENC_DVI_DDR_SEL	R/W	0	For external DVI device only.
8	VENC_DVI_INV_CLK	R/W	0	Invert DVI clock
7	VENC_DVI_SEL_INTERNAL_HDMI	R/W	0	0=Select the external DVI device which is compatible to chips predate M1 1=Select the internal HDMI tx which is in chips starting from meson.
~~5~~6:4	VENC_DVI_CLK_SEL	R/W	0	DVI Clock selection: 0: clk27 1: clk54 2: ½ of ENCP pixel_clk 3: clk108 4: ½ of ENCI pixel_clk 5: cts_vclk1 6-7: Reserved (Note : here the clk27/54/108 is signal Name, not the real frequency)
3	VENC_DVI_INV_VSYNC	R/W	0	1=Invert DVI/HDMI Vsync output polarity
2	VENC_DVI_INV_HSYNC	R/W	0	1=Invert DVI/HDMI Hsync output polarity
1	SYNC_SEL_OUT_SYNC	R/W	0	DVI/601 sync use output sync (not viu sync)
0	VENC_DVI_SRC_SEL	R/W	1	DVI source select (0: interlace, 1:progressive)

VENC_C656_CTRL 0x1b63

Bit(s)	Field Name	R/W	Default	Description
3	VENC_C656_CLKP	R/W	0	Clock out Polarity
2	VENC_C656_FLDP	R/W	0	Field Polarity
1	VENC_C656_VSOP	R/W	0	Vsyn Polarity
0	VENC_C656_HSOP	R/W	0	Hsyn Polarity

Upsamping is only used for 480i/576i, 480p/576p, not for 720p/1080i/1080p mode,
For 480i/576i upsampling, video signal is upsampled from 27Mhz to 108Mhz,

For 480p/576p upsampling, video signal is upsampled from 54Mz to 108Mhz
set VENC_UPSAMPLE_CTRL0 = 0x9061
set VENC_UPSAMPLE_CTRL1 = 0xa061
set VENC_UPSAMPLE_CTRL2 = 0x1b061

VENC_UPSAMPLE_CTRL0 0x1b64

Bit(s)	Field Name	R/W	Default	Description
15-12	UPSAMPLE_SEL	R/W	0	Upsample0 din selection 0: Interlace High bandwidth Luma 1: CVBS 2: S-Video luma 3: S-Video Chroma 4: Interlace Pb 5: Interlace Pr 6: Interlace R 7: Interlace G 8: Interlace B 9: Progressive Y a: Progressive Pb b: Progressive Pr c: Progressive R d: Progressive G e: Progressive B f: VDAC test value (VENC_VDAC_TST_VAL)
11-9	UNUSED	R	0	Unused
8	BYPASS	R/W	0	If true, bypass
7	F1_DIV_INV	R/W	0	If true, invert div
6	F1_UPSAMPLE_EN	R/W	0	Filter1 upsample enable
5	F1_EN	R/W	0	Filter1 filtering enable
4	F1_CLK_RATIO	R/W	0	If true, Filter1 clk ratio is 2, input data sample every 2 clocks, otherwise 1
3	F0_DIV_INV	R/W	0	If true, invert div
2	F0_UPSAMPLE_EN	R/W	0	Filter0 upsample enable
1	F0_EN	R/W	0	Filter0 filtering enable
0	F0_CLK_RATIO	R/W	0	If true, Filter0 clk ratio is 2, input data sample every 2 clocks, otherwise 1

VENC_UPSAMPLE_CTRL1 0x1b65

Bit(s)	Field Name	R/W	Default	Description
15-12	UPSAMPLE_SEL	R/W	0	Upsample1 din selection 0: Interlace High bandwidth Luma 1: CVBS 2: S-Video luma 3: S-Video Chroma 4: Interlace Pb 5: Interlace Pr 6: Interlace R 7: Interlace G 8: Interlace B

Bit(s)	Field Name	R/W	Default	Description
				9: Progressive Y a: Progressive Pb b: Progressive Pr c: Progressive R d: Progressive G e: Progressive B f: VDAC test value (VENC_VDAC_TST_VAL)
11-9	UNUSED	R	0	Unused
8	BYPASS	R/W	0	If true, bypass
7	F1_DIV_INV	R/W	0	If true, invert div
6	F1_UPSAMPLE_EN	R/W	0	Filter1 upsample enable
5	F1_EN	R/W	0	Filter1 filtering enable
4	F1_CLK_RATIO	R/W	0	If true, Filter1 clk ratio is 2, input data sample every 2 clocks, otherwise 1
3	F0_DIV_INV	R/W	0	If true, invert div
2	F0_UPSAMPLE_EN	R/W	0	Filter0 upsample enable
1	F0_EN	R/W	0	Filter0 filtering enable
0	F0_CLK_RATIO	R/W	0	If true, Filter0 clk ratio is 2, input data sample every 2 clocks, otherwise 1

VENC_UPSAMPLE_CTRL2 0x1b66

Bit(s)	Field Name	R/W	Default	Description
15-12	UPSAMPLE_SEL	R/W	0	Upsample2 din selection 0: Interlace High bandwidth Luma 1: CVBS 2: S-Video luma 3: S-Video Chroma 4: Interlace Pb 5: Interlace Pr 6: Interlace R 7: Interlace G 8: Interlace B 9: Progressive Y a: Progressive Pb b: Progressive Pr c: Progressive R d: Progressive G e: Progressive B f: VDAC test value (VENC_VDAC_TST_VAL)
11-9	UNUSED	R	0	Unused
8	BYPASS	R/W	0	If true, bypass
7	F1_DIV_INV	R/W	0	If true, invert div
6	F1_UPSAMPLE_EN	R/W	0	Filter1 upsample enable
5	F1_EN	R/W	0	Filter1 filtering enable
4	F1_CLK_RATIO	R/W	0	If true, Filter1 clk ratio is 2, input data sample every 2 clocks, otherwise 1
3	F0_DIV_INV	R/W	0	If true, invert div
2	F0_UPSAMPLE_EN	R/W	0	Filter0 upsample enable
1	F0_EN	R/W	0	Filter0 filtering enable
0	F0_CLK_RATIO	R/W	0	If true, Filter0 clk ratio is 2, input data sample every 2 clocks, otherwise 1

TCON_INVERT_CTL 0x1b67

Bit(s)	Field Name	R/W	Default	Description
15		R/W	1'b0	vsync invert
14		R/W	1'b0	hsync invert
13		R/W	1'b0	Oev3 invert

Bit(s)	Field Name	R/W	Default	Description
12		R/W	1'b0	Oev2 invert
11		R/W	1'b0	Cpv2 invert
10		R/W	1'b0	Cph3 invert
9		R/W	1'b0	Cph2 invert
8		R/W	1'b0	Cph1 invert
7		R/W	1'b0	oeh invert
6		R/W	1'b0	vcom invert
5		R/W	1'b0	Stv2 invert
4		R/W	1'b0	Stv1 invert
3		R/W	1'b0	Cpv1 invert
2		R/W	1'b0	Oev1 invert
1		R/W	1'b0	Sth1 invert
0		R/W	1'b0	Sth2 invert

VENC_VIDEO_PROG_MODE 0x1b68

Bit(s)	Field Name	R/W	Default	Description
9	VENC_DAC_CLK_SEL_CLK108	R/W	1'b0	Select clk108 as DAC clock
8	VENC_BIST_FIELD_SEL	R/W	1'b0	Venc bist and venc_field output selection. 0:Interlace, 1:Progressive.
7	VENC_VIU_VSIN_SEL	R/W	1'b0	VIU Vsync input select, 0:Progressive, 1:Interlace
6	VENC_VIU_HSIN_SEL	R/W	1'b0	VIU Hsync input select, 0:Progressive, 1:Interlace
5	VENC_VPIN_VSIN_SEL	R/W	1'b0	Pin Vsync input select, 0:Progressive, 1:Interlace
4	VENC_VPIN_HSIN_SEL	R/W	1'b0	Pin Hsync input select, 0:Progressive, 1:Interlace
3	VENC_DAC1_CLK_SEL	R/W	1'b0	DAC1 clock select, 0:clk54, 1:clk27
2	VENC_DAC0_CLK_SEL	R/W	1'b0	DAC0 clock select, 0:clk54, 1:clk27

VENC_ENCI_LINE 0x1b69

Bit(s)	Field Name	R/W	Default	Description
9 -0	VENC_ENCI_LINE	R	-	Current interlace encoder line

VENC_ENCI_PIXEL 0x1b6a

Bit(s)	Field Name	R/W	Default	Description
9 -0	VENC_ENCI_LINE	R	-	Current interlace encoder line

VENC_ENCP_LINE 0x1b6b

Bit(s)	Field Name	R/W	Default	Description
9 -0	VENC_ENCP_LINE	R	-	Current interlace encoder line

VENC_ENCP_PIXEL 0x1b6c

Bit(s)	Field Name	R/W	Default	Description
9 -0	VENC_ENCP_LINE	R	-	Current interlace encoder line

VENC_STATA 0x1b6d

Bit(s)	Field Name	R/W	Default	Description
2 -0	VENC_FILED	R	-	Current Venc Field

VENC_INTCTRL 0x1b6e

Bit(s)	Field Name	R/W	Default	Description
13	ENCP_TIMER_INT_EN	R/W	0	
12	ENCP_FLDINT_EN	R/W	0	
11	ENCP_PXRST_EN	R/W	0	
10	ENCP_TIMER_INT_EN	R/W	0	
9	ENCP_LNRST_INT_EN	R /W	0	Progressive encoder filed change interrupt enable
8	ENCP_PXRST_INT_EN	R /W	0	Progressive encoder line change interrupt enable
7	ENCL_TIMER_INT_EN	R/W	0	

Bit(s)	Field Name	R/W	Default	Description
6	ENCL_FLDINT_EN	R/W	0	
5	ENCL_PXRST_EN	R/W	0	
4	ENCI_TIMER_INT_EN	R/W	0	
3	ENCI_TTXLOAD_INT_EN	R /W	0	Interlace encoder teletext data interrupt enable
2	ENCI_FDRST_INT_EN	R /W	0	Interlace encoder field reset interrupt enable
1	ENCI_LNRST_INT_EN	R /W	0	Interlace encoder filed change interrupt enable
0	ENCI_PXRST_INT_EN	R /W	0	Interlace encoder line change interrupt enable

VENC_INTFLAG 0x1b6f

Bit(s)	Field Name	R/W	Default	Description
9	ENCP_LNRST_INT_F	R /W	0	Progressive encoder filed change interrupt flag
8	ENCP_PXRST_INT_F	R /W	0	Progressive encoder line change interrupt flag
3	ENCI_TTXLOAD_INT_F	R /W	0	Interlace encoder teletext data load interrupt flag
2	ENCI_FDRST_INT_F	R /W	0	Interlace encoder field reset interrupt flag
1	ENCI_LNRST_INT_F	R /W	0	Interlace encoder filed change interrupt flag
0	ENCI_PXRST_INT_F	R /W	0	Interlace encoder line change interrupt flag

VENC_VIDEO_TST_EN 0x1b70

Bit(s)	Field Name	R/W	Default	Description
0	VENC_VIDEO_TST_EN	R/W	0	BIST enable

VENC_VIDEO_TST_MDSEL 0x1b71

Bit(s)	Field Name	R/W	Default	Description
7-0	VENC_VIDEO_TST_MDSEL	R/W	8'h01	BIST Mode 0: TST_MODE_FIXVAL---- Fix Value on Y/Cb/Cr 1: TST_MODE_COLORBAR ---- 100/75 color bar 2: TST_MODE_THINLINE ---- Thin horizonl/vertical lines on screen 3: TST_MODE_DOTGRID ---- Dot grid on screen

Notes: In none color bar mode, value is from register TST_Y/TST_CB/TST_CR.

VENC_VIDEO_TST_Y 0x1b72

Bit(s)	Field Name	R/W	Default	Description
9 -0	VENC_VIDEO_TST_Y	R/W	10'd512	BIST fix value Y

Notes: Value is 10 bists,X4 if convert from 8 Bits CCIR601 value

VENC_VIDEO_TST_CB 0x1b73

Bit(s)	Field Name	R/W	Default	Description
9 -0	VENC_VIDEO_TST_CB	R/W	10'd512	BIST fix value Cb

Notes: Value is 10 bists,X4 if convert from 8 Bits CCIR601 value

VENC_VIDEO_TST_CR 0x1b74

Bit(s)	Field Name	R/W	Default	Description
9 -0	VENC_VIDEO_TST_CR	R/W	10'd512	BIST fix value Cr

Notes: Value is 10 bists,X4 if convert from 8 Bits CCIR601 value

VENC_VIDEO_TST_CLRBAR_STRT 0x1b75

Bit(s)	Field Name	R/W	Default	Description
12-0	VENC_VIDEO_TST_CLRBAR_STRT	R/W	11'd275	Colorbar BIST start position

Notes: VENC_VIDEO_TST_CLRBAR_STRT Interlace mode : 235, Progressive mode : 274

VENC_VIDEO_TST_CLRBAR_WIDTH 0x1b76

Bit(s)	Field Name	R/W	Default	Description
12 -0	VENC_VIDEO_TST_CLRBAR_WIDTH	R/W	11'd360	Colorbar BIST Width

Notes: VENC_VIDEO_TST_CLRBAR_WIDTH Interlace mode : 360, Progressive mode: 180

VENC_VIDEO_TST_VDCNT_STSET 0x1b77

Bit(s)	Field Name	R/W	Default	Description
1-0	VENC_VIDEO_TST_VDCNT_STSET	R/W	0	BIST video data shifting setting, adjust this value if the data sequence generated by BIST is incorrect.

VENC_VDAC_DACSEL0 0x1b78

Bit(s)	Field Name	R/W	Default	Description
15-12	VENC_VDAC_DLY	R/W	0	VDAC delay (0-15 clocks)
5	VENC_VDAC_SEL_ATV_DMD	R/W	0	1: select VDAC0 source from ATV demod
4-0	VENC_VDAC_DACSEL0	R/W	4'h2	Video Dac0 selection 0: Interlace Y 1: CVBS 2: S-Video luma 3: S-Video Chroma 4: Interlace Pb 5: Interlace Pr 6: Interlace R 7: Interlace G 8: Interlace B 9: Progressive Y a: Progressive Pb b: Progressive Pr c: Progressive R d: Progressive G e: Progressive B f: VDAC test value (VENC_VDAC_TST_VAL) 0x10: upsampled data0 0x11: upsampled data1 0x12 upsampled data2

VENC_VDAC_DACSEL1 0x1b79

Bit(s)	Field Name	R/W	Default	Description
			16'h4	Same as above

VENC_VDAC_DACSEL2 0x1b7a

Bit(s)	Field Name	R/W	Default	Description
			16'h5	Same as above

VENC_VDAC_DACSEL3 0x1b7b

Bit(s)	Field Name	R/W	Default	Description
			16'h1	Same as above

VENC_VDAC_DACSEL4 0x1b7c

Bit(s)	Field Name	R/W	Default	Description
			16'h2	Same as above

VENC_VDAC_DACSEL5 0x1b7d

Bit(s)	Field Name	R/W	Default	Description
			16'h3	Same as above

VENC_VDAC_SETTING 0x1b7e

Bit(s)	Field Name	R/W	Default	Description
0	VENC_VDAC0_PWDN	R/W	0	Powers down video DAC 0
1	VENC_VDAC1_PWDN	R/W	0	Powers down video DAC 1
2	VENC_VDAC2_PWDN	R/W	0	Powers down video DAC 2
3	VENC_VDAC3_PWDN	R/W	0	Powers down video DAC 3
4	VENC_VDAC4_PWDN	R/W	0	Powers down video DAC 4
5	VENC_VDAC5_PWDN	R/W	0	Powers down video DAC 5
6		R/W	0	Unused
7	VENC_VDAC_ALL_PWDN	R/W	0	Powers down all video DACs
8	VENC_VDAC_SOG	R/W	0	VDAC SOG signal (Sync on green, not used)
9	VENC_VDAC_IREN	R/W	0	VDAC IREN signal (7.5 IRE setup, not used)
12	VENC_VDAC_SYNC	R/W	0	VDAC sync signal when SYBL_en is 0
13	VENC_VDAC_BLNK	R/W	0	VDAC blank signal when SYBL_EN is 0
15	VENC_VDAC_SYBL_EN	R/W	0	Enable tv encoder to control VDAC sync and blank

VENC_VDAC_TST_VAL 0x1b7f

Bit(s)	Field Name	R/W	Default	Description
9 -0	VENC_VDAC_TST_VAL	R/W	10'h200	Video DAC test value

ENCP_VIDEO_EN 0x1b80

Bit(s)	Field Name	R/W	Default	Description
0	ENCP_VIDEO_EN	R/W	0	Progressive encoder enable

ENCP_VIDEO_SYNC_MODE 0x1b81

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_VIDEO_SYNC_MODE	R/W	8'h7	Video input Synchronization mode (4:Slave mode, 7:Master mode)

ENCP_MACV_EN 0x1b82

Bit(s)	Field Name	R/W	Default	Description
0	ENCP_MACV_EN	R/W	0	Macrovision enable

ENCP_VIDEO_Y_SCL 0x1b83

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_VIDEO_Y_SCL	R/W	8'd81	Y scale

ENCP_VIDEO_PB_SCL 0x1b84

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_VIDEO_PB_SCL	R/W	8'd79	Cb scale

ENCP_VIDEO_PR_SCL 0x1b85

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_VIDEO_PR_SCL	R/W	8'd79	Cr scale

ENCP_VIDEO_SYNC_SCL 0x1b86

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_VIDEO_SYNC_SCL	R/W	8'd128	Analog Sync value scale

ENCP_VIDEO_MACV_SCL 0x1b87

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_VIDEO_MACV_SCL	R/W	8'd128	Macrovision value scale

ENCP_VIDEO_Y_OFFST 0x1b88

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_Y_OFFST	R/W	10'h3c0	Y offset

ENCP_VIDEO_PB_OFFST 0x1b89

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_PB_OFFST	R/W	10'h0	Pb offset

ENCP_VIDEO_PR_OFFST 0x1b8a

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_PR_OFFST	R/W	10'h0	Pr offset

ENCP_VIDEO_SYNC_OFFST 0x1b8b

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_SYNC_OFFST	R/W	10'h0	Sync pulse offset

ENCP_VIDEO_MACV_OFFST 0x1b8c

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_MACV_OFFST	R/W	10'h0	Macrovision offset

ENCP_VIDEO_MODE 0x1b8d

Bit(s)	Field Name	R/W	Dfault	Description
15	ENCP_PX_LN_CNT_SHADOW_EN	R/W	0	pixel count and line count shadow enable
14	ENCP_VIDEO_MODE_DE_V	R/W	0	1=DE signal's polarity is active high. 0=DE signal's polarity is active low.
13	ENCP_VIDEO_MODE_EN_VSO_OFLD_FIX_EN	R/W	0	1=Extend ENCP_VIDEO_MAX_PXCNT by 1 pixel. 0=Treat ENCP_VIDEO_MAX_PXCNT as is.
12	ENCP_VIDEO_MODE_EN_FIELD_ODD	R/W	0	Enable odd field (for 1080i)
11	ENCP_VIDEO_MODE_EN_VSO_OFLD	R/W	0	Enable VSO odd field
10	ENCP_VIDEO _MODE_EN_VAVON_OFLD	R/W	0	Enable Vertical Active On for odd field
9	ENCP_VIDEO _MODE_EN_EQU_OFLD	R/W	0	Enable Equalization pulse for odd field
8	ENCP_VIDEO _MODE_EN_EQU	R/W	0	Enable Equalization pulse
6	ENCP_VIDEO _MODE_EN_HSEQ_SWITCH	R/W	0	Enable Hsync and equalization pulse switch in center
5	ENCP_VIDEO _MODE_EN_VP_OFLD	R/W	0	Enable Vertical Pulse for odd field
4	ENCP_VIDEO _MODE_EN_VP2	R/W	0	Enable 2nd vertical pulse in a line (1080i)
3	ENCP_VIDEO _MODE_EN_VPE_HALF_OFLD	R/W	0	Vertical pulse on end line of odd field is half
2	ENCP_VIDEO _MODE_EN_VPB_HALF_OFLD	R/W	0	Vertical pulse on begin line of odd field is half
1	ENCP_VIDEO _MODE_EN_VPE_HALF	R/W	0	Vertical pulse on end line of even field is half
0	ENCP_VIDEO _MODE_EN_VPB_HALF	R/W	0	Vertical pulse on begin line of even field is half
Note: This register should be set as 0x140 for 720p , and 0x1ffc for 1080i, and 0x0 for 480p/576p				

ENCP_VIDEO_MODE_ADV 0x1b8e

Bit(s)	Field Name	R/W	Default	Description
15-14	ENCP_SP_TIMING_CTRL	R/W	0	
13	ENCP_CR_BAPASS_LIM	R/W	0	
12	ENCP_CB_BAPASS_LIM	R/W	0	
11	ENCP_Y_BAPASS_LIM	R/W	0	
10	ENCP_SEL_GAMMA_RGB_IN	R/W	0	
9-8		R/W	0	Unused
7	ENCP_VIDEO_MODE_ADV_EN_HUE_MATRIX	R/W	0	Enable HUE matrix
6	ENCP_VIDEO_MODE_ADV_SWAP_PBPR	R/W	0	Swap PB PR
5	ENCP_VIDEO_MODE_ADV_EN_HS_PBPR	R/W	0	Enable sync pulse on PB PR
4	ENCP_VIDEO_MODE_ADV_GAIN_HDTV	R/W	0	YPBPR gain as HDTV type
3	ENCP_VIDEO_MODE_ADV_VFIFO_EN	R/W	0	Data input from VFIFO
2 :0	ENCP_VIDEO_MODE_ADV_VFIFO_UPMODE	R/W	1	Sampling rate: 0: 1 1: ½ 2: ¼

Bit(s)	Field Name	R/W	Default	Description
				3: 1/8

ENCP_DBG_PX_RST 0x1b90

Bit(s)	Field Name	R/W	Default	Description
15	ENCP_DBG_PX_RST_EN	R/W	0	Debug mode pixel reset enable
12 -0	ENCP_DBG_PX_RST_VAL	R/W	0	Debug mode pixel reset value

ENCP_DBG_LN_RST 0x1b91

Bit(s)	Field Name	R/W	Default	Description
15	ENCP_DBG_LN_RST_EN	R/W	0	Debug mode line reset enable
10 -0	ENCP_DBG_LN_RST_VAL	R/W	0	Debug mode line reset value

ENCP_DBG_PX_INT 0x1b92

Bit(s)	Field Name	R/W	Default	Description
15	ENCP_DBG_PX_INT_EN	R/W	0	Pixel Interrupt enable
12 -0	ENCP_DBG_PX_INT_VAL	R/W	0	Pixel value that trig the interrupt

ENCP_DBG_LN_INT 0x1b93

Bit(s)	Field Name	R/W	Default	Description
15	ENCP_DBG_LN_INT_EN	R/W	0	Line Interrupt enable
10 -0	ENCP_DBG_LN_INT_VAL	R/W	0	Line value that trig the interrupt

ENCP_VIDEO_YFP1_HTIME 0x1b94

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_YFP1_HTIME	R/W	240	Filter switch start point

ENCP_VIDEO_YFP2_HTIME 0x1b95

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_YFP2_HTIME	R/W	1657	Filter switch end point

ENCP_VIDEO_YC_DLY 0x1b96

Bit(s)	Field Name	R/W	Default	Description
5 –4	ENCP_VIDEO_Y_DLY	R/W	16'h0	Y delay
3 –2	ENCP_VIDEO_CB_DLY	R/W	16'h0	Cb delay
1 –0	ENCP_VIDEO_CR_DLY	R/W	16'h0	Cr delay

ENCP_VIDEO_MAX_PXCNT 0x1b97

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_MAX_PXCNT	R/W	13'd1715	Max pixel counter

ENCP_VIDEO_HSPULS_BEGIN 0x1b98

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_HSPULS_BEGIN	R/W	13'd1715	Analog Horizontal Sync Begin

ENCP_VIDEO_HSPULS_END 0x1b99

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_HSPULS_END	R/W	13'd125	Analog Horizontal Sync End

ENCP_VIDEO_HSPULS_SWITCH 0x1b9a

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_HSPULS_SWITCH	R/W	13'd88	Analog Horizontal switch point (for HDTV)

ENCP_VIDEO_VSPULS_BEGIN 0x1b9b

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_VSPULS_BEGIN	R/W	13'd0	Analog Veritcal Sync begin point

ENCP_VIDEO_VSPULS_END 0x1b9c

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_VSPULS_END	R/W	13'd1589	Analog Veritcal Sync end point

ENCP_VIDEO_VSPULS_BLINE 0x1b9d

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_VSPULS_BLINE	R/W	11'd5	Vso begin line

ENCP_VIDEO_VSPULS_ELINE 0x1b9e

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_VSPULS_ELINE	R/W	11'd10	Vso end line

ENCP_VIDEO_EQPULS_BEGIN 0x1b9f

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_EQPULS_BEGIN	R/W	13'd0	Analog Equalization pulse begin point

ENCP_VIDEO_EQPULS_END 0x1ba0

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_EQPULS_END	R/W	13'd1589	Analog Equalization pulse end point

ENCP_VIDEO_EQPULS_BLINE 0x1ba1

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_EQPULS_BLINE	R/W	11'd5	Equalization pulse begin line

ENCP_VIDEO_EQPULS_ELINE 0x1ba2

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_EQPULS_ELINE	R/W	11'd10	Equalization pulse end line

ENCP_VIDEO_HAVON_END 0x1ba3

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_HAVON_END	R/W	13'd1656	Vertical active video end point

ENCP_VIDEO_HAVON_BEGIN 0x1ba4

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_HAVON_BEGIN	R/W	13'd217	Vertical active video start point

ENCP_VIDEO_VAVON_ELINE 0x1baf

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_VAVON_ELINE	R/W	11'd519	Vertical active video on end line

ENCP_VIDEO_VAVON_BLINE 0x1ba6

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_VAVON_BLINE	R/W	11'd42	Vertical active video on start line

ENCP_VIDEO_HSO_BEGIN 0x1ba7

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_HSO_BEGIN	R/W	16	Digital Hsync out start point

ENCP_VIDEO_HSO_END 0x1ba8

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_HSO_END	R/W	32	Digital Hsync out end point

ENCP_VIDEO_VSO_BEGIN 0x1ba9

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_VSO_BEGIN	R/W	16	Digital Vsync out start point

ENCP_VIDEO_VSO_END 0x1baa

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCP_VIDEO_VSO_END	R/W	32	Digital Vsync out end point

ENCP_VIDEO_VSO_BLINE 0x1bab

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_VSO_BLINE	R/W	37	Digital Vsync out start line

ENCP_VIDEO_VSO_ELINE 0x1bac

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_VSO_ELINE	R/W	39	Digital Vsync out end line

ENCP_VIDEO_SYNC_WAVE_CURVE 0x1bad

Bit(s)	Field Name	R/W	Default	Description
0	ENCP_VIDEO_SYNC_WAVE_CURVE	R/W	1'b1	Enable curve wave on analog sync edge

ENCP_VIDEO_MAX_LNCNT 0x1bae

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_MAX_LNCNT	R/W	10'd524	Max line counter

ENCP_VIDEO_SY_VAL 0x1bb0

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_SY_VAL	R/W	0	Analog Sync Pulse value 1

ENCP_VIDEO_SY2_VAL 0x1bb1

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_SY2_VAL	R/W	480	Analog Sync Pulse value 2

ENCP_VIDEO_BLANKY_VAL 0x1bb2

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_BLANKY_VAL	R/W	10'd240	Blank Y value

ENCP_VIDEO_BLANKPB_VAL 0x1bb3

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_BLANKPB_VAL	R/W	10'd512	Blank Pb value

ENCP_VIDEO_BLANKPR_VAL 0x1bb4

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_VIDEO_BLANKPR_VAL	R/W	10'd512	Blank Pr value

ENCP_VIDEO_HOFFST 0x1bb5

Bit(s)	Field Name	R/W	Default	Description
13 -0	ENCP_VIDEO_HOFFST	R/W	2	Horizontal offset after HSI

ENCP_VIDEO_VOFFST 0x1bb6

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_VIDEO_VOFFST	R/W	0	Vertical offset after VSI

ENCP_VIDEO_RGB_CTRL 0x1bb7

Bit(s)	Field Name	R/W	Default	Description
12-8	CFG_BLANK_DLY	R/W	4	
6	CFG_MACV_R_EN	R/W	0	
5	CFG_MACV_G_EN	R/W	0	
4	CFG_MACV_B_EN	R/W	0	
3	CFG_RGB_SEPERATE_BLANK	R/W	0	
2	CFG_SYNC_ON_R	R/W	0	
1	CFG_SYNC_ON_G	R/W	1	
0	CFG_SYNC_ON_B	R/W	0	

ENCP_VIDEO_FILT_CTRL 0x1bb8

Bit(s)	Field Name	R/W	Default	Description
15	ENCP_VIDEO_FILT_YF_NO_RST	R/W	0	Disable auto reset Y filter each line
14	ENCP_VIDEO_FILT_CF_NO_RST	R/W	0	Disable auto reset C filter each line
14	CFILT_CHROMA444_EN	R/W	0	If true, chroma input is 444 instead of 422
12	ENCP_VIDEO_FILT_BYPASS_TOP	R/W	0	By pass all ENCP filter
11	ENCP_VIDEO_FILT_CHROMA_SWAP	R/W	0	Swap chroma Cb/Cr
10:8	ENCP_VIDEO_FILT_CF_BYPASS	R/W	0	Chroma filter by pass control
7:4	ENCP_VIDEO_FILT_YF_CFG1	R/W	0	4 Bits Y filter parameter 1, will be effect after ENCP_VIDEO_YFP1_HTIME Bit 3 : Edge mode Bit 2:0 : By pass ctrl
3:0	ENCP_VIDEO_FILT_YF_CFG2	R/W	0	4 Bits Y filter parameter 1, will be effect after ENCP_VIDEO_YFP1_HTIME Bit 3 : Edge mode Bit 2:0 : By pass ctrl

ENCP_ VIDEO_OFLD_VPEQ_OFST 0x1bb9

Bit(s)	Field Name	R/W	Default	Description
15:12	ENCP_VIDEO_OFLD_VPULS_OFST_BEGIN	R/W	0	Odd field Vsync pulse offset begin, 4 Bits signed.
11:8	ENCP_VIDEO_OFLD_VPULS_OFST_END	R/W	1	Odd field Vsync pulse offset end, 4 Bits signed.
7:4	ENCP_VIDEO_OFLD_EQPULS_OFST_BEGIN	R/W	0	Odd field EQU pulse offset begin, 4 Bits signed.
3:0	ENCP_VIDEO_OFLD_EQPULS_OFST_END	R/W	0	Odd field EQU pulse offset end, 4 Bits signed.

ENCP_ VIDEO_OFLD_VOAV_OFST 0x1bba

Bit(s)	Field Name	R/W	Default	Description
15:12	ENCP_VIDEO_OFLD_VSO_OFST_BEGIN	R/W	0	Odd field VSO offset begin, 4 Bits signed.
11:8	ENCP_VIDEO_OFLD_VSO_OFST_END	R/W	1	Odd field VSO offset end, 4 Bits signed.
7:4	ENCP_VIDEO_OFLD_VAVON_OFST_BEGIN	R/W	1	Odd field VAVON offset begin, 4 Bits signed.
3:0	ENCP_VIDEO_OFLD_VAVON_OFST_END	R/W	1	Odd field VAVON offset end, 4 Bits signed.

ENCP_ VIDEO_MATRIX_CB 0x1bbb

Bit(s)	Field Name	R/W	Default	Description
15:8	ENCP_VIDEO_MATRIX_MA	R/W	0	CbCr matrix parameter Ma (signed value)
7:0	ENCP_VIDEO_MATRIX_MB	R/W	0	CbCr matrix parameter Mb (signed value)

Note: These 2 register is for HUE adjustment. The formula is : Cb' = Cb*Ma + Cr*Mb, Cr' = Cb*Mc + Cr*Md
(effective only when Enable HUE matrix by Bit ENCP_VIDEO_MODE_ADV[7])

Note : see the descritption of register ENCI_CMPN_MATRIX_CB.

ENCP_ VIDEO_MATRIX_CR 0x1bbc

Bit(s)	Field Name	R/W	Default	Description
15:8	ENCP_VIDEO_MATRIX_MC	R/W	0	CbCr matrix parameter Mc (signed value)
7:0	ENCP_VIDEO_MATRIX_MD	R/W	0	CbCr matrix parameter Md (signed value)

ENCP_ VIDEO_RGBIN_CTRL 0x1bbd

Bit(s)	Field Name	R/W	Default	Description
1		R/W	0	USE RGB data from VIU
0		R/W	0	VIU RGB IN BLANK ZERO

ENCP_MACV_BLANKY_VAL 0x1bc0

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_MACV_BLANKY_VAL	R/W	0	Macrovision Blank Y value

ENCP_MACV_MAXY_VAL 0x1bc1

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_MACV_MAXY_VAL	R/W	590	Macrovision max Y value

ENCP_MACV_1ST_PSSYNC_STRT 0x1bc2

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCP_MACV_1ST_PSSYNC_STRT	R/W	238	Macrovision first pseudo sync start

ENCP_MACV_PSSYNC_STRT 0x1bc3

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_MACV_PSSYNC_STRT	R/W	1	Macrovision pseudo sync start

ENCP_MACV_AGC_STRT 0x1bc4

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_MACV_AGC_STRT	R/W	61	Macrovision AGC pulse start

ENCP_MACV_AGC_END 0x1bc5

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_MACV_AGC_END	R/W	141	Macrovision AGC pulse end

ENCP_MACV_WAVE_END 0x1bc6

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCP_MACV_WAVE_END	R/W	175	Macrovision wave end

ENCP_MACV_STRTLINE 0x1bc7

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_MACV_STRTLINE	R/W	11	Macrovision start line

ENCP_MACV_ENDLINE 0x1bc8

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCP_MACV_ENDLINE	R/W	19	Macrovision end line

ENCP_MACV_TS_CNT_MAX_L 0x1bb9

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCP_MACV_TS_CNT_MAX_L	R/W	16'h7dcd	Macrovistion Cyclic Variation Time step Counter, Low 16Bits

ENCP_MACV_TS_CNT_MAX_H 0x1bca

Bit(s)	Field Name	R/W	Default	Description
3 -0	ENCP_MACV_TS_CNT_MAX_H	R/W	4'h3	Macrovistion Cyclic Variation Time step Counter, High 4Bits

ENCP_MACV_TIME_DOWN 0x1bcb

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCP_MACV_TIME_DOWN	R/W	16'd3068	Macrovistion Cyclic Variation Time start going down

ENCP_MACV_TIME_LO 0x1bbc

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCP_MACV_TIME_LO	R/W	16'd3658	Macrovistion Cyclic Variation Time start maitain low

ENCP_MACV_TIME_UP 0x1bcd

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCP_MACV_TIME_UP	R/W	16'd4366	Macrovistion Cyclic Variation Time start going up

ENCP_MACV_TIME_RST 0x1bce

Bit(s)	Field Name	R/W	Default	Description
15 -0	ENCP_MACV_TIME_RST	R/W	16'd4956	Macrovistion Cyclic Variation reset

ENCP_VBI_CTRL 0x1bd0

Bit(s)	Field Name	R/W	Default	Description
1	ENCP_VBI_EN	R/W	0	Enable VBI
0	ENCP_VBI_NO_CURVE	R/W	0	VBI data no curve at edge

ENCP_VBI_SETTING 0x1bd1

Bit(s)	Field Name	R/W	Default	Description
1	ENCP_VBI_LN	R/W	0x16	VBI line number
0	ENCP_VBI_CNT	R/W	0x28	VBI data bitcount

ENCP_VBI_BEGIN 0x1bd2

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_VBI_BEGIN	R/W	0	VBI pulse begin point

ENCP_VBI_WIDTH 0x1bd3

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_VBI_WIDTH	R/W	0	VBI data bitwidth

ENCP_VBI_HVAL 0x1bd4

Bit(s)	Field Name	R/W	Default	Description
9-0	ENCP_VBI_HVAL	R/W	0	VBI pulse value when data bit is high

ENCP_VBI_DATA0 0x1bd5)

Bit(s)	Field Name	R/W	Default	Description
15-0	ENCP_VBI_DATA0	R/W	0	VBI data 0 (LSB first)

ENCP_VBI_DATA1 0x1bd6

Bit(s)	Field Name	R/W	Default	Description
15-0	ENCP_VBI_DATA1	R/W	0	VBI data 1 (LSB first)

VENC_VDAC_DAC0_GAINCTRL 0x1bf0

Bit(s)	Field Name	R/W	Default	Description
15	DAC_GAIN_BP	R/W	0	gain bypass, 1:bypass
14-8		R/W	0	Unused
7-0	DAC_GAIN	R/W	0	gain setting 8-bit

VENC_VDAC_DAC0_OFFSET 0x1bf1

Bit(s)	Field Name	R/W	Default	Description
10-0	DAC_OFFSET_VAL	R/W	0	offset setting, 11 Bits

VENC_VDAC_DAC1_GAINCTRL 0x1bf2

Bit(s)	Field Name	R/W	Default	Description
15	DAC_GAIN_BP	R/W	0	gain bypass, 1:bypass
14-8		R/W	0	Unused

Bit(s)	Field Name	R/W	Default	Description
7-0	DAC_GAIN	R/W	0	gain setting 8-bit

VENC_VDAC_DAC1_OFFSET 0x1bf3

Bit(s)	Field Name	R/W	Default	Description
10-0	DAC_OFFSET_VAL	R/W	0	offset setting, 11 Bits

VENC_VDAC_DAC2_GAINCTRL 0x1bf4

Bit(s)	Field Name	R/W	Default	Description
15	DAC_GAIN_BP	R/W	0	gain bypass, 1:bypass
14-8		R/W	0	Unused
7-0	DAC_GAIN	R/W	0	gain setting 8-bit

VENC_VDAC_DAC2_OFFSET 0x1bf5

Bit(s)	Field Name	R/W	Default	Description
10-0	DAC_OFFSET_VAL	R/W	0	offset setting, 11 Bits

VENC_VDAC_DAC3_GAINCTRL 0x1bf6

Bit(s)	Field Name	R/W	Default	Description
15	DAC_GAIN_BP	R/W	0	gain bypass, 1:bypass
14-8		R/W	0	Unused
7-0	DAC_GAIN	R/W	0	gain setting 8-bit

VENC_VDAC_DAC3_OFFSET 0x1bf7

Bit(s)	Field Name	R/W	Default	Description
10-0	DAC_OFFSET_VAL	R/W	0	offset setting, 11 Bits

VENC_VDAC_DAC4_GAINCTRL 0x1bf8

Bit(s)	Field Name	R/W	Default	Description
15	DAC_GAIN_BP	R/W	0	gain bypass, 1:bypass
14-8		R/W	0	Unused
7-0	DAC_GAIN	R/W	0	gain setting 8-bit

VENC_VDAC_DAC4_OFFSET 0x1bf9

Bit(s)	Field Name	R/W	Default	Description
10-0	DAC_OFFSET_VAL	R/W	0	offset setting, 11 Bits

VENC_VDAC_DAC5_GAINCTRL 0x1bfa

Bit(s)	Field Name	R/W	Default	Description
15	DAC_GAIN_BP	R/W	0	gain bypass, 1:bypass
14-8		R/W	0	Unused
7-0	DAC_GAIN	R/W	0	gain setting 8-bit

VENC_VDAC_DAC5_OFFSET 0x1bfb

Bit(s)	Field Name	R/W	Default	Description
10-0	DAC_OFFSET_VAL	R/W	0	offset setting, 11 Bits

VENC_VDAC_FIFO_CTRL 0x1bfc

Bit(s)	Field Name	R/W	Default	Description
14	FIFO_EN_ENCT	R/W	0	
13	FIFO_EN_ENCI	R/W	0	
12	FIFO_EN_CNCP	R/W	0	
11-6	DAC_CLOCK_2X	R/W	0	
5-0	DAC_CLOCK_4X	R/W	0	

ENCL_TCON_INVERT_CTL 0x1bfd

Bit(s)	Field Name	R/W	Default	Description
15		R/W	1'b0	vsync invert
14		R/W	1'b0	hsync invert
13		R/W	1'b0	Oev3 invert
12		R/W	1'b0	Oev2 invert
11		R/W	1'b0	Cpv2 invert
10		R/W	1'b0	Cph3 invert
9		R/W	1'b0	Cph2 invert
8		R/W	1'b0	Cph1 invert
7		R/W	1'b0	oeh invert
6		R/W	1'b0	vcom invert
5		R/W	1'b0	Stv2 invert
4		R/W	1'b0	Stv1 invert
3		R/W	1'b0	Cpv1 invert
2		R/W	1'b0	Oev1 invert
1		R/W	1'b0	Sth1 invert
0		R/W	1'b0	Sth2 invert

ENCI_DVI_HSO_BEGIN 0x1c00

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_DVI_HSO_BEGIN	R/W	1713	DVI/HDMI Interlace HSO begin position.

ENCI_DVI_HSO_END 0x1c01

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_DVI_HSO_END	R/W	121	DVI/HDMI Interlace HSO end position.

ENCI_DVI_VSO_BLINE_EVN 0x1c02

Bit(s)	Field Name	R/W	Default	Description
8-0	ENCI_DVI_VSO_BLINE_EVN	R/W	261	DVI/HDMI Interlace VSO start line for even field.

ENCI_DVI_VSO_BLINE_ODD 0x1c03

Bit(s)	Field Name	R/W	Default	Description
8-0	ENCI_DVI_VSO_BLINE_ODD	R/W	261	DVI/HDMI Interlace VSO start line for odd field.

ENCI_DVI_VSO_ELINE_EVN 0x1c04

Bit(s)	Field Name	R/W	Default	Description
8-0	ENCI_DVI_VSO_ELINE_EVN	R/W	1	DVI/HDMI Interlace VSO end line for even field.

ENCI_DVI_VSO_ELINE_ODD 0x1c05

Bit(s)	Field Name	R/W	Default	Description
8-0	ENCI_DVI_VSO_ELINE_ODD	R/W	2	DVI/HDMI Interlace VSO end line for odd field.

ENCI_DVI_VSO_BEGIN_EVN 0x1c06

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_DVI_VSO_BEGIN_EVN	R/W	855	DVI/HDMI Interlace VSO begin position for even field.

ENCI_DVI_VSO_BEGIN_ODD 0x1c07

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_DVI_VSO_BEGIN_ODD	R/W	1713	DVI/HDMI Interlace VSO begin position for odd field.

ENCI_DVI_VSO_END_EVN 0x1c08

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_DVI_VSO_END_EVN	R/W	1713	DVI/HDMI Interlace VSO end position for even field.

ENCI_DVI_VSO_END_ODD 0x1c09

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_DVI_VSO_END_ODD	R/W	855	DVI/HDMI Interlace VSO end position for odd field.

ENCI_CFILT_CTRL2 0x1c0a

Bit(s)	Field Name	R/W	Default	Description
15-12	ENCI_CFILT_CVBS_CB_DLY	R/W	0	Filter CVBS Cb delay. Delay same as below.
11-8	ENCI_CFILT_CVBS_CR_DLY	R/W	0	Filter CVBS Cr delay. Delay same as below.
7-4	ENCI_CFILT_CMPT_CB_DLY	R/W	0	Filter component Cb delay. Delay same as below.
3-0	ENCI_CFILT_CMPT_CR_DLY	R/W	0	Filter component Cr delay. 0=No delay; 1=Delay by 1 cycle; ... 6=Delay by 6 cycles; 7-16=Reserved.

ENCI_DACSEL0 0x1c0b

Bit(s)	Field Name	R/W	Default	Description
15-12	VENC_I_DACSEL_0	R/W	0	dac3
11-8	VENC_I_DACSEL_0	R/W	3	dac2
7-4	VENC_I_DACSEL_0	R/W	2	dac1
3-0	VENC_I_DACSEL_0	R/W	1	dac0

ENCI_DACSEL1 0x1c0c

Bit(s)	Field Name	R/W	Default	Description
9-8	DVI_SYNC_SEL	R/W	0	Dvi_sync_sel
7-4	VENC_I_DACSEL_1	R/W	5	dac5
3-0	VENC_I_DACSEL_1	R/W	4	dac4

ENCP_DACSEL0 0x1c0d

Bit(s)	Field Name	R/W	Default	Description
15-12	VENC_P_DACSEL_0	R/W	0	dac3
11-8	VENC_P_DACSEL_0	R/W	3	dac2
7-4	VENC_P_DACSEL_0	R/W	2	dac1
3-0	VENC_P_DACSEL_0	R/W	1	dac0

ENCP_DACSEL1 0x1c0e

Bit(s)	Field Name	R/W	Default	Description
9-8	DVI_SYNC_SEL	R/W	0	Dvi_sync_sel
7-4	VENC_P_DACSEL_1	R/W	5	dac5
3-0	VENC_P_DACSEL_1	R/W	4	dac4

ENCP_MAX_LINE_SWITCH_POINT 0x1c0f

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_DE_V_END_ODD	R/W	13'h1fff	max_pxcnt = (line >= cfg_max_line_switch_point) ? max_pxcnt_tmp - 1: max_pxcnt_tmp;

ENCI_TST_EN 0x1c10

Bit(s)	Field Name	R/W	Default	Description
0	ENCI_TST_EN	R/W	0	Enci_tst_en

ENCI_TST_MDSEL 0x1c11

Bit(s)	Field Name	R/W	Default	Description
1-0	ENCI_TST_MDSEL	R/W	1	Video test mode selectl: 0: enci_tst_mode_fixval 1: enci_tst_mode_colorbar

Bit(s)	Field Name	R/W	Default	Description
				2: enci_tst_mode_thinline 3: enci_tst_mode_dotgrid

ENCI_TST_Y 0x1c12

Bit(s)	Field Name	R/W	Default	Description
9-0	ENCI_TST_Y	R/W	512	Default value of Y in test mode

ENCI_TST_CB 0x1c13

Bit(s)	Field Name	R/W	Default	Description
9-0	ENCI_TST_CB	R/W	512	Default value of Pb in test mode

ENCI_TST_CR 0x1c14

Bit(s)	Field Name	R/W	Default	Description
9-0	ENCI_TST_CR	R/W	512	Default value of Pr in test mode

ENCI_TST_CLRBAR_STRT 0x1c15

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_TST_CLRBAR_STRT	R/W	275	Color bar start position

ENCI_TST_CLRBAR_WIDTH 0x1c16

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_TST_CLRBAR_WIDTH	R/W	360	Color bar width

ENCI_TST_VDCNT_STSEL 0x1c17

Bit(s)	Field Name	R/W	Default	Description
1-0	ENCI_TST_VDCNT_STSEL	R/W	0	For interlace, vdata count set when color bar start

ENCI_VFIFO2VD_CTL 0x1c18

Bit(s)	Field Name	R/W	Default	Description
15-8	VFIFO2VD_VD_SEL	R/W	'h1b	Vfifo2vd_vd_sel: 00_01_10_11 -> Y_Cb_Y_Cr
7	VFIFO2VD_DROP	R/W	0	Vfifo2vd_drop
6-1	VFIFO2VD_DELAY	R/W	0	Vfifo2vd_delay
0	VFIFO2VD_EN	R/W	0	Vfifo2vd_en

ENCI_VFIFO2VD_PIXEL_START 0x1c19

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCI_VFIFO2VD_PIXEL_START	R/W	0	Vfifo2vd_pixel_start

ENCI_VFIFO2VD_PIXEL_END 0x1c1a

Bit(s)	Field Name	R/W	Default	Description
15	VDATA_YC_USE_FIRST_VFIFO_REG	R/W	0	Vdata_yc_use_vfifo_req
14-13	RESERVED			
12-0	ENCI_VFIFO2VD_PIXEL_END	R/W	0	Vfifo2vd_pixel_end

ENCI_VFIFO2VD_LINE_TOP_START 0x1c1b

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_VFIFO2VD_LINE_TOP_START	R/W	0	enci_vfifo2vd_line_top_start

ENCI_VFIFO2VD_LINE_TOP_END 0x1c1c

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_VFIFO2VD_LINE_TOP_END	R/W	0	enci_vfifo2vd_line_top_end

ENCI_VFIFO2VD_LINE_BOT_START 0x1c1d

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_VFIFO2VD_LINE_BOT_START	R/W	0	enci_vfifo2vd_line_bot_start

ENCI_VFIFO2VD_LINE_BOT_END 0x1c1e

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCI_VFIFO2VD_LINE_BOT_END	R/W	0	enci_vfifo2vd_line_bot_end

ENCI_VFIFO2VD_CTL2 0x1c1f

Bit(s)	Field Name	R/W	Default	Description
1	CFG_VFIFO2VD_OUT_SCALER_BYPASS	R/W	1	cfg_vfifo2vd_out_scaler_bypass
0	CFG_VFIFO_DIN_FULL_RANGE	R/W	0	cfg_vfifo_din_full_range

ENCP_DVI_HSO_BEGIN 0x1c30

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_DVI_HSO_BEGIN	R/W	16	DVI/HDMI Hsync out start point

ENCP_DVI_HSO_END 0x1c31

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_DVI_HSO_END	R/W	32	DVI/HDMI Hsync out end point

ENCP_DVI_VSO_BLINE_EVN 0x1c32

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCP_DVI_VSO_BLINE_EVN	R/W	40	DVI/HDMI Vsync out start line for even field.

ENCP_DVI_VSO_BLINE_ODD 0x1c33

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCP_DVI_VSO_BLINE_ODD	R/W	40	DVI/HDMI Vsync out start line for odd field.

ENCP_DVI_VSO_ELINE_EVN 0x1c34

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCP_DVI_VSO_ELINE_EVN	R/W	42	DVI/HDMI Vsync out end line for even field.

ENCP_DVI_VSO_ELINE_ODD 0x1c35

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCP_DVI_VSO_ELINE_ODD	R/W	42	DVI/HDMI Vsync out end line for odd field.

ENCP_DVI_VSO_BEGIN_EVN 0x1c36

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_DVI_VSO_BEGIN_EVN	R/W	16	DVI/HDMI Vsync out start point for even field.

ENCP_DVI_VSO_BEGIN_ODD 0x1c37

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_DVI_VSO_BEGIN_ODD	R/W	16	DVI/HDMI Vsync out start point for odd field.

ENCP_DVI_VSO_END_EVN 0x1c38

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_DVI_VSO_END_EVN	R/W	32	DVI/HDMI Vsync out end point for even field.

ENCP_DVI_VSO_END_ODD 0x1c39

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_DVI_VSO_END_ODD	R/W	32	DVI/HDMI Vsync out end point for odd field.

ENCP_DE_H_BEGIN 0x1c3a

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_DE_H_BEGIN	R/W	217	DVI/HDMI horizontal active video start point.

ENCP_DE_H_END 0x1c3b

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCP_DE_H_END	R/W	1657	DVI/HDMI horizontal active video end point.

ENCP_DE_V_BEGIN_EVEN 0x1c3c

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCP_DE_V_BEGIN_EVEN	R/W	42	DVI/HDMI vertical active video start line for even field.

ENCP_DE_V_END_EVEN 0x1c3d

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCP_DE_V_END_EVEN	R/W	519	DVI/HDMI vertical active video end line for even field.

ENCP_DE_V_BEGIN_ODD 0x1c3e

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCP_DE_V_BEGIN_ODD	R/W	42	DVI/HDMI vertical active video start line for odd field.

ENCP_DE_V_END_ODD 0x1c3f

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCP_DE_V_END_ODD	R/W	519	DVI/HDMI vertical active video end line for odd field.

ENCI_SYNC_LINE_LENGTH 0x1c40

Bit(s)	Field Name	R/W	Default	Description
15-11	SYNC_PULSE_LENGTH	R/W	0	Sync_pulse_length
10-0	SYNC_PULSE_START_LINE	R/W	0	Sync_pulse_start_line

ENCI_SYNC_PIXEL_EN 0x1c41

Bit(s)	Field Name	R/W	Default	Description
15	SYNC_PULSE_EN	R/W	0	Sync_pulse_enable
14	RESERVED	R/W	0	
13	SHORT_FUSSY_SYNC	R/W	0	Short_fussy_sync
12-0	SYNC_PULSE_START_PIXEL	R/W	0	Sync_pulse_start_pixel

ENCI_SYNC_TO_LINE_EN 0x1c42

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_SYNC_ENALBE	R/W	0	Enci_sync_enable
14	ENCP_SYNC_ENALBE	R/W	0	Encp_sync_enable
13	ENCT_SYNC_ENALBE	R/W	0	Enct_sync_enable
12	ENCL_SYNC_ENALBE	R/W	0	Encl_sync_enable
11	FUSSY_SYNC_ENABLE	R/W	0	Fussy_sync_enable
10-0	SYNC_PULSE_TARGET_LINE	R/W	0	Sync_pulse_target_line

ENCI_SYNC_TO_PIXEL 0x1c43

Bit(s)	Field Name	R/W	Default	Description
12-0	SYNC_PULSE_TARGET_PIXEL	R/W	0	Sync_pulse_target_pixel

ENCP_SYNC_LINE_LENGTH 0x1c44

Bit(s)	Field Name	R/W	Default	Description
15-11	SYNC_PULSE_LENGTH	R/W	0	Sync_pulse_length
10-0	SYNC_PULSE_START_LINE	R/W	0	Sync_pulse_start_line

ENCP_SYNC_PIXEL_EN 0x1c45

Bit(s)	Field Name	R/W	Default	Description
15	SYNC_PULSE_EN	R/W	0	Sync_pulse_enable
14	RESERVED	R/W	0	
13	SHORT_FUSSY_SYNC	R/W	0	Short_fussy_sync
12-0	SYNC_PULSE_START_PIXEL	R/W	0	Sync_pulse_start_pixel

ENCP_SYNC_TO_LINE_EN 0x1c46

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_SYNC_ENALBE	R/W	0	Enci_sync_enable
14	ENCP_SYNC_ENALBE	R/W	0	Encp_sync_enable
13	ENCT_SYNC_ENALBE	R/W	0	Enct_sync_enable
12	ENCL_SYNC_ENALBE	R/W	0	Encl_sync_enable
11	FUSSY_SYNC_ENABLE	R/W	0	Fussy_sync_enable
10-0	SYNC_PULSE_TARGET_LINE	R/W	0	Sync_pulse_target_line

ENCP_SYNC_TO_PIXEL 0x1c47

Bit(s)	Field Name	R/W	Default	Description
12-0	SYNC_PULSE_TARGET_PIXEL	R/W	0	Sync_pulse_target_pixel

ENCL_SYNC_LINE_LENGTH 0x1c4c

Bit(s)	Field Name	R/W	Default	Description
15-11	SYNC_PULSE_LENGTH	R/W	0	Sync_pulse_length
10-0	SYNC_PULSE_START_LINE	R/W	0	Sync_pulse_start_line

ENCL_SYNC_PIXEL_EN 0x1c4d

Bit(s)	Field Name	R/W	Default	Description
15	SYNC_PULSE_EN	R/W	0	Sync_pulse_enable
14	RESERVED	R/W	0	
13	SHORT_FUSSY_SYNC	R/W	0	Short_fussy_sync
12-0	SYNC_PULSE_START_PIXEL	R/W	0	Sync_pulse_start_pixel

ENCL_SYNC_TO_LINE_EN 0x1c4e

Bit(s)	Field Name	R/W	Default	Description
15	ENCI_SYNC_ENALBE	R/W	0	Enci_sync_enable
14	ENCP_SYNC_ENALBE	R/W	0	Encp_sync_enable
13	ENCT_SYNC_ENALBE	R/W	0	Enct_sync_enable
12	ENCL_SYNC_ENALBE	R/W	0	Encl_sync_enable
11	FUSSY_SYNC_ENABLE	R/W	0	Fussy_sync_enable
10-0	SYNC_PULSE_TARGET_LINE	R/W	0	Sync_pulse_target_line

ENCL_SYNC_TO_PIXEL 0x1c4f

Bit(s)	Field Name	R/W	Default	Description
12-0	SYNC_PULSE_TARGET_PIXEL	R/W	0	Sync_pulse_target_pixel

ENCP_VFIFO2VD_CTL2 0x1c50

Bit(s)	Field Name	R/W	Default	Description
3	VFIFO2VD_ENCP_LCD_SCALER_BYPASS	R/W	1	0=Scale LCD input data to y [16*4,235*4], c [16*4,240*4] 1=Do not scale LCD input data
2	VFIFO2VD_ENCP_VADJ_SCALER_BYPASS	R/W	1	0=Scale enc480p_vadj input data to y [16*4,235*4], c [16*4,240*4] 1=Do not scale data to enc480p_vadj
1	VFIFO2VD_OUT_SCALER_BYPASS	R/W	1	0=Scale vfifo2vd's output vdata to y[16,235], c[16,240] 1=Do not scale vfifo2vd's output vdata
0	VFIFO_DIN_FULL_RANGE	R/W	0	0=Data from viu fifo is y[16*4,235*4], c[16*4,240*4] 1=Data from viu fifo is full range [0,1023]

VENC_DVI_SETTING_MORE 0x1c51

Bit(s)	Field Name	R/W	Default	Description
0	VENC_DVI_SEL_RGB	R/W	0	Applicable for using on-chip hdmi tx module only. This bit controls correct Bit(s)-mapping from Venc to hdmi_tx depending on whether YCbCr or RGB mode. 0=Map data bitfrom Venc to hdmi_tx for YCbCr mode; 1=Map data bitfrom Venc to hdmi_tx for RGB mode.

VENC_VDAC_DAC0_FILT_CTRL0 0x1c58

Bit(s)	Field Name	R/W	Default	Description
0	VENC_VDAC_DAC0_FILT_EN	R/W	0	0=Bypass filter; 1=Enable filter.

VENC_VDAC_DAC0_FILT_CTRL1 0x1c59

Notes: dout = ((din + din_d2) * coef1 + (din_d1 * coef0) + 32) >> 6

Bit(s)	Field Name	R/W	Default	Description
15-8	VENC_VDAC_DAC0_FILT_COEF1	R/W	8’h00	Filter coef1
7-0	VENC_VDAC_DAC0_FILT_COEF0	R/W	8’h40	Filter coef0

VENC_VDAC_DAC1_FILT_CTRL0 0x1c5a

Bit(s)	Field Name	R/W	Default	Description
0	VENC_VDAC_DAC1_FILT_EN	R/W	0	0=Bypass filter; 1=Enable filter.

VENC_VDAC_DAC1_FILT_CTRL1 0x1c5b

Notes: dout = ((din + din_d2) * coef1 + (din_d1 * coef0) + 32) >> 6

Bit(s)	Field Name	R/W	Default	Description
15-8	VENC_VDAC_DAC1_FILT_COEF1	R/W	8’h00	Filter coef1
7-0	VENC_VDAC_DAC1_FILT_COEF0	R/W	8’h40	Filter coef0

VENC_VDAC_DAC2_FILT_CTRL0 0x1c5c

Bit(s)	Field Name	R/W	Default	Description
0	VENC_VDAC_DAC2_FILT_EN	R/W	0	0=Bypass filter; 1=Enable filter.

VENC_VDAC_DAC2_FILT_CTRL1 0x1c5d

Notes: dout = ((din + din_d2) * coef1 + (din_d1 * coef0) + 32) >> 6

Bit(s)	Field Name	R/W	Default	Description
15-8	VENC_VDAC_DAC2_FILT_COEF1	R/W	8’h00	Filter coef1
7-0	VENC_VDAC_DAC2_FILT_COEF0	R/W	8’h40	Filter coef0

VENC_VDAC_DAC3_FILT_CTRL0 0x1c5e

Bit(s)	Field Name	R/W	Default	Description
0	VENC_VDAC_DAC3_FILT_EN	R/W	0	0=Bypass filter; 1=Enable filter.

VENC_VDAC_DAC3_FILT_CTRL1 0x1c5f

Notes: dout = ((din + din_d2) * coef1 + (din_d1 * coef0) + 32) >> 6

Bit(s)	Field Name	R/W	Default	Description
15-8	VENC_VDAC_DAC3_FILT_COEF1	R/W	8’h00	Filter coef1
7-0	VENC_VDAC_DAC3_FILT_COEF0	R/W	8’h40	Filter coef0

ENCL_VFIFO2VD_CTL 0x1c90

Bit(s)	Field Name	R/W	Default	Description
15-8	VFIFO2VD_VD_SEL	R/W	‘h1b	Vfifo2vd_vd_sel: 00_01_10_11 -> Y_Cb_Y_Cr

Bit(s)	Field Name	R/W	Default	Description
7	VFIFO2VD_DROP	R/W	0	Vfifo2vd_drop
6-1	VFIFO2VD_DELAY	R/W	0	Vfifo2vd_delay
0	VFIFO2VD_EN	R/W	0	Vfifo2vd_en

ENCL_VFIFO2VD_PIXEL_START 0x1c91

Bit(s)	Field Name	R/W	Default	Description
12-0	ENCL_VFIFO2VD_PIXEL_START	R/W	0	Vfifo2vd_pixel_start

ENCL_VFIFO2VD_PIXEL_END 0x1c92

Bit(s)	Field Name	R/W	Default	Description
15	VDATA_YC_USE_FIRST_VFIFO_REG	R/W	0	Vdata_yc_use_vfifo_req
14-13	RESERVED			
12-0	ENCL_VFIFO2VD_PIXEL_END	R/W	0	Vfifo2vd_pixel_end

ENCL_VFIFO2VD_LINE_TOP_START 0x1c93

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCL_VFIFO2VD_LINE_TOP_START	R/W	0	ENCL_vfifo2vd_line_top_start

ENCL_VFIFO2VD_LINE_TOP_END 0x1c94

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCL_VFIFO2VD_LINE_TOP_END	R/W	0	ENCL_vfifo2vd_line_top_end

ENCL_VFIFO2VD_LINE_BOT_START 0x1c95

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCL_VFIFO2VD_LINE_BOT_START	R/W	0	ENCL_vfifo2vd_line_bot_start

ENCL_VFIFO2VD_LINE_BOT_END 0x1c96

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCL_VFIFO2VD_LINE_BOT_END	R/W	0	ENCL_vfifo2vd_line_bot_end

ENCL_VFIFO2VD_CTL2 0x1c97

Bit(s)	Field Name	R/W	Default	Description
3	CFG_ENCL_LCD_SCALER_BYPASS	R/W	1	cfg_encl_lcd_scaler_bypass
2	CFG_ENCL_VADJ_SCALER_BYPASS	R/W	1	cfg_encl_vadj_scaler_bypass
1	CFG_VFIFO2VD_OUT_SCALER_BYPASS	R/W	1	cfg_vfifo2vd_out_scaler_bypass
0	CFG_VFIFO_DIN_FULL_RANGE	R/W	0	cfg_vfifo_din_full_range

ENCL_TST_EN 0x1c98

Bit(s)	Field Name	R/W	Default	Description
0	ENCL_TST_EN	R/W	0	ENCL_tst_en

ENCL_TST_MDSEL 0x1c99

Bit(s)	Field Name	R/W	Default	Description
1-0	ENCL_TST_MDSEL	R/W	1	Video test mode selectl: 0: ENCL_tst_mode_fixval 1: ENCL_tst_mode_colorbar 2: ENCL_tst_mode_thinline 3: ENCL_tst_mode_dotgrid

ENCL_TST_Y 0x1c9a

Bit(s)	Field Name	R/W	Default	Description
9-0	ENCL_TST_Y	R/W	512	Default value of Y in test mode

ENCL_TST_CB 0x1c9b

Bit(s)	Field Name	R/W	Default	Description
9-0	ENCL_TST_CB	R/W	512	Default value of Pb in test mode

ENCL_TST_CR 0x1c9c

Bit(s)	Field Name	R/W	Default	Description
9-0	ENCL_TST_CR	R/W	512	Default value of Pr in test mode

ENCL_TST_CLRBAR_STRT 0x1c9d

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCL_TST_CLRBAR_STRT	R/W	275	Color bar start position

ENCL_TST_CLRBAR_WIDTH 0x1c9e

Bit(s)	Field Name	R/W	Default	Description
10-0	ENCL_TST_CLRBAR_WIDTH	R/W	360	Color bar width

ENCL_TST_VDCNT_STSEL 0x1c9f

Bit(s)	Field Name	R/W	Default	Description
1-0	ENCL_TST_VDCNT_STSEL	R/W	0	For interlace, vdata count set when color bar start

ENCL_VIDEO_EN 0x1ca0

Bit(s)	Field Name	R/W	Default	Description
0	ENCL_VIDEO_EN	R/W	0	Progressive encoder enable

ENCL_VIDEO_Y_SCL 0x1ca1

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCL_VIDEO_Y_SCL	R/W	8'd81	Y scale

ENCL_VIDEO_PB_SCL 0x1ca2

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCL_VIDEO_PB_SCL	R/W	8'd79	Cb scale

ENCL_VIDEO_PR_SCL 0x1ca3

Bit(s)	Field Name	R/W	Default	Description
7 -0	ENCL_VIDEO_PR_SCL	R/W	8'd79	Cr scale

ENCL_VIDEO_Y_OFFST 0x1ca4

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCL_VIDEO_Y_OFFST	R/W	10'h3c0	Y offset

ENCL_VIDEO_PB_OFFST 0x1ca5

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCL_VIDEO_PB_OFFST	R/W	10'h0	Pb offset

ENCL_VIDEO_PR_OFFST 0x1ca6

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCL_VIDEO_PR_OFFST	R/W	10'h0	Pr offset

ENCL_VIDEO_MODE 0x1ca7

Bit(s)	Field Name	R/W	Dflt	Description
15	ENCL_PX_LN_CNT_SHADOW_EN	R/W	0	pixel count and line count shadow enable
14	ENCL_VIDEO_MODE_DE_V	R/W	0	1=DE signal's polarity is active high. 0=DE signal's polarity is active low.
13	ENCL_VIDEO_MODE_EN_VSO_OFLD_FIX_EN	R/W	0	1=Extend ENCL_VIDEO_MAX_PXCNT by 1 pixel. 0=Treat ENCL_VIDEO_MAX_PXCNT as is.

Bit(s)	Field Name	R/W	Dflt	Description
12	ENCL_VIDEO_MODE_EN_FIELD_ODD	R/W	0	Enable odd field (for 1080i)
11	ENCL_VIDEO_MODE_EN_VSO_OFLD	R/W	0	Enable VSO odd field
10	ENCL_VIDEO _MODE_EN_VAVON_OFLD	R/W	0	Enable Vertical Active On for odd field
9	ENCL_VIDEO _MODE_EN_EQU_OFLD	R/W	0	Enable Equalization pulse for odd field
8	ENCL_VIDEO _MODE_EN_EQU	R/W	0	Enable Equalization pulse
6	ENCL_VIDEO _MODE_EN_HSEQ_SWITCH	R/W	0	Enable Hsync and equalization pulse switch in center
5	ENCL_VIDEO _MODE_EN_VP_OFLD	R/W	0	Enable Vertical Pulse for odd field
4	ENCL_VIDEO _MODE_EN_VP2	R/W	0	Enable 2nd vertical pulse in a line (1080i)
3	ENCL_VIDEO _MODE_EN_VPE_HALF_OFLD	R/W	0	Vertical pulse on end line of odd field is half
2	ENCL_VIDEO _MODE_EN_VPB_HALF_OFLD	R/W	0	Vertical pulse on begin line of odd field is half
1	ENCL_VIDEO _MODE_EN_VPE_HALF	R/W	0	Vertical pulse on end line of even field is half
0	ENCL_VIDEO _MODE_EN_VPB_HALF	R/W	0	Vertical pulse on begin line of even field is half
Note: This register should be set as 0x140 for 720p , and 0x1ffc for 1080i, and 0x0 for 480p/576p				

ENCL_VIDEO_MODE_ADV 0x1ca8

Bit(s)	Field Name	R/W	Default	Description
15-14	ENCL_SP_TIMING_CTRL	R/W	0	
13-11	RESERVED	R/W	0	
10	ENCL_SEL_GAMMA_RGB_IN	R/W	0	
9-8		R/W	0	Unused
7	ENCL_VIDEO_MODE_ADV_EN_HUE_MATRIX	R/W	0	Enable HUE matrix
6	ENCL_VIDEO_MODE_ADV_SWAP_PBPR	R/W	0	Swap PB PR
5	ENCL_VIDEO_MODE_ADV_EN_HS_PBPR	R/W	0	Enable sync pulse on PB PR
4	ENCL_VIDEO_MODE_ADV_GAIN_HDTV	R/W	0	YPBPR gain as HDTV type
3	ENCL_VIDEO_MODE_ADV_VFIFO_EN	R/W	0	Data input from VFIFO
2 :0	ENCL_VIDEO_MODE_ADV_VFIFO_UPMODE	R/W	1	Sampling rate: 0: 1 1: ½ 2: ¼ 3: 1/8

ENCL_DBG_PX_RST 0x1ca9

Bit(s)	Field Name	R/W	Default	Description
15	ENCL_DBG_PX_RST_EN	R/W	0	Debug mode pixel reset enable
12 -0	ENCL_DBG_PX_RST_VAL	R/W	0	Debug mode pixel reset value

ENCL_DBG_LN_RST 0x1caa

Bit(s)	Field Name	R/W	Default	Description
15	ENCL_DBG_LN_RST_EN	R/W	0	Debug mode line reset enable
10 -0	ENCL_DBG_LN_RST_VAL	R/W	0	Debug mode line reset value

ENCL_DBG_PX_INT 0x1cab

Bit(s)	Field Name	R/W	Default	Description
15	ENCL_DBG_PX_INT_EN	R/W	0	Pixel Interrupt enable
12 -0	ENCL_DBG_PX_INT_VAL	R/W	0	Pixel value that trig the interrupt

ENCL_DBG_LN_INT 0x1cac

Bit(s)	Field Name	R/W	Default	Description
15	ENCL_DBG_LN_INT_EN	R/W	0	Line Interrupt enable
10 -0	ENCL_DBG_LN_INT_VAL	R/W	0	Line value that trig the interrupt

ENCL_VIDEO_YC_DLY 0x1caf

Bit(s)	Field Name	R/W	Default	Description
10	ENCL_VIDEO_Y_DLY	R/W	0	Y delay[2]
8	ENCL_VIDEO_CB_DLY	R/W	0	Cb delay[2]

Bit(s)	Field Name	R/W	Default	Description
6	ENCL_VIDEO_CR_DLY	R/W	0	Cr delay[2]
5 –4	ENCL_VIDEO_Y_DLY	R/W	0	Y delay[1:0]
3 –2	ENCL_VIDEO_CB_DLY	R/W	0	Cb delay[1:0]
1 –0	ENCL_VIDEO_CR_DLY	R/W	0	Cr delay[1:0]

ENCL_VIDEO_MAX_PXCNT 0x1cb0

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCL_VIDEO_MAX_PXCNT	R/W	13'd1715	Max pixel counter

ENCL_VIDEO_HAVON_END 0x1cb1

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCL_VIDEO_HAVON_END	R/W	13'd1656	Vertical active video end point

ENCL_VIDEO_HAVON_BEGIN 0x1cb2

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCL_VIDEO_HAVON_BEGIN	R/W	13'd217	Vertical active video start point

ENCL_VIDEO_VAVON_ELINE 0x1cb3

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCL_VIDEO_VAVON_ELINE	R/W	11'd519	Vertical active video on end line

ENCL_VIDEO_VAVON_BLINE 0x1cb4

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCL_VIDEO_VAVON_BLINE	R/W	11'd42	Vertical active video on start line

ENCL_VIDEO_HSO_BEGIN 0x1cb5

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCL_VIDEO_HSO_BEGIN	R/W	16	Digital Hsync out start point

ENCL_VIDEO_HSO_END 0x1cb6

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCL_VIDEO_HSO_END	R/W	32	Digital Hsync out end point

ENCL_VIDEO_VSO_BEGIN 0x1cb7

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCL_VIDEO_VSO_BEGIN	R/W	16	Digital Vsync out start point

ENCL_VIDEO_VSO_END 0x1cb8

Bit(s)	Field Name	R/W	Default	Description
12 -0	ENCL_VIDEO_VSO_END	R/W	32	Digital Vsync out end point

ENCL_VIDEO_VSO_BLINE 0x1cb9

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCL_VIDEO_VSO_BLINE	R/W	37	Digital Vsync out start line

ENCL_VIDEO_VSO_ELINE 0x1cba

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCL_VIDEO_VSO_ELINE	R/W	39	Digital Vsync out end line

ENCL_VIDEO_MAX_LNCNT 0x1cbb

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCL_VIDEO_MAX_LNCNT	R/W	10'd524	Max line counter

ENCL_VIDEO_BLANKY_VAL 0x1cbc

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCL_VIDEO_BLANKY_VAL	R/W	10'd240	Blank Y value

ENCL_VIDEO_BLANKPB_VAL 0x1cbd

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCL_VIDEO_BLANKPB_VAL	R/W	10'd512	Blank Pb value

ENCL_VIDEO_BLANKPR_VAL 0x1cbe

Bit(s)	Field Name	R/W	Default	Description
9 -0	ENCL_VIDEO_BLANKPR_VAL	R/W	10'd512	Blank Pr value

ENCL_VIDEO_HOFFST 0x1cbf

Bit(s)	Field Name	R/W	Default	Description
13 -0	ENCL_VIDEO_HOFFST	R/W	2	Horizontal offset after HSI

ENCL_VIDEO_VOFFST 0x1cc0

Bit(s)	Field Name	R/W	Default	Description
10 -0	ENCL_VIDEO_VOFFST	R/W	0	Vertical offset after VSI

ENCL_VIDEO_RGB_CTRL 0x1cc1

Bit(s)	Field Name	R/W	Default	Description
12-8	CFG_BLANK_DLY	R/W	4	
6	CFG_MACV_R_EN	R/W	0	
5	CFG_MACV_G_EN	R/W	0	
4	CFG_MACV_B_EN	R/W	0	
3	CFG_RGB_SEPERATE_BLANK	R/W	0	
2	CFG_SYNC_ON_R	R/W	0	
1	CFG_SYNC_ON_G	R/W	1	
0	CFG_SYNC_ON_B	R/W	0	

ENCL_VIDEO_OFLD_VOAV_OFST 0x1cc4

Bit(s)	Field Name	R/W	Default	Description
15:12	ENCL_VIDEO_OFLD_VSO_OFST_BEGIN	R/W	0	Odd field VSO offset begin, 4 Bits signed.
11:8	ENCL_VIDEO_OFLD_VSO_OFST_END	R/W	1	Odd field VSO offset end, 4 Bits signed.
7:4	ENCL_VIDEO_OFLD_VAVON_OFST_BEGIN	R/W	1	Odd field VAVON offset begin, 4 Bits signed.
3:0	ENCL_VIDEO_OFLD_VAVON_OFST_END	R/W	1	Odd field VAVON offset end, 4 Bits signed.

ENCL_VIDEO_MATRIX_CB 0x1cc5

Bit(s)	Field Name	R/W	Default	Description
15:8	ENCL_VIDEO_MATRIX_MA	R/W	0	CbCr matrix parameter Ma (signed value)
7:0	ENCL_VIDEO_MATRIX_MB	R/W	0	CbCr matrix parameter Mb (signed value)

Note: These 2 register is for HUE adjustment. The formula is : Cb' = Cb*Ma + Cr*Mb, Cr' = Cb*Mc + Cr*Md
(effective only when Enable HUE matrix by bit ENCL_VIDEO_MODE_ADV[7])

Note : see the descritption of register ENCI_CMPN_MATRIX_CB.

ENCL_VIDEO_MATRIX_CR 0x1cc6

Bit(s)	Field Name	R/W	Default	Description
15:8	ENCL_VIDEO_MATRIX_MC	R/W	0	CbCr matrix parameter Mc (signed value)
7:0	ENCL_VIDEO_MATRIX_MD	R/W	0	CbCr matrix parameter Md (signed value)

ENCL_VIDEO_RGBIN_CTRL 0x1cc7

Bit(s)	Field Name	R/W	Default	Description
1		R/W	0	USE RGB data from VIU
0	CFG_VIDEO_RGBIN_ZBLK	R/W	0	VIU RGB IN BLANK ZERO

ENCL_MAX_LINE_SWITH_POINT 0x1cc8

Bit(s)	Field Name	R/W	Default	Description
13	CFG_VID_LOCK_ADJ_EN	R/W	0	
12-0	CFG_MAX_LINE_SWITH_POINT	R/W	'h1fff	

ENCL_DACSEL0 0x1cc9

Bit(s)	Field Name	R/W	Default	Description
15-12	VENC_L_DACSEL_0	R/W	0	dac3
11-8	VENC_L_DACSEL_0	R/W	3	dac2
7-4	VENC_L_DACSEL_0	R/W	2	dac1
3-0	VENC_L_DACSEL_0	R/W	1	dac0

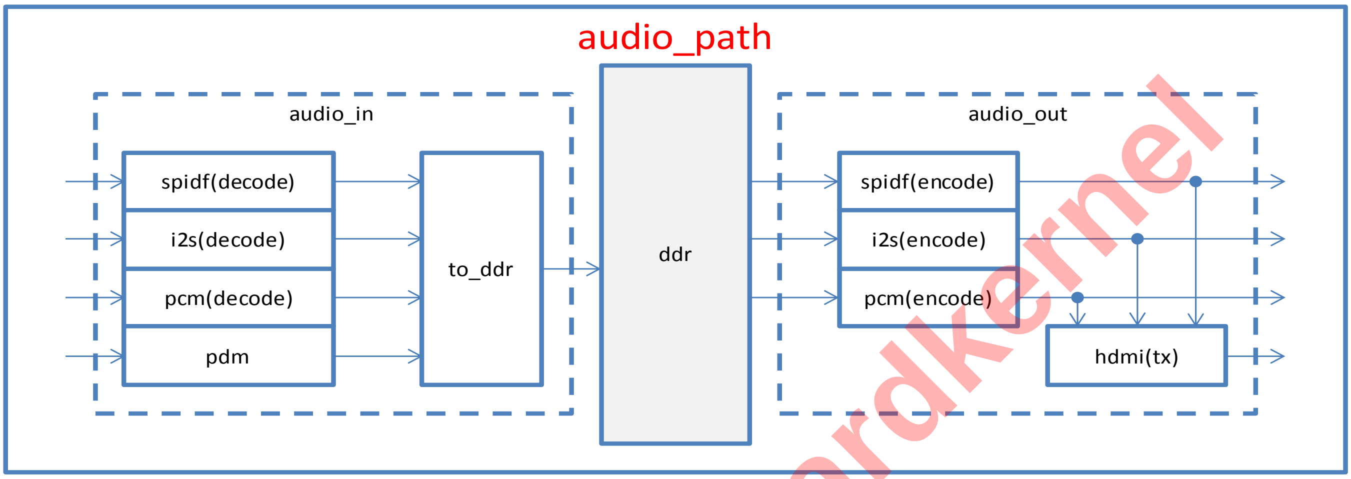
ENCL_DACSEL1 0x1cca

Bit(s)	Field Name	R/W	Default	Description
7-4	VENC_L_DACSEL_1	R/W	5	dac5
3-0	VENC_L_DACSEL_1	R/W	4	dac4

Section V Audio Path

Audio Path includes 2 parts: audio_in submodule and audio_out submodule, as illustrated in FigV.1. Audio_in part supports 4 formats of audio input, after decoding, these signal will be written to DDR via to_ddr module. Audio_out read signals from DDR and encode the signal to 4 formats of audio output.

Fig V.1 Diagram of Audio Path



30. Audio_Input

30.1 Overview

Audio_input supports 4 decoding formats: spidf, I2S, PCM and PDM, each of which has different decoding algorithm.

30.2 SPIDF

Spdif used biphase mark code(BMC) encode, it's double frequency of original data, and between two original data, there must have a invert operation.

At working status, the spdif module decodes the 1bit input it receives to 32 bit output.

The decoding procedure consists of the following 5 steps:

Resampling: lock input using a clock's(from control) posedge or negedge.

Sreg: shift store 32 input.

Find preamble: find 3 preamble and tell control.

Control: configured by register and find preamble, auto select clock.

Format: transfer 32Bit(s) data to a new format.

30.3 I2S(decode)

I2S(decode) supports 4 streams(8ch) input and 1 time division multiplexing output. Register I2S_ctrl[13:10] can be used to control it.
I2S will sent 24 Bits data in default, we can use I2S_ctrl[9:8] to mask some Bits,

30.4 PCM(decode)

The hardware will detect data_valid and frame_sync first.
Next hardware will counter data_valid, if counter reached slot_msb_Bits(pcmin_ctrl1[26:21]), that means finished receive slot0, then counter clear and start receive slot1/2/…
Each slot has 1 enable bit (pcmin_ctrl1[15:0]):

if [0] is 0, slot0 will not be sent out.
if [0] is 1, slot1 will be sent out.
if [1:0] is 2'b11, slot0 and slot1 will be sent out.
if [3:0] is 4'b1001, slot0 and slot3 will be sent out, but slot1 and slot2 will not.

Hardware has another counter to accumulate slot num. When one frame is finished(fs invert), hardware will compare it with theoretically (accumulate by pcmin_ctrl1[15:0]), if it's not the same, there will send a pcm_err to register(AUDIN_FIFO_INT[8]).

The format modification include: left_justified/msb_first/data_msb_bit (output data bit_width):

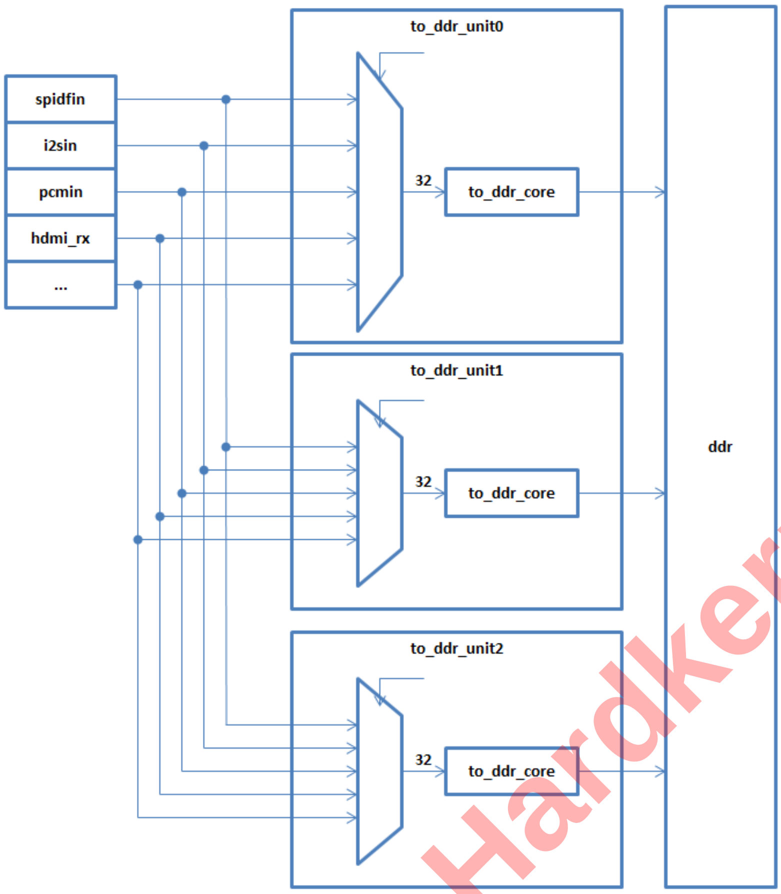
30.5 PDM

With PDM module, we can receive the pdm data and transfer it to sample data.

30.6 To_ddr

To_ddr_unit selects source audio data and modifies it, then write the modified data to the ddr memory.
The modification consists of 2 parts: audio sample format modification and the ddr address obtaining.
S905 can send 3 channels of audio data to ddr at the same time.

Fig V.30.5 Diagram of to_ddr



The to_ddr_unit functions in the following step:

Step1: select source audio.

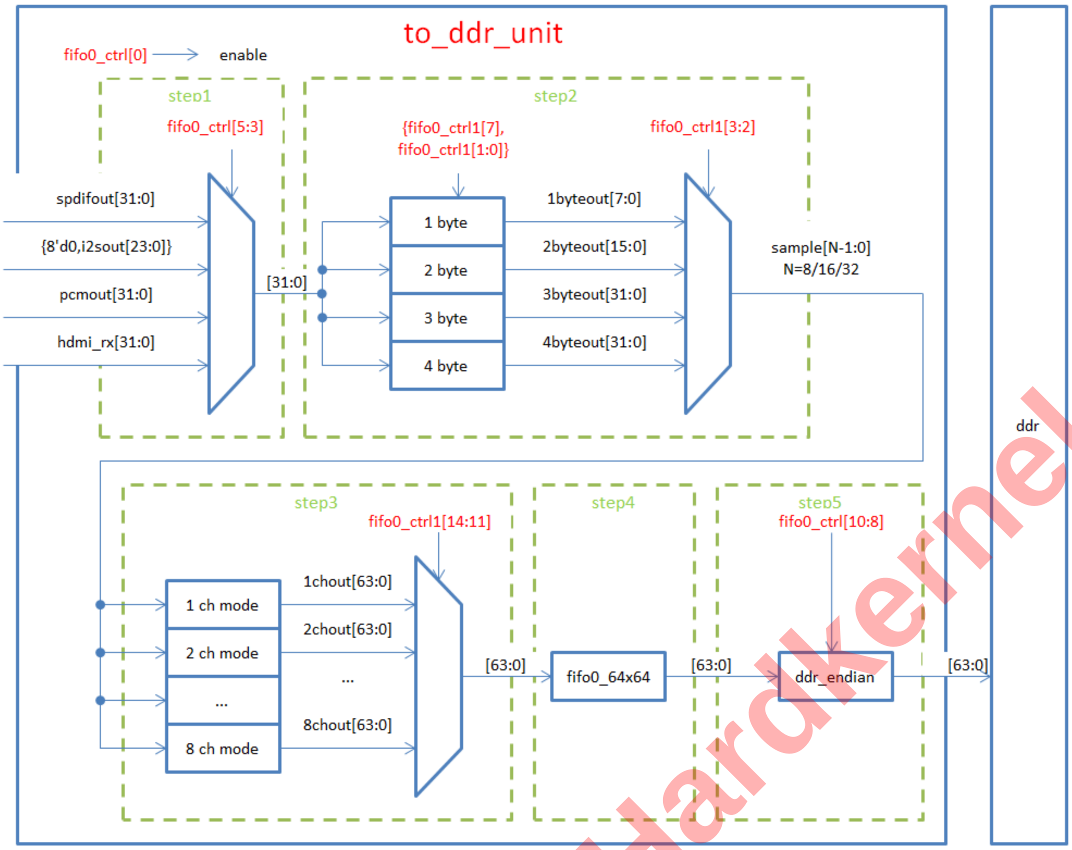
Step2: select byte number of audio sample.

Step3: select the mode of write adderss.

Step4: store audio sample to 64x64 fifo first, then read to ddr.

Step5: select endian mode before data to ddr.

Fig V.30.6 Data Path of to_ddr



30.7 Register Description

Audio In registers:

The final address of the following registers should be calculated with the following eqution:

Final Address = 0xC110A000 + offset*4

AUDIN_SPDIF_MODE 0x00

Bit(s)	R/W	Default	Description
31	RW	0x0	SPDIF_EN
30	RW	0x0	SPDIF_INT_EN
29	RW	0x0	SPDIF_BURST_PRE_INT_EN
28:25	RW	0x0	Reservered
24	RW	0x0	SPDIF_TIE_0
23	RW	0x0	SPDIF_SAMPLE_SEL
22	RW	0x0	SPDIF_REVERSE_EN
21	RW	0x1	SPDIFIN_SEL
20	RW	0x0	SPDIF_BIT_ORDER
19	RW	0x0	SPDIF_CHNL_ORDER
18	RW	0x0	SPDIF_DATA_TYPE_SEL
17	RW	0x0	Reservered
16:14	RW	0x0	SPDIF_XTDCLK_UPD_ITVL
13:0	RW	0x2501	SPDIF_CLKNUM_54U

AUDIN_SPDIF_FS_CLK_RLTN 0x01

Bit(s)	R/W	Default	Description
29：24	RW	0x7	SPDIF_CLKNUM_192K
23:18	RW	0xe	SPDIF_CLKNUM_96K
17:12	RW	0x1d	SPDIF_CLKNUM_48K
10：6	RW	0x1f	SPDIF_CLKNUM_44K
5：0	RW	0x2b	SPDIF_CLKNUM_32K

AUDIN_SPDIF_CHNL_STS_A 0x02

Bit(s)	R/W	Default	Description
31:0	R	0x0	The channel A status information

AUDIN_SPDIF_CHNL_STS_B 0x03

Bit(s)	R/W	Default	Description
31:0	R	0x0	The channel B status information

AUDIN_SPDIF_MISC0x04

Bit(s)	R/W	Default	Description
31:9	R	0x0	reserved
8	R	0x0	Burst
7	R	0x0	Valid_in
6:4	R	0x0	Xtdclk_sel: 0: 32K 1:44K 2:46K 3:48K 4:96K 5:192K
3	R	0x0	reserved
2	R	0x0	Parity error
1	R	0x0	Validity
0	R	0x0	userdata

AUDIN_SPDIF_NPCM_PCPD 0x05

Bit(s)	R/W	Default	Description
31:16	R	0x0	The burst sub pc
15:0	R	0x0	The burst sub pd

AUDIN_I2SIN_CTRL 0x10

Bit(s)	R/W	Default	Description
15	RW	0x0	I2SIN_EN
13:10	RW	0x0	I2SIN_CHAN_EN
9:8	RW	0x0	I2SIN_SIZE
7	RW	0x0	I2SIN_LRCLK_INVT
6:4	RW	0x0	I2SIN_LRCLK_SKEW
3	RW	0x0	I2SIN_POS_SYNC
2	RW	0x0	I2SIN_LRCLK_SEL
1	RW	0x0	I2SIN_CLK_SEL I2S clk selection : 0 : from pad input. 1 : from AIU.
0	RW	0x0	I2SIN_DIR

AUDIN_SOURCE_SEL 0x11

Bit(s)	R/W	Default	Description
31:15	RW	0x0	Reserved

Bit(s)	R/W	Default	Description
14:12	RW	0x0	Hdmirx_chsts_sel
11:8	RW	0x0	Hdmirx_chsts_en
7:6	RW	0x0	Reserved
5:4	RW	0x0	Spdif_src_sel
3:2	RW	0x0	Reserved
1:0	RW	0x0	I2sin_src_sel

AUDIN_DECODE_FORMAT 0x12

Bit(s)	R/W	Default	Description
31:25	RW	0x0	Reserved
24	RW	0x0	SPIDF enabled
23:22	RW	0x0	Reserved
21:20	RW	0x0	I2S_block_start_src:
19:17	RW	0x0	Reserved
16	RW	0x0	I2S enabled
15:8	RW	0x0	audio_channel_alloc
7	RW	0x0	hdmi_tx_audio_decoder input sel
6	RW	0x0	I2S_channel_config
5:4	RW	0x0	I2S_format_select
3:2	RW	0x0	I2S_bit_width
1	RW	0x0	ws polarity
0	RW	0x0	For SPDIF mode

AUDIN_DECODE_CONTROL_STATUS 0x13

Bit(s)	R/W	Default	Description
31:25	R	0x0	Reserved
24	R	0x0	channel_status stablility indicator
23:16	RW	0x0	Valid Bits for audio sample packet. [7] for valid_sp3_right, [6] for valid_sp3_left, ..., [1] for valid_sp0_right, [0] for valid_sp0_left.
15：8	RW	0x0	User Bits for audio sample packet. [7] for user_sp3_right, [6] for user_sp3_left, ..., [1] for user_sp0_right, [0] for user_sp0_left
7：4	RW	0x0	cntl_init_discard. Number of initial hdmi_tx_audio_decoder samples to discard from reset.
3	RW	0x0	cntl_invert_I2S_lrclk Invert WS before input to hdmi_tx_audio_decoder
2	RW	0x0	audio_valid_overwrite. Valid bit selection in audio packet. 0=use input data; 1=use
1	RW	0x0	audio_user_overwrite. User bit selection in audio packet. 0=use input data; 1=use
0	RW	0x0	audio_sample_valid,sample non-flat indication. 0=flat, non-valid; 1=non-flat, valid

AUDIN_DECODE_CHANNEL_STATUS_A_0 0x14

Bit(s)	R/W	Default	Description
31:0	R	0x0	Channel status information from HDMIRX, [31:0]

AUDIN_DECODE_CHANNEL_STATUS_A_1 0x15

Bit(s)	R/W	Default	Description
31:0	R	0x0	Channel status information from HDMIRX, [63:32]

AUDIN_DECODE_CHANNEL_STATUS_A_2 0x16

Bit(s)	R/W	Default	Description
31:0	R	0x0	Channel status information from HDMIRX, [95:64]

AUDIN_DECODE_CHANNEL_STATUS_A_3 0x17

Bit(s)	R/W	Default	Description
31:0	R	0x0	Channel status information from HDMIRX, [127:96]

AUDIN_DECODE_CHANNEL_STATUS_A_4 0x18

Bit(s)	R/W	Default	Description
31:0	R	0x0	Channel status information from HDMIRX, [159:128]

AUDIN_DECODE_CHANNEL_STATUS_A_5 0x19

Bit(s)	R/W	Default	Description
31:0	R	0x0	Channel status information from HDMIRX, [191:160]

AUDIN_FIFO0_START 0x20

Bit(s)	R/W	Default	Description
31:3	RW	0x1fffffff	The start address of fifo0 writes ddr.
2:0	R	0x0	reserved

AUDIN_FIFO0_END 0x21

Bit(s)	R/W	Default	Description
31:3	RW	0x1fffffff	The end address of fifo0 writes ddr.
2:0	R	0x0	reserved

AUDIN_FIFO0_PTR 0x22

Bit(s)	R/W	Default	Description
31:3	R	0x0	The current address of fifo0 writes ddr.
2:0	R	0x0	reserved

AUDIN_FIFO0_INTR 0x23

Bit(s)	R/W	Default	Description
31:3	RW	0x0	When current address of fifo0 writes ddr matched, fifo0 will generate IRQ
2:0	R	0x0	reserved

AUDIN_FIFO0_RDPTR 0x24

Bit(s)	R/W	Default	Description
31:3	RW	0x0	The read address of fifo0.
2:0	R	0x0	reserved

AUDIN_FIFO0_CTRL 0x25

Bit(s)	R/W	Default	Description
31:29	RW	0x0	reserved
28	RW	0x0	AUDIN_FIFO0_HOLD_LVL
27:26	RW	0x0	AUDIN_FIFO0_HOLD2_SEL
25:24	RW	0x0	AUDIN_FIFO0_HOLD1_SEL
23:22	RW	0x0	AUDIN_FIFO0_HOLD0_SEL
21	RW	0x0	AUDIN_FIFO0_HOLD2_EN
20	RW	0x0	AUDIN_FIFO0_HOLD1_EN
19	RW	0x0	AUDIN_FIFO0_HOLD0_EN
15	RW	0x0	AUDIN_FIFO0_UG, urgent request enable
14:11	RW	0x0	AUDIN_FIFO0_CHAN. channel number. in M1 suppose there's only 1 channel and 2 channel

10:8	RW	0x0	AUDIN_FIFO0_ENDIAN data endian control
3	RW	0x0	AUDIN_FIFO0_DIN_SEL // 0 spdifIN // 1 I2Sin // 2 PCMIN // 3 HDMI in // 4 DEMODULATOR IN
2	RW	0x0	AUDIN_FIFO0_LOAD write 1 to load address to AUDIN_FIFO0.
1	RW	0x0	AUDIN_FIFO0_RST
0	RW	0x0	AUDIN_FIFO0_EN

AUDIN_FIFO0_CTRL1 0x26

Bit(s)	R/W	Default	Description
31:8	RW	0x0	reserved
7	RW	0x0	Din_pos[2]
6	RW	0x0	Reserved
5:4	RW	0x0	Dest_sel
3:2	RW	0x0	Din_byte_num
1:0	RW	0x0	Din_pos[1:0]

AUDIN_FIFO0_LVL0 0x27

Bit(s)	R/W	Default	Description
31:3	R	0x0	Fifo0 empty lvl0
2:0	R	0x0	reserved

AUDIN_FIFO0_LVL1 0x28

Bit(s)	R/W	Default	Description
31:3	R	0x0	Fifo0 empty lvl1
2:0	R	0x0	reserved

AUDIN_FIFO0_LVL2 0x29

Bit(s)	R/W	Default	Description
31:3	R	0x0	Fifo0 empty lvl2
2:0	R	0x0	reserved

AUDIN_FIFO0_REQID 0x30

Bit(s)	R/W	Default	Description
31:18	RW	0x0	reserved
17:12	RW	0x3	Audin req burst number
11:6	RW	0x3f	Fifo0 req burst number
5:0	RW	0x0	Fifo0 req ID

AUDIN_FIFO0_WRAP 0x31

Bit(s)	R/W	Default	Description
31:16	R	0x0	reserved
15:0	R	0x0	Fifo0 wrap counter

AUDIN_FIFO1_START 0x33

Refer to FIFO0.

AUDIN_FIFO1_END 0x34

Refer to FIFO0.

AUDIN_FIFO1_PTR 0x35

Refer to FIFO0.

AUDIN_FIFO1_INTR 0x36

Refer to FIFO0.

AUDIN_FIFO1_RDPTR 0x37

Refer to FIFO0.

AUDIN_FIFO1_CTRL 0x38

Refer to FIFO0.

AUDIN_FIFO1_CTRL1 0x39

Refer to FIFO0.

AUDIN_FIFO1_LVL0 0x40

Refer to FIFO0.

AUDIN_FIFO1_LVL1 0x41

Refer to FIFO0.

AUDIN_FIFO1_LVL2 0x42

Refer to FIFO0.

AUDIN_FIFO1_REQID 0x43

Refer to FIFO0.

AUDIN_FIFO1_WRAP 0x44

Refer to FIFO0.

AUDIN_FIFO2_START 0x45

Refer to FIFO0.

AUDIN_FIFO2_END 0x46

Refer to FIFO0.

AUDIN_FIFO2_PTR 0x47

Refer to FIFO0.

AUDIN_FIFO2_INTR 0x48

Refer to FIFO0.

AUDIN_FIFO2_RDPTR 0x49

Refer to FIFO0.

AUDIN_FIFO2_CTRL 0x4a

Refer to FIFO0.

AUDIN_FIFO2_CTRL1 0x4b

Refer to FIFO0.

AUDIN_FIFO2_LVL0 0x4c

Refer to FIFO0.

AUDIN_FIFO2_LVL1 0x4d

Refer to FIFO0.

AUDIN_FIFO2_LVL2 0x4e

Refer to FIFO0.

AUDIN_FIFO2_REQID 0x4f

Refer to FIFO0.

AUDIN_FIFO2_WRAP 0x50

Refer to FIFO0.

AUDIN_INT_CTRL 0x51

Bit(s)	R/W	Default	Description
31:16	RW	0x0	reserved
15:14	RW	0x3	reserved
13	RW	0x1	Fifo2 flush mask
12	RW	0x1	Fifo2 int mask
11	RW	0x1	Fifo2 overflow int mask
10	RW	0x1	audout address trigger interrupt mask
9	RW	0x1	PCMOUT error interrupt mask
8	RW	0x1	PCMIN error interrupt mask
7	RW	0x1	AUDOUT_FIFO level low pulse interrupt mask. once the audout fifo counter lower than the 22:16Bits. it will generate one interrupt
6	RW	0x1	AUDOUT_FIFO level low level interrupt mask. if the audout fifo coutner is lower than 22:16 Bits, it will generate interrupt
5	RW	0x1	fifo1 PIO mode flush request interrupt mask
4	RW	0x1	fifo0 PIO mode flush request interrupt mask
3	RW	0x1	fifo1 address trigger interrupt mask
2	RW	0x1	fifo1 overflow interrupt mask
1	RW	0x1	fifo0 address trigger interrupt mask
0	RW	0x1	fifo0 overflow interrupt mask

AUDIN_FIFO_INT 0x52

Bit(s)	R/W	Default	Description
31:14	R	0x0	Reserved
13	R	0x0	Fifo2 flush int st
12	R	0x0	Fifo2 int st
11	R	0x0	Fifo2 overflow int st
10	R	0x0	audout address trigger interrupt. Write 1 to clean
9	R	0x0	PCMOUT error interrupt. Write 1 to clean
8	R	0x0	PCMIN error interrupt. Write 1 to clean
7	R	0x0	AUDOUT_FIFO level low pulse interrupt. Write 1 to clean
6	R	0x0	AUDOUT_FIFO level low level interrupt. Write 1 to clean
5	R	0x0	fifo1 PIO mode flush request interrupt. Write 1 to clean
4	R	0x0	fifo0 PIO mode flush request interrupt. Write 1 to clean

Bit(s)	R/W	Default	Description
3	R	0x0	fifo1 address trigger interrupt. Write 1 to clean
2	R	0x0	fifo1 overflow interrupt. Write 1 to clean
1	R	0x0	fifo0 address trigger interrupt. Write 1 to clean
0	R	0x0	fifo0 overflow interrupt. Write 1 to clean

PCMIN_CTRL0 0x60

Bit(s)	R/W	Default	Description
31	RW	0x0	PCMIN enable
30	RW	0x0	PMCIN soft reset. write 1 to reset PCMIN module
29	RW	0x0	PCMIN sync on clock posedge
18:16	RW	0x0	PCMIN fs skew 000: FS and data no skew. 001. delay fs one cycle. 010. delay fs two cycle. 011. delay fs 3 cycle. 111. delay data one cycle. 110. delay data 2 cycle. 101. delay data 3 cycle. 100. delay data 4 cycle.
15:4	RW	0x0	system clock data sample count
3	RW	0x0	system clock data sample selection 1 = use edge detection. 0 = use the clock data sample counter
2	RW	0x0	fs invert. invert the FS signal
1	RW	0x0	1 = the coming data is msb first. 0 = lsb first.
0	RW	0x0	1 = the coming data is left justified. 0 = the coming data is right justified.

PCMIN_CTRL1 0x61

Bit(s)	R/W	Default	Description
29	RW	0x0	pcmin SRC sel. 1= pcmin is from internal audio CODEC(I2S format). 0 = external PCM interface (from pad).
28	RW	0x0	pcmin clock sel. 1= internal from cts_pcm_clk. 0 = external PCM interface
27	RW	0x0	1: use negedge clock to sample the coming data. 0. use pcmin posedge clk to sample the data
26:21	RW	0x0	max slot number in one frame
20:16	RW	0x0	max bit number in one slot
15:0	RW	0x0	valid slot . Each Bit for one slot

PCMIN1_CTRL0 0x62

Bit(s)	R/W	Default	Description
31	RW	0x0	PCMIN enable.
30	RW	0x0	PMCIN soft reset. write 1 to reset PCMIN module.
29	RW	0x0	PCMIN sync on clock posedge.
18:16	RW	0x0	PCMIN fs skew. //000: FS and data no skew. //001. delay fs one cycle. //010. delay fs two cycle. //011. delay fs 3 cycle. //111. delay data one cycle. //110. delay data 2 cycle. //101. delay data 3 cycle. //100. delay data 4 cycle.
15:4	RW	0x0	system clock data sample count.

Bit(s)	R/W	Default	Description
3	RW	0x0	system clock data sample selection. 1 = use edge detection. 0 = use the clock data sample counter.
2	RW	0x0	fs invert. invert the FS signal.
1	RW	0x0	1 = the coming data is msb first. 0 = lsb first.
0	RW	0x0	1 = the coming data is left justified. 0 = the coming data is right justified.

PCMIN1_CTRL1 0x63

Bit(s)	R/W	Default	Description
29	RW	0x0	pcmin SRC sel. 1= pcmin is from internal audio CODEC(I2S format). 0 = external PCM interface (from pad).
28	RW	0x0	pcmin clock sel. 1= internal from cts_pcm_clk. 0 = external PCM interface.
27	RW	0x0	1: use negedge clock to sample the coming data. 0. use pcmin posedge clk to sample the data.
26:21	RW	0x0	max slot number in one frame.
20:16	RW	0x0	max bit number in one slot.
15:0	RW	0x0	valid slot . Each Bit for one slot.

PCMOUT_CTRL0 0x70

Bit(s)	R/W	Default	Description
31	RW	0x0	pcmout enable bit.
29	RW	0x0	pcmout 1= master mode. 0 = slave mode.
28	RW	0x0	system clock sync at pcmout posedge clock.
27	RW	0x0	system clock sync at clock edge of pcmout clock. 0 = sync on clock counter.
26：15	RW	0x0	system clock sync at counter number if sync on clock counter.
14	RW	0x0	pcmout is msb first.
13	RW	0x0	left justified.
12	RW	0x0	output data is at h24b of the input.
11：6	RW	0x0	in PCM slave mode. when pcmo received a FS, it will sync the slot bit counter to this number.
5：0	RW	0x0	in PCM slave mode. when pcmo received a FS, it will sync the frame slot counter to this number.

PCMOUT_CTRL1 0x71

Bit(s)	R/W	Default	Description
31：30	RW	0x0	pcmo output data byte number. 00 : 8Bits. 01: 16Bits. 10: 24Bits. 11: 32Bits.
28	RW	0x0	pcmo clock slow invert. invert the pcm output logic clock. for example, use negedge to output data.
27	RW	0x0	pcmo slave parts clock invert. invert the clock which is used to sample the fs_in when pcmo in slave mode.
26	RW	0x0	invert fs phase.
25	RW	0x0	invert the fs_o for master mode.
23：18	RW	0x0	fs_o start postion frame slot counter number
17：12	RW	0x0	fs_o start postion slot bit counter number.
11：6	RW	0x0	fs_o end postion frame slot counter number.
5：0	RW	0x0	fs_o end postion slot bit counter number.

PCMOUT_CTRL2 0x72

Bit(s)	R/W	Default	Description
31	RW	0x0	pcmo mute.
30：29	RW	0x0	pcmo_underrun mode. 00: the output data will use mute constant. 01: repeat the previous data.
27：22	RW	0x0	pcmo max slot number in one frame.
21：16	RW	0x0	pcmo max bit number in one slot.
15：0	RW	0x0	pcmo valid slot. Each Bit for one slot.

PCMOUT_CTRL3 0x73

Bit(s)	R/W	Default	Description
31:0	RW	0x0	pcmo mute constant value.

PCMOUT1_CTRL0 0x74

Bit(s)	R/W	Default	Description
31	RW	0x0	pcmout enable bit
29	RW	0x0	pcmout 1= master mode. 0 = slave mode
28	RW	0x0	system clock sync at pcmout posedge clock.
27	RW	0x0	system clock sync at clock edge of pcmout clock. 0 = sync on clock counter.
26:15	RW	0x0	system clock sync at counter number if sync on clock counter.
14	RW	0x0	pcmout is msb first.
13	RW	0x0	left justified.
12	RW	0x0	output data is at h24b of the input.
11:6	RW	0x0	in PCM slave mode. when pcmo received a FS, it will sync the slot bit counter to this number.
5:0	RW	0x0	in PCM slave mode. when pcmo received a FS, it will sync the frame slot counter to this number.

PCMOUT1_CTRL1 0x75

Bit(s)	R/W	Default	Description
31:30	RW	0x0	pcmo output data byte number. 00 : 8Bits. 01: 16Bits. 10: 24Bits. 11: 32Bits.
28	RW	0x0	pcmo clock slow invert. invert the pcm output logic clock. for example, use negedge to output data.
27	RW	0x0	pcmo slave parts clock invert. invert the clock which is used to sample the fs_in when pcmo in slave mode.
26	RW	0x0	invert fs phase
25	RW	0x0	invert the fs_o for master mode
23:18	RW	0x0	fs_o start postion frame slot counter number
17:12	RW	0x0	fs_o start postion slot bit counter number
11:6	RW	0x0	fs_o end postion frame slot counter number
5:0	RW	0x0	fs_o end postion slot bit counter number

PCMOUT1_CTRL2 0x76

Bit(s)	R/W	Default	Description
31	RW	0x0	pcmo mute
30:29	RW	0x0	pcmo_underrun mode. 00: the output data will use mute constant. 01: repeat the previous data
27:22	RW	0x0	pcmo max slot number in one frame
21:16	RW	0x0	pcmo max bit number in one slot
15:0	RW	0x0	pcmo valid slot. Each Bit for one slot.

PCMOUT1_CTRL3 0x77

Bit(s)	R/W	Default	Description

31:0	RW	0x0	Pcmo1 mute constant value.

AUDOUT_CTRL 0x80

Bit(s)	R/W	Default	Description
31	RW	0x0	AUDOUT FIFO enable.
30	RW	0x0	AUDOUT FIFO reset. write 1 to reset
29	RW	0x0	AUDOUT fifo load DMA address. write 1 to load.
28	RW	0x0	Clr audout wrap counter. write 1 to clear.
27	RW	0x0	clr audout rdrsp counter. write 1 to clear.
24	RW	0x0	audout next bufer enable. if in pingpeng buffer mode.
23:22	RW	0x0	audout level control write pointer selection.
21:25	RW	0x0	audout DMA one time request size.
14:8	RW	0x0	audout buffer level. buffer level must > one time DMA request size.
7	RW	0x0	audout buffer level control enable.
6	RW	0x0	1 audout DMA mode. 0. audout PIO mode.(CPU use cbus to push data.)
5	RW	0x0	audout use circur Buffer in DDR2/3 SDRAM. 1 = circur buffer mdoe. 0 = pingpang buffer mode.
4	RW	0x0	audout buffer selection if in ping pang buffer mode.
3	RW	0x0	audout DMA request urgent bit.
2:0	RW	0x0	audout DMA data endian control.

AUDOUT_CTRL1 0x81

Bit(s)	R/W	Default	Description
11:6	RW	0x0	AUDOUT DMA request burst number control for pre_mmc_arb.
5:0	RW	0x0	AUDOUT DMA request ID.

AUDOUT_BUF0_STA 0x82

Bit(s)	R/W	Default	Description
31:0	RW	0x0	buf0 start address. or circur buffer start address

AUDOUT_BUF0_EDA 0x83

Bit(s)	R/W	Default	Description
31:0	RW	0x0	buf0 end address. or circur buffer end address

AUDOUT_BUF0_WPTR 0x84

Bit(s)	R/W	Default	Description
31:0	RW	0x0	buf0 write pointer.

AUDOUT_BUF1_STA 0x85

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Buf1 start address. or circur buffer start address

AUDOUT_BUF1_EDA 0x86

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Buf1 end address. or circur buffer end address

AUDOUT_BUF1_WPTR 0x87

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Buf1 write pointer.

AUDOUT_FIFO_RPTR 0x88

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Buffer DMA read address

AUDOUT_INTR_PTR 0x89

Bit(s)	R/W	Default	Description
31:0	RW	0x0	When DMA read to this address, it will generate an interrupt to CPU

AUDOUT_FIFO_STS 0x8a

Bit(s)	R/W	Default	Description
31:7	R	0x0	reserved
6:0	R	0x0	AUDOUT FIFO depth counter.

AUDIN_MUTE_VAL 0x35

Bit(s)	R/W	Default	Description
31:0	RW	0x0	cntl_mute_val: Use this value during mute, if cntl_mute_mode=2.

AUDIN_FIFO0_PIO_STS 0xb0

Bit(s)	R/W	Default	Description
31	R	0x0	Fifo0 pio request.
30:0	R	0x0	Reserved

AUDIN_FIFO0_PIO_RDL 0xb1

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Fifo0 pio write data [31:0]

AUDIN_FIFO0_PIO_RDH 8'hb2 0xb2

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Fifo0 pio write data [63:32]

AUDIN_FIFO1_PIO_STS 0xb3

Bit(s)	R/W	Default	Description
31	R	0x0	Fifo1 pio request.
30:0	R	0x0	Reserved

AUDIN_FIFO1_PIO_RDL 0xb4

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Fifo1 pio write data [31:0]

AUDIN_FIFO1_PIO_RDH 0xb5

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Fifo1 pio write data [63:32]

AUDIN_FIF0O2_PIO_STS 0xb6

Bit(s)	R/W	Default	Description
31	R	0x0	Fifo2 pio request.
30:0	R	0x0	Reserved

AUDIN_FIFO2_PIO_RDL 0xb7

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Fifo2 pio write data [31:0]

AUDIN_FIFO2_PIO_RDH 0xb8

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Fifo2 pio write data [63:32]

AUDOUT_FIFO_PIO_STS 0xb9

Bit(s)	R/W	Default	Description
31	R	0x0	audout pio request.
30:7	R	0x0	Reserved
6:0	R	0x0	Audout fifo low level

AUDOUT_FIFO_PIO_WRL 0xba

Bit(s)	R/W	Default	Description
31:0	R	0x0	Audout fifo rdata [31:0]

AUDOUT_FIFO_PIO_WRH 0xbb

Bit(s)	R/W	Default	Description
31:0	R	0x0	Audout fifo rdata [63:32]

AUD_RESAMPLE_CTRL 0xbf

Bit(s)	R/W	Default	Description
31	RW	0x0	soft_reset: 1 = reset
30:29	RW	0x0	resample source select: 0: fifo0, 1:fifo1, 2:fifo2
28	RW	0x0	resample enable: 0 = disable, 1 = enable
27:26	RW	0x0	resample method select:2,3 reserved.
25:16	RW	0x0	outrdy generate count: equal mclk/lrclk*2
15:0	RW	0x0	average count initial value

AUD_RESAMPLE_CTRL1 0xc0

Bit(s)	R/W	Default	Description
31:0	RW	0x0	phase step

AUD_RESAMPLE_STATUS 0xc1

Bit(s)	R/W	Default	Description
21:0	RW	0x0	report the real frequency of input data

PDM Registers:

Final Address = 0xd0042000+offset*4

PDM_CTRL 0x40

Bit(s)	R/W	Default	Description
2	RW	0x0	CIC_DEC8OR16_SEL, 0:8, 0:16
1	RW	0x0	PDM_HPF_BYPASS
0	RW	0x0	PDM_ENABLE,1 enable

PDM_IN_CTRL 0x42

Bit(s)	R/W	Default	Description

18	RW	0x0	PDMIN_REV
17	RW	0x0	PDMCLK_REV
16	RW	0x0	GET_STA_EN
8	RW	0x0	SAMPLE_CNT

PDM_VOL_CTRL 0x43

Bit(s)	R/W	Default	Description
1	RW	0x0	PDML_INV
0	RW	0x0	PDMR_INV

PDM_VOL_GAIN_L 0x44

Bit(s)	R/W	Default	Description
25:0	RW	0x0	The left channel vol gain

PDM_VOL_GAIN_R 0x45

Bit(s)	R/W	Default	Description
25:0	RW	0x0	The right channel vol gain

PDM_STATUS 0x46

Bit(s)	R/W	Default	Description
31	R	0x0	Clk_cnt _overflow
30:24	R	0x0	Min_clk_cnt
23:16	R	0x0	Max_clk_cnt
15:8	R	0x0	Det_din_mincnt
7:0	R	0x0	Det_din_maxcnt

31. Audio Output

31.1 Overview

This part describe the audio output from the following aspect: SPIDF(encode) and I2S(encode), also all the registers related to audio path are listed in the end of this part.

31.2 SPDIF(encode)

The SPDIF(encode) module works in the following 4 steps:

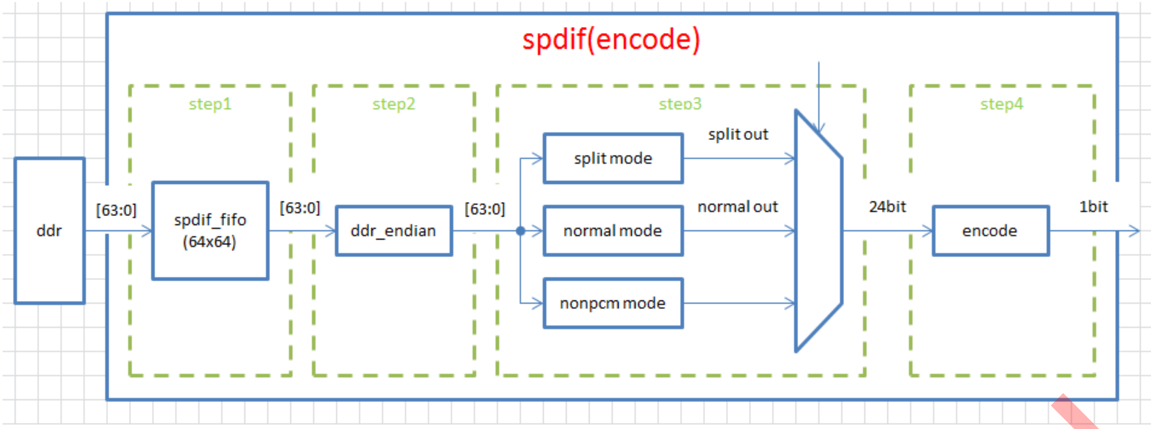
Step1: get the data from ddr.

Step2: write to fifo and make endian modification.

Step3: get the data from fifo by mode select.

Step4: encode.

Fig V.31.1 Diagram of spdif(encode)



SPDIF supports the following mode:

Table V.31.1 SPIDF Mode

	in ddr	
normal	2ch	16Bits**1
	8ch	16Bits**1
	2ch	32Bits**3
	8ch	32Bits**3
split	16Bits**1	
	24Bits**2	
	24Bits(32Bits) **3	
nonpcm	16Bits**4	

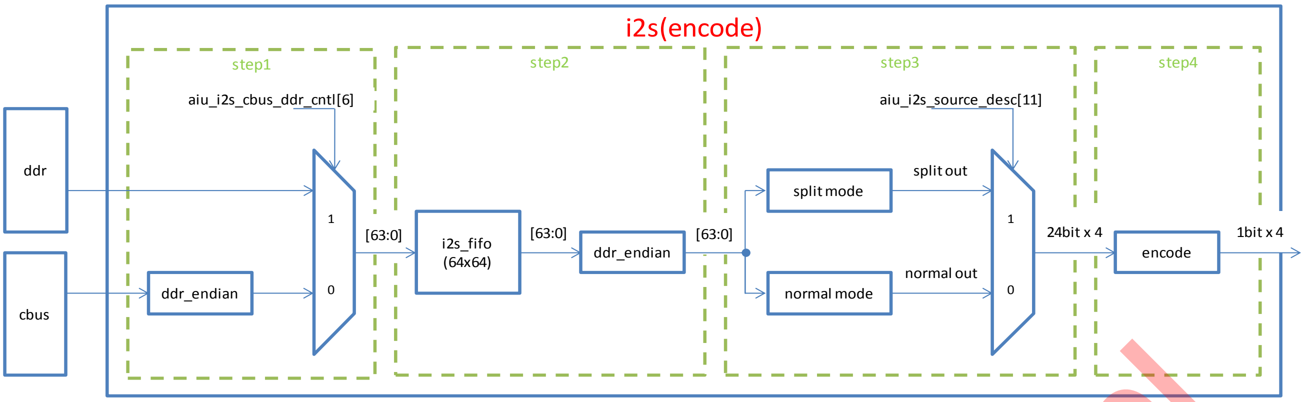
**1: In this mode, data in ddr is 16Bits.
**2: In this mode, data in ddr is 2x24Bits.
**3: In this mode, data in ddr is 32Bits.
**4: In this mode, data in ddr is 16Bits.
In normal mode, it support 2/8channel & 16Bits/24Bits/32Bits

31.3 I2S(encode)

The I2S(encode) module works in the following 4 steps:

Step1: get the data from ddr or cbus.
Step2: write to fifo and make endian modification.
Step3: get the data from fifo by mode select.
Step4: encode 4 streams.

Fig V.31.2 Diagram of I2S(encode)



Step3, I2S supports the following modes:

Table V.31.2 I2S Mode

	in ddr		output
normal	8ch	16Bits**1	4streams
	8ch	24Bits(32Bits)**2	4streams
split	2ch	16Bits**3	1stream
	8ch	16Bits**3	1stream
	8ch	24Bits(32Bits) **4	1stream
	8ch	24Bits(32Bits) **4	4stream

**1: In this mode, data in ddr is 16Bits,
**2: In this mode, data in ddr is 32Bits,
**3: In this mode, data in ddr is 16Bits,
**4: In this mode, data in ddr is 32Bits,
In normal mode, it support only 8channel & 4streams & 16Bits/24Bits.

The register aiu_mem_I2S_mask[15:0] can skip some read (by [15:8]) and output operation(by [7:0]).
For example:

if [15:8] = 8'b1111_1111, read ch0/ch1/ch2/ch3/ch4/ch5/ch6/ch7
if [15:8] = 8'b1110_1101, read ch0/ch2/ch3/ch5/ch6/ch7,ch1/ch4 skipped
if [7:0] = 8'b1111_1111, output ch0/ch1/ch2/ch3/ch4/ch5/ch6/ch7
if [7:0] = 8'b1110_1101, output ch0/mute/ch2/ch3/mute/ch5/ch6/ch7

In split mode, it will read data from ddr by linear sequence, and support 24Bits(1/4 streams) and 16Bits(1 stream) mode.

In split mode, there is no mask control, so aiu_mem_I2S_mask[15:0] must set 8'hffff_ffff.

I2S_encode_core can encode four I2S sample[23:0] to four 1 bitsignal at the same time.
The control includes:

hold, stop working until set to 1'b0.
underrun,
2'd0: send 0,
2'd1: send 0x800000,
2'd2: send last sample.
med_ctrl, if median work, out = (s1>(s0+s2)/2+th)?(s0+s2)/2:s1, that's mean if there are a burst noise sample, it will be replaced.
ch_swap: change the channel, assume input = L + R,
2'd0: output = L + R,

2'd1: output = L + L,
2'd2: output = R + R,
2'd3: output = R + L.

sel: use four mux4 to change the connect of in/out

sel0:

2'd0: out0 = in0,
2'd1: out0 = in1,
2'd2: out0 = in2,
2'd3: out0 = in3,

sel1:

2'd0: out1 = in0,
2'd1: out1 = in1,
2'd2: out1 = in2,
2'd3: out1 = in3,

sel2/sel3 are the same.

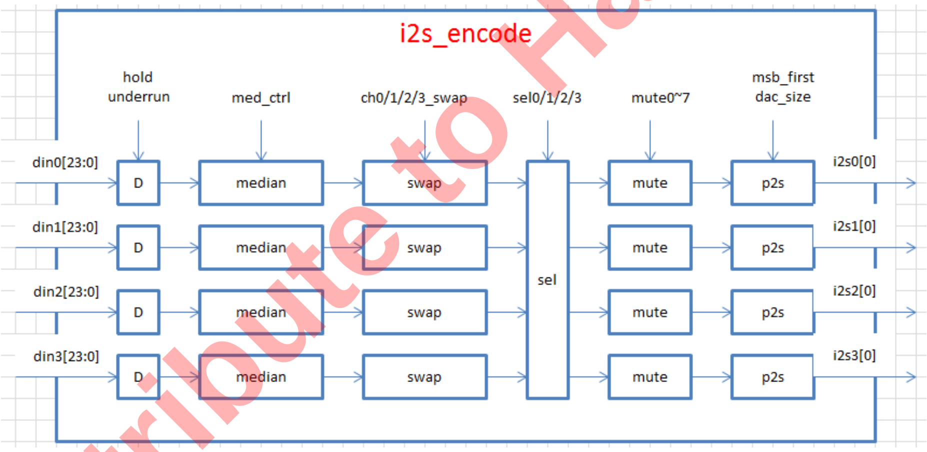
mute: [0] mute channel 0, [1] mute channel1, …[7] mute channel7

msb_first: 0:lsb first, 1: msb first.

dac_size:

2'd0: output 16Bits,
2'd1: output 20Bits,
2'd2/3: output 24Bits

Fig V.31.3 Diagram of I2S encode core



31.4 Register Description

The final addresses of the following registers should be calculated with the following equation:

Final address = 0xc1105400+offset*4

AIU_958_bpf 0x00

Bit(s)	R/W	Default	Description
15:0	RW	0x0	Bytes per frame in spdif.

AIU_958_brst 0x01

Bit(s)	R/W	Default	Description

15:0	RW	0x0	Burst info in spdif

AIU_958_length 0x02

Bit(s)	R/W	Default	Description
15:0	RW	0x0	The length of code in spdif

AIU_958_paddsize 0x03

Bit(s)	R/W	Default	Description
15:0	RW	0xc00	The padd size of spdif

AIU_958_misc 0x04

Bit(s)	R/W	Default	Description
15:14	RW	0x0	pcm_sample_ctl, 00-pcm_no_sample, 01-pcm_sample_up, 10-pcm_sample_down, 11-pcm_sample_down_drop
13	RW	0x0	if true, force each audio data to left or right according to the bit attached with the audio data.This bit should be used with Register AIU_958_force_left(0x505) together
12	RW	0x0	if true, the U(user data) is from the stream otherwise it is filled by zero while encoding iec958 frame
11	RW	0x0	if true big endian(highword,lowword) otherwise little endian(lowword,highword)for 32 bit mode
10:8	RW	0x0	shift number for 32 bit mode
7	RW	0x0	32 bit mode turn on while This bit is true and bit 1 is true
6:5	RW	0x0	Specifies output alignment for 16 bit pcm data. // 00 : dout = {8'b0, din}; // 01 : dout = {4'b0, din, 4'b0}; // 10 : dout = { din, 8'b0};
4	RW	0x0	True if data should be sent out MSB first. LSB first is the default in the spec.
3	RW	0x0	True if msb should be extended (only used with 16 bit pcm data.)
2	RW	0x0	True if msb of PCM data should be inverted.
1	RW	0x0	True if PCM data is 16 Bits wide. False if 24 bit or 32 bit mode.
0	RW	0x1	True if source data is non-PCM data. False if it is PCM data.

AIU_958_discard_num 0x06

Bit(s)	R/W	Default	Description
6:0	R	0x1	how many data discarded in the last dma after one frame data finish transfering to AIU. Should used together with register AIU_958_dcu_ff_ctrl, read only

AIU_958_dcu_ff_ctrl 0x07

Bit(s)	R/W	Default	Description
15:8	RW	0x0	A read from this register indicates the IEC958 FIFO count value
7	RW	0x0	ai_958_req_size if ture, set to 8 Bits interface, used to handle odd frame continous read
6	RW	0x0	continue seeking and dont discard the rest data in one dma after frame end
5	RW	0x0	if true, byte by byte seeking, otherwise word by word seeking
4	RW	0x0	if true, the function for sync head seeking is enabled
3:2	RW	0x0	IEC958 interrupt mode
1	RW	0x0	fifo auto disable, High means after one frame data put into the FIFO, the FIFO will automatically disabled
0	RW	0x0	fifo enable

AIU_958_chstat_l0 0x08

Bit(s)	R/W	Default	Description
31:0	R	0x0	channel status registers for Left channel

AIU_958_chstat_l1 0x09

Bit(s)	R/W	Default	Description
31:0	R	0x0	channel status registers for right channel

AIU_958_ctrl 0x0a

Bit(s)	R/W	Default	Description
9:8	RW	0x0	what to do if there is a fifo underrun 00 => insert 24'h000000 01 => insert mute constant as defined below 10 => repeat last l/r samples
7:5	RW	0x0	mute constant 000 => 24'h000000 001 => 24'h800000 010 => 24'h080000 011 => 24'h008000 100 => 24'h000001 101 => 24'h000010 110 => 24'h000100
4	RW	0x0	mute left speaker
3	RW	0x0	mute right speaker
2:1	RW	0x0	swap channels
0	RW	0x0	Set This bit to hold iec958 interface after the current subframe has been completely transmitted.

AIU_958_rpt 0x0b

Bit(s)	R/W	Default	Description
31:0	RW	0x0	A write operation to this register will cause one of the output samples to be repeated. This can be used to switch the left and the right channels.

AIU_I2S_mute_swap 0x0c

Bit(s)	R/W	Default	Description
15:8	RW	0x0	Mute 8 channel
7:6	RW	0x0	Ch6/7 swap sel.
5:4	RW	0x0	Ch4/5 swap sel.
3:2	RW	0x0	Ch2/3 swap sel.
1:0	RW	0x0	Ch0/1 swap sel.

AIU_I2S_source_desc 0x0d

Bit(s)	R/W	Default	Description
11	RW	0x0	Use_i2s_split
10	RW	0x0	Endian_32bit
9	RW	0x0	Mode_32bit
8:6	RW	0x0	Sft_bits
5	RW	0x0	Steam_16or24b
4:3	RW	0x0	Msb_position
2	RW	0x0	Msb_extend
1	RW	0x0	Msb_invert
0	RW	0x0	Num_streams:0:2ch;1:8ch;

AIU_I2S_med_ctrl 0x0e

Bit(s)	R/W	Default	Description

Bit(s)	R/W	Default	Description
1	RW	0x0	0=> data is offset binary 1=> data is signed
0	RW	0x0	enable median filter

AIU_I2S_med_thresh 0x0f

Bit(s)	R/W	Default	Description
15:0	RW	0x0	Median filter threshold constant

AIU_I2S_dac_cfg 0x10

Bit(s)	R/W	Default	Description
7	RW	0x0	sign extend sample before downshift
6:4	RW	0x0	payload downshift constant
3	RW	0x0	mute constant 0 => 'h0000000 1 => 'h800000
2	RW	0x0	send msb first
1:0	RW	0x0	Size of payload, 00 => 16 bit, alrclk = aoclk/32 01 => 20 bit, alrclk = aoclk/40 10 => 24 bit, alrclk = aoclk/48 11 => 24 bit, but alrclk = aoclk/64

AIU_I2S_misc 0x12

Bit(s)	R/W	Default	Description
4	RW	0x0	if true, force each audio data to left or right according to the bit attached with the audio data.This bit should be used with Register AIU_I2S_sync(0x511) together
3	RW	0x0	Same Audio source for IEC958 and I2S stream 0, both from I2S buffer
2	RW	0x0	Set This bit to put I2S interface in hold mode
1:0	RW	0x0	How to handle underruns // 00 => send zeros // 01 => send 'h800000 // 10 => repeat last samples

AIU_I2S_out_cfg 0x13

Bit(s)	R/W	Default	Description
7:0	RW	0x0	Audio output config. 2 Bits for each dac, 7:6 for dac3, 5:4 for dac2,3:2 for dac1, 1:0 for dac0 For each 2Bits: 00: connect channel0-1 to the dac 01: connect channel2-3 to the dac 10: connect channel4-5 to the dac 11: connect channel6-7 to the dac

AIU_rst_soft 0x15

Bit(s)	R/W	Default	Description
3	RW	0x0	reset slow domain iec958
2	RW	0x0	soft reset iec958 fast domain
1	RW	0x0	reset slow domain I2S
0	RW	0x0	soft reset I2S fast domain

AIU_clk_ctrl 0x16

Bit(s)	R/W	Default	Description
15	RW	0x0	enable_ddr_arb, set low to reset
14:13	RW	0x0	parser_A_addr_sel 00-A_addr_aififo2, 01-A_addr_iec958, 10-A_addr_aififo, 11-A_addr_I2S
12	RW	0x0	958 divisor more, if true, divided by 2, 4, 6, 8

Bit(s)	R/W	Default	Description
11	RW	0x0	amclk output divisor 0 => dont divide 1 => divide by 2
10	RW	0x0	clock source selection 0 => aiclk from pin 1 => ai_pll_clk from pll
9:8	RW	0x0	alrclk skew 00 => alrclk transitions at the same time msb is sent 01 => alrclk transitions on the cycle before msb is sent 10 => alrclk transitions on the cycle after msb is sent
7	RW	0x0	invert alrclk
6	RW	0x0	invert aoclk
5:4	RW	0x0	958 divisor 00 => divide by 1 01 => divide by 2 10 => divide by 3 11 => divide by 4
3:2	RW	0x0	I2S divisor. NOTE: this value is ignored if AIU_clk_ctrl_more[5:0] != 0 00 => divide by 1 01 => divide by 2 10 => divide by 4 11 => divide by 8
1	RW	0x0	enable 958 divider
0	RW	0x0	enable I2S divider

AIU_mix_adccfg 0x17

Bit(s)	R/W	Default	Description
12	RW	0x0	selects adc input
11:10	RW	0x0	adc size 00 => 16 Bits 01 => 18 Bits 10 => 20 Bits 11 => 24 Bits
9:8	RW	0x0	adc l/r swap mode 00 => stereo 01 => send the right adc input to both l and r speakers 10 => send the left adc input to both l and r speakers 11 => sum the left and right inputs and forward to both speakers
7:5	RW	0x0	adata/lrclk skew mode
4	RW	0x0	1=>invert the adc's lrclk (This is the lrclk going _out_of the chip.
3	RW	0x0	1=>Latch the data on the positive edge of the _internal_aoclk.
2	RW	0x0	1=>adc data is in signed 2's complement mode

AIU_mix_ctrl 0x18

Bit(s)	R/W	Default	Description
12	RW	0x0	if true, toggle each mixed audio data to left or right channel
11	RW	0x0	abuf din left selection, if true, select bit 24 of the data from abuf otherwise select bit 25 of the data from abuf
10:9	RW	0x0	mix sync select, when music, mic and abuf are mixed togather, the main sync source can be selected 00: not sync source 01: music data is the main sync source 10: abuf input data is the main sync source 11: music and abuf togather as the sync source
8	RW	0x0	0=> data from abuf is offset binary 1=> data from abuf is signed
7:6	RW	0x0	the source for data from aiu to abuf 00 => mic 01 => mic saled + abuf scaled 10 => mic scaled + abuf scaled + music scaled 11 => music

Bit(s)	R/W	Default	Description
5	RW	0x0	channel from aiu to abuf is on
4	RW	0x0	channel from abuf to aiu is on
3	RW	0x0	mic is on
2	RW	0x0	music is on
1	RW	0x0	if true the mixed data are outputed to I2S dac channel,otherwise the mixed data are outputed to IEC958 output
0	RW	0x0	if true music source for mixing is from I2S buffer, otherwise music source is from iec958 buffer

AIU_clk_ctrl_more 0x19

Bit(s)	R/W	Default	Description
15	RW	0x0	invert_audin_sclk
14	RW	0x0	enable_adc_sclk.
13:8	RW	0x0	divisor_adc_sclk.
7	RW	0x0	invert_acodec_adc_sclk
6	RW	0x0	Bit 6 hdmitx_sel_aoclkx2: 0=Select cts_clk_i958 as AIU clk to hdmi_tx_audio_master_clk; 1=Select cts_aoclkx2_int as AIU clk to hdmi_tx_audio_master_clk;
5:0	RW	0x0	More control on I2S divisor. For backward compatiblity, this value is ignored if is 0, if non-zero, it takes effect over AIU_clk_ctrl[3:2]. 0=I2S divisor will use the old value in AIU_clk_ctrl[3:2] (divide by 1/2/4/8) 1=divide by 2; 2=divide by 3; 3=divide by 4; ... and so on ... 63=divide by 64.

AIU_958_pop 0x1a

Bit(s)	R/W	Default	Description
15:0	RW	0x0	A read from this register pops 16 Bits of data off the 958 fifo. A write has no effect.

AIU_mix_gain 0x1b

Bit(s)	R/W	Default	Description
14:10	RW	0x0	mic gain
9:5	RW	0x0	abuf gain
4:0	RW	0x0	music gain

AIU_958_synword1 0x1c

Bit(s)	R/W	Default	Description
15:0	RW	0x0	sync head seeking, word1

AIU_958_synword2 0x1d

Bit(s)	R/W	Default	Description
15:0	RW	0x0	sync head seeking, word2

AIU_958_synword3 0x1e

Bit(s)	R/W	Default	Description
15:0	RW	0x0	sync head seeking, word3

AIU_958_synword1_mask 0x1f

Bit(s)	R/W	Default	Description
15:0	RW	0x0	sync head seeking, mask word1

AIU_958_synword2_mask 0x20

Bit(s)	R/W	Default	Description
15:0	RW	0x0	sync head seeking, mask word 2

AIU_958_synword3_mask 0x21

Bit(s)	R/W	Default	Description
15:0	RW	0x0	sync head seeking, mask word 3

AIU_958_ffrdout_thd 0x22

Bit(s)	R/W	Default	Description
15:0	RW	0x0	fifo read-out threshold, one condition to generate interrupt is met after fifo readout counter reach this value in a frame, please refer to register AIU_958_dcu_ff_ctrl

AIU_958_length_per_pause 0x23

Bit(s)	R/W	Default	Description
15:0	RW	0x0	For pause burst sequence adding, one pause burst sequence is consist of a serious pause burst.

AIU_958_pause_num 0x24

Bit(s)	R/W	Default	Description
15	RW	0x0	if true, one pause burst sequence will be added
14:0	RW	0x0	the number of pause burst in a pause burst sequence

AIU_958_pause_payload 0x25

Bit(s)	R/W	Default	Description
15:0	RW	0x0	When paused, use this payload .

AIU_958_auto_pause 0x26

Bit(s)	R/W	Default	Description
15	RW	0x0	if true, auto pause function enable
14	RW	0x0	pause pack option, just for debugging and adding one option
7:0	RW	0x0	auto_pause threshold

AIU_958_pause_pd_length 0x27

Bit(s)	R/W	Default	Description
15:0	RW	0x0	Pause pd length

AIU_CODEC_DAC_LRCLK_CTRL 0x28

Bit(s)	R/W	Default	Description
15:12		0x0	Reserved
11:0	RW	0x0	dac_lrclk_div

AIU_CODEC_ADC_LRCLK_CTRL 0x29

Bit(s)	R/W	Default	Description
15:14		0x0	Reserved
13	RW	0x0	inv_audin_lrclk: whether to invert lrclk before output to Audin
12	RW	0x0	inv_acodec_adc_lrclk: whether to invert lrclk before output to Audio Codec

11:0	RW	0x0	0 adc_lrclk_div

AIU_HDMI_CLK_DATA_CTRL 0x2a

Bit(s)	R/W	Default	Description
15:6		0x0	Reserved
5:4	RW	0x0	hdmi_data_sel: 00=output 0, disable hdmi data; 01=Select pcm data; 10=Select AIU I2S data; 11=Not allowed
3:2		0x0	Reserved
1:0	RW	0x0	hdmi_clk_sel: 00=Disable output hdmi clock; 01=Select pcm clock; 10=Select AIU clk; 11=Not allowed.

AIU_CODEC_CLK_DATA_CTRL 0x2b

Bit(s)	R/W	Default	Description
15:6		0x0	Reserved
5:4	RW	0x0	acodec_data_sel: 00=output 0, disable acodec_sdin; 01=Select pcm data; 10=Select AIU I2S data; 11=Not allowed.
3:2		0x0	Reserved
1:0	RW	0x0	acodec_clk_sel: 00=Disable output acodec_sclk; 01=Select pcm clock; 10=Select AIU aoclk; 11=Not allowed

AIU_958_chstat_r0 0x30

Bit(s)	R/W	Default	Description
15:0	RW	0x0	contains Bits 15:0 of the channel status word. Note that bit zero of the channel status word is sent out first.chstat_r1[15:0] contains Bits 31:16 of the channel status word

AIU_958_chstat_r1 0x31

Bit(s)	R/W	Default	Description
15:0	RW	0x0	contains Bits 15:0 of the channel status word. Note that bit zero of the channel status word is sent out first.chstat_r1[15:0] contains Bits 31:16 of the channel status word

AIU_958_valid_ctrl 0x32

Bit(s)	R/W	Default	Description
1	RW	0x0	if true, turn on Digital output Valid control
0	RW	0x0	0: output 0, 1: output 1 to the valid bit in audio digital output when bit 1 is true

AIU_AIFIFO2_CTRL 0x40

Bit(s)	R/W	Default	Description
3	RW	0x0	CRC pop aififo2 enable
2	RW	0x0	writing to This bit to 1 causes CRC module reset
1	RW	0x0	unused
1	RW	0x0	writing to This bit to 1 causes AIFIFO2 soft reset

AIU_AIFIFO2_STATUS 0x41

Bit(s)	R/W	Default	Description
4:0	R	0x0	how many Bits left in the first pop register

AIU_AIFIFO2_GBIT 0x42

Bit(s)	R/W	Default	Description
15:0	R	0x0	The gb data

AIU_AIFIFO2_CLB 0x43

Bit(s)	R/W	Default	Description

15:0	R	0x0	The gb data

AIU_CRC_CTRL 0x44

Bit(s)	R/W	Default	Description
13:8	RW	0x10	CRC polynomial equation order, between 1 to 32
3	RW	0x0	CRC pop data from FIFO enable
2	RW	0x0	CRC input register clear
1	RW	0x0	CRC core soft reset
0	RW	0x0	CRC caculation start

AIU_CRC_STATUS 0x45

Bit(s)	R/W	Default	Description
7:4	RW	0x0	CRC internal shift register bit select, just for debug purpose
3	RW	0x0	CRC internal shift register data valid, just for debug purpose
2	RW	0x0	CRC input register data valid
1	RW	0x0	CRC result, 1: CRC not correct, 0: CRC correct
0	RW	0x0	CRC state, 1: CRC busy, 0: CRC idle

AIU_CRC_SHIFT_REG 0x46

Bit(s)	R/W	Default	Description
15:0	R	0x0	CRC internal shift register, read only, for debug purpose

AIU_CRC_IREG 0x47

Bit(s)	R/W	Default	Description
15:0	RW	0x0	CRC data input register

AIU_CRC_CAL_REG1 0x48

Bit(s)	R/W	Default	Description
15:0	RW	0x0	CRC calculation register high-bit part [31:16]

AIU_CRC_CAL_REG0 0x49

Bit(s)	R/W	Default	Description
15:0	RW	0x0	CRC calculation register high-bit part [15:0]

CRC polynomial coefficient high-bit part [31:16], read/write

AIU_CRC_POLY_COEF1 0x4a

Bit(s)	R/W	Default	Description
15:0	RW	0x0	CRC calculation register high-bit part [15:0]

AIU_CRC_POLY_COEF0 0x4b

Bit(s)	R/W	Default	Description
15:0	RW	0x0	CRC polynomial coefficient low-bit part [15:0]

AIU_CRC_BIT_SIZE1 0x4c

Bit(s)	R/W	Default	Description
3:0	RW	0x0	CRC frame size, high-bit part [19:16]

AIU_CRC_BIT_SIZE0 0x4d

Bit(s)	R/W	Default	Description

15:0	RW	0x0	CRC frame size, low-bit part [15:0]

AIU_CRC_BIT_CNT1 0x4e

Bit(s)	R/W	Default	Description
3:0	R	0x0	How many Bits have been processed right now in the current frame [19:16]

AIU_CRC_BIT_CNT0 0x4f

Bit(s)	R/W	Default	Description
15:0	R	0x0	How many Bits have been processed right now in the current frame [15:0]

AIU_AMCLK_GATE_HI 0x50

Bit(s)	R/W	Default	Description
3	RW	0x0	Start msr clk
2:0	RW	0x0	The msr period [18:16]

AIU_AMCLK_GATE_LO 0x51

Bit(s)	R/W	Default	Description
15:0	RW	0x0	The msr period [15:0]

AIU_AMCLK_MSR 0x52

Bit(s)	R/W	Default	Description
15:0	R	0x0	The msr count

AIU_MEM_I2S_START_PTR 0x60

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The start address from DDR

AIU_MEM_I2S_RD_PTR 0x61

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The new read access address from DDR

AIU_MEM_I2S_END_PTR 0x62

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The end address from DDR

AIU_MEM_I2S_MASKS 0x63

Bit(s)	R/W	Default	Description
31:16	RW	0x0	IRQ block
15:8	RW	0x0	chan_mem_mask. Each Bit indicates which channels exist in memory
7:0	RW	0x0	chan_rd_mask. Each Bit indicates which channels are READ from memory

AIU_MEM_I2S_CONTROL 0x64

Bit(s)	R/W	Default	Description
11:10	RW	0x0	Select which hardware pointer to use to control the buffer level: 00 = parser 01 = audin_fifo0_wrpt 1x = audin_fifo1_wrpt
9	RW	0x0	Use level control: 1 = use buffer level control

Bit(s)	R/W	Default	Description
8	R	0x0	Read Only. This bit is 1 when there is data available for reading
7	R	0x0	Read only. This bit will be high when we're fetching data from the DDR memory.To reset this module, set cntl_enable = 0, and then wait for busy = 0.
6		0x0	cntl_mode_16bit:Set to 1 for 16 bit storage format in DDR
5:3	RW	0x0	endian
2	RW	0x0	cntl_empty_en Set to 1 to enable reading data from the FIFO
1	RW	0x0	cntl_fill_en Set to 1 to enable reading data from DDR memory
0	RW	0x0	cntl_init: After setting the read pointers, sizes, channel masks and read masks, set This bit to 1 and then to 0

AIU_MEM_IEC958_START_PTR 0x65

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The start address from DDR

AIU_MEM_IEC958_RD_PTR 0x66

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The read access address from DDR

AIU_MEM_IEC958_END_PTR 0x67

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The end address from DDR

AIU_MEM_IEC958_MASKS 0x68

Bit(s)	R/W	Default	Description
15:8	RW	0x0	chan_mem_mask. Each Bit indicates which channels exist in memory
7:0	RW	0x0	chan_rd_mask. Each Bit indicates which channels are READ from memory

AIU_MEM_IEC958_CONTROL 0x69

Bit(s)	R/W	Default	Description
31	RW	0x0	A_urgent
30	RW	0x0	ch_always_8
27:24	RW	0x0	rdata_rd_base_begin (used for select from different channel)
23:14		0x0	reserved
13	RW	0x0	cntl_sim_en
12	RW	0x0	cntl_use_level
11	R	0x0	Read only. This bit will be set to 1 when there is data in the FIFO to process
10	R	0x0	Read only. This bit will be high when we're fetching data from the DDR memory
9	RW	0x0	cntl_endian_jic Just in case endian. last minute byte swap of the data out of the FIFO to the rest of the IEC958 logic
8	RW	0x0	Set This bit to 1 to tell the IEC958 FIFO to read and process data linearly for raw data.
7	RW	0x0	cntl_mode_16bit:Set to 1 for 16 bit storage format in DDR. Only valid when mode_raw = 0
6	RW	0x0	cntl_rd_ddr Set This bit to read if you want AIU_MEM_IEC958_RD_PTR and AIU_MEM_IEC958_RD_PTR_HIGH to refer to the pointer into DDR memory.Otherwise, the curr_ptr,registers refer to the byte address of the data at the output of the FIFO to the rest of the IEC958 logic
5:3	RW	0x0	endian
2	RW	0x0	cntl_empty_en Set to 1 to enable reading the DDR memory FIFO and filling the pipeline to get-bit Set cntl_empty_en = cntl_fill_en = 0 when pulsing cntl_init
1	RW	0x0	cntl_fill_en Set to 1 to enable reading data from DDR memory

Bit(s)	R/W	Default	Description
0	RW	0x0	cntl_init

AIU_MEM_AIFIFO2_START_PTR 0x6a

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The start address from DDR

AIU_MEM_AIFIFO2_CURR_PTR 0x6b

Bit(s)	R/W	Default	Description
31:0	R	0x0	The current address from DDR

AIU_MEM_AIFIFO2_END_PTR 0x6c

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The end address from DDR

AIU_MEM_AIFIFO2_BYTES_AVAIL 0x6d

Bit(s)	R/W	Default	Description
31:0	R	0x0	Available bytes in afifo2.

AIU_MEM_AIFIFO2_CONTROL 0x6e

Bit(s)	R/W	Default	Description
15:11		0x0	unused
10	RW	0x0	use_level Set This bit to 1 to enable filling of the FIFO controlled by the buffer level control. If This bit is 0, then use Bit[1] to control the enabling of filling
9	RW	0x0	Data Ready. This bit is set when data can be popped
8	RW	0x0	fill busy This bit will be high when we're fetching data from the DDR memory.To reset this module, set cntl_enable = 0, and then wait for busy = 0.
7	RW	0x0	cntl_endian_jic Just in case endian. last minute byte swap of the data out of the FIFO to get bit
6		0x0	unused
5：3	RW	0x0	endian
2	RW	0x0	cntl_empty_en Set to 1 to enable reading the DDR memory FIFO and filling the pipeline to get-bit Set cntl_empty_en = cntl_fill_en = 0 when pulsing cntl_init
1	RW	0x0	cntl_fill_en Set to 1 to enable reading data from DDR memory
0	RW	0x0	cntl_init: After setting the read pointers, sizes, channel masks and read masks, set This bit to 1 and then to 0

AIU_MEM_AIFIFO2_MAN_WP 0x6f

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual write ptr.

AIU_MEM_AIFIFO2_MAN_RP 0x70

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual read ptr.

AIU_MEM_AIFIFO2_LEVEL 0x71

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Level = reg[31:0] – level_hold

AIU_MEM_AIFIFO2_BUF_CNTL 0x72

Bit(s)	R/W	Default	Description

1	RW	0x0	Set to 1 for manual write pointer mode
0	RW	0x0	Set high then low after everything has been initialized

AIU_MEM_I2S_MAN_WP 0x73

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual write ptr.

AIU_MEM_I2S_MAN_RP 0x74

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual read ptr.

AIU_MEM_I2S_LEVEL 0x75

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Level = reg[31:0] – level_hold

AIU_MEM_I2S_BUF_CNTL 0x76

Bit(s)	R/W	Default	Description
1	RW	0x0	mode 0 = parser (or audin_fifo0 or audin_fifo1), 1 for manual write pointer
0	RW	0x0	initialize Set high then low after everything has been initialized

AIU_MEM_I2S_BUF_WRAP_COUNT 0x77

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The wrap count

AIU_MEM_I2S_MEM_CTL 0x78

Bit(s)	R/W	Default	Description
29:24	RW	0x0	A_brst_num
21:16	RW	0x0	A_id
15:0	RW	0x0	level_hold

AIU_MEM_IEC958_MEM_CTL 0x79

Bit(s)	R/W	Default	Description
29:24	RW	0x0	A_brst_num
21:16	RW	0x0	A_id
15:0	RW	0x0	level_hold

AIU_MEM_IEC958_WRAP_COUNT 0x7a

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The wrap count

AIU_MEM_IEC958_IRQ_LEVEL 0x7b

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The irq level

AIU_MEM_IEC958_MAN_WP 0x7c

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual write ptr.

AIU_MEM_IEC958_MAN_RP 0x7d

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual read ptr.

AIU_MEM_IEC958_LEVEL 0x7e

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Level = reg[31:0] – level_hold

AIU_MEM_IEC958_BUF_CNTL 0x7f

Bit(s)	R/W	Default	Description
29:24	RW	0x0	A_brst_num
21:16	RW	0x0	A_id
15:0	RW	0x0	level_hold

AIU_AIFIFO_CTRL 0x80

Bit(s)	R/W	Default	Description
3	RW	0x0	CRC pop aififo enable
2	RW	0x0	writing to This bit to 1 causes CRC module reset
1	RW	0x0	enable aififo
0	RW	0x0	writing to This bit to 1 causes aififo soft reset

AIFIFO_STATUS 0x81

Same fucntion as the AIGBIT of AIFIFO in CDROM module write to this register how many Bits wanna pop, and reading this register gets the corresponding Bits data

Bit(s)	R/W	Default	Description
13	RW	0x0	aififo request to dcu status
12	RW	0x0	dcu select status
11:5	RW	0x0	aififo word counter number
4:0	RW	0x0	how many Bits left in the first pop register

AIFIFO_GBIT 0x82

Same function as the AICLB of AIFIFO in CDROM module return the leading zeros by reading this registers

Bit(s)	R/W	Default	Description
15:0	R	0x0	The gb data

AIFIFO_CLB 0x83

Bit(s)	R/W	Default	Description
15:0	R	0x0	The gb data

MEM_AIFIFO_START_PTR 0x84

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The start address from DDR

MEM_AIFIFO_CURR_PTR 0x85

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The current address from DDR

MEM_AIFIFO_END_PTR 0X86

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The start address from DDR

MEM_AIFIFO_BYTES_AVAIL 0x87

Bit(s)	R/W	Default	Description
31:0	RW	0x0	The available bytes.

AIU_MEM_AIFIFO_CONTROL 0x88

Bit(s)	R/W	Default	Description
15:11		0x0	unused
10	RW	0x0	use_level Set This bit to 1 to enable filling of the FIFO controlled by the buffer level control. If This bit is 0, then use Bit[1] to control the enabling of filling
9	RW	0x0	Data Ready. This bit is set when data can be popped
8	RW	0x0	fill busy This bit will be high when we're fetching data from the DDR memory
7	RW	0x0	cntl_endian_jic Just in case endian. last minute byte swap of the data out of the FIFO to get bit
6	RW	0x0	unused
5：3	RW	0x0	endian
2	RW	0x0	cntl_empty_en Set to 1 to enable reading the DDR memory FIFO and filling the pipeline to get-bit
1	RW	0x0	cntl_fill_en Set to 1 to enable reading data from DDR memory
0	RW	0x0	cntl_init

AIU_MEM_AIFIFO_MAN_WP 0x89

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual write ptr.

AIU_MEM_AIFIFO_MAN_RP 0x8a

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Manual read ptr.

AIU_MEM_AIFIFO_LEVEL 0x8b

Bit(s)	R/W	Default	Description
31:0	RW	0x0	Level = reg[31:0] – level_hold

AIU_MEM_AIFIFO_BUF_CNTL 0x8c

Bit(s)	R/W	Default	Description
1	RW	0x0	manual mode Set to 1 for manual write pointer mode
0	RW	0x0	Init Set high then low after everything has been initialized

AIU_MEM_AIFIFO_BUF_WRAP_COUNT 0x8d

Bit(s)	R/W	Default	Description
31:0	R	0x0	Fifo wrap count

AIU_MEM_AIFIFO2_BUF_WRAP_COUNT 0x8e

Bit(s)	R/W	Default	Description
31:0	R	0x0	Fifo2 wrap count

AIU_MEM_AIFIFO_MEM_CTL ox8f

Bit(s)	R/W	Default	Description
29:24	RW	0x0	A_brst_num
21:16	RW	0x0	A_id
15:0	RW	0x0	level_hold

AIFIFO_TIME_STAMP_CNTL 0x90

Bit(s)	R/W	Default	Description
31:16	RW	0x0	drop_bytes
15:14	RW	0x0	drop_status (Read-Only)
13:12	RW	0x0	sync_match_position (Read-Only)
11:6		0x0	reserved
5:4	RW	0x0	TIME_STAMP_NUMBER, 0-32Bits, 1-64Bits, 2-96Bits, 3-128Bits
3	RW	0x0	stamp_soft_reset
2	RW	0x0	TIME_STAMP_length_enable
1	RW	0x0	TIME_STAMP_sync64_enable
0	RW	0x0	TIME_STAMP_enable

AIFIFO_TIME_STAMP_SYNC_0 0x91

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_SYNC_CODE_0

AIFIFO_TIME_STAMP_SYNC_1 0x92

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_SYNC_CODE_1

AIFIFO_TIME_STAMP_0 0x93

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_0

AIFIFO_TIME_STAMP_1 0x94

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_1

AIFIFO_TIME_STAMP_2 0x95

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_2

AIFIFO_TIME_STAMP_3 0x96

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_3

AIFIFO_TIME_STAMP_LENGTH 0x97

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_LENGTH

AIFIFO2_TIME_STAMP_CNTL 0x98

Bit(s)	R/W	Default	Description
31：16	RW	0x0	drop_bytes
15：14	RW	0x0	drop_status (Read-Only)
13：12	RW	0x0	sync_match_position (Read-Only)
11：6		0x0	reserved
5：4	RW	0x0	TIME_STAMP_NUMBER, 0-32Bits, 1-64Bits, 2-96Bits, 3-128Bits
3	RW	0x0	stamp_soft_reset
2	RW	0x0	TIME_STAMP_length_enable
1	RW	0x0	TIME_STAMP_sync64_enable
0	RW	0x0	TIME_STAMP_enable

AIFIFO2_TIME_STAMP_SYNC_0 0x99

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_SYNC_CODE_0

AIFIFO2_TIME_STAMP_SYNC_1 0x9a

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_SYNC_CODE_1

AIFIFO2_TIME_STAMP_0 0x9b

Bit(s)	R/W	Default	Description
31：0	RW	0x0	TIME_STAMP_0

AIFIFO2_TIME_STAMP_1 0x9c

Bit(s)	R/W	Default	Description
31：0	RW	0x0	TIME_STAMP_1

AIFIFO2_TIME_STAMP_2 0x9d

Bit(s)	R/W	Default	Description
31：0	RW	0x0	TIME_STAMP_2

AIFIFO2_TIME_STAMP_3 0x9e

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_3

AIFIFO2_TIME_STAMP_LENGTH 0x9f

Bit(s)	R/W	Default	Description
31：0	RW	0x0	TIME_STAMP_LENGTH

IEC958_TIME_STAMP_CNTL 0xa0

Bit(s)	R/W	Default	Description
31：16	RW	0x0	drop_bytes
15：14	RW	0x0	drop_status (Read-Only)
13：12	RW	0x0	sync_match_position (Read-Only)
11：6		0x0	reserved
5：4	RW	0x0	TIME_STAMP_NUMBER, 0-32Bits, 1-64Bits, 2-96Bits, 3-128Bits
3	RW	0x0	stamp_soft_reset
2	RW	0x0	TIME_STAMP_length_enable

1	RW	0x0	TIME_STAMP_sync64_enable
0	RW	0x0	TIME_STAMP_enable

IEC958_TIME_STAMP_SYNC_0 0xa1

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_SYNC_CODE_0

IEC958_TIME_STAMP_SYNC_1 0xa2

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_SYNC_CODE_1

IEC958_TIME_STAMP_0 0xa3

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_0

IEC958_TIME_STAMP_1 0xa4

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_1

IEC958_TIME_STAMP_2 0xa5

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_2

IEC958_TIME_STAMP_3 0xa6

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_3

IEC958_TIME_STAMP_LENGTH 0xa7

Bit(s)	R/W	Default	Description
31:0	RW	0x0	TIME_STAMP_LENGTH

AIU_MEM_AIFIFO2_MEM_CTL 0xa8

Bit(s)	R/W	Default	Description
29:24	RW	0x0	A_brst_num
21:16	RW	0x0	A_id
15:0	RW	0x0	level_hold

AIU_I2S_CBUS_DDR_CNTL 0xa9

Bit(s)	R/W	Default	Description
31:26		0x0	unused
25	RW	0x0	A_req level
24	RW	0x0	data_req If This bit is 1, then (a_req_cnt != 'h0)
23：16	RW	0x0	a_req_cnt This value corresponds to the number of32-bit words
15:7		0x0	unused
6	RW	0x0	Set This bit to mux in the cbus_ddr_interface
5	RW	0x0	Set This bit to allow back to back A_req's to be serviced
4	RW	0x0	Set This bit to generate an IRQ on the first A_req
3：1	RW	0x0	Endian
0	RW	0x0	Set This bit enable the cbus_ddr_interface

AIU_I2S_CBUS_DDR_WDATA 0xaa

Bit(s)	R/W	Default	Description
31:0	RW	0x0	32-bit data to write to the cbus_ddr interface

AIU_I2S_CBUS_DDR_ADDR 0xab

Bit(s)	R/W	Default	Description
31:0	RW	0x0	First address associated with the first request by the I2S_fast() to read DDR data

Section VI Memory INTERFACE

This part describes S905's memory interfaces from the following aspects:

- DDR
- NAND
- EMMC/SDIO/SD
- SPICC
- SPIFC

32. DDR

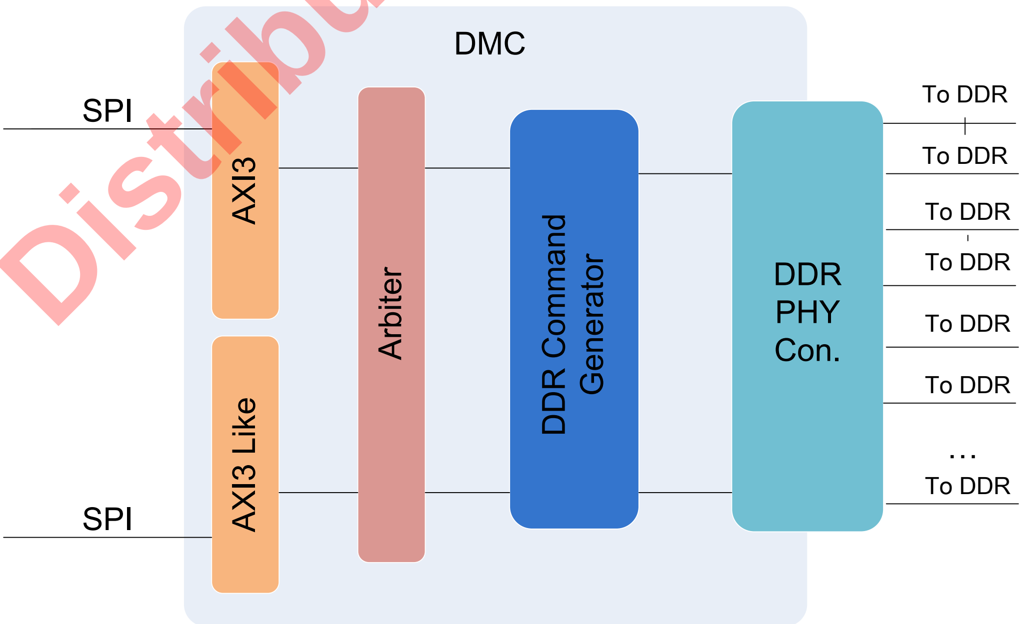
32.1 Overview

DDR memory interface consists of the 2 parts: DDR memory controller (DMC) and DDR PHY controller. The main features of this module are listed below:

- Electronic fence protected Security system.
- Optimized DDR read reordering to improve DDR efficiency.
- Dual channel 16Bits shared AC mode and signal channel 32Bits mode to support more DDR size combination.
- VPU ports changed to AXI like 128Bits interface. READ/write bus are separated.
- Dedicated GE2D port for maximum 2D graphic bandwidth.
- Device port directly to AXI arbitration.. No canvas address translation latency.
- PCTL moved inside DMC to optimize DDR command generation.
- Improved DDR Frequency update 933Mhz(DDR3/LPDDR3 1866MBPS).

Below is the diagram of DDR modul, in which SPI is the Serial Peripherial Interface for transport, AXI3 and AXI3-like are the interface (ports) between DMC and SPI, signals will go through the Arbiter to the DDR Commend Generator to generate DDR commend signal, and through DDR Phy Controler to execute read or write to DDR.

Fig VI.31.1 Diagram of DDR Interface



32.2 Register Description

DMC Register spec.

DMC unsecure register. Base address 0xc8838000. Each register takes 4 byte address.

Each register's final address = 0xc8838000 + offset * 4.

DMC_REQ_CTRL **0x0**

Bit(s)	R/W	Default	Description
31~16	R/W	0	Not used.
15	R/W	0	enable dmc request of port15. GE2D interface. Async interface.
14	R/W	0	enable dmc request of port 14. DOS HCODEC interface Sync interface.
13	R/W	0	enable dmc request of port 13. DOS VDEC interface Sync interface..
12	R/W	0	enable dmc request of port 12. VPU write interface 1 Sync interface.
11	R/W	0	enable dmc request of port 11. VPU write interface 0 Sync interface.
10	R/W	0	enable dmc request of port 10. VPU read interface 2. Sync interface.
9	R/W	0	enable dmc request of port 9. VPU read interface 1. Sync interface
8	R/W	0	enable dmc request of port 8. VPU read interface 0. Sync interface.
7	R/W	0	enable dmc request of port 7. DEVICE. Async interface.
6	R/W	0	enable dmc request of port 6. not used.
5	R/W	0	enable dmc request of port 5. not used.
4	R/W	0	enable dmc request of port 4. HEVC sync interface.
3	R/W	0	enable dmc request of port 3. HDCP/HDMI 32Bits. Async interface..
2	R/W	0	enable dmc request of port 2. Mali 1 Sync interface..
1	R/W	0	enable dmc request of port 1. Mali 0. Sync interface.
0	R/W	0	enable dmc request of port 0. CPU/A53 Sync interface.

DMC_SOFT_RST **0x01**

Bit(s)	R/W	Default	Description
31~29	R/W	0	Not used.
28	R/W	0	DMC low power control moudle soft reset_n. 0 : reset. 1 : normal working mode.
27	R/W	0	DMC QOS monitor module soft reset_n. 0 : reset. 1 : normal working mode.
26	R/W	0	DMC register modle soft reset_n. 0 : reset. 1 : normal working mode.
25	R/W	0	DMC canvas transfer module soft reset_n. 0 : reset. 1 : normal working mode..
24	R/W	0	DMC command buffers and command generation modules soft reset. 0 = reset. 1:
23~20	R/W	0	Not used.
19	R/W	0	DDR channel 1 PCTL module PCLK domain soft reset_n. 0 : reset. 1 : normal working mode.
18	R/W	0	DDR channel 1 PCTL module n_clk domain soft reset_n. 0 : reset. 1 : normal working mode.
17	R/W	0	DDR channel 0 PCTL module PCLK domain soft reset_n. 0 : reset. 1 : normal working mode.
16	R/W	0	DDR channel 0 PCTL module n_clk domain soft reset_n. 0 : reset. 1 : normal working mode.
15:0	R/W	0	16 input chan inteface n_clk domain reset control. if the channel is asynchronous FIFO interface, then both side of the clocks must be turn off before reset this module. If the channel is synchronous interface, you can reset it any time.
15	R/W	0	n_clk domain port 15 soft reset_n control. 0 : reset. 1: normal working mode.
14	R/W	0	n_clk domain port 14 soft reset_n control. 0 : reset. 1: normal working mode.
13	R/W	0	n_clk domain port 13 soft reset_n control. 0 : reset. 1: normal working mode.
12	R/W	0	n_clk domain port 12 soft reset_n control. 0 : reset. 1: normal working mode.
11	R/W	0	n_clk domain port 11 soft reset_n control. 0 : reset. 1: normal working mode.
10	R/W	0	n_clk domain port 10 soft reset_n control. 0 : reset. 1: normal working mode.
9	R/W	0	n_clk domain port 9 soft reset_n control. 0 : reset. 1: normal working mode.

Bit(s)	R/W	Default	Description
8	R/W	0	n_clk domain port 8 soft reset_n control. 0 : reset. 1: normal working mode.
7	R/W	0	n_clk domain port 7 soft reset_n control. 0 : reset. 1: normal working mode.
6	R/W	0	n_clk domain port 6 soft reset_n control. 0 : reset. 1: normal working mode.
5	R/W	0	n_clk domain port 5 soft reset_n control. 0 : reset. 1: normal working mode.
4	R/W	0	n_clk domain port 4 soft reset_n control. 0 : reset. 1: normal working mode.
3	R/W	0	n_clk domain port 3 soft reset_n control. 0 : reset. 1: normal working mode.
2	R/W	0	n_clk domain port 2 soft reset_n control. 0 : reset. 1: normal working mode.
1	R/W	0	n_clk domain port 1 soft reset_n control. 0 : reset. 1: normal working mode.
0	R/W	0	n_clk domain port 0 soft reset_n control. 0 : reset. 1: normal working mode.

DMC_SOFT_RST1 **0x02**

Bit(s)	R/W	Default	Description
31~16	R/W	0	Not used.
15~0	R/W	0	if the input port interface is asynchronous interface, then the related bit is for the main clock domain reset control. if the interface is synchronouse interface, This bit is not used.
14~8	R/W	0	Not used
7	R/W	0	input port 7 main clock domain soft reset_n.
6~4	R/W	0	Not used
3	R/W	0	input chan 3 main clock domain soft reset_n.
2~-	R/W	0	Not used

DMC_SOFT_STS1 **0x04**

Bit(s)	R/W	Default	Description
31~16	R/W	0	Not used.
15~0	R/W	0	Read only. the DMC_SOFT_RST1 signal in n_clk domain. the purpose of this register is if the n_clk is too fast or too slow related to APB clock, we can read this register to make sure another clock domain reset is done.

DMC_VERSION **0x05**

Bit(s)	R/W	Default	Description
31~0	R	0x000a001	Read only.

DMC_RAM_PD **0x11**

Bit(s)	R/W	Default	Description
31~6	R/W	0	Not used.
5:4	R/W	0	DDR channel1 read/write data path SRAM in power down mode. 2'b11: power down. 2'b00 working mode.
3:2	R/W	0	DDR channel0 read/write data path SRAM in power down mode. 2'b11: power down. 2'b00 working mode
1:0	R/W	0	CANVAS LUT SRAM in power down mode control. 2'b11: power down. 2'b00 working mode.

DMC_CAV_LUT_DATAL **0x12**

Bit(s)	R/W	Default	Description
31~0	R/W	0	low 32 Bits of canvas data which need to be configured to canvas LUT memory

DMC_CAV_LUT_DATAH **0x13**

Bit(s)	R/W	Default	Description

31~0	R/W	0	//high 32Bits of cavnas data which need to be configured to canvas memory.
			//64Bits CANVAS look up table
			//bit 61:58 Endian control.
			//bit 61: 1 : switch 2 64Bits data inside 128Bits boundary. 0 : no change.
			//bit 60: 1 : switch 2 32Bits data inside 64Bits data boundary. 0 : no change.
			//bit 59: 1 : switch 2 16Bits data inside 32Bits data boundary. 0 : no change.
			//bit 58: 1 : switch 2 8Bits data inside 16Bits data bournday. 0 : no change.
			//bit 57:56. Canvas block mode. 2 : 64x32, 1: 32x32; 0 : linear mode.
			//bit 55: canvas Y direction wrap control. 1: wrap back in y. 0: not wrap back.
			//bit 54: canvas X direction wrap control. 1: wrap back in X. 0: not wrap back.
			//bit 53:41. canvas Hight.
			//bit 40:29. canvas Width, unit: 8bytes. must in 32bytes boundary. that means last 2 Bits must be 0.
			//bit 28:0. cavnas start address. unit. 8 bytes. must be in 32bytes boundary. that means last 2Bits must be 0.

DC_CAV_LUT_ADDR **0x14**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~8	R/W	0	write 2'b10. it would trigger a canvas write operation. the data saved in DC_CAV_LUT_DATAL and DC_CAV_LUT_DATAH will be written to LUT table, the LUT table index is the bit 7:0 of this regsiter. write 2'b01, it would trigger a read operation. after the read finished, the LUT table value in index[7:0] would read back to DC_CAV_LUT_RDATAL and DC_CAV_LUT_RDATAH register.
7~0	R/W	0	256 canvas look up table index address

DC_CAV_LUT_RDATAL **0x15**

Bit(s)	R/W	Default	Description
31~0	R/W	0	CBUS low 32 Bits canvas read back data from LUT.

DC_CAV_LUT_RDATAH **0x16**

Bit(s)	R/W	Default	Description
31~0	R/W	0	CBUS high 32 Bits canvas read back data from LUT.

DMC_2ARB_CTRL **0x20**

Bit(s)	R/W	Default	Description
31~12	R/W	0	Not used
11:6	R/W	0	the final arbitration. weight for all AXI bus(ports 0~7).
5:0	R/W	0	the final arbitration. weight for all AMbus(ports 8~15).

DMC_REFR_CTRL1 **0x23**

Bit(s)	R/W	Default	Description
31~28	R/W	0	Not used

Bit(s)	R/W	Default	Description
26~24	R/W	0	theres 4 depath FIFO to same the REFR request. use this regsiter to set when FIFO level to set the refresh command to be highest priority.
23:8	R/W	0	Not used.
7	R/W	0	dmc to control auto_refresh enable
6~4	R/W	0	refresh number per refresh cycle.
3	R/W	0	pvt enable
2	R/W	0	zqc enable
1	R/W	0	ddr1 auto refresh enable.
0	R/W	0	ddr0 auto refresh enable.

DMC_REFR_CTRL2 **0x24**

Bit(s)	R/W	Default	Description
31~24	R/W	0	tZQCI
23~16	R/W	0	tPVTI
15:8	R/W	0	tREFI
7:0	R/W	0	t100ns

DMC_MON_CTRL2 **0x26**

Bit(s)	R/W	Default	Description
31	R/W	0	qos_mon_en. write 1 to trigger the enable. polling This bit 0, means finished. or use interrupt to check finish.
30	R/W	0	qos_mon interrupt clear. clear the qos monitor result. read 1 = qos mon finish interrupt.
29~21	R/W	0	Not used.
20	R/W	0	qos_mon_trig_sel. 1 = vsync. 0 = timer.
19~16	R/W	0	qos monitor port select. select one at one time only.
15:0	R/W	0	16 SubID ID[9:6] selections for selected port.

DMC_MON_CTRL2 **0x27**

Bit(s)	R/W	Default	Description
31~0	R/W	0	qos_mon_clk_timer. How long to measure the bandwidth.

DMC_MON_ALL_REQ_CNT **0x28**

Bit(s)	R/W	Default	Description
31~0	R	0	at the test period, the whole MMC request high time.

DMC_MON_ALL_GRANT _CNT **0x29**

Bit(s)	R/W	Default	Description
31~0	R	0	at the test period, the whole MMC data grant cycles.

DMC_MON_ONE _GRANT _CNT **0x2a**

Bit(s)	R/W	Default	Description
31~0	read	0	at the test period, the granted data cycles for the selected port and subIDs.

DMC_CLKG_CTRL0 **0x30**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.

Bit(s)	R/W	Default	Description
29	R/W	0	enable auto clock gating for write rsp generation.
28	R/W	0	enable auto clock gating for read rsp generation.
27	R/W	0	enable auto clock gating for ddr1 read back data buffer.
26	R/W	0	enable auto clock gating for ddr0 read back data buffer.
25	R/W	0	enable auto clock gating for ddr1 command filter.
24	R/W	0	enable auto clock gating for ddr0 command filter.
23	R/W	0	enable auto clock gating for ddr1 write reorder buffer.
22	R/W	0	enable auto clock gating for ddr0 write reorder buffer.
21	R/W	0	enable auto clock gating for ddr1 write data buffer.
20	R/W	0	enable auto clock gating for ddr0 write data buffer.
19	R/W	0	enable auto clock gating for ddr1 read reorder buffer.
18	R/W	0	enable auto clock gating for ddr0 read reorder buffer.
17	R/W	0	enable auto clock gating for read canvas.
16	R/W	0	enable auto clock gating for write canvas.
15	R/W	0	enable auto clock gating for port 15.
14	R/W	0	enable auto clock gating for port 14
13	R/W	0	enable auto clock gating for port 13.
12	R/W	0	enable auto clock gating for port 12.
11	R/W	0	enable auto clock gating for port 11.
10	R/W	0	enable auto clock gating for port 10.
9	R/W	0	enable auto clock gating for port 9.
8	R/W	0	enable auto clock gating for port 8.
7	R/W	0	enable auto clock gating for port 7.
6	R/W	0	enable auto clock gating for port 6.
5	R/W	0	enable auto clock gating for port 5.
4	R/W	0	enable auto clock gating for port 4.
3	R/W	0	enable auto clock gating for port 3.
2	R/W	0	enable auto clock gating for port 2.
1	R/W	0	enable auto clock gating for port 1.
0	R/W	0	enable auto clock gating for port 0.

DMC_CLKG_CTRL1 0x31

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29	R/W	0	Force to disable the clock of for write rsp generation.
28	R/W	0	Force to disable the clock of read rsp generation.
27	R/W	0	Force to disable the clock of ddr1 read back data buffer.
26	R/W	0	Force to disable the clock of ddr0 read back data buffer.
25	R/W	0	Force to disable the clock of ddr1 command filter.
24	R/W	0	Force to disable the clock of ddr0 command filter.
23	R/W	0	Force to disable the clock of ddr1 write reorder buffer.
22	R/W	0	Force to disable the clock of ddr0 write reorder buffer.
21	R/W	0	Force to disable the clock of ddr1 write data buffer.
20	R/W	0	Force to disable the clock of ddr0 write data buffer.
19	R/W	0	Force to disable the clock of ddr1 read reorder buffer.

Bit(s)	R/W	Default	Description
18	R/W	0	Force to disable the clock of ddr0 read reorder buffer.
17	R/W	0	Force to disable the clock of read canvas.
16	R/W	0	Force to disable the clock of write canvas.
15	R/W	0	Force to disable the clock of port 15.
14	R/W	0	Force to disable the clock of port 14
13	R/W	0	Force to disable the clock of port 13.
12	R/W	0	Force to disable the clock of port 12.
11	R/W	0	Force to disable the clock of port 11.
10	R/W	0	Force to disable the clock of port 10.
9	R/W	0	Force to disable the clock of port 9.
8	R/W	0	Force to disable the clock of port 8.
7	R/W	0	Force to disable the clock of port 7.
6	R/W	0	Force to disable the clock of port 6.
5	R/W	0	Force to disable the clock of port 5.
4	R/W	0	Force to disable the clock of port 4.
3	R/W	0	Force to disable the clock of port 3.
2	R/W	0	Force to disable the clock of port 2.
1	R/W	0	Force to disable the clock of port 1.
0	R/W	0	Force to disable the clock of port 0.

DMC_CHAN_STS **0x32**

Bit(s)	R/W	Default	Description
31~20	R/W	0	Not used.
19	R	0	ddr0 write data buffer idle. 1 : idle 0: busy.
18	R	0	ddr0 write data buffer idle. 1 : idle 0: busy.
17	R	0	ddr1 wbuf idle. 1 : idle 0: busy.
16	R	0	ddr0 wbuf idle. 1 : idle 0: busy.
15~8	R	0	AMBUS ports idle. 1 : idle 0: busy.
7~0	R	0	AXI ports idle. 1 : idle 0: busy.

DMC_N_CLK_CTRL **0x33**

Bit(s)	R/W	Default	Description
31~9	R/W	0	Not used.
8	R/W	0	Manual control for hcodec n_clk. 1: enable clock. 0 : disable clock.
7	R/W	0	Manual control for hevc n_clk. 1: enable clock. 0 : disable clock.
6	R/W	0	Manual control for hdcp n_clk. 1: enable clock. 0 : disable clock..
5	R/W	0	Manual control for DEVICE n_clk 1: enable clock. 0 : disable clock.
4	R/W	0	Manual control for ge2d n_clk. 1: enable clock. 0 : disable clock.
3	R/W	0	Manual control for Mali n_clk. 1: enable clock. 0 : disable clock.
2	R/W	0	Manual control for VPU n_clk. 1: enable clock. 0 : disable clock.
1	R/W	0	Manual control for VDEC n_clk. 1: enable clock. 0 : disable clock.
0	R/W	0	Manual control for CPU n_clk. 1: enable clock. 0 : disable clock.

DMC_CMD_FILTER_CTRL1 **0x40**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~20	R/W	0x1f	nugt read buf full access waiting limit

Bit(s)	R/W	Default	Description
19~10	R/W	0x1f	ugt read access waiting limit.
9~0	R/W	0x2f	nugt read access waiting limit

DMC_CMD_FILTER_CTRL2 0x41

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~20	R/W	0x0f	ugt read buf full access waiting limit
19~10	R/W	0x3f	nugt write access pending waiting limit
9~0	R/W	0x7f	ugt write access pending waiting limit.

DMC_CMD_FILTER_CTRL3 0x42

Bit(s)	R/W	Default	Description
31	R/W	0	force wbuf empty.
30~26	R/W	24	wbuf high level number
25~21	R/W	16	wbuf mid level number
20~16	R/W	8	wbuf low level number
15	RW	0	Not used.
14~10	R/W	20	rbuf high level number
9~5	R/W	12	rbuf middle level number
4~0	R/W	6	rbuf low level number

DMC_CMD_FILTER_CTRL4 0x43

Bit(s)	R/W	Default	Description
31~24	R/W	8	sugt rbuf pending limit.
23~16	R/W	30	auto precharge timer when bank is idle
15~8	R/W	0	not used.
7~0	R/W	30	rbuf idle timer if there's small number of write buffers pending

DMC_CMD_FILTER_CTRL5 0x44

Bit(s)	R/W	Default	Description
31~24	R/W	0x1f	Once ddr data bus switch to read, the maxmum read command number to give up the bus when there's write request pending for write buffer.
23~16	R/W	0x1f	Once ddr data bus switch to write, the maxmum write command number to give up the bus when there's read request pending too long.
15~8	R/W	0x0f	Once ddr data bus switch to read, the minimum read command number to transfer back to write stage if there's still pending read request.
7~0	R/W	0x0f	Once ddr data bus switch to write, the minimum write command number to transfer back to read stage if there's still pending write.

DMC_CMD_BUFFER_CTRL 0x45

Bit(s)	R/W	Default	Description
31~26	R/W	32	total write buffer number.
25~20	R/W	24	total read buffer number.
19~10	R/W	0x7f	ugt age waiting limit. over this age limit, this read buffer would turn to super urgent.
9~0	R/W	0x3ff	nugt age waiting limit. over this age limit, this read buffer would turn to super urgent..

DMC_PCTL_LP_CTRL 0x46

Bit(s)	R/W	Default	Description
31~23	R/W	0	Not used.
22	R/W	0	enable DDR chan1 PCTL n_clk auto clock disable feature.
21	R/W	0	disable DDR chan1 PCTL n_clk.

Bit(s)	R/W	Default	Description
20	R/W	0	DDR CHAN1 PCTL APB P_clk enable.
18	R/W	0	enable ddr0 PCTL n_clk auto clock disable feature.
17	R/W	0	disable ddr0 PCTL n_clk.
16	R/W	0	ddr0 PCTL APB P_clk enable..
15~8	R/W	0	latency to disable clock after c_active low.
7~0	R/W	0	latency to disable clock after dfi_lp_req && dfi_lp_ack.

DMC_RDDBUF_CTRL 0x47

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~5	R/W	8	read data BUFFER empty number restriction with no data output. when read data buffer empty number less than this threshold, restrict the dmc_cmd_filter only allow the command with id sequency number = 0 to be generated.
4~0	R/W	4	read data BUFFER empty number restriction with data outputing.

DMC_AM0_CHAN_CTRL 0x60

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.

DMC_AM0_QOS_INC 0x62

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AM0_QOS_INCBK 0x63

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AM0_QOS_DEC 0x64

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AM0_QOS_DECBK 0x65

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AM0_QOS_DIS 0x66

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AM0_QOS_DISBK **0x67**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AM0_QOS_CTRL0 **0x68**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AM0_QOS_CTRL1 **0x69**

Bit(s)	R/W	Default	Description
31~2	R/W	0	Not used.
1	R/W	0	side bank urgent increase enable.
0	R/W	0	side bank urgent decrease enable.

DMC_AM1_CHAN_CTRL **0x6a**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.

DMC_AM1_QOS_INC **0x6c**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AM1_QOS_INCBK **0x6d**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AM1_QOS_DEC **0x6e**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AM1_QOS_DECBK **0x6f**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.

Bit(s)	R/W	Default	Description
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AM1_QOS_DIS 0x70

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AM1_QOS_DISBK 0x71

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AM1_QOS_CTRL0 0x72

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AM1_QOS_CTRL1 0x73

Bit(s)	R/W	Default	Description
31~2	R/W	0	Not used.
1	R/W	0	side bank urgent increase enable.
0	R/W	0	side bank urgent decrease enable.

DMC_AM2_CHAN_CTRL 0x74

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.

DMC_AM2_QOS_INC 0x76

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AM2_QOS_INCBK 0x77

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AM2_QOS_DEC 0x78

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AM2_QOS_DECBK 0x79

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AM2_QOS_DIS 0x7a

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AM2_QOS_DISBK 0x7b

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AM2_QOS_CTRL0 0x7c

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AM2_QOS_CTRL1 0x7d

Bit(s)	R/W	Default	Description
31~2	R/W	0	Not used.
1	R/W	0	side bank urgent increase enable.
0	R/W	0	side bank urgent decrease enable.

DMC_AM3_CHAN_CTRL 0x7e

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.

DMC_AM3_QOS_INC 0x80

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AM3_QOS_INCBK **0x81**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AM3_QOS_DEC **0x82**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AM3_QOS_DECBK **0x83**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AM3_QOS_DIS **0x84**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AM3_QOS_DISBK **0x85**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AM3_QOS_CTRL0 **0x86**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AM3_QOS_CTRL1 **0x87**

Bit(s)	R/W	Default	Description
31~2	R/W	0	Not used.
1	R/W	0	side bank urgent increase enable.
0	R/W	0	side bank urgent decrease enable.

DMC_AM4_CHAN_CTRL **0x88**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.

Bit(s)	R/W	Default	Description
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.

DMC_AM4_QOS_INC 0x8a

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AM4_QOS_INCBK 0x8b

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AM4_QOS_DEC 0x8c

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AM4_QOS_DECBK 0x8d

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AM4_QOS_DIS 0x8e

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AM4_QOS_DISBK 0x8f

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AM4_QOS_CTRL0 0x90

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AM4_QOS_CTRL1 **0x91**

Bit(s)	R/W	Default	Description
31~2	R/W	0	Not used.
1	R/W	0	side bank urgent increase enable.
0	R/W	0	side bank urgent decrease enable.

DMC_AM5_CHAN_CTRL **0x92**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.

DMC_AM5_QOS_INC **0x94**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AM5_QOS_INCBK **0x95**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AM5_QOS_DEC **0x96**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AM5_QOS_DECBK **0x97**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AM5_QOS_DIS **0x98**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AM5_QOS_DISBK **0x99**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AM5_QOS_CTRL0 **0x9a**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.

Bit(s)	R/W	Default	Description
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AM6_CHAN_CTRL **0x9c**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.

DMC_AM6_QOS_INC **0x9e**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AM6_QOS_INCBK **0x9f**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AM6_QOS_DEC **0xa0**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AM6_QOS_DECBK **0xa1**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AM6_QOS_DIS **0xa2**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AM6_QOS_DISBK **0xa3**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AM6_QOS_CTRL0 **0xa4**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AM7_CHAN_CTRL 0xa6

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.

DMC_AM7_HOLD _CTRL 0xa7

Bit(s)	R/W	Default	Description
31~24	R/W	0x18	Write hold number. If the outstanding write request meet this number disable the write request.
23~16	R/W	0x10	Write hold release number. Enable the request if outstanding request is lower than this number.
15~8	R/W	0x18	Read hold number. If the outstanding write request meet this number disable the write request.
7~0	R/W	0x10	READ hold release number. Enable the request if outstanding request is lower than this number.

DMC_AM7_QOS_INC 0xa8

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AM7_QOS_INCBK 0xa9

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AM7_QOS_DEC 0xaa

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AM7_QOS_DECBK 0xab

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AM7_QOS_DIS 0xac

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.

Bit(s)	R/W	Default	Description
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AM7_QOS_DISBK **0xad**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AM7_QOS_CTRL0 **0xae**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AXI0 _CHAN_CTRL **0xb0**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
19	R/W	0	AXI0 default urgent bit
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.
7~0	R/W	0	force this channel all request to be urgent request.

DMC_AXI0_QOS_INC **0xb2**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AXI0_QOS_INCBK **0xb3**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AXI0_QOS_DEC **0xb4**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AXI0_QOS_DECBK **0xb5**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.

Bit(s)	R/W	Default	Description
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AXI0_QOS_DIS **0xb6**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AXI0_QOS_DISBK **0xb7**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AXI0_QOS_CTRL0 **0xb8**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AXI0_QOS_CTRL1 **0xb9**

Bit(s)	R/W	Default	Description
31~20	R/W	0	Not used.
19~16	R	0	FIQ pin status.
15~12	R	0	IRQ pin status.
11	R/W	1	ARM FIQ controlled super urgent enable.
10	R/W	0	ARM FIQ controlled urgent enable.
9	R/W	0	ARM IRQ controlled super urgent enable.
8	R/W	1	ARM IRQ controlled urgent enable.
7	R/W	1	IRQ/FIQ enable.
6~5	R/W	0	Not used.
4	R/W	1	enable AXI0 auto urgent enable. When there's no other request, treat the AXI0 as super urgent request. other wise, use the bit 3:0 to set the urgent.
3~2	R/W	0	AXI0 urgent level if the VIU read ports are not IDLE.
1~0	R/W	2'b01	AXI0 uregent level if the VIU read ports are IDLE.

DMC_AXI1_CHAN_CTRL **0xba**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
19	R/W	0	AXI0 default urgent bit
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.

Bit(s)	R/W	Default	Description
3~0	R/W	0xf	canvas arbiter arbiter weight.
7~0	R/W	0	force this channel all request to be urgent request.

DMC_AXI1_QOS_INC **0xbc**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AXI1_QOS_INCBK **0xbd**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AXI1_QOS_DEC **0xbe**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AXI1_QOS_DECBK **0xbf**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AXI1_QOS_DIS **0xc0**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AXI1_QOS_DISBK **0xc1**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AXI1_QOS_CTRL0 **0xc2**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AXI2_CHAN_CTRL **0xc4**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.

Bit(s)	R/W	Default	Description
19	R/W	0	AXI0 default urgent bit
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.
7~0	R/W	0	force this channel all request to be urgent request.

DMC_AXI2_QOS_INC 0xc6

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AXI2_QOS_INCBK 0xc7

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AXI2_QOS_DEC 0xc8

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AXI2_QOS_DECBK 0xc9

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AXI2_QOS_DIS 0xca

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AXI2_QOS_DISBK 0xcb

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AXI2_QOS_CTRL0 0xcc

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.

Bit(s)	R/W	Default	Description
0	R/W	0	qos enable.

DMC_AXI3_CHAN_CTRL **0xce**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
19	R/W	0	AXI0 default urgent bit
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.
7~0	R/W	0	force this channel all request to be urgent request.

DMC_AXI3_HOLD _CTRL **0xcf**

Bit(s)	R/W	Default	Description
31~24	R/W	0x18	Write hold number. If the outstanding write request meet this number disable the write request.
23~16	R/W	0x10	Write hold release number. Enable the request if outstanding request is lower than this number.
15~8	R/W	0x18	Read hold number. If the outstanding write request meet this number disable the write request.
7~0	R/W	0x10	READ hold release number. Enable the request if outstanding request is lower than this number.

DMC_AXI3_QOS_INC **0xd0**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AXI3_QOS_INCBK **0xd1**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AXI3_QOS_DEC **0xd2**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AXI3_QOS_DECBK **0xd3**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AXI3_QOS_DIS **0xd4**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AXI3_QOS_DISBK **0xd5**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.

Bit(s)	R/W	Default	Description
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AXI3_QOS_CTRL0 **0xd6**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AXI4_CHAN_CTRL **0xd8**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
19	R/W	0	AXI0 default urgent bit
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.
7~0	R/W	0	force this channel all request to be urgent request.

DMC_AXI4_QOS_INC **0xda**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AXI4_QOS_INCBK **0xdb**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AXI4_QOS_DEC **0xdc**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AXI4_QOS_DECBK **0xdd**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AXI4_QOS_DIS **0xde**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.

Bit(s)	R/W	Default	Description
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AXI4_QOS_DISBK **0xdf**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AXI4_QOS_CTRL0 **0xe0**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.
4	R/W	0	qos idle mode enable. enable the idle counter.
3	R/W	0	qos disable enable. enable the feature to disable request.
2	R/W	0	qos decrease urgent enable. enable the decrease urgent function.
1	R/W	0	qos inccrease urgent enable. enabel the increase urgent function.
0	R/W	0	qos enable.

DMC_AXI7_CHAN_CTRL **0xf6**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29:20	R/W	0xff	write request pending cycle number to inc urgent level if not granted.
19	R/W	0	AXI0 default urgent bit
18	R/W	0	force this channel all request to be super urgent request.
17	R/W	0	force this channel all request to be urgent request.
16	R/W	0	force this channel all request to be non urgent request.
13~4	R/W	0x3c	read request pending cycle number to inc urgent level if not granted.
3~0	R/W	0xf	canvas arbiter arbiter weight.
7~0	R/W	0	force this channel all request to be urgent request.

DMC_AXI7_HOLD _CTRL **0xf7**

Bit(s)	R/W	Default	Description
31~24	R/W	0x18	Write hold number. If the outstanding write request meet this number disable the write request.
23~16	R/W	0x10	Write hold release number. Enable the request if outstanding request is lower than this number.
15~8	R/W	0x18	Read hold number. If the outstanding write request meet this number disable the write request.
7~0	R/W	0x10	READ hold release number. Enable the request if outstanding request is lower than this number.

DMC_AXI7_QOS_INC **0xf8**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the leacky bucket counter less this number increase the urgent.

DMC_AXI7_QOS_INCBK **0xf9**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	once the increase urgent triggered, after leacky bucket counter is larger than this number, deassert the increase urgent function.

DMC_AXI7_QOS_DEC **0xfa**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	leacky bucket counter is larger this number, decrease the urgent of this request.

DMC_AXI7_QOS_DECBK **0xfb**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	if the decrease urgent triggered, after leacky buck counter less this number, deassert the decrease urgent function.

DMC_AXI7_QOS_DIS **0xfc**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	when leacky bucket counter larger this number, disable each request some cycles. the disable cycle number is defined in bit 19:12 of QOS_CTRL0

DMC_AXI7_QOS_DISBK **0xfd**

Bit(s)	R/W	Default	Description
31~10	R/W	0	Not used.
9~0	R/W	0	after disable the request, when the leacky bucket counter less than this number, reenable this request..

DMC_AXI7_QOS_CTRL0 **0xfe**

Bit(s)	R/W	Default	Description
31~20	R/W	0	qos idle number. if the channel no request for that long, set leaky bucket counter to 0.
19~14	R/W	0	qos disable cycles. if the leaky bucket counter larger than QOS_DIS register number, than disable the each request how many cycles.
13~6	R/W	0	leackey bucket counter minus number..
5	R/W	0	qos mode. 1 : use bankdwidth as the QOS control. 0 : Use latency as QOS control.

DMC secure register.

Base address 0x0xda838400. Each register takes 4 byte address

DMC_SEC_CTRL **0x0**

Bit(s)	R/W	Default	Description
31	R/W	0	wriTE bit 31 to 1 to update the setting in shadow register for range control registers.
30~0	R/W	0	Not used.

DMC_SEC_RANGE0_CTRL **0x1**

Bit(s)	R/W	Default	Description
31~16	R/W	0	16Bits Range 0 end address. unit : 64Kbyte.
15~0	R/W	0	16Bits Range 0 start address. unit: 64Kbyte.

DMC_SEC_RANGE1_CTRL **0x2**

Bit(s)	R/W	Default	Description
31~16	R/W	0	16Bits Range 1 end address. unit : 64Kbyte.
15~0	R/W	0	16Bits Range 1 start address. unit: 64Kbyte.

DMC_SEC_RANGE2_CTRL **0x3**

Bit(s)	R/W	Default	Description
31~16	R/W	0	16Bits Range 2 end address. unit : 64Kbyte.
15~0	R/W	0	16Bits Range 2 start address. unit: 64Kbyte.

DMC_SEC_RANGE3_CTRL **0x4**

Bit(s)	R/W	Default	Description
31~16	R/W	0	16Bits Range 3 end address. unit : 64Kbyte.
15~0	R/W	0	16Bits Range 3 start address. unit: 64Kbyte.

DMC_SEC_RANGE4_CTRL 0x5

Bit(s)	R/W	Default	Description
31~16	R/W	0	16Bits Range 4 end address. unit : 64Kbyte.
15~0	R/W	0	16Bits Range 4 start address. unit: 64Kbyte.

DMC_SEC_RANGE5_CTRL 0x6

Bit(s)	R/W	Default	Description
31~16	R/W	0	16Bits Range 5 end address. unit : 64Kbyte.
15~0	R/W	0	16Bits Range 5 start address. unit: 64Kbyte.

DMC_SEC_RANGE_CTRL 0x7

Bit(s)	R/W	Default	Description
31~7	R/W	0	Not used.
6	R/W	0	default range security level. 1: secure. 0: unsecure.
5	R/W	0	Range 5 security level. 1 : secure. 0 : unsecure.
4	R/W	0	Range 4 security level. 1 : secure. 0 : unsecure.
3	R/W	0	Range 3 security level. 1 : secure. 0 : unsecure.
2	R/W	0	Range 2 security level. 1 : secure. 0 : unsecure.
1	R/W	0	Range 1 security level. 1 : secure. 0 : unsecure.
0	R/W	0	Range 0 security level. 1 : secure. 0 : unsecure.

DMC_SEC_AXI_PORT_CTRL 0xe

Bit(s)	R/W	Default	Description
31~24	R/W	0	Not used.
23	R/W	0	AXI port3 (HDCP) secure region write access enable bit 1: enable. 0 : disable.
22	R/W	0	AXI port3 (HDCP) non secure region write access enable bit. 1: enable. 0 : disable.
21	R/W	0	AXI port2 (Mali 1) secure region write access enable bit. 1: enable. 0 : disable.
20	R/W	0	AXI port2 (Mali 1) non secure region write access enable bit. 1: enable. 0 : disable.
19	R/W	0	AXI port1 (Mali 0) secure region write access enable bit. 1: enable. 0 : disable.
18	R/W	0	AXI port1 (Mali 0) non secure region write access enable bit. 1: enable. 0 : disable.
17	R/W	0	AXI port0 (CPU) secure region write access enable bit. 1: enable. 0 : disable.
16	R/W	0	AXI port0 (CPU) non secure region write access enable bit. 1: enable. 0 : disable.
15~8	R/W	0	
7	R/W	0	AXI port3 (HDCP) secure region read access enable bit. 1: enable. 0 : disable.
6	R/W	0	AXI port3 (HDCP) non secure region read access enable bit. 1: enable. 0 : disable.
5	R/W	0	AXI port2 (Mali 1) secure region read access enable bit. 1: enable. 0 : disable.
4	R/W	0	AXI port2 (Mali 1) non secure region read access enable bit. 1: enable. 0 : disable.
3	R/W	0	AXI port1 (Mali 0) secure region read access enable bit. 1: enable. 0 : disable.
2	R/W	0	AXI port1 (Mali 0) non secure region read access enable bit. 1: enable. 0 : disable.
1	R/W	0	AXI port0 (CPU) secure region read access enable bit. 1: enable. 0 : disable.
0	R/W	0	AXI port0 (CPU) non secure region read access enable bit. 1: enable. 0 : disable.

DMC_VDEC_SEC_READ_CTRL 0x10

Bit(s)	R/W	Default	Description
31	R/W	0	VDEC subID15 (not used) secure region read access enable bit. 1: enable. 0 : disable.
30	R/W	0	VDEC subID15 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
29	R/W	0	VDEC subID14 (not used) secure region read access enable bit. 1: enable. 0 : disable.
28	R/W	0	VDEC subID14 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
27	R/W	0	VDEC subID13 (not used) secure region read access enable bit. 1: enable. 0 : disable.

Bit(s)	R/W	Default	Description
26	R/W	0	VDEC subID13 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
25	R/W	0	VDEC subID12 (not used) secure region read access enable bit. 1: enable. 0 : disable.
24	R/W	0	VDEC subID12 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
23	R/W	0	VDEC subID11 (not used) secure region read access enable bit. 1: enable. 0 : disable.
22	R/W	0	VDEC subID11 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
21	R/W	0	VDEC subID10 (mbbot) secure region read access enable bit. 1: enable. 0 : disable.
20	R/W	0	VDEC subID10 (mbbot) non secure region read access enable bit. 1: enable. 0 : disable.
19	R/W	0	VDEC subID9 (not used.) secure region read access enable bit. 1: enable. 0 : disable
18	R/W	0	VDEC subID9 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
17	R/W	0	VDEC subID8 (not used.) secure region read access enable bit. 1: enable. 0 : disable.
16	R/W	0	VDEC subID8 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
15	R/W	0	VDEC subID7 (dw) secure region read access enable bit. 1: enable. 0 : disable.
14	R/W	0	VDEC subID7 (dw) non secure region read access enable bit. 1: enable. 0 : disable..
13	R/W	0	VDEC subID6 (comb) secure region read access enable bit. 1: enable. 0 : disable.
12	R/W	0	VDEC subID6 (comb) non secure region read access enable bit. 1: enable. 0 : disable.
11	R/W	0	VDEC subID5 (lmem) secure region read access enable bit. 1: enable. 0 : disable.
10	R/W	0	VDEC subID5 (lmem) non secure region read access enable bit. 1: enable. 0 : disable.
9	R/W	0	VDEC subID4 (imem) secure region read access enable bit. 1: enable. 0 : disable.
8	R/W	0	VDEC subID4 (imem) non secure region read access enable bit. 1: enable. 0 : disable.
7	R/W	0	VDEC subID3 (picdc) secure region read access enable bit. 1: enable. 0 : disable.
6	R/W	0	VDEC subID3 (picdc) non secure region read access enable bit. 1: enable. 0 : disable.
5	R/W	0	VDEC subID2 (psc) secure region read access enable bit. 1: enable. 0 : disable.
4	R/W	0	VDEC subID2 (psc) non secure region read access enable bit. 1: enable. 0 : disable.
3	R/W	0	VDEC subID1 (dcac) secure region read access enable bit. 1: enable. 0 : disable.
2	R/W	0	VDEC subID1 (dcac) non secure region read access enable bit. 1: enable. 0 : disable.
1	R/W	0	VDEC subID0 (vld) secure region read access enable bit. 1: enable. 0 : disable.
0	R/W	0	VDEC subID0 (vld) non secure region read access enable bit. 1: enable. 0 : disable.

DMC_VDEC_SEC_WRITE _CTRL 0x11

Bit(s)	R/W	Default	Description
31	R/W	0	VDEC subID15 (not used) secure region write access enable bit. 1: enable. 0 : disable.
30	R/W	0	VDEC subID15 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
29	R/W	0	VDEC subID14 (not used) secure region write access enable bit. 1: enable. 0 : disable.
28	R/W	0	VDEC subID14 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
27	R/W	0	VDEC subID13 (not used) secure region write access enable bit. 1: enable. 0 : disable.
26	R/W	0	VDEC subID13 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
25	R/W	0	VDEC subID12 (not used) secure region write access enable bit. 1: enable. 0 : disable.
24	R/W	0	VDEC subID12 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
23	R/W	0	VDEC subID11 (not used) secure region write access enable bit. 1: enable. 0 : disable.
22	R/W	0	VDEC subID11 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
21	R/W	0	VDEC subID10 (mbbot) secure region write access enable bit. 1: enable. 0 : disable.
20	R/W	0	VDEC subID10 (mbbot) non secure region write access enable bit. 1: enable. 0 : disable.
19	R/W	0	VDEC subID9 (not used.) secure region write access enable bit. 1: enable. 0 : disable
18	R/W	0	VDEC subID9 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
17	R/W	0	VDEC subID8 (not used.) secure region write access enable bit. 1: enable. 0 : disable.
16	R/W	0	VDEC subID8 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
15	R/W	0	VDEC subID7 (dw) secure region write access enable bit. 1: enable. 0 : disable.
14	R/W	0	VDEC subID7 (dw) non secure region write access enable bit. 1: enable. 0 : disable..
13	R/W	0	VDEC subID6 (comb) secure region write access enable bit. 1: enable. 0 : disable.
12	R/W	0	VDEC subID6 (comb) non secure region write access enable bit. 1: enable. 0 : disable.
11	R/W	0	VDEC subID5 (lmem) secure region write access enable bit. 1: enable. 0 : disable.
10	R/W	0	VDEC subID5 (lmem) non secure region write access enable bit. 1: enable. 0 : disable.
9	R/W	0	VDEC subID4 (imem) secure region write access enable bit. 1: enable. 0 : disable.
8	R/W	0	VDEC subID4 (imem) non secure region write access enable bit. 1: enable. 0 : disable.

Bit(s)	R/W	Default	Description
7	R/W	0	VDEC subID3 (picdc) secure region write access enable bit. 1: enable. 0 : disable.
6	R/W	0	VDEC subID3 (picdc) non secure region write access enable bit. 1: enable. 0 : disable.
5	R/W	0	VDEC subID2 (psc) secure region write access enable bit. 1: enable. 0 : disable.
4	R/W	0	VDEC subID2 (psc) non secure region write access enable bit. 1: enable. 0 : disable.
3	R/W	0	VDEC subID1 (dcac) secure region write access enable bit. 1: enable. 0 : disable.
2	R/W	0	VDEC subID1 (dcac) non secure region write access enable bit. 1: enable. 0 : disable.
1	R/W	0	VDEC subID0 (vld) secure region write access enable bit. 1: enable. 0 : disable.
0	R/W	0	VDEC subID0 (vld) non secure region write access enable bit. 1: enable. 0 : disable.

DMC_VDEC_SEC_CFG 0x12

DWC_VDEC_SEC_READ_CTRL and DMC_VDEC_SEC_WRITE_CTRL register APB bus configuation enable. 2 bit for each port. one for read, one for write.

Bit(s)	R/W	Default	Description
31	R/W	0	VDEC subID15 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
30	R/W	0	VDEC subID14 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
29	R/W	0	VDEC subID13 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
28	R/W	0	VDEC subID12 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
27	R/W	0	VDEC subID11 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
26	R/W	0	VDEC subID10 (mbbot) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
25	R/W	0	VDEC subID9 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
24	R/W	0	VDEC subID8 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
23	R/W	0	VDEC subID7 (dw) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
22	R/W	0	VDEC subID6 (comb) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
21	R/W	0	VDEC subID5 (lmem) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
20	R/W	0	VDEC subID4 (imem) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
19	R/W	0	VDEC subID3 (picdc) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
18	R/W	0	VDEC subID2 (psc) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
17	R/W	0	VDEC subID1 (dcac) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
16	R/W	0	VDEC subID0 (vld) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
15	R/W	0	VDEC subID15 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
14	R/W	0	VDEC subID14 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
13	R/W	0	VDEC subID13 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
12	R/W	0	VDEC subID12 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
11	R/W	0	VDEC subID11 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
10	R/W	0	VDEC subID10 (mbbot) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.

Bit(s)	R/W	Default	Description
9	R/W	0	VDEC subID9 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
8	R/W	0	VDEC subID8 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
7	R/W	0	VDEC subID7 (dw) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
6	R/W	0	VDEC subID6 (comb) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
5	R/W	0	VDEC subID5 (lmem) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
4	R/W	0	VDEC subID4 (imem) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
3	R/W	0	VDEC subID3 (picdc) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
2	R/W	0	VDEC subID2 (psc) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
1	R/W	0	VDEC subID1 (dcac) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
0	R/W	0	VDEC subID0 (vld) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.

DMC_VDEC_EF_TRIG_CTRL 0x13

VDEC Electronic fence trigger selection and trigger secure type. 1 bit for trigger select for one read port. 1 bit for trigger type for one read port. Electronic fence would be triggered by the read from defined secure level from selected subIDs

Bit(s)	R/W	Default	Description
31	R/W	0	trigger type selection for subID15 (). 1 = secure access. 0 : non secure access.
30	R/W	0	trigger type selection for subID14 (). 1 = secure access. 0 : non secure access.
29	R/W	0	trigger type selection for subID13 (). 1 = secure access. 0 : non secure access
28	R/W	0	trigger type selection for subID12 (). 1 = secure access. 0 : non secure access
27	R/W	0	trigger type selection for subID11 (). 1 = secure access. 0 : non secure access
26	R/W	0	trigger type selection for subID10 (mbbot). 1 = secure access. 0 : non secure access
25	R/W	0	trigger type selection for subID9 (). 1 = secure access. 0 : non secure access
24	R/W	0	trigger type selection for subID8 (). 1 = secure access. 0 : non secure access
23	R/W	0	trigger type selection for subID7 (DW). 1 = secure access. 0 : non secure access
22	R/W	0	trigger type selection for subID6 (COMB). 1 = secure access. 0 : non secure access
21	R/W	0	trigger type selection for subID5 (LMEM). 1 = secure access. 0 : non secure access
20	R/W	0	trigger type selection for subID4 (IMEM). 1 = secure access. 0 : non secure access
19	R/W	0	trigger type selection for subID3 (PICDC). 1 = secure access. 0 : non secure access
18	R/W	0	trigger type selection for subID2 (PSC). 1 = secure access. 0 : non secure access.
17	R/W	0	trigger type selection for subID1 (dcac). 1 = secure access. 0 : non secure access.
16	R/W	0	trigger type selection for subID0 (vld). 1 = secure access. 0 : non secure access
15	R/W	0	trigger source selection for subID15 (). 1 = selected. 0 : not selected.
14	R/W	0	trigger source selection for subID14 (). 1 = selected. 0 : not selected.
13	R/W	0	trigger source selection for subID13 (). 1 = selected. 0 : not selected..
12	R/W	0	trigger source selection for subID12 (). 1 = selected. 0 : not selected..
11	R/W	0	trigger source selection for subID11 (). 1 = selected. 0 : not selected.
10	R/W	0	trigger source selection for subID10 (mbbot). 1 = selected. 0 : not selected..
9	R/W	0	trigger source selection for subID9 (). 1 = selected. 0 : not selected..
8	R/W	0	trigger source selection for subID8 (). 1 = selected. 0 : not selected.
7	R/W	0	trigger source selection for subID7 (dw). 1 = selected. 0 : not selected.
6	R/W	0	trigger source selection for subID6 (comb). 1 = selected. 0 : not selected.
5	R/W	0	trigger source selection for subID5 (lmem). 1 = selected. 0 : not selected..
4	R/W	0	trigger source selection for subID4 (imem). 1 = selected. 0 : not selected.
3	R/W	0	trigger source selection for subID3 (picdc). 1 = selected. 0 : not selected.
2	R/W	0	trigger source selection for subID2 (psc). 1 = selected. 0 : not selected..
1	R/W	0	trigger source selection for subID1 (dcac). 1 = selected. 0 : not selected..

Bit(s)	R/W	Default	Description
0	R/W	0	trigger source selection for subID0 (vld). 1 = selected. 0 : not selected.

DMC_VDEC_EF_PROT 0x14

To define which subID would be affected after the EF got triggered.

Bit(s)	R/W	Default	Description
31	R/W	0	EF would affect subID15 () write access secure control. 1 = selected. 0 : not selected. .
30	R/W	0	EF would affect subID14 () write access secure control. 1 = selected. 0 : not selected.
29	R/W	0	EF would affect subID13 () write access secure control. 1 = selected. 0 : not selected.
28	R/W	0	EF would affect subID12 () write access secure control. 1 = selected. 0 : not selected.
27	R/W	0	EF would affect subID11 () write access secure control. 1 = selected. 0 : not selected.
26	R/W	0	EF would affect subID10 (mbbot) write access secure control. 1 = selected. 0 : not selected.
25	R/W	0	EF would affect subID9 () write access secure control. 1 = selected. 0 : not selected.
24	R/W	0	EF would affect subID8 () write access secure control. 1 = selected. 0 : not selected.
23	R/W	0	EF would affect subID7 (dw) write access secure control. 1 = selected. 0 : not selected.
22	R/W	0	EF would affect subID6 (comb) write access secure control. 1 = selected. 0 : not selected.
21	R/W	0	EF would affect subID5 (lmem) write access secure control. 1 = selected. 0 : not selected.
20	R/W	0	EF would affect subID4 (imem) write access secure control. 1 = selected. 0 : not selected.
19	R/W	0	EF would affect subID3 (picdc) write access secure control. 1 = selected. 0 : not selected.
18	R/W	0	EF would affect subID2 (psc) write access secure control. 1 = selected. 0 : not selected.
17	R/W	0	EF would affect subID1 (dcac) write access secure control. 1 = selected. 0 : not selected.
16	R/W	0	EF would affect subID0 (vld) write access secure control. 1 = selected. 0 : not selected.
15	R/W	0	EF would affect subID15 () read access secure control. 1 = selected. 0 : not selected. .
14	R/W	0	EF would affect subID14 () read access secure control. 1 = selected. 0 : not selected.
13	R/W	0	EF would affect subID13 () read access secure control. 1 = selected. 0 : not selected.
12	R/W	0	EF would affect subID12 () read access secure control. 1 = selected. 0 : not selected.
11	R/W	0	EF would affect subID11 () read access secure control. 1 = selected. 0 : not selected.
10	R/W	0	EF would affect subID10 (mbbot) read access secure control. 1 = selected. 0 : not selected.
9	R/W	0	EF would affect subID9 () read access secure control. 1 = selected. 0 : not selected.
8	R/W	0	EF would affect subID8 () read access secure control. 1 = selected. 0 : not selected.
7	R/W	0	EF would affect subID7 (dw) read access secure control. 1 = selected. 0 : not selected.
6	R/W	0	EF would affect subID6 (comb) read access secure control. 1 = selected. 0 : not selected.
5	R/W	0	EF would affect subID5 (lmem) read access secure control. 1 = selected. 0 : not selected.
4	R/W	0	EF would affect subID4 (imem) read access secure control. 1 = selected. 0 : not selected.
3	R/W	0	EF would affect subID3 (picdc) read access secure control. 1 = selected. 0 : not selected.
2	R/W	0	EF would affect subID2 (psc) read access secure control. 1 = selected. 0 : not selected.
1	R/W	0	EF would affect subID1 (dcac) read access secure control. 1 = selected. 0 : not selected.
0	R/W	0	EF would affect subID0 (vld) read access secure control. 1 = selected. 0 : not selected.

DMC_VDEC_EF_READ 0x15

This register contains the vdec read security control Bits after the EF got triggered. If the DMC_VDEC_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_VDEC_SEC_READ_CTRL related Bits.

DMC_VDEC_EF_WRITE 0x16

This register contains the vdec write security control Bits after the EF got triggered. If the DMC_VDEC_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_VDEC_SEC_WRITE _CTRL related Bits.

DMC_HCODEC_SEC_READ_CTRL 0x17

Bit(s)	R/W	Default	Description
31	R/W	0	HCODEC subID15 (not used) secure region read access enable bit. 1: enable. 0 : disable.
30	R/W	0	HCODEC subID15 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
29	R/W	0	HCODEC subID14 (not used) secure region read access enable bit. 1: enable. 0 : disable.
28	R/W	0	HCODEC subID14 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
27	R/W	0	HCODEC subID13 (not used) secure region read access enable bit. 1: enable. 0 : disable.
26	R/W	0	HCODEC subID13 (not used) non secure region read access enable bit. 1: enable. 0 : disable.

Bit(s)	R/W	Default	Description
25	R/W	0	HCODEC subID12 (me) secure region read access enable bit. 1: enable. 0 : disable.
24	R/W	0	HCODEC subID12 (me) non secure region read access enable bit. 1: enable. 0 : disable.
23	R/W	0	HCODEC subID11 (mfdin) secure region read access enable bit. 1: enable. 0 : disable.
22	R/W	0	HCODEC subID11 (mfdin) non secure region read access enable bit. 1: enable. 0 : disable.
21	R/W	0	HCODEC subID10 (mcmbot) secure region read access enable bit. 1: enable. 0 : disable.
20	R/W	0	HCODEC subID10 (mcmbot) non secure region read access enable bit. 1: enable. 0 : disable.
19	R/W	0	HCODEC subID9 (i_pred.) secure region read access enable bit. 1: enable. 0 : disable
18	R/W	0	HCODEC subID9 (i_pred) non secure region read access enable bit. 1: enable. 0 : disable.
17	R/W	0	HCODEC subID8 (qdct.) secure region read access enable bit. 1: enable. 0 : disable.
16	R/W	0	HCODEC subID8 (qdct) non secure region read access enable bit. 1: enable. 0 : disable.
15	R/W	0	HCODEC subID7 (vlc) secure region read access enable bit. 1: enable. 0 : disable.
14	R/W	0	HCODEC subID7 (vlc) non secure region read access enable bit. 1: enable. 0 : disable..
13	R/W	0	HCODEC subID6 (comb) secure region read access enable bit. 1: enable. 0 : disable.
12	R/W	0	HCODEC subID6 (comb) non secure region read access enable bit. 1: enable. 0 : disable.
11	R/W	0	HCODEC subID5 (lmem) secure region read access enable bit. 1: enable. 0 : disable.
10	R/W	0	HCODEC subID5 (lmem) non secure region read access enable bit. 1: enable. 0 : disable.
9	R/W	0	HCODEC subID4 (imem) secure region read access enable bit. 1: enable. 0 : disable.
8	R/W	0	HCODEC subID4 (imem) non secure region read access enable bit. 1: enable. 0 : disable.
7	R/W	0	HCODEC subID3 (mcrcc) secure region read access enable bit. 1: enable. 0 : disable.
6	R/W	0	HCODEC subID3 (mcrcc) non secure region read access enable bit. 1: enable. 0 : disable.
5	R/W	0	HCODEC subID2 (psc) secure region read access enable bit. 1: enable. 0 : disable.
4	R/W	0	HCODEC subID2 (psc) non secure region read access enable bit. 1: enable. 0 : disable.
3	R/W	0	HCODEC subID1 (dcac) secure region read access enable bit. 1: enable. 0 : disable.
2	R/W	0	HCODEC subID1 (dcac) non secure region read access enable bit. 1: enable. 0 : disable.
1	R/W	0	HCODEC subID0 (vld) secure region read access enable bit. 1: enable. 0 : disable.
0	R/W	0	HCODEC subID0 (vld) non secure region read access enable bit. 1: enable. 0 : disable.

DMC_HCODEC_SEC_WRITE _CTRL **0x18**

Bit(s)	R/W	Default	Description
31	R/W	0	HCODEC subID15 (not used) secure region write access enable bit. 1: enable. 0 : disable.
30	R/W	0	HCODEC subID15 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
29	R/W	0	HCODEC subID14 (not used) secure region write access enable bit. 1: enable. 0 : disable.
28	R/W	0	HCODEC subID14 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
27	R/W	0	HCODEC subID13 (not used) secure region write access enable bit. 1: enable. 0 : disable.
26	R/W	0	HCODEC subID13 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
25	R/W	0	HCODEC subID12 (me) secure region write access enable bit. 1: enable. 0 : disable.
24	R/W	0	HCODEC subID12 (me) non secure region write access enable bit. 1: enable. 0 : disable.
23	R/W	0	HCODEC subID11 (mfdin) secure region write access enable bit. 1: enable. 0 : disable.
22	R/W	0	HCODEC subID11 (mfdin) non secure region write access enable bit. 1: enable. 0 : disable.
21	R/W	0	HCODEC subID10 (mcmbot) secure region write access enable bit. 1: enable. 0 : disable.
20	R/W	0	HCODEC subID10 (mcmbot) non secure region write access enable bit. 1: enable. 0 : disable.
19	R/W	0	HCODEC subID9 (i_pred.) secure region write access enable bit. 1: enable. 0 : disable
18	R/W	0	HCODEC subID9 (i_pred) non secure region write access enable bit. 1: enable. 0 : disable.
17	R/W	0	HCODEC subID8 (qdct.) secure region write access enable bit. 1: enable. 0 : disable.
16	R/W	0	HCODEC subID8 (qdct) non secure region write access enable bit. 1: enable. 0 : disable.
15	R/W	0	HCODEC subID7 (vlc) secure region write access enable bit. 1: enable. 0 : disable.
14	R/W	0	HCODEC subID7 (vlc) non secure region write access enable bit. 1: enable. 0 : disable..
13	R/W	0	HCODEC subID6 (comb) secure region write access enable bit. 1: enable. 0 : disable.
12	R/W	0	HCODEC subID6 (comb) non secure region write access enable bit. 1: enable. 0 : disable.
11	R/W	0	HCODEC subID5 (lmem) secure region write access enable bit. 1: enable. 0 : disable.
10	R/W	0	HCODEC subID5 (lmem) non secure region write access enable bit. 1: enable. 0 : disable.
9	R/W	0	HCODEC subID4 (imem) secure region write access enable bit. 1: enable. 0 : disable.
8	R/W	0	HCODEC subID4 (imem) non secure region write access enable bit. 1: enable. 0 : disable.
7	R/W	0	HCODEC subID3 (mcrcc) secure region write access enable bit. 1: enable. 0 : disable.

Bit(s)	R/W	Default	Description
6	R/W	0	HCODEC subID3 (mcrcc) non secure region write access enable bit. 1: enable. 0 : disable.
5	R/W	0	HCODEC subID2 (psc) secure region write access enable bit. 1: enable. 0 : disable.
4	R/W	0	HCODEC subID2 (psc) non secure region write access enable bit. 1: enable. 0 : disable.
3	R/W	0	HCODEC subID1 (dcac) secure region write access enable bit. 1: enable. 0 : disable.
2	R/W	0	HCODEC subID1 (dcac) non secure region write access enable bit. 1: enable. 0 : disable.
1	R/W	0	HCODEC subID0 (vld) secure region write access enable bit. 1: enable. 0 : disable.
0	R/W	0	HCODEC subID0 (vld) non secure region write access enable bit. 1: enable. 0 : disable.

DMC_HCODEC_SEC_CFG 0x19

DWC_HCODEC_SEC_READ_CTRL and DMC_HCODEC_SEC_WRITE_CTRL register APB bus configuation enable. 2 bit for each port. one for read, one for write.

Bit(s)	R/W	Default	Description
31	R/W	0	HCODEC subID15 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
30	R/W	0	HCODEC subID14 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
29	R/W	0	HCODEC subID13 () To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
28	R/W	0	HCODEC subID12 (me) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
27	R/W	0	HCODEC subID11 (mfdin) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
26	R/W	0	HCODEC subID10 (mcmbot) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
25	R/W	0	HCODEC subID9 (i_pred) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
24	R/W	0	HCODEC subID8 (qdct) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
23	R/W	0	HCODEC subID7 (vlc) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
22	R/W	0	HCODEC subID6 (comb) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
21	R/W	0	HCODEC subID5 (lmem) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
20	R/W	0	HCODEC subID4 (imem) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
19	R/W	0	HCODEC subID3 (mcrcc) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
18	R/W	0	HCODEC subID2 (psc) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
17	R/W	0	HCODEC subID1 (dcac) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
16	R/W	0	HCODEC subID0 (vld) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
15	R/W	0	HCODEC subID15 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
14	R/W	0	HCODEC subID14 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
13	R/W	0	HCODEC subID13 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
12	R/W	0	HCODEC subID12 (me) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
11	R/W	0	HCODEC subID11 (mfdin) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
10	R/W	0	HCODEC subID10 (mcmbot) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
9	R/W	0	HCODEC subID9 (i_pred) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.

Bit(s)	R/W	Default	Description
8	R/W	0	HCODEC subID8 (qdct) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
7	R/W	0	HCODEC subID7 (vlc) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
6	R/W	0	HCODEC subID6 (comb) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
5	R/W	0	HCODEC subID5 (lmem) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
4	R/W	0	HCODEC subID4 (imem) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
3	R/W	0	HCODEC subID3 (mcrcc) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
2	R/W	0	HCODEC subID2 (psc) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
1	R/W	0	HCODEC subID1 (dcac) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
0	R/W	0	HCODEC subID0 (vld) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.

DMC_HCODEC_EF_TRIG_CTRL 0x1a

HCODEC Electronic fence trigger selection and trigger secure type. 1 bit for trigger select for one read port. 1 bit for trigger type for one read port. Electronic fence would be triggered by the read from defined secure level from selected subIDs

Bit(s)	R/W	Default	Description
31	R/W	0	trigger type selection for subID15 (). 1 = secure access. 0 : non secure access.
30	R/W	0	trigger type selection for subID14 (). 1 = secure access. 0 : non secure access.
29	R/W	0	trigger type selection for subID13 (). 1 = secure access. 0 : non secure access
28	R/W	0	trigger type selection for subID12 (me). 1 = secure access. 0 : non secure access
27	R/W	0	trigger type selection for subID11 (mfdin). 1 = secure access. 0 : non secure access
26	R/W	0	trigger type selection for subID10 (mcmbot). 1 = secure access. 0 : non secure access
25	R/W	0	trigger type selection for subID9 (i_pred). 1 = secure access. 0 : non secure access
24	R/W	0	trigger type selection for subID8 (qdct). 1 = secure access. 0 : non secure access
23	R/W	0	trigger type selection for subID7 (vlc). 1 = secure access. 0 : non secure access
22	R/W	0	trigger type selection for subID6 (COMB). 1 = secure access. 0 : non secure access
21	R/W	0	trigger type selection for subID5 (LMEM). 1 = secure access. 0 : non secure access
20	R/W	0	trigger type selection for subID4 (IMEM). 1 = secure access. 0 : non secure access
19	R/W	0	trigger type selection for subID3 (mcrcc). 1 = secure access. 0 : non secure access
18	R/W	0	trigger type selection for subID2 (PSC). 1 = secure access. 0 : non secure access.
17	R/W	0	trigger type selection for subID1 (dcac). 1 = secure access. 0 : non secure access.
16	R/W	0	trigger type selection for subID0 (vld). 1 = secure access. 0 : non secure access
15	R/W	0	trigger source selection for subID15 (). 1 = selected. 0 : not selected.
14	R/W	0	trigger source selection for subID14 (). 1 = selected. 0 : not selected.
13	R/W	0	trigger source selection for subID13 (). 1 = selected. 0 : not selected..
12	R/W	0	trigger source selection for subID12 (me). 1 = selected. 0 : not selected..
11	R/W	0	trigger source selection for subID11 (mfdin). 1 = selected. 0 : not selected.
10	R/W	0	trigger source selection for subID10 (mcmbot). 1 = selected. 0 : not selected..
9	R/W	0	trigger source selection for subID9 (i_pred). 1 = selected. 0 : not selected..
8	R/W	0	trigger source selection for subID8 (qdct). 1 = selected. 0 : not selected.
7	R/W	0	trigger source selection for subID7 (vlc). 1 = selected. 0 : not selected.
6	R/W	0	trigger source selection for subID6 (comb). 1 = selected. 0 : not selected.
5	R/W	0	trigger source selection for subID5 (lmem). 1 = selected. 0 : not selected..
4	R/W	0	trigger source selection for subID4 (imem). 1 = selected. 0 : not selected.
3	R/W	0	trigger source selection for subID3 (mcrcc). 1 = selected. 0 : not selected.
2	R/W	0	trigger source selection for subID2 (psc). 1 = selected. 0 : not selected..
1	R/W	0	trigger source selection for subID1 (dcac). 1 = selected. 0 : not selected..
0	R/W	0	trigger source selection for subID0 (vld). 1 = selected. 0 : not selected.

DMC_HCODEC_EF_PROT 0x1b

To define which subID would be affected after the EF got triggered.

Bit(s)	R/W	Default	Description
31	R/W	0	EF would affect subID15 () write access secure control. 1 = selected. 0 : not selected. .
30	R/W	0	EF would affect subID14 () write access secure control. 1 = selected. 0 : not selected.
29	R/W	0	EF would affect subID13 () write access secure control. 1 = selected. 0 : not selected.
28	R/W	0	EF would affect subID12 (me) write access secure control. 1 = selected. 0 : not selected.
27	R/W	0	EF would affect subID11 (mfdin) write access secure control. 1 = selected. 0 : not selected.
26	R/W	0	EF would affect subID10 (mcmbot) write access secure control. 1 = selected. 0 : not selected.
25	R/W	0	EF would affect subID9 (i_pred) write access secure control. 1 = selected. 0 : not selected.
24	R/W	0	EF would affect subID8 (qdct) write access secure control. 1 = selected. 0 : not selected.
23	R/W	0	EF would affect subID7 (vlc) write access secure control. 1 = selected. 0 : not selected.
22	R/W	0	EF would affect subID6 (comb) write access secure control. 1 = selected. 0 : not selected.
21	R/W	0	EF would affect subID5 (lmem) write access secure control. 1 = selected. 0 : not selected.
20	R/W	0	EF would affect subID4 (imem) write access secure control. 1 = selected. 0 : not selected.
19	R/W	0	EF would affect subID3 (mcrcc) write access secure control. 1 = selected. 0 : not selected.
18	R/W	0	EF would affect subID2 (psc) write access secure control. 1 = selected. 0 : not selected.
17	R/W	0	EF would affect subID1 (dcac) write access secure control. 1 = selected. 0 : not selected.
16	R/W	0	EF would affect subID0 (vld) write access secure control. 1 = selected. 0 : not selected.
15	R/W	0	EF would affect subID15 () read access secure control. 1 = selected. 0 : not selected. .
14	R/W	0	EF would affect subID14 () read access secure control. 1 = selected. 0 : not selected.
13	R/W	0	EF would affect subID13 () read access secure control. 1 = selected. 0 : not selected.
12	R/W	0	EF would affect subID12 (me) read access secure control. 1 = selected. 0 : not selected.
11	R/W	0	EF would affect subID11 (mfdin) read access secure control. 1 = selected. 0 : not selected.
10	R/W	0	EF would affect subID10 (mcmbot) read access secure control. 1 = selected. 0 : not selected.
9	R/W	0	EF would affect subID9 (i_pred) read access secure control. 1 = selected. 0 : not selected.
8	R/W	0	EF would affect subID8 (qdct) read access secure control. 1 = selected. 0 : not selected.
7	R/W	0	EF would affect subID7 (vlc) read access secure control. 1 = selected. 0 : not selected.
6	R/W	0	EF would affect subID6 (comb) read access secure control. 1 = selected. 0 : not selected.
5	R/W	0	EF would affect subID5 (lmem) read access secure control. 1 = selected. 0 : not selected.
4	R/W	0	EF would affect subID4 (imem) read access secure control. 1 = selected. 0 : not selected.
3	R/W	0	EF would affect subID3 (mcrcc) read access secure control. 1 = selected. 0 : not selected.
2	R/W	0	EF would affect subID2 (psc) read access secure control. 1 = selected. 0 : not selected.
1	R/W	0	EF would affect subID1 (dcac) read access secure control. 1 = selected. 0 : not selected.
0	R/W	0	EF would affect subID0 (vld) read access secure control. 1 = selected. 0 : not selected.

DMC_HCODEC_EF_READ 0x1c

This register contains the HCODEC read security control Bits after the EF got triggered. If the DMC_HCODEC_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_HCODEC_SEC_READ_CTRL related Bits.

DMC_HCODEC_EF_WRITE 0x1d

This register contains the HCODEC write security control Bits after the EF got triggered. If the DMC_HCODEC_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_HCODEC_SEC_WRITE _CTRL related Bits.

DMC_HEVC_SEC_READ_CTRL 0x1e

Bit(s)	R/W	Default	Description
31~18	R/W	0	Not used.
17	R/W	0	HEVC LMEM secure region read access enable bit. 1: enable. 0 : disable.
16	R/W	0	HEVC LMEM non secure region read access enable bit. 1: enable. 0 : disable.
15	R/W	0	HEVC subid 7(MPRED) secure region read access enable bit. 1: enable. 0 : disable.
14	R/W	0	HEVC subid 7(MPRED) non secure region read access enable bit. 1: enable. 0 : disable..
13	R/W	0	HEVC subid 6(DBLK_D) secure region read access enable bit. 1: enable. 0 : disable.
12	R/W	0	HEVC subid 6(DBLK_D) non secure region read access enable bit. 1: enable. 0 : disable.
11	R/W	0	HEVC subid 5(DBLK_P) secure region read access enable bit. 1: enable. 0 : disable.
10	R/W	0	HEVC subid 5(DBLK_P) non secure region read access enable bit. 1: enable. 0 : disable.

Bit(s)	R/W	Default	Description
9	R/W	0	HEVC subid 4(IPP) secure region read access enable bit. 1: enable. 0 : disable.
8	R/W	0	HEVC subid 4(IPP) non secure region read access enable bit. 1: enable. 0 : disable.
7	R/W	0	HEVC subid 3(MPP) secure region read access enable bit. 1: enable. 0 : disable.
6	R/W	0	HEVC subid 3(MPP) non secure region read access enable bit. 1: enable. 0 : disable.
5	R/W	0	HEVC subID2 (SAO) secure region read access enable bit. 1: enable. 0 : disable.
4	R/W	0	HEVC subID2 (SAO) non secure region read access enable bit. 1: enable. 0 : disable.
3	R/W	0	HEVC subID1 (stream) secure region read access enable bit. 1: enable. 0 : disable.
2	R/W	0	HEVC subID1 (stream) non secure region read access enable bit. 1: enable. 0 : disable.
1	R/W	0	HEVC subID0 (IMEM) secure region read access enable bit. 1: enable. 0 : disable.
0	R/W	0	HEVC subID0 (IMEM) non secure region read access enable bit. 1: enable. 0 : disable.

DMC_HEVC_SEC_WRITE_CTRL 0x1f

Bit(s)	R/W	Default	Description
31~18	R/W	0	Not used.
17	R/W	0	HEVC LMEM secure region read access enable bit. 1: enable. 0 : disable.
17	R/W	0	HEVC LMEM non secure region read access enable bit. 1: enable. 0 : disable.
15	R/W	0	HEVC subid 7(MPRED) secure region read access enable bit. 1: enable. 0 : disable.
14	R/W	0	HEVC subid 7(MPRED) non secure region read access enable bit. 1: enable. 0 : disable..
13	R/W	0	HEVC subid 6(DBLK_D) secure region read access enable bit. 1: enable. 0 : disable.
12	R/W	0	HEVC subid 6(DBLK_D) non secure region read access enable bit. 1: enable. 0 : disable.
11	R/W	0	HEVC subid 5(DBLK_P) secure region read access enable bit. 1: enable. 0 : disable.
10	R/W	0	HEVC subid 5(DBLK_P) non secure region read access enable bit. 1: enable. 0 : disable.
9	R/W	0	HEVC subid 4(IPP) secure region read access enable bit. 1: enable. 0 : disable.
8	R/W	0	HEVC subid 4(IPP) non secure region read access enable bit. 1: enable. 0 : disable.
7	R/W	0	HEVC subid 3(MPP) secure region read access enable bit. 1: enable. 0 : disable.
6	R/W	0	HEVC subid 3(MPP) non secure region read access enable bit. 1: enable. 0 : disable.
5	R/W	0	HEVC subID2 (SAO) secure region read access enable bit. 1: enable. 0 : disable.
4	R/W	0	HEVC subID2 (SAO) non secure region read access enable bit. 1: enable. 0 : disable.
3	R/W	0	HEVC subID1 (stream) secure region read access enable bit. 1: enable. 0 : disable.
2	R/W	0	HEVC subID1 (stream) non secure region read access enable bit. 1: enable. 0 : disable.
1	R/W	0	HEVC subID0 (IMEM) secure region read access enable bit. 1: enable. 0 : disable.
0	R/W	0	HEVC subID0 (IMEM) non secure region read access enable bit. 1: enable. 0 : disable.

DMC_HEVC_SEC_CFG 0x20

DWC_HEVC _SEC_READ_CTRL and DMC_HEVC _SEC_WRITE_CTRL register APB bus configuation enable. 2 bit for each port. one for read, one for write.

Bit(s)	R/W	Default	Description
31~25	R/W	0	Not used
24	R/W	0	HEVC subID (LMEM) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
23	R/W	0	HEVC subid 7(MPRED) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
22	R/W	0	HEVC subid 6(DBLK_D) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
21	R/W	0	HEVC subid 5(DBLK_P) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
20	R/W	0	HEVC subid 4(IPP) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
19	R/W	0	HEVC subid 3(MPP) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
18	R/W	0	HEVC subID2 (SAO) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
17	R/W	0	HEVC subID1 (stream) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.

Bit(s)	R/W	Default	Description
16	R/W	0	HEVC subID0 (IMEM) To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
15~9	R/W	0	Not used
8	R/W	0	HEVC subID (LMEM) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
7	R/W	0	HEVC subid 7(MPRED) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
6	R/W	0	HEVC subid 6(DBLK_D) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
5	R/W	0	HEVC subid 5(DBLK_P) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
4	R/W	0	HEVC subid 4(IPP) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
3	R/W	0	HEVC subid 3(MPP) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
2	R/W	0	HEVC subID2 (SAO) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
1	R/W	0	HEVC subID1 (stream) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
0	R/W	0	HEVC subID0 (IMEM) To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.

DMC_HEVC _EF_TRIG_CTRL 0x21

HEVC Electronic fence trigger selection and trigger secure type. 1 bit for trigger select for one read port. 1 bit for trigger type for one read port. Electronic fence would be triggered by the read from defined secure level from selected subIDs

Bit(s)	R/W	Default	Description
31~25	R/W	0	Not used.
24	R/W	0	trigger type selection for subID LMEM 1 = secure access. 0 : non secure access.
23	R/W	0	trigger type selection for subID7 (MPRED) 1 = secure access. 0 : non secure access
22	R/W	0	trigger type selection for subID6(DBLK_D). 1 = selected. 0 : not selected.
21	R/W	0	trigger type e selection for subID5 (DBLK_P). 1 = selected. 0 : not selected.
20	R/W	0	trigger type selection for subID4 (IPP). 1 = selected. 0 : not selected..
19	R/W	0	trigger type selection for subID3 (MPP). 1 = selected. 0 : not selected..
18	R/W	0	trigger type selection for subID2 (SAO). 1 = selected. 0 : not selected.
17	R/W	0	trigger type selection for subID1 (stream). 1 = selected. 0 : not selected..
16	R/W	0	trigger type selection for subID0 (IMEM). 1 = selected. 0 : not selected..
15~9	R/W	0	Not used.
8	R/W	0	trigger source selection for subID8 (LMEM). 1 = selected. 0 : not selected.
7	R/W	0	trigger source selection for subID7 (MPRED). 1 = selected. 0 : not selected.
6	R/W	0	trigger source selection for subID6 (DBLK_D). 1 = selected. 0 : not selected.
5	R/W	0	trigger source selection for subID5 (DBLK_P). 1 = selected. 0 : not selected..
4	R/W	0	trigger source selection for subID4 (IPP). 1 = selected. 0 : not selected.
3	R/W	0	trigger source selection for subID3 (MPP). 1 = selected. 0 : not selected.
2	R/W	0	trigger source selection for subID2 (SAO). 1 = selected. 0 : not selected..
1	R/W	0	trigger source selection for subID1 (stream). 1 = selected. 0 : not selected..
0	R/W	0	trigger source selection for subID0 (IMEM). 1 = selected. 0 : not selected.

DMC_HEVC _EF_PROT 0x22

To define which subID would be affected after the EF got triggered.

Bit(s)	R/W	Default	Description
31~25	R/W	0	Not used..
24	R/W	0	EF would affect subID LMEM write access secure control. 1 = selected. 0 : not selected.
23	R/W	0	EF would affect subID7 (mpred) write access secure control. 1 = selected. 0 : not selected.
22	R/W	0	EF would affect subID6 (DBLK_D) write access secure control. 1 = selected. 0 : not selected.
21	R/W	0	EF would affect subID5 (DBLK_P) write access secure control. 1 = selected. 0 : not selected.

Bit(s)	R/W	Default	Description
20	R/W	0	EF would affect subID4 (IPP) write access secure control. 1 = selected. 0 : not selected.
19	R/W	0	EF would affect subID3 (MPP) write access secure control. 1 = selected. 0 : not selected.
18	R/W	0	EF would affect subID2 (SAO) write access secure control. 1 = selected. 0 : not selected.
17	R/W	0	EF would affect subID1 (STREAM) write access secure control. 1 = selected. 0 : not selected.
16	R/W	0	EF would affect subID0 (IMEM) write access secure control. 1 = selected. 0 : not selected.
15~9	R/W	0	Not used.
8	R/W	0	EF would affect subID8= (LMEM) read access secure control. 1 = selected. 0 : not selected.
7	R/W	0	EF would affect subID7 (MPRED) read access secure control. 1 = selected. 0 : not selected.
6	R/W	0	EF would affect subID6 (DBLK_D) read access secure control. 1 = selected. 0 : not selected.
5	R/W	0	EF would affect subID5 (DBLK_P) read access secure control. 1 = selected. 0 : not selected.
4	R/W	0	EF would affect subID4 (IPP) read access secure control. 1 = selected. 0 : not selected.
3	R/W	0	EF would affect subID3 (MPP) read access secure control. 1 = selected. 0 : not selected.
2	R/W	0	EF would affect subID2 (SAO) read access secure control. 1 = selected. 0 : not selected.
1	R/W	0	EF would affect subID1 (STREAM) read access secure control. 1 = selected. 0 : not selected.
0	R/W	0	EF would affect subID0 (IMEM) read access secure control. 1 = selected. 0 : not selected.

DMC_HEVC _EF_READ 0x23

This register contains the HEVC read security control Bits after the EF got triggered. If the DMC_HEVC _EF_PROT register bit 8:0 related bit was enabled, then the related secure control Bits would be copied to DMC_HEVC_SEC_READ_CTRL related Bits.

DMC_HEVC _EF_WRITE 0x24

This register contains the HEVC write security control Bits after the EF got triggered. If the DMC_HEVC _EF_PROT register bit 8:0 related bit was enabled, then the related secure control Bits would be copied to DMC_HEVC _SEC_WRITE _CTRL related Bits.

DMC_VPU _SEC_READ_CTRL 0x32

Bit(s)	R/W	Default	Description
31	R/W	0	VPU subID15 (RDMA_RD) secure region read access enable bit. 1: enable. 0 : disable.
30	R/W	0	VPU subID15 (RDMA_RD) non secure region read access enable bit. 1: enable. 0 : disable.
29	R/W	0	VPU subID14 (not used) secure region read access enable bit. 1: enable. 0 : disable.
28	R/W	0	VPU subID14 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
27	R/W	0	VPU subID13 (not used) secure region read access enable bit. 1: enable. 0 : disable.
26	R/W	0	VPU subID13 (not used) non secure region read access enable bit. 1: enable. 0 : disable.
25	R/W	0	VPU subID12 (DI_MISC) secure region read access enable bit. 1: enable. 0 : disable.
24	R/W	0	VPU subID12 (DI_MISC) non secure region read access enable bit. 1: enable. 0 : disable.
23	R/W	0	VPU subID11 (DI_CHAN2) secure region read access enable bit. 1: enable. 0 : disable.
22	R/W	0	VPU subID11 (DI_CHAN2) non secure region read access enable bit. 1: enable. 0 : disable.
21	R/W	0	VPU subID10 (DI_INP) secure region read access enable bit. 1: enable. 0 : disable.
20	R/W	0	VPU subID10 (DI_INP) non secure region read access enable bit. 1: enable. 0 : disable.
19	R/W	0	VPU subID9 (DI_MEM) secure region read access enable bit. 1: enable. 0 : disable
18	R/W	0	VPU subID9(DI_MEM) non secure region read access enable bit. 1: enable. 0 : disable.
17	R/W	0	VPU subID8 (DI_IF1) secure region read access enable bit. 1: enable. 0 : disable.
16	R/W	0	VPU subID8 (DI_IF1) non secure region read access enable bit. 1: enable. 0 : disable.
15	R/W	0	VPU subID7 () secure region read access enable bit. 1: enable. 0 : disable.
14	R/W	0	VPU subID7 () non secure region read access enable bit. 1: enable. 0 : disable..
13	R/W	0	VPU subID6 () secure region read access enable bit. 1: enable. 0 : disable.
12	R/W	0	VPU subID6 () non secure region read access enable bit. 1: enable. 0 : disable.
11	R/W	0	VPU subID5 () secure region read access enable bit. 1: enable. 0 : disable.
10	R/W	0	VPU subID5 () non secure region read access enable bit. 1: enable. 0 : disable.
9	R/W	0	VPU subID4 (AFBC_DEC) secure region read access enable bit. 1: enable. 0 : disable.
8	R/W	0	VPU subID4 (AFBC_DEC) non secure region read access enable bit. 1: enable. 0 : disable.
7	R/W	0	VPU subID3 (VD2) secure region read access enable bit. 1: enable. 0 : disable.
6	R/W	0	VPU subID3 (VD2) non secure region read access enable bit. 1: enable. 0 : disable.
5	R/W	0	VPU subID2 (VD1) secure region read access enable bit. 1: enable. 0 : disable.
4	R/W	0	VPU subID2 (VD1) non secure region read access enable bit. 1: enable. 0 : disable.

Bit(s)	R/W	Default	Description
3	R/W	0	VPU subID1 (OSD2) secure region read access enable bit. 1: enable. 0 : disable.
2	R/W	0	VPU subID1 (OSD2) non secure region read access enable bit. 1: enable. 0 : disable.
1	R/W	0	VPU subID0 (OSD1) secure region read access enable bit. 1: enable. 0 : disable.
0	R/W	0	VPU subID0 (OSD1) non secure region read access enable bit. 1: enable. 0 : disable.

DMC_VPU_SEC_WRITE _CTRL 0x33

Bit(s)	R/W	Default	Description
31	R/W	0	VPU subID15 (RDMA_WR) secure region write access enable bit. 1: enable. 0 : disable.
30	R/W	0	VPU subID15 (RDMA_WR) non secure region write access enable bit. 1: enable. 0 : disable.
29	R/W	0	VPU subID14 (not used) secure region write access enable bit. 1: enable. 0 : disable.
28	R/W	0	VPU subID14 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
27	R/W	0	VPU subID13 (not used) secure region write access enable bit. 1: enable. 0 : disable.
26	R/W	0	VPU subID13 (not used) non secure region write access enable bit. 1: enable. 0 : disable.
25	R/W	0	VPU subID12 (DI_MISC) secure region write access enable bit. 1: enable. 0 : disable.
24	R/W	0	VPU subID12 (DI_MISC) non secure region write access enable bit. 1: enable. 0 : disable.
23	R/W	0	VPU subID11 (DI_WR) secure region write access enable bit. 1: enable. 0 : disable.
22	R/W	0	VPU subID11 (DI_WR) non secure region write access enable bit. 1: enable. 0 : disable.
21	R/W	0	VPU subID10 (NR_WR) secure region write access enable bit. 1: enable. 0 : disable.
20	R/W	0	VPU subID10 (NR_WR) non secure region write access enable bit. 1: enable. 0 : disable.
19	R/W	0	VPU subID9 (VDIN1) secure region write access enable bit. 1: enable. 0 : disable
18	R/W	0	VPU subID9 (VDIN1) non secure region write access enable bit. 1: enable. 0 : disable.
17	R/W	0	VPU subID8 (VDIN0.) secure region write access enable bit. 1: enable. 0 : disable.
16	R/W	0	VPU subID8 (VDIN0) non secure region write access enable bit. 1: enable. 0 : disable.
15	R/W	0	VPU subID7 () secure region write access enable bit. 1: enable. 0 : disable.
14	R/W	0	VPU subID7 () non secure region write access enable bit. 1: enable. 0 : disable..
13	R/W	0	VPU subID6 () secure region write access enable bit. 1: enable. 0 : disable.
12	R/W	0	VPU subID6 () non secure region write access enable bit. 1: enable. 0 : disable.
11	R/W	0	VPU subID5 () secure region write access enable bit. 1: enable. 0 : disable.
10	R/W	0	VPU subID5 () non secure region write access enable bit. 1: enable. 0 : disable.
9	R/W	0	VPU subID4 () secure region write access enable bit. 1: enable. 0 : disable.
8	R/W	0	VPU subID4 () non secure region write access enable bit. 1: enable. 0 : disable.
7	R/W	0	VPU subID3 () secure region write access enable bit. 1: enable. 0 : disable.
6	R/W	0	VPU subID3 () non secure region write access enable bit. 1: enable. 0 : disable.
5	R/W	0	VPU subID2 () secure region write access enable bit. 1: enable. 0 : disable.
4	R/W	0	VPU subID2 () non secure region write access enable bit. 1: enable. 0 : disable.
3	R/W	0	VPU subID1 () secure region write access enable bit. 1: enable. 0 : disable.
2	R/W	0	VPU subID1 () non secure region write access enable bit. 1: enable. 0 : disable.
1	R/W	0	VPU subID0 () secure region write access enable bit. 1: enable. 0 : disable.
0	R/W	0	VPU subID0 () non secure region write access enable bit. 1: enable. 0 : disable.

DMC_VPU_SEC_CFG 0x19

DWC_VPU_SEC_READ_CTRL and DMC_VPU_SEC_WRITE_CTRL register APB bus configuation enable. 2 bit for each port. one for read, one for write.

Bit(s)	R/W	Default	Description
31	R/W	0	VPU subID15 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
30	R/W	0	VPU subID14To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
29	R/W	0	VPU subID13 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
28	R/W	0	VPU subID12 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
27	R/W	0	VPU subID11 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
26	R/W	0	VPU subID10 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.

Bit(s)	R/W	Default	Description
25	R/W	0	VPU subID9 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
24	R/W	0	VPU subID8 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
23	R/W	0	VPU subID7 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
22	R/W	0	VPU subID6 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
21	R/W	0	VPU subID5 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
20	R/W	0	VPU subID4 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
19	R/W	0	VPU subID3 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
18	R/W	0	VPU subID2 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
17	R/W	0	VPU subID1 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
16	R/W	0	VPU subID0 To enable APB bus modifiy the write security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
15	R/W	0	VPU subID15 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
14	R/W	0	VPU subID14 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
13	R/W	0	VPU subID13 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
12	R/W	0	VPU subID12 To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
11	R/W	0	VPU subID11 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
10	R/W	0	VPU subID10 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
9	R/W	0	VPU subID9 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
8	R/W	0	VPU subID8 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
7	R/W	0	VPU subID7 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
6	R/W	0	VPU subID6 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
5	R/W	0	VPU subID5 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
4	R/W	0	VPU subID4 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
3	R/W	0	VPU subID3 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
2	R/W	0	VPU subID2 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
1	R/W	0	VPU subID1 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.
0	R/W	0	VPU subID0 () To enable APB bus modifiy the read security control Bits. 1 : eable the APB modify. 0 : disable APB bus modify.

DMC_VPU_EF0_TRIG_CTRL **0x26**

VPU Electronic fence trigger selection and trigger secure type. 1 bit for trigger select for one read port. 1 bit for trigger type for one read port. Electronic fence would be triggered by the read from defined secure level from selected subIDs

Bit(s)	R/W	Default	Description
31	R/W	0	trigger type selection for subID15 (). 1 = secure access. 0 : non secure access.

Bit(s)	R/W	Default	Description
30	R/W	0	trigger type selection for subID14 (). 1 = secure access. 0 : non secure access.
29	R/W	0	trigger type selection for subID13 (). 1 = secure access. 0 : non secure access
28	R/W	0	trigger type selection for subID12 (). 1 = secure access. 0 : non secure access
27	R/W	0	trigger type selection for subID11 (). 1 = secure access. 0 : non secure access
26	R/W	0	trigger type selection for subID10 (t). 1 = secure access. 0 : non secure access
25	R/W	0	trigger type selection for subID9 (). 1 = secure access. 0 : non secure access
24	R/W	0	trigger type selection for subID8 (). 1 = secure access. 0 : non secure access
23	R/W	0	trigger type selection for subID7 (). 1 = secure access. 0 : non secure access
22	R/W	0	trigger type selection for subID6 (). 1 = secure access. 0 : non secure access
21	R/W	0	trigger type selection for subID5 (). 1 = secure access. 0 : non secure access
20	R/W	0	trigger type selection for subID4 (). 1 = secure access. 0 : non secure access
19	R/W	0	trigger type selection for subID3 (). 1 = secure access. 0 : non secure access
18	R/W	0	trigger type selection for subID2 (). 1 = secure access. 0 : non secure access.
17	R/W	0	trigger type selection for subID1 (). 1 = secure access. 0 : non secure access.
16	R/W	0	trigger type selection for subID0 (). 1 = secure access. 0 : non secure access
15	R/W	0	trigger source selection for subID15 (). 1 = selected. 0 : not selected.
14	R/W	0	trigger source selection for subID14 (). 1 = selected. 0 : not selected.
13	R/W	0	trigger source selection for subID13 (). 1 = selected. 0 : not selected..
12	R/W	0	trigger source selection for subID12 (). 1 = selected. 0 : not selected..
11	R/W	0	trigger source selection for subID11 (). 1 = selected. 0 : not selected.
10	R/W	0	trigger source selection for subID10 (). 1 = selected. 0 : not selected..
9	R/W	0	trigger source selection for subID9 (). 1 = selected. 0 : not selected..
8	R/W	0	trigger source selection for subID8 (). 1 = selected. 0 : not selected.
7	R/W	0	trigger source selection for subID7 (). 1 = selected. 0 : not selected.
6	R/W	0	trigger source selection for subID6 (). 1 = selected. 0 : not selected.
5	R/W	0	trigger source selection for subID5 (). 1 = selected. 0 : not selected..
4	R/W	0	trigger source selection for subID4 (). 1 = selected. 0 : not selected.
3	R/W	0	trigger source selection for subID3 (). 1 = selected. 0 : not selected.
2	R/W	0	trigger source selection for subID2 (). 1 = selected. 0 : not selected..
1	R/W	0	trigger source selection for subID1 (). 1 = selected. 0 : not selected..
0	R/W	0	trigger source selection for subID0 (). 1 = selected. 0 : not selected.

DMC_VPU_EF0_PROT **0x27**

To define which subID would be affected after the EF got triggered.

Bit(s)	R/W	Default	Description
31	R/W	0	EF would affect subID15 () write access secure control. 1 = selected. 0 : not selected. .
30	R/W	0	EF would affect subID14 () write access secure control. 1 = selected. 0 : not selected.
29	R/W	0	EF would affect subID13 () write access secure control. 1 = selected. 0 : not selected.
28	R/W	0	EF would affect subID12 () write access secure control. 1 = selected. 0 : not selected.
27	R/W	0	EF would affect subID11 () write access secure control. 1 = selected. 0 : not selected.
26	R/W	0	EF would affect subID10 () write access secure control. 1 = selected. 0 : not selected.
25	R/W	0	EF would affect subID9 () write access secure control. 1 = selected. 0 : not selected.
24	R/W	0	EF would affect subID8 () write access secure control. 1 = selected. 0 : not selected.
23	R/W	0	EF would affect subID7 () write access secure control. 1 = selected. 0 : not selected.
22	R/W	0	EF would affect subID6 () write access secure control. 1 = selected. 0 : not selected.
21	R/W	0	EF would affect subID5 () write access secure control. 1 = selected. 0 : not selected.
20	R/W	0	EF would affect subID4 () write access secure control. 1 = selected. 0 : not selected.
19	R/W	0	EF would affect subID3 () write access secure control. 1 = selected. 0 : not selected.
18	R/W	0	EF would affect subID2 () write access secure control. 1 = selected. 0 : not selected.
17	R/W	0	EF would affect subID1 () write access secure control. 1 = selected. 0 : not selected.
16	R/W	0	EF would affect subID0 () write access secure control. 1 = selected. 0 : not selected.
15	R/W	0	EF would affect subID15 () read access secure control. 1 = selected. 0 : not selected. .
14	R/W	0	EF would affect subID14 () read access secure control. 1 = selected. 0 : not selected.
13	R/W	0	EF would affect subID13 () read access secure control. 1 = selected. 0 : not selected.

Bit(s)	R/W	Default	Description
12	R/W	0	EF would affect subID12 () read access secure control. 1 = selected. 0 : not selected.
11	R/W	0	EF would affect subID11 () read access secure control. 1 = selected. 0 : not selected.
10	R/W	0	EF would affect subID10 () read access secure control. 1 = selected. 0 : not selected.
9	R/W	0	EF would affect subID9 () read access secure control. 1 = selected. 0 : not selected.
8	R/W	0	EF would affect subID8 () read access secure control. 1 = selected. 0 : not selected.
7	R/W	0	EF would affect subID7 () read access secure control. 1 = selected. 0 : not selected.
6	R/W	0	EF would affect subID6 () read access secure control. 1 = selected. 0 : not selected.
5	R/W	0	EF would affect subID5 () read access secure control. 1 = selected. 0 : not selected.
4	R/W	0	EF would affect subID4 () read access secure control. 1 = selected. 0 : not selected.
3	R/W	0	EF would affect subID3 () read access secure control. 1 = selected. 0 : not selected.
2	R/W	0	EF would affect subID2 ()read access secure control. 1 = selected. 0 : not selected.
1	R/W	0	EF would affect subID1 () read access secure control. 1 = selected. 0 : not selected.
0	R/W	0	EF would affect subID0 () read access secure control. 1 = selected. 0 : not selected.

DMC_VPU_EF0_READ 0x28

This register contains the VPU read security control Bits after the EF got triggered. If the DMC_VPU_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_VPU_SEC_READ_CTRL related Bits.

DMC_VPU_EF0_WRITE 0x29

This register contains the VPU write security control Bits after the EF got triggered. If the DMC_VPU_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_VPU_SEC_WRITE _CTRL related Bits.

DMC_VPU_EF1_TRIG_CTRL 0x2a

VPU Electronic fence trigger selection and trigger secure type. 1 bit for trigger select for one read port. 1 bit for trigger type for one read port. Electronic fence would be triggered by the read from defined secure level from selected subIDs

Bit(s)	R/W	Default	Description
31	R/W	0	trigger type selection for subID15 (). 1 = secure access. 0 : non secure access.
30	R/W	0	trigger type selection for subID14 (). 1 = secure access. 0 : non secure access.
29	R/W	0	trigger type selection for subID13 (). 1 = secure access. 0 : non secure access
28	R/W	0	trigger type selection for subID12 (). 1 = secure access. 0 : non secure access
27	R/W	0	trigger type selection for subID11 (). 1 = secure access. 0 : non secure access
26	R/W	0	trigger type selection for subID10 (t). 1 = secure access. 0 : non secure access
25	R/W	0	trigger type selection for subID9 (). 1 = secure access. 0 : non secure access
24	R/W	0	trigger type selection for subID8 (). 1 = secure access. 0 : non secure access
23	R/W	0	trigger type selection for subID7 (). 1 = secure access. 0 : non secure access
22	R/W	0	trigger type selection for subID6 (). 1 = secure access. 0 : non secure access
21	R/W	0	trigger type selection for subID5 (). 1 = secure access. 0 : non secure access
20	R/W	0	trigger type selection for subID4 (). 1 = secure access. 0 : non secure access
19	R/W	0	trigger type selection for subID3 (). 1 = secure access. 0 : non secure access
18	R/W	0	trigger type selection for subID2 (). 1 = secure access. 0 : non secure access.
17	R/W	0	trigger type selection for subID1 (). 1 = secure access. 0 : non secure access.
16	R/W	0	trigger type selection for subID0 (). 1 = secure access. 0 : non secure access
15	R/W	0	trigger source selection for subID15 (). 1 = selected. 0 : not selected.
14	R/W	0	trigger source selection for subID14 (). 1 = selected. 0 : not selected.
13	R/W	0	trigger source selection for subID13 (). 1 = selected. 0 : not selected..
12	R/W	0	trigger source selection for subID12 (). 1 = selected. 0 : not selected..
11	R/W	0	trigger source selection for subID11 (). 1 = selected. 0 : not selected.
10	R/W	0	trigger source selection for subID10 (). 1 = selected. 0 : not selected..
9	R/W	0	trigger source selection for subID9 (). 1 = selected. 0 : not selected..
8	R/W	0	trigger source selection for subID8 (). 1 = selected. 0 : not selected.
7	R/W	0	trigger source selection for subID7 (). 1 = selected. 0 : not selected.
6	R/W	0	trigger source selection for subID6 (). 1 = selected. 0 : not selected.
5	R/W	0	trigger source selection for subID5 (). 1 = selected. 0 : not selected..
4	R/W	0	trigger source selection for subID4 (). 1 = selected. 0 : not selected.

Bit(s)	R/W	Default	Description
3	R/W	0	trigger source selection for subID3 (). 1 = selected. 0 : not selected.
2	R/W	0	trigger source selection for subID2 (). 1 = selected. 0 : not selected..
1	R/W	0	trigger source selection for subID1 (). 1 = selected. 0 : not selected..
0	R/W	0	trigger source selection for subID0 (). 1 = selected. 0 : not selected.

DMC_VPU_EF1_PROT 0x2b

To define which subID would be affected after the EF got triggered.

Bit(s)	R/W	Default	Description
31	R/W	0	EF would affect subID15 () write access secure control. 1 = selected. 0 : not selected. .
30	R/W	0	EF would affect subID14 () write access secure control. 1 = selected. 0 : not selected.
29	R/W	0	EF would affect subID13 () write access secure control. 1 = selected. 0 : not selected.
28	R/W	0	EF would affect subID12 () write access secure control. 1 = selected. 0 : not selected.
27	R/W	0	EF would affect subID11 () write access secure control. 1 = selected. 0 : not selected.
26	R/W	0	EF would affect subID10 () write access secure control. 1 = selected. 0 : not selected.
25	R/W	0	EF would affect subID9 () write access secure control. 1 = selected. 0 : not selected.
24	R/W	0	EF would affect subID8 () write access secure control. 1 = selected. 0 : not selected.
23	R/W	0	EF would affect subID7 () write access secure control. 1 = selected. 0 : not selected.
22	R/W	0	EF would affect subID6 () write access secure control. 1 = selected. 0 : not selected.
21	R/W	0	EF would affect subID5 () write access secure control. 1 = selected. 0 : not selected.
20	R/W	0	EF would affect subID4 () write access secure control. 1 = selected. 0 : not selected.
19	R/W	0	EF would affect subID3 () write access secure control. 1 = selected. 0 : not selected.
18	R/W	0	EF would affect subID2 () write access secure control. 1 = selected. 0 : not selected.
17	R/W	0	EF would affect subID1 () write access secure control. 1 = selected. 0 : not selected.
16	R/W	0	EF would affect subID0 () write access secure control. 1 = selected. 0 : not selected.
15	R/W	0	EF would affect subID15 () read access secure control. 1 = selected. 0 : not selected. .
14	R/W	0	EF would affect subID14 () read access secure control. 1 = selected. 0 : not selected.
13	R/W	0	EF would affect subID13 () read access secure control. 1 = selected. 0 : not selected.
12	R/W	0	EF would affect subID12 () read access secure control. 1 = selected. 0 : not selected.
11	R/W	0	EF would affect subID11 () read access secure control. 1 = selected. 0 : not selected.
10	R/W	0	EF would affect subID10 () read access secure control. 1 = selected. 0 : not selected.
9	R/W	0	EF would affect subID9 () read access secure control. 1 = selected. 0 : not selected.
8	R/W	0	EF would affect subID8 () read access secure control. 1 = selected. 0 : not selected.
7	R/W	0	EF would affect subID7 () read access secure control. 1 = selected. 0 : not selected.
6	R/W	0	EF would affect subID6 () read access secure control. 1 = selected. 0 : not selected.
5	R/W	0	EF would affect subID5 () read access secure control. 1 = selected. 0 : not selected.
4	R/W	0	EF would affect subID4 () read access secure control. 1 = selected. 0 : not selected.
3	R/W	0	EF would affect subID3 () read access secure control. 1 = selected. 0 : not selected.
2	R/W	0	EF would affect subID2 ()read access secure control. 1 = selected. 0 : not selected.
1	R/W	0	EF would affect subID1 () read access secure control. 1 = selected. 0 : not selected.
0	R/W	0	EF would affect subID0 () read access secure control. 1 = selected. 0 : not selected.

DMC_VPU_EF1_READ 0x2c

This register contains the VPU read security control Bits after the EF got triggered. If the DMC_VPU_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_VPU_SEC_READ_CTRL related Bits.

DMC_VPU_EF1_WRITE 0x2d

This register contains the VPU write security control Bits after the EF got triggered. If the DMC_VPU_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_VPU_SEC_WRITE _CTRL related Bits.

DMC_VPU_EF2_TRIG_CTRL 0x2e

VPU Electronic fence trigger selection and trigger secure type. 1 bit for trigger select for one read port. 1 bit for trigger type for one read port. Electronic fence would be triggered by the read from defined secure level from selected subIDs

Bit(s)	R/W	Default	Description
31	R/W	0	trigger type selection for subID15 (). 1 = secure access. 0 : non secure access.

Bit(s)	R/W	Default	Description
30	R/W	0	trigger type selection for subID14 (). 1 = secure access. 0 : non secure access.
29	R/W	0	trigger type selection for subID13 (). 1 = secure access. 0 : non secure access
28	R/W	0	trigger type selection for subID12 (). 1 = secure access. 0 : non secure access
27	R/W	0	trigger type selection for subID11 (). 1 = secure access. 0 : non secure access
26	R/W	0	trigger type selection for subID10 (t). 1 = secure access. 0 : non secure access
25	R/W	0	trigger type selection for subID9 (). 1 = secure access. 0 : non secure access
24	R/W	0	trigger type selection for subID8 (). 1 = secure access. 0 : non secure access
23	R/W	0	trigger type selection for subID7 (). 1 = secure access. 0 : non secure access
22	R/W	0	trigger type selection for subID6 (). 1 = secure access. 0 : non secure access
21	R/W	0	trigger type selection for subID5 (). 1 = secure access. 0 : non secure access
20	R/W	0	trigger type selection for subID4 (). 1 = secure access. 0 : non secure access
19	R/W	0	trigger type selection for subID3 (). 1 = secure access. 0 : non secure access
18	R/W	0	trigger type selection for subID2 (). 1 = secure access. 0 : non secure access.
17	R/W	0	trigger type selection for subID1 (). 1 = secure access. 0 : non secure access.
16	R/W	0	trigger type selection for subID0 (). 1 = secure access. 0 : non secure access
15	R/W	0	trigger source selection for subID15 (). 1 = selected. 0 : not selected.
14	R/W	0	trigger source selection for subID14 (). 1 = selected. 0 : not selected.
13	R/W	0	trigger source selection for subID13 (). 1 = selected. 0 : not selected..
12	R/W	0	trigger source selection for subID12 (). 1 = selected. 0 : not selected..
11	R/W	0	trigger source selection for subID11 (). 1 = selected. 0 : not selected.
10	R/W	0	trigger source selection for subID10 (). 1 = selected. 0 : not selected..
9	R/W	0	trigger source selection for subID9 (). 1 = selected. 0 : not selected..
8	R/W	0	trigger source selection for subID8 (). 1 = selected. 0 : not selected.
7	R/W	0	trigger source selection for subID7 (). 1 = selected. 0 : not selected.
6	R/W	0	trigger source selection for subID6 (). 1 = selected. 0 : not selected.
5	R/W	0	trigger source selection for subID5 (). 1 = selected. 0 : not selected..
4	R/W	0	trigger source selection for subID4 (). 1 = selected. 0 : not selected.
3	R/W	0	trigger source selection for subID3 (). 1 = selected. 0 : not selected.
2	R/W	0	trigger source selection for subID2 (). 1 = selected. 0 : not selected..
1	R/W	0	trigger source selection for subID1 (). 1 = selected. 0 : not selected..
0	R/W	0	trigger source selection for subID0 (). 1 = selected. 0 : not selected.

DMC_VPU_EF2_PROT **0x2f**

To define which subID would be affected after the EF got triggered.

Bit(s)	R/W	Default	Description
31	R/W	0	EF would affect subID15 () write access secure control. 1 = selected. 0 : not selected. .
30	R/W	0	EF would affect subID14 () write access secure control. 1 = selected. 0 : not selected.
29	R/W	0	EF would affect subID13 () write access secure control. 1 = selected. 0 : not selected.
28	R/W	0	EF would affect subID12 () write access secure control. 1 = selected. 0 : not selected.
27	R/W	0	EF would affect subID11 () write access secure control. 1 = selected. 0 : not selected.
26	R/W	0	EF would affect subID10 () write access secure control. 1 = selected. 0 : not selected.
25	R/W	0	EF would affect subID9 () write access secure control. 1 = selected. 0 : not selected.
24	R/W	0	EF would affect subID8 () write access secure control. 1 = selected. 0 : not selected.
23	R/W	0	EF would affect subID7 () write access secure control. 1 = selected. 0 : not selected.
22	R/W	0	EF would affect subID6 () write access secure control. 1 = selected. 0 : not selected.
21	R/W	0	EF would affect subID5 () write access secure control. 1 = selected. 0 : not selected.
20	R/W	0	EF would affect subID4 () write access secure control. 1 = selected. 0 : not selected.
19	R/W	0	EF would affect subID3 () write access secure control. 1 = selected. 0 : not selected.
18	R/W	0	EF would affect subID2 () write access secure control. 1 = selected. 0 : not selected.
17	R/W	0	EF would affect subID1 () write access secure control. 1 = selected. 0 : not selected.
16	R/W	0	EF would affect subID0 () write access secure control. 1 = selected. 0 : not selected.
15	R/W	0	EF would affect subID15 () read access secure control. 1 = selected. 0 : not selected. .
14	R/W	0	EF would affect subID14 () read access secure control. 1 = selected. 0 : not selected.
13	R/W	0	EF would affect subID13 () read access secure control. 1 = selected. 0 : not selected.

Bit(s)	R/W	Default	Description
12	R/W	0	EF would affect subID12 () read access secure control. 1 = selected. 0 : not selected.
11	R/W	0	EF would affect subID11 () read access secure control. 1 = selected. 0 : not selected.
10	R/W	0	EF would affect subID10 () read access secure control. 1 = selected. 0 : not selected.
9	R/W	0	EF would affect subID9 () read access secure control. 1 = selected. 0 : not selected.
8	R/W	0	EF would affect subID8 () read access secure control. 1 = selected. 0 : not selected.
7	R/W	0	EF would affect subID7 () read access secure control. 1 = selected. 0 : not selected.
6	R/W	0	EF would affect subID6 () read access secure control. 1 = selected. 0 : not selected.
5	R/W	0	EF would affect subID5 () read access secure control. 1 = selected. 0 : not selected.
4	R/W	0	EF would affect subID4 () read access secure control. 1 = selected. 0 : not selected.
3	R/W	0	EF would affect subID3 () read access secure control. 1 = selected. 0 : not selected.
2	R/W	0	EF would affect subID2 ()read access secure control. 1 = selected. 0 : not selected.
1	R/W	0	EF would affect subID1 () read access secure control. 1 = selected. 0 : not selected.
0	R/W	0	EF would affect subID0 () read access secure control. 1 = selected. 0 : not selected.

DMC_VPU_EF2_READ 0x30

This register contains the VPU read security control Bits after the EF got triggered. If the DMC_VPU_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_VPU_SEC_READ_CTRL related Bits.

DMC_VPU_EF2_WRITE 0x31

This register contains the VPU write security control Bits after the EF got triggered. If the DMC_VPU_EF_PROT register Bit 15:0 related bit was enabled, then the related secure control Bits would be copied to DMC_VPU_SEC_WRITE _CTRL related Bits.

DMC_GE2D_SEC_CTRL 0x34

GE2D is ambus port 7. There's only 2 read subID and 1 write subID for GE2D ports. Used one

Bit(s)	R/W	Default	Description
31~22	R/W	0	Not used.
21~16	R/W	0	GE2D secure control after EF triggered.
14	R/W	0	GE2D EF protection selection after EF triggered for write.
13	R/W	0	GE2d EF protection selection after EF triggered for source 1
12	R/W	0	GE2d EF protection selection after EF triggered for source 0
11:10	R/W	0	trigger type selection for 2 source. 1 : secure. 0 : unsecure.
9:8	R/W	0	Trigger source selection for 2 source.
7:6	R/W	0	Not used.
5	R/W	0	Secure enable for GE2D write. 1 = enable. 0 = disable.
4	R/W	0	Non-Secure enable for GE2D write. 1 = enable. 0 = disable.
3	R/W	0	Secure enable for GE2D read source 1. 1 = enable. 0 = disable.
2	R/W	0	Non-Secure enable for GE2D read source 1. 1 = enable. 0 = disable.
1	R/W	0	Secure enable for GE2D read source 0. 1 = enable. 0 = disable.
0	R/W	0	Non-Secure enable for GE2D read source 0. 1 = enable. 0 = disable.

DMC_PARSER_SEC_CTRL 0x35

Parser is in device port with the subID == 9

Bit(s)	R/W	Default	Description
31~12	R/W	0	Not used.
11:8	R/W	0	Parser write and read security control Bits after EF triggerd.
7	R/W	0	Parser EF protection selection Parser write.
6	R/W	0	Parser EF protection selection for Parser read.
5	R/W	0	Parser EF trigger read type 1 : secure. 0: unsecure.
4	R/W	0	Parser eF trigger read enable. 1 : enable 0 : disable.
3:2	R/W	0	Parser write security control Bits.
1:0	R/W	0	Parser read security control Bits.

DMC_DEVICE_SEC_READ_CTRL 0x36

Bit(s)	R/W	Default	Description
31	R/W	0	DEVICE subID15 () secure region read access enable bit. 1: enable. 0 : disable.

Bit(s)	R/W	Default	Description
30	R/W	0	DEVICE subID15 (non secure region read access enable bit. 1: enable. 0 : disable.
29	R/W	0	DEVICE subID14 (SANA) secure region read access enable bit. 1: enable. 0 : disable.
28	R/W	0	DEVICE subID14 (SANA) non secure region read access enable bit. 1: enable. 0 : disable.
27	R/W	0	DEVICE subID13 (ETH) secure region read access enable bit. 1: enable. 0 : disable.
26	R/W	0	DEVICE subID13 (ETH) non secure region read access enable bit. 1: enable. 0 : disable.
25	R/W	0	DEVICE subID12 (SPICC) secure region read access enable bit. 1: enable. 0 : disable.
24	R/W	0	DEVICE subID12 (SPICC) non secure region read access enable bit. 1: enable. 0 : disable.
23	R/W	0	DEVICE subID11 (SD_EMMC_C) secure region read access enable bit. 1: enable. 0 : disable.
22	R/W	0	DEVICE subID11 (SD_EMMC_C) non secure region read access enable bit. 1: enable. 0 : disable.
21	R/W	0	DEVICE subID10 (M3 CPU) secure region read access enable bit. 1: enable. 0 : disable.
20	R/W	0	DEVICE subID10 (M3 CPU) non secure region read access enable bit. 1: enable. 0 : disable.
19	R/W	0	Not used.
18	R/W	0	Not used.
17	R/W	0	DEVICE subID8 (AIU.) secure region read access enable bit. 1: enable. 0 : disable.
16	R/W	0	DEVICE subID8 (AIU) non secure region read access enable bit. 1: enable. 0 : disable.
15	R/W	0	DEVICE subID7 (AUDIN) secure region read access enable bit. 1: enable. 0 : disable.
14	R/W	0	DEVICE subID7 (AUDIN) non secure region read access enable bit. 1: enable. 0 : disable..
13	R/W	0	DEVICE subID6 (AUDOUT) secure region read access enable bit. 1: enable. 0 : disable.
12	R/W	0	DEVICE subID6 (AUDOUT) non secure region read access enable bit. 1: enable. 0 : disable.
11	R/W	0	DEVICE subID5 (USB1) secure region read access enable bit. 1: enable. 0 : disable.
10	R/W	0	DEVICE subID5 (USB1) non secure region read access enable bit. 1: enable. 0 : disable.
9	R/W	0	DEVICE subID4 (SD_EMMC_B) secure region read access enable bit. 1: enable. 0 : disable.
8	R/W	0	DEVICE subID4 (SD_EMMC_B) non secure region read access enable bit. 1: enable. 0 : disable.
7	R/W	0	DEVICE subID3 (ARB0) secure region read access enable bit. 1: enable. 0 : disable.
6	R/W	0	DEVICE subID3 (ARB0) non secure region read access enable bit. 1: enable. 0 : disable.
5	R/W	0	DEVICE subID2 (BLKMV) secure region read access enable bit. 1: enable. 0 : disable.
4	R/W	0	DEVICE subID2 (BLKMV) non secure region read access enable bit. 1: enable. 0 : disable.
3	R/W	0	DEVICE subID1 (USB0) secure region read access enable bit. 1: enable. 0 : disable.
2	R/W	0	DEVICE subID1 (USB0) non secure region read access enable bit. 1: enable. 0 : disable.
1	R/W	0	DEVICE subID0 (SD_EMMC_A) secure region read access enable bit. 1: enable. 0 : disable.
0	R/W	0	DEVICE subID0 (SD_EMMC_A) non secure region read access enable bit. 1: enable. 0 : disable.

DMC_DEVICE_SEC_WRITE _CTRL 0x37

Bit(s)	R/W	Default	Description
31	R/W	0	DEVICE subID15 () secure region write access enable bit. 1: enable. 0 : disable.
30	R/W	0	DEVICE subID15 (non secure region write access enable bit. 1: enable. 0 : disable.
29	R/W	0	DEVICE subID14 (SANA) secure region write access enable bit. 1: enable. 0 : disable.
28	R/W	0	DEVICE subID14 (SANA) non secure region write access enable bit. 1: enable. 0 : disable.
27	R/W	0	DEVICE subID13 (ETH) secure region write access enable bit. 1: enable. 0 : disable.
26	R/W	0	DEVICE subID13 (ETH) non secure region write access enable bit. 1: enable. 0 : disable.
25	R/W	0	DEVICE subID12 (SPICC) secure region write access enable bit. 1: enable. 0 : disable.
24	R/W	0	DEVICE subID12 (SPICC) non secure region write access enable bit. 1: enable. 0 : disable.
23	R/W	0	DEVICE subID11 (SD_EMMC_C) secure region write access enable bit. 1: enable. 0 : disable.
22	R/W	0	DEVICE subID11 (SD_EMMC_C) non secure region write access enable bit. 1: enable. 0 : disable.
21	R/W	0	DEVICE subID10 (M3 CPU) secure region write access enable bit. 1: enable. 0 : disable.
20	R/W	0	DEVICE subID10 (M3 CPU) non secure region write access enable bit. 1: enable. 0 : disable.
19	R/W	0	Not used.
18	R/W	0	Not used.
17	R/W	0	DEVICE subID8 (AIU.) secure region write access enable bit. 1: enable. 0 : disable.
16	R/W	0	DEVICE subID8 (AIU) non secure region write access enable bit. 1: enable. 0 : disable.
15	R/W	0	DEVICE subID7 (AUDIN) secure region write access enable bit. 1: enable. 0 : disable.
14	R/W	0	DEVICE subID7 (AUDIN) non secure region write access enable bit. 1: enable. 0 : disable..
13	R/W	0	DEVICE subID6 (AUDOUT) secure region write access enable bit. 1: enable. 0 : disable.
12	R/W	0	DEVICE subID6 (AUDOUT) non secure region write access enable bit. 1: enable. 0 : disable.

Bit(s)	R/W	Default	Description
11	R/W	0	DEVICE subID5 (USB1) secure region write access enable bit. 1: enable. 0 : disable.
10	R/W	0	DEVICE subID5 (USB1) non secure region write access enable bit. 1: enable. 0 : disable.
9	R/W	0	DEVICE subID4 (SD_EMMC_B) secure region write access enable bit. 1: enable. 0 : disable.
8	R/W	0	DEVICE subID4 (SD_EMMC_B) non secure region write access enable bit. 1: enable. 0 : disable.
7	R/W	0	DEVICE subID3 (ARB0) secure region write access enable bit. 1: enable. 0 : disable.
6	R/W	0	DEVICE subID3 (ARB0) non secure region write access enable bit. 1: enable. 0 : disable.
5	R/W	0	DEVICE subID2 (BLKMV) secure region write access enable bit. 1: enable. 0 : disable.
4	R/W	0	DEVICE subID2 (BLKMV) non secure region write access enable bit. 1: enable. 0 : disable.
3	R/W	0	DEVICE subID1 (USB0) secure region write access enable bit. 1: enable. 0 : disable.
2	R/W	0	DEVICE subID1 (USB0) non secure region write access enable bit. 1: enable. 0 : disable.
1	R/W	0	DEVICE subID0 (SD_EMMC_A) secure region write access enable bit. 1: enable. 0 : disable.
0	R/W	0	DEVICE subID0 (SD_EMMC_A) non secure region write access enable bit. 1: enable. 0 : disable.

DMC_DES_KEY0_HI 0x90

Bit(s)	R/W	Default	Description
31~0	R/W	0	DES KEY high 32Bits for unsecure region.

DMC_DES_KEY0_LO 0x91

Bit(s)	R/W	Default	Description
31~0	R/W	0	DES KEY low 32Bits for unsecure region.

DMC_DES_KEY1_HI 0x92

Bit(s)	R/W	Default	Description
31~0	R/W	0	DES KEY high 32Bits for secure region.

DMC_DES_KEY1_LO 0x93

Bit(s)	R/W	Default	Description
31~0	R/W	0	DES KEY low 32Bits for secure region.

DMC_DES_PADDING 0x9a

Bit(s)	R/W	Default	Description
31~0	R/W	0	32Bits address padding used for DES data generation.

DMC_CA_RMAP_L 0x9b

DMC_CA_RMAP_H 0x9c

There's a 4 Bits column address remap for the column address generation. Column address bit 9:6 would be remapped through this table.

Bit(s)	R/W	Default	Description
63:60	R/W	0	New address for input value 15.
59:56	R/W	0	New address for input value 14.
55:52	R/W	0	New address for input value 13.
51:48	R/W	0	New address for input value 12.
47:44	R/W	0	New address for input value 11.
43:40	R/W	0	New address for input value 10.
39:36	R/W	0	New address for input value 9.
35:32	R/W	0	New address for input value 8.
31:28	R/W	0	New address for input value 7.
27:24	R/W	0	New address for input value 6.
23:20	R/W	0	New address for input value 5.
19:16	R/W	0	New address for input value 4.
15:12	R/W	0	New address for input value 3.
11:7	R/W	0	New address for input value 2.
7:4	R/W	0	New address for input value 1.
3:0	R/W	0	New address for input value 0.

DMC_PROT0_RANGE **0xa0**

protection 0 address range. the range define is 64Kbyte boundary. current address [31:16] >= start address && current address [31:16] <= end address.

Bit(s)	R/W	Default	Description
31:16	R/W	0	Range end address
15:0	R/W	0	Range start address

DMC_PROT0_CTRL **0xa1**

Bit(s)	R/W	Default	Description
31:20	R/W	0	Not used.
19	R/W	0	protection 0 for write access enable bit.
18	R/W	0	protection 0 for read access enable bit.
17	R/W	0	protection 0 write access block function. if enabled, the access wouldn't write to the DDR SDRAM. if not enabled only generate a interrupt, but the access still wrote to DDR.
16	R/W	0	Not used.
15:0	R/W	0	Each Bit to enable one of the 16 ports for the protection function.

DMC_PROT1_RANGE **0xa2**

protection 1 address range. the range define is 64Kbyte boundary. current address [31:16] >= start address && current address [31:16] <= end address.

Bit(s)	R/W	Default	Description
31:16	R/W	0	Range end address
15:0	R/W	0	Range start address

DMC_PROT1_CTRL **0xa3**

Bit(s)	R/W	Default	Description
31:20	R/W	0	Not used.
19	R/W	0	protection 1 for write access enable bit.
18	R/W	0	protection 1 for read access enable bit.
17	R/W	0	protection 1 write access block function. if enabled, the access wouldn't write to the DDR SDRAM. if not enabled only generate a interrupt, but the access still wrote to DDR.
16	R/W	0	Not used.
15:0	R/W	0	Each Bit to enable one of the 16 ports for the protection function.

DMC_WTCH0_D0 **0xa4**

DMC_WTCH0_D1 **0xa5**

DMC_WTCH0_D2 **0xa6**

DMC_WTCH0_D3 **0xa7**

WTCH0 will watch upto 128Bits data access {d3, d2,d1,d0}

DMC_WTCH0_RANGE **0xa8**

Bit(s)	R/W	Default	Description
31:16	R/W	0	Range end address
15:0	R/W	0	Range start address

DMC_WATCH0_CTRL **0xa9**

Bit(s)	R/W	Default	Description
31:16	R/W	0	16Bits write data strb
15:0	R/W	0	16Bits input ports select

DMC_WATCH0_CTRL1 **0xaa**

Bit(s)	R/W	Default	Description
31:3	R/W	0	Not used
2	R/W	0	watch point 0 enable.

Bit(s)	R/W	Default	Description
1:0	R/W	0	watch point0 type. 2'b00 : double bytes. only watchpoint data 15:0 and data strb 1:0 is valid. 2'b01: 4 bytes. 2'b10: 8 bytes. 2'b11, all 16bytes.

DMC_WTCH1_D0 **0xab**

DMC_WTCH1_D1 **0xac**

DMC_WTCH1_D2 **0xad**

DMC_WTCH1_D3 **0xae**

WTCH0 will watch upto 128Bits data access {d3, d2,d1,d0}

DMC_WTCH1_RANGE **0xaf**

Bit(s)	R/W	Default	Description
31:16	R/W	0	Range end address
15:0	R/W	0	Range start address

DMC_WATCH1_CTRL **0xb0**

Bit(s)	R/W	Default	Description
31:16	R/W	0	16Bits write data strb
15:0	R/W	0	16Bits input ports select

DMC_WATCH0=1_CTRL1 **0xb1**

Bit(s)	R/W	Default	Description
31:3	R/W	0	Not used
2	R/W	0	watch point 1 enable.
1:0	R/W	0	watch point1 type. 2'b00 : double bytes. only watchpoint data 15:0 and data strb 1:0 is valid. 2'b01: 4 bytes. 2'b10: 8 bytes. 2'b11, all 16bytes.

DMC_TRAP0 _RANGE **0xb2**

trap function: all read access with predefined PORT or SubIDs must be in the predefine range. Other wire the read access would be blocked. And an error will be generated.

Bit(s)	R/W	Default	Description
31:16	R/W	0	Range end address
15:0	R/W	0	Range start address

DMC_TRAP0 _CTRL **0xb3**

Bit(s)	R/W	Default	Description
31	R/W	0	Not used.
30	R/W	0	Trap0 port ID 2 selection enable.
29	R/W	0	Trap0 port ID 1 selection enable.
28	R/W	0	Trap0 port ID 0 selection enable.
27	R/W	0	Trap0 port ID 2 subID selection enable.
26	R/W	0	Trap0 port ID 1 subID selection enable.
25	R/W	0	Trap0 port ID 0 subID selection enable.
23~20	R/W	0	Trap0 port port ID2 ID number.
19~16	R/W	0	Trap0 port port ID1 ID number.
15~12	R/W	0	Trap0 port port ID0 ID number.
11~8	R/W	0	Trap0 port port ID2 subID number.
7~4	R/W	0	Trap0 port port ID1 subID number.
3~0	R/W	0	Trap0 port port ID0 subID number.

DMC_TRAP1 _RANGE **0xb4**

trap function: all read access with predefined PORT or SubIDs must be in the predefine range. Other wire the read access would be blocked. And an error will be generated.

Bit(s)	R/W	Default	Description
31:16	R/W	0	Range end address
15:0	R/W	0	Range start address

DMC_TRAP1 _CTRL **0xb5**

Bit(s)	R/W	Default	Description
31	R/W	0	Not used.
30	R/W	0	Trap1 port ID 2 selection enable.
29	R/W	0	Trap1 port ID 1 selection enable.
28	R/W	0	Trap1 port ID 0 selection enable.
27	R/W	0	Trap1 port ID 2 subID selection enable.
26	R/W	0	Trap1 port ID 1 subID selection enable.
25	R/W	0	Trap1 port ID 0 subID selection enable.
23~20	R/W	0	Trap1 port port ID2 ID number.
19~16	R/W	0	Trap1 port port ID1 ID number.
15~12	R/W	0	Trap1 port port ID0 ID number.
11~8	R/W	0	Trap1 port port ID2 subID number.
7~4	R/W	0	Trap1 port port ID1 subID number.
3~0	R/W	0	Trap1 port port ID0 subID number.

DMC_SEC_STATUS **0xb6**

Bit(s)	R/W	Default	Description
31~4	R/W	0	Not used.
3	R/W	0	DDR channel 1 write secure violation.(secure, address over DDR size, trap violation, protection violation)
29	R/W	0	DDR channel 1 read secure violation.
28	R/W	0	DDR channel 0 write secure violation.
27	R/W	0	DDR channel 0 read secure violation.

DMC_VIO_ADDR0 **0xb7**

Bit(s)	R/W	Default	Description
31~0	R/W	0	DDR channel 0 write secure violation address.

DMC_VIO_ADDR1 **0xb8**

Bit(s)	R/W	Default	Description
31~23	R/W	0	Not used.
22	R/W	0	DDR channel 0 write secure check violation.
21	R/W	0	DDR channel 0 write protection 1 violation.
20	R/W	0	DDR Channel 0 write protection 0 vilation.
19	R/W	0	DDR channel 0 write watch 1 catch.
18	R/W	0	DDR channel 0 write watch 0 catch.
17	R/W	0	DDR channel 0 write address overflow. Write out of DDR size.
16~14	R/W	0	DDR channel 0 write violation AWPROT Bits.
13~0	R/W	0	DDR channel 0 write violation access ID.

DMC_VIO_ADDR2 **0xb9**

Bit(s)	R/W	Default	Description
31~0	R/W	0	DDR channel 1 write secure violation address.

DMC_VIO_ADDR3 **0xba**

Bit(s)	R/W	Default	Description
31~23	R/W	0	Not used.
22	R/W	0	DDR channel 1 write secure check violation.
21	R/W	0	DDR channel 1 write protection 1 violation.

Bit(s)	R/W	Default	Description
20	R/W	0	DDR Channel 1 write protection 0 vilation.
19	R/W	0	DDR channel 1 write watch 1 catch.
18	R/W	0	DDR channel 1 write watch 0 catch.
17	R/W	0	DDR channel 1 write address overflow. Write out of DDR size.
16~14	R/W	0	DDR channel 1 write violation AWPROT Bits.
13~0	R/W	0	DDR channel 1 write violation access ID.

DMC_VIO_ADDR4 0xbb

Bit(s)	R/W	Default	Description
31~0	R/W	0	DDR channel 0 read secure violation address.

DMC_VIO_ADDR5 0xbc

Bit(s)	R/W	Default	Description
31~23	R/W	0	Not used.
22	R/W	0	DDR channel 0 read secure check violation.
21	R/W	0	DDR channel 0 read protection 1 violation.
20	R/W	0	DDR Channel 0 read protection 0 vilation.
19	R/W	0	DDR channel 0 read trap1 violation
18	R/W	0	DDR channel 0 read trap 0 violation..
17	R/W	0	DDR channel 0 read address overflow. Write out of DDR size.
16~14	R/W	0	DDR channel 0 read violation ARPROT Bits.
13~0	R/W	0	DDR channel 0 read violation access ID.

DMC_VIO_ADDR6 0xbd

Bit(s)	R/W	Default	Description
31~0	R/W	0	DDR channel 1 read secure violation address.

DMC_VIO_ADDR7 0xbe

Bit(s)	R/W	Default	Description
31~23	R/W	0	Not used.
22	R/W	0	DDR channel 1 readsecure check violation.
21	R/W	0	DDR channel 1 read protection 1 violation.
20	R/W	0	DDR Channel 1 read protection 0 violation.
19	R/W	0	DDR channel 1 read trap1 violation..
18	R/W	0	DDR channel 1 read trap 0 violation. .
17	R/W	0	DDR channel 1 read address overflow. Write out of DDR size.
16~14	R/W	0	DDR channel 1 read violation AWPROT Bits.
13~0	R/W	0	DDR channel 1 read violation access ID.

DDR0_ADDRMAP_4 0xd4

For DDR channel 0, row, bank and rank address can be selected from any one of 32Bits linear address.

Since the DDR is at least 16Bits. So bit 0 of the 32Bits linear address is never used. So in this address map, if the value = 0, we'll treat This bit is not used.

Because we used the burst 8 for DDR3/LPDDR3/LPDDR2, so the column address[2:0] would be always 0.

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	30	rank select..
24~20	R/W	0	Bank address 3 (not used in DDR3/LPDDR3).
19~15	R/W	29	Bank address 2
14~10	R/W	13	Bank address 1
9~5	R/W	12	Bank address 0
4~0	R/W	0	Row address Bit 15.

DDR0_ADDRMAP_3 0xd3

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	28	Row address bit 14.
24~20	R/W	27	Row address bit 13.
19~15	R/W	26	Row address bit 12.
14~10	R/W	25	Row address bit 11.
9~5	R/W	24	Row address bit 10.
4~0	R/W	23	Row address bit 9..

DDR0_ADDRMAP_2 0xd2

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	22	Row address bit 8.
24~20	R/W	21	Row address bit 7.
19~15	R/W	20	Row address bit 16.
14~10	R/W	19	Row address bit 5.
9~5	R/W	18	Row address bit 4.
4~0	R/W	17	Row address bit 3.

DDR0_ADDRMAP_1 0xd1

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	16	Row address bit 2.
24~20	R/W	15	Row address bit 1.
19~15	R/W	14	Row address bit 0.
14~10	R/W	0	Column address bit 11.
9~5	R/W	0	Column address bit 10.
4~0	R/W	11	Column address bit 9.

DDR0_ADDRMAP_0 0xd0

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	10	Column address bit 8.
24~20	R/W	9	Column address bit 7.
19~15	R/W	8	Column address bit 6.
14~10	R/W	7	Column address bit 5.
9~5	R/W	6	Column address bit 4..
4~0	R/W	5	Column address bit 3..

DDR1_ADDRMAP_4 0xd9

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	30	rank select..
24~20	R/W	0	Bank address 3 (not used in DDR3/LPDDR3).
19~15	R/W	29	Bank address 2
14~10	R/W	13	Bank address 1
9~5	R/W	12	Bank address 0
4~0	R/W	0	Row address Bit 15.

DDR1_ADDRMAP_3 0xd8

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	28	Row address bit 14.
24~20	R/W	27	Row address bit 13.
19~15	R/W	26	Row address bit 12.
14~10	R/W	25	Row address bit 11.

Bit(s)	R/W	Default	Description
9~5	R/W	24	Row address bit 10.
4~0	R/W	23	Row address bit 9..

DDR1_ADDRMAP_2 **0xd7**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	22	Row address bit 8.
24~20	R/W	21	Row address bit 7.
19~15	R/W	20	Row address bit 16.
14~10	R/W	19	Row address bit 5.
9~5	R/W	18	Row address bit 4.
4~0	R/W	17	Row address bit 3.

DDR1_ADDRMAP_1 **0xd6**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	16	Row address bit 2.
24~20	R/W	15	Row address bit 1.
19~15	R/W	14	Row address bit 0.
14~10	R/W	0	Column address bit 11.
9~5	R/W	0	Column address bit 10.
4~0	R/W	11	Column address bit 9.

DDR1_ADDRMAP_0 **0xd5**

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~25	R/W	10	Column address bit 8.
24~20	R/W	9	Column address bit 7.
19~15	R/W	8	Column address bit 6.
14~10	R/W	7	Column address bit 5.
9~5	R/W	6	Column address bit 4..
4~0	R/W	4	Column address bit 3..

DMC_DDR_CTRL **0xda**

Bit(s)	R/W	Default	Description
31~23	R/W	0	Not used.
22	R/W	0	rank1 is same as rank0. only in not shared-AC mdoe. and chan0 second rank not selected. that's means still in rank0 32Bits mode.
21	R/W	0	channel0 second rank selection enable. only in not shared-AC mode.
20	R/W	0	Shared AC mode.
19	R/W	0	bit 19: DDR channel 1 16Bits data interface. 1 : 16Bits data inteface. 0 : 32Bits data interface . always 0.
18	R/W	0	bit 18: DDR channel 0 16Bits data interface.1 : 16Bits data inteface. 0 : 32Bits data interface. always 0
17	R/W	0	for DDR channel 1. 1: only use 16Bits data in a 32Bits phy data interface. 0: normal 32Bits data interface.
16	R/W	0	for DDR channel 0. 1 only use 16Bits data in a 32Bits phy data interface. 0 : normal data interface.
15~11	R/W	0	Not used.

Bit(s)	R/W	Default	Description
10~8	R/W	0	Channel select bit for shared_ac_mode. We can select one of linear address Bits 15 to 8 for the DDR channel select Bits. 3'b000: use bit8 for the channel select. bit 8 = 0 this access goes to channel 0. bit 8 = 1, this access goes to channel 1. 3'b001: use bit9 for the channel select. bit 9 = 0 this access goes to channel 0. bit 9 = 1, this access goes to channel 1. 3'b010: use bit10 for the channel select. bit 10 = 0 this access goes to channel 0. bit 10 = 1, this access goes to channel 1. 3'b011: use bit11 for the channel select. bit 11 = 0 this access goes to channel 0. bit 11 = 1, this access goes to channel 1. 3'b100: use bit12 for the channel select. bit 12 = 0 this access goes to channel 0. bit 12 = 1, this access goes to channel 1. 3'b101: use bit13 for the channel select. bit 13 = 0 this access goes to channel 0. bit 13 = 1, this access goes to channel 1. 3'b110: use bit14 for the channel select. bit 14 = 0 this access goes to channel 0. bit 14 = 1, this access goes to channel 1. 3'b111: use Bit 15 for the channel select. bit 15 = 0 this access goes to channel 0. bit 15 = 1, this access goes to channel 1. If (ddr0_size != ddr1_size && linear address <= 2*(minimum(ddr1_size, ddr0_size)) || ddr0_size == ddr1_size) use this channel select bit to select this address goes to DDR0 or DDR1. Else if (ddr0_size != ddr1_size && linear address > 2*(minimum(ddr1_size, ddr0_size))) This access goes to the ddr channel with bigger size.
7	R/W	0	DDR1_ONLY. 1: DDR channel 1 only. when both channel 0 and 1 in the design. 0 : normal.
6	R/W	0	DDR0_ONLY. 1: DDR channel 0 only. when both channel 0 and 1 in the design. 0 : normal.
5~3	R/W	0	DDR channel 1 size. 3'b000: DDR channel 1 : 128Mbyte. 3'b001: DDR channel 1 : 256Mbyte. 3'b010: DDR channel 1 : 512Mbyte. 3'b011: DDR channel 1 : 1GMbyte. 3'b100: DDR channel 1 : 2GMbyte.
2~0	R/W	0	DDR channel 0 size. 3'b000: DDR channel 0 : 128Mbyte. 3'b001: DDR channel 0 : 256Mbyte. 3'b010: DDR channel 0 : 512Mbyte. 3'b011: DDR channel 0 : 1GMbyte. 3'b100: DDR channel 0 : 2GMbyte.

DMC DDR Channel 0 DRAM register.

Base address 0xc8839000.

DMC DDR Channel 1 DRAM register.

Base address 0xc8839400.

MMC DDR PHY control register.

Base address 0xc8836800.

AM_DDR_PLL_CNTL **0x0**

Bit(s)	R/W	Default	Description
31	R	0	PLL lock status
30	R/W	0	PLL power down. 1 = PLL power down. 0 = PLL enable.
29	R/W	0	PLL reset.
28	R/W	0	SSEN
27~24	R/W	0	SS_AMP
23~20	R/W	0	SS_CLK
17~16	R/W	0	OD.
15~14	R/W	0	OD1

Bit(s)	R/W	Default	Description
13~9	R/W	0	N
8~0	R/W	0	M.

AM_DDR_PLL_CNTL1 0x1

Bit(s)	R/W	Default	Description
31~28	R/W	0	DPLL_LM_W
27~22	R/W	0	DPLL_LM_S
21	R/W	0	DPFD_LMODE
20~19	R/W	0	DC_VC_IN
18~17	R/W	0	DCO_SDMCK_SEL
16	R/W	0	DCO_M_EN
15	R/W	0	SDM_PR_EN.
14	R/W	0	DIV_MODE
13~2	R/W	0	DIV_FRAC
1	R/W	0	AFC_DSEL_BYPASS.
0	R/W	0	AFC_DSEL_IN

AM_DDR_PLL_CNTL2 0x2

Bit(s)	R/W	Default	Description
31~30	R/W	0	Not used.
29~26	R/W	0	FILTER_PVT2.
25~22	R/W	0	FILTER PVT1
21~11	R/W	0	FILTER ACQ2
10~0	R/W	0	FILTER ACQ1

AM_DDR_PLL_CNTL3 0x3

Bit(s)	R/W	Default	Description
31~20	R/W	0	DPLL_REVE
13~6	R/W	0	TDC_BUF.
5	R/W	0	PVT_FIX_EN.
4~3	R/W	0	DCO_IUP
2	R/W	0	IIR_BYPASS_N.
1	R/W	0	TDC_EN
0	R/W	0	Not used.

AM_DDR_PLL_CNTL4 0xc8836810

Bit(s)	R/W	Default	Description
31~22	R/W	0	Not used.
21~20	R/W	0	DPLL_CLK_EN
19~14	R/W	0	Not used.
13	R/W	0	DCO_SDM_EN
12	R/W	0	BGP_EN.
11~8	R/W	0	GPB_C
7~0	R/W	0	Not used.

AM_DDR_PLL_STS 0xc8836814

Bit(s)	R/W	Default	Description
31	R/W	0	DDR_PLL_LOCK
30~9	R/W	0	Not used.
8~1	R/W	0	DPLL_OUT_RSV
0	R/W	0	AFC_DONE

DDR_CLK_CNTL **0xc8836818**

Bit(s)	R/W	Default	Description
31	R/W	0	ddr_pll_clk enable. enable the clock from DDR_PLL to clock generation. whenever change the DDR_PLL frequency, disable the clock, after the DDR_PLL locked, then enable it again..
30	R/W	0	ddr_pll_prod_test_en. enable the clock to clock/32 which to clock frequency measurement and
29	R/W	0	ddr_phy_ctl_clk enable
28	R/W	0	clock generation logic soft reset. 0 = reset.
27	R/W	0	phy_4xclk phase inverter..
26	R/W	0	pll_freq divide/2. 1: use pll div/2 clock as the n_clk. 0: use pll clock as n_clk.
25~0	R/W	0	Not used.

DDR0_CLK_CNTL **0xc8836c00**

Bit(s)	R/W	Default	Description
31~4	R/W	0	Not used
3	R/W	0	force to disable PUB PCLK.production test pin.
2	R/W	0	PUB auto ctrl n_clk clock gating enable. when the DFI_LP_REQ and DFI_LP_ACK detected , auto gated PUB n_clk.
1	R/W	0	force to disable PUB PCLK.
0	R/W	0	PUB pclk auto clock gating enable. when the IP detected PCTL enter power down mode, use This bit to gating pub pclk.

DDR0_SOFT_RESET **0xc8836c04**

Bit(s)	R/W	Default	Description
31~4	R/W	0	Not used
3	R/W	0	PUB n_CLK domain soft reset. 1 : reset. 0 normal.
2	R/W	0	PUB p_CLk domain soft reset. 1: reset. 0 normal.
1	R/W	0	Not used.
0	R/W	0	Not used.

DDR0_APD_CTRL **0xc8836c08**

Bit(s)	R/W	Default	Description
31~16	R/W	0	Not used
15~8	R/W	0	power down enter latency. when IP checked the dfi_lp_req && dfi_lp_ack, give PCTL and pub additional latency let them settle down, then gating the clock.
7~0	R/W	0	no active latency. after c_active_in become to low, wait additional latency to check the pctl low power state.

DDR PHY PUB register.

Base address 0xc8836000. Please refer dwc_ddr_multiphy_g2_pubm2_databook.pdf.

33. NAND

33.1 Overview

S905 supports SLC/MLC/TLC NAND Flash with 60-bit ECC.

33.2 Register Definitions

The base address of NAND registers is 0xd0074000, and the final address of each register is listed below:

Table VI.33.1 NAND Register List

Register Name	Description	Address	R/W
P_NAND_CMD	Write Command and Read Status	Base + 0x00	R/W
P_NAND_CFG	Configuration	Base + 0x04	R/W
P_NAND_DADR	Data Address	Base + 0x08	R/W
P_NAND_IADR	Information Address	Base + 0x0c	R/W
P_NAND_BUF	Read Data Buffer	Base + 0x10	R
P_NAND_INFO	Information	Base + 0x14	R
P_NAND_DC	DDR interface	Base + 0x18	R
P_NAND_ADR	DDR Address	Base + 0x1c	R
P_NAND_DL	DDR Low 32 Bits Data	Base + 0x20	R/W
P_NAND_DH	DDR High 32 Bits Data	Base + 0x24	R/W
P_NAND_CADR	Command Queus Address	Base + 0x28	R/W
P_NAND_SADR	Status Address	Base + 0x2c	R/W
P_NAND_PINS	CS2: SDRAM/NAND pin sharing	Base + 0x30	R/W
P_NAND_VER	Version number	Base + 0x38	R

P_NAND_CMD

Write : Send NAND command to controller, the command format is specified in previous section.

Bit(s)	Name	Description
21:0	Cmd	NAND command sent to NAND queue buffer
30	Cmd_go	When 1, and NAND bus is in waiting Rb mode, due to time out or longer than expected Rb waiting, the command queue will move on by disable RB waiting in current command.
31	Cmd_reset	When 1 the NAND command queue buffer is reset to zero.

Read : Read NAND controller status

Bit(s)	Name	Description
19:0	Cmd_curr	NAND command current on NAND bus, still going, not finished.
24:20	Cmd_cnt	Number of NAND commands still in NAND command queue buffer, the buffer size is 32.
25	Timer out	When 1 wait Rb command timed out.
26	Rb0	Current Rb0 status, 1: ready, 0: busy.
27	Rb1	Current Rb1 status, 1: ready, 0: busy.
28	Rb2	Current Rb2 status, 1: ready, 0: busy.
29	Rb3	Current Rb3 status, 1: ready, 0: busy.
30	Mem_rdy	When 1, DDR interface is idle and ready to accept memory movement request.
31	Ecc_rdy	When 1, ECC BCH encoder/decoder is idle and read to accept encode or decode activity.

P_NAND_CFG

Bit(s)	Name	Description
4:0	Bus_cyc	The number of system clock cycles in one NAND cycle – 1, for example, if the bus_cyc is 3, then the NAND cycle is 4 system clock cycles, the minimum setting is 3, the maximum setting is 31. program this register according NAND timing mode.
9:5	Bus_tim	The timing to lock the NAND data when read NAND data or status, please refer to "Timing Calculator" for details.
11:10	Sync	00: Async mode 01: Micron Sync mode 10: Toshiba-Samsung toggle mode
12	Cmd_start	When set to "1", if the NAND controller internal 32 command buffer has less than 16 commands, the command DMA starts reading commands from DDR and saves them to internal buffer, the DMA keeps watching the internal buffer, reads whenever there are less than 16 commands left, if an all "zero" command is met, This bit is cleared and current command DMA is done.

13	Cmd_auto	When set to ‘1’, the command DMA will check the previous command queue end location, whether it is changed from all “zero” back to valid command, the auto check period is 1 ms.
14	Apb_mode	Special NAND mode for ROM boot or debug, when 1, DDR interface is redirected to APB register, all the read/write activities are through APB registers. When used in ROM boot and DDR is not ready.
15	Spare_only	When 1, the NAND controller read NAND with/without ECC, but only save the information bytes into DDR memory, the main data is discarded, designed for software to survey the NAND flash spare bytes and prepare NAND programming.
16	Sync_adj	Used to adjust data timing in sync or toggle mode, 0: default timing, 1: delay 1 system clock cycle.
20	Sts_irq_en	Enable STS IRQ.
21	Cmd_irq_en	Enable RB pin or RB IO IRQ.
26	Oob_on	Set to 1 oob_mode 16/0, Set to 0 no oob bytes.
27	Oob_mode	New in M8 v2, Set to 1 enable new oob mode. First page 16 bytes, all other pages 0 byte.
28	Dc_ugt	Set NAND controller DDR interface to Urgent mode.
29	Nand_wpn	When 1, the NAND wpn pin is set to low, the NAND is in write protection mode, default to 0, the NAND is not protected.
30	Core_power	When 1, internal NAND controller core clock gating is override to always on. The clock gating is disabled.
31	Top_power	When 1, internal NAND top clock gating is override to always on, the clock gating for top is disabled.

P_NAND_DADR

Set DDR data address by registers, the address is 32 Bits, since the DDR data address can also be set by NAND commands, when both happens at the same time, register setting is ignored, the NAND command setting takes effect. Software should avoid conflict address setting.

P_NAND_IADR

Set DDR information (spare bytes) address by registers, the address is 32 Bits, since the DDR information address can also be set by NAND commands, when both happens at the same time, register setting is ignored, the NAND command setting takes effect. Software should avoid conflict address setting.

P_NAND_BUF

When read NAND status, features or data, the results are buffer in this register, the register is 32 Bits, it can only hold 4 bytes, if the host not doesn’t read out the results, it will be over written by the following “read”.

P_NAND_INFO

One 32 Bits information per each 512 bytes in ECC mode.

Bit(s)	Name	Description
7:0	Info 0	Information (spare) byte 0, errors already corrected by BCH.
15:8	Info 1	Information (spare) byte 1, errors already corrected by BCH
21:16	Pages	Count down page number in current DMA read, starts from the total page size, count down to 1.
28:24	Errcnt	Number of errors corrected by BCH in current page, 0 means no error in current page, 0x1f means this page is uncorrectable.
29	Unc	When 1, this page is uncorrectable by BCH, this page is bad.
30	Ecc	When 1, current NAND read is with ECC on.
31	Done	When 1, the information content and data read from NAND are valid, otherwise the “read” is not done.

P_NAND_DC

Used for apb_mode, internal NAND controller still uses DDR interface, only the DDR request and DDR grant are redirected from DDR to apb registers, this enables the host to read NAND without DDR, for ROM boot and debug.

Bit(s)	Name	Description

7:0	Dc_wr_dm	DDR write data mask, Each Bit masks one byte.
8	Dc_wr	When 1, write data from NAND to DDR. When 0, read data from DDR to NAND.
9	Dc_lbrst	When 1, the 64 Bits data is the last in current DDR burst, used with Dc_req.
10	Dc_ugt	When 1, current DDR request of read/write is urgent, in NAND controller, the Dc_ugt is set to 0, none-urgent.
11	Dc_req	When 1, the NAND controller send request to DDR to read or write data, in case of apb_mode, when dc_req is “1”, the host is responsible for send to or receive from NAND controller. Note: this is the only signal the host needs to check when in apb_mode.

P_NAND_ADR

32 Bits DDR address when NAND controller read or write to DDR memory, any address space within the DDR memory installed in the system is valid.

P_NAND_DL

The DDR interface uses 64 Bits width bus, this register is for low 32 Bits, [31:0].

P_NAND_DH

The DDR interface uses 64 Bits width bus, this register is for high 32 Bits, [63:32].
Read and write to this register will generate “grant” and “dc_wr_avail” or “dc_rd_avail”.

Always read or write low 32 Bits first, then read or write to high 32 Bits and NAND controller hardware will generate “grant” and “dc_wr_avail” or “dc_rd_avail”, combined with the data, the DDR address advances to next address.

NAND controller programs NAND flash in apb_mode:

- Check P_NAND_DC till “dc_req” is high.
- Write low 32 Bits to P_NAND_DL.
- Write high 32 Bits to P_NAND_DH.
- Go back to beginning till all the data is written.

NAND controller reads data from NAND flash in apb_mode:

- Check P_NAND_DC till “dc_req” is high.
- Read low 32 Bits from P_NAND_DL.
- Read high 32 Bits from P_NAND_DH.
- Go back to beginning till all the data is read.

Since the DDR interface in NAND controller process the data in group of 16 double words (64 Bits), the software can only check “dc_req” at the beginning of each 16 double words.

P_NAND_CADR

Set command queue memory address, 32 Bits, any memory location.
This address can only be programmed by APB bus.

P_NAND_SADR

Set status memory location, 32 Bits, any memory location.
This address can also be programmed through command queue.

P_NAND_PINS

Bit(s)	Name	Description
13:0	Pins_len	When pins are acquired by NAND, it will use Pins_len number of NAND bus cycles before releasing pins. Defult is 8.
27:14	Pins_off	When pins are released by NAND, it will wait Pins_off number of NAND bus cycles before sending next request. Default is 2.
31	Not shared	When 1 the pins is not shared, default is 0, pins are shared.

P_NAND_VER

Start from M8, NAND controller hardware version ID, 16 Bits year in hexadecimal, 8 Bits month in hexadecimal, maximum ECC in decimal.

Project	Version ID	Description
M6, M6TV older	0	N/A
M6TVlite	0x2012081e	Designed on Aug 2012, ECC 30
M8	0x2012083c	Designed on Aug 2012, ECC 60

34. eMMC/SD/SDIO

34.1 Overview

S905 has the following features of eMMC/SD/SDIO

- Supports SDSC/SDHC/SDXC card and SDIO specification version 2.x/3.x/4.x DS/HS modes up to UHS-I SDR104
- Supports eMMC and MMC card specification version 5.0 up to HS400 with data content DES crypto
- 1 bit, 4 Bits, 8 Bits date lines supported (8 Bits only for MMC)
- Descriptor chain architecture, timing tuning and adjustment
- Supports descriptor-based internal DMA controller

This module uses eMMC/SD/SDIO CONTROLLERs to connect varied SD/MMC Card, SDIO device (e.g. Wi-Fi module), or eMMC protocol compatible memory with high throughput.

34.2 Pin Description

Table VI.34.1 Pin Description of eMMC/SD/SDIO Module

Name	Type	Description	Speed (MHz)
CLK	Output	SD eMMC clock, 0~200MHz	200
DS	eMMC optional SD Card or SDIO not used Input (used as device IRQ in SDIO) R_{DS} pull-down used in HS400 mode.	Data Strobe, HS400 mode only	200
DAT[7:0]	SD Card/SDIO 4 Bits, eMMC 8 Bits Input/Output/Push-Pull Internal pull-up for pins not used	Data, 1,4,8 mode	200
CMD	Input/Output/Push-Pull/Open-Drain Open-drain for initialization Push-pull for fast command transfer R_{OD} is connected when in open-drain mode.	Command Response	100
Rst_n	eMMC required	Hardware reset	Low
IRQ	SDIO required SD Card or eMMC not used.	Device interrupt can be replaced by DAT[1]	Low

34.3 eMMC/SD Mode

eMMC Mode:

Table VI.34.2. eMMC Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer
Legacy MMC card	Single	3/1.8/1.2V	1, 4, 8	0-26MHz	26MB/s
High Speed SDR	Single	3/1.8/1.2V	1,4, 8	0-52MHz	52MB/s
High Speed DDR	Dual	3/1.8/1.2V	4, 8	0-52MHz	104MB/s
HS200	Single	1.8/1.2V	4, 8	0-200MHz	200MB/s
HS400 (highest)	Dual	1.8/1.2V	8	0-200MHz	400MB/s

The HS200 mode offers the following features:

- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 4 or 8-bits bus width supported
- Single ended signaling with 4 Drive Strengths
- Signaling levels of 1.8V and 1.2V
- Tuning concept for Read Operations

The HS400 mode has the following features

- DDR Data sampling method
- CLK frequency up to 200MHz, Data rate is up to 400MB/s
- Only 8-bit bus width supported
- Signaling levels of 1.8V and 1.2V
- Support up to 5 Drive Strengths
- Data strobe signal is toggled only for Data out and CRC response

SD Mode:

TableVI.34.3. SD Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer
Default Speed	Single	3.3V	1, 4	0-25MHz	12.5MB/s
High Speed	Single	3.3V	1, 4	0-50MHz	25MB/s
SDR12	Single	1.8V	1,4	0-25MHz	12.5MB/s
SDR25	Single	1.8V	1,4	0-50MHz	25MB/s
SDR50	Single	1.8V	1,4	0-100MHz	50MB/s
SDR104 (highest)	Single	1.8V	1,4	0-208MHz	104MB/s
DDR50	Dual	1.8V	4	0-50MHz	50MB/s

34.4 Clock

In S905, clock source has the options to select from the table below.

Table VI.34.4. Clock Sources

Clock source	Name	Frequency MHz	Note
0	Cts_oscin_clk	24	Default
1	Fclk_div2	1000	
2	Fclk_div3	667	
3	Fclk_div5	400	
4	Fclk_div7	286	
5	Mp2_clk_out	Programmable	
6	Mp3_clk_out	Programmable	
7	Gp0_pll_clk		

34.5 Descriptor

Descriptor Structure

The descriptor has a size of 4x32 Bits.

TableVI.34.5 Descriptor Structure

byte	7	6	5	4	3	2	1	0
0	length[7:0]							

<table>
<tr><td>1</td><td colspan="4">Timeout 4 Bits</td><td>End of chain</td><td>R1b</td><td>block mode</td><td>length[8]</td></tr>
<tr><td>2</td><td>data num</td><td>resp num</td><td>resp 128</td><td>resp nocrc</td><td>Data wr</td><td>Data io</td><td>No cmd</td><td>No resp</td></tr>
<tr><td>3</td><td>owner</td><td>error</td><td colspan="6">cmd index 6 Bits</td></tr>
<tr><td>4</td><td colspan="8" rowspan="4">cmd argument 32 Bits</td></tr>
<tr><td>5</td></tr>
<tr><td>6</td></tr>
<tr><td>7</td></tr>
<tr><td>8</td><td colspan="8" rowspan="4">data address 32 Bits or data 0-4 bytes
[1]Big Endian, [0]SRAM</td></tr>
<tr><td>9</td></tr>
<tr><td>10</td></tr>
<tr><td>11</td></tr>
<tr><td>12</td><td colspan="8" rowspan="4">response address 32 Bits or response irq en
[0]SRAM</td></tr>
<tr><td>13</td></tr>
<tr><td>14</td></tr>
<tr><td>15</td></tr>
</table>

Descriptor Definition

TableVI.34.5 Descriptor Definition

Name	Bits	Description
Length	Cmd_cfg[8:0]	same as spec, copy the content from command argument into this field, different byte size and 512 bytes, different number of blocks and infinite blocks. If the command is operating on bytes, block mode = 0, this field contains the number of bytes to read or write, A value of 0 shall cause 512 bytes to be read to written, if the command is operating on blocks, block mode = 1, this field contains the number of blocks, a value of 0 is infinite number of blocks.
Block_mode	Cmd_cfg[9]	1: the read or write shall be performed on block basis. The block size is from SD/eMMC device, and saved in APB3 register in module. 0: the read or write is byte based.
R1b	Cmd_cfg[10]	1: check the DAT0 busy after received response R1 0: do not check the DAT0 busy state.
End_of_chain	Cmd_cfg[11]	1: it is the end of descriptor chain, the host stops and issues IRQ after this descriptor is done. 0: the host reads next descriptor and continues. The command chain execution is started by write an APB3 register and stopped by the “end of chain” or clear a APB3 start register, or found one descriptor with owner is set to 0.
Timeout	Cmd_cfg[15:12]	$2^{timeout}$ ms when timeout != 0, max timeout 32.768s, when over the timeout limit, error bit is set, IRQ is issued. When timeout is 0, no time limit.
No_resp	Cmd_cfg[16]	1: this command doesn’t have response, used with command doesn’t have response. 0: there is a response. The module waits for response, the response timeout setting is in APB3 register.
No_cmd	Cmd_cfg[17]	1: this descriptor doesn’t have command in it, it does data DMA only, used with command to read or write SD/eMMC with data from multiple locations.
Data_io	Cmd_cfg[18]	1: there is data action in this descriptor, used with command have data process. 0: there is no data read/write action.
Data_wr	Cmd_cfg[19]	1: host writes data to SD/eMMC 0: host read data from SD/eMMC
Resp_nocrc	Cmd_cfg[20]	1: R3 response doesn’t have CRC. 0: host does CRC check.
Resp_128	Cmd_cfg[21]	1: R3 response with 128 Bits information. 0: 32 Bits responses.
Resp_num	Cmd_cfg[22]	1: the resp_addr is the IRQ enable Bits, used to check the response error status, when there is an error, IRQ[14] is issued, the first 4 bytes of response is saved into resp_addr.

		0: save response into SRAM or DDR location.
Data_num	Cmd_cfg[23]	1: save 4 bytes of data back into descriptor itself at bytes 8~11.
Cmd_index	Cmd_cfg[29:24]	The SD/eMMC command index. Desc REG wr: 4 reg44, 12 reg4c.
Error	Cmd_cfg[30]	Write back by host. The combined error from command, response, data, includes CRC error and timeout. When it is set the descriptor execution is stopped and an IRQ is issued. The CPU can read SD_EMMC_STATUS register to get detail information.
Owner	Cmd_cfg[31]	Programmed by CPU to 1, cleared by host to 0. 1: the descriptor is valid and owned by host, after it is done, even it has error, the owner bit is cleared, the descriptor is owned by CPU. In case of descriptor chain execution when host found a descriptor with “0” owner bit, it will stop.
Cmd_arg	Desc 4~7 bytes	32 Bits. The actual command argument some of the previous fields are copied from this command argument, the software need to make sure they are consistent. Desc REG wr: new value Data_addr: write mask, 1: change, 0: no change.
Data_addr	Desc 8~11 bytes	32 Bits. If the data_num is 0, the content is data address. If the data_num is 1, ths content is 4 data bytes. When it is an address: Data_addr[0]: 1: SRAM address, 0: DDR address. If the data_addr[31:12] matches with SD_EMMC_BASE, it is SRAM address. Data_addr[1]: 1: 4 bytes big endian, 0: little endian(default).
Resp_addr	Desc 12~15 bytes	32 Bits If the resp_num is 0, the content is resp address. If the resp_num is 1, before execution, it is the response IRQ enable Bits, after execution, it is the first 4 response bytes. When it is an address: Resp_addr[0]: 1: SRAM address, 0: DDR address. If the resp_addr[31:12] matches with SD_EMMC_BASE, it is SRAM address.

34.6 Timing Specification

FigureVI.34.1 MMC/SD/SDIO Timing Diagram

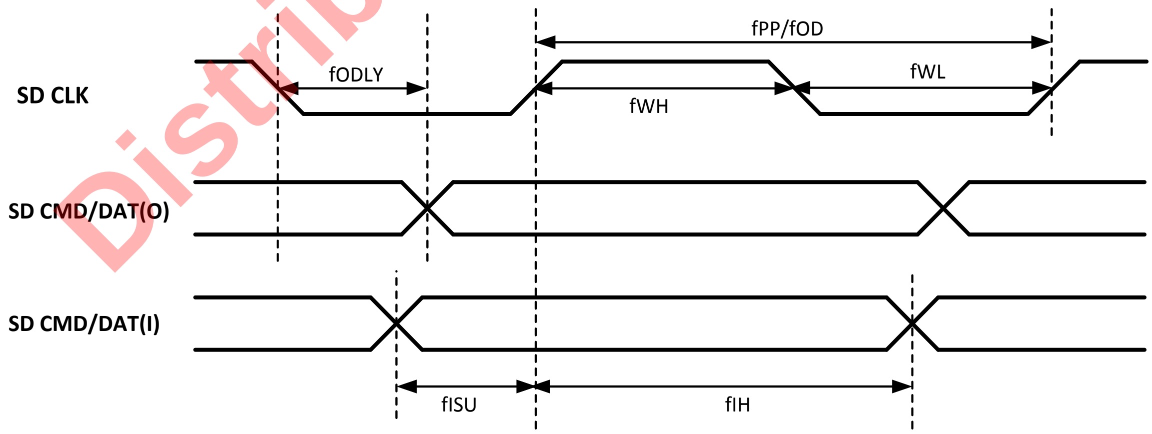


Table VI.34.6 SDHC Timing Specification

Symbol	Description	Min.	Max.	Unit	Notes
fPP	Clock Frequency Low Speed	0	400	KHz	
	Clock Frequency Full/High Speed	0	25/80	MHz	
	Clock Frequency UHS-I Speed	0	100	MHz	

fOD	Clock Frequency Identification Mode	100	400	KHz	
tWL	Clock Low Time	5		ns	
tWH	Clock High Time	5		ns	
tODLY	Output Delay	-2.5	2.5	ns	
tISU	Input Setup Time	4		ns	
tIH	Input Hold Time	4		ns	

Table VI.34.7 SDIO Timing Specification

Symbol	Description	Min.	Max.	Unit	Notes
fPP	Clock Frequency Low Speed	0	400	KHz	
	Clock Frequency Full/High Speed	0	25/50	MHz	
fOD	Clock Frequency Identification Mode	100	400	KHz	
tWL	Clock Low Time	8		ns	
tWH	Clock High Time	8		ns	
tODLY	Output Delay	-3.5	3.5	ns	
tISU	Input Setup Time	6		ns	
tIH	Input Hold Time	6		ns	

34.7 Register Definitions

Each register final address = module base address+ offset * 4

Where module address addresses are 0xd0070000 for port A (Wifi/SDIO) and portC(eMMC) and 0xd0072000 for port B (SD card).

SD_EMMC_CLOCK 0x0

Bit(s)	R/W	Default	Description
31:26	R	0	unused
25	R/W	0	Cfg_irq_sdio_sleep: 1: enable IRQ sdio when in sleep mode. When DAT1 IRQ, the controller uses PCLK to detect DAT1 level and starts core clock, the core initials
24	R/W	0	Cfg_always_on: 1: Keep clock always on 0: Clock on/off controlled by activities. Any APB3 access or descriptor execution will turn clock on. Recommended value: 0
23:20	R/W	0	Cfg_rx_delay: RX clock delay line 0: no delay, n: delay n*200ps Maximum delay 3ns.
19:16	R/W	0	Cfg_tx_delay: TX clock delay line 0: no delay, n: delay n*200ps Maximum delay 3ns.
15:14	R/W	0	Cfg_sram_pd: Sram power down
13:12			Cfg_rx_phase: RX clock phase 0: 0 phase, 1: 90 phase, 2: 180 phase, 3: 270 phase. Recommended value: 0
11:10	R/W	0	Cfg_tx_phase: TX clock phase 0: 0 phase, 1: 90 phase, 2: 180 phase, 3: 270 phase. Recommended value: 2
9:8	R/W	0	Cfg_co_phase: Core clock phase 0: 0 phase, 1: 90 phase, 2: 180 phase, 3: 270 phase. Recommended value: 2
7:6	R/W	0	Cfg_src: Clock source 0: Crystal 24MHz or other frequencies selected by clock reset test control register. 1: Fix PLL, 1000MHz Recommended value: 1
5:0	R/W	0	Cfg_div: Clock divider Frequency = clock source/cfg_div Clock off: cfg_div==0, the clock is disabled Divider bypass: cfg_div==1, clock source is used as core clock without divider Maximum divider 63.

SD_EMMC_DELAY 0x4

Bit(s)	R/W	Default	Description
31:28	R/W	0	Dly[7]: Data 7 delay line
27:24	R/W	0	Dly[6]: Data 6 delay line
23:20	R/W	0	Dly[5]: Data 5 delay line
19:16	R/W	0	Dly[4]: Data 4 delay line
15:12	R/W	0	Dly[3]: Data 3 delay line
11:8	R/W	0	Dly[2]: Data 2 delay line
7:4	R/W	0	Dly[1]: Data 1 delay line
3:0	R/W	0	Dly[0]: Data 0 delay line Total delay = 200ps * Dly When Dly == 0, no delay. When Dly ==15, 3ns delay. NOTE: the 200ps is typical delay, actually delay may vary from chip to chip, from different temperature.

SD_EMMC_ADJUST 0x8

Bit(s)	R/W	Default	Description
31:22			Unused
21:16	R/W	0	Adj_delay: Resample the input signals when clock index==adj_delay

Bit(s)	R/W	Default	Description
14	R/W	0	Cali_rise: 1: test the rising edge, recording rising edge location only. 0: test the falling edge
13	R/W	0	Adj_enable: Adjust interface timing by resampling the input signals
12	R/W	0	Cali_enable: 1: Enable calibration 0: shut off to save power.
11:8	R/W	0	Cali_sel: Select one signal to be tested Signals are labeled from 0 to 9 the same as delay lines. Only one signal is tested at anytime. For example: Cali_sel == 8, test CMD line.
7:4	R/W	0	Dly[9]: DS delay line
3:0	R/W	0	Dly[8]: Command delay line

SD_EMMC_CALOUT 0x10

Bit(s)	R/W	Default	Description
31:16			Unused
15:8	R		Cali_setup: Calibration reading The event happens at this index, The index starts from rising edge of core clock from 0, 1, 2, …
7	R		Cali_vld: The reading is valid When there is no rising edge or falling edge event, the valid is low, this reading is not valid.
5:0	R		Cali_idx: Copied from BASE+0x8 [15:8] include cali_sel, cali_enable, adj_enable, cali_rise.

SD_EMMC_START 0x40

Bit(s)	R/W	Default	Description
31:2	R/W	0	Desc_addr[31:2]: Descriptor address, the last 2 Bits are 0, SRAM: 4 bytes aligned, the valid address range is from 0x200~0x3ff DDR: 8 bytes aligned the valid address is anywhere in DDR, the length of chain is unlimited. Desc_addr = ADDR>>2.
1	R/W	0	Desc_busy: Start/Stop 1: Start command chain execution process. 0: Stop Write 1 to this register starts execution. Write 0 to this register stops execution.
0	R/W	0	Desc_int: SRAM/DDR 1: Read descriptor from internal SRAM, limited to 32 descriptors. 0: Read descriptor from external DDR

SD_EMMC_CFG 0x44

Bit(s)	R/W	Default	Description
31:28	R/W	0	Cfg_ip_txd_adj: Data 1 interrupt, when in TXD mode, the data 1 irq is a input signal, the round trip delay is uncertain factor, change this cfg to compensate the delay.
27	R/W	0	Cfg_err_abort: 1: abort current read/write and issue IRQ 0: continue on current read/write blocks.
26	R/W	0	Cfg_irq_ds: 1: Use DS pin as SDIO IRQ input, 0: Use DAT1 pin as SDIO IRQ input.
25	R/W	0	Cfg_txd_retry: When TXD CRC error, host sends the block again. The total number of retries of one descriptor is limited to 15, after 15 retries, the TXD_err is set to high.
24	R/W	0	Cfg_txd_add_err: TXD add error test. Test feature, should not be used in normal condition. It will inverted the first CRC Bits of the 3rd block. Block index starts from 0, 1, 2, …
23	R/W	0	Cfg_auto_clk: SD/eMMC Clock Control 1: when BUS is idle and no descriptor is available, automatically turn off clock, to save power. 0:.whenever core clock is on the SD/eMMC clock is ON, it is still on/off during read data from SD/eMMC.

Bit(s)	R/W	Default	Description
22	R/W	0	Cfg_stop_clk: SD/eMMC Clock Control 1: no clock for external SD/eMMC, used in voltage switch. 0: normal clock, the clock is automatically on/off during reading mode to back off reading in case of DDR slow response.
21	R/W	0	Cfg_cmd_low: Hold CMD as output Low eMMC boot mode.
20	R/W	0	Cfg_chk_ds: Check data strobe in HS400
19	R/W	0	Cfg_ignore_owner: Use this descriptor even if its owner bit is “0”.
18	R/W	0	Cfg_sdclk_always_on: 1: SD/eMMC clock is always ON 0: SD/eMMC clock is controlled by host. WARNING: Set SD/eMMC clock to always ON, host may lose data when DDR is slow.
17	R/W	0	Cfg_blk_gap_ip: 1: Enable SDIO data block gap interrupt period 0: Disabled.
16	R/W	0	Cfg_out_fall: DDR mode only The command and TXD start from rising edge. Set 1 to start from falling edge.
15:12	R/W	0	Cfg_rc_cc: Wait response-command, command-command gap before next command, $2^{cfg\_rc\_cc}$ core clock cycles.
11:8	R/W	0	Cfg_resp_timeout: Wait response till $2c^{fg\_resp\_timeout}$ core clock cycles. Maximum 32768 core cycles.
7:4	R/W	0	Cfg_bl_len: Block length $2^{cfg\_bl\_len}$, because internal buffer size is limited to 512 bytes, the cfg_bl_len <=9.
3	R/W	0	Cfg_dc_ugt: 1: DDR access urgent 0: DDR access normal
2	R/W	0	Cfg_ddr: 1: DDR mode 0: SDR mode
1:0	R/W	0	Cfg_bus_width: 0: 1 bit 1: 4 Bits 2: 8 Bits 3: 2 Bits (not supported)

SD_EMMC_STATUS 0x48

Bit(s)	R/W	Default	Description
31	R		Core_busy: 1: core is busy, desc_busy or sd_emmc_irq or bus_fsm is not idle. 0: core is idle.
30	R		Desc_busy: 1: Desc input process is busy, more descriptors in chain. 0: no more descriptor in chain or desc_err.
29:26	R		Bus_fsm: BUS fsm
25	R		DS: Input data strobe
24	R		CMD_i: Input response signal
23:16	R		DAT_i: Input data signals
15	R/W		IRQ_sdio: SDIO device uses DAT[1] to request IRQ
14	R/W		Resp_status: When resp_num is set to 1, the resp_addr is the response status IRQ enable Bits, if there is an error.
13	R/W		End_of_Chain: End of Chain IRQ, Normal IRQ
12	R/W		Desc_timeout: Descriptor execution time over time limit. The timeout limit is set by descriptor itself. Consider the multiple block read/write, set the proper timeout limits.
11	R/W		Resp_timeout: No response received before time limit. The timeout limit is set by cfg_resp_timeout.
10	R/W		Resp_err: Response CRC error
9	R/W		Desc_err: SD/eMMC controller doesn’t own descriptor. The owner bit is “0”, set cfg_ignore_owner to ignore this error.
8	R/W		Txd_err: TX data CRC error, For multiple block write, any one of blocks CRC error.
7:0	R/W		Rxd_err: RX data CRC error per wire, for multiple block read, the CRC errors are Ored together.

SD_EMMC_IRQ_EN 0x4c

Bit(s)	R/W	Default	Description
31:17			Unused
16	R/W	0	Cfg_secure: Data read/write with crypto DES
15	R/W	0	en_IRQ_sdio: Enable sdio interrupt.
14	R/W	0	En_resp_status: Response status error.
13	R/W	0	en_End_of_Chain: End of Chain IRQ
12	R/W	0	en_Desc_timeout: Descriptor execution time over time limit.
11	R/W	0	en_Resp_timeout: No response received before time limit.
10	R/W	0	en_Resp_err: Response CRC error
9	R/W	0	en_Desc_err: SD/eMMC controller doesn't own descriptor.
8	R/W	0	En_txd_err: TX data CRC error
7:0	R/W	0	en_Rxd_err: RX data CRC error per wire.

Descriptor_REG0 0x50

Bit(s)	R/W	Default	Description
31:0	R/W		SD_EMMC_CMD_CFG APB read wait Same as descriptor first word, resp_num = 1, response saved back into descriptor only. Read from this APB will hold APB bus

Descriptor_REG1 0x54

Bit(s)	R/W	Default	Description
31:0	R/W		SD_EMMC_CMD_ARG APB write start Same as descriptor second word. **Write to this APB address starts execution.** If the current desc is busy, it will be executed after current descriptor is done.

Descriptor_REG2 0x58

Bit(s)	R/W	Default	Description
31:0	R/W		SD_EMMC_CMD_DAT : Same as descriptor third word, 32 Bits data.

Descriptor_REG3 0x5c

Bit(s)	R/W	Default	Description
31:0	R/W		SD_EMMC_CMD_RSP: Write: response status IRQ enable Bits. Read: Response Bit 31:0

Descriptor_REG4 0x60

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CMD_RSP1: Response bit 63:32

Descriptor_REG5 0x64

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CMD_RSP2: Response bit 95:64

Descriptor_REG6 0x68

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CMD_RSP3: Response bit 127:96

Descriptor_REG7 0x6c

Bit(s)	R/W	Default	Description
31:0			Reserved

Current_Next_Descriptor_REG0 0x70

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CURR_CFG: Current descriptor under execution.

Current_Next_Descriptor_REG1 0x74

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CURR_ARG

Current_Next_Descriptor_REG2 0x78

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CURR_DAT

Current_Next_Descriptor_REG3 0x7c

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_CURR_RSP

Current_Next_Descriptor_REG4 0x80

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_NEXT_CFG: Next descriptor waiting for execution, already read out from SRAM or DDR, can't be changed.

Current_Next_Descriptor_REG5 0x84

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_NEXT_ARG

Current_Next_Descriptor_REG6 0x88

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_NEXT_DAT

Current_Next_Descriptor_REG7 0x8c

Bit(s)	R/W	Default	Description
31:0	R		SD_EMMC_NEXT_RSP

SD_EMMC_RXD 0x90

Bit(s)	R/W	Default	Description
31:25	R		Unused
24:16	R		Data_blk: Rxd Blocks received from BUS Txd blocks received from DDR.
15:10			unused
9:0	R		Data_cnt: Rxd words received from BUS. Txd words received from DDR.

SD_EMMC_RXD 0x94

Bit(s)	R/W	Default	Description
31:25			Unused
24:16	R		Txd_blk: Txd BUS block counter
15			unused
14:0	R		Txd_cnt: Txd BUS cycle counter

35. SERIAL PERIPHERAL INTERFACE COMMUNICATION CONTROLLER

35.1 Overview

SPI Communication Controller is designed for connecting general SPI protocol compatible module. This controller allows rapid data communication with less software interrupts than conventional serial communications.

35.2 Features

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four chip selects to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 64-bit wide by 16-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Both PIO(Programming In/Out interface) and DMA(Direct Memory Access interface) supported

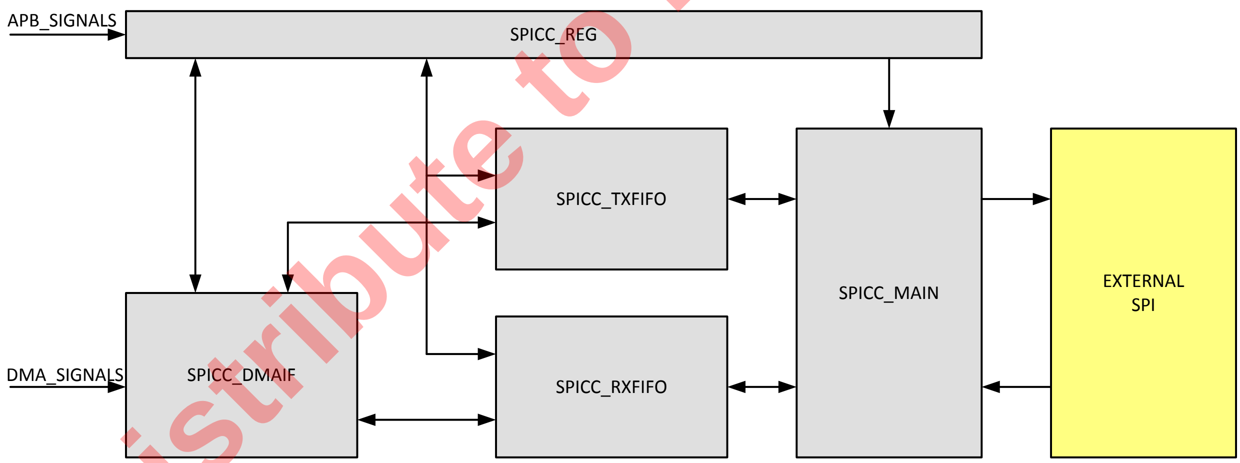
35.3 Functional Description

The following are two SPICC modes of operation:

- Master Mode—When the SPICC module is configured as a master, it uses a serial link to transfer data between the SPICC and an external device. A chip-enable signal and a clock signal are used to transfer data between these two devices. If the external device is a transmit-only device, the SPICC master's output port can be ignored and used for other purposes. To use the internal TXFIFO and RXFIFO, two auxiliary output signals, SS and SPI_RDY, are used for data transfer rate control. The user can also program the sample period control register to a fixed data transfer rate.
- Slave Mode–When the SPICC module is configured as a slave, the user can configure the SPICC Control register to match the external SPI master's timing. In this configuration, SS becomes an input signal, and is used to control data transfers through the Shift register, as well as to load/store the data FIFO.

There are 5 sub-modules in sd host controller, i.e. sd_ctrl, sd_async, sd_dphy_tx, sd_dphy_rx, and sd_clkgen. Transmitting and receiving are using different channel, that means they have different buffer.

Fig VI.35.1 SPICC Block Diagram



- spicc_reg is driven by host cpu, and spicc_reg is responsible for configuring other modules.
- spicc_dmaif is responsible for dealing with DMA operatoins.
- spicc_txfifo contains a transmission FIFO.
- spicc_rxfifo contains a receiving FIFO.
- spicc_main is responsible for main control of basic spi operation.

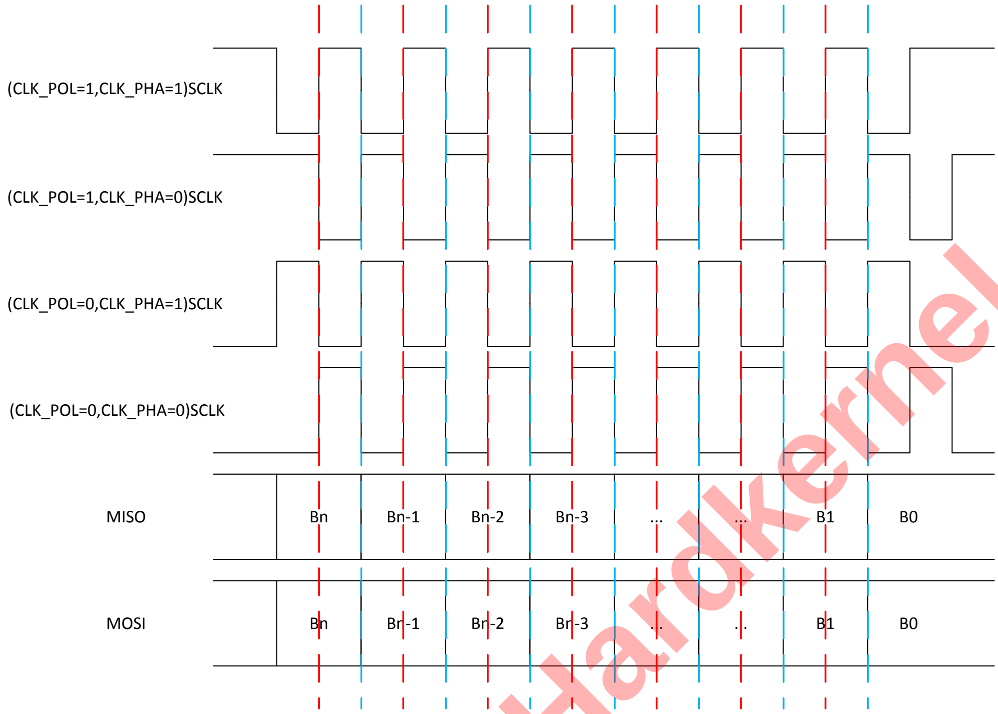
Here are SPI External Signals:

Table VI.35.1 SPI External Signals

Signal Name	I/O	Description
spicc_sclk	IO	SCLK, SPI Clock
spicc_miso	IO	MISO, Master Input Slave Output
spicc_mosi	IO	MOSI, Master Output Slave In
spicc_ss[3:0]	IO	SS, SPI chip Select, Supports up to 4 slaves.
spicc_rdy_i	I	RDY input, Data Ready Input

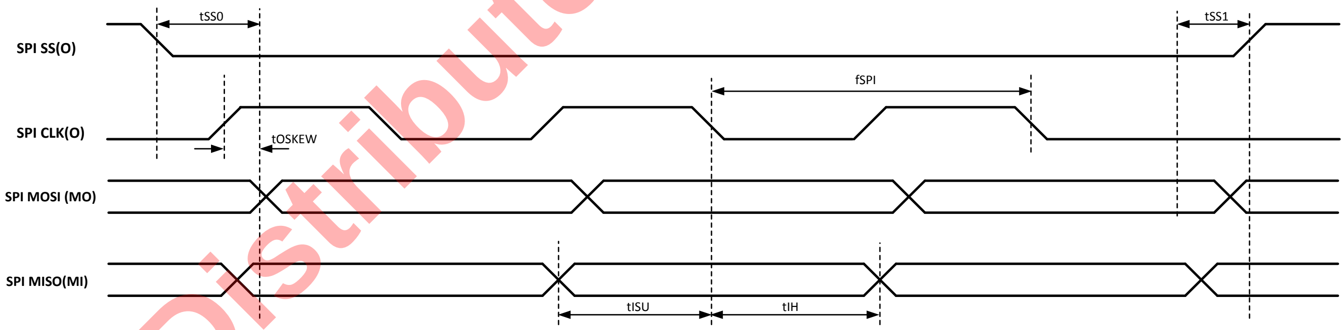
And here is SPI Generic Timing:

Fig VI.35.2 SPI Generic Timing



35.4 Timing Specification

Fig VI.35.3. SPICC Timing Diagram



Master Mode, CPOL=0, CPHA=1

Table VI.35.2. SPICC Master Timing Specification

Symbol	Description	Min.	Max.	Unit	Notes
fSPI	Clock Frequency	0	30	MHz	
tOSKEW	Output SKEW	-3.5	3.5	ns	
tISU	Input Setup Time	8		ns	
tIH	Input Hold Time	8		ns	
tSS0	SS active time before transition	8		ns	
tSS1	SS inactive time after transition	8		ns	

Slave Mode, CPOL=0, CPHA=1

Table VI.35.3. SPICC Slave Timing Specification

Symbol	Description	Min.	Max.	Unit	Notes
fSPI	Clock Frequency	0	30	MHz	
tOSKEW	Output SKEW	-3.5	3.5	ns	
tISU	Input Setup Time	8		ns	
tIH	Input Hold Time	8		ns	
tSS0	SS active time before transition	5		ns	
tSS1	SS inactive time after transition	5		ns	

35.5 Register Description

RXDATA 0xc1108d80

Bit(s)	R/W	Default	Description
31:0	R	0	Rx Data

Note1: when PIO mode, programmer can get data from this register.

TXDATA 0xc1108d84

Bit(s)	R/W	Default	Description
31:0	W	0	Tx Data

Note1: when PIO mode, programmer need send data to this register.

CONREG 0xc1108d88

Bit(s)	R/W	Default	Description
31:19	RW	0	[13]burst_length ([5:0]bit number of one word/package, [12:6]burst length-1)
18:16	RW	0	[3]data_rate (sclk will be divided by system clock with equation: 2^(data_rate+2), Example: if system clock = 128MHz and data_rate=2, sclk's frequency equals 8MHz)
15:14			Reserved
13:12	RW	0	[2]chip_select (00:select ss_0, 01:select ss_1, 10:select ss_2, 11:select ss_3,)
11:10			Reserved
9:8	RW	0	[2]drctl (0:ignore RDY input, 1:Data ready using pin rdy_i's failing edge, 2:Data ready using pin rdy_i's low level, 3:reserved)
7	RW	0	[1]sspol (0:SS polarity Low active,1:High active)
6	RW	0	[1]ssctl (see details in Note1)
5	RW	0	[1]pha (clock/data phase control, see section 2.2)
4	RW	0	[1]pol (clock polarity control, see section 2.2)
3	RW	0	[1]smc (start mode control, see Note2)
2	RW	0	[1]xch(exchange bit, ATTN:will automatically cleared when burst finished, see Note3)
1	RW	0	[1]mode (0:slave,1:master)
0	RW	0	[1]en (0:spicc disable,1:enable)

Note1: In one burst of master mode, if ssctl ==0, ss will output 0 between each spi transition. And if ssctl ==1, ss will output 1.
Note2: smc is for start mode control. If smc ==0, burst will start when xch is set to 1'b1; if smc==1, burst will start when txfifo is not empty.
Note3: setting xch will issue a burst when smc==0, and This bit will be self-cleared after burst is finished.

INTREG 0xc1108d8c

Bit(s)	R/W	Default	Description
31:8			Reserved
7	RW	0	[1]tcen(transfer completed interrrupt enable)
6	RW	0	[1]roen(rxfifo overflow interrrupt enable)
5	RW	0	[1]rfen(rxfifo full interrrupt enable)
4	RW	0	[1]rhen(rxfifo half full interrrupt enable)
3	RW	0	[1]rren(rxfifo ready interrrupt enable)
2	RW	0	[1]tfen(txfifo full interrrupt enable)
1	RW	0	[1]then(txfifo half full interrrupt enable)
0	RW	0	[1]teen(txfifo empty interrrupt enable)

Note1: Interrupt Status presents in STATREG.

DMAREG 0xc1108d90

Bit(s)	R/W	Default	Description
31:26	RW	0	[6]DMA Burst Number
25:20	RW	0	[6]DMA Thread ID
19	RW	0	[1]DMA Urgent
18:15	RW	0x7	[4]Number in one Write request burst(0:1,1:2...)
14:11	RW	0x7	[4]Number in one Read request burst(0:1,1:2...)
10:6	RW	0x8	[5]RxFIFO threshold(RxFIFO's count>=thres, will request write)
5:1	RW	0	[5]TxFIFO threshold(TxFIFO's count<=thres, will request read)
0	RW	0	[1]DMA Enable

STATREG 0xc1108d94

Bit(s)	R/W	Default	Description
31:8			Reserved
7	RW	0	[1]tc(transfer completed, w1c, see Note1)
6	R	0	[1]ro(rxfifo overflow)
5	R	0	[1]rf(rxfifo full)
4	R	0	[1]rh(rxfifo half full)
3	R	0	[1]rr(rxfifo ready)
2	R	0	[1]tf(txfifo full)

Note1: tc is the status bit which indicates a burst transfer is completed. And a burst transfer should be started by writing xch 1'b1. This bit supports w1c(Write 1 clear).

PERIODREG 0xc1108d98

Bit(s)	R/W	Default	Description
31:15			Reserved
14:0	RW	0	[15]period(wait cycles, see Note1)

Note1: Programmer can add wait cycles through this register if transmission rate need to be controlled.

TESTREG 0xc1108d9c

Bit(s)	R/W	Default	Description
31:23	RW	0	Reserved
Read Only (Need pay attention)			
22:21	R	0	[2]fiforst(fifo soft reset)
20:15	R	0x15	[6]dlyctl(delay control)
14	R	0	[1]swap(data swap for reading rxfifo)

Bit(s)	R/W	Default	Description
13	R	0	[1]lbc(loop back control)
Write Only (Need pay attention)			
23:22	W	0	[2]fiforst(fifo soft reset)
21:16	W	0x15	[6]dlyctl(delay control)
15	W	0	[1]swap(data swap for reading rxfifo)
14	W	0	[1]lbc(loop back control)
12:10	R	0	[3]smstatus(internal state machine status)
9:5	R	0	[5]rxcnt(internal RxFIFO counter)

Note1: Programmer can only use the TESTREG[9:0], rxcnt(internal RxFIFO counter) and txcnt(internal TxFIFO counter) , and other Bits just for test.

DRADDR 0xc1108da0

Bit(s)	R/W	Default	Description
31:0	RW	0	Read Address of DMA

DWADDR 0xc1108da4

Bit(s)	R/W	Default	Description
31:0	RW	0	Write Address of DMA

36. SERIAL PERIPHERAL INTERFACE FLASH CONTROLLER

36.1 Overview

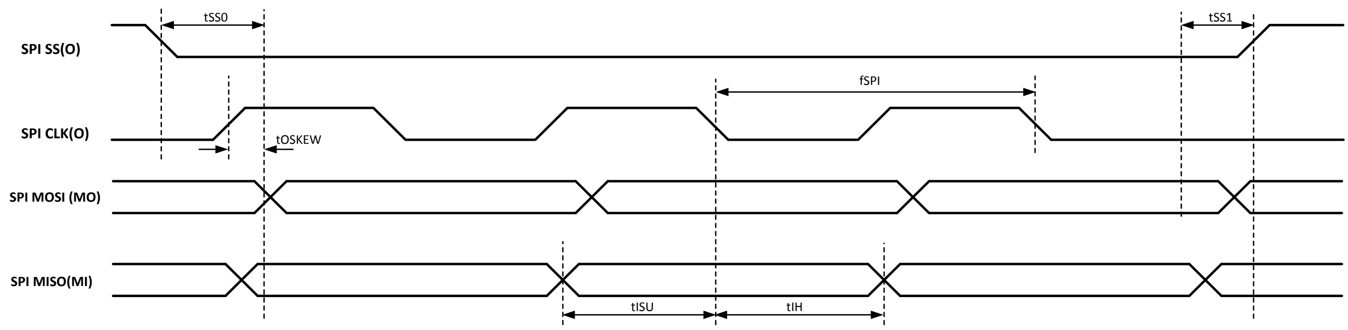
SPI Flash Controller is designed for connecting varied SPI Flash memory.

36.2 Features

- Support three operation modes, NOR Flash mode, Master mode, and Slave mode.
- Support read/write buffer up to 64bytes.
- Support no clock toggling during DUMMY state.
- Support hold by an external pin during a transition.
- AHB read support byte and halfword.
- Support bit-number rather than byte-number for each stage.
- Support 2/4 wire writing like fast reading
- Support both rising-edge and falling-edge for SPI slave sampling and SPI master sampling.
- Support 1 wire for SPI_D and SPI_Q.
- Support SPI_CK setup and hold time by cycles
- Support 8 bit clock divider, so SPI_CK can be low as 1/256 HCLK
- Support byte-order in a word
- Support no command state, so the command is sent/received in address state by 2/4 wires.
- Support both data input and data output in a transition. SPI_DOUT->(SPI_DUMMY)->SPI_DIN

36.3 Timing Specification

Fig VI.36.1 SPIFC Timing Diagram



Master Mode, CPOL=0, CPHA=1

Table VI.36.1 SPIFC Master Timing Specification

Symbol	Description	Min.	Max.	Unit	Notes
fSPI	Clock Frequency	0	20	MHz	
tWL	Clock Low Time	20		ns	
tWH	Clock High Time	20		ns	
tOSKEW	Output SKEW	-5	5	ns	
tISU	Input Setup Time	10		ns	
tIH	Input Hold Time	10		ns	
tSS0	SS active time before transition	0		ns	
tSS1	SS inactive time after transition	0		ns	
tWP0	WP active time before transition	Software Controlled		ns	
tWP1	WP inactive time after transition	Software Controlled		ns	

36.4 Register Description

SPIFC FLASH Command register 0xc1108c80

Bit(s)	R/W	Default	Description
31	R/W	0	READ command. 1 = read. When it becames 0, the read command is finished. The READ command could be (0xEB, 0x6B, 0xBB, 0x3B, 0x0B, 0x03). By default is 0x0B. One read command will read continous 32x8Bits data. And saved in data cache.
30	R/W	0	WREN command. (0x06)
29	R/W	0	WRDI command. (0x04).
28	R/W	0	RDID command. (0x9f).
27	R/W	0	RDSR command. (0x05).
26	R/W	0	WRSR command. (0x01).
25	R/W	0	Page program command. (0xAD or 0x02).
24	R/W	0	SE command (0x20).
23	R/W	0	BE command (0xD8).
22	R/W	0	CE command.(0xC7).
21	R/W	0	Deep Power Down command(0xB9).
20	R/W	0	RES command. (0xAB).
19	R/W	0	HPM command.(0xA3). (Just For winbond SPI flash).
18	R/W	0	USER defined command.
17:0	R/W	0	Reserved for future.

SPIFC address register 0xc1108c84

Bit(s)	R/W	Default	Description
31:0	R/W	0	The address[31:0] of the user command

SPIFC control register 0xc1108c88

Bit(s)	R/W	Default	Description
31:27	R/W	0	Reserved.
26	R/W	0	WriTE bit order. 1 = 0, 1, 2, 3, 4, 5, 6, 7. 0 = 7, 6, 5, 4, 3, 2, 1, 0.
25	R/W	0	Read bit order. . 1 = 0, 1, 2, 3, 4, 5, 6, 7. 0 = 7, 6, 5, 4, 3, 2, 1, 0.
24	R/W	0	Fast read QIO mode.
23	R/W	0	Fast read DIO mode.
22	R/W	0	Write 2 bytes status mode. For some of winbond SPI flash, the status register is 16Bits.
21	R/W	1	SPI flash WP pin value if use SPI flash WP pin as write protection.
20	R/W	0	Fast read QOUT mode.
19	R/W	1	1 = SPI share pins with SDRAM. 0 = doesn't share.
18	R/W	0	SPI hold mode. 1=SPI controller would use SPI hold function. 0 = SPI controller won't use hold function. The SPI flash hold pin can be tie high on the board. Or SPI controller can use hold pin as QIO/QOUT mode.
17	R/W	1	1 = enable AHB request. 0 = disable AHB request when you reconfigure SPI controller or running APB bus commands.
16	R/W	0	1 =enable SST SPI Flash aai command. The APB bus PP command will send AAI command.
15	R/W	1	1 = release from Deep Power-Down command is with read electronic signature.
14	R/W	0	Fast read DOUT mode.
13	R/W	1	Fast read mode. AHB bus read requirement and APB bus read command use the command 0x0Bh.
12:0	R/W	0	Reserved for future.

SPIFC control register 0xc1108c8c

Bit(s)	R/W	Default	Description
31:28	R/W	5	SPI Clock cycles for SPI flash timing requirement tCSH.
27:16	R/W	0xfff	SPI Clock cycles for SPI flash timing requirement tRES.
15:0	R/W	0x0120	System clock cycles for SPI bus timer. In SPI share bus and SPI hold function mode. SPI bus timer used , if SPI use the bus for a limit time, SPI controller will diassert SPI hold pin to halt the SPI Flash, and give the bus control to SDRAM.

SPIFC status register 0xc1108c90

Bit(s)	R/W	Default	Description
31:24	R/W	0	Reserved.
23:16	R/W	0	For winbond SPI flash, this 8 Bits used for DIOmode M7~M0,
15:0	R/W	0	SPI status register value. WRSR command will write this value to SPI flash status. RDSR or RES command will save the read result to this register.

When SPI controller in the slave mode, this register are the status for the SPI master to read out.

Bit(s)	R/W	Default	Description
31:0	R/W	0	In SPI Slave mode, the read status of the user command

SPIFC control register 2 0xc1108c904

Bit(s)	R/W	Default	Description
31:28	R/W	0	Delay cycle number of SPI_CS input in SPI slave mode or SPI_CS output in SPI master mode 0= not delay, 1 = delayed by 1 cycle of system clock, 2 = delayed by 2 cycles of system clock , …
27:26	R/W	0	delay mode of SPI_CS input in SPI slave mode or SPI_CS output in SPI master mode 0= not latched by the edges of SPI_CK 1= latched by the falling edges of SPI_CK 2 = latched by the rising edges of SPI_CK
25:23	R/W	0	Delay cycle number of SPI Data from SPI Master to SPI Slave In SPI master mode, it is for data outputs; in SPI slave mode, it is for data inputs. 0= not delay, 1 = delayed by 1 cycle of system clock, 2 = delayed by 2 cycles of system clock , …
22:21	R/W	0	Delay mode of SPI Data from SPI Master to SPI Slave In SPI master mode, it is for data outputs; in SPI slave mode, it is for data inputs. 0= not latched by the edges of SPI_CK 1= latched by the falling edges of SPI_CK 2 = latched by the rising edges of SPI_CK
20:18	R/W	0	Delay cycle number of SPI Data from SPI Slave to SPI Master. In SPI master mode, it is for data inputs; in SPI slave mode, it is for data outputs.

Bit(s)	R/W	Default	Description
			0= not delay, 1 = delayed by 1 cycle of system clock, 2 = delayed by 2 cycles of system clock , …
17:16	R/W	0	Delay mode of SPI Data from SPI Slave to SPI Master. In SPI master mode, it is for data inputs; in SPI slave mode, it is for data outputs. 0= not latched by the edges of SPI_CK 1= latched by the falling edges of SPI_CK 2 = latched by the rising edges of SPI_CK
15:12	R/W	0	In SPI master mode, SPI_CK rising edge mode 4'b1000 = later by 1/4 cycle of SPI_CK 4'b1001 = later by 1/8 cycle of SPI_CK 4'b1010 = later by 1/16 cycle of SPI_CK 4'b1011 = later by 1/32 cycle of SPI_CK 4'b1100 = earlier by 1/4 cycle of SPI_CK 4'b1101 = earlier by 1/8 cycle of SPI_CK 4'b1110 = earlier by 1/16 cycle of SPI_CK 4'b1111 = earlier by 1/32 cycle of SPI_CK Others = Normal
11:8	R/W	0	In SPI master mode, SPI_CK falling edge mode 4'b1000 = later by 1/4 cycle of SPI_CK 4'b1001 = later by 1/8 cycle of SPI_CK 4'b1010 = later by 1/16 cycle of SPI_CK 4'b1011 = later by 1/32 cycle of SPI_CK 4'b1100 = earlier by 1/4 cycle of SPI_CK 4'b1101 = earlier by 1/8 cycle of SPI_CK 4'b1110 = earlier by 1/16 cycle of SPI_CK 4'b1111 = earlier by 1/32 cycle of SPI_CK Others = Normal
7:4	R/W	1	In master mode, SPI clock cycles for SPI hold timing.
3:0	R/W	1	In master mode, SPI clock sycles for SPI setup timing. SPI setup time and SPI hold time is used to configure how soon the controller can enable spi_cs_n after the controller get the bus and how long the controller still keep the bus after the spi_cs_n become to be high.
31:28	R/W	0	Delay cycle number of SPI_CS input in SPI slave mode or SPI_CS output in SPI master mode 0= not delay, 1 = delayed by 1 cycle of system clock, 2 = delayed by 2 cycles of system clock , …
27:26	R/W	0	delay mode of SPI_CS input in SPI slave mode or SPI_CS output in SPI master mode 0= not latched by the edges of SPI_CK 1= latched by the falling edges of SPI_CK 2 = latched by the rising edges of SPI_CK
25:23	R/W	0	Delay cycle number of SPI Data from SPI Master to SPI Slave In SPI master mode, it is for data outputs; in SPI slave mode, it is for data inputs. 0= not delay, 1 = delayed by 1 cycle of system clock, 2 = delayed by 2 cycles of system clock , …
22:21	R/W	0	Delay mode of SPI Data from SPI Master to SPI Slave In SPI master mode, it is for data outputs; in SPI slave mode, it is for data inputs. 0= not latched by the edges of SPI_CK 1= latched by the falling edges of SPI_CK 2 = latched by the rising edges of SPI_CK
20:18	R/W	0	Delay cycle number of SPI Data from SPI Slave to SPI Master. In SPI master mode, it is for data inputs; in SPI slave mode, it is for data outputs. 0= not delay, 1 = delayed by 1 cycle of system clock, 2 = delayed by 2 cycles of system clock , …
17:16	R/W	0	Delay mode of SPI Data from SPI Slave to SPI Master. In SPI master mode, it is for data inputs; in SPI slave mode, it is for data outputs. 0= not latched by the edges of SPI_CK 1= latched by the falling edges of SPI_CK 2 = latched by the rising edges of SPI_CK
15:12	R/W	0	In SPI master mode, SPI_CK rising edge mode 4'b1000 = later by 1/4 cycle of SPI_CK 4'b1001 = later by 1/8 cycle of SPI_CK 4'b1010 = later by 1/16 cycle of SPI_CK 4'b1011 = later by 1/32 cycle of SPI_CK 4'b1100 = earlier by 1/4 cycle of SPI_CK 4'b1101 = earlier by 1/8 cycle of SPI_CK 4'b1110 = earlier by 1/16 cycle of SPI_CK

Bit(s)	R/W	Default	Description
			4'b1111 = earlier by 1/32 cycle of SPI_CK Others = Normal
11:8	R/W	0	In SPI master mode, SPI_CK falling edge mode 4'b1000 = later by 1/4 cycle of SPI_CK 4'b1001 = later by 1/8 cycle of SPI_CK 4'b1010 = later by 1/16 cycle of SPI_CK 4'b1011 = later by 1/32 cycle of SPI_CK 4'b1100 = earlier by 1/4 cycle of SPI_CK 4'b1101 = earlier by 1/8 cycle of SPI_CK 4'b1110 = earlier by 1/16 cycle of SPI_CK 4'b1111 = earlier by 1/32 cycle of SPI_CK Others = Normal
7:4	R/W	1	In master mode, SPI clock cycles for SPI hold timing.
3:0	R/W	1	In master mode, SPI clock sycles for SPI setup timing. SPI setup time and SPI hold time is used to configure how soon the controller can enable spi_cs_n after the controller get the bus and how long the controller still keep the bus after the spi_cs_n become to be high.

SPIFC Clock register 0xc1108c98

Bit(s)	R/W	Default	Description
31	R/W	1	1=SPI clock frequency is same as system clock. 0 = SPI clock frequency will use clock divider.
30:18	R/W	0	Clock counter for Pre-scale divider: 0= not pre-scale divider, 1= pre-scale divided by 2, 2= pre-scale divided by 3, ...,
17:12	R/W	0	Clock counter for clock divider.
11:6	R/W	0	Clock high counter in SPI master mode. In SPI slave mode, it is for the delay counter for the rising edges of spi_ck_i
5:0	R/W	0	Clock low counter, in SPI master mode. In SPI slave mode, it is for the delay counter for the falling edges of spi_ck_i If the SPI clock frequcncy = sys_clock_frequency / n. Then the clock divider counter = n – 1; the clock high counter = n /2 – 1; the clock low counter = n– 1; For example, if you want to SPI clock freqency is divided by 2 of the system clock. The clock divider counter = 1, clock high counter = 0, clock low counter = 1. For SPI clock frequency = system clock / 4. The clock divider counter = 3, clock high counter = 1, clock low counter = 3.
31	R/W	1	1=SPI clock frequency is same as system clock. 0 = SPI clock frequency will use clock divider.
30:18	R/W	0	Clock counter for Pre-scale divider: 0= not pre-scale divider, 1= pre-scale divided by 2, 2= pre-scale divided by 3, ...,
17:12	R/W	0	Clock counter for clock divider.
11:6	R/W	0	Clock high counter in SPI master mode. In SPI slave mode, it is for the delay counter for the rising edges of spi_ck_i
5:0	R/W	0	Clock low counter, in SPI master mode. In SPI slave mode, it is for the delay counter for the falling edges of spi_ck_i If the SPI clock frequcncy = sys_clock_frequency / n. Then the clock divider counter = n – 1; the clock high counter = n /2 – 1; the clock low counter = n– 1; For example, if you want to SPI clock freqency is divided by 2 of the system clock. The clock divider counter = 1, clock high counter = 0, clock low counter = 1. For SPI clock frequency = system clock / 4. The clock divider counter = 3, clock high counter = 1, clock low counter = 3.

SPIFC User register 0xc1108c9c

Bit(s)	R/W	Default	Description
31	R/W	1	USER command COMMAND bit. 1 = user command includes command. 0 = no command. If some SPI slaves may support 2/4 IO at the first cycle, clear This bit.
30	R/W	0	USER command Address bit. 1 = user command includes address. 0 = no address.
29	R/W	0	USER command DUMMY bit. 1= user command includes Dummy bytes.
28	R/W	0	USER command DIn bit. 1 = user command includes data in. 0 = no data in.
27	R/W	0	USER command DO bit. 1 = user command includes data output. 0 = no data output. If both DIN and DO are valid, SPI master is firstly in data output state and then in data input state. If all of DUMMY, DO and DIN are valid, SPI master is firstly in data output state and then in dummy state, finally in data input state.

Bit(s)	R/W	Default	Description
26	R/W	0	USER command dummy idle bit. 1= no SPI clock toggling in dummy state. 0= normal
25	R/W	0	USER command highpart bit for SPI_DOUT stage. It is for data-output in spi master mode and for data-input in spi slave mode. 1 = only high half part of buffer are used. 0 = low half part or the whole 64bytes are used.
24	R/W	0	USER command highpart bit for SPI_DIN stage. It is for data-input in spi master mode and for data-output in spi slave mode. 1 = only high half part of buffer are used. 0 = low half part or the whole 64bytes are used.
23	R/W	0	User command external hold bit for prep. 1 = in prep state, SPI master controller can be hold by the external pin SPI_HOLD
22	R/W	0	User command external hold bit for command. 1 = in command state, SPI master controller can be hold by the external pin SPI_HOLD
21	R/W	0	User command external hold bit for address. 1 = in address state, SPI master controller can be hold by the external pin SPI_HOLD
20	R/W	0	User command external hold bit for dummy. 1 = in dummy state, SPI master controller can be hold by the external pin SPI_HOLD
19	R/W	0	User command external hold bit for data input. 1 = in data input state, SPI master controller can be hold by the external pin SPI_HOLD
18	R/W	0	User command external hold bit for data output. 1 = in data output state, SPI master controller can be hold by the external pin SPI_HOLD
17	R/W	1	User command external hold polarity bit. 1 = high is valid for hold, 0 = low is valid for hold.
16	R/W	0	Single DIO mode: Data output and input apply only 1 wire.
15	R/W	0	Fast write QIO mode.
14	R/W	0	Fast write DIO mode.
13	R/W	0	Fast write QOUT mode.
12	R/W	0	Fast write DOUT mode.
11	R/W	0	Write byte order. 0 = d[7:0], d[15:8], d[23:16], d[31:24]. 1 = d[31:24], d[23:16], d[15:8], d[7:0]
10	R/W	0	Read byte order. . 0 = d[7:0], d[15:8], d[23:16], d[31:24]. 1 = d[31:24], d[23:16], d[15:8], d[7:0]
9:8	R/W	0	AHB endian mode: 0= little-endian; 1= big-endian; 2~3 reserved
7	R/W	0	In SPI master mode, the clock output edge bit: 0 = SPI_CK is inverted, 1 = SPI_CK is not inverted
6	R/W	1	In SPI slave mode, the clock input edge bit: 0 = SPI_CK_I is inverted, 1 = SPI_CK_I is not inverted
5	R/W	0	SPI CS setup bit: 1 = valid in prep state
4	R/W	0	SPI CS hold bit: 1 = valid in done state
3	R/W	0	AHB-read apply the configurations of user-command, such as command value, Bit(s)-length,...
2	R/W	1	Backward Compatible: 1 = compatible to Apollo SPI This bit affect the three registers: “SPI Flash Commmand Register”, “SPI Address Register” and “SPI Control Register”
1	R/W	0	AHB-read support 4byte address, when AHB-read apply the configurations of user-command. 1 = 4byte address, 0 = 3byte address
0	R/W	0	In SPI master mode, Enable bit for Data input during SPI_DOUT stage. 1 = enable; 0 = disable This bit shall not be used in 2/4wire or SIO. When This bit is 1, during SPI_DOUT stage, data input are stored into cacheline/buffer from address 0, i.e., bit 24 is not controlling the start address. The data output can be specified by bit 25

SPIFC User register 1 0xc1108ca0

Bit(s)	R/W	Default	Description
31:26	R/W	0	USER command bit number for address state 0 = 1 bit, 1= 2 Bits, …
25:17	R/W	0	USER command bit number for data output state 0 = 1 bit, 1= 2 Bits, …
16:8	R/W	0	USER command bit number for data input state 0 = 1 bit, 1= 2 Bits, …
7:0	R/W	0	USER command cycle number for dummy state 0 = 1 cycle, 1= 2 cycles, …

SPIFC User register 2 0xc1108ca4

Bit(s)	R/W	Default	Description
31:28	R/W	0	USER command bit number for command state

Bit(s)	R/W	Default	Description
			0 = 1 bit, 1= 2 Bits, …
27:16	R/W	0	Reserved
15:0	R/W	0	The command content of the user command

SPIFC User register 3 0xc1108ca8

Bit(s)	R/W	Default	Description
31:0	R/W	0	In SPI Master mode, the address[63:32] of the user command In SPI Slave mode, the write status of the user command

SPIFC PIN register 0xc1108cac

Bit(s)	R/W	Default	Description
31	R/W	0	Pin swap when it is in DIN stage and SPI data input are 4wire. This feature is for Ubec Zigbee chips. 1 = swap between {spi_q, spi_d_i} and {spi_hold_i, spi_wp_i} 0 = normal
30	R/W	0	In SPI Master mode, CS keep active after a transition. 1 = enable; 0 = disable
29	R/W	0	Idle edge of SPI_CK 0 = low when it is idle 1 = high when it is idle
28:24	R/W	0	Reserved
23	R/W	0	In the SPI slave mode, spi_cs_i polarity: 1= high voltage is active 0= low voltage is active
22:21	R/W	0	In the SPI slave mode, spi_ck_i and spi_cs_i source pins 0=SPI_CK and SPI_CS pins, respectively 1=SPI_CS2 and SPI_CS1 pins, respectively 2=SPI_HOLD and SPI_WP pins, respectively
20	R/W	0	SPI_CS2 and SPI_CS1 pin function MUX 0= spi_ck and spi_cs in the SPI master mode 1= input pads for spi_ck_i and spi_cs_i, respectively, in the SPI slave mode
19	R/W	0	SPI_CK and SPI_CS pin function MUX 0= spi_ck and spi_cs in the SPI master mode 1= input pads for spi_ck_i and spi_cs_i, respectively, in the SPI slave mode
18:17	R/W	0	SPI_HOLD and SPI_WP pin function MUX 0= normal 1= spi_q and spi_d, respectively 2= spi_cs3 and spi_cs2, repectively 3= input pads for spi_ck_i and spi_cs_i, respectively, in the SPI slave mode
16	R/W	0	SPI_D and SPI_Q switch 1= SPI_D and SPI_Q pin-functions are swapped 0= normal
15:11	R/W	0	In Master mode, these are spi_ck MUX Bit[4:0] for spi_cs4 (SPI_HOLD pin), spi_cs3 (SPI_WP pin), spi_cs2, spi_cs1 and spi_cs, respectively 1= this pin is spi_ck, if this pin is not idle 0= this pin is spi_cs, if this pin is not idle
10:6	R/W	0	In Master mode, these are polarity Bit[4:0] for spi_cs4 (SPI_HOLD pin), spi_cs3 (SPI_WP pin), spi_cs2, spi_cs1 and spi_cs, respectively 1= high voltage is active 0= low voltage is active
5:0	R/W	0x1E	In Master mode, these are idle Bit[5:0] for SPI_CK, for spi_cs4 (SPI_HOLD pin), spi_cs3 (SPI_WP pin), spi_cs2, spi_cs1 and spi_cs, respectively 1= idle, i.e., the spi_ck signal is 0 or the spi_cs is at the inactive level 0= active if SPI controller is working

SPIFC Slave register 0xc1108cb0

Bit(s)	R/W	Default	Description
31	R/W	0	SPI controller SW reset: 1 = reset, 0 = none
30	R/W	0	SPI slave mode: 1 = slave, 0 = master

Bit(s)	R/W	Default	Description
29	R/W	0	In SPI slave mode, the enable bit for the command of write-buffer-and-read-buffer 0= disable, 1=enable
28	R/W	0	In SPI slave mode, the enable bit for the command of write-status-and-read-status 0= disable, 1=enable
27	R/W	0	SPI slave command define enable 0=Apply the last 3Bits of Flash commands and two extra command 1=Apply the user defined command in SPI Slave register 3
26:4	R/W	0	Reserved
11:10	R/W	0	spi_cs_i recovery mode: 0= and 1= or 2= normal 3= delayed
9:5	R/W	0	Interrupt enable for bit 4:0 1= enable, 0=disable
4	R/W	0	A SPI transition is done. (whatever it is in SPI master mode or SPI slave mode)
3	R/W	0	In SPI slave mode, a status write is done
2	R/W	0	In SPI slave mode, a status read is done
1	R/W	0	In SPI slave mode, a buffer write is done
0	R/W	0	In SPI slave mode, a buffer read is done

SPIFC Slave register 1 0xc1108cb4

Bit(s)	R/W	Default	Description
31:27	R/W	0	In SPI slave mode, status bit number 0 = 1 bit, 1= 2 Bits, …
26	R/W	0	In SPI slave mode, status fast read/write enable bit: 1 = enable, 0 = disable
25	R/W	0	In SPI slave mode, status read back enable bit: 1 = reading status is written status in SPI User register 3, 0 = reading status is in SPI Status register.
24:16	R/W	0	In SPI slave mode, buffer bit number 0 = 1 bit, 1= 2 Bits, …
15:10	R/W	0	In SPI slave mode, address bit number for reading buffer 0 = 1 bit, 1= 2 Bits, …
9:4	R/W	0	In SPI slave mode, address bit number for writing buffer 0 = 1 bit, 1= 2 Bits, …
3	R/W	0	In SPI slave mode, dummy enable bit for writing status 1=enable, 0=disable
2	R/W	0	In SPI slave mode, Dummy enable bit for reading status 1=enable, 0=disable
1	R/W	0	In SPI slave mode, Dummy enable bit for writing buffer 1=enable, 0=disable
0	R/W	0	In SPI slave mode, Dummy enable bit for reading buffer 1=enable, 0=disable

SPIFC Slave register 2 0xc1108cb8

Bit(s)	R/W	Default	Description
31:24	R/W	0	In SPI slave mode, Dummy cycle number for writing buffer 0 = 1 cycle, 1= 2 cycles, …
23:16	R/W	0	In SPI slave mode, Dummy cycle number for reading buffer 0 = 1 cycle, 1= 2 cycles, …
15:8	R/W	0	In SPI slave mode, Dummy cycle number for writing status 0 = 1 cycle, 1= 2 cycles, …
7:0	R/W	0	In SPI slave mode, Dummy cycle number for reading status 0 = 1 cycle, 1= 2 cycles, …

SPIFC Slave register 3 0xc1108cbC

Bit(s)	R/W	Default	Description
31:24	R/W	0	In SPI slave mode, Command value for writing status, when bit 27 “SPI slave command define enable” in SPI Slave register is 1

Bit(s)	R/W	Default	Description
23:16	R/W	0	In SPI slave mode, Command value for reading status, when bit 27 "SPI slave command define enable" in SPI Slave register is 1
15:8	R/W	0	In SPI slave mode, Command value for writing buffer, when bit 27 "SPI slave command define enable" in SPI Slave register is 1
7:0	R/W	0	In SPI slave mode, Command value for reading buffer, when bit 27 "SPI slave command define enable" in SPI Slave register is 1

SPIFC controller cache 0~7 0xc1108cc0~0xc1108cdc

Bit(s)	R/W	Default	Description
31:0	R/W	0	Cache line Word 0~7. Cache is used to read data both for AHB or APB read command. Cache is also used for APB page programming etc.

SPIFC controller buffer 8~15 0xc1108ce0~0xc1108cfc

Bit(s)	R/W	Default	Description
31:0	R/W	0	Buffer Word 8. Buffer is used to read/write data only for APB read/write user commands.

Section VII I/O Interface

This part describes S905's I/O interfaces from the following aspects:

- USB
- Ethernet
- SDIO
- Transport Interface and Transport Stream Demux
- ISO7816
- IR Remote
- SAR ADC
- I2C
- UART
- PWM

37. UNIVERSAL SERIAL BUS

37.1 Overview

The chips integrates in one USB OTG (On-the-GO) controller and one USB Host controller.

The USB OTG controller is a Dual-Role-Device (DRD) controller that supports both device and host functions and complies fully with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.3a and Revision 2.0. It can also be configured as a host-only or device-only controller, fully compliant with the USB 2.0 Specification. The USB host controller supports host functions and is fully compliant with USB2.0 specification,

37.2 Features

The OTG controller features:

- Support for the following speeds: High-Speed (HS, 480-Mbps),Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes
- Multiple DMA/non DMA mode access support on the application side
- Supports up to 16 bidirectional endpoints, including control endpoint 0.
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- Supports up to 16 host channels.

The Host controller features:

- Support for the following speeds: High-Speed (HS, 480-Mbps),Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes
- Multiple DMA/non DMA mode access support on the application side
- Supports up to 16 host channels.

38. ETHERNET MAC

38.1 Overview

The Ethernet MAC controller provides a complete Ethernet interface from the chip to a Reduced Gigabit Media Independent Interface (RGMII) or Reduced Media Independent Interface (RMII) compliant Ethernet PHY.

38.2 Features

- 10/100/1000 MAC 3.70a
- RGMII/RMII
- AHB 32 Bits internal bus
- RX FIFO 4KB, TX FIFO 2KB
- 2 MAC addresses
- EEE
- Power Management

38.3 Timing Specification

Management Data Timing

Fig VII.38.1. Management Data Timing Diagram

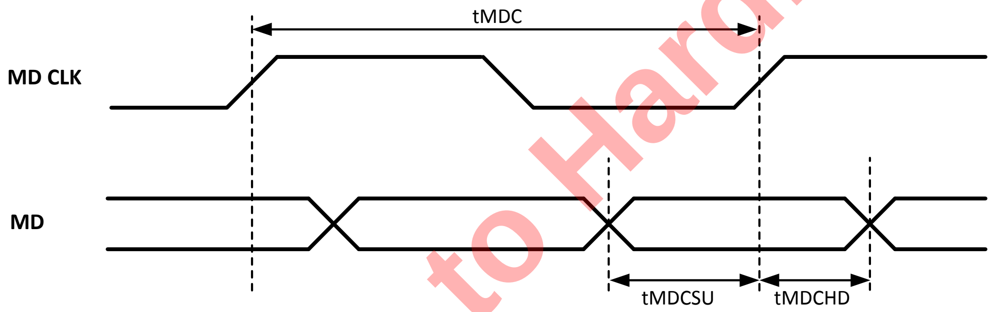


Table VII.38.1. Management Data Timing Specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
tMDC	MDC clock Period	400	500		ns	From MAC
tMDCSU	Setup time to rising edge of MDC	10			ns	
tMDCHD	Hold time to rising edge of MDC	10			ns	

RMII Timing

Fig VII.38.2 RMII Timing Diagram

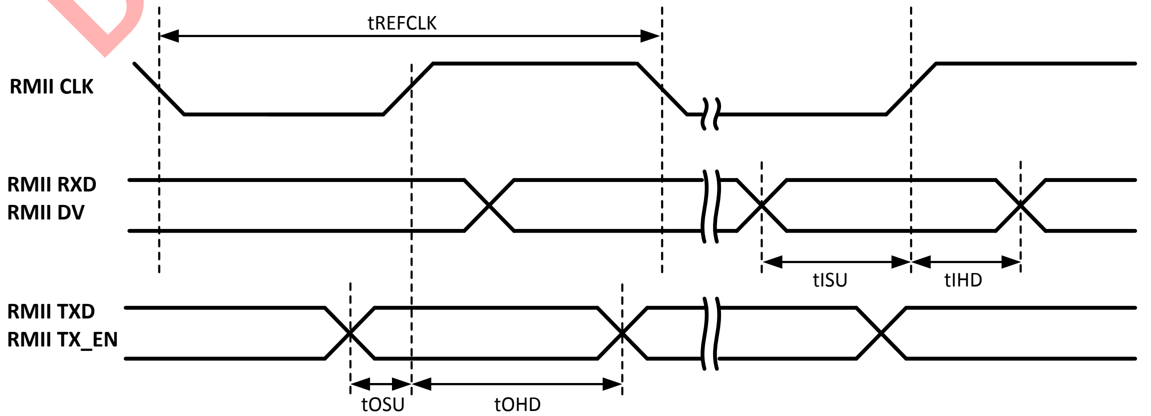


Table VII.38.2.RMII Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tREFCLK	RMII clock period		20		ns	50MHz from PHY
tOSU	TXD & TX_EN setup time to rising edge of RMII clock	1.8	10		ns	To PHY
tOHD	TXD & TX_EN hold time to rising edge of RMII clock	1.4	10		ns	To PHY
tISU	RXD & DV setup time to rising edge of RMII clock	1.0	10		ns	From PHY
tIHD	RXD & DV hold time to rising edge of RMII clock	1.0	10		ns	From PHY

RGMII Timing

Fig VII.38.3 RGMII Receive Timing Diagram

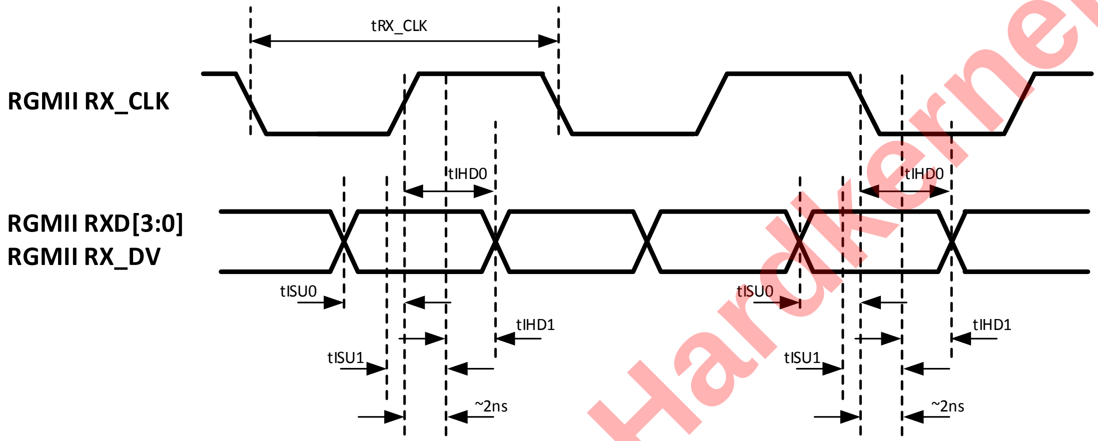


Table VII.38.3 RGMII Receive Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tRX_CLK	RGMII RX_CLK clock period		8		ns	125MHz from PHY
tSETUP	RXD[3:0] & RX_DV setup time (PHY internal delay enabled)	1.2			ns	From PHY
tHOLD	RXD[3:0] & RX_DV hold time (PHY internal delay enabled)	1.2			ns	From PHY
tSKEW	RXD[3:0] & RX_DV skew between these 5 signals (PHY internal delay disabled)	-0.5		0.5	ns	From PHY

When PHY internal delay is enabled, check setup/hold timing.
When PHY internal delay is disabled, check signal skew.

Fig VII.38.4 RGMII Transmit Timing Diagram

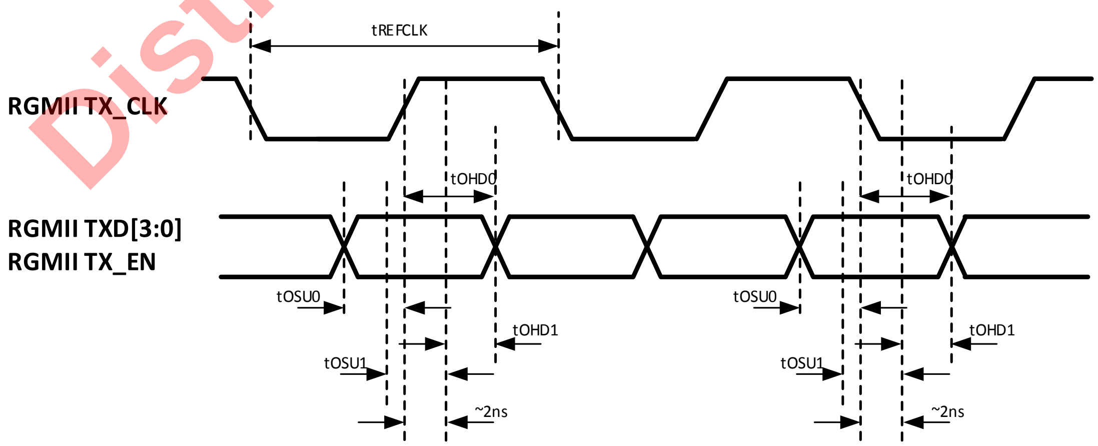


Table VII.38.4 RGMII Transmit Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tTX_CLK	RGMII TX_CLK clock period		8		ns	125MHz to PHY
tOSU	TXD & TX_EN setup time to rising edge of RGMII clock (no clock delay added)	1			ns	From PHY
	TXD & TX_EN setup time to rising edge of RGMII clock (clock delay added)	-0.9			ns	From PHY
tOHD	RXD & DV hold time to rising edge of RGMII clock (no clock delay added)	0.8			ns	From PHY
	RXD & DV hold time to rising edge of RGMII clock (clock delay added)	2.7			ns	From PHY

38.4 Register Description

PRG_ETHERNET_ADDR0 0xc8834108

Bit(s)	R/W	Default	Description
31	R/W	0	Set AHB to DDR interface as urgent.
30	R/W	0	RGMII mode Use RX_CLK as TX_CLK.
29-27	R/W	0	RMII & RGMII mode Select one signal from {RXDV, RXD[3:0]} to calibrate.
26	R/W	0	RMII & RGMII mode 0: test falling edge 1: test rising edge
25	R/W	0	RMII & RGMII mode Start calibration logic
24-20	R/W	0	RMII & RGMII mode 5 Bits correspondent to {RXDV, RXD[3:0]}, set to 1 will delay the data capture by 1 cycle.
19-15	R/W	0	Set bit14 to 0. RMII & RGMII mode Capture input data at clock index equal to adj_delay.
14	R/W	0	Set RXDV and RXD setup time, data is aligned with index 0. When set to 1, auto delay and skew
13	R/W	0	RMII & RGMII mode Enable data delay adjustment and calibration logic.
12	R/W	0	RMII & RGMII mode Enable TX_CLK and PHY_REF_CLK generator.
11	R/W	0	RMII mode Use inverted internal clk_rmii_i to generate 25/2.5 tx_rx_clk.
10	R/W	0	Generate 25MHz clock for PHY
9-7	R/W	0	RMII & RGMII mode, 000: invalid value. 001: mp2_clk_out is 250MHz. 010: mp2_clk_out is 500MHz. ... Mp2_clk_out is "ratio" *250MHz.
6-5	R/W	0	RGMII mode, TX_CLK related to TXD 00: clock delay 0 cycle. 01: clock delay ¼ cycle. 10: clock delay ½ cycle. 11: clock delay ¾ cycle.
4	R	0	Unused
3	R/W	0	RMII mode CLK_RMII RGMII mode RX_CLK Use inverted signal when set to 1.
2	R/W	0	Sideband Descriptor Endianness Control Function: When set high, this signal configures the DMA to transfer descriptors in reverse endianness of the data format. When low (by default), the descriptors are transferred in the same endian format as the data. This signal is sampled during active reset (including soft-reset) only and ignored after reset is de-asserted.
1	R/W	0	Sideband Data Endianness Control

Bit(s)	R/W	Default	Description
			Function: When set high, this signal configures the DMA to transfer data in big-endian format. When low (by default), the data is transferred in little-endian format. This signal is sampled during active reset (including soft-reset) only and ignored after reset is de-asserted.
0	R/W	0	PHY Interface Select Function: These pins select one of the multiple PHY interfaces of MAC. This is sampled only during reset assertion and ignored after that. 1: internal value 001: RGMII 0: internal value 100: RMII

PRG_ETHERNET_ADDR1 0xc883410c

Bit(s)	R/W	Default	Description
31-16	R	0	Unused
15	R/W	0	The result is valid
14	R/W	0	The results is rising edge test or falling edge test.
13-11	R/W	0	The signal under test.
10	R/W	0	The Calibration logic is waiting for event.
9-5	R/W	0	The RX_CLK length in 1ns.
4-0	R/W	0	Signal switch position in 1ns.

39. SDIO

Please refer to eMMC/SD/SDIO part for SDIO information.

40. INTER-INTEGRATED CIRCUIT (I2C)

40.1 Overview

Inter-Integrated Circuit (IIC or I2C) is a multi-slave serial communication bus between ICs. S905 integrates the I2C interface and signals allowing communications with other I2C peripheral devices.

40.2 Features

The I^{2}C Master Module has the following features:

- Support for 7-bit and 10-bit addressable devices
- Programmable bus speed including standard speed (100kBits/s) and fast speed (400kBits/sec)
- Error transfer detection
- “Transfer complete” indication by polling or interrupt (Interrupts handled by the ISA module. See the ISA module for details).
- Internal buffer holding up to 8 bytes for transfer (in either direction)
- Flexible architecture allowing the software to dictate the format of the I^{2}C bit streams
- Manual setting of the I^{2}C bus to accommodate a software only mode

40.3 Timing Specification

There are two modes to the I2C master interface: Standard (100khz) and fast (400khz).

Fig VII.40.1 I2C Interface Timing Diagram

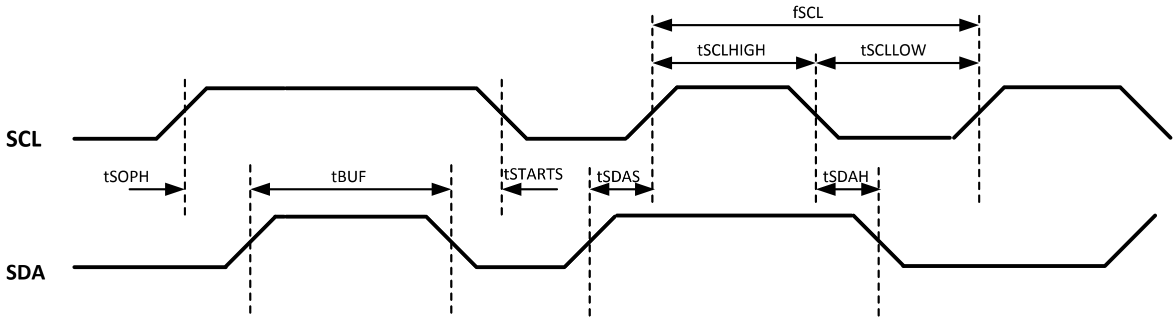


Table VII.40.1 I2C Interface Timing Specification

Symbol	Description	Min.	Max.	Unit	Notes
fSCL	SCL clock frequency		Std. 100 Fast 400	kHz	
tSDAS	Data setup before the rising edge of clock	Std. 4.0 Fast 0.6		µs	
tSDAH	Data hold after the falling edge of clock	Std. 4.0 Fast 0.6	-	µs	
tSTARTS	Clock hold time after the falling edge of SDA when a START command is issued	Std. 4.0 Fast 0.6	-	µs	
tSTOPH	Clock setup time before the rising edge of SDA when a STOP command is issued	Std. 4.0 Fast 0.6		µs	
tBUF	Delay between start and stop	Software Controlled		µs	
tSCLLOW	Clock LOW time	Std. 8.0 Fast 1.3		µs	
tSCLHIGH	Clock HIGH time	Std. 8.0 Fast 1.3		µs	

40.4 Register Description

Each register final address = 0xC1100000 + offset * 4

I2C_M_0_CONTROL_REG 0x2140

Bit(s)	R/W	Default	Description
31	R/W	0	CNTL_JIC: There is internal logic to dynamically enable the gated clocks. If this gated clock logic doesn't work, you can set This bit to always enable the clock. Setting This bit wastes power.
30	R	0	Unused
29-28	R/W	0	QTR_CLK_EXT: These two Bits extend the clock divider to 12 Bits: QTR_CLK = {[29:28],[21:12]}
27	R	0	unused
26	R	0	Read back level of the SDA line
25	R	0	Read back level of the SCL line
24	R/W	0	Sets the level of the SDA line if manual mode is enabled. If This bit is '0', then the SDA line is pulled low. If This bit is '1' then the SDA line is tri-stated.
23	R/W	0	Sets the level of the SCL line if manual mode is enabled. If This bit is '0', then the SCL line is pulled low. If This bit is '1' then the SCL line is tri-stated.
22	R/W	0	This bit is used to enable manual mode. Manual I^2C mode is controlled by Bits 12,13,14 and 15 above.
21:12	R/W	0x142	**QTR_CLK_DLY**. This value corresponds to period of the SCL clock divided by 4 Quarter Clock Delay = * System Clock Frequency For example, if the system clock is 133Mhz, and the I^2C clock period is 10uS (100khz), then Quarter Clock Delay = * 133 Mhz = 332

Bit(s)	R/W	Default	Description
11:8	R	-	READ_DATA_COUNT: This value corresponds to the number of bytes READ over the I²C bus. If this value is zero, then no data has been read. If this value is 1, then Bits [7:0] in TOKEN_RDATA_REG0 contains valid data. The software can read this register after an I²C transaction to get the number of bytes to read from the I²C device.
7:4	R	-	CURRENT_TOKEN: This value reflects the current token being processed. In the event of an error, the software can use this value to determine the error location.
3	R	-	ERROR: This read only Bit is set if the I²C device generates a NACK during writing. This bit is cleared at on the clock cycle after the START Bit is set to 1 indicating the start of list processing. Errors can be ignored by setting the ACK_IGNORE Bit(s) below. Errors will be generated on Writes to devices that return NACK instead of ACK. A NACK is returned by a device if it is unable to accept any more data (for example because it is processing some other real-time function). In the event of an ERROR, the I²C module will automatically generate a STOP condition on the bus.
2	R	-	STATUS: This bit reflects the status of the List processor: 0: IDLE 1: Running. The list processor will enter this state on the clock cycle after the START Bit is set. The software can poll the status register to determine when processing is complete.
1	R/W	0	ACK_IGNORE: Set to 1 to disable I²C ACK detection. The I²C bus uses an ACK signal after every byte transfer to detect problems during the transfer. Current Software implementations of the I²C bus ignore this ACK. This bit is for compatibility with the current Amlogic software. This bit should be set to 0 to allow NACK operations to abort I²C bus transactions. If a NACK occurs, the ERROR bit above will be set.
0	R/W	0	START: Set to 1 to start list processing. Setting This bit to 0 while the list processor is operating causes the list processor to abort the current I²C operation and generate an I²C STOP command on the I²C bus. Normally This bit is set to 1 and left high until processing is complete. To re-start the list processor with a new list (after a previous list has been exhausted), simply set This bit to zero then to one.

I2C_M_0_SLAVE ADDRESS 0x2141

Bit(s)	R/W	Default	Description
31:29	R	0	Reserved
28	R/W	0	USE_CNTL_SCL_LOW: If This bit is set to 1, then Bits[27:16] control the SCL low time.
27:16	R/W	0	SCL Low delay.
15:14	R	0	Unused
13-11	R/W	0	SCL_FILTER: A filter was added in the SCL input path to allow for filtering of slow rise times. 0 = no filtering, 7 = max filtering
10:8	R/W	0	SDA FILTER: A filter was added in the SDA input path to allow for filtering of slow rise times. 0 = no filtering, 7 = max filtering
7:0	R/W	0x00	SLAVE_ADDRESS. This is a 7-bit value for a 7-bit I²C device, or (0xF0 | {A9,A8}) for a 10-bit I²C device. By convention, the slave address is typically stored in by first left shifting it so that it's MSB is D7 (The I²C bus assumes the 7-bit address is left shifted one). Additionally, since the SLAVE address is always an 7-bit value, D0 is always 0. NOTE: The I²C always transfers 8-bits even for address. The I²C hardware will use D0 to dictate the direction of the bus. Therefore, D0 should always be '0' when this register is set.

I2C_M_0_TOKEN_LIST_REG0 0x2142

The register below describes the first 8 tokens in the token list.

Bit(s)	R/W	Default	Description
31:28	R/W	0x00	8th token in the list to process
27:24	R/W	0x00	7th token in the list to process
23:20	R/W	0x00	6th token in the list to process
19:16	R/W	0x00	5th token in the list to process
15:12	R/W	0x00	4th token in the list to process
11:8	R/W	0x00	3rd token in the list to process
7:4	R/W	0x00	2nd token in the list to process
3:0	R/W	0x00	1st token in the list to process (See the table below for token definitions)

Table VII.40.2 Token Definitions

Command Token	Value	Data	Description
END	0x0	N/A	Used to tell the I²C module that this is the end of the Token list. This token is not associated with the I²C bus, but rather with the state-machine that drives the token list processor.
START	0x1	N/A	The START Token is used to tell an I²C device that this is the beginning of an I²C transfer
SLAVE_ADDR-WRITE	0x2	7-bits	This bit-sequence is used to address a device and tell the device it is being WRITTEN
SLAVE_ADDR-READ	0x3	7-bits	This bit sequence is used to address a device and tell the device it is being READ.
DATA	0x4	8-bits	This 8-bit byte sequence is a byte transfer (READ or WRITE). The DATA token corresponds to a WRITE if it follows a SLAVE_ADDR-WRITE token. The DATA token corresponds to a READ if it follows a SLAVE_ADDR-READ token.
DATA-LAST	0x5	8-bits	Used to indicate the last 8-bit byte transfer is a byte transfer of a READ.
STOP	0x6	N/A	This tells the I²C device it is no longer being addressed

Write data associated with the DATA token should be placed into the I2C_TOKEN_WDATA_REG0 or I2C_TOKEN_WDATA_REG1 registers. Read data associated with the DATA or DATA-LAST token can be read from the I2C_TOKEN_RDATA_REG0 or I2C_TOKEN_RDATA_REG1 registers.

I2C_M_0_TOKEN_LIST_REG1 0x2143

Bit(s)	R/W	Default	Description
31:28	R/W	0x00	16th token in the list to process
27:24	R/W	0x00	15th token in the list to process
23:20	R/W	0x00	14th token in the list to process
19:16	R/W	0x00	13th token in the list to process
15:12	R/W	0x00	12th token in the list to process
11:8	R/W	0x00	11th token in the list to process
7:4	R/W	0x00	10th token in the list to process
3:0	R/W	0x00	9th token in the list to process

I2C_M_0_TOKEN_WDATA_REG0 0x2144

Bit(s)	R/W	Default	Description
31:24	R/W	0x00	4th data byte written for a DATA (write) token.
23:16	R/W	0x00	3rd data byte written for a DATA (write) token.
15:8	R/W	0x00	2nd data byte written for a DATA (write) token.
7:0	R/W	0x00	1st data byte written for a DATA (write) token.

I2C_M_0_TOKEN_WDATA_REG1 0x2145

Bit(s)	R/W	Default	Description
31:24	R/W	0x00	8th data byte written for a DATA (write) token.
23:16	R/W	0x00	7th data byte written for a DATA (write) token.
15:8	R/W	0x00	6th data byte written for a DATA (write) token.
7:0	R/W	0x00	5th data byte written for a DATA (write) token.

I2C_M_0_TOKEN_RDATA_REG0 0x2146

Bit(s)	R/W	Default	Description
31:24	R/W	0x00	4th data byte read for a DATA or DATA-LAST (READ) token.
23:16	R/W	0x00	3rd data byte read for a DATA or DATA-LAST (READ) token.
15:8	R/W	0x00	2nd data byte read for a DATA or DATA-LAST (READ) token.
7:0	R/W	0x00	1st data byte read for a DATA or DATA-LAST (READ) token.

I2C_M_0_TOKEN_RDATA_REG1 0x2146

Bit(s)	R/W	Default	Description
31:24	R/W	0x00	8th data byte read for a DATA or DATA-LAST (READ) token.
23:16	R/W	0x00	7th data byte read for a DATA or DATA-LAST (READ) token.
15:8	R/W	0x00	6th data byte read for a DATA or DATA-LAST (READ) token.
7:0	R/W	0x00	5th data byte read for a DATA or DATA-LAST (READ) token.

41. UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

41.1 Overview

There are a number of UART's in the chip that offer 2-wire (RX/TX) and 4-wire (RX/TX, CTS/RTS) connections at the digital I/O pins. Each UART contains one transmit FIFO and a receive FIFO (see depths below). The FIFO's are filled by the CPU and read by the CPU. In some cases, the receive FIFO can be configured to be pushed directly to DDR memory without CPU intervention.

Table VII.41.1 UART List

UART	RX/TX FIFO depths	RX FIFO DMA to DDR	Comment
UART0	128 bytes	Yes	Located in the EE domain
UART1	64 bytes	Yes	Located in the EE domain
UART2	64 bytes	Yes	Located in the EE domain
UART0-AO	64 bytes	No	Located in the Always On domain
UART2-AO	64 bytes	No	Located in the Always On domain

41.2 Features

Input filters: The CTS (clear to send) and RX (receive) input paths have input filters to deal with slow rise times. The filters are configurable to use a 125nS or 1uS sampling mechanism. There is an implied 3 system clock cycle delay (15nS for a typical system clock of 200Mhz) that is used to synchronize and detect the rising/falling edge of the RXD signal. The RXD signal may be passed through an optional filter to deglitch the external signal in noisy conditions. The deglitch filter has two settings which add to the ¡§detection delay¡¨ of the RXD signal by the internal logic:

- Filter setting 1 (125nS strobe): 375nS ~ 2.6uS
- Filter setting 2 (1uS strobe): 3uS ~ 21uS

The filter is described in the register specification. If the filter is disabled, the shortest RXD low time and high time is 12 system clock cycles (60nS for a system clock of 200Mhz).

Clear to Send: CTS is a signal sent from the receiver UART back to the transmitting UART to tell the transmitting UART to stop sending data. The CTS signal must be received before the next START symbol is sent. The transmitting UART is allowed to send one more byte after the CTS signal is recognized. The CTS signal coming into the chip goes through some synchronization and detection which adds an additional 5 system clocks (typically 25nS for a 200Mhz system clock). This setup time for CTS detection is called CTS_{stop}. The CTS input also has an optional filter can be used to deglitch the incoming CTS signal. If the filter is disabled, the CTS signal must be de-asserted 5 system clock cycles before the start of the next BYTE transfer. If the CTS filter is enabled, then additional time must be added to the 25nS requirement. There are two programmable filter settings that effectively delay CTS being seen by the internal logic:

- Filter setting 1 (125nS strobe): 375nS ~ 2.6uS
- Filter setting 2 (1uS strobe): 3uS ~ 21uS

Interrupts: The UARTs can generate interrupts if the receive FIFO exceeds a pre-programmed threshold. An interrupt can also be generated if there is a frame or parity error.

Clock independent operation: Because the system clock can be altered to accommodate dynamic frequency scaling, the UARTs have an option in which they use the 24Mhz crystal clock as the source for the UART.

41.3 Functional Description

The UART requires that a Baud Rate be established. The UART supports rates as slow as 1Hz up to rates as high as 8 MBits/Sec. Once the baud rate has been established, bytes are transmitted as they are written to the transmit-FIFO by the CPU. A large transmit-FIFO exists to allow the CPU to pre-load a transmit package because the CPU can often write faster than the UART can transmit the data.

Data this automatically received by the UART is placed into the receive FIFO one byte at a time. The receive-FIFO decouples the UART from the CPU allowing the CPU to read the UART byte data at a rate not dictated by the UART.

Fig VII.41.1 UART Timing Diagram

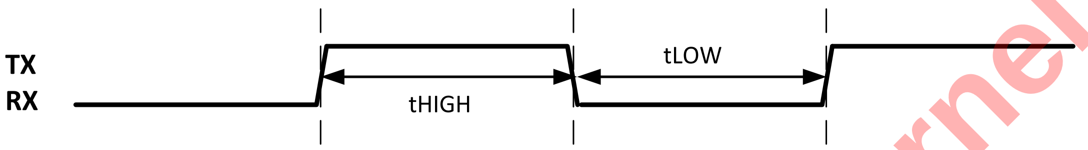


Table VII.41.2 UART Timing Specification

Symbol	Description	Min.	Max.	Unit	Notes
tHIGH	TX/RX high time	60ns	167ms		
tLOW	TX/RX low time	60ns	167ms		

41.4 Register Description

The following register definition is uniformly applied to all UART instantiations in the chip.

Table VII.41.3 UART Register List

Instantiations	Base Address
UART0	0xc11084c0 ~ 0xc11084d4
UART1	0xc11084dc ~ 0xc11084f0
UART2	0xc1108700 ~ 0xc1108714
UART0-AO	0xc81004c0 ~ 0xc81004d4
UART2-AO	0xc81004e0 ~ 0xc81004f4

UARTx_WFIFO: Write data

Bit(s)	R/W	Default	Description
31-8	R	0	unused
7-0	R/W	-	Write FIFO data. The Write FIFO holds 64 bytes. The Write FIFO can be written as long as it is not full.

UARTx_RFIFO: Read Data

Bit(s)	R/W	Default	Description
31-8	R	0	unused
7-0	R/W	-	Read FIFO data. The Read FIFO holds 64 bytes. The empty flag can be used to determine if data is available

UARTx_CONTROL: UART Mode

Bit(s)	R/W	Default	Description
31	R/W	0	Invert the RTS signal
30	R/W	0	Mask Error: Set to 1 to mask errors
29	R/W	0	Invert the CTS signal
28	R/W	0	Transmit byte Interrupt: Set to 1 to enable the generation an interrupt whenever a byte is read from the transmit FIFO
27	R/W	0	Receive byte Interrupt: Set to 1 to enable the generation an interrupt whenever a byte is written to the receive FIFO

Bit(s)	R/W	Default	Description
26	R/W	0	Set to 1 to invert the TX pin
25	R/W	0	Set to 1 to invert the RX pin
24	R/W	0	Clear Error
23	R/W	0	Reset the receive state machine
22	R/W	0	Reset the transmit state machine
21-20	R/W	0	Character length: 00 = 8 Bits, 01 = 7 Bits, 10 = 6 Bits, 11 = 5 Bits
19	R/W	1	Parity Enable: Set to 1 to enable parity
18	R/W	0	Parity type: 0 = even, 1 = odd
17-16	R/W	0	Stop bit length: 00 = 1 bit, 01 = 2 Bits
15	R/W	0	Two Wire mode:
14	R/W	0	Unused
13	R/W	0	Receive Enable. Set to 1 to enable the UART receive function
12	R/W	0	Transmit Enable. Set to 1 to enable the UART transmit function
11-0	R/W	0x120	Baud rate: This value sets the baud rate by dividing the MPEG system clock.

UARTx_STATUS: UART Status

Bit(s)	R/W	Default	Description
31-27	R	0	Unused
26	R	0	UART_RECV_BUSY: This bit will be 1 if the uart receive state machine is busy
25	R	0	UART_XMIT_BUSY: This bit will be 1 if the uart transmit state machine is busy
24	R	0	RECV_FIFO_OVERFLOW:
23	R	0	CTS Level
22	R	0	Transmit FIFO Empty
21	R	0	Transmit FIFO Full
20	R	0	Receive FIFO empty
19	R	0	Receive FIFO full
18	R	0	This bit is set if the FIFO is written when it is full. To clear This bit, wriTE bit 24 of register 0x2132
17	R	0	Frame error. To clear This bit, wriTE bit 24 of register 0x2132
16	R	0	Parity error. To clear This bit, wriTE bit 24 of register 0x2132
15	R	0	Unused
14-8	R	0	Transmit FIFO count. Number of bytes in the transmit FIFO
7	R	0	Unused
8-0	R	0	Receive FIFO count. Number of bytes in the receive FIFO

UARTx_MISC: UART IRQ CONTROL

Bit(s)	R/W	Default	Description
31	R/W	0	Added a "just in case" bit that can be set to 1 to enable clocks always. The default is 0 meaning the auto-clock gating logic is enabled.
30	R/W	0	USE old Rx Baud: There was a bug in the RX baud rate generator. The Rx baud rate generator was re-designed to compute a baud rate correctly. If you want to use the old (stupid) logic, you can set This bit to 1.
29	R/W	0	ASYNC_FIFO_PURGE: This bit can be set to 1 after all UART bytes have been received in order to purge the data into the Async FIFO. This bit is needed because the UART receives 8-bit data, but the ASYNC FIFO can only be written with 16-bit data. In this case there might be a residual byte if the UART is not receiving an even number of bytes.
28	R/W	0	ASYNC_FIFO_EN: If This bit is set to 1, then the UART received data is automatically sent to the Async FIFO module which will in turn automatically send the data to DDR memory
27	R/W	0	CTS: Filter Timebase select: 1 = 1uS, 0 = 111nS timebase. A filter was added to the CTS input to allow for a little digital filtering. The amount of filtering is controlled by this timebase (longer = more filtering) and the value in Bits FILTER_SEL below.
26-24	R/W	0	CTS: FILTER_SEL: 0 = no filter, 7 = max filtering
23-20	R/W	0	BAUD_RATE_EXT: These 4 Bits extend the baud rate divider to 16-bits: Baud Rate = {Reg4[23:20],Reg2[11:0]}
19	R/W	0	RX: Filter Timebase select: 1 = 1uS, 0 = 111nS timebase. A filter was added to the RX input to allow for a little digital filtering. The amount of filtering is controlled by this timebase (longer = more filtering) and the value in Bits FILTER_SEL below.
18-16	R/W	0	RX: FILTER_SEL: 0 = no filter, 7 = max filtering
15-8	R/W	32	XMIT_IRQ_CNT: The UART can be configured to generate an interrupt if the number of bytes in the transmit FIFO drops below this value.
7:0	R/W	15	RECV_IRQ_CNT: The UART can be configured to generate an interrupt after a certain number of bytes have been received by the UART.

UARTx_REG5

Bit(s)	R/W	Default	Description
31-24	R/W	0	unused

Bit(s)	R/W	Default	Description
24	R/W	0	USE_XTAL_CLK: If This bit is set, then the clock for generating the UART Baud rate comes from the crystal pad. This allows the UART to operate independent of clk81.
23	R/W	0	USE New Baud rate. Over the years, the baud rate has been extended by concatenating Bits from different registers. To take advantage of the full 23-bit baud rate generate (extended to 23 Bits to accommodate very low baud rates), you must set This bit. If This bit is set, then the baud rate is configured using Bits [22:0] below
22:0	R/W	15	NEW_BAUD_RATE: If Bit[23] = 1 above, then the baud rate for the UART is computed using these Bits.

42. INFRARED REMOTE

42.1 Overview

An IR signal based Remote Control (RC) signal decoder and blaster are built in S905 to provide software a low-cost, convenient way to implement remote control function in applications. This module is located in the AO power domain.

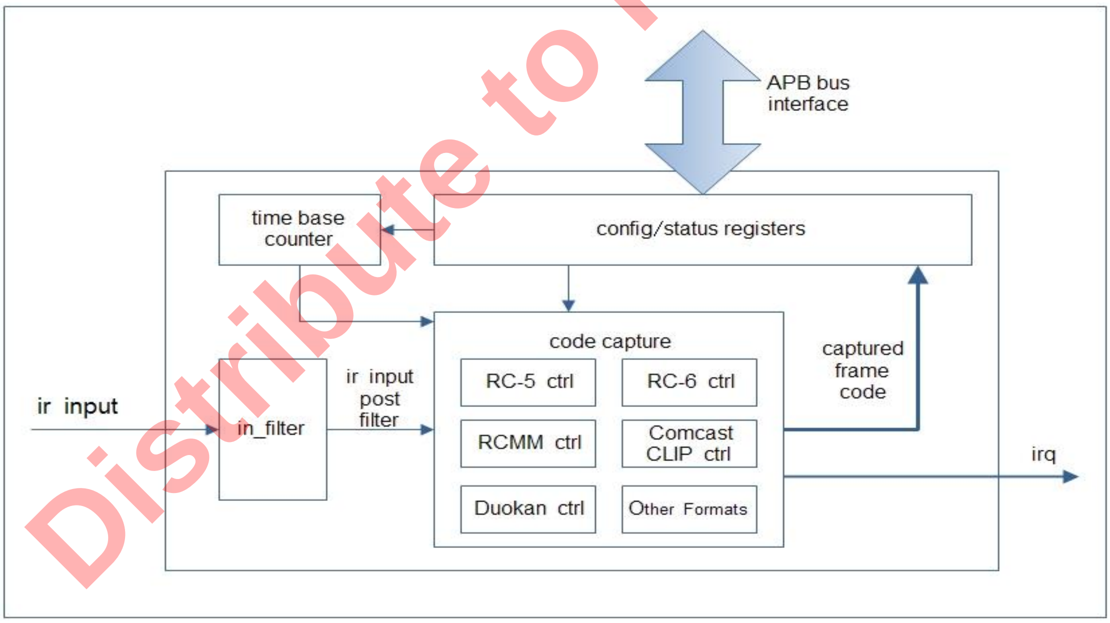
42.2 Decoder Functional Description

The decoder mainly consisted of two blocks:

- Decoder with input filter
- A set of registers including control & clock, data and tuning

The function diagram of IR decoder is illustrated in the figure below.

Fig VII.42.1 IR Decoder Function Block



IR Decoder decodes the IR remote control input signal. 13 operation modes are supported:

- Hardware Decode IR transmission protocol compatible frame decoder mode (NEC MITSUBISHI Thomson Toshiba Sony SIRC RC5 RC6 RCMM Duokan Comcast Sanyo Modes)
- General programmable time measurement frame decoder mode (General Mode)

In Hardware Decode Mode, the Decoder uses signal pattern search mechanism to decode data frame. It can detect logical ‘0’ ,‘1’ ,“00”,”01”,”10” and ”11”, as well as data frame start and end. Whenever Decoder detects and decodes the data frame, the data are kept in data register.

In General Mode, the Decoder uses edge detection mechanism to decode data frame. It can detect each input signal edge and record the time between two edges. The time measurement result is kept in control register.

The user should set proper operation mode corresponding to the selection of remote controller.

There is a simple time-based signal Filter between the signal input and the Decoder. The Filter is programmable and helps to improve signal integrity.

42.3 NEC Infrared Transmission Protocol Example

Message Bit

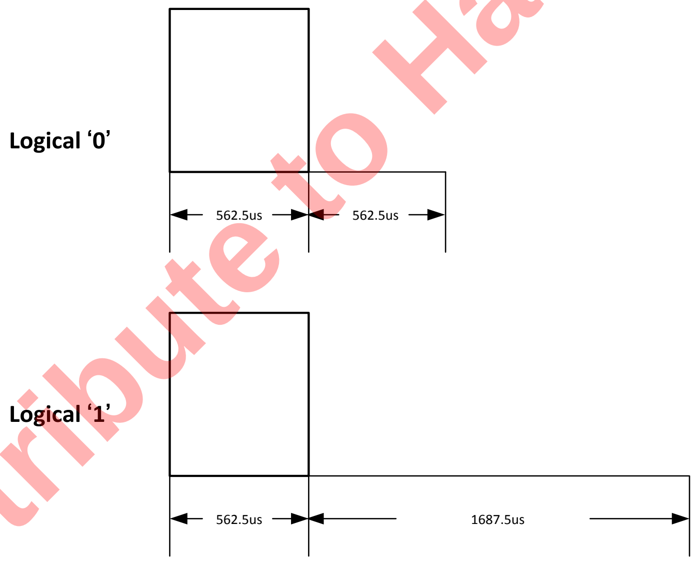
Standard NEC IR transmission protocol uses pulse distance encoding of the message Bits. The basic clock circle time is 562.5us.

The logical Bits are defined and transmitted as follow:

- Logical '0' – a 562.5us pulse burst (1 clock) followed by a 562.5us space (1 clock). The total transmit time is 1.125ms.
- Logical '1' – a 562.5us pulse burst (1 clock) followed by a 1.6875ms space (3 clocks). The total transmit time is 2.25ms.

The signals are illustrated in the picture below.

Fig VII.42.2 Message Bit Signal



Data Frame

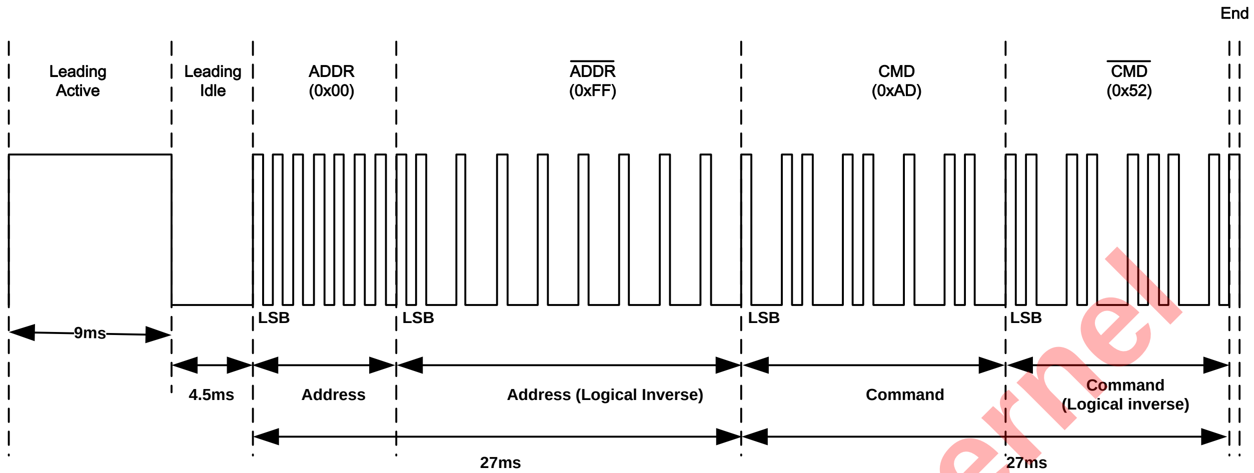
A data transmit frame is exchanged via IR to represent a message when a key is pressed on the remote control. Typically, the data frame consists of, in order:

- A Leading Active – 9ms pulse burst (16 clocks)
- A Leading Idle – 4.5ms space (8 clocks)
- An 8-bit receiver address (ADDR), LSB first.
- The complementary 8-bit receiver address (), LSB first
- An 8-bit command (CMD), LSB first
- The complementary 8-bit command (), LST first
- A final 562.5us pulse burst to indicate the end of message transmission.

The byte ADDR/ and CMD/ are sent with least significant bit (LSB) first.

The example of data frame is illustrated below with ADDR=0x00 and CMD=0xAD.

Fig VII.42.3. Data Frame



Repeat Code(s)

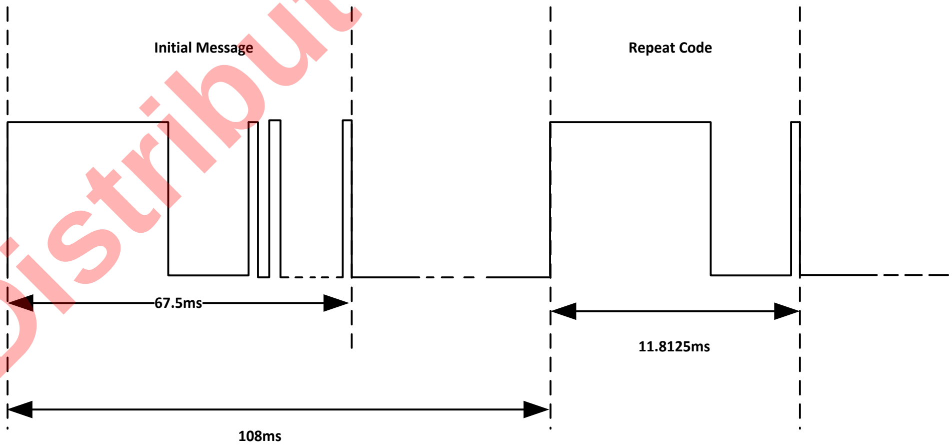
A repeat code will be issued if the key on the remote controller is kept pressed. A repeat code will continue to be sent out at 108ms intervals until the key is released.

Typically, the repeat code consists of, in order:

- A Leading Active – 9ms pulse burst (16 clocks)
- A Leading Idle – 2.25ms space (4 clocks)
- A final 562.5us pulse burst to indicate the end of message transmission.

The example of repeat code is illustrated below

Fig VII.42.4. Repeat Code



42.4 Register Description

AO_MF_IR_DEC_LDR_ACTIVE: Leader Active control 0xc8100580

This register controls the min/max Leader Active time window. For example, for NEC format, the Leader Active time is about 9mS. To identify a Leader Active time between 8.60 mS and 9.40 mS (assuming base resolution = 20uS), user can set Max duration = 0x1d6 (‘d470) to represent 9.40 mS, and set Min duration = 0x1ae (‘d430) to represent 8.60 mS.

Bit(s)	R/W	Default	Description
31-29	R	0	Unused
28-16	R/W	0	Max duration of Leader's active part
15-13	R	0	Unused
12-0	R/W	0	Min duration of Leader's active part

AO_MF_IR_DEC_LDR_IDLE: Leader Idle control 0xc8100584

Bit(s)	R/W	Default	Description
31-29	R	0	Unused
28-16	R/W	0	Max duration of Leader's idle part
15-13	R	0	Unused
12-0	R/W	0	Min duration of Leader's idle part

AO_MF_IR_DEC_LDR_REPEAT: Repeat Leader Idle Time 0xc8100588

Bit(s)	R/W	Default	Description
31-26	R	0	Unused
25-16	R/W	0	Max duration of Repeat Code's Leader. In NECformat, it defines for the repeat leader's idle part. In Toshiba format, it defines for the repeat leader's second idle part (In Toshiba format, the repeat leader's first idle part has the same duration time as the normal leader idle part.)
15-10	R	0	Unused
9-0	R/W	0	Min duration of Repeat Code's Leader

AO_MF_IR_DEC_BIT_0: 0xc810058C

Bit(s)	R/W	Default	Description
31-26	R	0	Unused
25-16	R/W	0	Max duration of Duration Setting Regiser 0. It defines max tining duration for: Logic"0" for NEC/Toshiba/Sony/Thomas format or Half trailer bit for RC6 format (RC6's half trailer bit typically 888.89us) or time of Duokan/RCMM/4ppm format's Logic "00"
15-10	R	0	Unused
9-0	R/W	0	Min duration of Duration Setting Regiser 0.

AO_MF_IR_DEC_REG0: 0xc8100590

Bit(s)	R/W	Default	Description
31	R/W	0	Clock gating control just in case. Set 1 can force clock gating disabled.
30-28	R/W	0	Filter ctrl. Set the monitor timing for input filter, bigger value means longer monitor time. Value 0 = no filtering.
27-25	R	0	Unused
24-12	R/W	0	Max frame time. Max duration of one whole frame.
11-0	R/W	0	Base time parameter. Used to generate the timing resolution. Resolution = (base_time_paramter + 1) * (1/ Freq_sys_clk). For example, if Frequency of sys_clk is 1Mhz, and base_time_parameter=19, Then resolution = (19+1)*(1uS) = 20uS.

AO_MF_IR_DEC_STATUS: 0xc8100598

Bit(s)	R/W	Default	Description
31	R/W	0	Frame data valid 1. (This bit is set to 1 when a captured frame is updated/stored into "FrameBody_1" register. A read of "**FrameBody_1**" register will clear This bit. "FrameBody_1" register is used to store the over 32bit MSBs of the formats whose length is more than 32 bit)

Bit(s)	R/W	Default	Description
30	R/W	0	bit_1_match_en. Set to 1 to enable the check of whether logic"1" bit matches timing configure during the frame input process.
29-20	R/W	0	Max Duration 1. Max duration of Duration Setting Regiser 1. It defines max duration for: Logic"1" for NEC/Toshiba/Sony format or Whole trailer bit for RC6 format (RC6's whole trailer bit typically 1777.78us) or time of Duokan/RCMM/4ppm format's Logic "01"
19-10	R/W	0	Min Duration 1. Min duration of Duration Setting Regiser 1.
9	R	0	irq_status. Appear as 1 if there is an interrupt.
8	R	0	ir_i_sync. IR remote serial input after synchronization. This is the level of the digital signal coming into the IR module for decoding. This is the same as reading the I/O pad level.
7	R	0	Busy. When =1, means state machine is active.
6-4	R	0	Decoder_status (for debug only). 000: OK 001: last frame timed out 010: leader time error (invalid IR signal) 011: repeat error (repeat leader, but other IR transitions found). 100: Invalid bit
3-0	R	0	Frame status. bit 3: Frame data valid (This bit is set to 1 when a captured frame is updated/stored into "FrameBody" register. A read of "**FrameBody**" register will clear This bit. If store and read occurs at the same time, This bit is set to 1 in common, But if "Hold first" is set to true and this valid Bit is already 1, a read clear takes precedance and This bit is clear to 0.) bit 2: data code error (data != ~data in IR bit stream) bit 1: custom code error (custom_code != ~custom_code in IR bit stream) bit 0: 1 = received frame is repeat key, 0 = received frame is normal key

AO_MF_IR_DEC_REG1: 0xc810059C

Bit(s)	R/W	Default	Description
31	R/W	0	Set to 1 to use faster timebase. .
30	R/W	0	cntl_1us_eq_clk. Just use sys_clk to relace 1uS tick.
29	R/W	0	cntl_xtal3_eq_clk. Just use sys_clk to relace 111ns tick.
28-16	R	0	Pulse Width Counter. It stores the internal counter of pulse width duration. Commonly used as time measurement when **decode_mode** is set to measure width mode (software decode). Time measurement starts at the last time the internal time counter was reset by the rising and/or falling edge of the IR signal. The selection of reset on rising and/or falling edge is determined by the **IRQ Selection** field (Bits 3-2 below)
15	R/W	0	Enable. 1 = enable the state machine of IR decoder. 0 = disable the state machine of IR decoder.
14	R/W	0	cntl_use_sys_clk. Use sys_clk for the timebase. It's useful when sys_clk at low frequency (such as 32Khz) and cannot create 1uS timebase tick. 1 = use the system clock as timebase. 0 = use the 1uS timebase tick as timebase.
13-8	R/W	0	bit_length minus 1. (N-1). Used to set the value of frame body's bit length (frame body commonly includes address and data code part). If a format has 24 bit frame body, this value shall be set to 23.
7	R/W	0	Record_at_error. 1= record the frame body and status forcibly, even if data/custom code error check enabled by frame_mask and relative error occurs. 0 = if data/custom code error check enabled by frame_mask and relative error occurs, not record the frame body and status forcibly

Bit(s)	R/W	Default	Description
6	R/W	0	Hold_first Used to hold the first captured frame data. If This bit is set to 1, then the "**FrameBody/FrameBody_1**" register will only be updated if hasn't already been updated. Once updated, the "**FrameBody/FrameBody_1**" register will not be updated again until it has been read. This bit can be used to guarantee the first TV remote code captured will not be overwritten by subsequent transmissions from a TV remote. **NOTE: Read the"FrameBody" register can clear the internal "Frame data valid" flag, and read the "FrameBody_1" register can clear the "Frame data valid 1" flag.**
5-4	R/W	0	Frame_mask. Some formats' body include bit-inversed data or custom/address code for error check. 00 = ignore error check from either data or custom/address code 01= check if data code matches its inverse values, ignore error check from custom/address code 10= check if custom/address code matches its inverse values, ignore error check from data code 11= check if data and custom codes match their inverse values
3-2	R/W	0	Irq_sel. IRQ Selection and width measurement reset: 00: IR Decoder done 01: IR input rising or falling edge detected 10: IR input falling edge detected 11: IR rising edge detected
1	R/W	0	IR input polarity selection. Used to adjust/invert the polarity of IR input waveform.
0	R/W	0	Decoder Reset. Set to 1 to reset the IR decoder. This is useful because the IR remote state machine thinks in terms of milliseconds and may take tens of milliseconds to return to idle by itself.

AO_MF_IR_DEC_REG2 0xc81005A0

Bit(s)	R/W	Default	Description
31-27	R	0	Unused
26	R/W	0	Width_low_enable. Enable counter record of low pulse width duration. 0 = do not force enable of width low counter record 1 = force enable of width low counter record Some IR formats' decoding need to use internal width low counter record. By default, the width low counter record is enabled automatically for related formats. This bit is used for enable forcibly just in case. Besides, if "leader plus stop bit" method is enabled for repeat detection, This bit is also need to be enabled.
25	R/W	0	Width_high_enable. Enable counter record of high pulse width duration. 0 = do not force enable of width high counter record 1 = force enable of width high counter record Some IR formats' decoding need to use internal width high counter record. By default, the width high counter record is enabled automatically for related formats. This bit is used for enable forcibly just in case.
24	R/W	0	Enable "leader plus stop bit" method for repeat detection. 0 = "leader plus stop bit" method disabled 1 = "leader plus stop bit" method enabled Some IR formats use one normal frame's leader followed by a stop bit to represet repeat. There is no frame data in this kind repeat frame. To use this method, **width_low_enable** (Bit 26 of 0x20 offset register) shall be set to 1, and **max_duration_3** and **min_duration_3** in 0x28 offset register shall be set to appropriate value for stop bit's timing duration.
23-22	R	0	Unused
21-16	R/W	0	Repeat_Bit_index. These Bits are used for compare bit method to set the index of the bit that is used as repeat flag. The index value can be 0 to 63. Compare bit method is one of the methods for repeat detection . Some IR formats use one bit in frame to represet whether the frame is repeat.
15	R/W	0	Running_count_tick_mode. This bit is only valid when **use_clock_to_counter** Bit is 0. 0 = use 100uS as increasing time unit of frame-to-frame counter 1 = use 10uS as increasing time unit of frame-to-frame counter
14	R/W	0	Use_clock_to_counter. If This bit is set to 1, the **running_count_tick_mode** Bit is ignored. 0 = do not use system clock as increasing time unit of frame-to-frame counter 1 = use system clock as increasing time unit of frame-to-frame counter

Bit(s)	R/W	Default	Description
13	R/W	0	Enable frame-to-frame time counter (running-counter). 0 = frame-to-frame time counter disabled 1 = frame-to-frame time counter enabled If enabled, the frame-to-frame counter increases every 100uS or 10uS until it reaches its max value(all Bits are 1) or it is reset. When it reaches its max value, it keeps the value until it is reset. When it is reset, it becomes zero and then begin increasing again. The counter can be reset even when it has not reached its max value. The increasing time unit can be 100uS or 10uS or system clock frequency which is set by **running_count_tick_mode** and **use_clock_to_counter** settings. When a frame's data are capured and stored into FrameBody/FrameBody_1 register, frame-to-frame counter is reset to zero. After reset to zero, the frame-to-frame counter will begin increasing again, until it reaches its max value or it is reset. For repeat frame detection, users can use hardware detection by enabling compare frame or compare bit method, or users can read frame-to-frame counter to let software to make the decision.
12	R/W	0	Enable repeat time check for repeat detection. This bit is valid only when compare frame method or compare Bit method is enabled. 0 = repeat time check disabled 1 = repeat time check enabled When repeat frame detection is enabled by enabling compare frame or compare Bit method, the frame time interval may need to be checked in order to decide whether the frames are repeat (key pressed without release) or not. You can configure the **repeat_time_max** value by setting **0x38 offset** register. If frame interval is smaller than the "repeat time max", it may considered as repeat. If frame interval is bigger than the "repeat time max", it is considered as not repeat.
11	R/W	0	Enable compare frame method for repeat detection. 0 = compare frame method disabled 1 = compare frame method enabled Some IR formats transer the same data frame as repeat frame when the key is kept pressed without release. For repeat detection, compare frame method can be used. If a new frame and the old received frame are the same and the repeat time is under the limit(frame-to-frame time counter value is smaller than the repeat_time_max), the status register's **frame_status0** is set to 1 automatically as repeat detected flag. You can configure the **repeat_time_max** value by setting **0x38 offset** register.
10	R/W	0	Enable compare Bit method for repeat detection. 0 = compare Bit method disabled 1 = compare Bit method enabled Some IR formats use only one bit to represet whether the frame is repeat. You can compare only one bit instead of compare the whole frame for repeat detection. If compare frame method is enabled, then This bit is ignored.
9	R/W	0	Disable read-clear of FrameBody/FrameBody_1. 0 = read-clear enabled 1 = read-clear disabled FrameBody/FrameBody_1 registers are read-cleared in default. When these register are read, they are cleared to zero. This bit is used to disable this read-clear feature. (FrameBody/FrameBody_1 registers are used to store captured frame data).
8	R/W	0	input stream bit order. 0 = LSB first mode (first bit in input stream is considered as LSB) 1= MSB first mode (first bit in input stream is considered as MSB) Note: Commonly the following formats shall set 1 to enable MSB first mode (unless you insist on LSBfirst mode for your specified use): RC5, RC5 extend, RC6, RCMM, Duokan, Comcast
7:4	R	0	Unused
3:0	R/W	0	Decode_mode.(format selection) 0x0 =NEC 0x1= skip leader (just Bits, without leader) 0x2=General time measurement (measure width, software decode) 0x3=MITSUBISHI 0x4=Thomson 0x5=Toshiba 0x6=Sony SIRC 0x7=RC5

Bit(s)	R/W	Default	Description
			0x8=Reserved 0x9=RC6 0xA=RCMM 0xB=Duokan 0xC=Reserved 0xD=Reserved 0xE=Comcast 0xF=Sanyo

AO_MF_IR_DEC_DURATN2 0xc81005A4

Bit(s)	R/W	Default	Description
31-26	R	0	Unused
25-16	R/W	0	Max duration of Duration Setting Regiser 2. It defines max duration for: Half bit for RC5/6 format (RC5 typically 888.89us for half bit, RC6 typically 444.44us) or time of Duokan/RCMM/4ppm format's Logic "10" or time of Comcast/16ppm's base duration
15-10	R	0	Unused
9-0	R/W	0	Min duration of Duration Setting Regiser 2.

AO_MF_IR_DEC_DURATN3 0xc81005A8

Bit(s)	R/W	Default	Description
31-26	R	0	Unused
25-16	R/W	0	Max duration of Duration Setting Regiser 3. It defines max duration for: Whole bit for RC5/6 format (RC5 typically 1777.78us for whole bit, RC6 typically 888.89us) or time of Duokan/RCMM/4ppm format's Logic "11" or time of Comcast/16ppm's offset duration
15-10	R	0	Unused
9-0	R/W	0	Min duration of Duration Setting Regiser 3.

AO_MF_IR_DEC_REG3 0xc81005B8

Bit(s)	R/W	Default	Description
31-20	R	0	Unused
19-0	R/W	0	Repeat time max. Used to set the maximum time between two repeat frames for repeat frame detection. Time unit is 100uS or 10uS according to the running_count_tick_mode. When repeat frame detection is enabled by enabling compare frame or compare Bit method, the frame time interval may need to be checked in order to decide whether the frames are repeat (key pressed without release) or not. If frame interval is smaller than the "repeat time max", it may considered as repeat. If frame interval is bigger than the "repeat time max", it is considered as not repeat.

AO_MF_IR_DEC_FRAME: Frame Body (Frame Data, LSB 32Bit) 0xc8100594

Note: New keys will be ignored until ***FrameBody*** register is read if the *hold first key* Bit is set in the decode control register. Reading this register resets an internal frame data valid flag.

Bit(s)	R/W	Default	Description
31-0	R	0	32 bit Read-Only register stores frame body (LSB 32 bit) captured from IR remote data flow, commonly includes custom/address code and data code.

AO_MF_IR_DEC_FRAME: Frame Body 1 (Frame Data, MSB 32Bit) 0xc81005AC

Note: New keys will be ignored until ***FrameBody*** register is read if the *hold first key* Bit is set in the decode control register. Reading this register resets an internal frame data valid flag.

Bit(s)	R/W	Default	Description
31-0	R	0	Stores frame body excess 32 bit range. (MSB 32 bit)

AO_MF_IR_DEC_STATUS_1 0xc81005B0

Bit(s)	R/W	Default	Description
31-20	R	0	Unused
19-0	R	0	Stores the last frame-to-frame counter value before the last counter reset caused by the last frame data record/update.

AO_MF_IR_DEC_STATUS_2 0xc81005B4

Bit(s)	R/W	Default	Description
31-20	R	0	Unused
19-0	R	0	Stores the value of the frame-to-frame counter which is running currently.

IR_BLASTER_CNTL0 0xc81000c0

Bit(s)	R/W	Default	Description
31-27	R	0	unused
26	R	-	BUSY: If This bit is 1, then the IR Blaster module is busy.
25	R	-	This output is 1 when the FIFO is Full
24	R	-	This output is 1 when the FIFO is Empty
23-16	R	-	FIFO Level
15-14	R/W	0	Unused
13-12	R/W	0	MODULATOR_TB: This input controls the clock used to create the modulator output. The modulator is typically run between 32khz and 56khz. The modulator output will equal a divided value of the following: 00: system clock “clk” 01: mpeg_xtal3_tick 10: mpeg_1uS_tick 11: mpeg_10uS_tick
11-4	R/W	0	SLOW_CLOCK_DIV: This is a divider value used to divide down the input “clk”. The divider is N+1 so a value of 0 equals divide by 1.
3	R/W	0	SLOW_CLOCK_MODE: Set this signal high to use a special mode in which the “clk” input is driven by a slow clock less than 1Mhz. This is used for low power cases where we want to run the IR Blaster between 32khz and 1Mhz
2	R/W	0	INIT_LOW: Setting This bit to 1 initializes the output to be high. Please set This bit back to 0 when done
1	R/W	0	INIT_LOW: Setting This bit to 1 initializes the output to be low. Please set This bit back to 0 when done
0	R/W	0	ENABLE: 1 = Enable. If This bit is set to 0, then the IR blaster module is reset and put into an IDLE state.

IR_BLASTER_CNTL1 0xc81000c4

Bit(s)	R/W	Default	Description
31-28	R/W	0	unused
27-16	R/W	0	This value is used with “modulator_tb[1:0]” above to create a low pulse. The time is computed as (mod_lo_count+1) x modulator_tb. The purpose for having a low/high count is the modulator output might not be 50% duty cycle. Hi/Lo counters allow us to modulate using a non-50% duty cycle waveform.
15-12	R/W	0	Unused
11-0	R/W	0	This value is used with “modulator_tb[1:0]” above to create a high pulse. The time is computed as (mod_hi_count+1) x modulator_tb

IR_BLASTER_CNTL2 0xc81000c8

Bit(s)	R/W	Default	Description
31-17	R	0	unused
16	W	0	Set This bit to 1 to write the data below to the FIFO
15-12	R	0	Unused
11-0	R/W	0	FIFO data to be written: Bit[12] output level (or modulation enable/disable: 1 = enable) Bit[11:10] Timebase: 00 = 1uS 01 = 10uS 10 = 100uS 11 = Modulator clock Bit[9:0] Count of timebase units to delay

43. PULSE-WIDTH MODULATION

43.1 Overview

The chip has 4 PWM modules that can be connected to various digital I/O pins, among which 3 are in EE domain and 1 is in AO domain. Each PWM is driven by a programmable divider driven by a 4:1 clock selector. The PWM signal is generated using two 16-bit counters. One is the High and Low counter, which is individually programmable with values between 1 and 65535. Using a combination of the divided clock (divide by N) and the HIGH and LOW counters, a wide number of PWM configurations are possible. The other is delta-sigma couter, generate 18-birt sigma, the PWM-out is the highest sigma. The PWM outputs vs counters are also illustrate below.

Fig VII.43.1 PWM Block Diagram

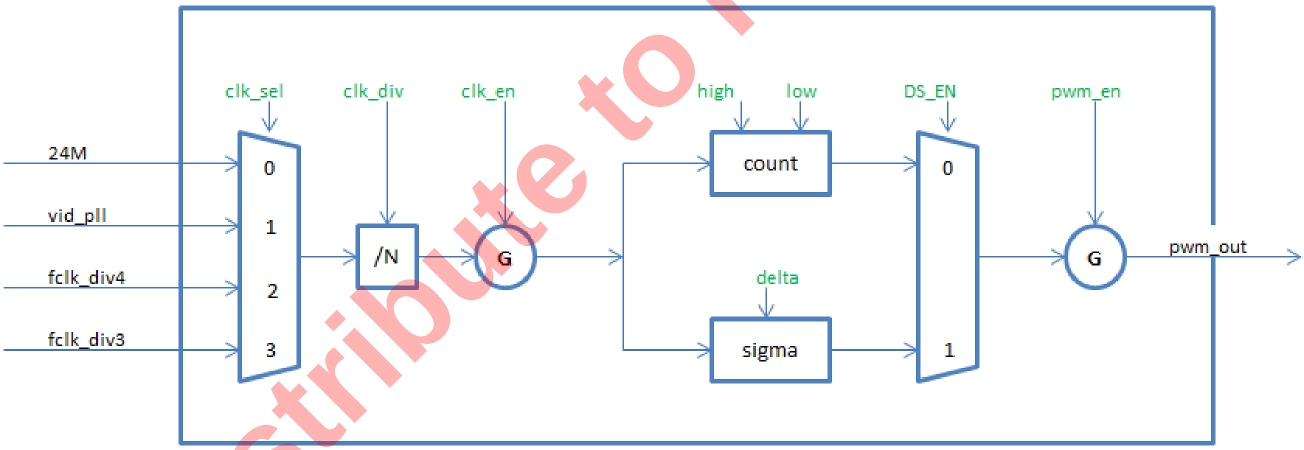


Fig VII.43.2 High/Low counter

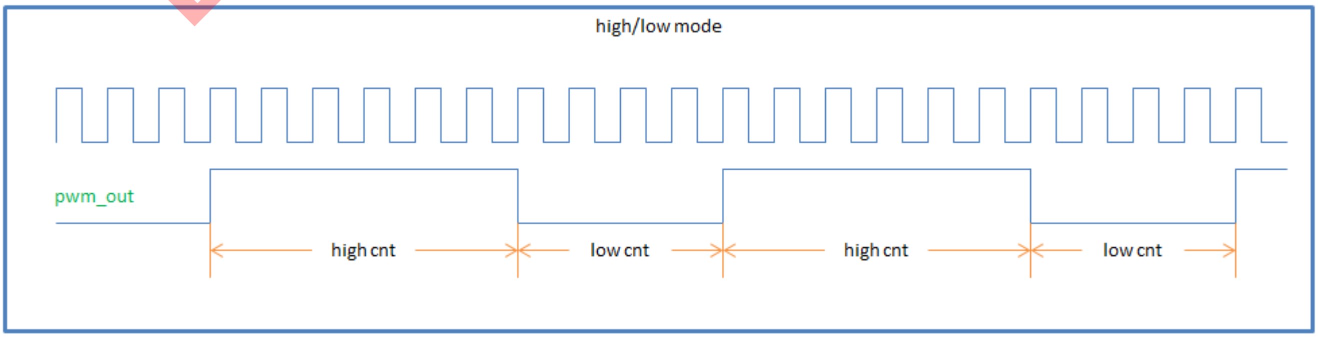
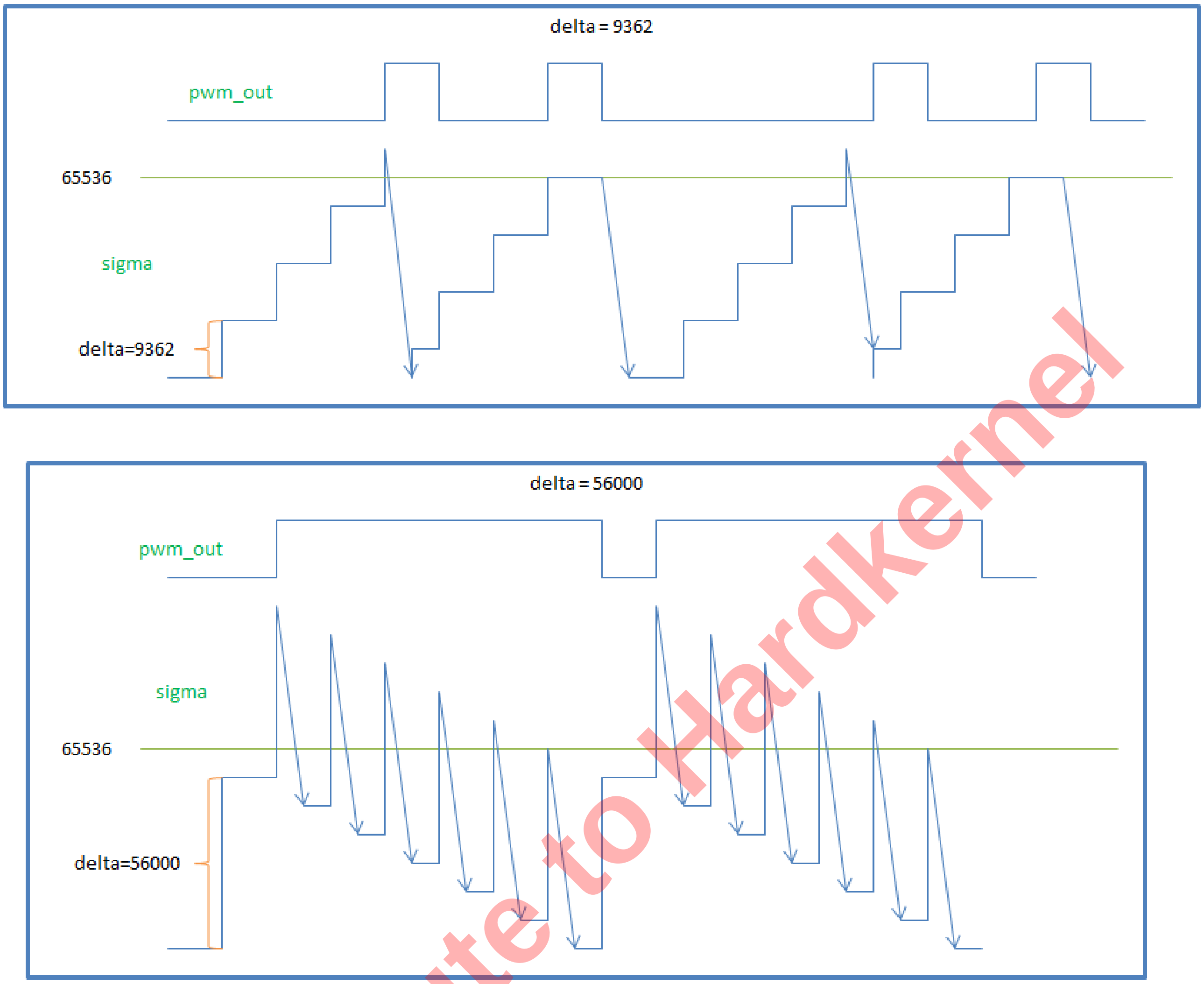


Fig VII.43.3 Delta-sigma conter, delta = 9362 & delta = 56000



43.2 Register Description

Each PWM module contains two PWM generators call A and B, and controlled by 4 registers.

For PWM modules in EE domain, the each register's final address = 0xc1100000 + offset*4

PWM_PWM_A 0x2154

Bit(s)	R/W	Default	Description
31-15	R/W	0	PWM_A_HIGH: This sets the high time (in clock counts) for the PWM_A generator output
15-0	R/W	0	PWM_A_LOW: This sets the high time (in clock counts) for the PWM_A generator output

PWM_PWM_B 0x2155

Bit(s)	R/W	Default	Description
31-15	R/W	0	PWM_B_HIGH: This sets the high time (in clock counts) for the PWM_A generator output

Bit(s)	R/W	Default	Description
15-0	R/W	0	PWM_B_LOW: This sets the high time (in clock counts) for the PWM_A generator output

PWM_MISC_REG_AB 0x2156

Bit(s)	R/W	Default	Description
31-24	R	0	Unused
23	R/W	0	PWM_B_CLK_EN: Set This bit to 1 to enable PWM A clock
22-16	R/W	0	PWM_B_CLK_DIV: Selects the divider (N+1) for the PWM A clock. See the clock tress document
15	R/W	0	PWM_A_CLK_EN: Set This bit to 1 to enable PWM A clock
14-8	R/W	0	PWM_A_CLK_DIV: Selects the divider (N+1) for the PWM A clock. See the clock tress document
7-6	R/W	0	PWM_B_CLK_SEL: Select the clock for the PWM B. See the clock tress document
5-4	R/W	0	PWM_A_CLK_SEL: Select the clock for the PWM A. See the clock tress document
3	R/W	0	DS_B_EN: This bit is only valid if PWM_B_EN is 0: if This bit is set to 1, then the PWM_B output is configured to generate a delta sigma output based on the settings in the register below. If This bit is set to 0, then the PWM_B output is set low.
2	R/W	0	DS_A_EN: This bit is only valid if PWM_A_EN is 0: if This bit is set to 1, then the PWM_A output is configured to generate a delta sigma output based on the settings in the register below. If This bit is set to 0, then the PWM_A output is set low.
1	R/W	0	PWM_B_EN: If This bit is set to 1, then the PWM_B output is configured to generate a PWM output based on the register above. If This bit is 0, then the PWM_B output is controlled by DS_B_EN above.
0	R/W	0	PWM_A_EN: If This bit is set to 1, then the PWM_A output is configured to generate a PWM output based on the register above. If This bit is 0, then the PWM_A output is controlled by DS_A_EN above.

PWM_DELTA_SIGMA_AB 0x2157

Bit(s)	R/W	Default	Description
31-15	R/W	0	DS_B_VAL: This value represents the delta sigma setting for channel B (PWM_B)
15-0	R/W	0	DS_A_VAL: This value represents the delta sigma setting for channel A (PWM_A)

PWM_PWM_C 0x2194

PWM_PWM_D 0x2195

PWM_MISC_REG_CD 0x2196

PWM_DELTA_SIGMA_CD 0x2197

PWM_PWM_E 0x21b0

PWM_PWM_F 0x21b1

PWM_MISC_REG_EF 0x21b2

PWM_DELTA_SIGMA_EF 0x21b3

For PWM modules in AO domain, the each register's final address = 0xc8100400 + offset*4

AO_PWM_PWM_A 0x54

AO_PWM_PWM_B 0x55

AO_PWM_MISC_REG_AB 0x56

AO_PWM_DELTA_SIGMA_AB 0x57

44. ISO7816

44.1 Overview

S905 adopts ISO7816 interface for smart card.

44.2 Register Definition

Each register's final address = 0xc1100000 + offset*4.

SC_REG0 0x2110

Bit(s)	R/W	Default	Description
31	W	0	**START_ATR**: If This bit is set to 1, then the "answer to reset" logic that consists of a counter with two thresholds. The counter counts 1us, 10uS, 100uS, 1mS or CLK pulses. This bit is usually set at the same time CLK_EN or RST_LEVEL are set since smart cards either use clocks or RESET to govern the answer to reset process. See the diagram below. This is a write only bit.
30	R	0	**DETECT_LEVEL**: Level on the detect pin
29	R	0	**IO_LEVEL**: Level on the I/O pin
28	R	0	unused
27	W	0	**START_ATR**: If This bit is set to 1, then the "answer to reset" logic that consists of a counter with two thresholds. The counter counts 1us, 10uS, 100uS, 1mS or CLK pulses. This bit is usually set at the same time CLK_EN or RST_LEVEL are set since smart cards either use clocks or RESET to govern the answer to reset process. See the diagram below.
26	R/W	0	**RST_LEVEL**: This bit sets the level on the RESET pin. This bit can be set at the same time the START_ATR Bit is set to begin the "answer to reset" for a smartcard that uses reset.
25	R/W	0	**CLK_OEN**: This bit controls the output enable of the CLK pad. If This bit is set to 1, then the CLK pad is set to an input. This allows the answer to reset logic to monitor the external clock (count external clocks).
24	R/W	0	**CLK_EN**: If This bit is set to 1, then the CLK output from the module is enabled. If This bit is set to 0, then the CLK output is disabled (and set low). This bit can be set at the same time the START_ATR Bit is set to begin the "answer to reset" for a smartcard that uses a clock.
23-20	R/W	0	**RECV_FIFO_THRESHOLD**: This value controls the number of bytes in the receive FIFO before an interrupt (or status bit) is generated. The receive FIFO is 8 bytes deep. If this value is set to say 6, then an interrupt will be generated (or a status bit set) when 6 bytes have been received.
19	R/W	0	**ENABLE**: If This bit is 0, then all state machines are set to idle. If This bit is set to 1, then smartcard module is enabled. By default, when ENABLE is 1, the receive logic is enabled and ready to receive data.
18-16	R/W	5	**FIRST_ETU_OFFSET**: The ETU generator is reset upon seeing the falling edge of the start pulse. The time between the start pulse falling edge to the first ½ ETU mark is shifted a little due to internal logic detecting the starting edge. This shift (delay) is approximately 185nS. For ETU values that are say 104uS, this 185nS is negligible. For ETU values that are down near 1uS, the 185nS is a problem. This value can be used to steal back time and re-center the first ½ ETU mark in the correct position for ETU values around 1uS. This value probably never needs to be changed.
15-0	R/W	2813	**ETU Divider**. Smart Card characters are defined by a width called an ETU (Elementary Time Unit). An internal ETU generator is used to define the width of Each Bit in a character frame. The value in this register is used to divide down the oscillator input (27Mhz) to generate an ETU. For example, the oscillator input is 47Mhz, and the ETU is (1/9600) seconds (104.2uS), then this value should be programmed to 13436. 104.2uS * 27Mhz = 2813 Since the counter is an N-1 counter, set the value to 2812.

SC_ANSWER_TO_RESET 0x2111

Bit(s)	R/W	Default	Description
31-30	R	0	Unused

Bit(s)	R/W	Default	Description
29-28	R/W	0	**ETU_CLK_SEL**: This is a new feature in the smartcard starting with the M6TVlite chip. In the past, the ETU generator was driven from the XTAL pin of the SOC. Although this clock is typically higher than the smartcard clock, the ETU generator will walk a little relative to the smartcard clock. In M6TVlite and future chips, the ETU generator can take a clock from the smartcard clock (input from the pad or output to the pad). 00: SOC Crystal 01: smartcard clock input from the Pad 10: smartcard clock generated internally and sent to the smartcard pad 11: no clock. The advantage of using the smartcard clock (for example selection 10) is the ETU will track the smartcard clock and the ETU divider value should match the F value of the smartcard (e.g. F = 372).
27	R/W	0	**ATR_HOLDOFF_EN**: If This bit is set to 1, then the Answer to Reset logic will disable the receive logic until the answer to reset counter reaches ATR_HOLDOFF_TCNT. If This bit is set to 0, then the answer to reset logic doesn't effect the receive logic.
26-24	R/W	0	**ATR_CLK_MUX**: The answer to reset counter can count time or system clocks. 000: count 1uS ticks 001: count 10uS ticks 010: count 10uS ticks 011: count 10uS ticks 100: count smart card clocks (generated from inside the chip). 101:: count smart card clocks (from outside the chip).
23-16	R/W	80	**ATR_HOLDOFF_TCNT**: Answer to reset hold count. Typically 400 smartcard clocks but could also be a count of time (see the input mux to the answer to reset counter). This value is used to disable the receive logic until the answer to reset counter reaches the ATR_HOLDOFF_TCNT. During "Answer to Reset" the receive logic should ignore the first 400 clocks of the smartcard output.
15-0	R/W	8000	**ATR_FINAL_TCNT**: Answer to reset final count. Typically 40000 smartcard clocks but could also be a count of time (see the input mux to the answer to reset counter). If the answer to reset counter reaches this value and we haven't seen a start pulse, then an ATR_EXPIRED interrupt will be generated. If a start pulse has been seen by the receiver logic, then the answer to reset logic shuts itself off.

When the answer to reset logic is started by writing START_ATR, it will continue to count until:
it reaches the ATR_FINAL_TCNT
The receive logic receives one or more bytes.

If the counter reaches ATR_FINAL_TCNT (no byte received), then an ATR_EXPIRED interrupt will be generated. The ATR_EXPIRED status bit will be set in case the software wants to use polling instead of interrupts.

If the receiver receives a byte before the counter reaches ATR_FINAL_TCNT, then the counter will be set to 0, and the ATR_ENABLED status bit will be set to 0. That is, a received byte prevents the generation of the ATR_EXPIRED interrupt (and status bit).

Therefore, the software can simply start the answer to reset logic and wait for ATR_ENABLED to drop low. If ATR_ENABLED is low and ATR_EXPIRED is high, then no byte was received. If ATR_ENABLED is low and ATR_EXPIRED is low, then a byte must have been received.

SC_REG2 0x2112

Bit(s)	R/W	Default	Description
31-29	R/W	0	**CLK_SEL**: These Bits control the clock selection: See clock trees document
28-26	R	0	**RECV_RETRY_CNT**: If the card is sending data and we detect an error we can request a retry. This counts the number of retries we detected (max 7)
25-23	R/W	0	**IO_FILTER_SEL**: The I/O input signal has a small filter that allows the hardware to filter out noise on slow rise time signals. 0 = no filter. Otherwise, a filter is applied to the input using the filter window = 200nS * (n-1). This filter can be used to filter out problems due to slow rise/fall times.
22-20	R/W	0	**DET_FILTER_SEL**: The DETECT input signal has a small filter that allows the hardware to filter out noise on slow rise time signals. 0 = no filter. Otherwise, a filter is applied to the input using the filter window = 200nS * (n-1). This filter can be used to filter out problems due to slow rise/fall times.

Bit(s)	R/W	Default	Description
19-12	R/W	0	**CLK_TCNT**: The frequency on the CLK pin is controlled by these Bits. These Bits are used to divide down the system clock to generate a clock. The divider divides the system clock by (N + 1).
11	R/W	0	**PULSE_IRQ**: Set This bit to 1 if you want the smartcard module to generate a pulse interrupt to the CPUs. In previous smartcard designs, the smartcard module would generate a level interrupt. The interrupt routine would need to clear the interrupt in the smartcard instead of just in the ISA module.
10	R/W	0	**RECV_NO_PARITY**: Ignore parity. This bit can be used to tell the receiver module to ignore the parity of the received character. This is useful during debug.
9	R/W	0	**RECV_PARITY**: 1 = Invert Parity during receiving
8	R/W	0	**RECV_LSBMSB**: 1 = Swap MSBits / LsBits during receiving
7	R/W	0	**RECV_INVERT**: 1 = invert the data Bits (excluding the parity) during receiving
6	R/W	0	**XMIT_REPEAT_DIS**: Set This bit to 1 to disable character repeats when an error is detected.
5-3	R/W	0	**XMIT_RETRIES**: Number of attempts to make sending a character. In the event the CARD responds with an Error, the smart card module will attempt to re-send the character "N" times. If the value in this register is 1, then the transmitter will only send the character once. If there is an error returned by the CARD, then we will not try again. The value in these Bits should be greater than or equal to 1.
2	R/W	0	**XMIT_PARITY**: 1 = Invert Parity
1	R/W	0	**XMIT_LSBMSB**: 1 = Swap MSBits / LSBits
0	R/W	0	**XMIT_INVERT**: 1 = invert the data Bits (excluding the parity)

SC_STATUS_REG 0x2113

Bit(s)	R/W	Default	Description
31	R	0	True if the Answer to Reset logic is counting and waiting for a byte to be received from the smart card.
30	R	0	True if the transmitter module is enabled. This will be true if there are bytes in the transmit FIFO
29	R	0	True if the receiver module is enabled (not transmitting)
28	R	0	True if the receiver module is in the process of receiving a byte from the smart card
27	R	0	True if the transmit FIFO is FULL (contains 8 bytes)
26	R	0	True if the transmit FIFO is empty
25-22	R	0	Number of bytes in the Transmit FIFO
21	R	0	True if the receive FIFO is FULL (contains 8 bytes)
20	R	0	True if the receive FIFO is empty
19-16	R	0	Number of bytes in the Receive FIFO
15-10	R	0	unused
9	R	0	True if Card Detect Interrupt
8	R	0	True if Answer to Reset expired. This will occur if START_ATR is issued and no bytes are received from the smart card in the programmed time frame.
7	R	0	True if there was a transmission error. That is, the card responded with an Error when we transferred a byte to the smart card.
6	R	0	True if there was a receive error (parity error)
5	R	0	True if the CPU tried to write a byte to the transmit FIFO while the receiver was still receiving data. Transmitting and receiving data are mutually exclusive (guaranteed by hardware / software)
4	R	0	True if the receiver tried to write to a full receiver FIFO
3	R	0	True if the Block Wait Time (BWT) expired
2	R	0	True if the Character Wait Time (CWT) expired
1	R	0	True if the last byte in the transmit FIFO was transferred to the smart card
0	R	0	True if the number of bytes in the receive FIFO is greater than or equal to **RECV_FIFO_THRESHOLD**.

SC_INTERRUPT_REG 0x2114

The interrupt register has two parts. The bottom 11 Bits contain the interrupt status of those interrupts that have a corresponding mask bit set to 1. If you write the bottom 11 Bits with a 1, then the corresponding interrupt will be cleared. The upper 11 Bits are the mask enables for the interrupts. The status of disabled interrupts can still be seen in the status register.

For example: To generate an interrupt if the Answer to Reset expires, simply Set bit 24 below. If answer to reset expires, then bit 8 will be set below and an interrupt will be generated. To clear the interrupt simply wriTE bit 8 with a 1. Note: You can also see the status of the interrupts in the STATUS register.

Bit(s)	R/W	Default	Description
31-26	R	0	unused
25	R/W	0	MASK for Bit[9] below. Set to 1 to enable this interrupt.
24	R/W	0	MASK for Bit[8] below. Set to 1 to enable this interrupt.
23	R/W	0	MASK for Bit[7] below. Set to 1 to enable this interrupt.
22	R/W	0	MASK for Bit[6] below. Set to 1 to enable this interrupt.
21	R/W	0	MASK for Bit[5] below. Set to 1 to enable this interrupt.
20	R/W	0	MASK for Bit[4] below. Set to 1 to enable this interrupt.
19	R/W	0	MASK for Bit[3] below. Set to 1 to enable this interrupt.
18	R/W	0	MASK for Bit[2] below. Set to 1 to enable this interrupt.
17	R/W	0	MASK for Bit[1] below. Set to 1 to enable this interrupt.
16	R/W	0	MASK for Bit[0] below. Set to 1 to enable this interrupt.
15-10	R	0	unused
9	R/W	0	True if Card Detect Interrupt.
8	R/W	0	True if Answer to Reset expired and the Mask bit above is set. This will occur if START_ATR is issued and no bytes are received from the smart card in the programmed time frame. *Writing This bit will clear this interrupt.*
7	R/W	0	True if there was a transmission error and the Mask bit above is set. That is, the card responded with an Error when we transferred a byte to the smart card. *Writing This bit will clear this interrupt.*
6	R/W	0	True if there was a receive error (parity error) and the Mask bit above is set. *Writing This bit will clear this interrupt.*
5	R/W	0	True if the CPU tried to write a byte to the transmit FIFO while the receiver was still receiving data. Transmitting and receiving data are mutually exclusive (guaranteed by hardware / software) and the Mask bit above is set. *Writing This bit will clear this interrupt.*
4	R/W	0	True if the receiver tried to write to a full receiver FIFO and the Mask bit above is set. *Writing This bit will clear this interrupt.*
3	R/W	0	True if the Block Wait Time (BWT) expired and the Mask bit above is set. *Writing This bit will clear this interrupt.*
2	R/W	0	True if the Character Wait Time (CWT) expired and the Mask bit above is set. *Writing This bit will clear this interrupt.*
1	R/W	0	True if the last byte in the transmit FIFO was transferred to the smart card and the Mask bit above is set. *Writing This bit will clear this interrupt.*
0	R/W	0	True if the number of bytes in the receive FIFO is greater than or equal to **RECV_FIFO_THRESHOLD** and the Mask bit above is set. *Writing This bit will clear this interrupt.*

SC_REG5 0x2115

Bit(s)	R/W	Default	Description
31-20	R	0	ETU_MSR_CNT: This value represents the ETU measured value. The value has a resolution of 1uS
19	R/W	0	RECV_ETU_ERROR_CNT: According to the specification, if there is a parity error on receive the smartcard module will generate an error ether 1 or two ETU's wide. In previous designs the ERROR pulse was 1 ETU wide. If This bit is set to 1, then an ERROR pulse that is 2 ETU's wide will be generated.
18	R/W	0	ETU_MSR_EN: If This bit is set, then the hardware will measure the time between the first falling edge of the IO pin to the next rising edge of the I/O pin. This can be used to measure the ETU of a card in the event that the ETU is not known.
17	R/W	0	CWT_DETECT_EN: Set This bit to detect character wait time violations. The CWT is defined as the maximum time between the leading edge of two consecutive characters in the same block. The CWT may be used by the receiving node to detect the end of a block. That is, if the CWT is expired, then the card is not sending any more data.
16	R/W	0	BTW_DETECT_EN: Set This bit to detect block wait time violations. The Block wait time is the time between the leading edges of two characters in opposite directions. The BWT is used to detect an unresponsive card.
15-0	R/W	999	Block Wait Time Base time generator. This counter counts 1mS ticks. These ticks are counted by the Block Wait Time logic to identify block wait time violations. The counter corresponds to (N+1) * 0.001 Seconds.

SC_REG6 0x2116

Bit(s)	R/W	Default	Description
31-24	R	0	Unused

Bit(s)	R/W	Default	Description
23-20	R/W	4	BWI: The BWI is used to define the Block Wait Time (BWT). The BWT is defined as + 11 work ETU Since the time frame for the Block Wait Time is long (seconds) relative to the speed of the system clock, the Block Wait Time is re-defined without the 11 work ETU's to reduce logic: The BWT_TIME_BASE is established in Control Register 5. For example, if the BWT_TIME_BASE is set to pulse every 146nS, and BWI is set to 10 (decimal), then the Block Wait Time will expire at 146nS * 1024 = 149.5uS. Note: The block Wait time can be used to determine an unresponsive card. Status bit 18 of Control Register 4 indicates that the Block Wait Time has expired. An interrupt can also be generated in the event that the Block Wait Time expires. Typically the Block Wait Time logic is reset at the beginning of a transmitted character.
19-12	R/W	20	BGT: Block Guard Time. The block guard time is defined as the minimum time between the leading edges of two consecutive characters sent in opposite directions. This value defines the BGT in an (N+2) relationship. For example, a value of 20 corresponds to a BGT of 22 work ETU.
11-8	R/W	13	CWI value. The CWT is defined as the wait time between characters. The CWI value defines the CTW time as (2^{CWI} + 11) work ETU
7-0	R/W	0	N parameter: the N parameter is used to provide extra guard time between characters. xmit_char_time = (N_param == 8'd255) ? 'd10 : ('d11 + N_param);

SC FIFO 0x2117

Bit(s)	R/W	Default	Description
31-8	R	0	Unused
7-0	R/W	0	Writing this register writes the Transmit FIFO Reading this register reads the Receive FIFO

45. SAR ADC

45.1 Overview

This SAR ADC is a general purpose ADC for measuring analog signals. The module can make RAW ADC measurements or average a number of measurements to introduce filtering. The SAR ADC is a single block so an analog mux is placed in front of the mux to allow multiple different measurements to be made sequentially. Timing of the samples, and delays between muxing are all programmable as is the averaging to be applied to the SAR ADC.

45.2 Register Description

Each register final address = 0xC1100000 + offset * 4

SAR_ADC_REG0: Control Register #0 0x21a0

Bit(s)	R/W	Default	Description
31	R	0	PANEL DETECT level.
30	R/W	0	DELTA_BUSY: If This bit is 1, then it indicates the delta processing engine is busy
29	R/W	0	AVG_BUSY: If This bit is 1, then it indicates the averaging engine is busy
28	R/W	0	SAMPLE_BUSY: If This bit is 1, then it indicates the sampling engine is busy
27	R/W	0	FIFO_FULL:
26	R/W	0	FIFO_EMPTY:

Bit(s)	R/W	Default	Description
25-21	R/W	4	FIFO_COUNT: Current count of samples in the acquisition FIFO
20-19	R/W	0	ADC_BIAS_CTRL
18-16	R/W	0	CURR_CHAN_ID: These Bits represent the current channel (0..7) that is being sampled.
15	R/W	0	ADC_TEMP_SEN_SEL
14	R/W	0	SAMPLING_STOP: This bit can be used to cleanly stop the sampling process in the event that continuous sampling is enabled. To stop sampling, simply set This bit and wait for all processing modules to no longer indicate that they are busy.
13-12	R/W	0	CHAN_DELTA_EN: There are two Bits corresponding to Channels 0 and 1. Channel 0 and channel 1 can be individually enabled to take advantage of the delta processing module.
11	R/W	0	Unused
10	R/W	0	DETECT_IRQ_POL: This bit sets the polarity of the detect signal. The detect signal is used during X/Y panel applications to detect if the panel is touched
9	R/W	0	DETECT_IRQ_EN: If This bit is set to 1, then an interrupt will be generated if the DETECT signal is low/high. The polarity is set in the bit above.
8-4	R/W	0	FIFO_CNT_IRQ: When the FIFO contains N samples, then generate an interrupt (if bit 3 is set below).
3	R/W	0	FIFO_IRQ_EN: Set This bit to 1 to enable an IRQ when the acquisition FIFO reaches a certain level.
2	W	0	SAMPLE_START: This bit should be written to 1 to start sampling.
1	R/W	0	CONTINUOUS_EN: If This bit is set to 1, then the channel list will be continually processed
0	R/W	0	SAMPLING_ENABLE: Setting This bit to '1' enables the touch panel controller sampling engine, averaging module, XY processing engine and the FIFO.

SAR_ADC_CHAN_LIST:Channel List 0x21a1

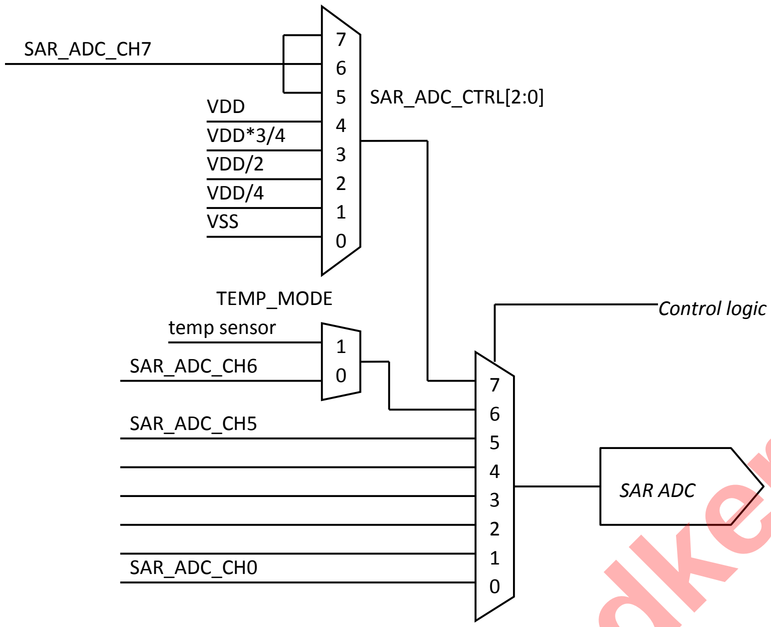
Bit(s)	R/W	Default	Description
31-27	R/W	0	unused
26-24	R/W	2	Length of the list of channels to process. If this value is 2, then only channels in Bits [8:0] below are processed.
23-21	R/W	7	8th channel
20-18	R/W	6	7th channel
17-15	R/W	5	6th channel
14-12	R/W	4	5th channel
11-9	R/W	3	4th channel
8-6	R/W	2	3rd channel
5-3	R/W	1	2nd channel
2-0	R/W	0	First channel in the list of channels to process

SAR_ADC_AVG_CNTL:Sampling/Averaging Modes 0x21a2

Each channel listed in the CHANNEL_LIST is given independent control of the number of samples to acquire and averaging mode

Bit(s)	R/W	Default	Description
31-30	R/W	0	Channel 7: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
29-28	R/W	0	Channel 6: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
27-26	R/W	0	Channel 5: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
25-24	R/W	0	Channel 4: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
23-22	R/W	0	Channel 3: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
21-20	R/W	0	Channel 2: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
19-18	R/W	0	Channel 1: Averaging mode: 0 = no averaging, 1 = simple averaging, 2 = median averaging.
17-16	R/W	0	Channel 0: Averaging mode: 0 = no averaging. 1 = simple averaging of the number of samples acquired (1,2,4 or 8). 2 = median averaging. NOTE: If these Bits are set to 2, then you must set the number of samples to acquire below to 8.
15-13	R/W	0	Channel 7: Number of samples to acquire 2^N:
13-12	R/W	0	Channel 6: Number of samples to acquire 2^N:
11-10	R/W	0	Channel 5: Number of samples to acquire 2^N:
9-8	R/W	0	Channel 4: Number of samples to acquire 2^N:
7-6	R/W	0	Channel 3: Number of samples to acquire 2^N:
5-4	R/W	0	Channel 2: Number of samples to acquire 2^N:
3-2	R/W	0	Channel 1: Number of samples to acquire 2^N:
1-0	R/W	0	Channel 0: Number of samples to acquire 2^N: 0 = 1, 1 = 2, 2 = 4, 4 = 8.

SAR_ADC_REG3: Control Register #3 0x21a3



Bit(s)	R/W	Default	Description
31	R/W	0	CNTL_USE_SC_DLY: hold time delay was added to the start conversion clock. Unfortunately, it appears that the analog ADC design requires that we use the inverted clock so This bit is meaningless.
30	R/W	0	SAR ADC_CLK_EN: 1 = enable the SAR ADC clock
29	R/W	0	reserved
28	R/W	0	reserved
27	R/W	0	SARADC_CTRL[4]: is used to control the internal ring counter. 1 = enable the continuous ring counter. 0 = disable
26	R/W	0	SARADC_CTRL[3]: used to select the internal sampling clock phase
25~23	R/W	0	SARADC_CTRL[2:0]: 000 ssa 001 vdda/4 010 vdda/2 011 vdda*3/4 100 vdda 101, 110, 111 unused
22	R/W	0	DETECT_EN: This bit controls the analog switch that connects a 50k resistor to the X+ signal. Setting This bit to 1 closes the analog switch
21	R/W	0	ADC_EN: Set This bit to 1 to enable the ADC
20-18	R/W	2	PANEL_DETECT_COUNT: Increasing this value increases the filtering on the panel detect signal using the timebase settings in Bits [17:16] below.
17-16	R/W	0	PANEL_DETECT_FILTER_TB: 0 = count 1uS ticks, 1 = count 10uS ticks, 2 = count 100uS ticks. 3 = count 1mS ticks
15-10	R/W	20	ADC_CLK_DIV: The ADC clock is derived by dividing the 27Mhz crystal by N+1. This value divides the 27Mhz clock to generate an ADC clock. A value of 20 for example divides the 27Mhz clock by 21 to generate an equivalent 1.28Mhz clock.
9-8	R/W	1	BLOCK_DLY_SEL: 0 = count 1uS ticks, 1 = count 10uS ticks, 2 = count 100uS ticks. 3 = count 1mS ticks
7-0	R/W	10	BLOCK_DLY: After all channels in the CHANNEL_LIST have been processed, the sampling engine will delay for an amount of time before re-processing the CHANNEL_LIST again. Combined with Bits [9:8] above, this value is used to generate a delay between processing blocks of channels.

SAR_ADC_DELAY:INPUT / SAMPLING DELAY 0x21a4

As the CHANNEL_LIST is process, the input switches are set according to the requirements of the channel. After setting the switches there is a programmable delay before sampling begins. Additionally, each channel specifies the number of samples for that particular channel. The sampling rate is programmed below.

Bit(s)	R/W	Default	Description
15-10	R	0	unused

Bit(s)	R/W	Default	Description
25-24	R/W	0	INPUT_DLY_SEL: 0 = 111nS ticks, 1 = count 1uS ticks, 2 = count 10uS ticks, 3 = count 100uS ticks
16-23	R/W	3	INPUT_DLY_CNY: For channels that acquire 2,4 or 8 samples, the delay between two samples is controlled by this count (N+1) combined with the delay selection in the two Bits above.
15-10	R	0	unused
9-8	R/W	0	SAMPLE_DLY_SEL: 0 = count 1uS ticks, 1 = count 10uS ticks, 2 = count 100uS ticks. 3 = count 1mS ticks
7-0	R/W	9	SAMPLE_DLY_CNY: For channels that acquire 2,4 or 8 samples, the delay between two samples is controlled by this count (N+1) combined with the delay selection in the two Bits above.

SAR_ADC_LAST_RD: Last Sample 0x21a5

For channel 0 and channel 1, (the special X/Y channels) the last sample pushed into the FIFO for each channel is saved in a register. This allows the software to see the last sample for channel 0 and channel 1 even when the FIFO overflows. For example, if we are sampling quickly and there is a gesture on the screen, we can use the contents of the FIFO to see the direction of the gesture and use the last sample values to see where the pen finally came to rest.

Bit(s)	R/W	Default	Description
31-24	R	0	unused
23-16	R	0	LAST_CHANNEL1
15-10	R	0	unused
9-0	R	0	LAST_CHANNEL0

SAR_ADC_FIFO_RD: Control Register #6 (FIFO RD) 0x21a6

Bit(s)	R/W	Default	Description
31-16	R	0	Unused
15	R	0	Unused
14-12	R	0	Channel ID. This value identifies the channel associated with the data in Bits [9:0] below
11-10	R	0	Unused
9-0	R	0	Sample value: 9-bit raw or averaged ADC sample written to the FIFO.

SAR_ADC_AUX_SW:Channel 2~7 ADC MUX, Switch Controls 0x21a7

Channels 2 ~ 7 can program the ADC input mux to any selection between 0 and 7. This register allows the software to associate a mux selection with a particular channel. In addition to the ADC mux, there are a number of switches that can be set in any particular state. Channels 2 ~ 7 share a common switch setting. Channels 0 and 1 on the other hand have programmable switch settings (see other registers below).

Bit(s)	R/W	Default	Description
31-26	R	0	unused
25-23	R/W	7	Channel 7 ADC_MUX setting when channel 7 is being measured.
22-20	R/W	7	Channel 6 ADC_MUX setting when channel 6 is being measured.
19-17	R/W	7	Channel 5 ADC_MUX setting when channel 5 is being measured.
16-14	R/W	6	Channel 4 ADC_MUX setting when channel 4 is being measured.
13-11	R/W	0	Channel 3 ADC_MUX setting when channel 3 is being measured.
10-8	R/W	1	Channel 2 ADC_MUX setting when channel 2 is being measured.
7	R	0	unused
6	R/W	0	VREF_P_MUX setting when channel 2,3..7 is being measured
5	R/W	0	VREF_N_MUX setting when channel 2,3..7 is being measured
4	R/W	0	MODE_SEL setting when channel 2,3..7 is being measured
3	R/W	1	YP_DRIVE_SW setting when channel 2,3..7 is being measured
2	R/W	1	XP_DRIVE_SW setting when channel 2,3..7 is being measured
1	R/W	0	YM_DRIVE_SW setting when channel 2,3..7 is being measured
0	R/W	0	YM_DRIVE_SW setting when channel 2,3..7 is being measured

SAR_ADC_CHAN_10_SW:Channel 0, 1 ADC MUX, Switch Controls 0x21a8

Channels 0 and 1 have independent programmable switch settings when either/both of these channels are being measured.

Bit(s)	R/W	Default	Description
31-26	R	0	unused
25-23	R/W	2	Channel 1 ADC MUX setting
22	R/W	0	Channel 1 VREF_P_MUX

Bit(s)	R/W	Default	Description
21	R/W	0	Channel 1 VREF_N_MUX
20	R/W	0	Channel 1 MODE_SEL
19	R/W	1	Channel 1 YP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
18	R/W	1	Channel 1 XP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
17	R/W	0	Channel 1 YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
16	R/W	0	Channel 1 YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
15-10	R		unused
9-7	R/W	3	Channel 0 ADC MUX setting
6	R/W	0	Channel 0 VREF_P_MUX
5	R/W	0	Channel 0 VREF_N_MUX
4	R/W	0	Channel 0 MODE_SEL
3	R/W	1	Channel 0 YP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
2	R/W	1	Channel 0 XP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
1	R/W	0	Channel 0 YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
0	R/W	0	Channel 0 YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND

SAR_ADC_DETECT_IDLE_SW:DETECT / IDLE Mode switches 0x21a9

IDLE MODE:

When nothing is being measured, the switches should be put into a safe state. This safe state is accomplished using Bits [9:0] below.

DETECT MODE:

When bit [26] is set, the input muxes / switches are configured according to the Bits below. Typically the software configures the switches below to correspond to the detect touch mode. That is, Y- internal MOSFET is closed so that the Y plane of the touch screen is connected to Ground. Additionally, the DETECT_EN bit(different register) set to 1 so that the 50k resistor to VDD is connected to X+. In this configuration, the detect comparator connected to the 50k resistor will be weakly pulled up to VDD through the 50k resistor. If the user touches the screen, the X and Y planes of the touch screen will contact causing the X+ signal to be pulled to ground.

Bit(s)	R/W	Default	Description
31-27	R	0	unused
26	R/W	0	DETECT_SW_EN: If This bit is set, then Bits [25:16] below are applied to the analog muxes/switches of the touch panel controller.
25-23	R/W	5	DETECT MODE ADC MUX setting
22	R/W	0	DETECT MODE VREF_P_MUX setting
21	R/W	0	DETECT MODE VREF_N_MUX setting
20	R/W	0	DETECT MODE MODE_SEL setting
19	R/W	1	DETECT MODE YP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
18	R/W	1	DETECT MODE XP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating

Bit(s)	R/W	Default	Description
17	R/W	0	DETECT MODE YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
16	R/W	0	DETECT MODE YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
15-10	R		Unused
9-7	R/W	5	IDLE MODE ADC MUX setting
6	R/W	0	IDLE MODE VREF_P_MUX setting
5	R/W	0	IDLE MODE VREF_N_MUX setting
4	R/W	0	IDLE MODE MODE_SEL setting
3	R/W	1	IDLE MODE YP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
2	R/W	1	IDLE MODE XP_DRIVE_SW setting: 0: TADC_CH6N = 3.3v 1: TADC_CH6N = floating
1	R/W	0	IDLE MODE YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND
0	R/W	0	IDLE MODE YM_DRIVE_SW setting: 0: TADC_CH4N = floating 1: TADC_CH4N = GND

SAR_ADC_DELTA_10:Delta Mode Deltas 0x21aa

Bit(s)	R/W	Default	Description
31-28	R	0	unused
27	R/W		TEMP_SEL
26	R/W		TS_REVE[1]
25-16	R/W	0	Channel 1 delta value when delta processing for channel 1 is enabled.
15	R/W		TS_REVE[0]
14-11	R/W		TS_C[3:0]
10	R/W	0	TS_VBG_EN
9-0	R/W	0	Channel 0 delta value when delta processing for channel 0 is enabled.

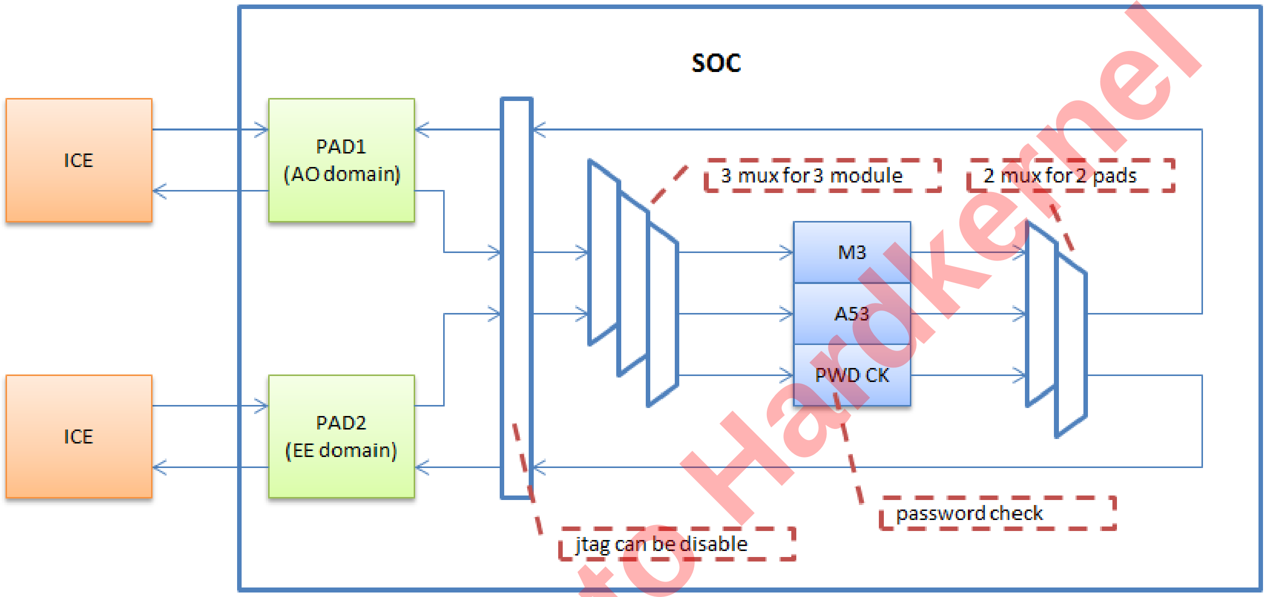
Section VIII System Interface

46. JTAG

46.1 Overview

JTAG is an interface for internal test. The structure of S905 JTAG module is shown in the following diagram:

Fig VIII.47.1 Diagram of JTAG



47. Temp Sensor

47.1 Overview

The temperature sensor uses TSMC 28nm CMOS mix signal process and can provide a PTAT voltage which contains the temperature information of the chip. This block together with the followed SAR ADC can give the chip temperature. Figure shows block diagram of the temperature sensor.

FigVIII.48.1 Temperature Sensor Diagram

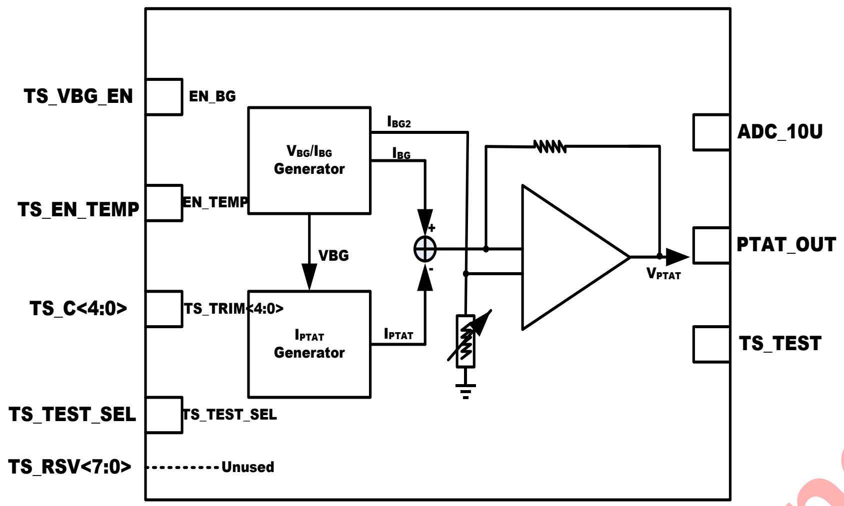
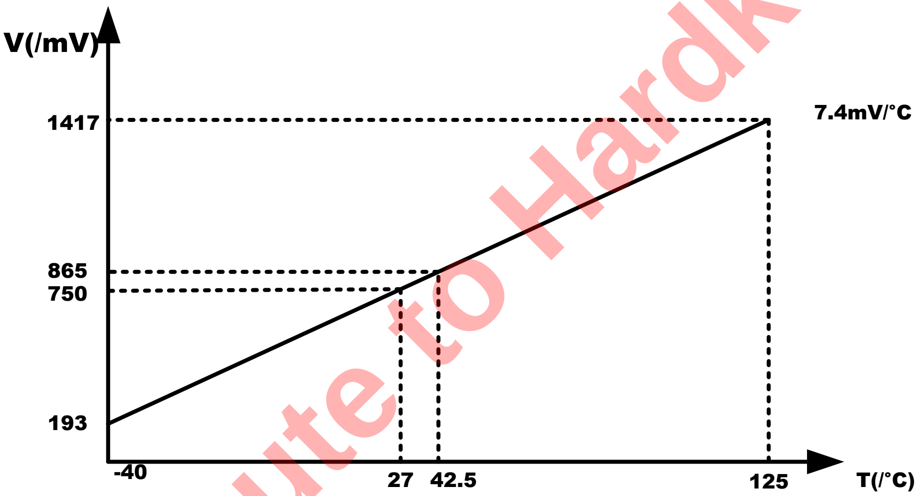


Fig VIII.48.2 Temperature sensor output

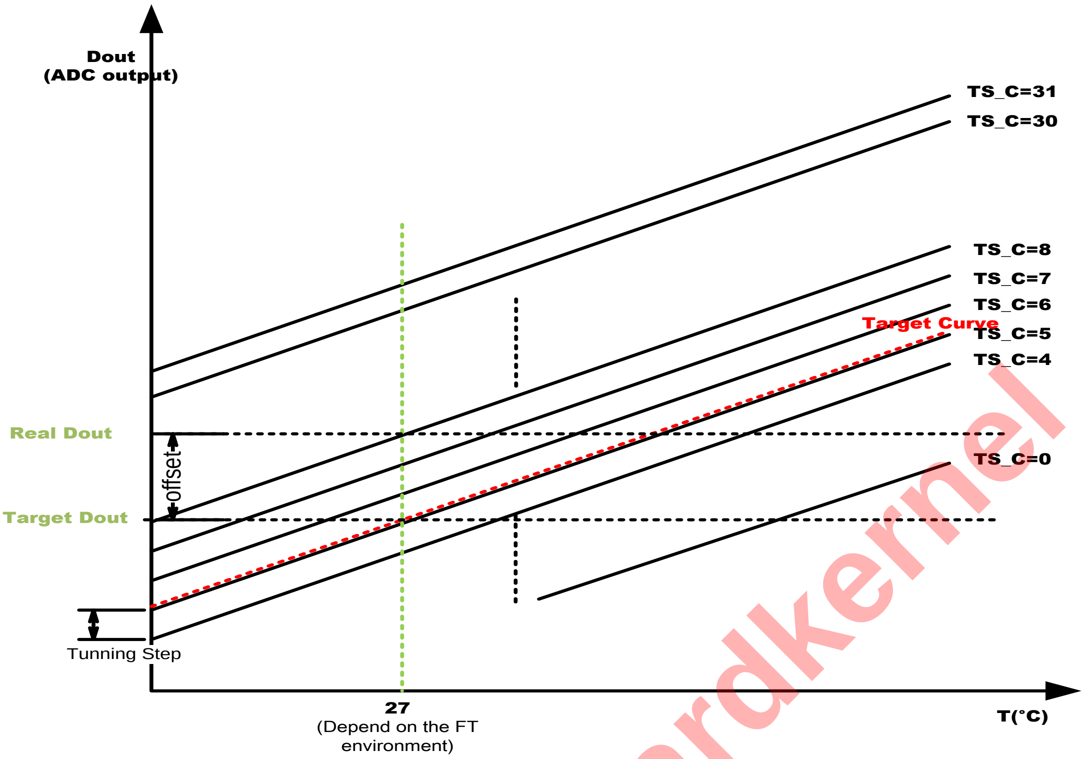


47.2 Trimming

Trimming is suggested before using this block. Fig.2 denotes the ideal output voltage of this block which also gives the direction of trimming. We use 16 Bits e-fuse resistor to trim this block, 10 Bits for the recording of the result of SARADC in FT process , 5 Bits for coarse trimming(Anti-saturation of this block) and 1 bitfor trimming fag. Two fixed points (27°,750mV) and (42.5, 865mV) are provided in Fig.2, you can select either one of them as the coarse trimming target.

Fig.3 shows the real calibration curve for temperature sensor, please note the Y coordinate is different from Fig.2, but they are the input and output of the SARADC respectively. In chip application, the temperature can be calculated when we get the real time Dout if the line is determined. While in theory we can determine a line if the slope and a real arbitrary point are given, that is to say the slope(given by designer) and the Dout at a specified temperature in Fig.3.

Fig VIII.48.3 Temperature sensor calibration curve



Below is the calibration flow:

1. Get the real Dout when set the TS_C to 16;
2. According to the offset and Tunning step the ΔTS_C can be calculated(The tunning step and target Dout are given by designer);
3. Calculate the final TS_C, TS_C_{final}=16+ΔTS_C;
4. Read the Dout when set the TS_C to the final value;
5. Store the final the TS_C and the Dout which are get in step 4 to effuse;

47.3 Register Definition

0xc810062c

Bits	R/W	Default	Description
31-30	R	reserved	-
29-22	R/W	00000000	TS_RSV<7:0>:Unused bit, can set to 0
21	R/W	1	Enable SARADC channel 6 sampling
20	R/W	0	TS_TEST_SEL: Enable the test mode
19	R/W	1	TS_EN_TEMP:Write 1 to enable temperature sensor circuit.
18-14	R/W	10000	TS_C<4:0>.Trimming temperature sensor's output voltage.0000: 550mV 1111:850mV
13	R/W	1	TS_VBG_EN. Write 1 to enable bandgap.
12-0	R/W	reserved	-