DATA SHEET

SA1638
Low voltage IF I/Q transceiver

Product specification

IC17 Data Handbook

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Philips
Semiconductors

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Low voltage IF I/Q transceiver SA1638

DESCRIPTION

The SA1638 is a combined Rx and Tx IF I/Q circuit. The receive path contains an IF amplifier, a pair of quadrature down-mixers, and a pair of baseband filters and amplifiers. A second pair of mixers in the transmit path transposes a quadrature baseband input up to the IF frequency. An external VCO signal is divided down internally and buffered to provide quadrature local oscillator signals for the mixers. A further divider chain, reference divider and phase detector are provided to avoid the need for an external IF synthesizer. Rx or Tx path or the entire circuit may be powered down by logic inputs. On-board voltage regulators are provided to allow direct connection to a battery supply.

FEATURES

- Direct supply: 3.3V to 7.5V
- Two DC regulators giving 3.0V output
- Low current consumption: 18mA for Rx or 22mA for Tx
- Input/output IF frequency from 70-400 MHz
- Internal IF PLL for synthesizing the local oscillator signal
- High performance on-board integrated receive filters with bandwidth tunable between 50-850 kHz
- Switchable alternative bandwidth setting available to allow channel bandwidth flexibility in operation
- Designed for a widely used I and Q baseband GSM interface
- Control registers power up in a default state
- Optional DC offset trim capability to <200mV
- Only a standard reference input frequency required, choice of 13, 26, 39 or 52MHz
- Fully compatible with SA1620 GSM RF front-end (see Figure 9)

APPLICATIONS

- IF circuitry for GSM 900MHz hand-held units
- IF circuitry for PCN (DCS1800) hand-held units
- Quadrature up and down mixer stage

PIN CONFIGURATION

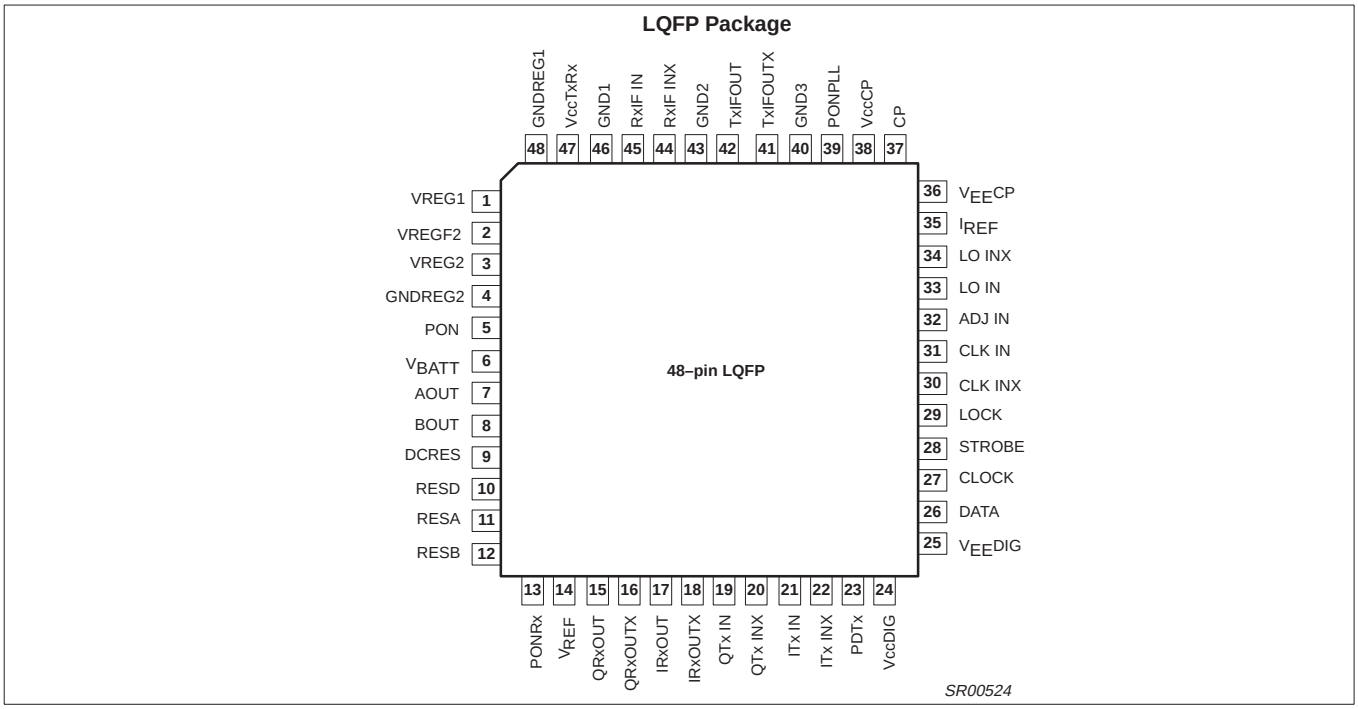


Figure 1. SA1638 Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (LQFP)	-40 to +85°C	SA1638BE	SOT313-2

BLOCK DIAGRAM

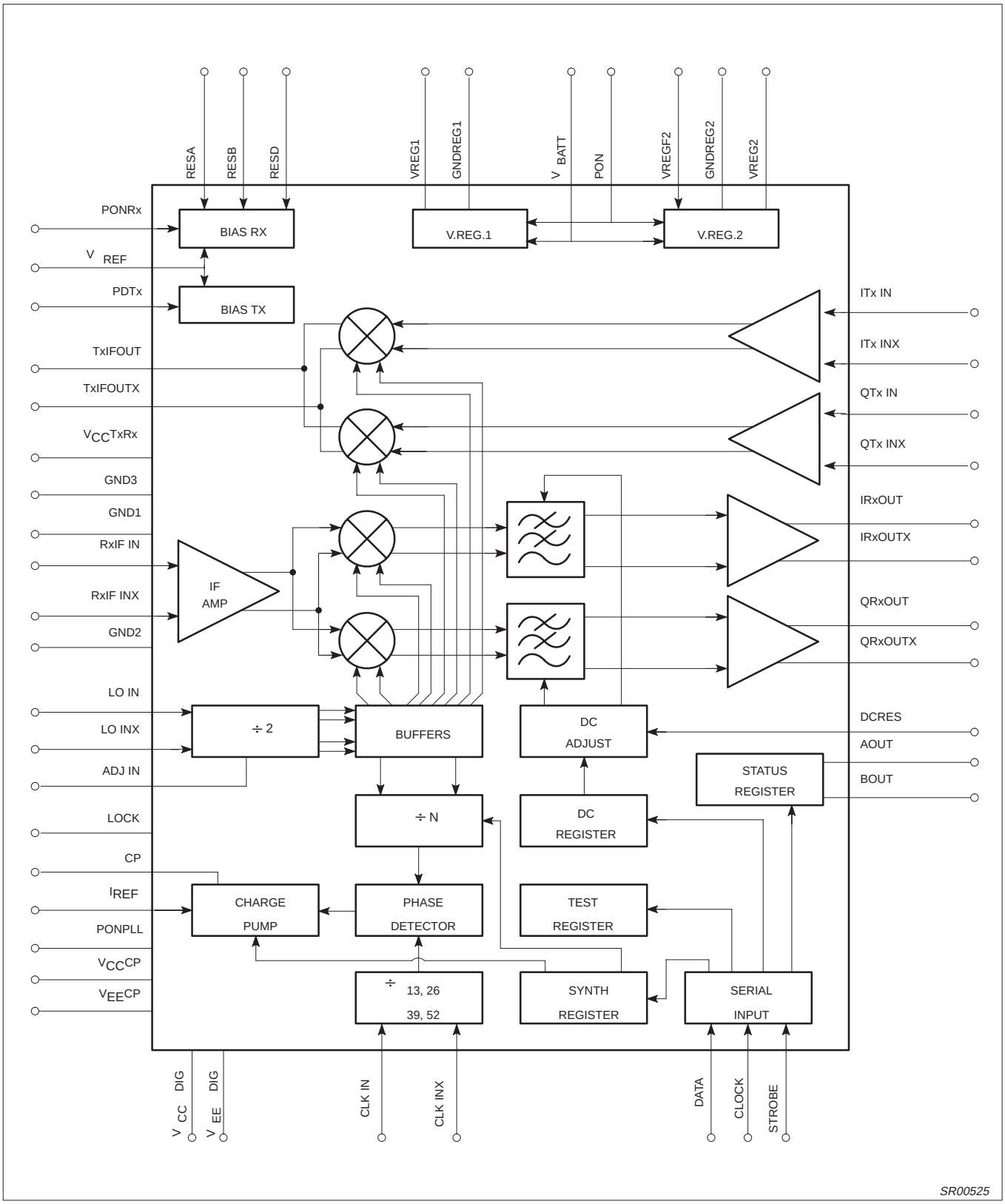


Figure 2. SA1638 Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VREG1	Output voltage of regulator 1
2	VREGF2	Feedback of regulator 2
3	VREG2	Output voltage of regulator 2
4	GNDREG2	Ground of regulator 2
5	PON	Power-on input for voltage regulators 1 and 2 (active high)
6	V_{BATT}	Input voltage for regulators 1 and 2
7	AOUT	Programmable logic output (see Figure 9)
8	BOUT	Programmable logic output (see Figure 9)
9	DCRES	Reference current setting resistor for DC offset circuit
10	RESD	Additional external current defining resistor for filters
11	RESA	Principal external current defining resistor for filters
12	RESB	Principal external current defining resistor for filters
13	PONRx	Power-on input for Rx (active high)
14	V_{REF}	Reference voltage
15	QRxOUT	Differential receive baseband output
16	QRxOUTX	Differential receive baseband output
17	IRxOUT	Differential receive baseband output
18	IRxOUTX	Differential receive baseband output
19	QTx IN	Differential transmit baseband input
20	QTx INX	Differential transmit baseband input
21	ITx IN	Differential transmit baseband input
22	ITx INX	Differential transmit baseband input
23	PDTx	Power-on for transmitter (active low)
24	V_{CC}DIG	Digital circuit supply
25	V_{EE}DIG	Digital ground
26	DATA	Serial bus data input
27	CLOCK	Serial bus clock input
28	STROBE	Serial bus strobe input
29	LOCK	Test control/synthesizer lock indicator
30	CLK INX	Differential reference divider input
31	CLK IN	Differential reference divider input
32	ADJ IN	Used for test only. Do not connect
33	LO IN	Differential LO input
34	LO INX	Differential LO input
35	I_{REF}	Reference current setting for charge pump
36	V_{EE}CP	Charge pump ground
37	CP	Charge pump output
38	V_{CC}CP	Charge pump circuit supply
39	POnPLL	Power-on input for synthesizer circuits (active high)
40	GND3	Ground (internal connection to GND1 and GND2)
41	TxIFOUTX	Differential transmit IFoutput (open collector)
42	TxIFOUT	Differential transmit IFoutput (open collector)
43	GND2	Ground (internal connection to GND1 and GND3)
44	RxIF INX	Differential receive IF input
45	RxIF IN	Differential receive IF input
46	GND1	Ground (internal connection to GND2 and GND3)
47	V_{CC}TxRx	Transmit and receive circuits supply voltage (also feedback of Regulator 1)
48	GNDREG1	Ground of regulator 1

NOTE: There are no ESD protection diodes at Pins 41 and 42. Thus, open collector outputs may have increased DC voltage or higher AC peak voltage.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}XXX$	Supply voltages: V_{CC}TxRx, V_{CC}DIG, V_{CC}CP	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXXX}+0.3)	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin LQFP: θ_{JA} = 67°C/W.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC}XXX$	Supply voltages: V_{CC}TxRx, V_{CC}DIG	2.7 to 5.5	V
V_{CC}CP	Charge pump supply voltage	2.9 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

Voltage Regulators

T_A = 25°C, P_{ON} = 3V, P_{ON}RX = 0V, PDTX = 3V, P_{ON}PLL = 0V, V_{BATT} = 3.3V, $I_{OUT}1$ = $I_{OUT}2$ = 15mA, $V_{REG}1$ connected to V_{CC}TxRx, $V_{REG}2$ connected to V_{REG}F2; V_{CC}DIG = V_{CC}CP = 3V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			Min	–3σ	Typ	+3σ	Max	
$V_{REG}1$, $V_{REG}2$	Nominal V_{OUT}		2.85	2.93	3.00	3.07	3.15	V
V_{BATT}			3.3				7.5	V
$I_{OUT}1$, $I_{OUT}2$	Maximum output current for each regulator[1]						30	mA
I_{BATT}	Supply current for both regulators	I_{LOAD} = 0mA		4.3	5	5.7	7	mA
$I_{BATT\ PD}$	Power-down supply current	P_{ON} = 0V, I_{LOAD} = 0mA		7.7	9	10.3	15	µA
$C_{REG}1^2$	$V_{REG}1$ cap load		0.1				1000	µF
$C_{REG}2^2$	$V_{REG}2$ cap load		0.1				500	µF
LINEREG	Line regulation	DC, V_{BATT} = 3.3V to 7.5V	–0.4	–0.2	0.001	0.2	0.4	%
LOADREG	Load regulation	I_{LOAD} = 15mA to 30mA	–5	–0.37	-0.17	0.03	5	%
BW	Bandwidth		100					kHz
F_{PON}	Feedthrough attenuation from P_{ON} to each regulator				≤ -40			dB
F_{REG}	Feedthrough attenuation from V_{BATT} to each regulator	f ≤ 100kHz f = 10MHz f = 100MHz f = 400MHz			≤ -61 ≤ -32 ≤ -37 ≤ -48			dB
t_{ON}	Turn ON time				10			µs

NOTES:
1. At $T_j \geq$ 150°C a thermal switch reduces the output current to avoid damage.
2. Recommended load capacitors: In every case $C_{REG}1$ = $C_{REG}2$ = 100nF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000µF with series resistance ≤5Ω. The low series resistance is very important to ensure regulator stability.
3. Standard deviations are based on the characterization results of 90 ICs.

DC ELECTRICAL CHARACTERISTICS

V_{CC}TxRx=V_{CC}DIG=V_{CC}CP=PONRx=PONPLL= +3V; V_{EE}DIG = V_{EE}CP=GND1=GND2=GND3=PDTx = 0V; T_A = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
I_{CC}	Supply current							mA
	Rx and IF synthesizer active	PONRx = PONPLL = PDTx = Hi		14.4	16	17.6	20	
	Tx and IF synthesizer active	PONRx = PDTx = Low; PONPLL = Hi		17.4	19.5	21.6	24	
	Power-down mode	PONRx = PONPLL = Low; PDTx = Hi			0.068			
V_{REF}	Reference voltage	Generated internally		1.39	1.57	1.75		V
IV_{REF}	V_{REF} I_{SINK} I_{SOURCE}				5 5			µA
I_{OUT}	DC output current	At pins TxIFOUT and TxIFOUTX	1.5	1.86	2.0	2.14	2.7	mA
Digital inputs (P_{ON})								
V_{IH}	High level input voltage range		2.0				V_{BATT}	V
V_{IL}	Low level input voltage range		0				0.8	V
Digital inputs (PDTx, P_{ON}Rx, P_{ON}PLL, P_{ON})								
V_{IH}	High level input voltage range		2.0				V_{CC}TxRx	V
V_{IL}	Low level input voltage range		0				0.8	V
Digital inputs (Clock, Data, Strobe)								
V_{IH}	High level input voltage range		2.0				V_{CC}Dig	V
V_{IL}	Low level input voltage range		0				0.8	V
Digital outputs (LOCK, AOUT, BOUT)								
V_{OH}	Output voltage HIGH	I_O = -2mA	V_{CC}DIG–0.4					V
V_{OL}	Output voltage LOW	I_O = 2mA					0.4	V

AC ELECTRICAL CHARACTERISTICS

V_{CC}TxRx=V_{CC}DIG=V_{CC}CP=PONRx=PONPLL= +3V; V_{EE}DIG = V_{EE}CP=GND1=GND2=GND3=PDTx = 0V; LO_{IN} = 100mV_{PEAK}, 800MHz; CLK_{IN} = 100mV_{PEAK}, 52MHz; serial registers programmed with default values; T_A = 25°C unless otherwise stated. Test Circuit Figure 8.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
IF Transmit Modulator								
BW	Input modulation bandwidth	200Ω source impedance		0.82	0.94	1.06		MHz
V_{COM}	Common mode range for baseband inputs	DC at pins ITxIN, ITxINx, QTxIN, QTxINx	1		1.5		2	V
V_{IN}	Peak input signal amplitude	Centered on V_{COM}			0.75			V
	Third harmonic distortion[1]	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75$V_{PEAK;}$ fin = 20kHz		-61	-57	-53	-40	dB
R_{INTx}	Input resistance	Between pins: ITxIn and ITxInX or QTxIn and QTxInX	112					kΩ
C_{INTx}	Input capacitance	At ITxIn, ITxInX, QTxIn, QTxInX					10	pF
	Output saturation limit						V_{CC}TxRx-0.3	V
I_{OUT}	RMS output current	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V_{PEAK}	0.6	0.73	0.82	0.91	1.08	mA
S_{LO}	LO suppression[1]	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V_{PEAK}; fin = 20k	+30		+43			dB
SSB	Sideband suppression[1]	| ITxIn | = | ITxInX | = | QTxIn | = | QTxInX | = 0.75V_{PEAK}; fin = 20k	+35		+50			dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
IF Transmit Modulator (continued)								
	Noise density at 600kHz	|ITxIn| = |ITxInX| = |QTxIn| = |QTxInX| = 0.75V_{PEAK}		-130	-129	-128		dBc/Hz
	Noise density at 10MHz			-133	-131	-129		
t_{ON}	Turn ON time	PdTx = LO, transmit signal to 90%			5			µs
t_{OFF}	Turn OFF time	PdTx = HI, transmit signal to 10%			5			µs
IF Receiver (R = 36kΩ between pins RESA and RESB)								
RInRx	Differential input impedance	f_{IN} = 400MHz			5 || 0.6			kΩ || pF
ROutRx	Output impedance				1			kΩ
	Output common mode voltage				V_{REF}			V
f3dB	Low pass filter -3dB bandwidth		70		83		90	kHz
	Low pass filter attenuation: 200kHz 400kHz 600kHz 6.5MHz 13.0MHz		 6.5 30	 8.9 38.1	 10.7 45 70 >80 >80	 12.5 51.9		dB
VG	Voltage gain	Differential output PD into GSM baseband relative to 1200Ω source EMF	43	49.4	51	52.7	58	dB
NF	Noise figure[8]	1200Ω source and external matching resistor and inductor		5.7	7.0	8.3		dB
	Channel matching: Gain Phase	f_{IN} = 400.005MHz	 -1.5		 -0.26 0.0		 1.5	 dB degrees
	Output DC offset[2]	Differential, DCRES=562kΩ	-60		-25		60	mV
I_{OUT}	Output drive current at each pin	Source (Sink)			10 (700)			µA
V_{OUT}	Minimum differential output swing				2.0			V
P_{-1dB}	Input 1dB compression point: In band 200kHz 400kHz 600kHz	1200Ω source EMF	 -59 -54	 -55.3 -49.3	 -53 -47 -47 -47	 -50.7 -44.8	 -47 -40	dBV
t_{ON}	Turn ON time[3]	POnRx = HI, to baseband signal out			2			µs
t_{OFF}	Turn OFF time	POnRx = LO, to no baseband signal out			2			µs
IF Synthesizer								
f_{LO}	Local oscillator input frequency range[9]		140				800	MHz
Z_{LOIN}	Differential input impedance	Between pins LO_{IN} and $LO_{IN}X$, f_{IN} = 800MHz			276 || 0.6			Ω || pF
V_{LOIN}	LO peak input voltage range	Single-ended Referred to 50Ω	50				100	mV
	Programmable divider: Division range Step size		64		 1		511	
f_{CLKIN}	Reference clock input frequency	V_{CLKIN} = 100mV_{PEAK}					52	MHz
Z_{CLKIN}	Differential input impedance	Between pins ClkIn and ClkInX			10 || 1.0			kΩ || pF
V_{CLKIN}	CLK_{IN} peak input voltage range	Single-ended, referred to 50Ω	50				400	mV
I_{REF}	Charge pump input reference current				31.2			µA
| I_{CP} |	Charge pump output current: c0...c2 = 000 c0...c2 = 111 Step size	I_{REF} =31.2µA, V_{CP} = V_{CC}CP/2	 0.425 0.85 0.045	 0.487 0.979 0.062	 0.5 1.0 0.071	 0.513 1.021 0.08	 0.575 1.15 0.105	mA

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
IF Synthesizer (cont.)								
$\frac{\Delta I_{CP}}{I_{CP}}$	Relative output current variation[4]	I_{REF} =31.2µA		0.1	1.3	2.5	±10	%
ΔI_{CP_M}	Output current matching[5]	I_{REF} =31.2µA, V_{CP} = V_{CC}CP/2					±12	%
$\lvert I_{CP\_L} \rvert$	Output leakage current	V_{CP} = 0.3V to V_{CC}CP-0.3V		-0.02	0.1	0.22	±15	nA
t_{ON}	Turn ON time	POnPLL = HI, to full charge pump current			15			µs
t_{OFF}	Turn OFF time[6]	POnPLL = LO, to I_{CC}CP, I_{CC}DIG <5% of operational supply current			15			µs
Serial Interface[7]								
f_{CLOCK}	Clock frequency						10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30					ns
t_H	Hold time: CLOCK to DATA		30					ns
t_W	Pulse width: CLOCK		30					ns
	Pulse width: STROBE		30					

NOTES:
1. Parameter measured relative to modulation sideband amplitude.
2. After programming the DC offset register for minimum offset. DCRES = 562kΩ.
3. The turn on time relates only to the power up time of the circuit. The settling time of the integrated baseband filters has to be added (for GSM–mode = 8µs with filter bandwidth setting resistor = 36kΩ).
4. The relative output current variation is defined thus: $\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{\lvert(I_2 + I_1)\rvert}$; with V_1 = 0.3V, V_2 = V_{CC}CP – 0.3V (see Figure 3).
5. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.
6. As soon as P_{ON}PLL is set to LO, the phase detector is reset and no charge pumps pulses are generated.
7. Guaranteed by design.
8. NF = $\left[20 \log \left(\frac{E_{no}}{\sqrt{4kTR}} \right) \right] - VG$ where, E_{no} is the output noise voltage measured in a 1Hz bandwidth, R = 1200Ω, VG = gain in dB.
9. Minimium frequency is guaranteed by design.

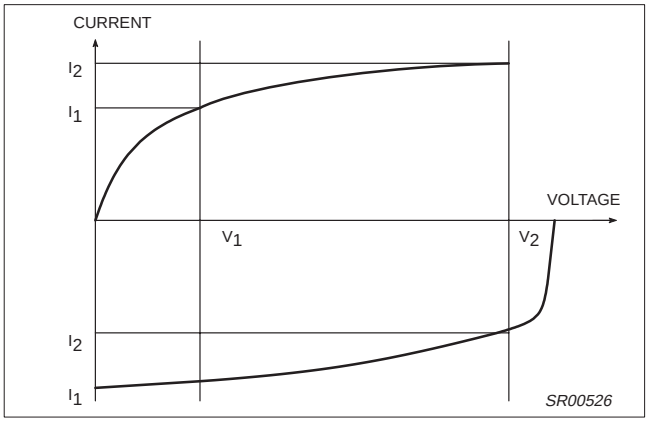


Figure 3. Relative Output Current Variation

FUNCTIONAL DESCRIPTION

Serial Programming Input

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program the counter ratios, charge pump current, status- and DC-offset register, mode select and test register. The programming data is structured into two 21-bit words; each word includes 4 chip address bits and 1 subaddress bit. Figure 2 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the value of the subaddress bit the data is latched into different working registers. Table 3 shows the contents of each word.

Default States

Upon power up (V_{CC}DIG is applied) a reset signal is generated, which sets all registers to a default state. The logic level at the STROBE pin should be low during power up to guarantee a proper reset. These default states are shown in Table 3.

Reference Divider

The reference divider can be programmed to four different division ratios (:13, :26, :39, :52), see registers r0, r1; default setting: divide by 13.

Main Divider

The external VCO signal, applied to the LO_{IN} and LO_{IN}X inputs, is divided by two and then fed to the main divider (:N). The main divider is a programmable 9 bit divider, the minimum division ratio is

divide by 64. The division ratio is binary coded and set in the registers n0 to n8. The default setting is a divide by 400.

At the completion of a main divider cycle, a main divider output is generated which will drive the phase detector.

Phase Detector

The phase detector is a D-type flip-flop phase and frequency detector shown in Figure 5. The flip-flops are set by the negative edges of the output signals of the dividers. The rising edge of the signal L will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump acts to increase the VCO frequency; a sink current acts to decrease the VCO frequency.

Current Setting

The charge pump current is defined by the current set between the pin I_{REF} and $V_{EE}CP$. The current value to be set there is 31.2µA. This current can be set by an external resistor to be connected between the pin I_{REF} and $V_{EE}CP$. The typical value R_{EXT} (current setting resistor) can be calculated with the formula

$$R_{EXT} = \frac{V_{CC}CP - 1.4V}{31.2\mu A}$$

The current can be set to zero by connecting the pin I_{REF} to $V_{CC}CP$.

Charge Pumps

The charge pumps at pin CP are driven by the phase dectector and the current value is determined by the binary value of the charge pumps register CN = c2, c1, c0, default 1mA. The active charge pump current is typically:

$$|I_{CP}| = (c0 + 2c1 + 4c2) \cdot 71\mu A + 500\mu A$$

Lock Detect

The output LOCK is H when the phase detector indicates a lock condition. This condition is defined as a phase difference of less than ±1 cycle on the reference input CLK_{IN}, $CLK_{IN}X$.

Test Modes (Synthesizer, Transmit Mixer)

The LOCK output is selectable as a test output. Bits x0, x1 control the selection, the default setting is normal lock output as described in the Lock detect section. The selection of a Bit x0, x1 combination has a twofold effect: First it routes a divider output signal to the LOCK pin, second it disables mixer stages in the transmit path. Setting x0,1 = 11 disables both transmit path mixers. This mode can be used to prevent the transmitter from producing an IF output signal even if the transmit part is powered on (PDTx = 0V). This can be used to simplify the control timing while commanding the transmit and receive simultaneously without the transmit part causing interference.

Table 1. Test Modes

x0	x1	Synthesizer Signal at LOCK Pin	Transmit Mixer	
			Q-mixer	I-mixer
0	0	normal lock detect	on	on
1	0	CLK_{IN} divided by reference divider ratio	off	on
0	1	LO_{IN} ÷ 2 * (main divider ratio)	on	off
1	1	main divider output, that goes to the phase detector	off	off

Status Register

The s0 and s1 status bits determine the values of the logic output pins A_{OUT} and B_{OUT}. These outputs can be connected to the AGC control inputs A and B of the SA1620. (See Figure 9)

DC Offset Register

Registers i0 to i3 and q0 to q3 control a correction to the output DC offset of the I and Q channels of the receiver. The polarity of the DC offset correction in the I and Q channels are determined by i0 and q0, respectively. The other bits set the magnitude of the offset correction. The step size of the two offset correction DACs is fixed by an external resistor between the DCRES pin and ground. A value of 120kΩ will give a step size of 200mV.

Mode Select Register

t0: switches the RX IF gain.
- t0 = 0 no attenuation
- t0 = 1 10dB attenuation

The attenuation switch is included between the IF amplifier and the I and Q mixers, thereby influencing the noise figure negligibly. The purpose of this switch is to provide another AGC step which does not influence the receiver noise figure. Please note that this gain change will influence the DC offset of the I and Q mixers.

t1 = 0 test mode only, always to be set to 0.

t2, t3 sets the mode of the level locked loop (LLL)

The LLL is a circuit which processes the LO input signal in order to provide an LO signal with a perfect 50% duty cycle, which determines the precision of the 90° shift of the I and Q mixing signals generated by the ÷2 divider. For an external tuning of the 90° phase shift of the I and Q mixing signals, a trimming resistor may be connected (but is not required) between the ADJ_{IN} pin and ground, and the LLL has to be put in one of the following modes:

Table 2. Mode Select Register

t2	t3	LLL Status
0	0	LLL on (no external tune, monitor performance, default)
0	1	LLL on (with medium external tune)
1	0	LLL off (tune externally)
1	1	LLL on (with fine external tune)

t4 selects the bandwidth of the RC low pass filters at the I, Q Rx mixer outputs
- t4 = 0 cutt-off frequency (-3dB) 110kHz
- t4 = 1 cutt-off frequency (-3dB) 792kHz

t5 selects the bandwidth of the integrated 5th-order gyrator filters. The filters are tuneable over a range of 50kHz to 1MHz with external resistors. The -3dB bandwidth is inversely proportional to the value of the external resistor.

With

t5, two external resistor values are selectable.
- t5 = 0 the resistance between the pins RESA and RESB determines the cutoff frequency. For GSM a nominal bandwidth of 80kHz is chosen when the external resistor is 36kΩ.
- t5 = 1 a second resistor between the pins RESB and RESD is connected in parallel to the first external resistor, thus increasing the filter bandwidth. The relative amplification is decreased in this mode.

The overall filter response in the receive section is the sum of the filter responses of the passive RC low-pass filter and the active gyrator filter.

Power Down Modes

There are 4 power-on pins in the SA1638: P_{ON}, P_{ON}Rx, PDTx, P_{ON}PLL.

P_{ON} = H powers up both voltage regulators $V_{REG}1$ and $V_{REG}2$. P_{ON} should be set to L, if these internal voltage regulators are not to be used.

P_{ON}Rx = H powers up the receiver part.

PDTx = L powers up the transmitter part.

P_{ON}PLL = H powers up the synthesizer part. As it also powers up the first divide by 2 stage for generating the 0/90 degree phase shifted signals for the transmit and receive mixers, it also has to be set H if either the transmit part or the receive part is used. P_{ON}PLL = L powers down the dividers, resets the phase detector and disconnects the current setting pin I_{REF}. In P_{ON}PLL = L mode, the values in the serial input registers are still kept and the part still can be reprogrammed as long as V_{CC}DIG is present.

Table 3. Definition of SA1638 Serial Registers

First data word: (shown with default values)

Address SA1638				Sub Adr	N-Divider									Ref ÷ Reg		Charge-Pump			Reg Test	
MSB																				LSB
a0	a1	a2	a3	sa	n0	n1	n2	n3	n4	n5	n6	n7	n8	r0	r1	c0	c1	c2	x0	x1
1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	1	1	1	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 0 for first data word
N-Divider:	9 bits, n0...n8, values 64 (00100 0000) to 511 (111111111) allowed for IF-choice, default 400
Reference Divider Register:	2 bits, r0...r1, 00 = ÷13, 01 = ÷26, 10 = ÷39, 11 = ÷52. Default: 00
Charge-Pump Register:	3 bits, c0...c2, Binary current setting factor for charge pumps, values 000 = minimum current to 111 = maximum current, default maximum charge pump current
Test Register:	2 bits, x0...x1, default 00, see Functional Description

Second data word: (shown with default values)

Address SA1638				Sub Adr	Status Reg	DC Offset Register								Mode Select Register						
						Q-Channel					I-Channel									
MSB																				LSB
a0	a1	a2	a3	sa	s0	s1	q0	q1	q2	q3	i0	i1	i2	i3	t0	t1	t2	t3	t4	t5
1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 1 for second data word
Status Register:	2 bits, s0 sets pin A_{OUT}; s1 sets pin B_{OUT}, see Functional Description
DC Offset Register:	4 bits per channel, i0...i3 and q0...q3, no correction as default i0 and q0 switches offset polarity, 0 to lower voltage, 1 to higher voltage il...i3 and q1...q3, 000 no correction to 111 max. correction enabled
Mode Select Register:	6 bits, t0...t5, 000000 = normal GSM-Operation as default, see Functional Description

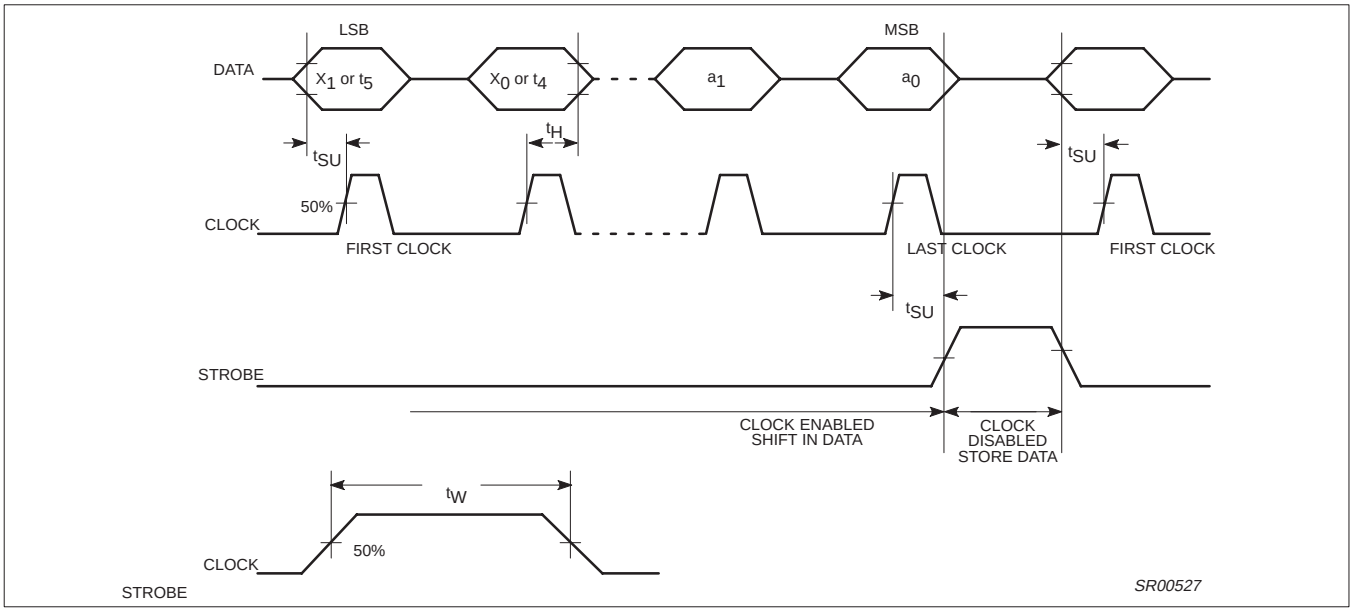


Figure 4. Serial Input Timing Sequence

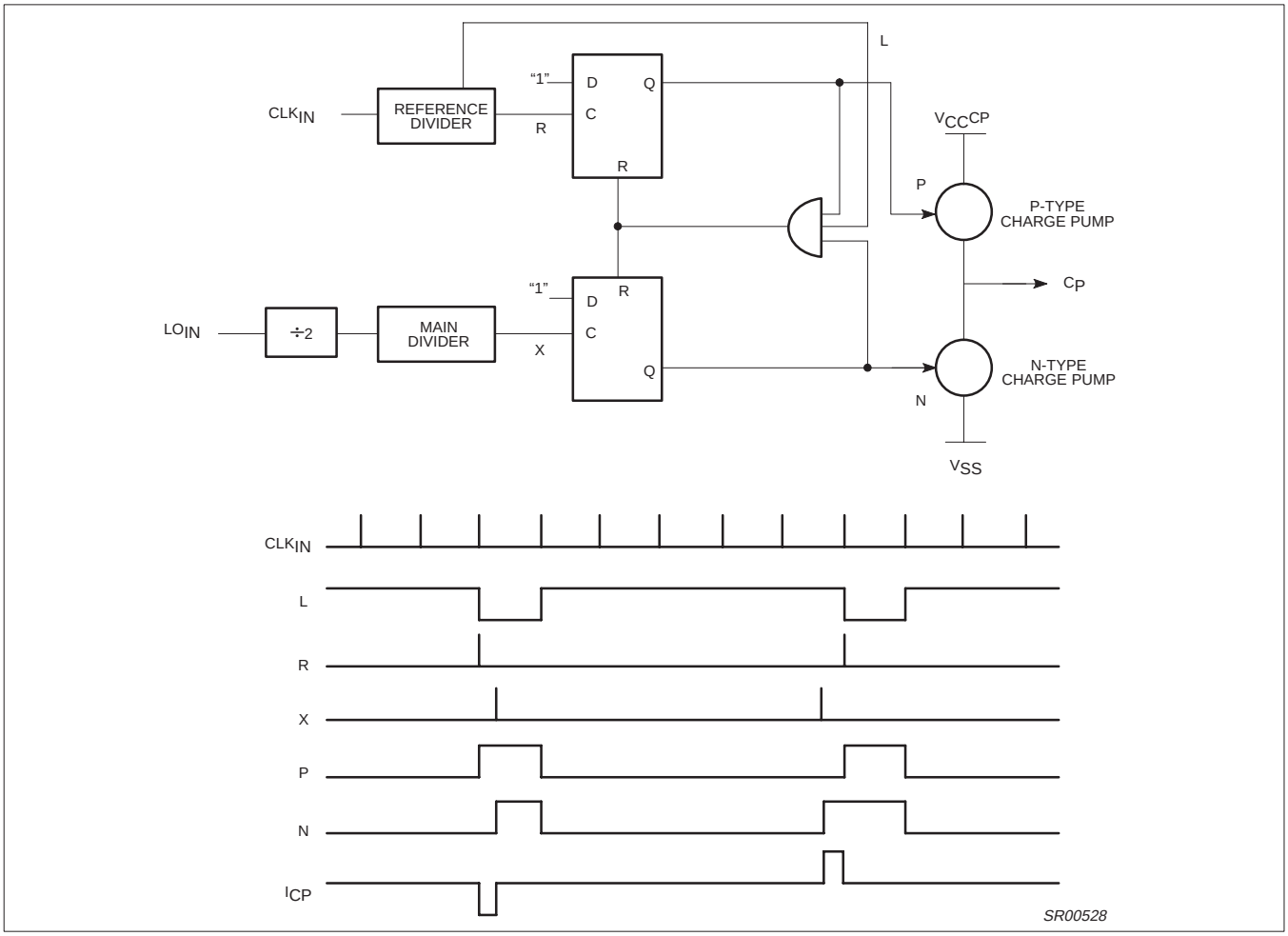
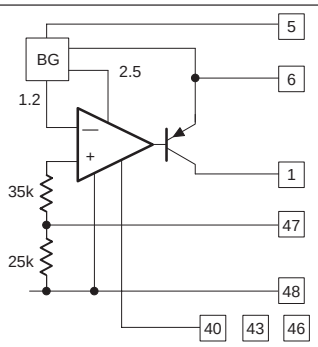
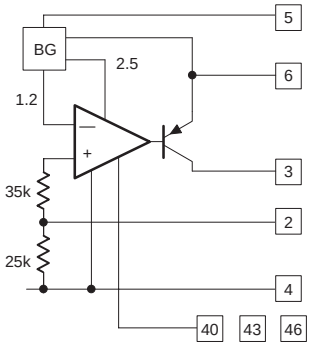
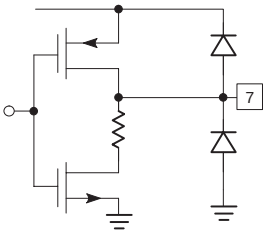
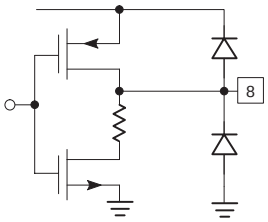
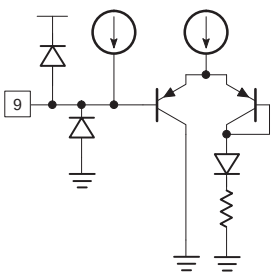
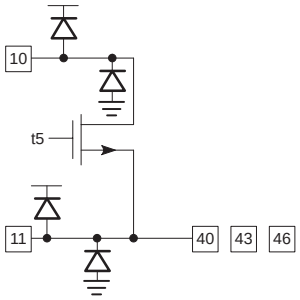
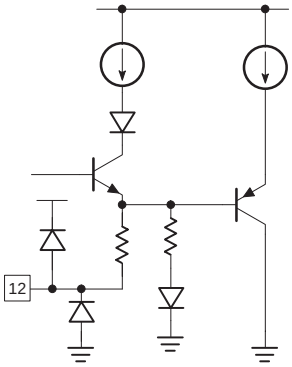
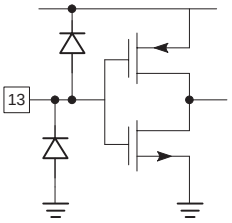
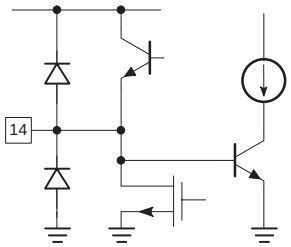
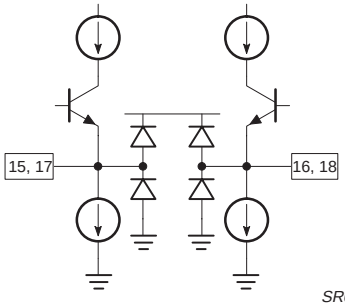


Figure 5. Phase Detector Structure with Timing

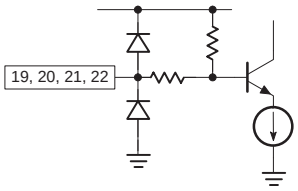
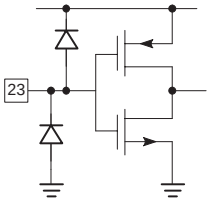
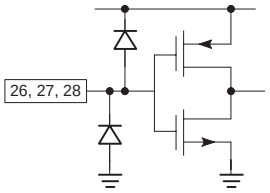
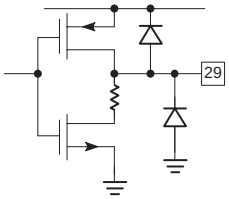
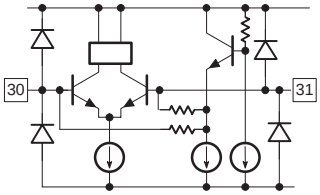
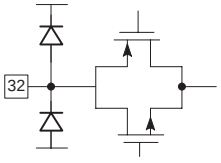
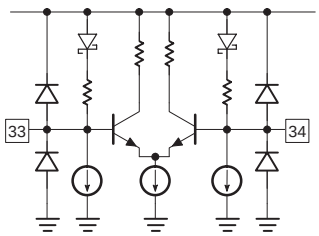
PIN FUNCTIONS

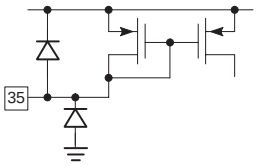
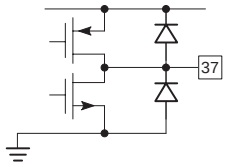
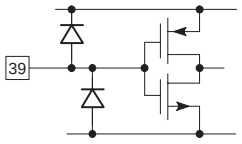
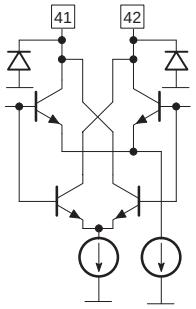
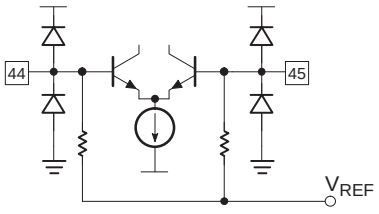
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
47	V_{CC}TxRx	3.0	
48	$GND_{REG}1$	0.0	
1	$V_{REG}1$	3.0	
2	$V_{REG}F2$	3.0	
3	$V_{REG}2$	3.0	
4	$GND_{REG}2$	0.0	
5	P_{ON}	3.3	
6	V_{BATT}	3.3	
7	A_{OUT}	3.0	
8	B_{OUT}	3.0	
9	DC_{RES}	1.6	
10	RES_D	0.05	
11	RES_A	0.00	
12	RES_B	0.05	
13	$P_{ON}Rx$	3.0	
14	V_{REF}	1.5	
15	QRX_{OUT}	1.5	
16	$QRX_{OUT}X$	1.5	
17	IRX_{OUT}	1.5	
18	$IRX_{OUT}X$	1.5	

SR00529

Figure 6. Pin Functions

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
19	QTX_{IN}	1.5	
20	$QTX_{IN}X$	1.5	
21	ITX_{IN}	1.5	
22	$ITX_{IN}X$	1.5	
23	PdTx	0.0	
24	$V_{CC}DIG$	3.0	
25	$V_{EE}DIG$	3.0	
26	DATA		
27	CLOCK		
28	STROBE		
29	LOCK		
30	CLK_{IN}	2.0	
31	$CLK_{IN}X$	2.0	
32	ADJ_{IN}	2.0	
33	LO_{IN}	2.0	
34	$LO_{IN}X$	2.0	

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
35	I_{REF}	1.6	
36	$V_{EE}CP$	0.0	
37	CP		
38	$V_{CC}CP$	3.0	
39	$P_{ON}PLL$	3.0	
40	GND3	0.0	
41	$TXIF_{OUT}X$	OPEN COLLECTOR	
42	$TXIF_{OUT}X$	OPEN COLLECTOR	
43	GND2	0.0	
44	$RxIF_{IN}X$	1.5	
45	$RxIF_{IN}$	1.5	
46	GND1	0.0	
47	$V_{CC}TxRx$	3.0	
48	$GND_{REG}1$	0.0	

SR00530

Figure 7. Pin Functions (cont.)

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The IF may be chosen freely in the range 70–400 MHz. The same IF can be used in the transmit and receive directions. Alternately, different IFs can be used if the SA1638 synthesizer frequency is switched between transmit and receive timeslots. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs in the SA1620 allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. Placing the AGC gain switches at the front results in some attenuation most of the time, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +7.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption, the output power can be reduced to an appropriate level by choice of an external resistor.
- DC offsets generated in the receive channel are independent of the LNA AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filter requirements to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the SA1620 LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

DC Offset Correction

DC offset correction is provided by two DACs each feeding into one of the two Rx channels. The step size of both DACs is set by the value of the external resistor between DCRES and ground. Thus any original offset less than 1.5V magnitude in either channel can be reduced to the specified level by selecting the appropriate DAC setting via the serial interface.

Integrated Receive Filters

The low-pass characteristics of the Rx channel are determined by two low-pass responses. The first of these is a passive filter at the output of the quadrature mixers and the second is the low-pass filters which follow the post-mixer amplifiers. These specifications refer only to the response of the default state, but this may be switched by the control register to an alternative setting with a nominal 3dB point of 792kHz.

The corner frequency of the low pass filters can be adjusted over a wide range by varying the value of the external resistor between RESA and RESB. The range of feasible corner frequencies extends at least between 50kHz and 500kHz.

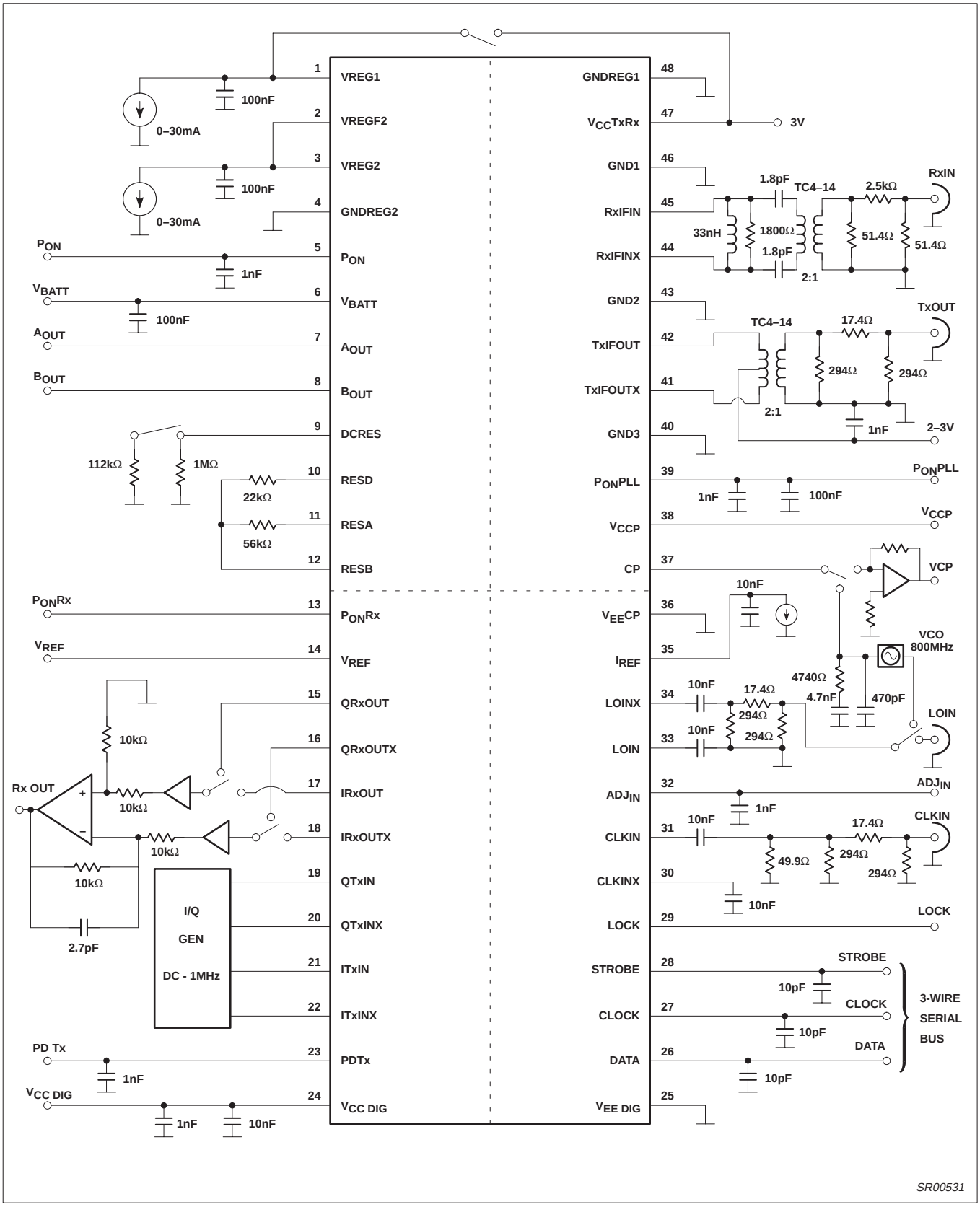


Figure 8. SA1638 Test Circuit

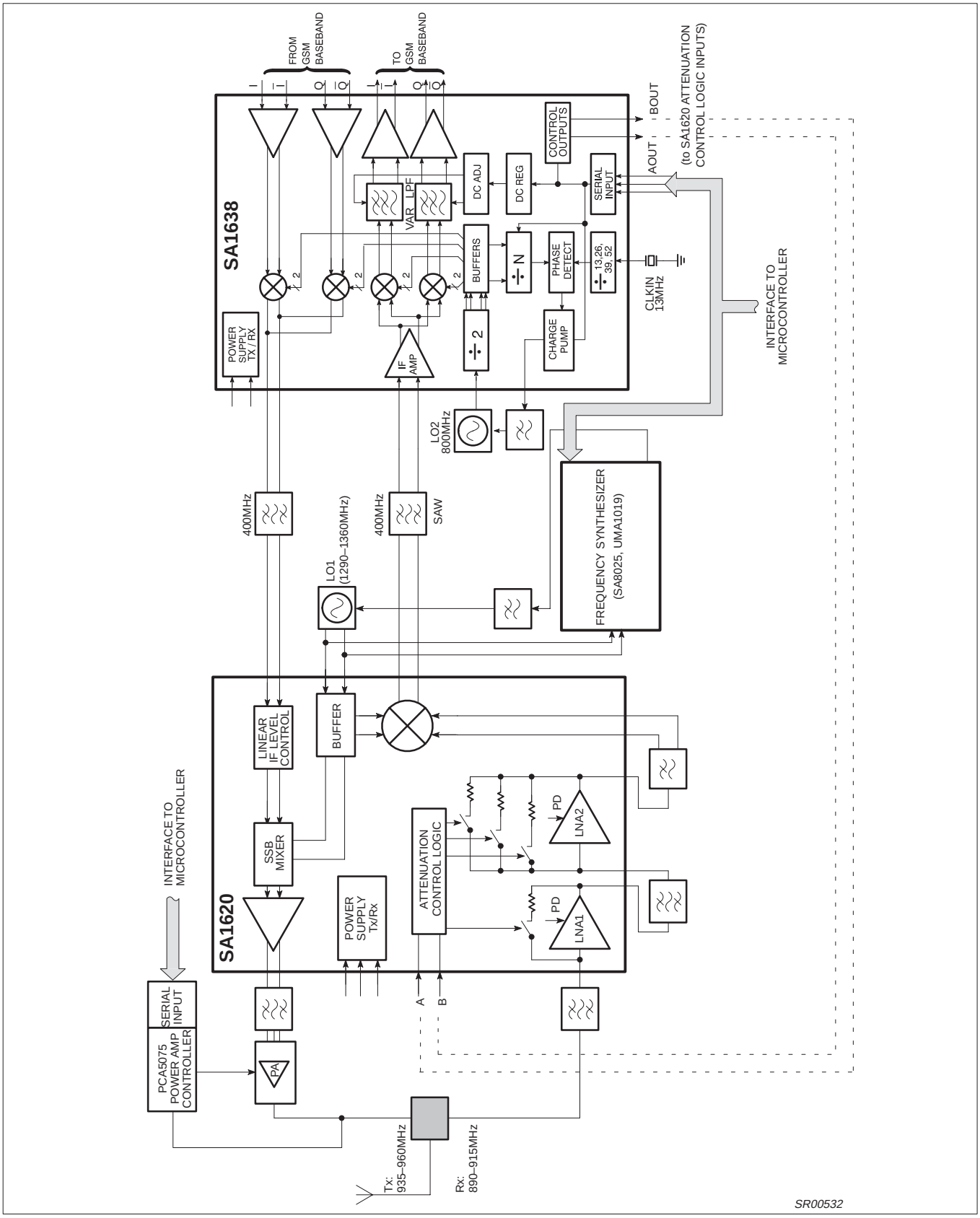
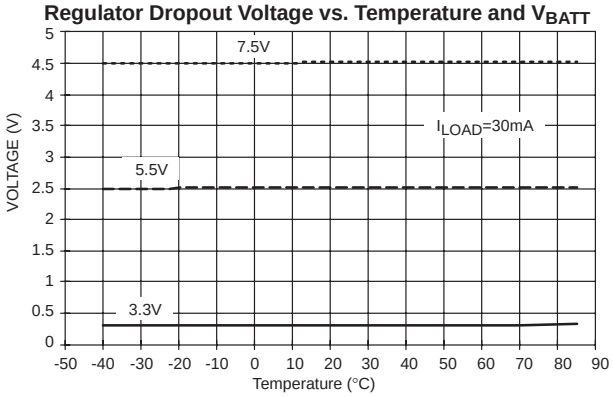


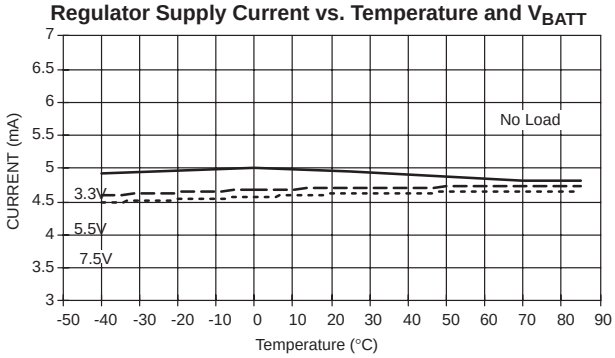
Figure 9. SA1620 / SA1638 System Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

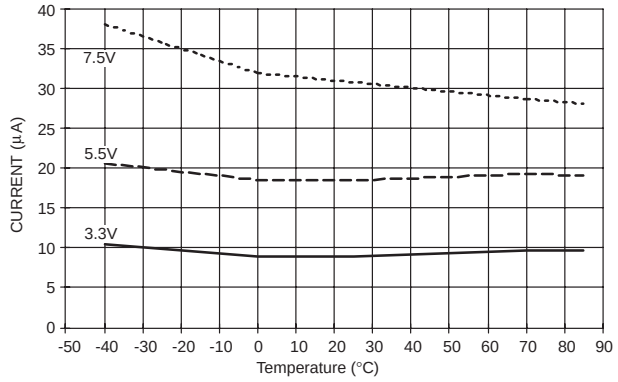
Regulator Dropout Voltage vs. Temperature and V_{BATT}



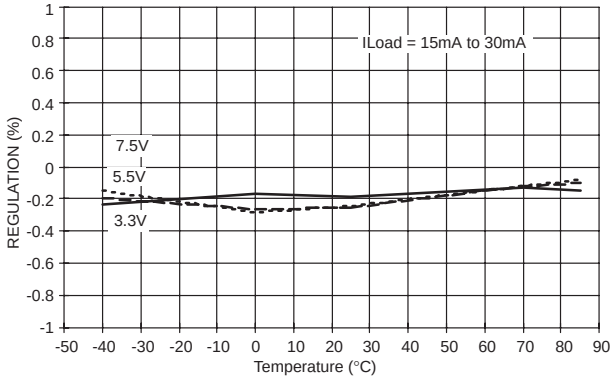
Regulator Supply Current vs. Temperature and V_{BATT}



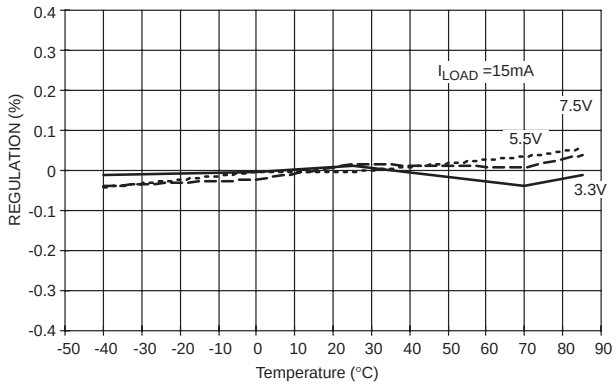
Regulator Powerdown Supply Current vs. Temperature and V_{BATT}



Regulator Load Regulation vs. Temperature and V_{BATT}



Regulator Line Regulation vs. Temperature and V_{BATT}



Regulator Output Voltage vs. Temperature and V_{BATT}

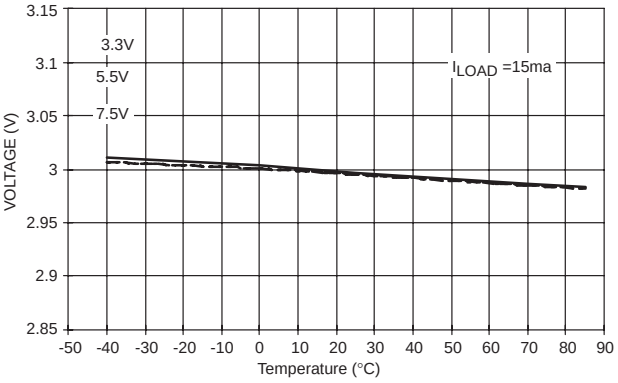
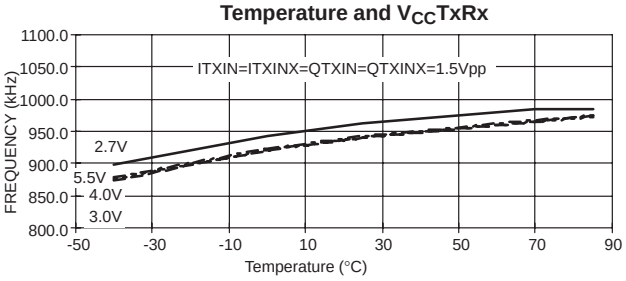


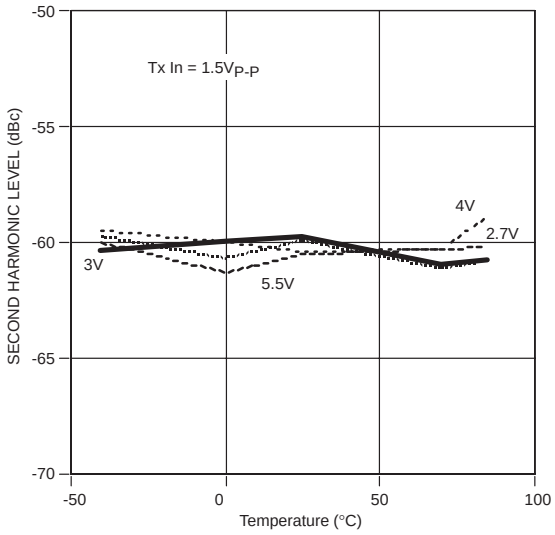
Figure 10. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

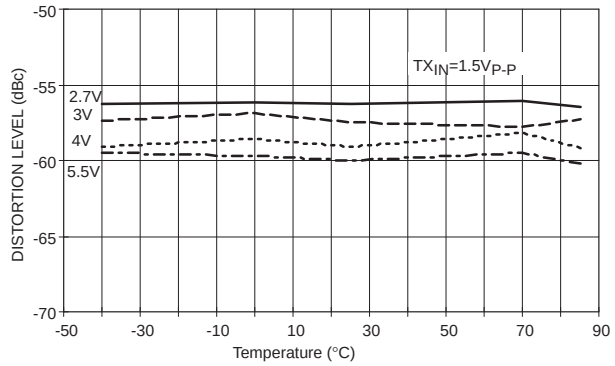
Transmitter Input Modulation Bandwidth vs. Temperature and V_{CC}TxRx



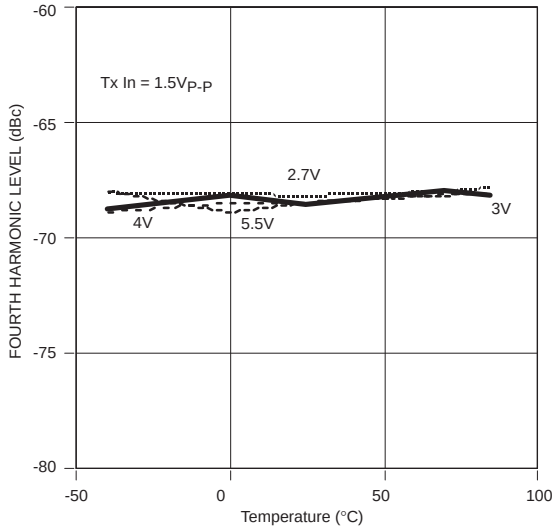
Transmitter Output Second Harmonic Distortion



Transmitter Output Third Harmonic vs. Temperature and V_{CC}TxRx



Transmitter Output Fourth Harmonic Distortion



Transmitter Output Fifth Harmonic Distortion

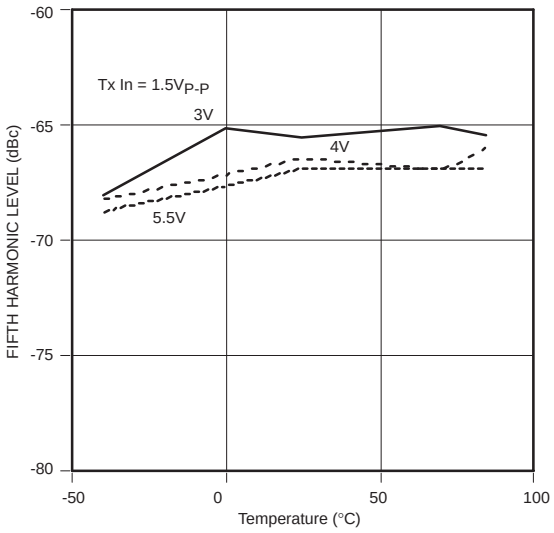
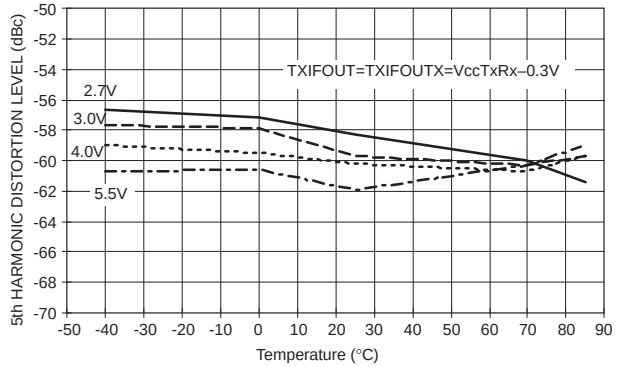


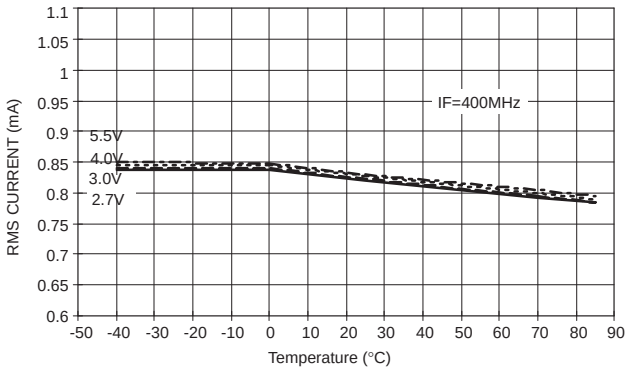
Figure 11. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

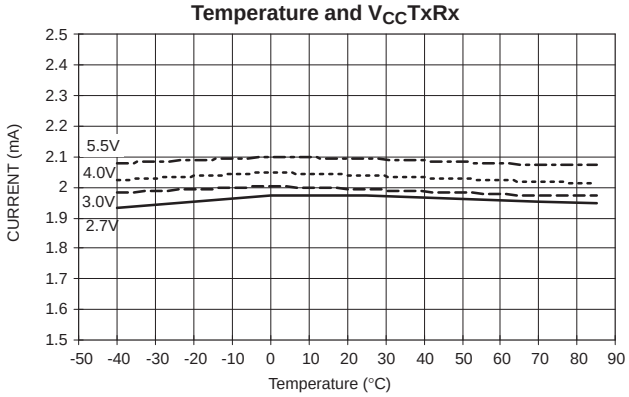
Transmitter Output Saturation vs. Temperature and VccTxRx



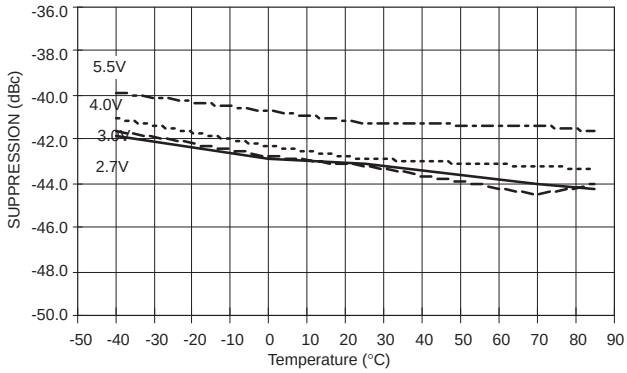
Transmitter RMS Output Current vs. Temperature and V_{CC}TxRx



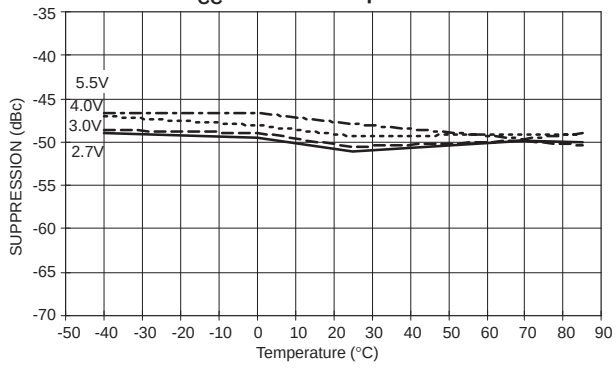
Transmitter DC Output Current vs. Temperature and V_{CC}TxRx



Transmitter LO Suppression vs. Temperature and VccTxRx



Transmitter Side Band Suppresion vs. V_{CC}TxRx and Temperature



Transmit Noise Floor vs Temperature and Supply Voltage

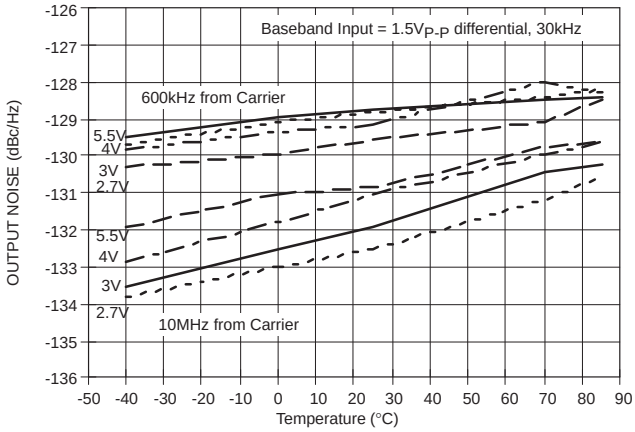
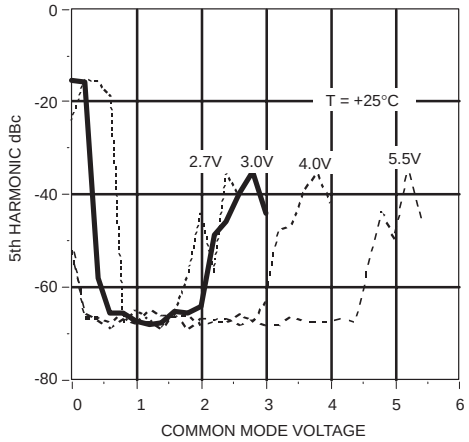


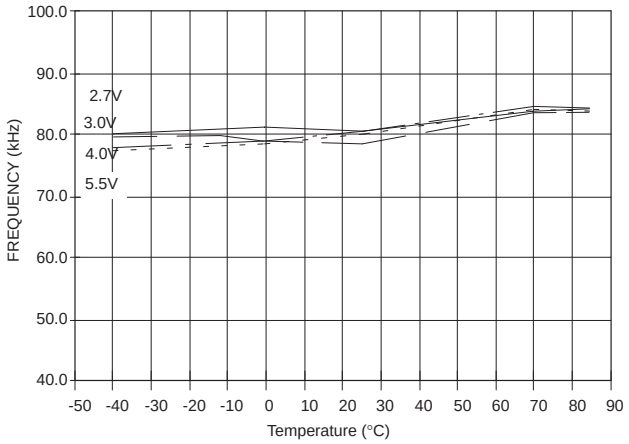
Figure 12. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

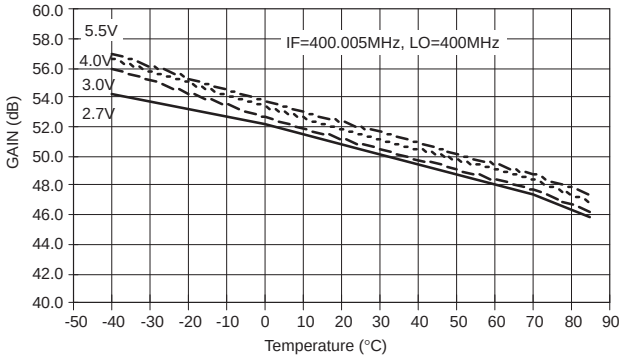
Transmitter Input Common Mode Range Vs. Supply Voltage



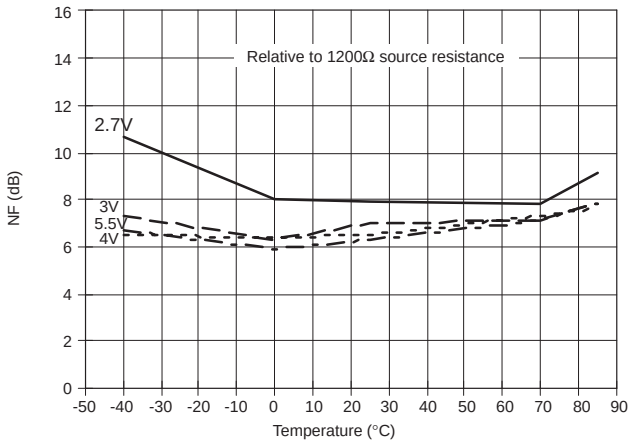
Receiver 3dB Bandwidth vs. Temperature and V_{CC}TxRx



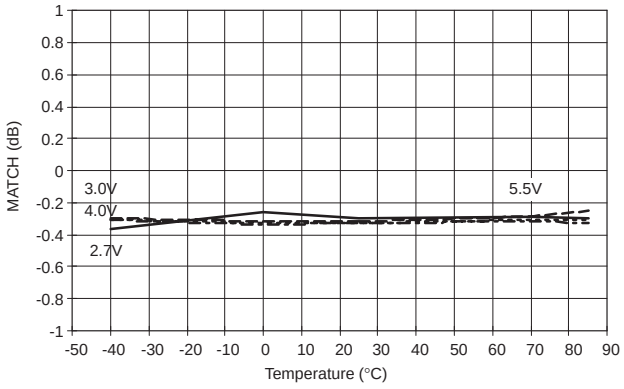
Receiver Gain vs. Temperature and V_{CC}TxRx



Receiver NF vs Temperature and Supply Voltage



Receiver Gain match vs V_{CC}TxRx and Temperature



Receiver Channel Matching Phase Error vs. Temperature and V_{CC}TxRx

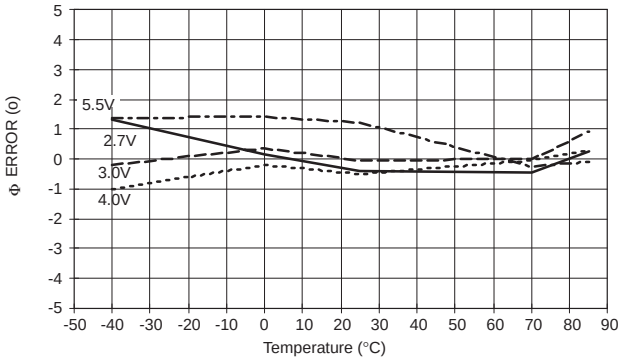
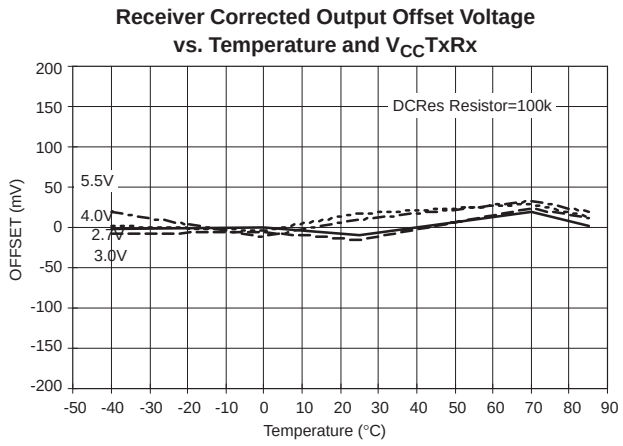
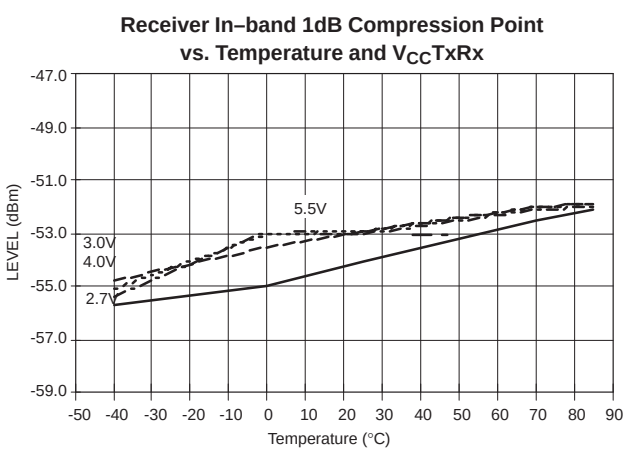
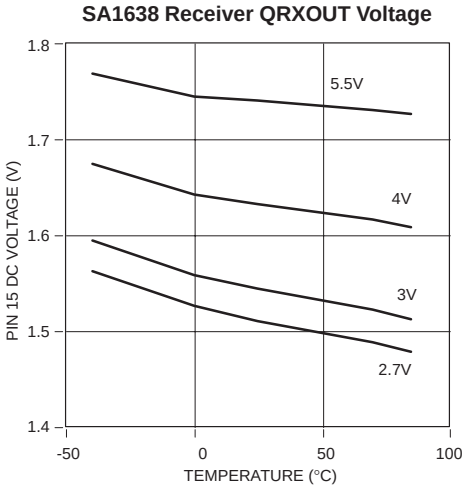


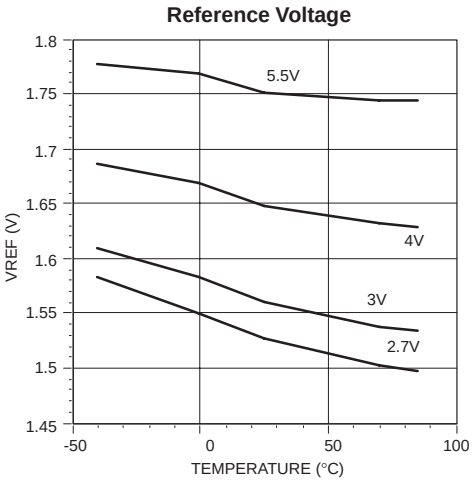
Figure 13. Typical Performance Characteristics (continued)

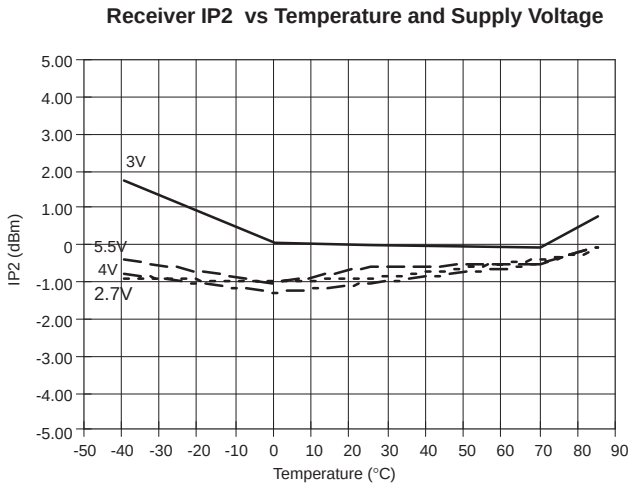
TYPICAL PERFORMANCE CHARACTERISTICS (continued)











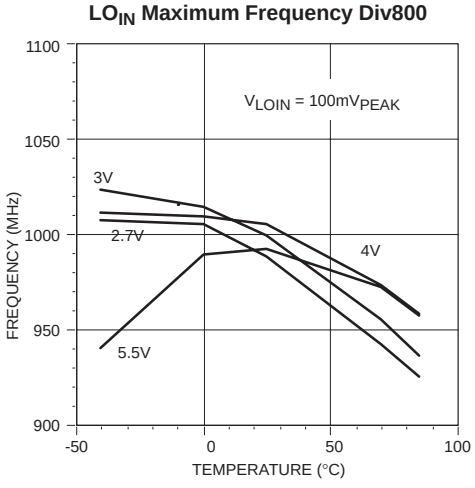


Figure 14. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

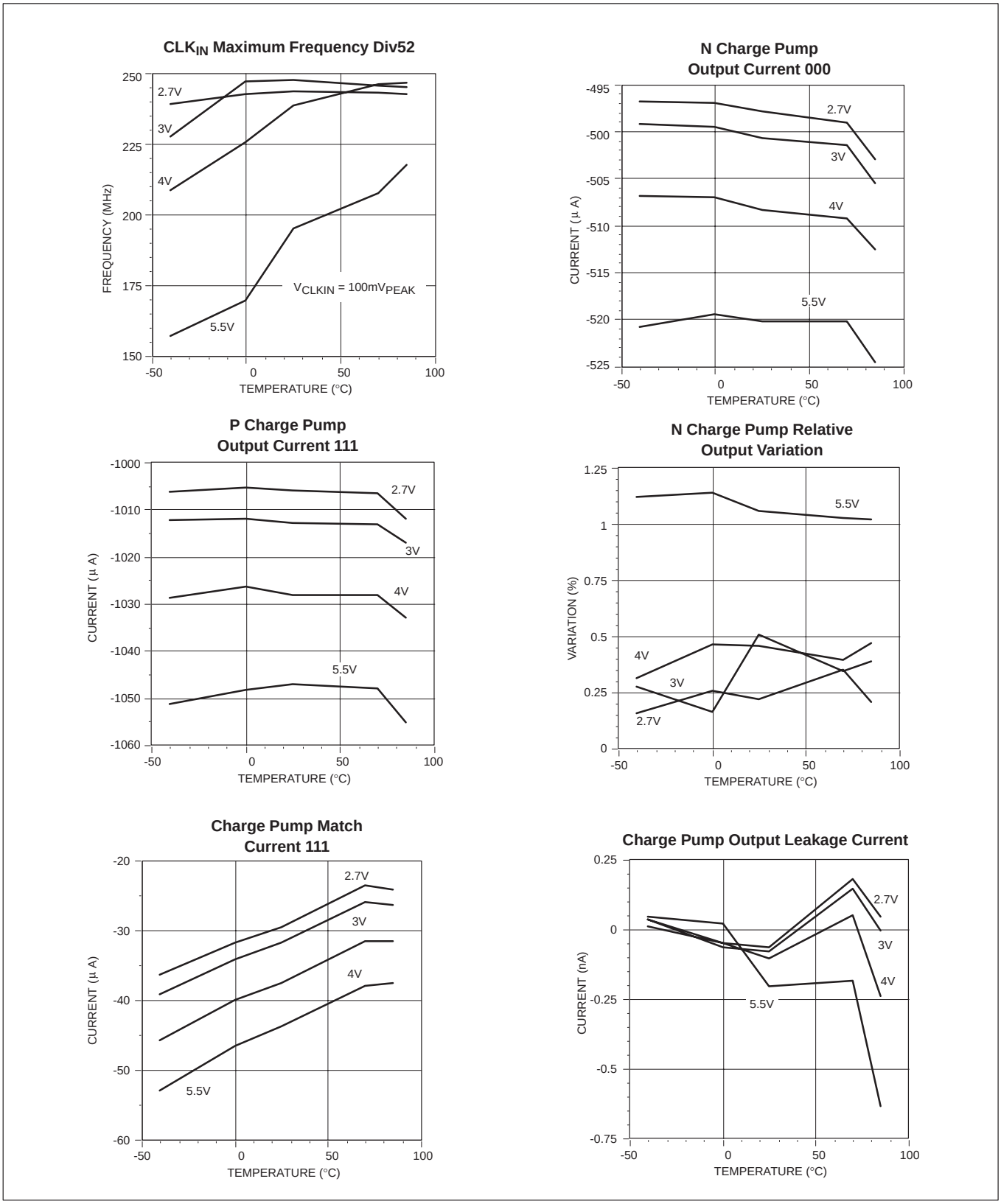
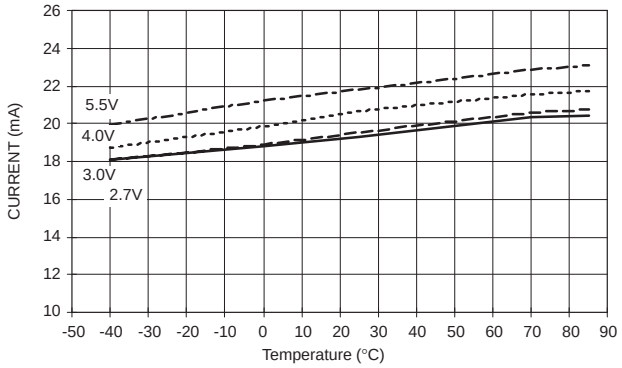


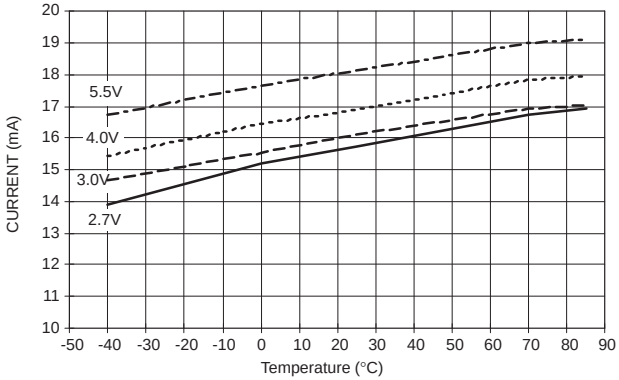
Figure 15. Typical Performance Characteristics (continued)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

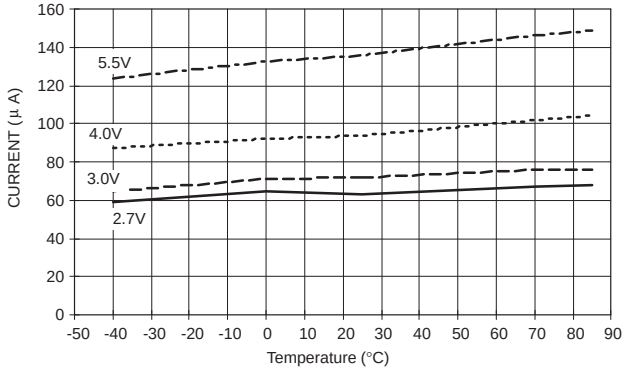
Transmitter Supply Current vs. Temperature and V_{CC}TxRx



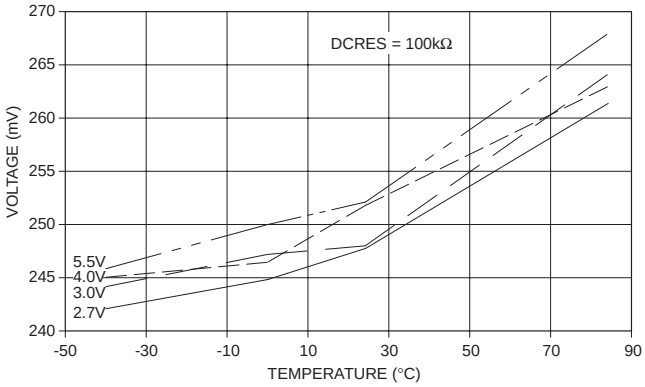
Receiver Supply Current vs. Temperature and V_{CC}TxRx



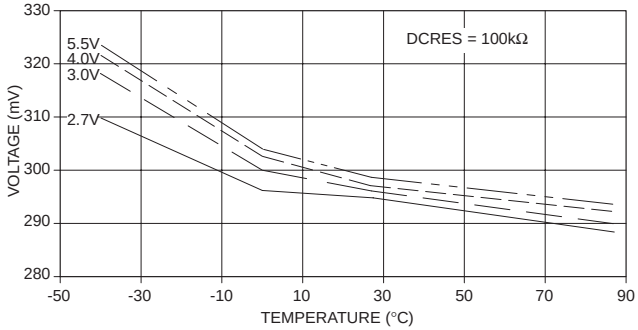
Power Down Supply Current vs. Temperature and V_{CC}TxRx



Receiver Uncorrected Output Offset Voltage vs Temperature and V_{CC}TxRx



Receiver Output Offset Control Step Size vs Temperature and V_{CC}TxRx



Receiver Output Offset Control Step Size vs Temperature and V_{CC}TxRx

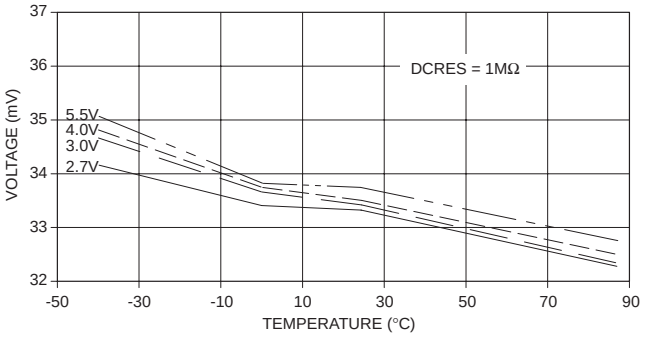
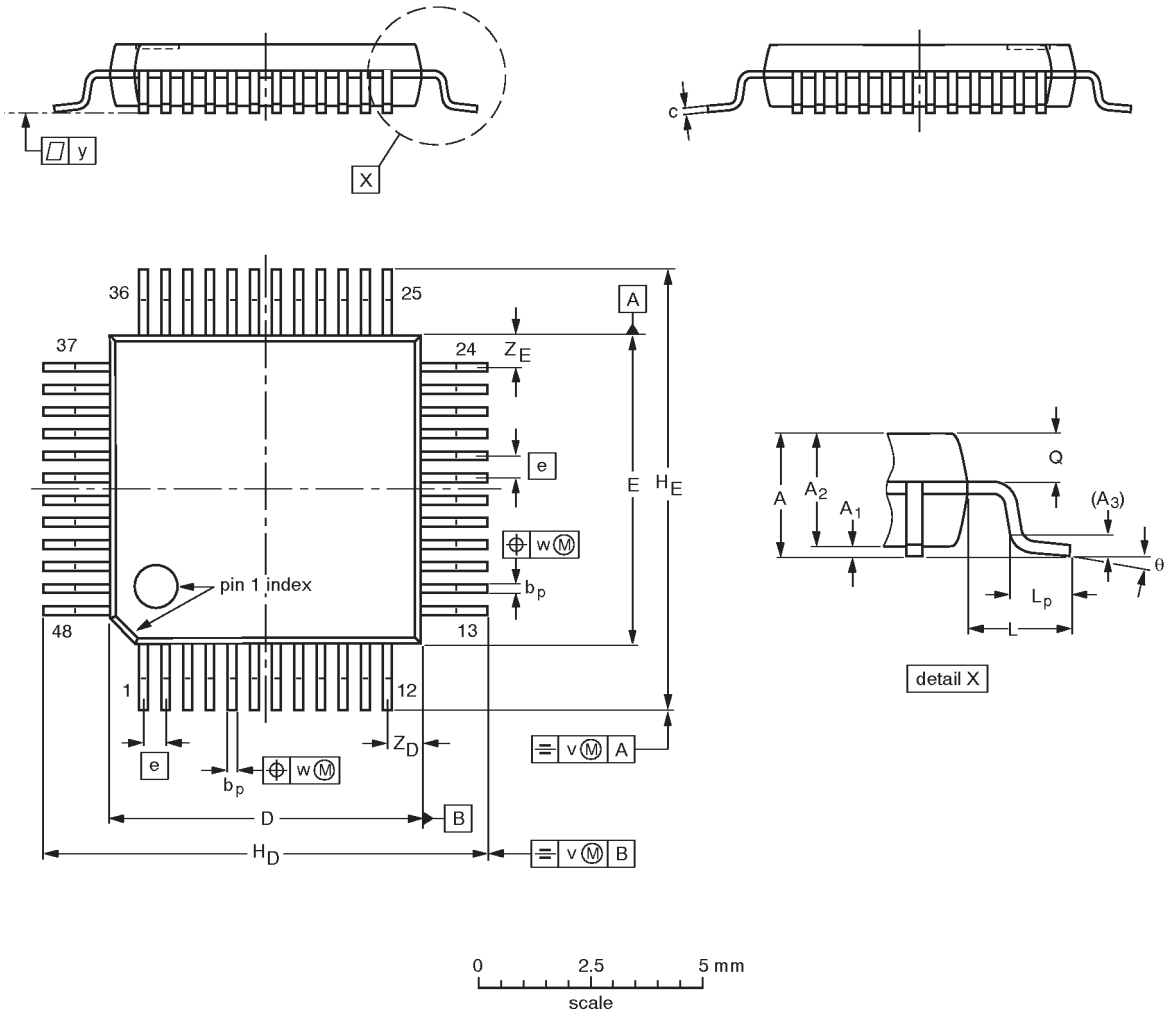


Figure 16. Typical Performance Characteristics (continued)

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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