SA21308A00DED

Low I_Q, Low Dropout, Automotive 500mA LDO

General Description

The SA21308A is a 500mA current linear regulator featuring ultra-low ground current and low dropout voltage.

The device offers an adjustable output voltage with ±1% reference accuracy over temperature, also includes comprehensive protection features including over current limiting, short circuit protection, and over-temperature operation.

The SA21308A is available in a compact DFN2×2-6 package.

Applications

- Infotainment Power Supplies
- Automotive Cluster Displays
- Cameras
- Telematics Control Units
- General Purpose Automotive

Features

- Input Voltage Range: 1.62V to 6V
- Adjustable Output Voltage: 0.55V to 5.5V
- Low Dropout Voltage: 110mV (Typ.) at 500mA (3.3V V_{OUT})
- Power Supply Rejection Ratio (PSRR): 55dB @ 1kHz
- Output Accuracy:
  - ±0.85% at 25°C
  - ±1% from -40°C to 125°C
- Stable with a Minimum of 2.2μF or Larger Ceramic Output Capacitor
- Low Current Consumption: Typical 25μA Quiescent and 0.1μA in Shutdown
- Over Current Limit and Short Circuit Protection
- Over Temperature Protection with Auto Recovery
- Moisture Sensitivity Level (MSL): 1
- Compact DFN2×2-6 Package
- Automotive AEC-Q100 Grade 1 Qualified

Typical Application

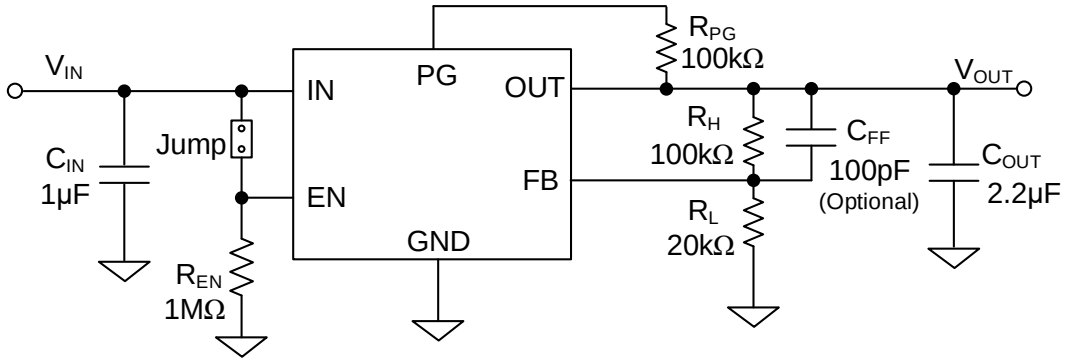


Figure 1. Typical Application Schematic

Ordering Information

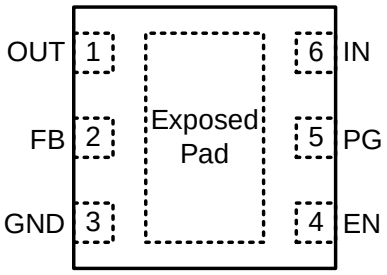
SA21308□□□(□□□)

- Package Code
- Output Voltage Code
- Optional Spec Code

Ordering Part Number	Output Version	Package Type	Top Mark
SA21308A00DED	Adjustable	DFN2×2-6 (RoHS Compliant and Halogen Free)	HFXxyz

x=year code, y=week code, z= lot number code

Pinout (Top View)



DFN2×2-6

Pin Description

Pin No.	Pin Name	Description
1	OUT	Output voltage pin. Decouple this pin to GND with a minimum 2.2μF ceramic capacitor.
2	FB	Feedback pin. This pin is the input to the control loop error amplifier and is used to set the output voltage of the device.
3	GND	Device GND. Connect to the device thermal pad.
4	EN	Enable pin. This pin turns the LDO on and off. If $V_{EN} \geq V_{EN(HI)}$, the regulator is enabled. If $V_{EN} \leq V_{EN(LO)}$, the regulator is disabled. The EN pin must be connected to IN if the enable function is not used.
5	PG	Open-drain power-good indicator pin for the LDO output voltage. A 10kΩ to 100kΩ external pull-up resistor is required. This pin can be left floating or connected to GND if not used.
6	IN	Input pin. Decouple this pin to GND with a recommended 1μF or larger ceramic capacitor.
Exposed Pad		The exposed pad is electrically connected to GND. Connect a GND plane or large copper area for improved thermal performance.

Block Diagram

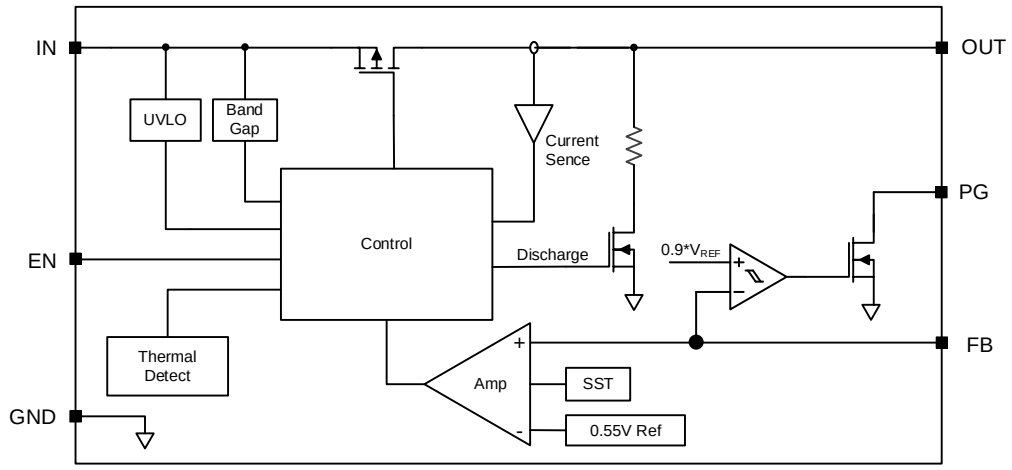


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
IN, EN, PG, OUT		-0.3	6.5	V
FB		-0.3	2	
Junction Temperature, Operating		-40	150	°C
Lead Temperature (Soldering, 10s)			260	
Storage Temperature		-65	150	
V_{ESD} Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101		±750	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction to Ambient Thermal Resistance	68.0	°C/W
$\theta_{JC, Top}$ Junction to Top of the Case Thermal Resistance	47.8	
$\theta_{JC, Bot}$ Junction to Bottom of the Case Thermal Resistance	14.1	
PD Power Dissipation T_A = 25°C	1.83	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	1.62	6	V
OUT	0.55	5.5	
Output Current	0.001	0.5	A
Ambient Temperature, Range	-40	125	°C

Electrical Characteristics

(V_{IN}=$V_{OUT(NOM)}$+0.5V or 1.62V (which is greater), I_{OUT}=1mA, V_{EN}=V_{IN}, C_{IN}=1μF, C_{OUT}=2.2μF, T_J = -40°C~125°C, unless otherwise specified, all typical values are at T_J=25°C (Note 4)).

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		1.62		6	V
	UVLO, rising	$V_{ULVO, rising}$	V_{IN} rising		1.45	1.62	V
	UVLO, falling	$V_{ULVO, falling}$	V_{IN} falling		1.41	1.58	
	UVLO Hysteresis	V_{UVLO_HYS}	V_{IN} hysteresis		40		mV
	Shutdown Current	I_{SHDN}	V_{EN}=0V,-40℃ ≤ T_J ≤ 125℃		0.1	1.5	μA
	Ground Current	I_{GND}	I_{OUT}=0mA, T_J=25℃			50	μA
			I_{OUT}=0mA, -40℃ ≤ T_J ≤ 125℃		25	55	
Output	Voltage	V_{OUT}		0.55		5.5	V
	Output Accuracy (Note 6)	V_{OUT_ACC}	T_J=25℃	-0.85		0.85	%
			-40℃ ≤ T_J ≤ 125℃	-1		1	
	Line Regulation	ΔV_{LNR}	$V_{OUT(NOM)}$+0.5V≤V_{IN}≤6V		2	7.5	mV
	Load Regulation	ΔV_{LDR}	V_{IN}≥2.0V,0.1mA≤I_{OUT}≤0.5A		0.03		V/A
Feedback	Voltage	V_{FB}			0.55		V
	Feedback Pin Current	I_{FB}			0.01	0.1	μA
Enable	High Voltage	$V_{EN(HI)}$		1.1			V
	Low Voltage	$V_{EN(LO)}$				0.3	
	Enable Pin Current	I_{EN}	V_{IN}=V_{EN}=6V		10		nA
Current Limit	Output Current Limit	I_{CL}	V_{IN}=2V,$V_{OUT(NOM)}$<1V, V_{OUT}=$V_{OUT(NOM)}$-0.2V; V_{IN}=$V_{OUT(NOM)}$+1V,$V_{OUT(NOM)}$≥1V, V_{OUT}= $V_{OUT(NOM)}$×0.85	500	790	1150	mA
	Short-Circuit Current Limit	I_{SC}	V_{IN}=2V,$V_{OUT(NOM)}$<1V,V_{OUT}=0V; V_{IN}=$V_{OUT(NOM)}$+1V,$V_{OUT(NOM)}$≥1V, V_{OUT}=0V	180	300	450	mA
Power Good	High Threshold	PG_{HTH}	V_{OUT} increasing	88	92	96	%V_{OUT}
	Low Threshold	PG_{LTH}	V_{OUT} decreasing	85	90	94	%V_{OUT}
	Hysteresis	PG_{HYST}			2		%V_{OUT}
	PG Pin Low-Level Output Voltage	$V_{OL(PG)}$	V_{IN}≥2.75V, I_{SINK}=2.0mA			300	mV
	Leakage Current	$I_{lkg(PG)}$	V_{OUT}>PG_{HTH}, V_{PG}=6V		7	50	nA
	PG Delay Time Rising	t_{PGDH}	Time from 92% V_{OUT} to 20% of PG	40	165	290	μs
	PG Delay Time Falling	t_{PGDL}	Time from 90% V_{OUT} to 80% of PG		7		μs

Electrical Characteristics (Cont.)

(V_{IN}=$V_{OUT(NOM)}$+0.5V or 1.62V (which is greater), I_{OUT}=1mA, V_{EN}=V_{IN}, C_{IN}=1μF, C_{OUT}=2.2μF, T_J = -40°C~125°C, unless otherwise specified, all typical values are at T_J=25°C (Note 4)).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dropout Voltage	$\triangle V_{DROP}$	I_{OUT}=500mA,V_{OUT}=0.95×$V_{OUT(NOM)}$, 1.5V≤ V_{OUT}<2V		220	340	mV
		I_{OUT}=500mA,V_{OUT}=0.95×$V_{OUT(NOM)}$, 2V≤ V_{OUT}<2.5V		160	250	mV
		I_{OUT}=500mA,V_{OUT}=0.95×$V_{OUT(NOM)}$, 2.5V≤ V_{OUT}<3.3V		120	210	mV
		I_{OUT}=500mA,V_{OUT}=0.95×$V_{OUT(NOM)}$, 3.3V≤ V_{OUT}≤5.5V		110	185	mV
Startup Time	t_{STR}	From EN low-to-high transition to V_{OUT}=$V_{OUT(NOM)}$×0.95	200	500	850	μs
Power Supply Rejection Ratio (Note 5)	PSRR	V_{IN}=2.8V,V_{OUT}=1.8V,I_{OUT}=500mA, f=1kHz		55		dB
		V_{IN}=2.8V,V_{OUT}=1.8V,I_{OUT}=500mA, f=100kHz		35		dB
		V_{IN}=2.8V,V_{OUT}=1.8V,I_{OUT}=500mA, f=1MHz		30		dB
Pull Down Resistance	$R_{PULLDOWN}$	V_{IN}=6V, V_{EN}=0V		95		Ω
Thermal Shutdown Temperature (Note 5)	T_{SD}			170		°C
Thermal Shutdown Reset (Note 5)	T_{Reset}			155		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Measured with natural convection at T_A = 25°C on a thermal conductivity test board with vias based on JEDEC 51-5, 7.

Note 3: The device is not guaranteed to function outside its operating conditions.

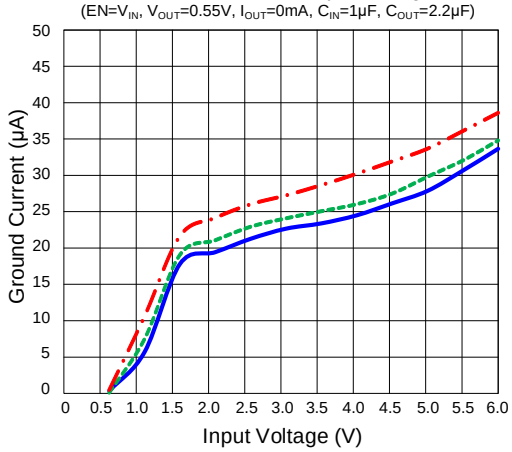
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$= 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

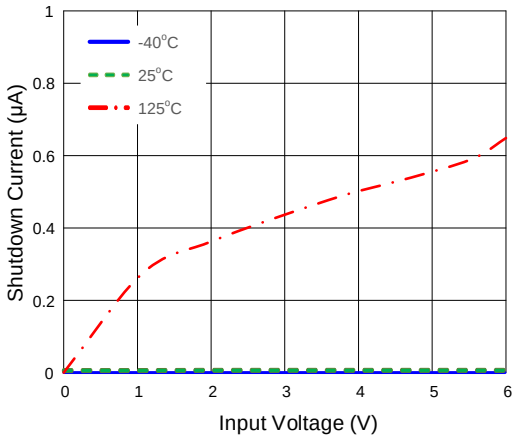
Note 6: Tolerances of the external feedback resistors are not considered.

Typical Performance Characteristics

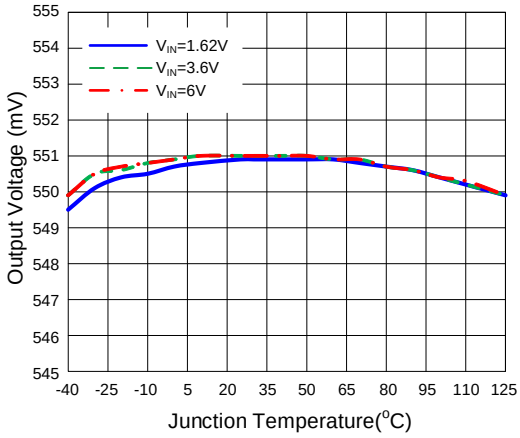
Ground Current vs. Input Voltage
(EN=V_{IN}, V_{OUT}=0.55V, I_{OUT}=0mA, C_{IN}=1μF, C_{OUT}=2.2μF)



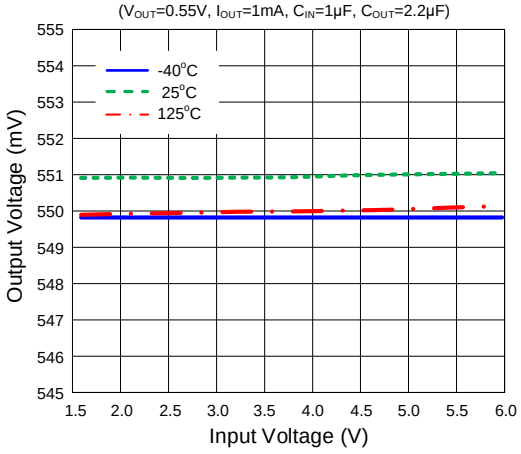
Shutdown Current vs. Input Voltage
(EN=0V, C_{IN}=1μF, C_{OUT}=2.2μF)



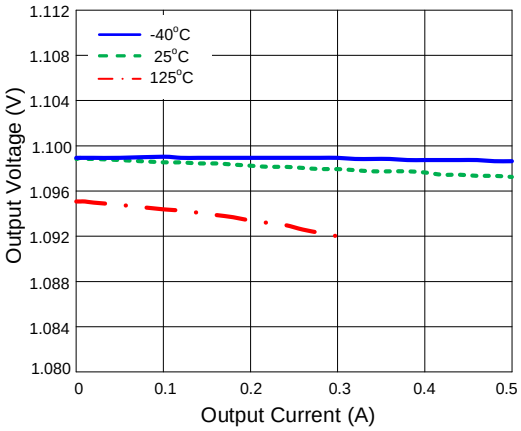
Output Voltage vs. Junction Temperature
(V_{OUT}=0.55V,I_{OUT}=1mA, C_{IN}=1μF, C_{OUT}=2.2μF)



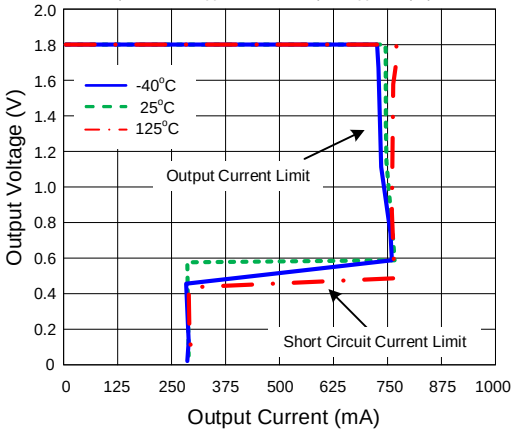
Output Voltage vs. Input Voltage
(V_{OUT}=0.55V, I_{OUT}=1mA, C_{IN}=1μF, C_{OUT}=2.2μF)



Output Voltage vs. Output Current
(V_{IN}=3.6V, V_{OUT}=1.1V, C_{IN}=1μF, C_{OUT}=2.2μF)

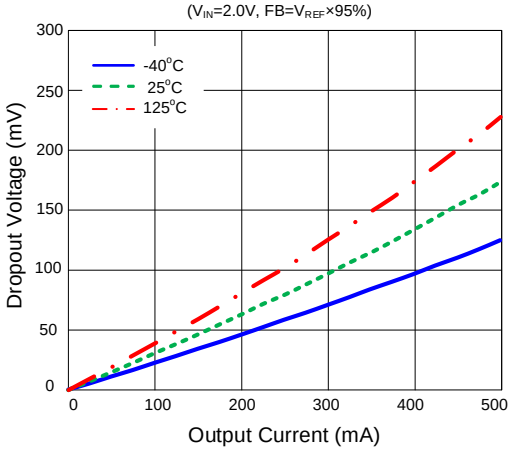


Output Voltage vs. Output Current
(V_{IN}=3.6V, V_{OUT}=1.8V, C_{IN}=1μF, C_{OUT}=2.2μF)



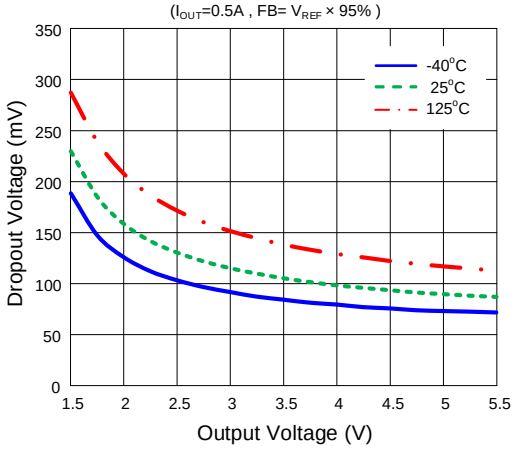
Dropout Voltage vs. Output Current

(V_{IN}=2.0V, FB=V_{REF}×95%)



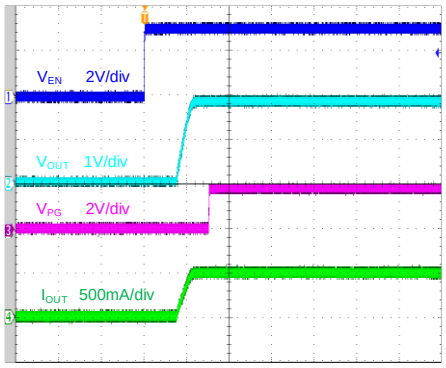
Dropout Voltage vs. Output Volatge

(I_{OUT}=0.5A , FB= V_{REF} × 95%)



Startup from Enable

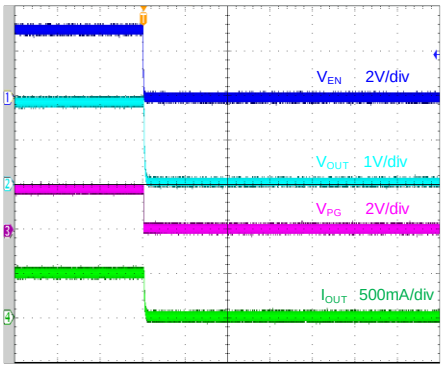
(V_{IN}=3.6V, V_{OUT}=1.8V, I_{OUT}=0.5A,C_{IN}=1μF, C_{OUT}=2.2μF)



Time (400μs/div)

Shutdown from Enable

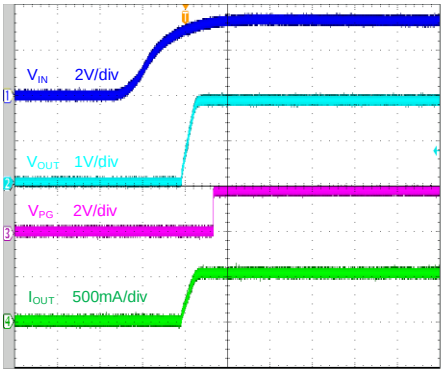
(V_{IN}=3.6V, V_{OUT}=1.8V, I_{OUT}=0.5A,C_{IN}=1μF, C_{OUT}=2.2μF)



Time (200μs/div)

Startup from V_{IN}

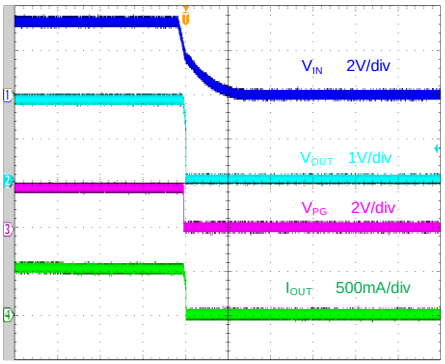
(V_{IN}=V_{EN}=3.6V, V_{OUT}=1.8V, I_{OUT}=0.5A, C_{IN}=1μF, C_{OUT}=2.2μF)



Time (400μs/div)

Shutdown from V_{IN}

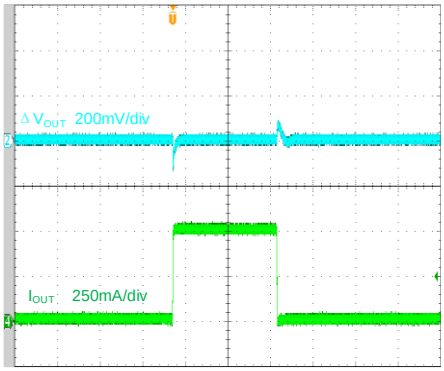
(V_{IN}=V_{EN}=3.6V, V_{OUT}=1.8V, I_{OUT}=0.5A, C_{IN}=1μF, C_{OUT}=2.2μF)



Time (10ms/div)

Load Transient

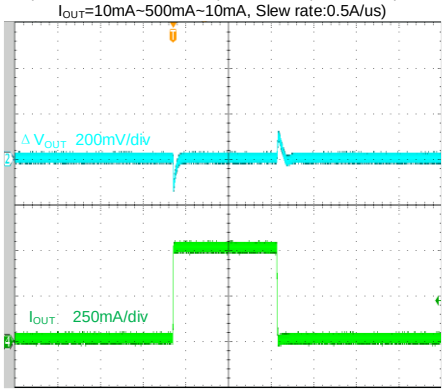
(V_{IN}=3.3V, V_{OUT}=1.8V, C_{IN}=1μF, C_{OUT}=2.2μF, C_{FF}=100pF, I_{OUT}=10mA~500mA~10mA, Slew rate:0.5A/us)



Time (100μs/div)

Load Transient

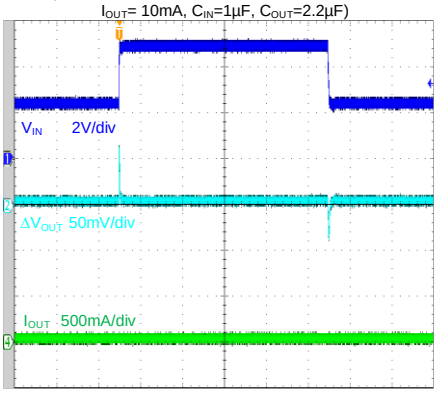
(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=1μF, C_{OUT}=2.2μF,C_{FF}=100pF, I_{OUT}=10mA~500mA~10mA, Slew rate:0.5A/us)



Time (100μs/div)

Line Transient

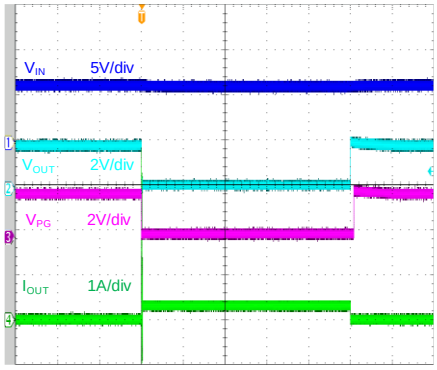
(V_{IN}=2.3V~5V~2.3V,Slew rate:1V/us, V_{OUT}=1.8V, I_{OUT}= 10mA, C_{IN}=1μF, C_{OUT}=2.2μF)



Time (500us/div)

Short Circuit Protection

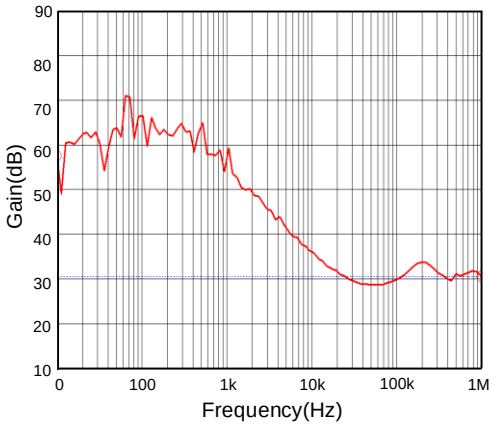
(V_{IN}=6V,V_{OUT}=1.8V, C_{IN}=1μF, C_{OUT}=2.2μF, I_{OUT}=Null~ Short Circuit~ Null)



Time (2ms/div)

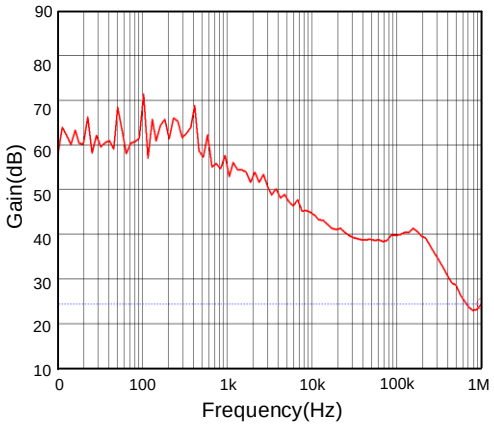
PSRR

(V_{IN}=2.8V, V_{OUT}=1.8V, I_{OUT}=500mA, C_{OUT}=2.2μF)



PSRR

(V_{IN}=2.8V, V_{OUT}=1.8V, I_{OUT}=500mA, C_{OUT}=2.2μF, C_{FF}=1nF)



Detailed Description

General Features

Input Under Voltage Lock-Out (UVLO)

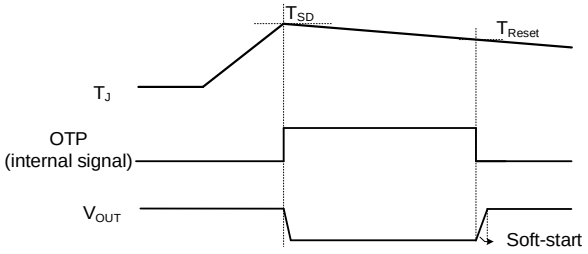
To prevent operation before all internal circuitry is ready, the device remains in a shutdown state until VIN exceeds the UVLO (rising) threshold. Once this threshold is met and EN is active, the device initiates a soft-start ramp. If V_{IN} subsequently falls below the UVLO falling threshold (defined as $V_{IN,\ UVLO}$ minus the UVLO hysteresis) the device shuts down again.

Enable Function (EN)

The enable pin for the SA21308A is active high. The output voltage is enabled when the enable pin voltage exceeds $V_{EN(HI)}$ and disabled when the enable pin voltage falls below $V_{EN(LO)}$. If independent control of the output voltage is not required, connect the enable pin to the input.

Over-Temperature Protection (OTP)

The SA21308A includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will turn off the device when the junction temperature exceeds 170°C. Once the junction temperature cools down by approximately 15°C the device will resume normal operation.



Over-Current Limit and Short-Circuit Protection (OCL&SCP)

The device includes over current limiting and output short-circuit protection. The current limitation circuit regulates the output current to its limitation threshold (I_{CL}) to prevent device damage. If V_{OUT} drops below approximately 40% of the OUT set point, the short-circuit protection reduces the output current to the fold-back short-circuit current limit (I_{SC}) to further decrease the power dissipation. Under over current or short-circuit conditions, the power loss of the device is relatively high, potentially triggering thermal protection.

Power Good Function (PG)

The device features an open-drain PG output that goes to high-impedance when the feedback voltage (V_{FB}) exceeds the power good high threshold (PG_{HTH}). Conversely, PG is pulled low when the V_{FB} drops below the power good low threshold (PG_{LTH}). PG is an open-drain output, requiring a pull-up resistor (typically between 10 kΩ and 100 kΩ) connected to a stable active supply voltage rail. Additionally, PG is pulled low if the device encounters other fault conditions such as OTP and UVLO.

Input Capacitor C_{IN}

For normal operation, it is recommended to place a 1μF low-ESR ceramic capacitor (X7R grade or better) close to the IN and GND pins. Using a larger input ceramic capacitor can help improve noise immunity as well as improve power-supply rejection ratio (PSRR) and transient response. Care should be taken to minimize the loop area formed by C_{IN} and the IN/GND pins.

Output Capacitor C_{OUT}

For stable operation across the entire temperature range, a minimum of 2.2μF low-ESR ceramic capacitor is recommended. Use larger output capacitor values such as 10μF to reduce noise, improve load-transient response and enhance PSRR. Some ceramic dielectrics exhibit significant variations in capacitance and equivalent series resistance (ESR) with temperature.

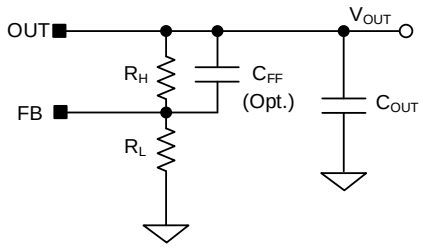
Feedback Resistor Dividers R_H and R_L

Select resistors R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, choose large resistance values (between 1kΩ and 1MΩ) for both resistors. For example, if V_{OUT} is 1.8V, and R_H is chosen to be 100kΩ, then R_L can be calculated using the following equation to be 44 kΩ:

$$R_L = \frac{0.55V}{V_{OUT} - 0.55V} \times R_H$$

Feedforward Capacitor (C_{FF})

The SA21308A integrates compensation components to achieve good stability and transient response. In some applications, adding a small ceramic capacitor (with a typical value between 10 pF and 1 nF) in parallel with R_H may further enhance the load transient response, therefore, it is recommended for applications with significant load transient step requirements.



Dropout Voltage

The SA21308A features a very low dropout voltage attributed to the extra low $R_{DS(ON)}$ of the main PMOS, which determines the minimum usable supply voltage. $V_{DROPOUT}=V_{IN}-V_{OUT}=R_{DS(ON)}\times I_{OUT}$.

Thermal Design Considerations

The SA21308A can deliver a current of up to 500mA over the full operating temperature range. However, the maximum output current must be derated when operating at a higher ambient temperature. Across all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across the regulator.

$P_D=(V_{IN}-V_{OUT})\times I_{OUT}+V_{IN}\times I_{GND}$

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by the following thermal equation:

$P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

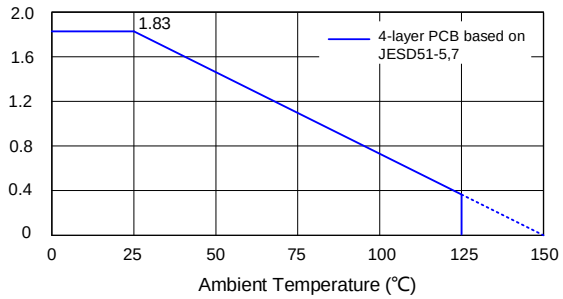
To comply with the recommended operating conditions, the maximum junction temperature is 150°C, and the junction to ambient thermal resistance θ_{JA} is layout dependent. For the DFN2×2-6 package, the thermal resistance θ_{JA} is 68.0°C/W when measured on a four-layer thermal test board with thermal vias based on JESD51-5, 7.

The maximum power dissipation at T_A=25°C may be calculated by the following formula:

$P_{D(MAX)}$ = (150°C − 25°C) / (68.0°C)/W) = 1.83W

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. Use the derating curve in the figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

Maximum Power Derating Curve



Layout Design

For optimal performance of the SA21308A, the following guidelines must be strictly followed:

1. Place the input/output capacitors as close to the device as possible, minimizing the loop formed by these connections to improve transient performance.
2. Keep all power traces as short and wide as possible. The exposed pad should be connected to a large ground copper area and include multiple GND vias to the GND plane for efficient heat dissipation and noise reduction.
3. A 2-layer or 4-layer board is recommended for thermal performance and better current-handling capability.

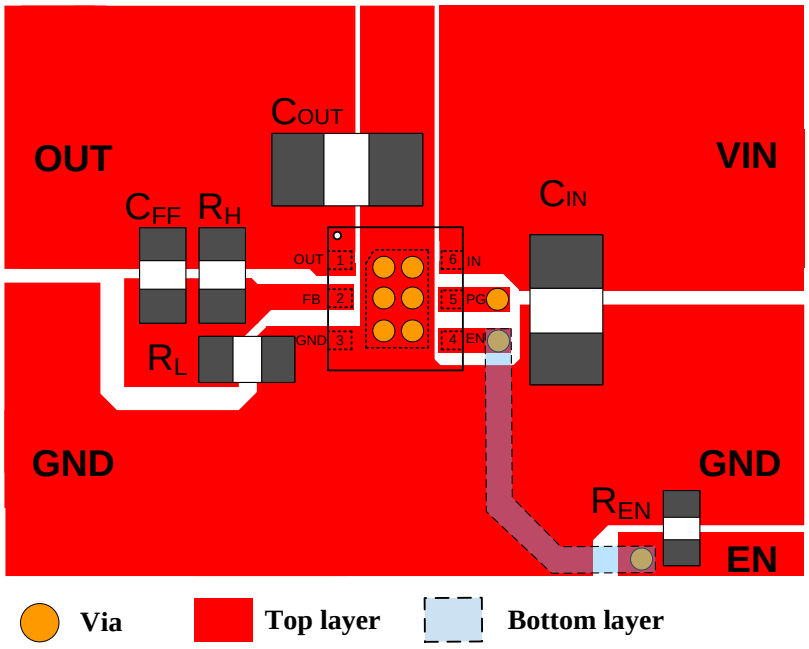
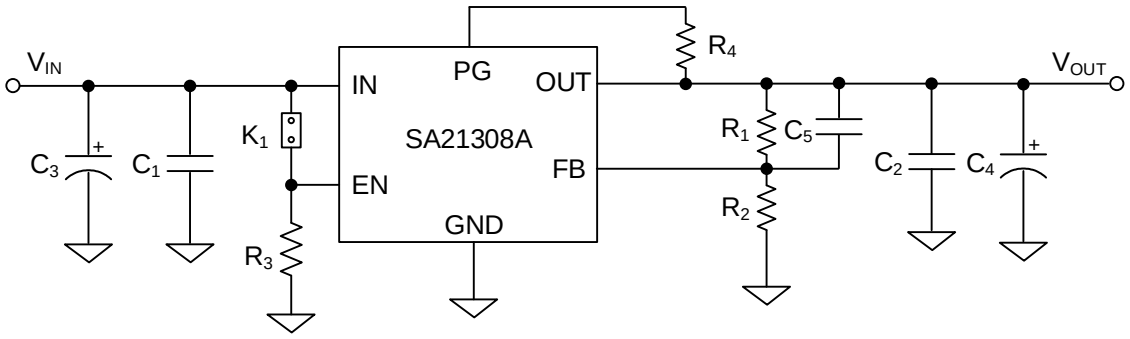


Figure 3. PCB Layout Suggestion

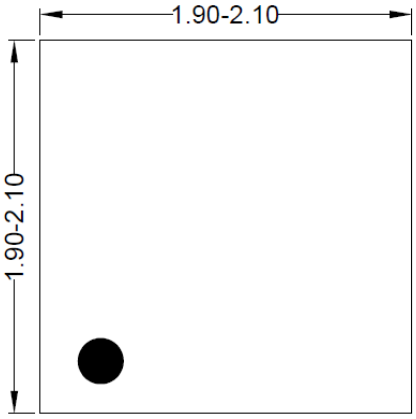
Schematic



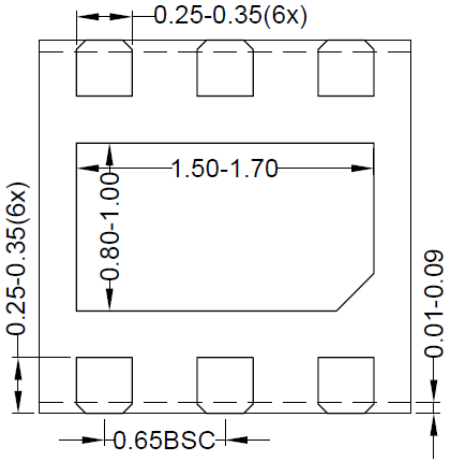
BOM List

Designator	Description	Part Number	Manufacturer
C_1	1μF/25V/X7R,0805	GRM21BR71E105K	muRata
C_2	2.2μF/25V/X7R,0805	GRM21BR71E225K	muRata
C_3, C_4	NC		
C_5	100pF/50V/C0G,0603	GRM1885C1H101J	muRata
R_1	100kΩ, 0603, 1%		
R_2	44.2kΩ, 0603, 1%		
R_3	1MΩ, 0603, 1%		
R_4	100kΩ, 0603, 1%		

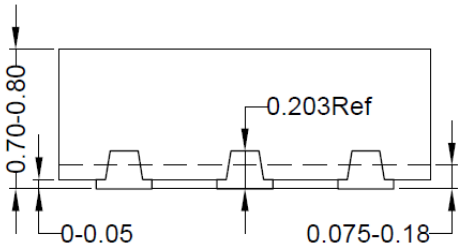
DFN2×2-6 Package Outline



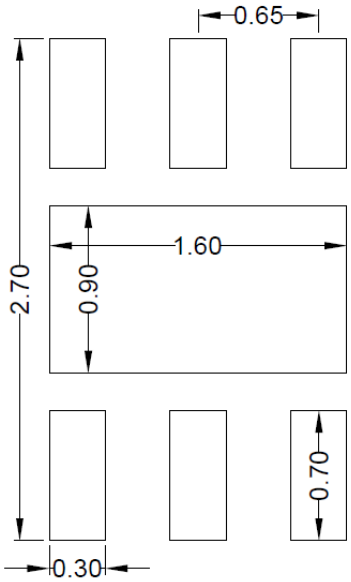
Top View



Bottom View



Front View



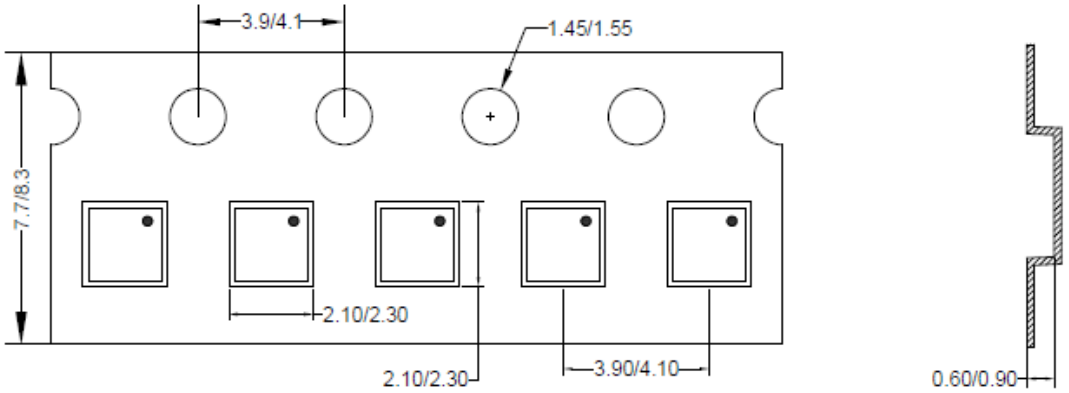
Recommended PCB Layout
(Reference only)

Notes: *All dimension in millimeter and exclude mold flash & metal burr.*

Tape and Reel Information

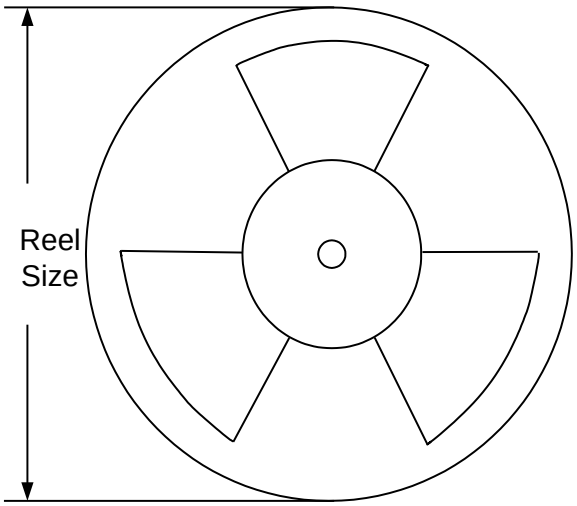
1. Tape Dimensions and Pin1 Orientation

DFN2×2



Feed Direction ⟶

2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2×2	8	4	7	280	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Sep. 24, 2025	Revision 1.0	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com