# SA21340PFCP

## 36V 300mA LDO with Programmable Reset

## General Description

The SA21340PFCP is an automotive grade, 300mA high-current capacity linear regulator with ultra-low ground current and low drop-out voltage. The SA21340PFCP has a fixed 3.3V output voltage. The device offers protective features, including an over-current limit, output short protection, and over-temperature operation.

The SA21340PFCP is available in a compact SO8E package.

## Applications

- Industrial/Automotive Application
- Portable/Battery-Powered Equipment
- Gateway Application
- Remote Keyless Entry Systems
- Cellular Handsets
- SMPS Post-regulator/ DC-DC Modules
- Medical Imaging

## Features

- Wide Input Range: 4V to 36V
- Fixed 3.3V Output Voltage
- Output Voltage Accuracy: 2%
- Low Drop-out Voltage of 300mV at Full Load 300mA
- 300mA Maximum Load Current
- Ultra-low Quiescent Current
- Extremely Low Shutdown Current
- Stability with Tantalum or Ceramic Capacitors
- Excellent Load and Line Regulation
- Enable Control Input
- Over Current Limit Protection
- Output Short Circuit Protection (Hiccup Mode)
- Over Temperature Protection
- Thermal Shutdown
- RoHS Compliant and Halogen Free
- Package: SO8E
- Automotive AEC- Q100 Grade 1 Qualified

## Typical Application

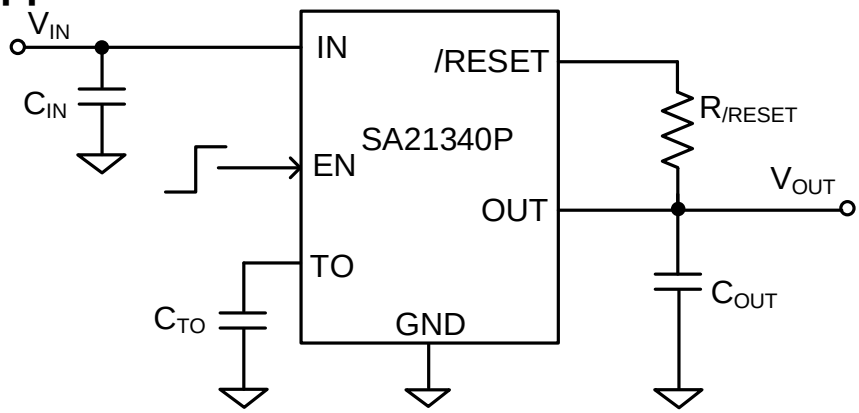


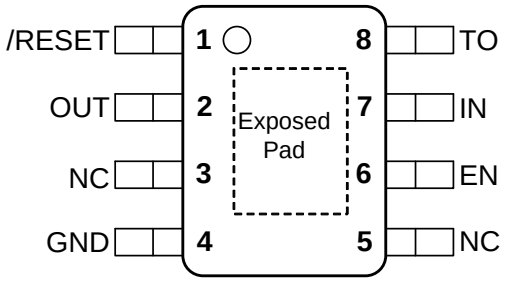

*Figure1. Schematic Diagram*

## Ordering Information

| Ordering Part Number | Package Type | Top Mark |
|---|---|---|
| SA21340PFCP | SO8E<br>RoHS Compliant and Halogen Free | **GMY*xyz*** |

***x=year code, y=week code, z= lot number code***

## Pinout (top view)




| Pin Name | Pin number | Pin Description |
|---|---|---|
| /RESET | 1 | Open drain reset output. /RESET low when OUT is below the reset threshold and remains low for the reset timeout period after the reset conditions end. If no capacitor connects at the TO pin, RESET pulls high immediately after $V_{OUT}$ exceeds the reset threshold. if it is not used, leave it floating or connect to GND. |
| OUT | 2 | Output pin, decoupled with a 4.7μF MLCC capacitor to GND. |
| NC | 3, 5 | No connection. |
| GND | 4 | Ground pin. |
| EN | 6 | Enable pin. Pull high to enable the chip. Do not leave it floating. |
| IN | 7 | Input pin, decoupled with at least 10μF MLCC capacitor to GND. |
| TO | 8 | Reset timeout programming pin. Connect a capacitor from this pin to GND for different reset timeout time. |
| Exposed Pad | / | The exposed pad should be connected to the ground plane for better thermal performance. |

## Block Diagram

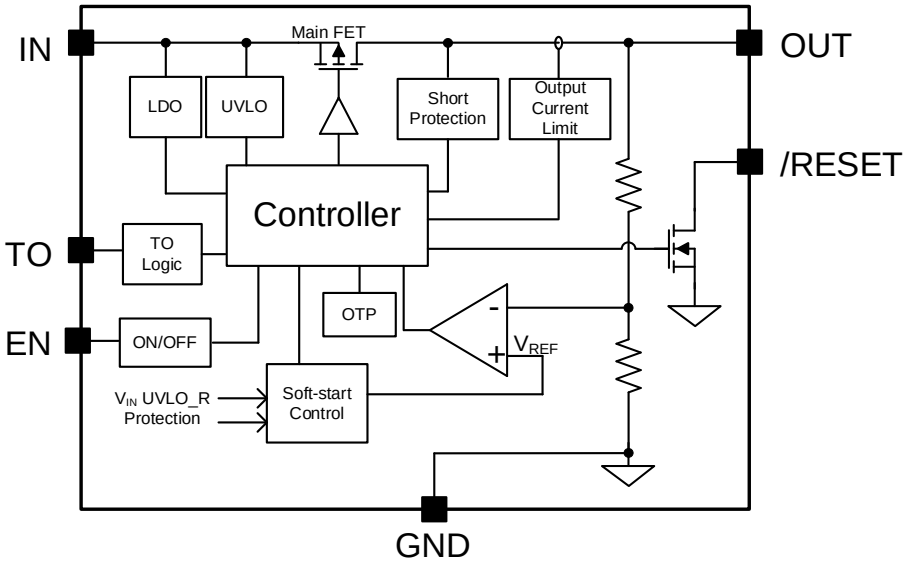



*Figure2. Block Diagram*

## Absolute Maximum Ratings

| Parameter (Note 1) | Min | Max | Unit |
|---|---|---|---|
| IN, EN, OUT, /RESET to GND | -0.3 | 40 | V |
| TO | -0.3 | 3.6 | |
| Lead Temperature (Soldering, 10 sec.) | | 260 | °C |
| Junction Temperature, Operating | -40 | 150 | |
| Storage Temperature | -65 | 150 | |

## Thermal Information

| Parameter (Note 2) | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ Junction-to-ambient Thermal Resistance | 38.3 | °C/W |
| $\theta_{JC}$ Junction-to-case Thermal Resistance | 12.6 | |
| $P_D$ Power Dissipation $T_A$=25°C | 2.6 | W |

## ESD Susceptibility

| Parameter | Min | Max | Unit |
|---|---|---|---|
| HBM (Human Body Mode) | | 2000 | V |
| CDM (Charged Device Mode) | | 500 | V |

## Recommended Operating Conditions

| Parameter (Note 3) | Min | Max | Unit |
|---|---|---|---|
| IN | 4 | 36 | V |
| EN, OUT, /RESET | 0 | 36 | |
| TO | 0 | 3.3 | |
| Ambient Temperature | -40 | 125 | °C |

# Electrical Characteristics

($V_{IN}$=$V_{EN}$=12V, $T_J$=-40°C~125°C, unless otherwise specified, the values are guaranteed by test, design or statistical correlation.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | | 4 | | 36 | V |
| Input Voltage UVLO Threshold | $V_{UVLO}$ | $V_{IN}$ rising | 2.9 | 3.3 | 4 | V |
| UVLO Hysteresis | $V_{UVLO\_HYS}$ | | | 200 | | mV |
| Output Voltage | $V_{OUT}$ | $T_J$ = -40°C~125°C | 3.234 | 3.3 | 3.366 | V |
| | | $T_J$ = 25°C | 3.267 | 3.3 | 3.333 | V |
| Line Regulation | $\Delta V_{LNR}$ | $I_{OUT}$ = 10mA, 4V≤ $V_{IN}$ ≤ 36V | | 1 | 1.5 | mV/V |
| Load Regulation | $\Delta V_{LDR}$ | $V_{IN}$=5V, 10mA ≤ $I_{OUT}$ ≤ 0.3A | | 0.25 | 0.5 | % |
| Dropout Voltage | $\Delta V_{DROP}$ | $I_{OUT}$=10mA | | 10 | 20 | mV |
| | | $I_{OUT}$=300mA | | 300 | 540 | mV |
| Quiescent Current | $I_Q$ | $I_{OUT}$=0mA<br>$V_{IN}$=($V_{OUT}$+1V) ~ 36V | | 15 | 22 | μA |
| Shutdown Current | $I_{SHDN}$ | $V_{EN}$=0V, $V_{IN}$=24V | | | 5 | μA |
| Current Limit | $I_{LIMIT}$ | Force $V_{OUT}$ = 3V | 600 | 900 | 1200 | mA |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Short Protection Threshold | $V_{SHORT}$ | Force $V_{OUT}$ from 3.3V to 0V | 0.264 | 0.528 | 0.99 | V |
| Output Short Off Time | $t_{SHORT, OFF}$ | | | 16 | | ms |
| Power Supply Rejection Ratio (Note 4) | PSRR | Frequency = 100Hz, $C_{OUT}$=4.7μF, $I_{OUT}$=10mA, $T_A$=25°C | | 60 | | dB |
| | | Frequency = 100kHz, $C_{OUT}$=4.7μF, $I_{OUT}$=10mA, $T_A$=25°C | | 35 | | dB |
| Enable Input Logic-High Voltage | $V_{EN, H}$ | | 1.5 | | | V |
| Enable Input Logic-Low Voltage | $V_{EN, L}$ | | | | 0.4 | V |
| Soft-start Time | $t_{SS}$ | | | 1 | | ms |
| $V_{TO}$ /REST High-level Threshold | $V_{TR}$ | $V_{TO}$ rising | 1.4 | 1.8 | 2.2 | V |
| TO Default Rise Up Time | $t_{TO,Rise}$ | OUT High, TO Floating, rising from 0 to $V_{TR}$ | | 1.6 | | us |
| TO Charge Current | $I_{TR}$ | | 8 | 16 | 24 | uA |
| VOUT /RESET Threshold | $V_{OR}$ | OUT rising | 85 | 90 | 95 | %$V_{OUT}$ |
| VOUT /RESET Threshold Hysteresis | $V_{OR,HYS}$ | OUT falling | | 5 | | %$V_{OUT}$ |
| /RESET Output-Voltage Low | | | | | 0.4 | V |
| Thermal Shutdown Temperature (Note 4) | $T_{SD}$ | | | 170 | | °C |
| Thermal Shutdown Hysteresis (Note 4) | $T_{HYS}$ | | | 20 | | °C |

**Note 1**: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

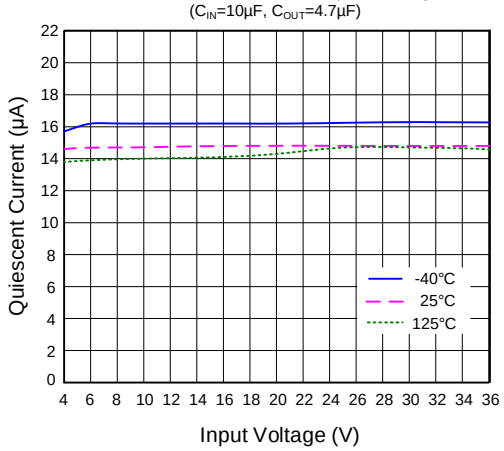
**Note 2**: $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

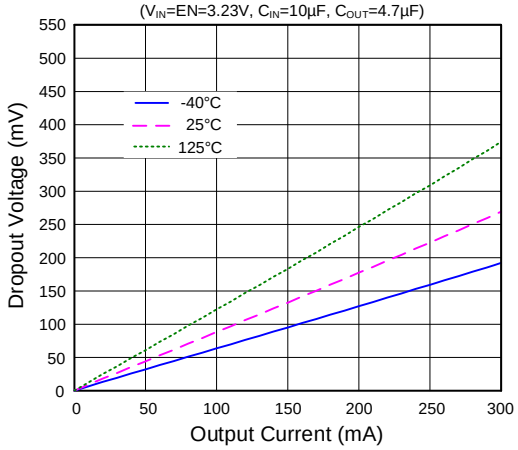
**Note 4:** Guaranteed by design.

# Typical Performance Characteristics

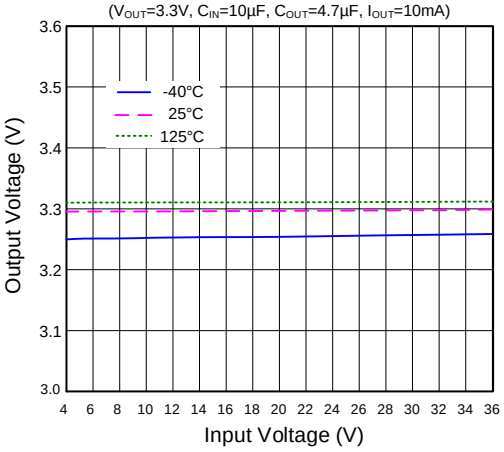
Quiescent Current vs. Input Voltage
($C_{IN}$=10μF, $C_{OUT}$=4.7μF)



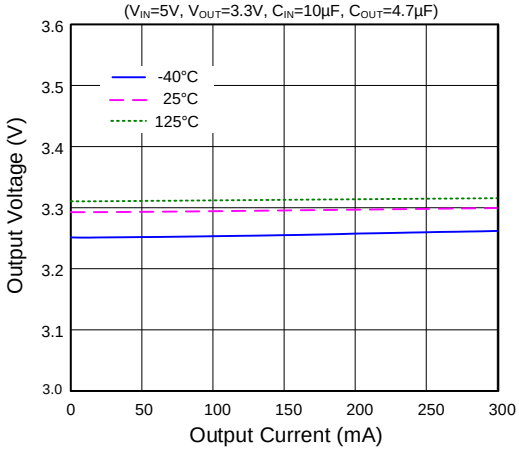

Dropout Voltage vs. Output Current
($V_{IN}$=EN=3.23V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF)



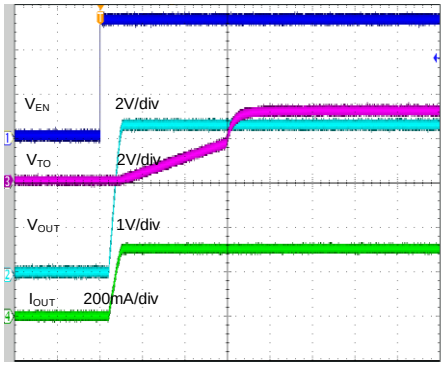

Output Voltage vs. Input Voltage
($V_{OUT}$=3.3V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF, $I_{OUT}$=10mA)




Output Voltage vs. Output Current
($V_{IN}$=5V, $V_{OUT}$=3.3V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF)

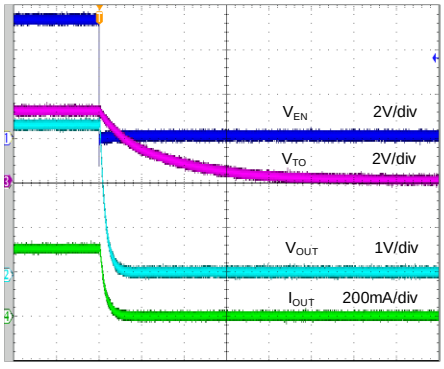



Startup from Enable
($V_{IN}$=5V, $V_{OUT}$=3.3V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF, $I_{OUT}$=300mA)




Time (4ms/div)

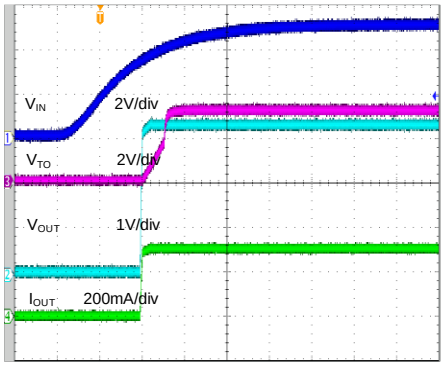
Shutdown from Enable
($V_{IN}$=5V, $V_{OUT}$=3.3V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF, $I_{OUT}$=300mA)




Time (200μs/div)

Startup from $V_{IN}$

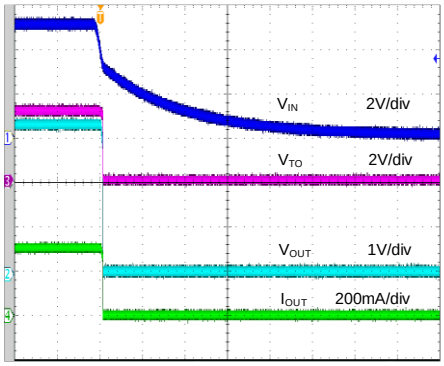
($V_{IN}$=5V, $V_{OUT}$=3.3V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF, $I_{OUT}$=300mA)




Time (20ms/div)

Shutdown from $V_{IN}$

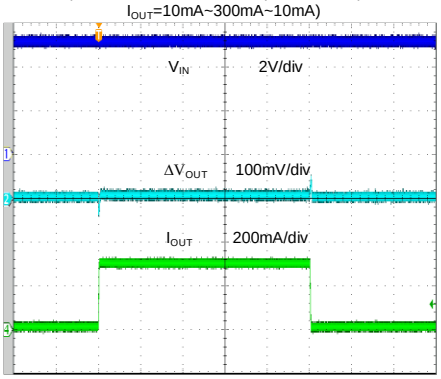
($V_{IN}$=5V, $V_{OUT}$=3.3V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF, $I_{OUT}$=300mA)




Time (100ms/div)

Load Transient

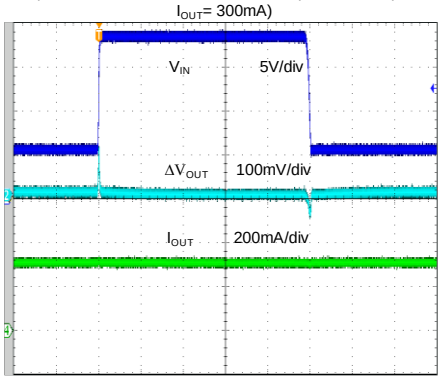
($V_{IN}$=5V, $V_{OUT}$=3.3V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF, $I_{OUT}$=10mA~300mA~10mA)




Time (1ms/div)

Line Transient

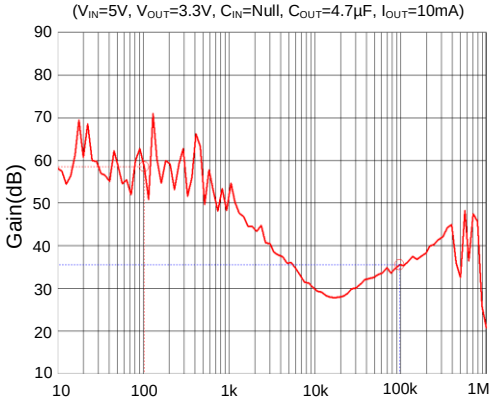
($V_{IN}$=5V~18V~5V, $V_{OUT}$=3.3V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF, $I_{OUT}$= 300mA)




Time (2ms/div)

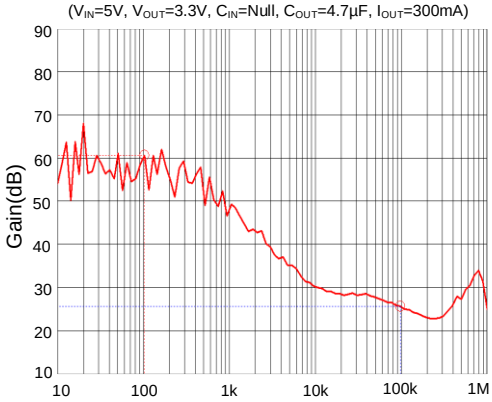
PSRR

($V_{IN}$=5V, $V_{OUT}$=3.3V, $C_{IN}$=Null, $C_{OUT}$=4.7μF, $I_{OUT}$=10mA)



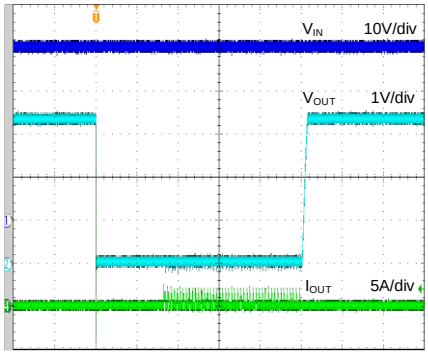

PSRR

($V_{IN}$=5V, $V_{OUT}$=3.3V, $C_{IN}$=Null, $C_{OUT}$=4.7μF, $I_{OUT}$=300mA)



Short Protection

($V_{IN}$=36V,$V_{OUT}$=3.3V, $C_{IN}$=10μF, $C_{OUT}$=4.7μF,
$I_{OUT}$=Null~ Short Circuit~ Null)




Time (10ms/div)

# Applications Information

The SA21340PFCP is a 300mA high-current capacity linear regulator with ultra-low ground current and low drop out voltage. The SA21340PFCP has a fixed 3.3V output voltage. The device offers protection features, including an over-current limit, output short protection and over-temperature operation.

## Over Temperature Protection (OTP)

The SA21340PFCP includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will turn off the device when the junction temperature exceeds 170°C. Once the junction temperature cools down by approximately 20°C the IC will resume normal operation.

## Output Short Circuit Protect

If $V_{OUT}$ drops below 16% of the OUT set point, the short circuit protection mode will be initiated, and the device will be shut down for approximately 16ms. The device will then restart with a complete soft-start cycle. If the short circuit condition remains, another 'hiccup' cycle of shutdown and restart will continue indefinitely unless the OTP threshold is reached.

## /RESET Function

The SA21340PFCP includes an open-drain reset output. Once the output voltage exceeds the reset threshold voltage (90% of the OUT set point), the $C_{TO}$ is charged with the current $I_{TR}$, the /RESET will be high when the voltage on $C_{TO}$ is larger than $V_{TR}$. If the output voltage is lower than the reset threshold voltage, the device discharges $C_{TO}$ fast and the /RESET pin is driven to low when the voltage on TO is lower than $V_{TF}$.

## Timeout

The SA21340PFCP features an adjustable reset timeout period. The internal capacitance produces a 1.6μs default delay when the TO pin is floating. Connect a capacitor from TO to GND to set a higher timeout period than the default value. Use the following formula to determine the reset timeout capacitor:

$$C_{TO} = \frac{16\mu A \times t_{TIMEOUT}}{1.8V}$$

## Input Capacitor $C_{IN}$ and Output Capacitor $C_{OUT}$

To minimize the potential noise problem and improve power-supply rejection ratio (PSRR) and transient response, place a typical X7R or better grade ceramic capacitor close to the IN and GND pins. Care should be taken to minimize the loop area formed by $C_{IN}$, and the IN/GND pins. A 10μF low ESR ceramic capacitor is recommended for most applications.

For stable operation over the full temperature range, a 4.7μF low-ESR ceramic capacitor is recommended. Use larger output-capacitor values such as 22μF to reduce noise, improve load-transient response and PSRR. Some ceramic dielectrics exhibit large capacitance and ESR variations with temperature.

## Thermal Considerations

The SA21340PFCP can deliver a current of up to 300mA over the full operating temperature range. However, the maximum output current must be derated at higher ambient temperature. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$P_D=(V_{IN}-V_{OUT})\times I_{OUT}+V_{IN}\times I_{GND}$

The final operating junction temperature for any set of condition can be estimated by the following thermal equation:

$P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature of die and $T_A$ is the maximum ambient temperature. The junction to ambient thermal resistance ($\theta_{JA}$) footprint is 38.2°C/W for SO8E package.

## PCB Layout Guide

For the best performance of the SA21340PFCP, the following guidelines must be strictly followed:

1. Keep all power trace as short and wide as possible. And it is desirable to use 2-layer or 4-layer board for thermal performance and better capability of current flow. At least 6 vias are suggested to put around each

power pin to distribute current to different PCB layer. These power pins include IN and OUT.

2. Place input/output capacitor close to the IC for better transient performance.

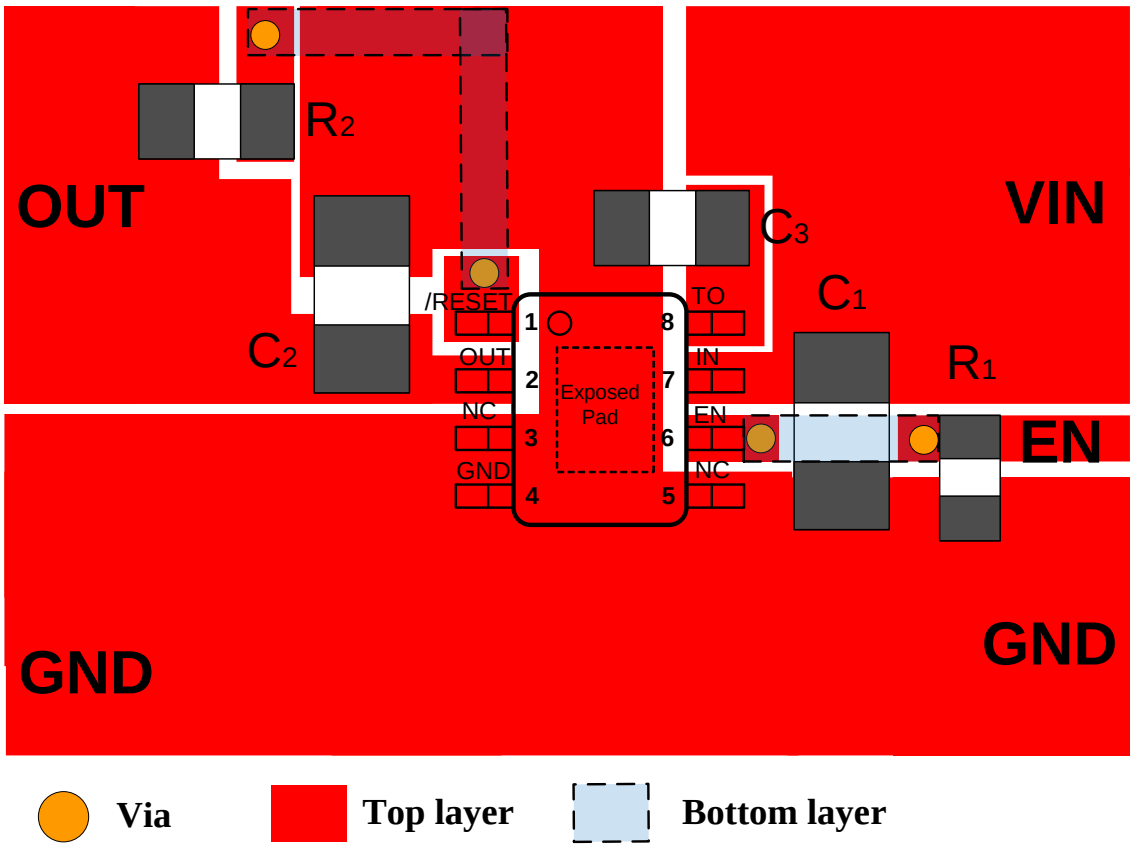
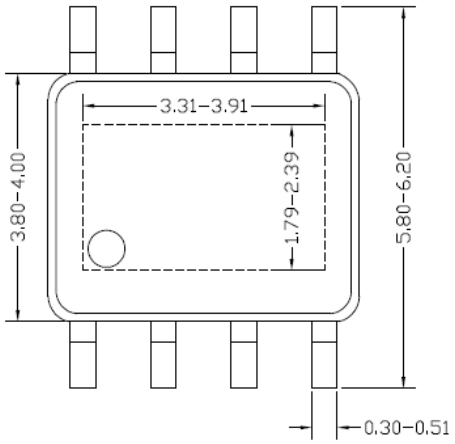
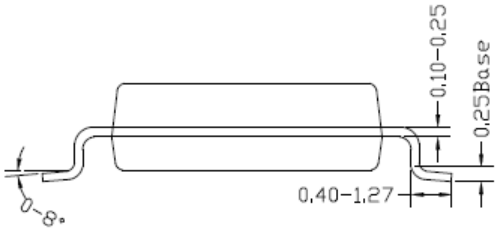



*Figure3. PCB Layout Suggestion*

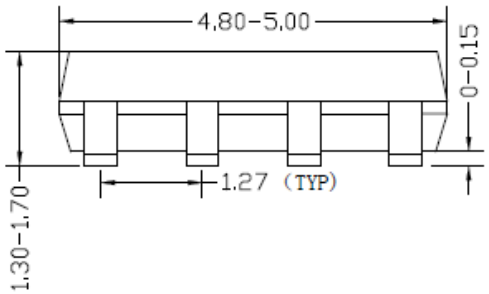
# SO8E Package Outline & PCB Layout



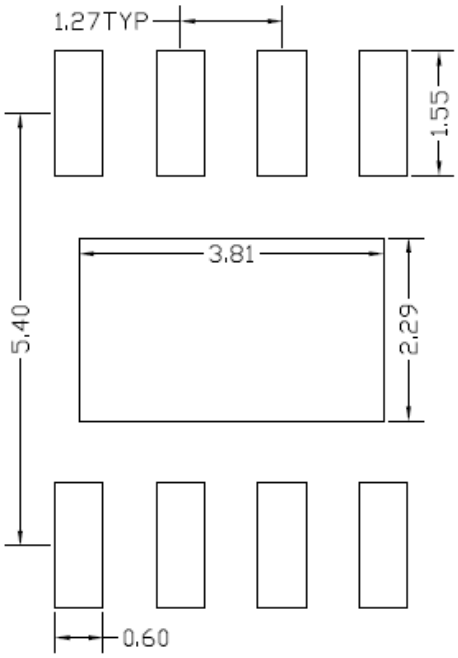

Top view




Side view




Front view



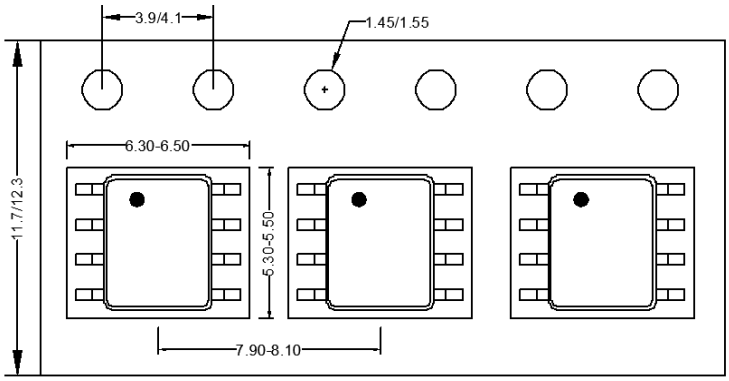

Recommended PCB Layout
(Reference Only)

***Notes:*** ***All dimension in millimeter and exclude mold flash & metal burr.***

# Taping & Reel Specification

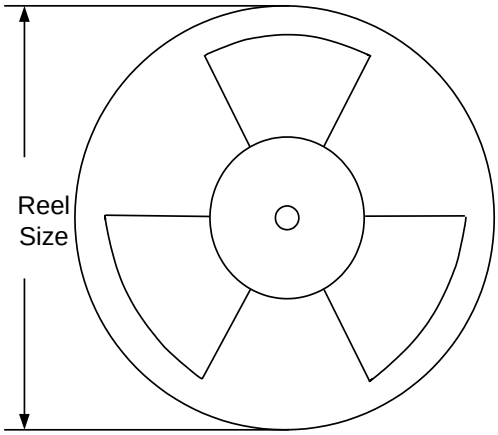
## 1. Taping orientation

**SO8E**




**Feeding direction** ⟶

## 2. Carrier Tape & Reel specification for packages




| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer * length(mm) | Leader * length (mm) | Qty per reel (pcs) |
|---|---|---|---|---|---|---|
| SO8E | 12 | 8 | 13" | 400 | 400 | 2500 |

**Others: NA**

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| Oct.25, 2024 | Revision 1.0 | Initial Production Release |
| Oct.25, 2023 | Revision 0.9 | Initial Release |

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