

General Description

The SA21345CDFD is an automotive grade, efficient, precise low-dropout voltage regulator designed for high input voltage and ultra-low quiescent current applications.

The SA21345CDFD provides adjustable output voltage and very low drop out (300mV at 300mA). It offers protection features including over-current protection, thermal shutdown, and stable operation with low ESR ceramic or tantalum capacitors due to the optimized internal compensation.

The SA21345CDFD is available in a compact DFN2×2-8 package.

Features

- Wide Input Voltage Range: 4V to 36V
- 300mA Maximum Load Current
- Low Dropout Voltage of (300mV @ 300mA)
- Low Quiescent Current (10μA typ.)
- Low Shutdown Current (6μA max.)
- Stability with Tantalum or Ceramic Capacitors
- Excellent Load and Line Regulation
- Enable Control Input
- Over Current Protection
- Thermal Shutdown
- Package: DFN2×2-8
- Automotive AEC- Q100 Grade 1 Qualified

Applications

- Automotive Applications
- Battery-Powered Equipment
- Gateway Applications
- Remote Keyless Entry Systems
- SMPS Post-regulator/ DC-DC Modules

Typical Application

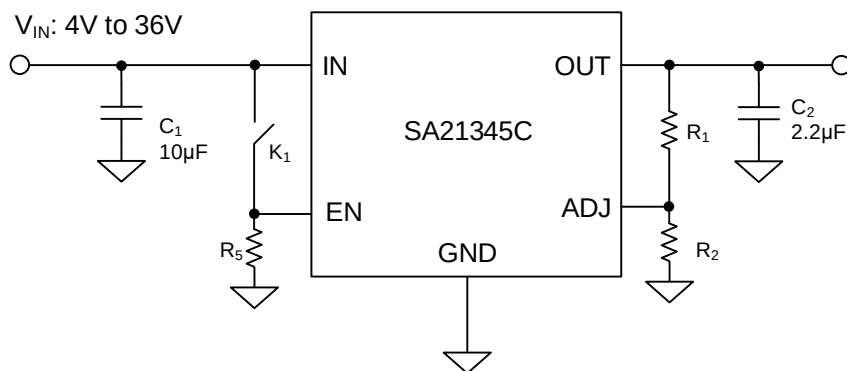


Figure1. Schematic Diagram

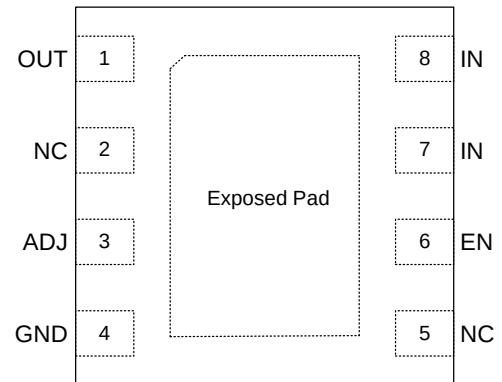
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA21345CDFD	DFN2×2-8 RoHS Compliant and Halogen Free	GTHxyz

Device code: GTH

x=year code, y=week code, z=lot number code

Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
OUT	1	Output pin. Bypass this pin to the ground pin with a 2.2μF output capacitor.
NC	2,5	Not connected.
ADJ	3	Output voltage adjust pin. Feedback the output voltage through resistor voltage divider network. $V_{OUT}=0.6 \times (1+R_1/R_2)$
GND	4	Ground pin.
EN	6	Enable pin. Pull it low to shut down or pull it high to enable, do not leave floating.
IN	7,8	Power supply input. Bypass this pin to the Ground pin with a 10μF capacitor.
Exposed Pad		The exposed pad should be connected to the ground plane for better thermal performance.

Block Diagram

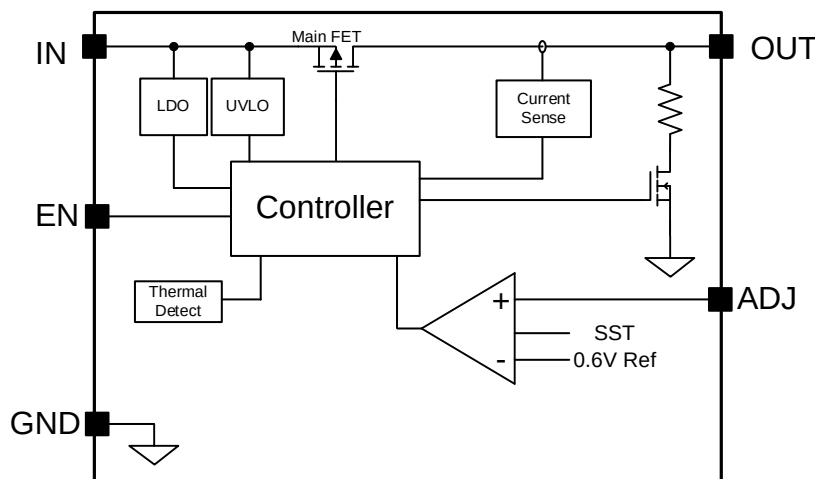


Figure2. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN to GND	-0.3	40	V
OUT, EN, ADJ to GND	-0.3	min (0.3V+V _{IN} , 40V)	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ _{JA} Junction-to-ambient Thermal Resistance	57	°C/W
θ _{JC} Junction-to-case Thermal Resistance	26	
P _D Power Dissipation T _A =25°C	1.754	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
IN	4	36	V
Ambient Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} =12V V_{OUT}=3.3V, V_{EN}=V_{IN} T_J = -40°C~125°C, unless otherwise specified (Note 4))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V _{IN}	I _{OUT} =10mA	4		36	V
Reference Voltage	V _{REF}		588	600	612	mV
Input Voltage UVLO Threshold	V _{ULVO}	V _{IN} rising	2.9	3.4	4	V
UVLO Hysteresis	V _{UVLO_HYS}			0.1		V
Line Regulation	ΔV _{LNR}	V _{IN} =(V _{OUT} +0.3V) to 36V, I _O =10mA		1	1.5	mV/V
Load Regulation	ΔV _{LDR}	V _{IN} =5V, I _O =10mA to 300mA		0.25	0.5	%
Dropout Voltage	ΔV _{DROP}	I _O =10mA		10	20	mV
		I _O =150mA		150	300	mV
		I _O =300mA		300	550	mV
Quiescent Current	I _Q	No Load		10	17	μA
Shutdown Current	I _{SHDN}	V _{EN} =0V, V _{IN} =24V			6	μA
Output Current	I _O	V _{IN} =V _{OUT} +0.6V	0		300	mA
Output Current Limit	I _{LIM}	V _{IN} =6V, V _{OUT} =0.9×V _{OUT} (normal)	300		900	mA
Output Short Protection Threshold	V _{ADJ,SHORT}	V _{FB} Falling	8	16	30	%V _{REF}
Power Supply Rejection Ratio (Note 5)	PSRR	f=1kHz, C _{OUT} =10μF		60		dB
		f=150kHz, C _{OUT} =10μF		30		dB
Enable Input Logic-High Voltage	V _{EN_H}	V _{IN} =5V	1.5			V
Enable Input Logic-Low Voltage	V _{EN_L}	V _{IN} =5V			0.4	V
Shutdown Discharge Resistance	R _{DIS}			600		Ω
Thermal Shutdown Temperature(Note 5)	T _{SD}			150		°C



SA21345CDFD

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown Hysteresis(Note 5)	T _{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

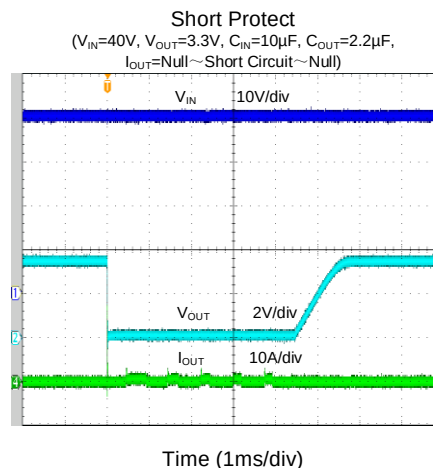
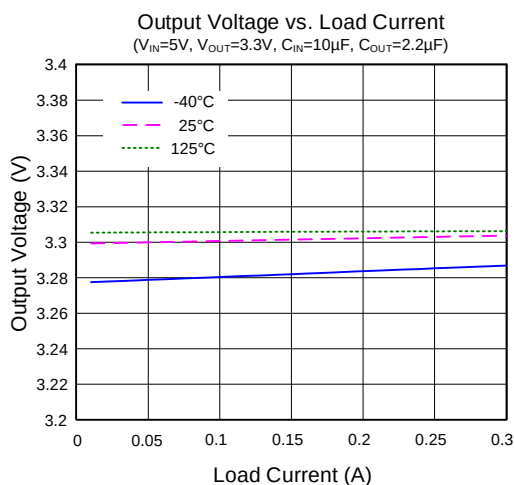
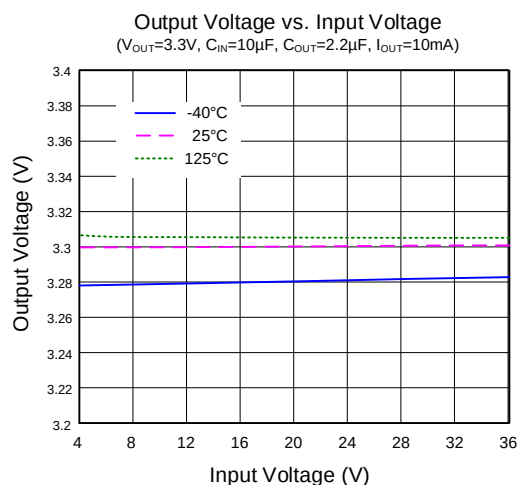
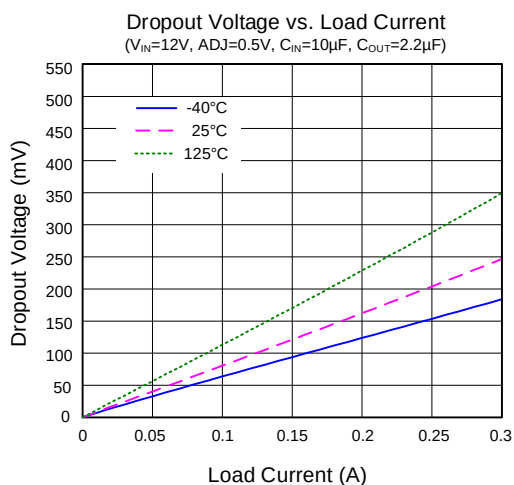
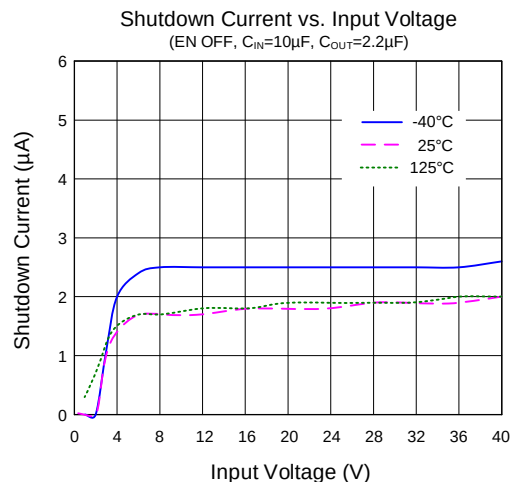
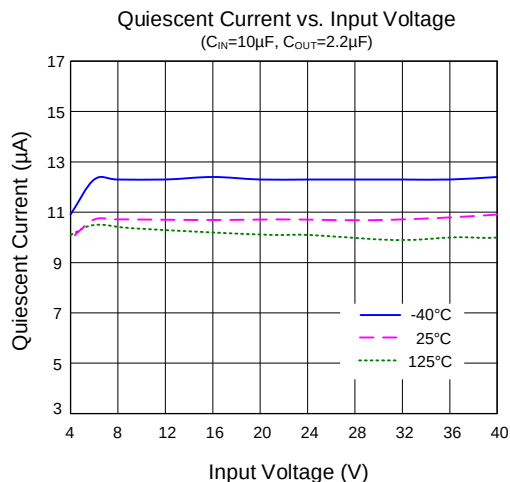
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^\circ\text{C}$. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

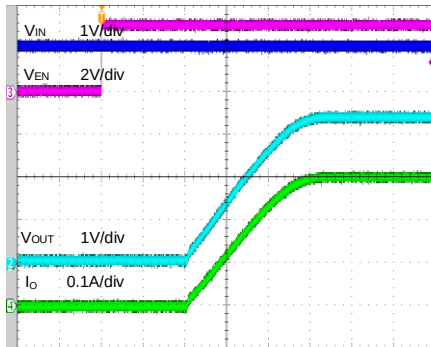
Note 5: Guaranteed by design.

Note 6: Operating lifetime is derated for junction temperatures greater than 125°C .

Typical Performance Characteristics

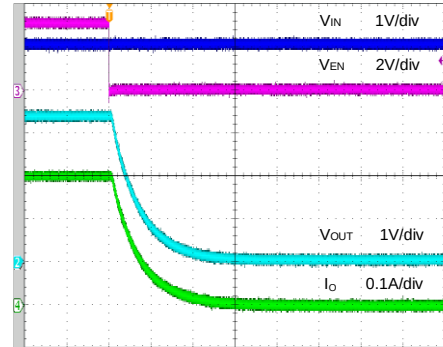


Startup from Enable
($V_{IN}=5V$, $V_{OUT}=3.3V$, $C_{IN}=10\mu F$, $C_{OUT}=2.2\mu F$, $I_{OUT}=300mA$)



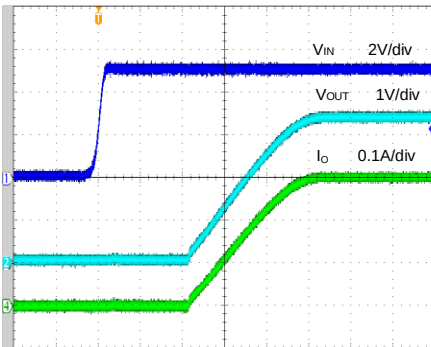
Time (400µs/div)

Shutdown from Enable
($V_{IN}=5V$, $V_{OUT}=3.3V$, $C_{IN}=10\mu F$, $C_{OUT}=2.2\mu F$, $I_{OUT}=300mA$)



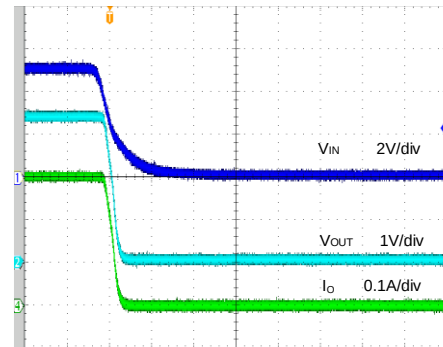
Time (40µs/div)

Startup from VIN
($V_{IN}=5V$, $V_{OUT}=3.3V$, $C_{IN}=10\mu F$, $C_{OUT}=2.2\mu F$, $I_{OUT}=300mA$)



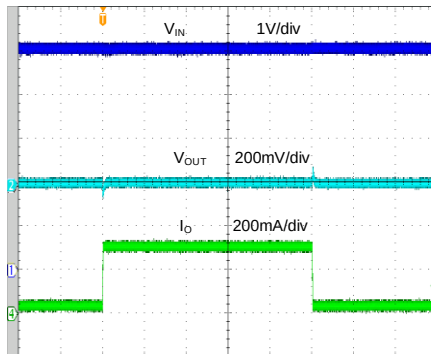
Time (400µs/div)

Shutdown from VIN
($V_{IN}=5V$, $V_{OUT}=3.3V$, $C_{IN}=10\mu F$, $C_{OUT}=2.2\mu F$, $I_{OUT}=300mA$)



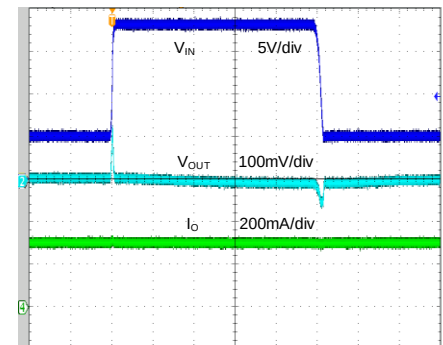
Time (400µs/div)

Load Transient
 $V_{IN}=5V$, $V_{OUT}=3.3V$, $C_{IN}=10\mu F$, $C_{OUT}=2.2\mu F$,
 $I_{OUT}=30mA \sim 300mA \sim 30mA$

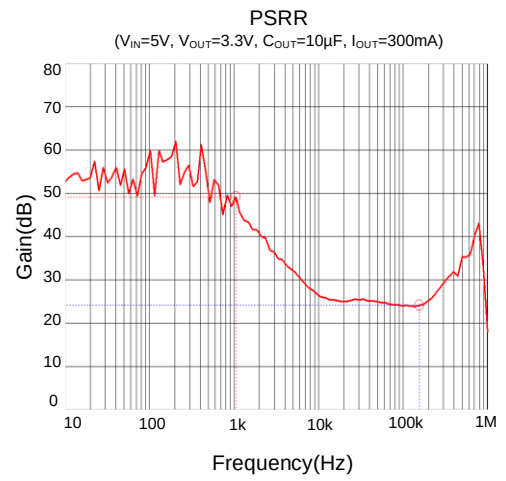
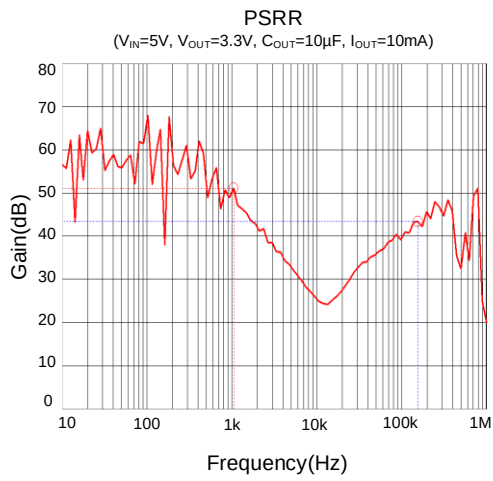


Time (400µs/div)

Line Transient
($V_{IN}=5V \sim 18V \sim 5V$, $V_{OUT}=3.3V$, $C_{IN}=10\mu F$, $C_{OUT}=2.2\mu F$,
 $I_{OUT}=300mA$)



Time (1ms/div)



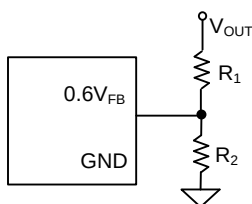
Applications Information

The SA21345CDFD is a 300mA linear regulator with a low dropout voltage. Like any low-dropout regulator, the SA21345CDFD requires input and output decoupling capacitors. The SA21345CDFD has an adjustable output which can be set by two external resistors. The device offers protection features, including over-current limit, output short and over-temperature protections.

Feedback Resistor Dividers R_1 and R_2 :

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, choosing large resistance values for both R_1 and R_2 is recommended. A value of between 10k Ω and 10M Ω is highly recommended for both resistors. If V_{OUT} is 3.3V and $R_1=1.6\text{M}\Omega$ is selected, then using the following equation, R_2 can be calculated to be 357k Ω :

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$



Input Capacitor C_{IN} :

An input capacitor with a value of 10 μF between the device input and ground pin is recommended. A typical X5R or better ceramic capacitor is recommended for most applications. This input capacitor must be located close to the device to minimize the input noise.

Output Capacitor C_{OUT} :

The SA21345CDFD is designed specifically to work with very small ceramic output capacitors for transient stability. A 2.2 μF output capacitance can be used in this application. Higher capacitance values help to improve stability. For low output voltage application, like output is 1V, a higher output capacitor, like 10 μF is recommended to get enough phase margin.

Dropout Voltage:

The SA21345CDFD has a very low dropout voltage due to its low $R_{DS(ON)}$ of the main PMOS, which determines the lowest usable supply.

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Over Current and Short Circuit Protection:

The device includes over current and short circuit protection. The current limitation circuit regulates the output current to its limitation threshold to protect IC from damage. Under over current or short circuit condition, the power loss of the IC is relatively high. And that may trigger the thermal protection.

Thermal Considerations:

The SA21345CDFD can deliver a current of up to 300mA over the full operating temperature range. However, the maximum output current must be derated at a higher ambient temperature. During all possible conditions, the junction temperature must be within the range specified under the operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

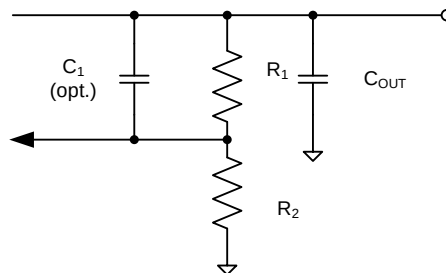
The final operating junction temperature for any set of condition can be estimated by the following thermal equation:

$$P_{D(MAX)} \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

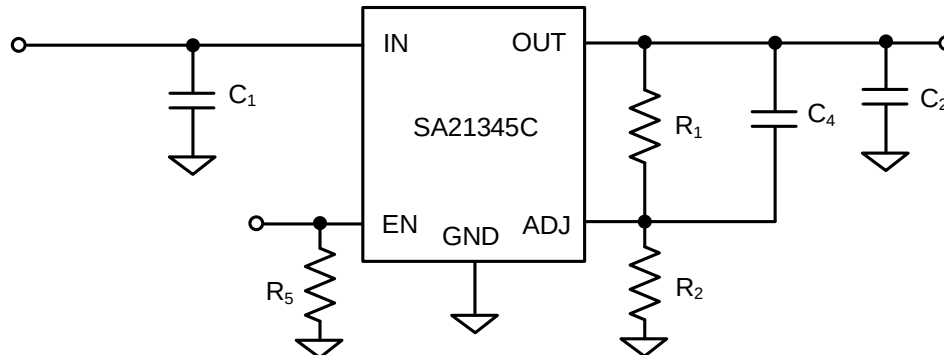
Where $T_{J(MAX)}$ is the maximum junction temperature of die and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) footprint is 57 $^{\circ}\text{C/W}$ for DFN2 $\times$ 2-8 package.

Load Transient Considerations:

The SA21345CDFD integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic cap in parallel with R_1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



Application Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
C ₁	10μF/50V, 1206, X5R	GRM31CR61H106K	Murata
C ₂	2.2μF/25V, 1206, X5R	GRM31CR61E225K	Murata
C ₄	Null		
R ₁	100kΩ		
R ₂	22.1kΩ		
R ₅	1MΩ		

PCB Layout Guide

For best performance of the SA21345CDFD, the following guidelines must be strictly followed:

1. Keep all power trace as short and wide as possible. And it is desirable to use 2-layer or 4-layer board for thermal performance and better capability of current flow.
2. Place input/output capacitor close to the IC for better transient performance.

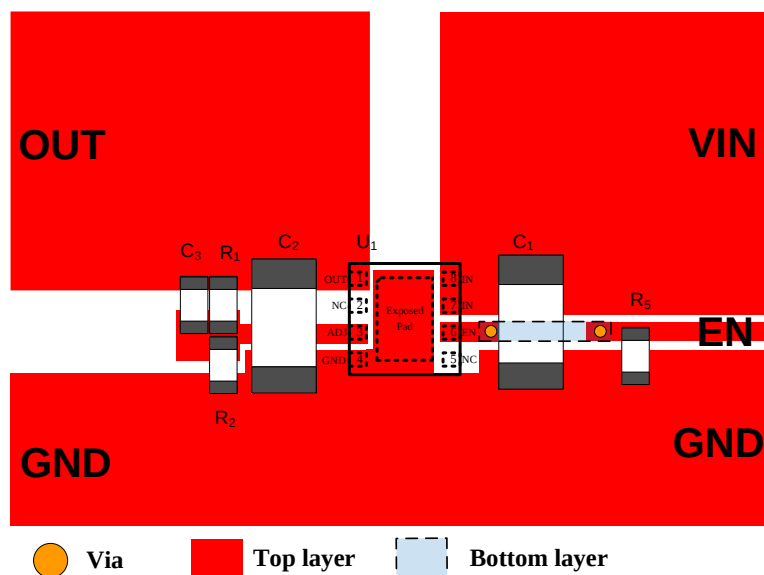
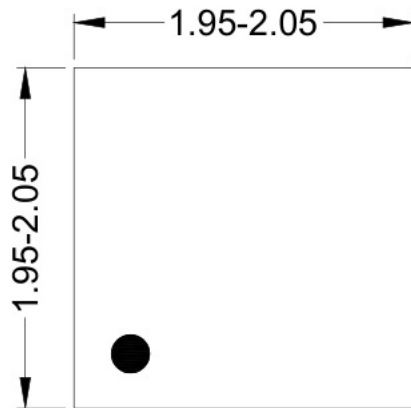
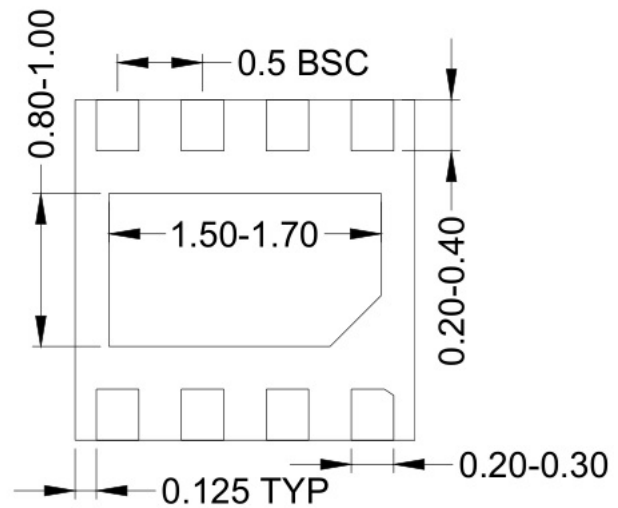


Figure3. PCB Layout Suggestion

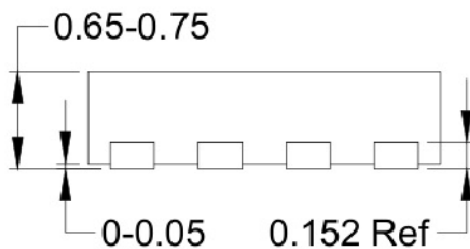
DFN2×2-8 Package Outline Drawing



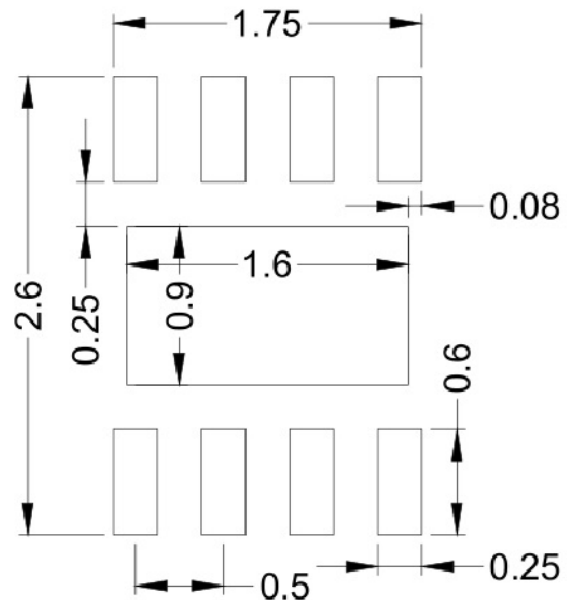
Top View



Bottom View



Side View

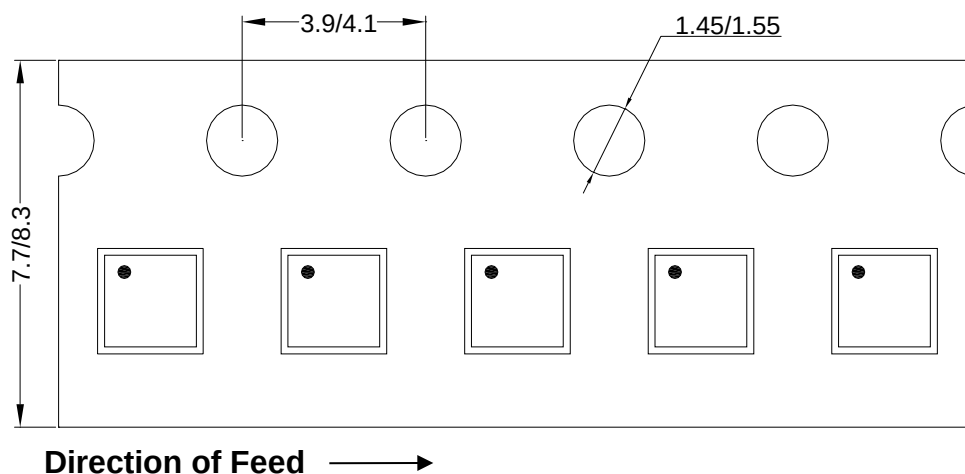


**Recommended PCB layout
(Reference only)**

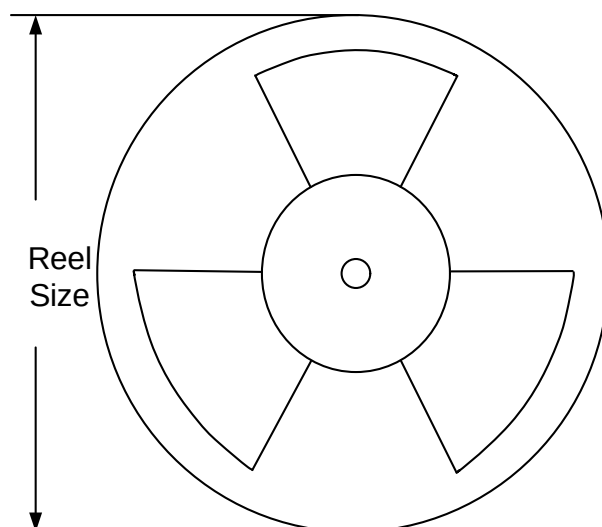
Notes: All dimensions are in millimeters and don't include mold flash & metal burr.

Tape and Reel Information

1. Tape Dimensions and Pin1 Orientation



2. Reel Dimensions



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN2x2	8	4	7"	400	160	3000



Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Aug. 29, 2024	Revision 1.0	Initial Release



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