

General Description

The SA21345Q is an efficient, precise LDO designed for high input voltage and ultra low quiescent current applications.

The SA21345Q provides adjustable output voltage and very low dropout (300mV at 300mA). Other features include the operation stability with low ESR ceramic or tantalum capacitors due to the optimized internal compensation, over current protection and thermal shutdown.

The SA21345Q is available in SO8E package.

Ordering Information

SA21345□(□□□)
 └─── Package Code
 └─── Optional Spec Code

Ordering Number	Package type	Note
SA21345QFCP	SO8E	

Features

- Wide Input Voltage Range: 4V to 36V
- Low Dropout Voltage (300mV @ 300mA)
- Ultra-low Quiescent Current
- Extremely Low Shutdown Current
- Stability with Tantalum or Ceramic Capacitor
- Excellent Load and Line Regulation
- 300mA Maximum Load Current
- Enable Control Input
- Over Current Protection
- Thermal Shutdown
- Compact Package: SO8E
- Automotive AEC- Q100 Grade 1 Qualified

Applications

- Automotive Application
- Battery-Powered Equipment
- Gateway Application
- Remote Keyless Entry Systems
- SMPS Post-regulator/ DC-DC Modules

Typical Applications

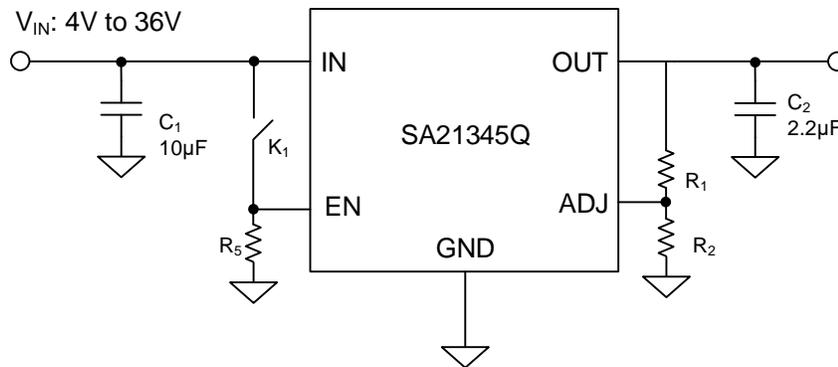
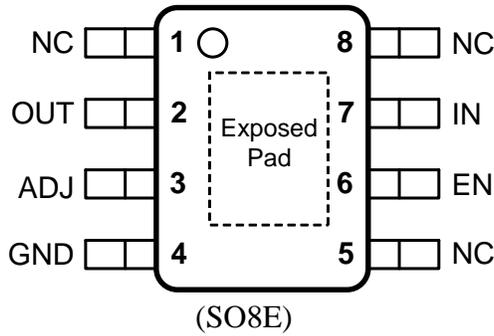


Figure1. Schematic Diagram

Pinout (top view)



Top mark: GTKxyz (Device code: GTK, x=year code, y=week code, z=lot number code)

Pin Description

Pin Name	Pin number	Pin Description
NC	1,5,8	Not connected.
OUT	2	Output pin. Bypass this pin to the Ground pin with a 2.2μF output capacitor.
ADJ	3	Output voltage adjust pin. Feedback the output voltage through resistor voltage divider network. $V_{OUT}=0.6 \times (1+R_1/R_2)$
GND	4	Ground pin.
EN	6	Enable pin. Pull it low to shutdown or pull it high to enable, do not leave it floating.
IN	7	IC power supply input. Bypass this pin to Ground pin with a 10μF capacitor.
Exposed Pad	/	The exposed pad should be connected to ground plane for better thermal performance.

Block Diagram

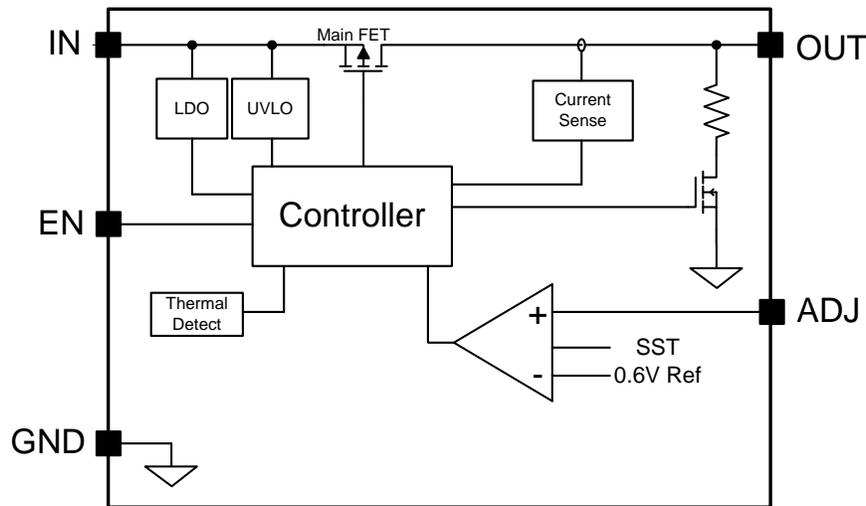


Figure2. Block Diagram



SILERGY

SA21345Q

Absolute Maximum Ratings (Note 1)

IN to GND	-----	-0.3V to 40V
OUT, EN, ADJ to GND	-----	-0.3V to min (0.3V+V _{IN} , 40V)
Power Dissipation, P _D @ T _A = 25°C SO8E	-----	3.3W
Package Thermal Resistance (Note 2)		
θ _{JA}	-----	30°C/W
θ _{JC}	-----	20 °C/W
Junction Temperature	-----	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-65°C to 150°C
ESD Susceptibility		
HBM (Human Body Mode)	-----	2kV
CDM (Charged Device Mode)	-----	500V

Recommended Operating Conditions (Note 3)

Supply Input Voltage	-----	4V to 36V
Ambient Temperature Range	-----	-40°C to 125°C

Electrical Characteristics

($V_{IN}=12V$, $V_{OUT}=3.3V$, $V_{EN}=V_{IN}$, $T_J = -40^{\circ}C \sim 125^{\circ}C$, unless otherwise specified, the values are guaranteed by test design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}	$I_{OUT}=10mA$	4		36	V
Reference Voltage	V_{REF}	$I_{OUT}=10mA$	588	600	612	mV
Input Voltage UVLO Threshold	V_{ULVO}	V_{IN} rising	2.9	3.4	4	V
UVLO Hysteresis	V_{UVLO_HYS}			0.1		V
Line Regulation	ΔV_{LNR}	$V_{IN}=(V_{OUT}+0.3V)$ to 36V, $I_O=10mA$		1	1.5	mV/V
Load Regulation	ΔV_{LDR}	$I_O=10mA$ to 300mA		0.25	0.5	%
Dropout Voltage	ΔV_{DROP}	$V_{IN}=12V$, $V_{ADJ}=0.5V$, $I_O=10mA$		10	20	mV
		$V_{IN}=12V$, $V_{ADJ}=0.5V$, $I_O=150mA$		150	300	mV
		$V_{IN}=12V$, $V_{ADJ}=0.5V$, $I_O=300mA$		300	550	mV
Quiescent Current	I_Q	No Load		10	17	μA
Shutdown Current	I_{SHDN}	$V_{EN}=0V$, $V_{IN}=24V$			7	μA
Output Current	I_O	$V_{IN}=V_{OUT}+0.6V$	0		300	mA
Output Current limit	I_{LIM}	$V_{IN}=6V$, $V_{OUT}=0.9 \times V_{OUT}(\text{normal})$	300		900	mA
Output Short Protection Threshold	$V_{ADJ.SHORT}$	V_{FB} Falling	8	16	30	% V_{REF}
Power Supply Rejection Ratio (Note 4)	PSRR	$f=1kHz$, $C_{OUT}=10\mu F$		60		dB
		$f=150kHz$, $C_{OUT}=10\mu F$		30		dB
Enable Input Logic-High Voltage	V_{EN_H}	$V_{IN}=5V$	1.5			V
Enable Input Logic-Low Voltage	V_{EN_L}	$V_{IN}=5V$			0.4	V
Shutdown Discharge Resistance	R_{DIS}	$V_{IN}=12V$, $EN=0V$, $V_{OUT}=2V$		600		Ω
Thermal Shutdown Temperature (Note 4)	T_{SD}			150		$^{\circ}C$
Thermal Shutdown Hysteresis (Note 4)	T_{HYS}			20		$^{\circ}C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

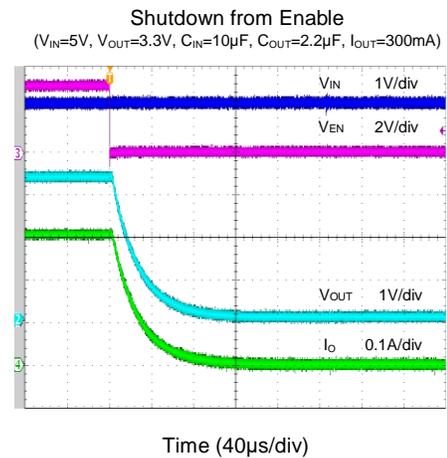
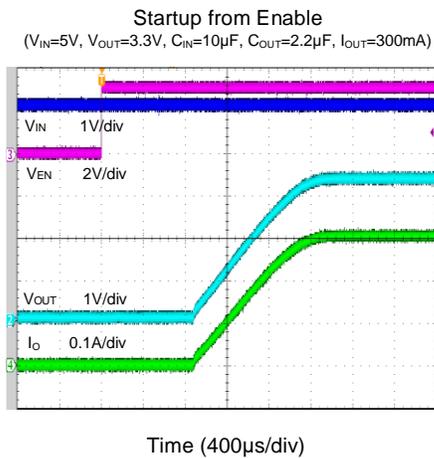
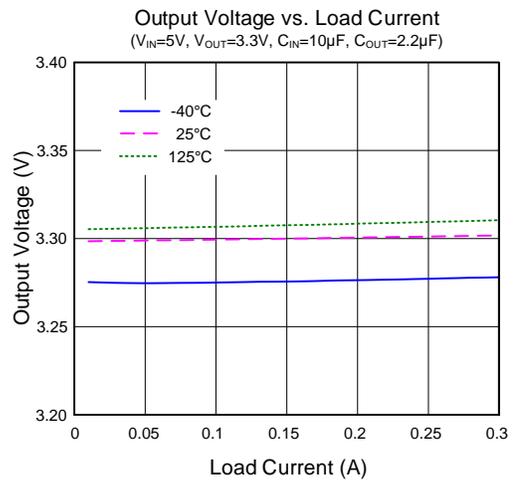
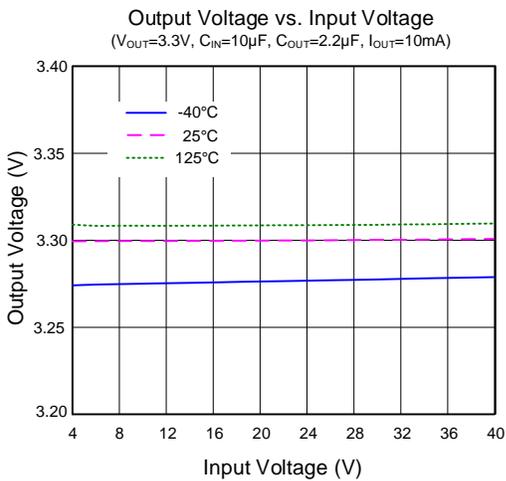
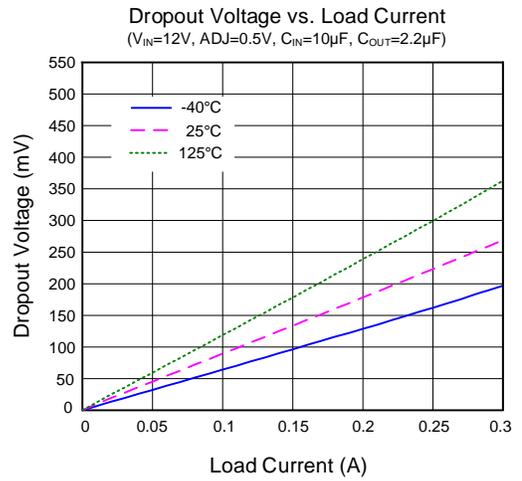
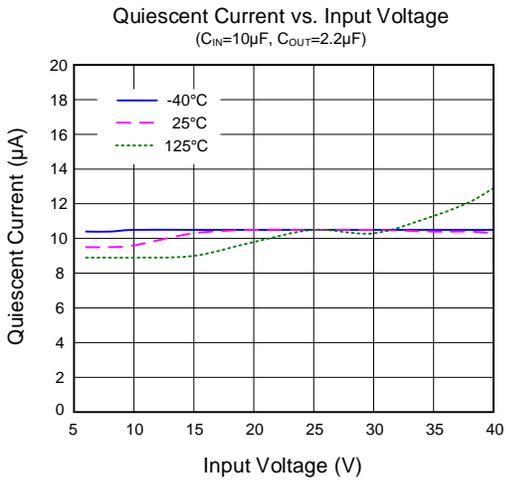
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

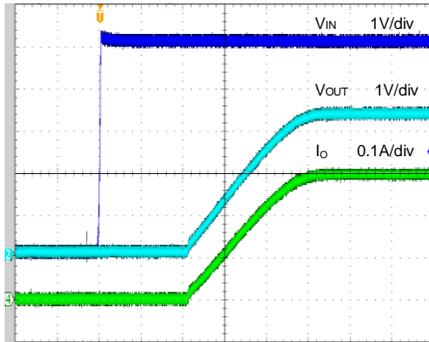
Note 4: Guaranteed by design.

Note 5: Operating lifetime is derated for junction temperatures greater than $125^{\circ}C$.

Typical Performance Characteristics

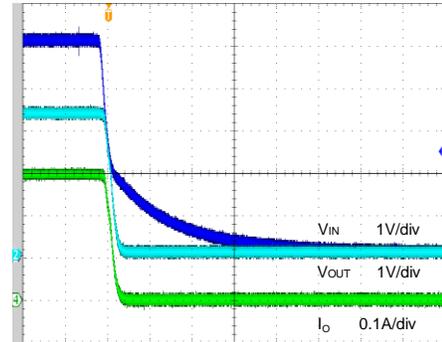


Startup from V_{IN}
 $(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10\mu F, C_{OUT}=2.2\mu F, I_{OUT}=300mA)$



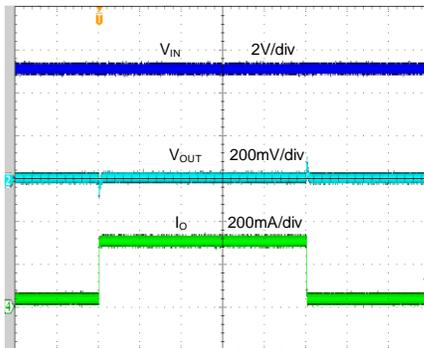
Time (400 μ s/div)

Shutdown from V_{IN}
 $(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10\mu F, C_{OUT}=2.2\mu F, I_{OUT}=300mA)$



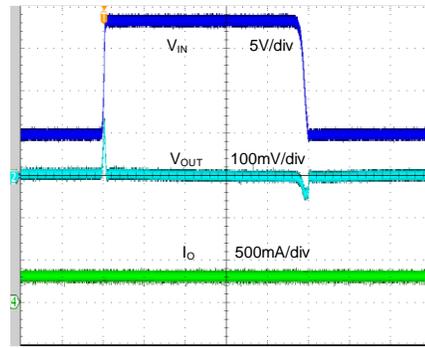
Time (400 μ s/div)

Load Transient
 $V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=10\mu F, C_{OUT}=2.2\mu F,$
 $I_{OUT}=30mA \sim 300mA \sim 30mA)$



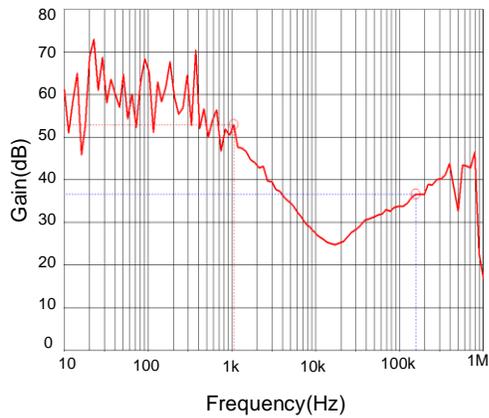
Time (400 μ s/div)

Line Transient
 $(V_{IN}=5V \sim 18V \sim 5V, V_{OUT}=3.3V, C_{IN}=10\mu F, C_{OUT}=2.2\mu F,$
 $I_{OUT}=300mA)$

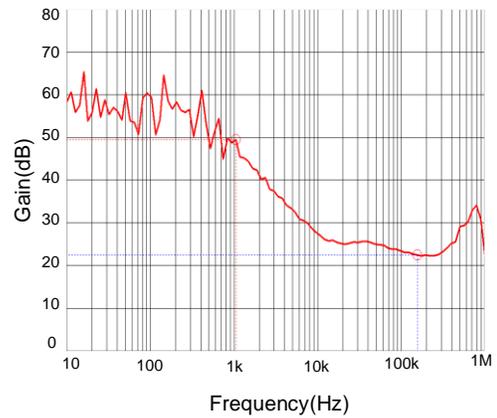


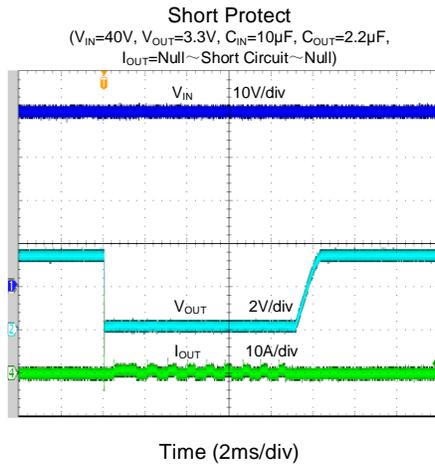
Time (800 μ s/div)

PSRR
 $(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=Null, C_{OUT}=4.7\mu F, I_{OUT}=10mA)$



PSRR
 $(V_{IN}=5V, V_{OUT}=3.3V, C_{IN}=Null, C_{OUT}=4.7\mu F, I_{OUT}=300mA)$





Operation

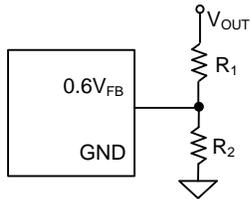
The SA21345Q is a 300mA linear regulator with a low dropout voltage. Like any low-dropout regulator, the SA21345Q requires input and output decoupling capacitors. The SA21345Q has an adjustable output which can be set by two external resistors. The device with fully protection includes over current limit, output short protection and over temperature operation.

Applications Information

Feedback Resistor Dividers R₁ and R₂:

Choose R₁ and R₂ to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R₁ and R₂. A value of between 10kΩ and 10MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R₁=1.6MΩ is chosen, then using following equation, R₂ can be calculated to be 357kΩ:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$



Input Capacitor C_{IN}:

An input capacitor about 10μF is required between the device input pin and ground pin. A typical X5R or better grade ceramic capacitor is recommended in this application. This input capacitor must be located close to the device to minimize the input noise.

Output Capacitor C_{OUT}:

For transient stability, the SA21345Q is designed specifically to work with very small ceramic output capacitors. 2.2μF output capacitance can be used in this application. Higher capacitance values help to improve transient. The output capacitor's ESR is critical because it forms a zero to provide phase lead which is required for loop stability.

Dropout Voltage:

The SA21345Q has a very low dropout voltage due to its extra low R_{DS(ON)} of the main PMOS determines the lowest usable supply.

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Over Current and Short Circuit Protection:

The device includes over current and short circuit protection. The current limitation circuit regulates the output current to its limitation threshold to protect IC from damage. Under over current or short circuit condition, the power loss of the IC is relatively high. And that may trigger the thermal protection.

Thermal Considerations:

The SA21345Q can deliver a current of up to 300mA over the full operating temperature range. However, the maximum output current must be derated at higher ambient temperature. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

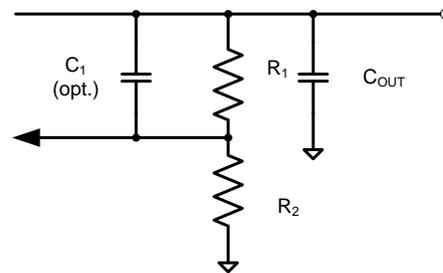
The final operating junction temperature for any set of condition can be estimated by the following thermal equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where T_{J(MAX)} is the maximum junction temperature of die and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) footprint is 30°C/W for SO8E package.

Load Transient Considerations:

The SA21345Q integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic cap in parallel with R₁ may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



PCB Layout Guide:

For best performance of the SA21345Q, the following guidelines must be strictly followed:

1. Keep all power trace as short and wide as possible. And it is desirable to use 2-layer or 4-

layer board for thermal performance and better capability of current flow.

2. Place input/output capacitor close to the IC for better transient performance.

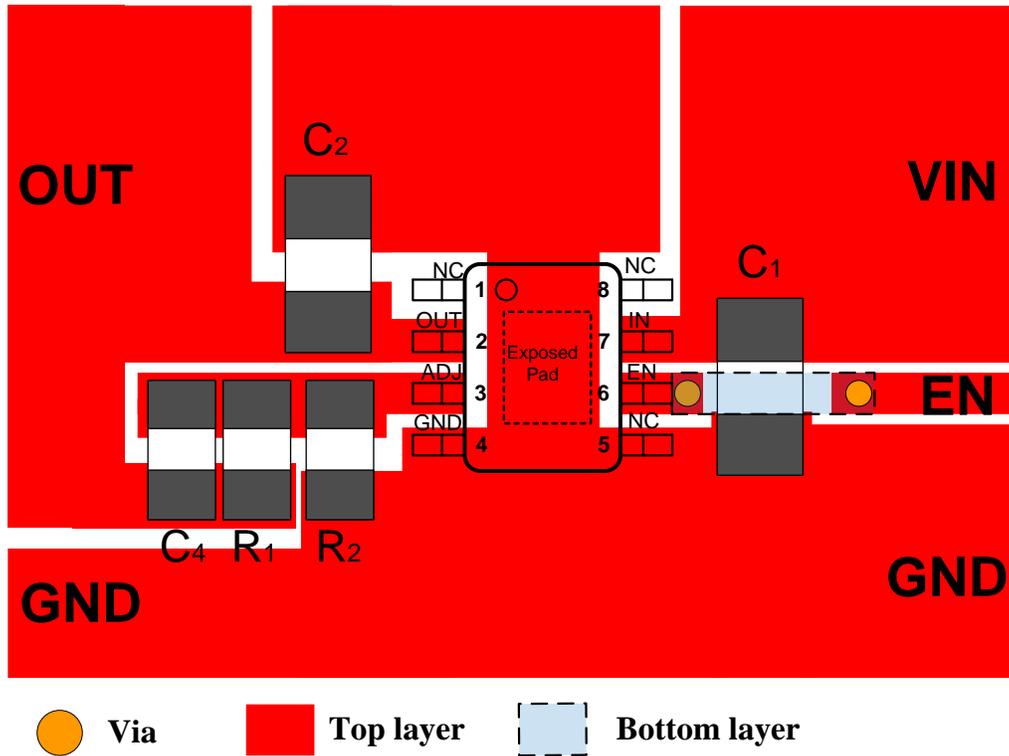
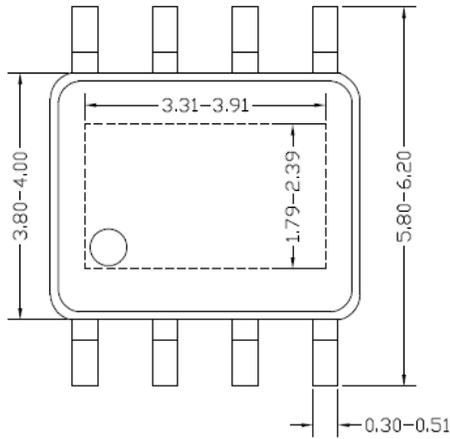
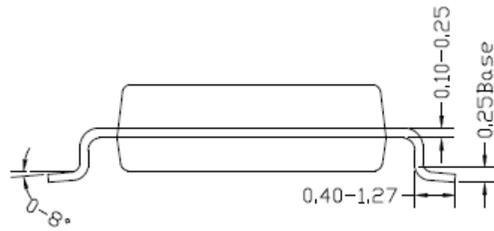


Figure3. PCB Layout Suggestion

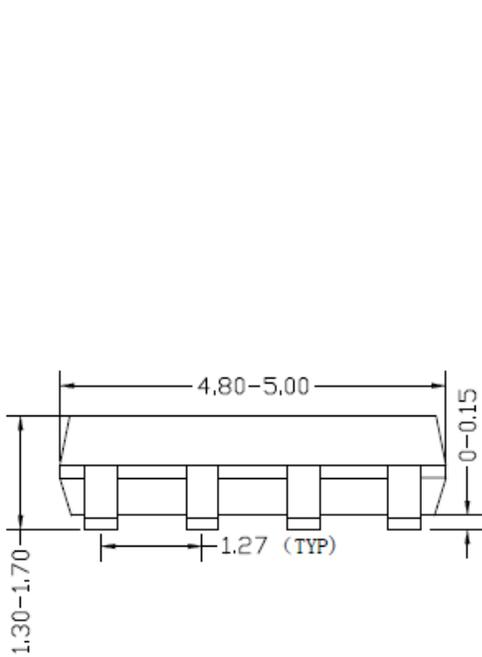
SO8E Package Outline & PCB layout



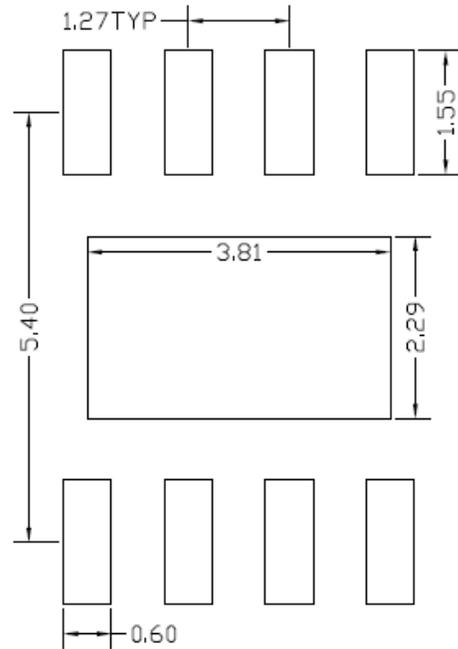
Top view



Side view



Front view



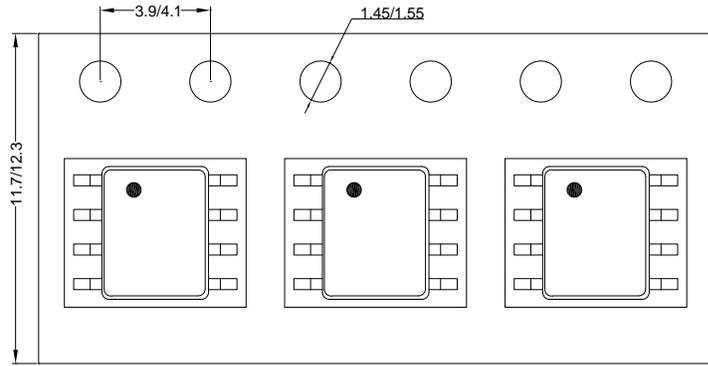
**Recommended PCB Layout
(Reference Only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

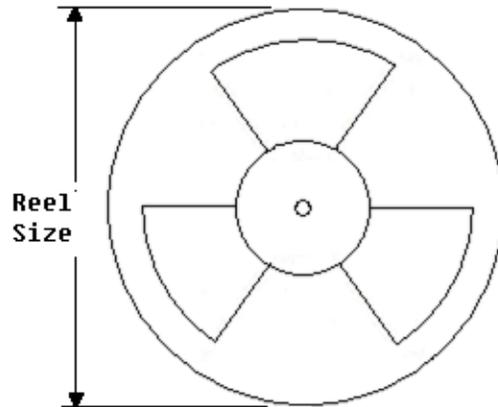
1. Taping orientation

SO8E



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8E	12	8	13"	400	400	2500

3. Others: NA



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Nov.23, 2023	Revision 0.9	Initial Release



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