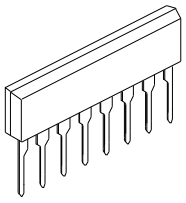
VOLTAGE CONTROLLED AMPLIFIER FOR ELECTRONIC VOLUME CONTROL

DESCRIPTION

The SA2159 is a voltage-controlled amplifier (VCA) circuit. The chip is a high-performance current–in/current-out devices including two opposing-polarity, voltage-sensitive control ports. Due to super low-noise application, the circuit adopts high $h_{FE.}$ Complementary NPN/PNP pairs configuration. It requires little external support circuitry and selects a space-efficient plastic 8-pin single–in–line (SIP) package. The SA2159 VCA combines a number of advantages such as low noise, low distortion, low offset and high gain-bandwidth to offer discrete performance at IC prices.



SIP-8

FEATURES

* Wide dynamic range:>115dB
* Wide gain range:>130dB
* Logarithmic gain control
* Low distortion:(0.008%@0dB gain, 0.035%@15dB gain)
* Wide gain-bandwidth: 6MHz
* Single in–line package
* Dual gain-control ports(pos/neg)

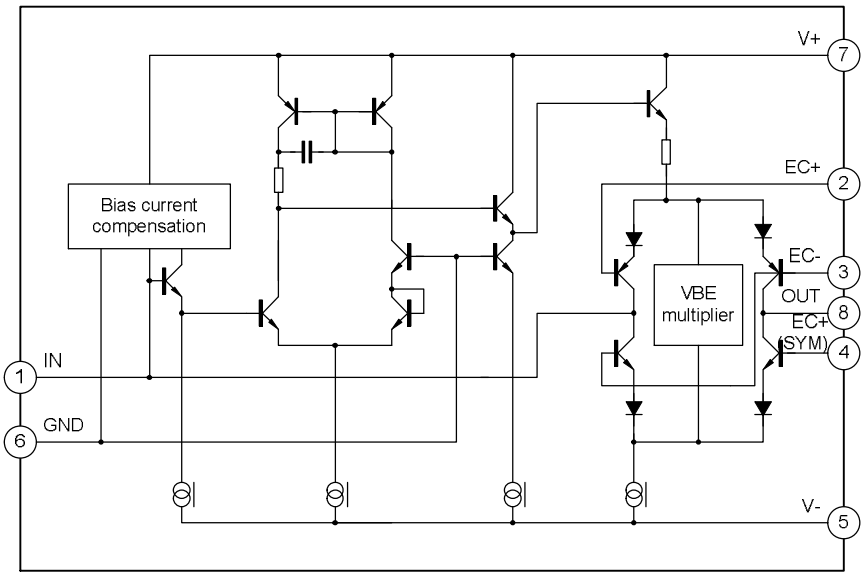
APPLICATIONS

* Faders
* Expanders
* Compressors
* Equalizers
* Oscillators
* Filters
* Automation systems

ORDERING INFORMATIONS

Device	Package
SA2159	SIP-8

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Tamb=25°C)

Characteristic	Symbol	Ratings	Unit
Positive Supply Voltage	VCC	+15	V
Negative Supply Voltage	VEE	-15	V
Supply Current	ICC	30	mA
Power Dissipation	PD	330	mW
Operating Temperature Range	TOP	-20~+75	°C
Storage Temperature Range	TST	-40~+125	°C

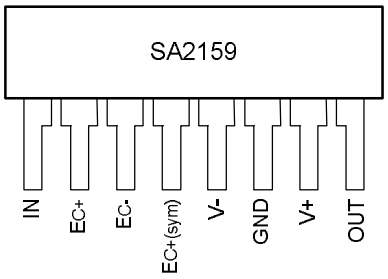
RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Test conditions	Min	Typ	Max	Unit
Supply Voltage	VCC		+4	+12	+15	V
Supply Voltage	VEE		-4	-12	-15	V
Bias Current	ISET	VCC- VEE=24V	-	2	2.4	mA
Signal Current	IIN+IOUT	ISET=2.4mA	-	125	550	μA

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, VCC+=+15V, VCC-=-15V, Tamb =25°C)

Characteristics	Symbol	Test conditions	Min	Typ	Max	Unit
Supply Current	ICC	No signal	-	2	3	mA
Equiv. Input Bias Current	IB	No signal	-	5	20	nA
Input Offset Voltage	VOFF(IN)	No signal	-	+10	-	mV
Output Offset Voltage	VOFF(OUT)	ROUT=20KΩ 0 dB gain THD adj for min	-	1		mV
Gain Cell Idling Current	IIDLE		-	20	-	μA
Gain-Control Constant	 EC+ EC-	Tamb=20°C -60dB<gain<+40 dB Pins 2&4(fig.13) Pin 3	 5.8 -5.8	 5.9 -5.9	 6.1 -6.1	 mV/dB mV/dB
Gain-Control Temp Co	ΔEC/ΔTamb	Tamb~27°C	-	-0.33	-	%/°C
Gain-Control Linearity		-60~40dB gain	-	0.5	2	%
Offset Isolation(Fig.14)		EC+=-360mV, EC-=+360mV	110	115	-	dB
Output Noise	en(OUT)	20Hz-20kHz ROUT=20KΩ 0dBain +15dBain	 - -	 -97 -88	 -89 -82	 dBV dBV
Symmetry Control Voltage	VSYM	AV=0dB, THD<0.07%	-4	0	+4	mV
Total Harmonic Distortion	THD	IOUT=30μA,1KHz 0dB gain +20dB gain -20dB gain	 - - -	 0.007 0.02 0.02	 0.07 0.10 0.15	 % % %

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	Description
1	IN	Signal input
2	EC+	Positive exponential control
3	EC-	Negative exponential control
4	EC+(SYM)	Symmetry control
5	V-	Negative power
6	GND	Ground
7	V+	Positive power
8	OUT	Output

FUNCTION DESCRIPTION

OPERATING THEORY

The SA2159 VCA is designed for high performance in audio frequency applications which requires exponential gain control, low distortion, wide dynamic range and low DC bias modulation. The gain control part controls gain by converting an input current signal to a bipolar logged voltage, adding a DC control voltage and reconverting the summed voltage back to a current through a bipolar antilog circuit.

The simplified internal circuit diagram of the IC is shown in figure 1. The AC input signal current flows in the input pin 1, which is maintained at a virtual ground potential by the internal op amp.

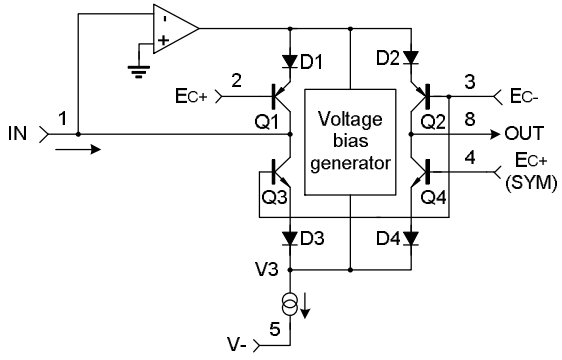


Figure 1. Simplified internal circuit diagram

Positive input currents

For positive input currents (IIN defined as flowing into pin 1), the op amp turns Q1 and D1 off, while simultaneously turns Q3 and D3 on. Thus, the input signal current is forced to flow through Q3 and D3.

Logging & Antilogging

We know the basic properties Vbe of the transistor and the collector current Ic as:

Vbe = V_T ln (Ic/Is)

It is assumed that D3/Q3 and Q4/D4 are matched, we therefore can conclude:

V3 = EC- - 2V_T ln (Ic3 / Is)

Where V3 is the voltage at the junction of D3 and D4, VT is the thermal voltage, kT/q, Ic3 is the current in the collector of Q3, and IS is the reverse-saturation current of Q3.

In typical applications (see typical applications diagram.), pin 4 is normally at or very near ground. Pin 8 is connected to a virtual ground. In this way, the voltage at the cathodes of D3 and D4 will cause an exponentially-related current to flow in D4 and Q4, and out through pin 8. Mathematically:

V3 = EC+ - 2V_T ln (Ic4 / Is)

Exponential gain control

It can be derived from said two equations:

V3 = EC- - 2V_T ln (Ic3 / Is) = EC+ - 2V_T ln (Ic4 / Is)

EC+ - EC- = 2V_T ln (Ic4 / Is) - 2V_T ln (Ic3 / Is) = 2V_T ln (Ic4 / Ic3)

Rearranging terms,

Ic4 = ic3 e (EC+ - EC-) / 2V_T

Av = Ic4 / Ic3 = e (EC+ - EC-) / 2V_T

Where AV is the current gain, which is exponential with the difference in the voltage EC+ and EC-

For pin 4 at or very near ground, at room temperature, and converting to a base of 10 for the exponential, this reduces to:

Av = 10 - EC- / 0.118

Another way of expressing this relationship is:

Gain = 20 log Av = - EC- / 0.0059, where the unit of Gain is dB.

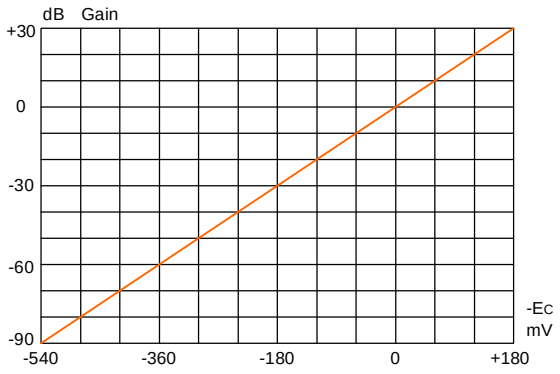


Figure 2. Gain versus control voltage at 25°C

Negative input currents

For negative input currents, the operation of Q1/D1 and Q3/D3 is symmetric with Q2/D2 and Q4/D4. pin 2 is connected to ground, or very nearly ground potential (see the section below on symmetry adjustment for more detail), Since the top pair versus the bottom pair transistors are inverted (NPN/PNP) and the bases are cross-connected between the input (left) half and the output (right) half of each pair, the polarity (positive/negative, in dB) of the gain is the same.

Symmetry adjustment

The layout design construction of the devices assures relatively good matching between the paired transistors, but even small VBE mismatches can cause a dc output current to flow in pin 8, which will ultimately manifest itself as a DC offset voltage. The DC offset voltage will be modulated by gain commands, and may become audible as “thumps” if gain commands changes very large and fast.

Transistor matching also affects distortion. If the top half of the gain cell is perfectly matched, while the bottom half is not well match, then the gain commanded by the voltage at pin 3 will affect the two halves of the core differently. Since positive and negative halves of input signals are handled by separate parts of the core, this gives rise to even order distortion production.

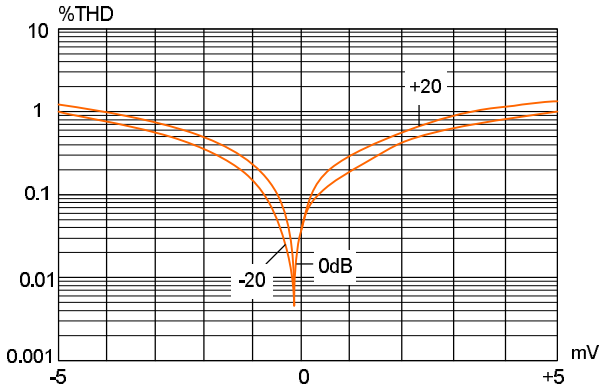


Figure 3. Typical THD versus symmetry voltage

Accordingly, the base of Q1 and Q4 are brought out to pin 2 and pin 4, respectively. This allows applying a small static voltage differential to the two bases. The applied voltage differential must be set to the sum of the Vbe mismatches around the core. Typical applications diagram includes a typical symmetry voltage application circuitry. The symmetry trim pot controls primarily even-order harmonic distortion, and is adjusted for minimum distortion in the output waveform.

Opposite polarity control

As may be seen from the equation, the bases of Q1 and Q4 can also be used as an additional control port, which can be used as opposite control port of pin 3. Both pins must be applied to the control voltage simultaneously, while the voltage applied between the two pins must be small difference. (A typical connection is shown in Figure 4.) Either pin 3, or pins 2 and 4, or both ports together may be used for gain control. Mathematically:$Av = 10^{-EC-/0.118}$, or Gain = 20 log Av = - EC- / 0.0059, where the unit of Gain is dB.

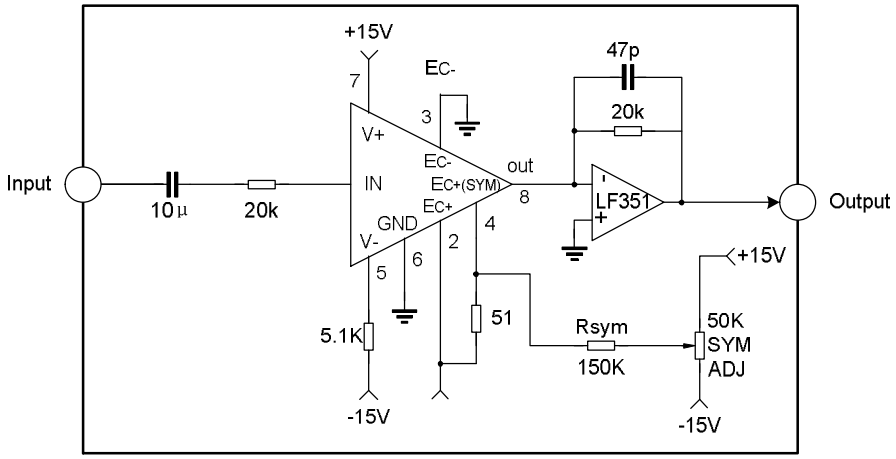


Figure 4. Using Both Control Ports Pin 2 and Pin4

Control port source impedance

The control ports (pin 2 through 4) are connected directly to the bases of the logging and /or antilogging transistors. Since the collector currents of transistors are signal-related, the base currents will also be signal-related. If the source impedance of the control voltage is large, the signal-related base currents will cause signal-related voltage to appear at the control ports, which will affect precise logging and antilogging, in turn causing distortion. At high signal levels, even 100Ω can spoil the good performance of these parts. Due to signal current based on a transistor β of approximately 300(NPN) or 100(PNP), the distortion caused by a specific and non-zero source impedance by determining the base voltage modulation can be estimated.

In SA2159 VCA design, the source impedance of pin 2 and pin 3 are zero, while the source impedance of pin 4 is 50Ω because pin 4 is intended for connection to the symmetry control.

DC input signals

Any dc currents in the feedback loop of the internal op amp will show up as dc terms in the output signal, and will be modulated by gain commands. The bias current compensation circuit inside the chip offers the input bias current to the input differential amplifier. Ac input coupling is strongly recommended to prevent an input dc current supplied from external application circuit of the VCA.

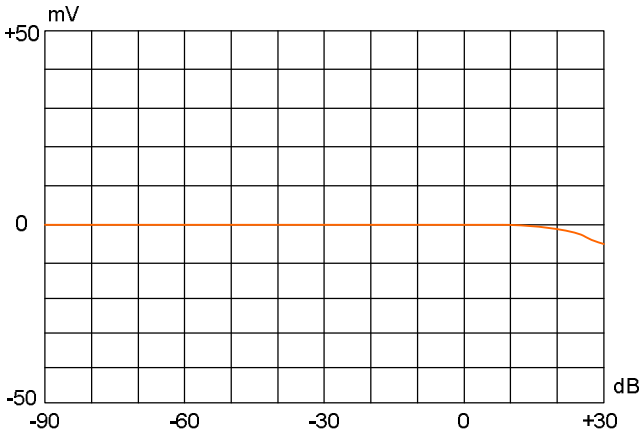


Figure 5. DC offset vs. gain, after symmetry adjustment

Current programming

An external Iset can set the size of the current source at the bottom of the core. Iset is normally determined by a resistor between V- and pin 5 (Vpin 5 = -2.7V, typically). Iset should be 200μA larger than the total of the peak input and output signal currents because Iset divides into two portions: approximately 200μA is used for internal biasing, and the rest is available for the current source at the bottom of the core.

Note that since the sum of the input and output currents plus ISET must be supplied through the output impedance of the internal op amp, this impedance is approximately 2kΩ, the voltage available to drive the core will lower.

Headroom

The logarithmic characteristics of the core transistors also limit maximum signal currents. The devices used in the SA2159 are specially designed to conform to an ideal log-linear curve over a wide range of currents, but their limit value is approximately 1mA. Distortion will increase with increasing current levels because of falling log conformance. Figure 6 through 8 show typical distortion versus 1 kHz signal level for the SA2159 at -15dB, 0 dB, and +15dB gain. Thus, the maximum signal level for a particular design will be determined by the acceptable distortion.

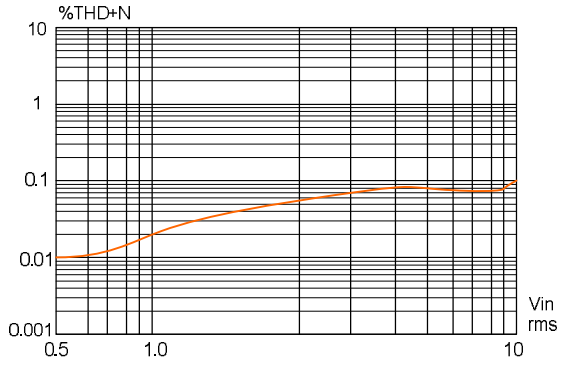


Figure 6. 1KHz THD +Noise Vs. input,-15dB gain

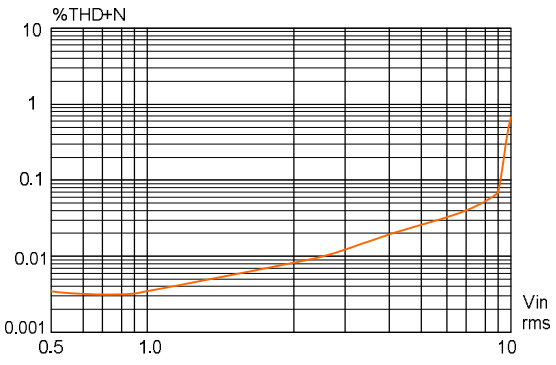


Figure 7. 1kHz THD+Noise Vs. level, 0dB gain

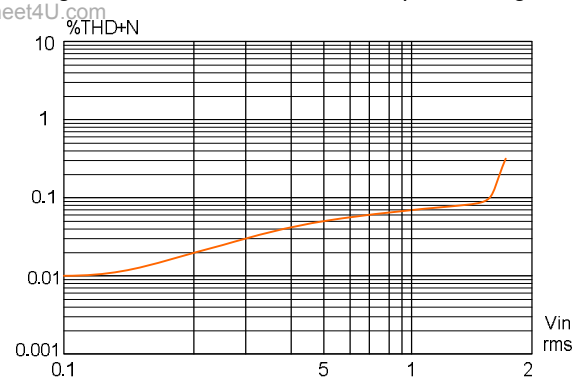


Figure 8. 1kHz THD+Noise Vs. Input, +15dB gain

APPLICATIONS

Input

As mentioned above, because input and output signals are currents, not voltages, the current input/output mode provides great flexibility in application.

Internal negative feedback loop provides a virtual ground to the input pin 1 (See Figure 1). Within the linear range of the device, the input resistor (shown as 20kΩ in typical application circuit) should be scaled to convert the available ac input voltage to a current. In order to obtain best distortion performance, peak input currents should be kept under 1 mA. The input impedances must be less than 30kΩ to assure the circuit stability.

The feedback impedances around the internal op amp (essentially Q1/D1 and Q3/D3) are fixed. Low values for the input resistor will require more closed-loop gain from the op amp.

Since the open-loop gain naturally falls off at high frequencies, this resistor should be kept to 10kΩ or above in order to prevent high frequency distortion when the gain is too much. Distortion vs. frequency for a 1V signal at 0dB gain with a 20 kΩ input resistor is shown in Figure 9.

As mentioned above, any dc input currents will cause dc signals in the output. The dc signals will be modulated by gain command, in turn causing audible thump. Therefore, in order to control quality audio applications, capacitive coupling must be adopted in actual application, which can give acceptable low frequency performance.

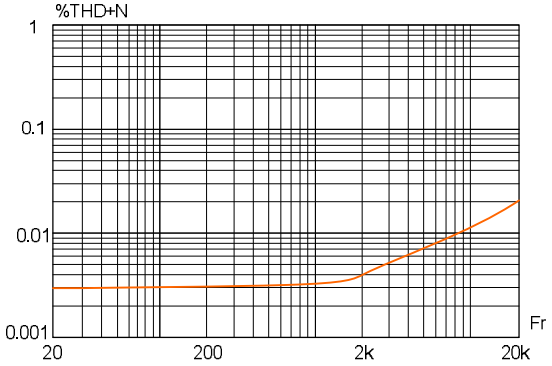


Figure 9. Typical THD Vs. frequency, 0dB gain

Output

The output pin (pin 8) should be connected to a virtual ground node, so that current flowing in it may be converted to a voltage. Choose the external op amp can improve audio performance.

A small feedback capacitor around the output op amp is necessary to cancel the output capacitance of the VCA, so that most op amps can operate steadily. The capacitance at pin 8 is typically 30 pf.

Power supplies

The positive supply is connected directly to pin 7 without special bypassing circuit, but it is good practice to include a small (~1μf) electrolytic close to the VCA IC on the PCB. There is no particularly dependence between performance and supply voltage. The lowest supply voltage is determined by the sum of the input and output currents plus ISET, which must be supplied through the resistor (~2kΩ) at the top of the core transistors while still allowing enough voltage swing to bias the internal op amp and the core transistors themselves. Reducing signal currents may help accommodate low supply voltages.

The process characteristics and internal power consumption determine the highest supply voltage. +15V is the nominal limit.

A resistive current source determining the current available for the core is connected to the negative supply terminal. As mentioned before, this source must supply 200μA current over the sum of the required signal currents including input signal current, output signal current and the bias to run the rest of the IC. 2.4mA is recommended for most pro audio applications where +15V supplies are common and headroom is important.

Bypassing at pin 5 is not necessary because pin 5 is a current supply, not a voltage supply.

Pin 6 is used as a ground reference for the VCA which connect the non-inverting input of the internal op amp, as a portion of the internal bias network. It may not be used as an additional input pin.

Voltage control

Pin 3 is the primary voltage control pin. This point controls gain is inversely proportional to applied voltage: positive voltage causes loss, negative voltage causes gain. The current gain of the VCA is unity when pin 3 is at 0V and varies with voltage at approximately -5.9m/dB, at room temperature.

As implied by the equation for Av at the foot of page 3, the gain is sensitive to temperature. The constant of proportionality is 0.33% of the decibel gain commanded, per degree Celsius, referenced to 27°C (300K). The formula is:

Gain = (EC+ - EC-) / (0.0059 * 1.0033 * ΔT).

Where ΔT is the difference between the actual temperature and room temperature (27°C)

For most audio applications, this change with temperature is of little consequence. However, if necessary, it may be compensated by a resistor which varies its value by 0.33%/°C.

When pin 3 is used for voltage control, Pin 2 is connected to ground and pin 4 is used to apply a small symmetry voltage (~±4 mV) to correct for VBE mismatches within the VCA IC. Therefore, in order to obtain optimum performance, pin 4 connects with an external impedance of approximately 50Ω. A trim pot is used to adjust the voltage between pin 4 and pin 2 as shown in typical application circuit. Voltage adjustment range is ±4 mV.

Pin 2 and pin4 can be used together as an opposite sense voltage control port (See Figure 4). Pin 3 may be grounded and pin 2 driven against the symmetry-adjustment voltage. The change of voltage at pin 4 does have a small effect on the symmetry voltage, but this is of little practical consequence in most applications.

The chip can combine all control ports together with differential drive (See Figure 10). While the driving circuitry is more complex, this configuration offers better performance at high attenuation levels (<-90dB) where the single control port circuits begin to saturate Q1 (for EC- drive) or Q3 (for EC+ drive). When either of these transistors saturates, the internal op amp will accommodate the change in current demand by responding with a small change in its input offset voltage. This leads to an accumulation of charge on the input capacitor, which in turn can cause thump when the high attenuation is suddenly removed(e.g., when a muted channel is opened). Differential control drive avoids the large dc levels otherwise required to command high attenuation (+600mV or -100dB gain at pin 3 alone, vs. ±300mV when using both pin 3 and pins 2 and 4).

Control port drive impedance

In order to reduce distortion, it is necessary to use low source impedance at the control port. Thus, this often suggests an op amp is used to drive the control port directly (see below under noise considerations). However, due to falling loop gain at high frequencies, the closed-loop output impedance of an op amp typically rises. The output impedance is therefore inductive at high frequencies. Excessive inductance can cause the VCA to

oscillate internally. In such cases, a 100Ω resistor in series with a 1.5nf capacitor between the control port and ground will usually suffice to prevent the instability.

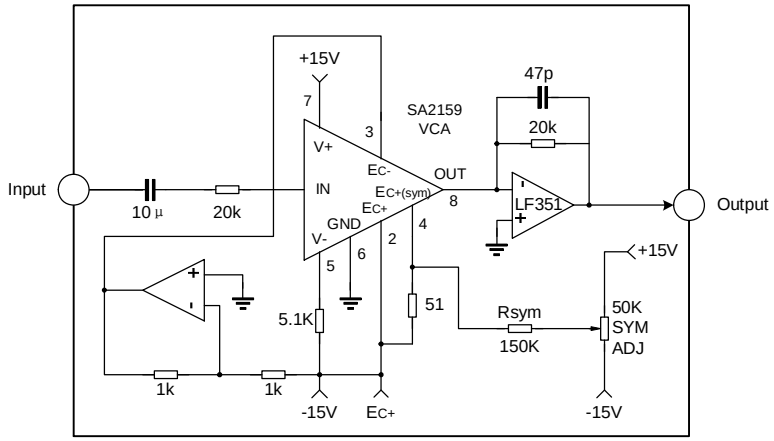


Figure 10. Using both control ports (differential drive)

Noise considerations

For good audio designers, it is important to consider the effects of noisy devices on the signal path. As is well known, this includes not only active devices, but also impedance. High value resistors have inherent thermal noise. And the wrong choice of impedance levels will easily bring on the noise performance of an otherwise quiet circuit being spoiled.

However, the effect of noisy circuitry and high impedance levels in the control path of voltage-control circuitry is easily neglected. When no signal is present at the signal input, The SA2159 VCA noise at the control input is rejected like double-balanced multipliers. Most everyone measures noise in the absence of signal, so noise of control circuitry is often neglected. However, noise at the control port of these parts will cause noise modulation of the signal. If driving the control ports is not quiet signals, this problem will become very grave.

Quiet electronics throughout be control-voltage circuitry can be used to avoid excessive noise. One useful technique is to process control voltages at a multiple of the eventual control constant (e.g., 59mV/dB –ten times higher than the VCA requires). And then attenuate the control signal just before the final drive amplifier. It is necessary to pay attention to Impedance levels and noisy op amps.

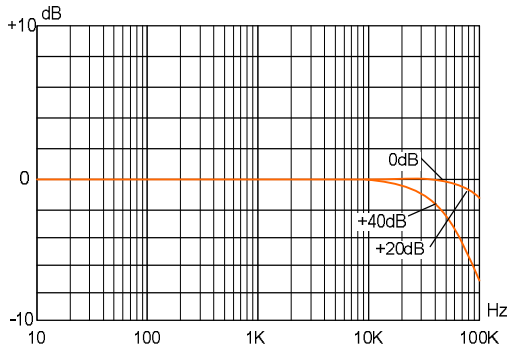


Figure 11. Typical frequency response vs. gain

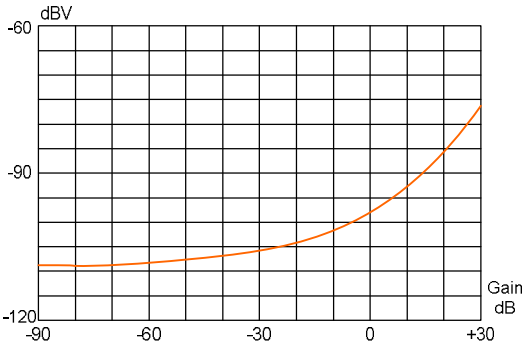
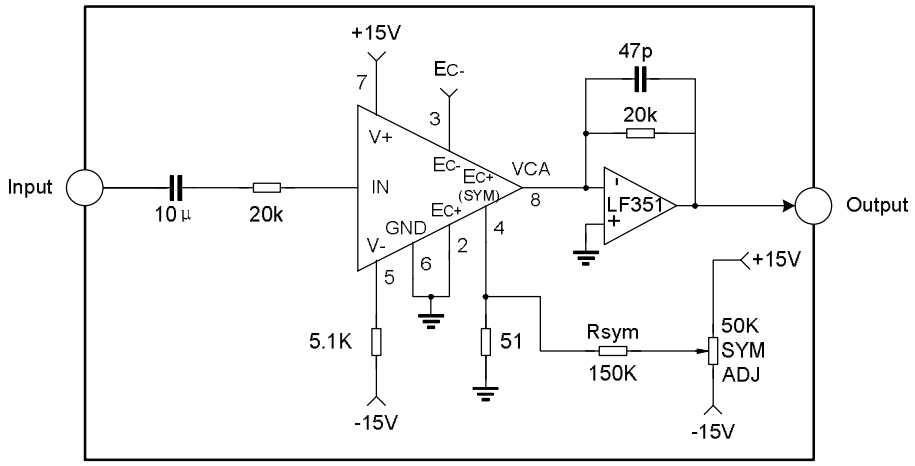


Figure 12. Typical noise (20kHz NBW) vs. gain

TYPICAL APPLICATION CIRCUIT



PACKAGE OUTLINE

SIP-8 Unit: mm