SA23002A

5.5V, 2A Single Synchronous Buck Converter

General Description

The SA23002A is a synchronous Buck converter with built-in power MOSFETs to supply adjustable power voltage requests. The device is capable of providing up to 2A of output current.

The SA23002A has an input voltage range of 2.8V to 5.5V. It could work with up to 2.35MHz switching frequency, due to which small inductor is applicable.

Ordering Information

SA23002 □(□□ □)

Package Code

Optional Spec Code

Ordering Number	Package Type	Note
SA23002ADFD	DFN2×2-8	----

Key Features

- AEC-Q100-Grade 1 -40°C ~125°C
- 2.8V to 5.5V Input Voltage Range
- External Adjustable Voltage with ±1.5% Reference Accuracy
- Typical 1μA Shut Down Current
- Fixed 2.35MHz Switching Frequency
- PWM and PFM Operating Selectable
- 100% Duty Cycle for Lowest Dropout
- Cycle by Cycle Current Limit Protection
- Hiccup-Mode Short-Circuit Protection
- Thermal Shutdown
- Package: DFN2×2-8

Applications

- Automotive Infotainment and Cluster
- Advanced Driver Assistance System (ADAS)
- Automotive Display
- Other Electronic Equipment

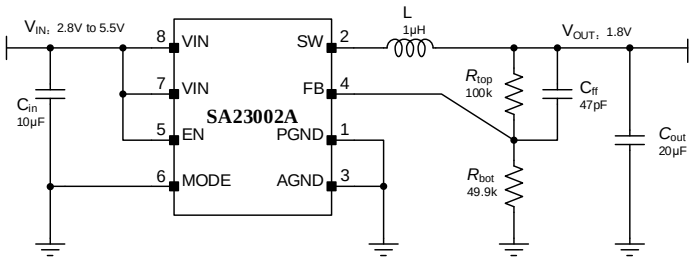


Figure 1. Schematic Diagram

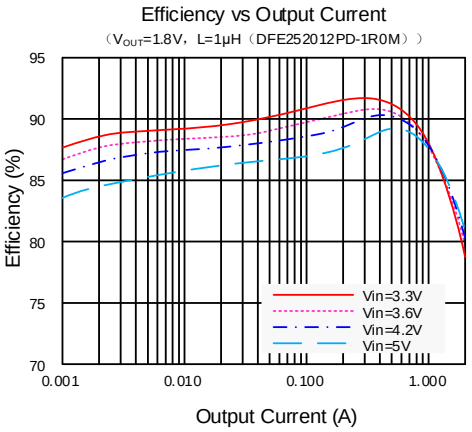


Figure 2. Efficiency vs Output Current

Block Diagram

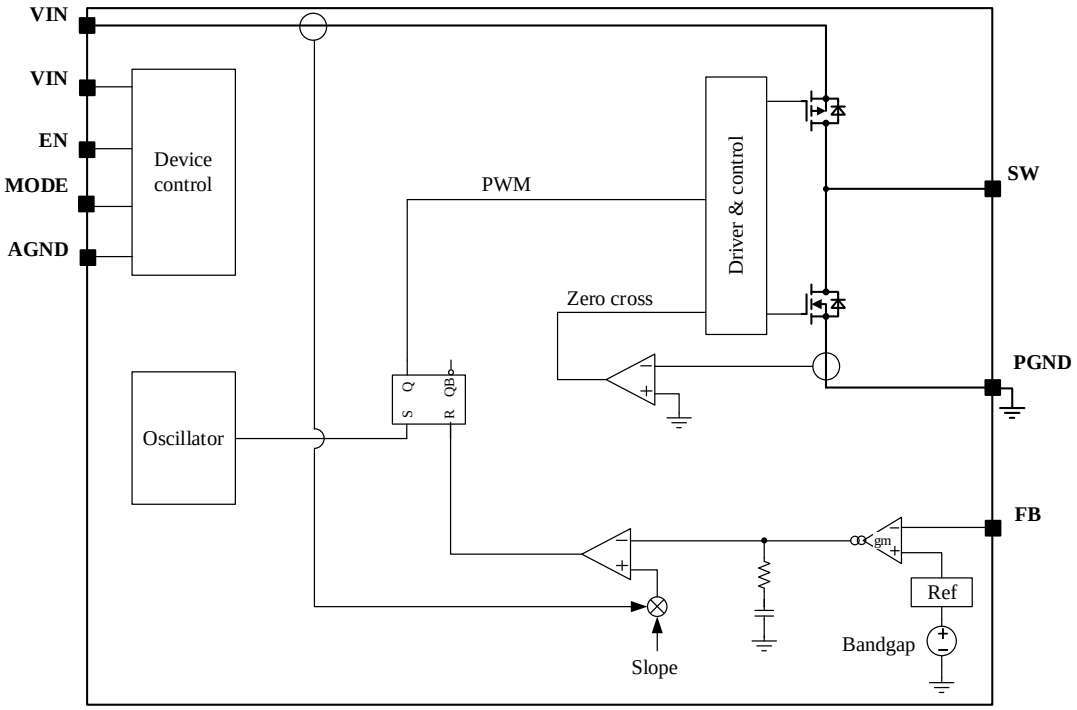
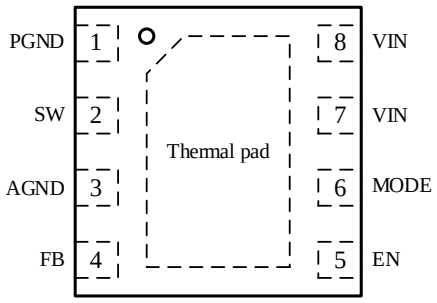


Figure 3. Functional Block Diagram

Pin-Out (Top View)



(DFN2×2-8)

Top Mark: **FFW*xyz*** **(**Device code:FFW, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
PGND	1	Power ground.
SW	2	Switching node.
AGND	3	Analog ground.
FB	4	Output voltage feedback pin. The output voltage reference is 0.6V.
EN	5	Device enable pin, logic high enable. There is no pull down resistor inside, do not leave it floating, and pull-up resistor should be less than 500kΩ.
MODE	6	PFM/FCCM Mode selection. When the MODE pin is high, the device is forced to operate in FCCM. When the pin is low, the device enters PFM in light load. There is no pull down resistor inside, do not leave it floating.
VIN	7，8	VIN power supply.

Absolute Maximum Ratings (Note 1)

VIN ---------- -0.3V to 6.5V
FB, EN, MODE, ---------- -0.3V to VIN+0.3V
Dynamic SW to GND voltage in 20ns Duration ---------- -3V to VIN+1.5V
Power Dissipation, P_D @ T_A = 25℃ ---------- 2.2W
Package Thermal Resistance (Note 2)
θ_{JA}---------- 56.5°C/W
θ_{JC_bot}---------- 14.5°C/W
Ψ_{JT} ---------- 3.5°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility
HBM (Human Body Mode) ----------2000V
CDM(Charge Device Mode)All pins----------500V

Recommended Operating Conditions (Note 3)

VIN ----------2.8V to 5.5V
Ambient Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(2.8V≤V_{IN}≤5.5V, -40°C≤T_j≤125°C. typical values at V_{IN}=5V and T_j=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN						
UVLO Rising Threshold	V_{UVLO_R}		2.6	2.7	2.8	V
UVLO Falling Threshold	V_{UVLO_F}		2.45	2.55	2.65	V
Shut Down Current A	I_{SDA}	V_{EN}=0V,T_j=25°C		1	2	μA
Shut Down Current B	I_{SDB}	V_{EN}=0V,T_j=125°C		6	12	μA
Quiescent Current	I_Q	V_{EN}=1.5V, no load, PFM		22	35	μA
EN						
EN Logic '1'Threshold	V_{EN_H}		1.2			V
EN Logic '0'Threshold	V_{EN_L}				0.4	V
Power Stage						
Switching Frequency	f_{sw}		2	2.35	2.7	MHz
HS FET Rdson	R_{dson_HS}	V_{IN}=5V		120		mΩ
LS FET Rdson	R_{dson_LS}	V_{IN}=5V		85		mΩ
Discharge Resistor	$R_{discharge}$			200		Ω
FB& SS						
Output Feedback Reference	V_{ref}		591	600	609	mV
Soft-start Time	T_{SS}	T_j=25°C	0.1	0.2	0.5	ms
Mode						
Input Bias Current	I_{IN}			0.01	1	μA
Logic '1'Threshold	V_{MODE_H}		1.2			V
Logic '0'Threshold	V_{MODE_L}				0.4	V
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		150	165	180	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		10	15	20	°C
Current Limit						
Peak Current Limit	I_{limit_p}		2.8	3.5	4.2	A
Valley Foldback Current Limit	I_{limit_v}		2	2.8	3.5	A
Negative Valley Current Limit	I_{limit_n}		0.7	1.2	1.7	A
Short Circuit Protection						
Short Circuit Threshold	V_{scp}	V_{FB} as percent of V_{REF}	20	30	40	%V_{REF}
Short Circuit Response Time	t_{scp}	From V_{FB}<V_{SCP} to stop switching; No delay on the other side, V_{IN}=5V	5	10	20	μs

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A=25˚C on an 6cm × 6cm two-layer Silergy Evaluation Board with 1oz copper.

Note 3: The device is not guaranteed to electrical parameter outside its recommended operating conditions.

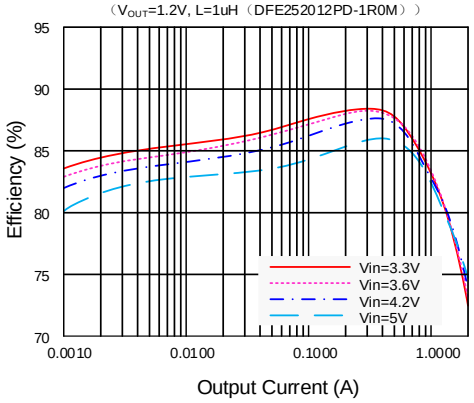
Note 4: Guaranteed by design. Not tested in production.

Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 5V, V_{OUT} =1.8 V, L = 1μH, C_{OUT} = 20μF, unless otherwise noted)

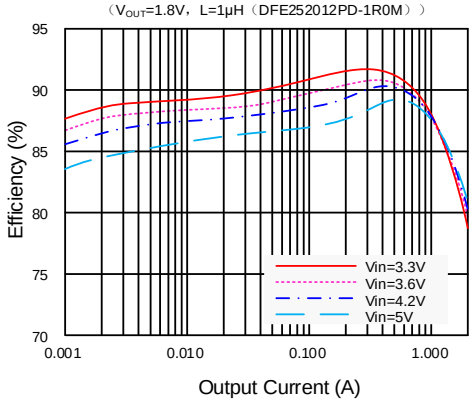
Efficiency vs Output Current

（V_{OUT}=1.2V, L=1uH（DFE252012PD-1R0M））



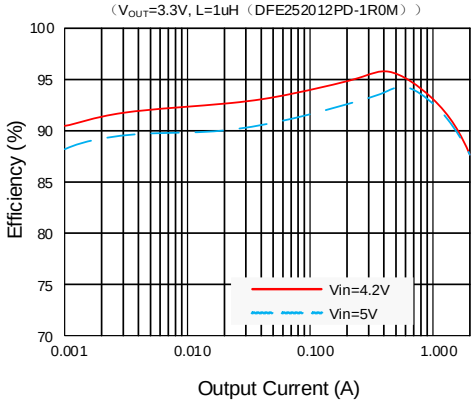
Efficiency vs Output Current

（V_{OUT}=1.8V，L=1μH（DFE252012PD-1R0M））



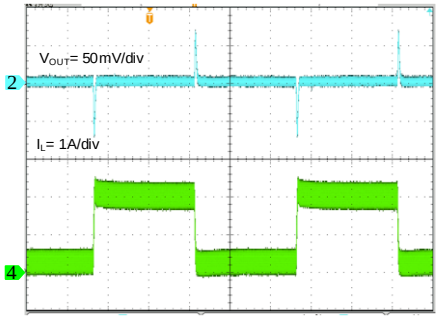
Efficiency vs Output Current

（V_{OUT}=3.3V, L=1uH（DFE252012PD-1R0M））



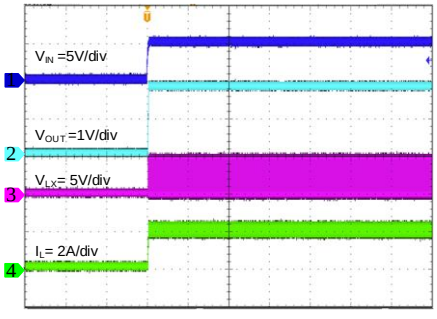
Load Transient Response

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0.2~2A)



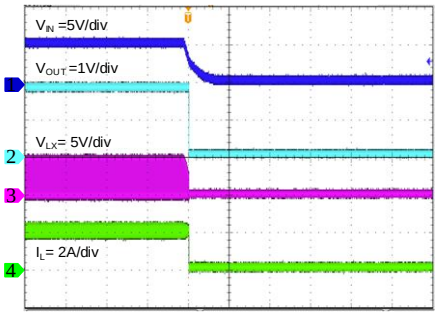
Startup from VIN

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



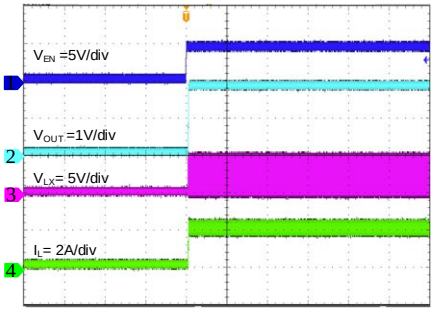
Shutdown from VIN

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Startup from VEN

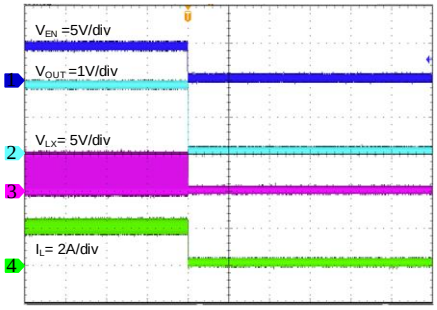
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (10ms/div)

Shutdown from VEN

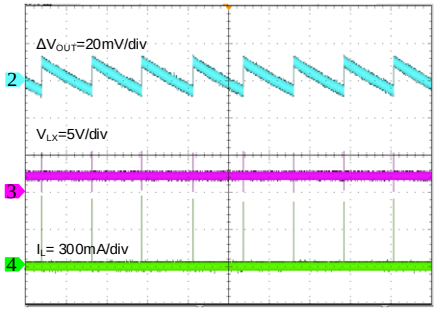
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (10ms/div)

Output Ripple

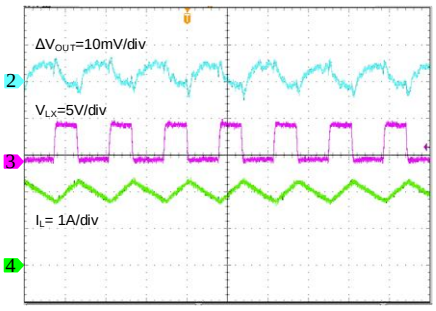
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)



Time (40ms/div)

Output Ripple

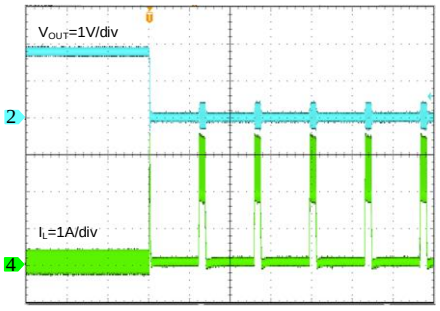
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (400ns/div)

Output Short Circuit

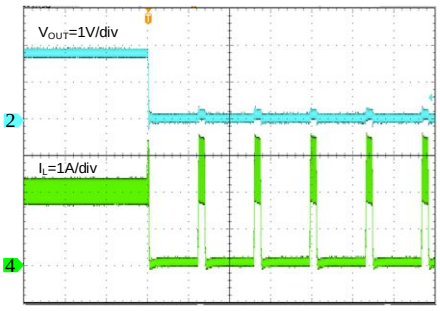
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)



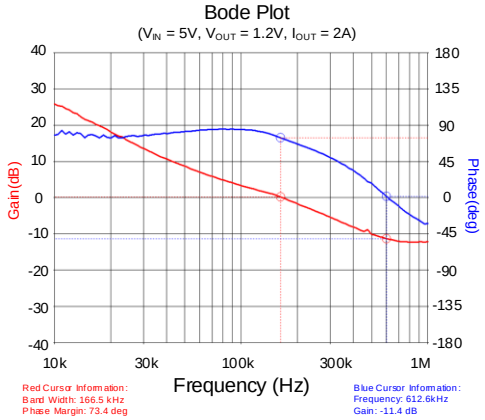
Time (2ms/div)

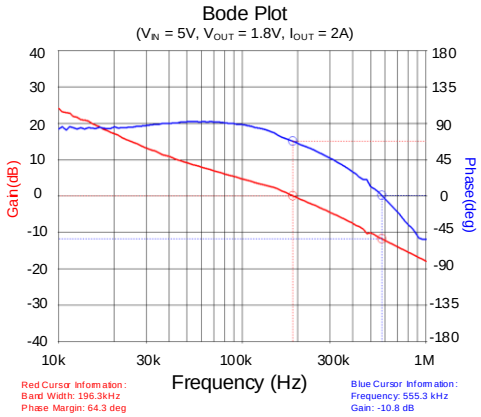
Output Short Circuit

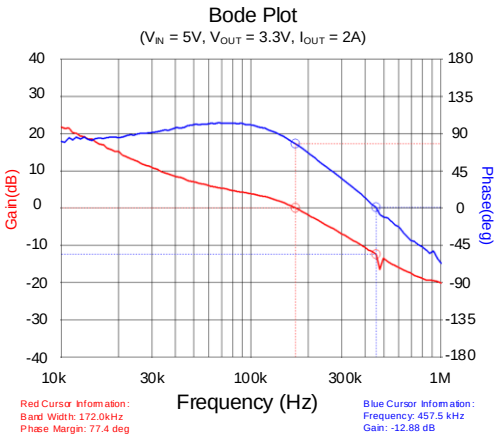
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (2ms/div)







Applications Information

The SA23002A develops a high efficiency synchronous Buck regulator for Automotive Electronics. The device is capable of providing up to 2A of output current.

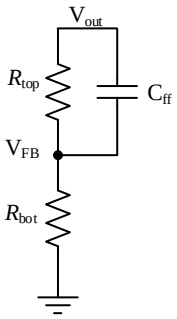
Feedback Resistor Dividers R_{top} and R_{bot}

Choose R_{TOP} and R_{BOT} to program the proper output voltage. Choose large resistance values between 10kΩ and 105kΩ for both R_{TOP} and R_{BOT} to minimize power consumption under light loads (refer to the Typical Application section for recommended feedback Resistor values).

The output voltage can be configured using the following equation:

$$Vout = (1+\frac{R_{top}}{R_{bot}})\times V_{FB}$$

V_{FB} is typically 0.6V.



Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}\times(1-V_{OUT}/V_{IN\_MAX})}{F_S \times I_{OUT\_MAX}\times 40\%}$$

Where Fs is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SA23002A regulator is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected greater than the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT}\times(1-V_{OUT}/V_{IN\_MAX})}{F_S \times L \times 2}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with smaller DCR to achieve a good overall efficiency.

Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT\_MAX}\times\sqrt{D(1-D)}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} = \frac{I_{OUT}\times V_{OUT}\times(V_{IN}-V_{OUT})}{\Delta V_{IN}\times F_s\times\eta\times V_{IN}^2}$$

ΔV_{IN} is desired input voltage ripple

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor really close to the VIN and GND pins. Care should be taken to minimize the loop area formed by CIN, and VIN/GND pins. In this case, a 10uF(0603) low ESR ceramic capacitor is recommended, and there is no need to place a 100nF ceramic capacitor between SA23002A and 10uF capacitor.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. It is recommended to use X7R or better grade ceramic capacitor greater than 20μF capacitance.

Peak Current Mode Control

The Buck regulator provides a supply voltage lower than input voltage. The PWM controller measures the output voltage via a resistor divider connected between Pin FB and ground, and determines the appropriate pulse width duty cycle (on time).

The SA23002A incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as a fixed−frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and the error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse-by-pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows for a simpler compensation.

ON-OFF Sequence

When the device is enabled and the input voltage is above the UVLO threshold, the internal reference is activated and the analog circuits are settled. Afterwards, the soft-start is activated and the output voltage is ramped up.

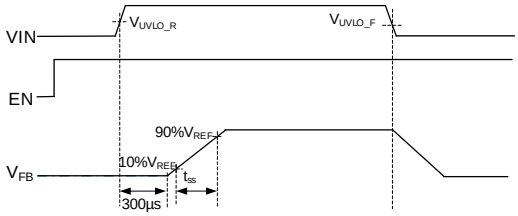


Figure 4. VIN ON/OFF Sequence

The device is enabled by setting the EN pin high. When the input voltage is above the UVLO threshold and the device is enabled, the output voltage ramps up from 10% to 90% of nominal value with t_{SS} of 200μs (typical).

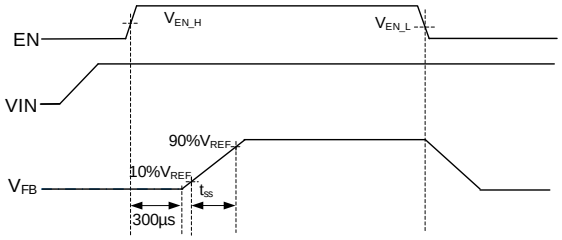


Figure 5. EN ON/OFF Sequence

Adaptive Frequency Fold-back at Min Toff Operation (Dropout)

The SA23002A provides adaptive frequency decreasing function during large duty condition when min Toff happens. Different from the traditional peak current control mode, it ensures the stability of the circuit in dropout condition. When VIN drops below configured VOUT voltage, the SA23002A will enter dropout mode where its high-side FET will always ON.

Light Load Operation

The device supports automatic PWM/PFM operation by external MODE pin. The converter operates in regulated frequency PWM mode at the medium to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Protection Features

The SA23002A has integrated output short circuit protection, output over voltage protection, output over current protection and thermal shutdown protection features.

Table 1. Protection Features

Protection	Threshold	Deglitch Time	Operation
Thermal Shutdown	Rising: 165℃ Falling: 150℃	-	Shutdown when temperature>165℃ Restart when temperature<150℃
Cycle by Cycle Current Limit	3.5A		Peak limit = valley limit; Valley Foldback to 80% after 3 cycles.
Output SCP	V_{FB}<30%V_{REF}	10us	Hiccup per 2.5ms.

Current Limit

The device features cycle by cycle current limit protections. When the current sense amplifier detects a voltage above the peak current limit, the peak current limit causes the HS FET to turn off for the remainder of the cycle.

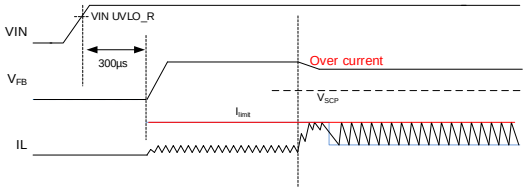


Figure 6. Cycle by Cycle Current Limit

Short Circuit Protection

The device will attempt to protect the power MOSFET from damage. When the output voltage falls below the short circuit threshold, after the initial short circuit blanking time, the device will remain off for the hiccup time and then go through the soft-start.

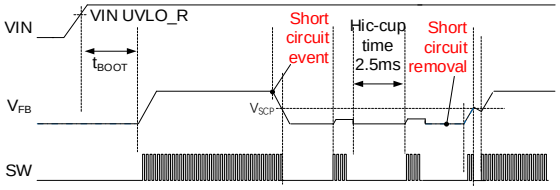


Figure 7. Short Circuit Protection

Over Temperature Protection

The device provides thermal shutdown protection. The device goes into thermal shutdown when the junction temperature exceeds typically 165℃, in this mode, the HS switch and LS switch are turned off. When the junction temperature falls below typically 150℃, the buck will be re-enabled automatically.

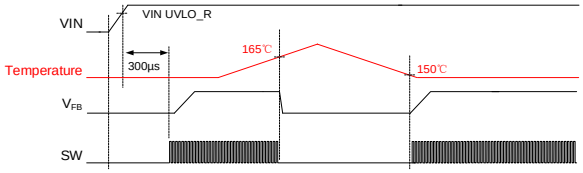
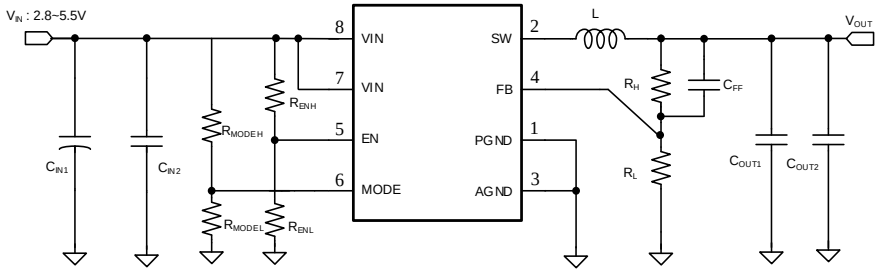


Figure 8. Over Temperature Protection

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V Electrolytic Capacitor		
C_{IN2}, C_{OUT1}, C_{OUT2}	10μF/6.3V/X7T, 0603	GCM188D70J106ME36D	muRata
L	1μH/inductor,3.2A	DFE252012PD-1R0M	muRata
C_{FF}	47pF/50V/C0G, 0603		
R_H	100kΩ, 1%, 0603		
R_L	49.9kΩ, 1%, 0603		
R_{MODEH}	10kΩ, 1%, 0603		
R_{MODEL}	1MΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommended Component Values for Typical Applications

Table 1. Setting the Output Voltage (C_{OUT} ≥ 20μF, V_{OUT} ≥ 0.6V)

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
0.6	0	NC	NC	1.0μH/DFE252012PD-1R0M	10μF*3/6.3V, 0603, X7T
0.8	10	30	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
0.9	15	30	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.0	20	30	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.1	20	24	68	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.2	51	51	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.5	30	20	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.8	100	49.9	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
2.5	105	33	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
3.3	100	22.1	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T

Table 2. Setting the Output Voltage (C_{OUT} = 10μF, V_{OUT} ≥ 1.2V)

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
1.2	10	10	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
1.5	30	20	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
1.8	30	15	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
2.5	47.5	15	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
3.3	100	22.1	10	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T

Layout Design

The layout design of SA23002A is very important for proper operation. Following are the tips for good PCB layout.

- It is desirable to maximize the PCB copper area connected to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- The PCB copper area associated with SW pin must be minimized to avoid the potential noise problem.
- The feedback components R_{top} and R_{bot}, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem.

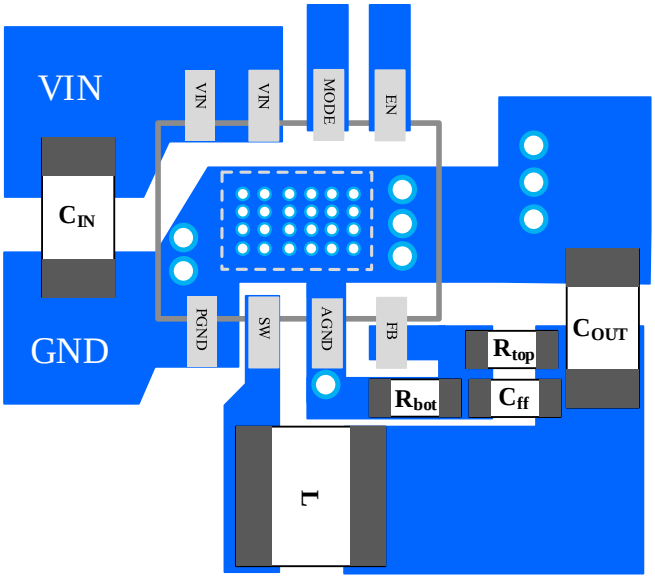
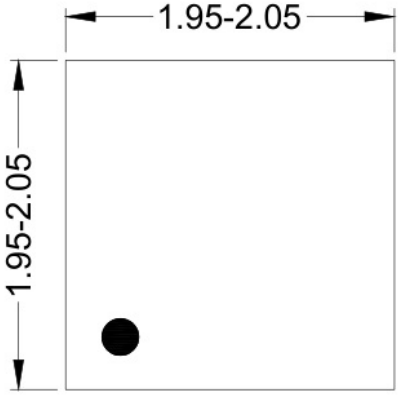
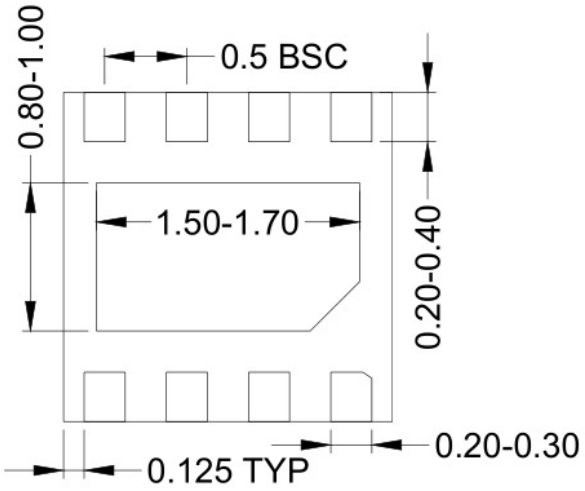


Figure 9. Layout Design

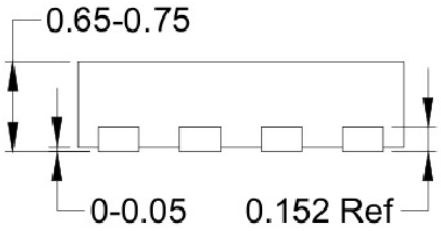
DFN2×2-8 Package Outline Drawing



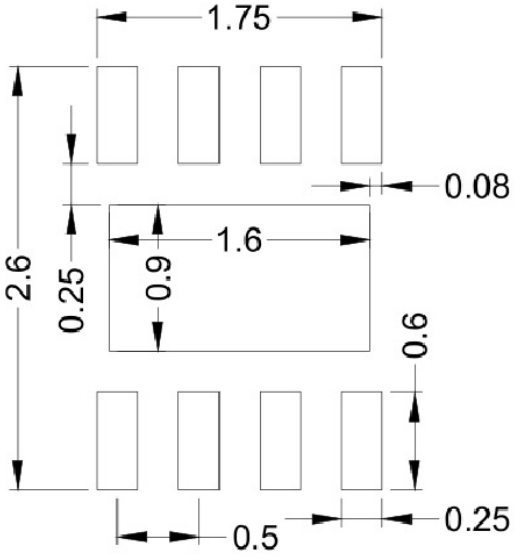
Top View



Bottom View



Side View



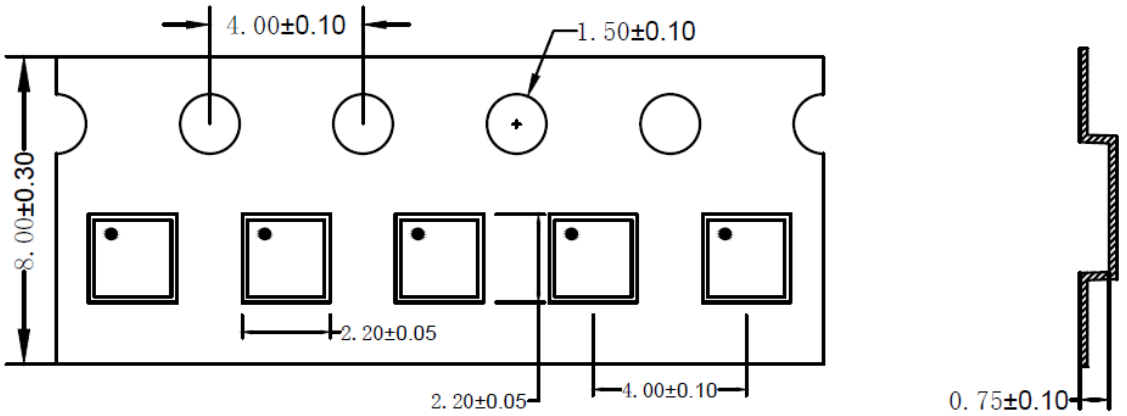
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

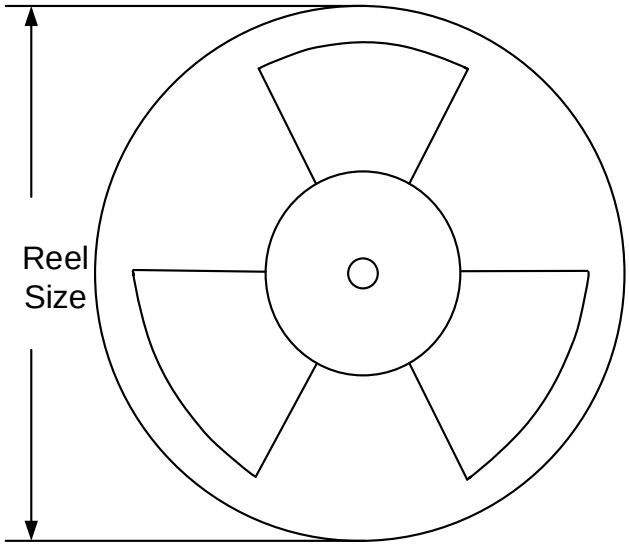
Taping & Reel Specification

1. Taping Orientation

DFN2×2



2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2×2	8	4	7"	400	400	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jul. 11, 2023	Revision 0.9	Initial Release.
Oct. 09, 2023	Revision 0.9A	1. Add the application circuit diagram and recommended parameters. 2. Add Bode Plots. 3. Modify the descriptions of Absolute Maximum Ratings and Recommended 4. Modify the recommended input voltage range and ISD current description. 5. Modify the recommended voltage divider range. 6. Modify the short circuit waveform description. 7. Add description of ON-OFF sequence. 8. Add description of peak current mode. 9. Modify operation mode from PSM to PFM of Key Features in page 1. 10. Modify the description of thermal resistance test condition. 11. Modify the description of Current limit and Short Circuit Protection.

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