SA23002B

High-Efficiency, 5.5V, 2A Single Synchronous Buck Converter

General Description

The SA23002B high efficiency 2.35MHz synchronous buck converter operates over an input voltage range of 2.8V to 5.5V and can deliver an output current up to 2A. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss. The 2.35MHz constant switching frequency reduces the required external inductor and capacitor values.

The SA23002B uses a peak current mode control architecture. It operates in fixed frequency pulse width modulation (PWM) mode at medium to heavy loads, and in pulse frequency modulation (PFM) mode during light loads, thereby maintaining high efficiency over the entire load current range. It also provides cycle-by-cycle current limit protection, output short-circuit protection, and overtemperature protection.

The SA23002B is available in a compact DFN2x2-8 package. The device is part of a family which shares the same package and pinout. The other parts in the family is: SA23002CDFD (2A output current, FCCM operating during light load).

Key Features

- 2.8V to 5.5V Input Voltage Range
- Up to 2A Output Current
- External Adjustable Voltage with ±1.5% Reference Accuracy
- 1μA Shutdown Current (Typical)
- Fixed 2.35MHz Switching Frequency
- 100% Duty-Cycle Capable
- PFM Mode for High Efficiency at Light Load
- Cycle-by-Cycle Current Limit Protection
- Hiccup Mode Short-Circuit Protection
- Power Good Indicator
- Thermal Shutdown
- Compact DFN2×2-8 Package
- AEC-Q100 Qualified for Automotive Applications

Applications

- Automotive Infotainment and Cluster
- Advanced Driver Assistance System (ADAS)
- Automotive Display
- Other Electronic Equipment

Typical Application

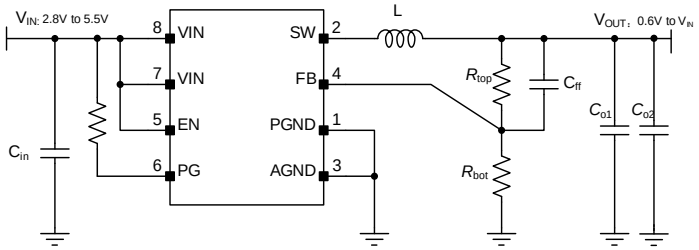


Figure 1. Schematic Diagram

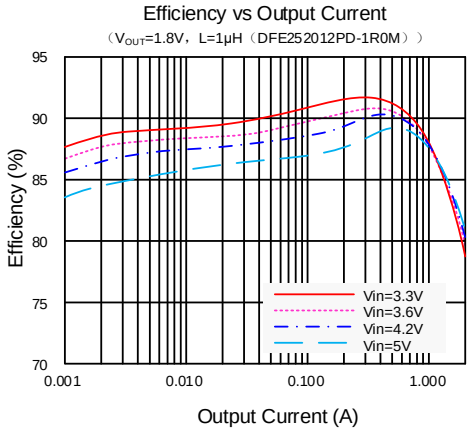


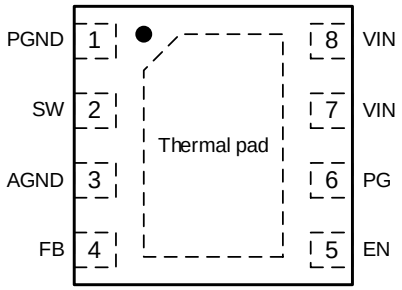
Figure 2. Efficiency vs Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SA23002BDFD	DFN2×2-8 RoHS-Compliant and Halogen-Free	**FFYxyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



(DFN2×2-8)

Pin Description

Pin No	Pin Name	Pin Description
1	PGND	Power ground.
2	SW	Inductor pin. Connect this pin to the switching node of inductor.
3	AGND	Analog ground.
4	FB	Output voltage feedback pin. The output voltage reference is 0.6V.
5	EN	Device enable pin. Logic high enable. There is no internal pulldown resistor; do not leave floating.
6	PG	Power good pin. Open-drain output. A pullup resistor is required (100kΩ, for example).
7, 8	VIN	Power input pin. Decouple this pin from the GND pin with at least a 10μF ceramic capacitor.

Block Diagram

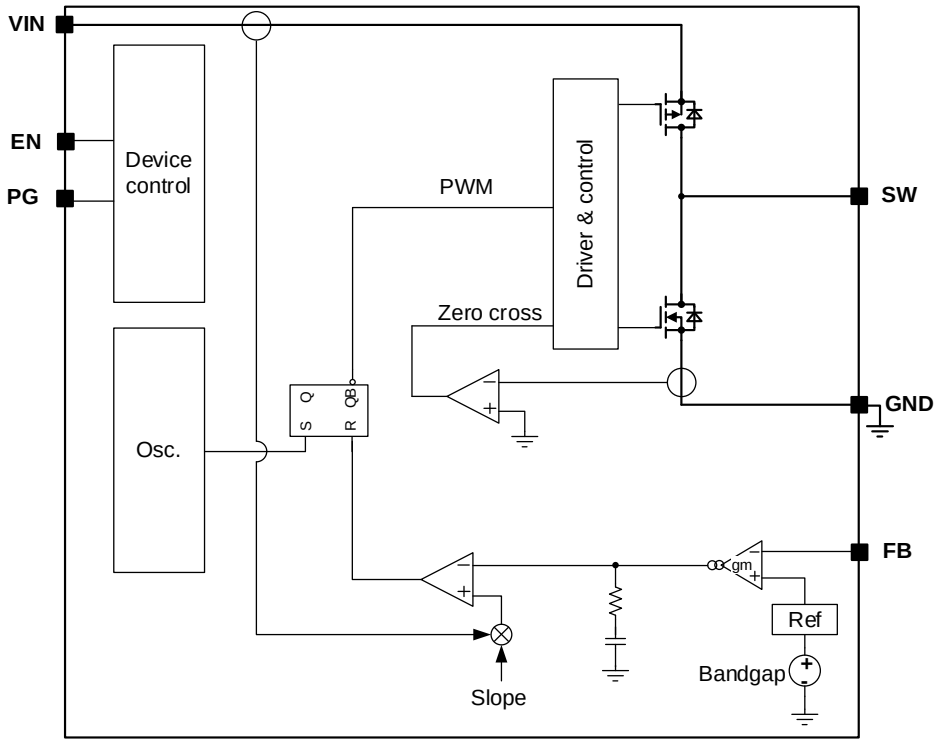


Figure 3. Functional Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN	-0.3	6.5	V
FB, EN, PG	-0.3	VIN+0.3	
Dynamic SW-to-GND Voltage in 20ns Duration	-3	VIN+1.5	
Junction Temperature Range	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-65	150	
ESD Susceptibility			
HBM (Human Body Model)	2000		V
CDM (Charge Device Model) All Pins	500		

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	56.5	°C/W
θ_{JB} Junction-to-Board Thermal Resistance	19	
θ_{JC_TOP} Junction-to-Case (Top) Thermal Resistance	35.1	
Ψ_{JT} Junction-to-Top Characterization Parameter	3.5	
P_D Power Dissipation @ T_A = 25°C	2.2	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	2.8	5.5	V
Ambient Temperature	-40	125	°C
Junction Temperature	-40	150	°C

Electrical Characteristics

(2.8V ≤ VIN ≤ 5.5V, -40°C ≤ T_J ≤ 125°C. typical values at VIN = 5V and T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VIN	UVLO Rising Threshold	V_{UVLO_R}		2.6	2.7	2.8	V
	UVLO Falling Threshold	V_{UVLO_F}		2.45	2.55	2.65	V
	Shutdown Current A	I_{SDA}	EN = 0V, T_J = 25 ºC		1	2	μA
	Shutdown Current B	I_{SDB}	EN = 0V, T_J = 125 ºC		6	12	μA
	Quiescent Current	I_Q	EN = logic high, no load		22	35	μA
EN	EN Logic High Threshold	V_{EN_H}		1.2			V
	EN Logic Low Threshold	V_{EN_L}				0.4	V
Power Stage	Switching Frequency	f_{sw}		2	2.35	2.7	MHz
	HS FET $R_{DS(ON)}$	$R_{DS(ON)\_HS}$			120		mΩ
	LS FET $R_{DS(ON)}$	$R_{DS(ON)\_LS}$			85		mΩ
	Discharge Resistor	$R_{DISCHARGE}$			200		Ω
FB& SS	Output Feedback Reference	V_{REF}		591	600	609	mV
	Soft-Start Time	t_{SS}		0.1	0.2	0.5	ms
PG	Falling (Fault) Voltage	V_{PGTH_FF}	V_{FB} as percent of V_{REF}	80	85	90	%
	Rising (Good) Voltage	V_{PGTH_RG}	V_{FB} as percent of V_{REF}	85	90	95	%
	Rising (Fault) Voltage	V_{PGTH_RF}	V_{FB} as percent of V_{REF}	110	115	120	%
	Falling (Good) Voltage	V_{PGTH_FG}	V_{FB} as percent of V_{REF}	105	110	115	%
	Delay Time	t_{PG_DELAY}			17		μs
Thermal Shutdown	Thermal Shutdown Threshold	T_{SD}		150	165	180	ºC
	Thermal Shutdown Hysteresis	T_{SDHYS}		10	15	20	ºC
Current Limit	Peak Current Limit	I_{LIMIT_P}		2.8	3.5	4.2	A
	Valley Foldback Current Limit	I_{LIMIT_V}		2	2.8	3.5	A
	Negative Valley Current Limit	I_{LIMIT_N}		0.7	1.2	1.7	A
Short-Circuit Protection	Short-Circuit Threshold	V_{SCP}	V_{FB} as percent of V_{REF}	20	30	40	%V_{REF}
	Short-Circuit Response Time	t_{SCP}	From V_{FB} < V_{SCP} to stop switching; No delay on the other side, VIN = 5V	5	10	20	μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistances are measured in the natural convection at T_A = 25˚C on a 6cm × 6cm two-layer Silergy Evaluation Board with 1oz copper.

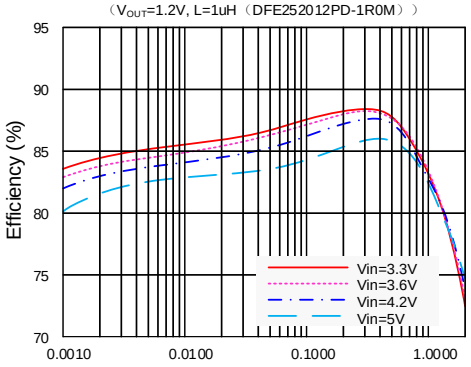
Note 3: The device is not guaranteed for electrical parameters outside the test conditions listed in the Electrical Characteristics Table.

Typical Performance Characteristics

(T_A = 25°C, VIN = 5V, V_{OUT} = 1.8 V, L = 1μH, C_{OUT} = 20μF, unless otherwise noted)

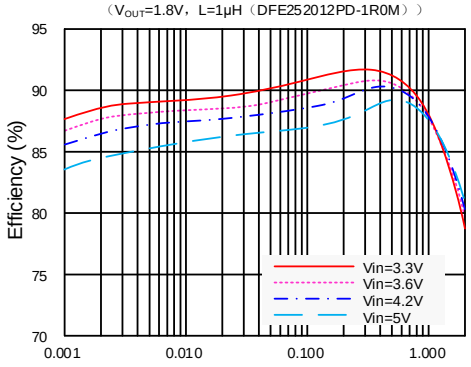
Efficiency vs Output Current

(V_{OUT}=1.2V, L=1uH（DFE252012PD-1R0M））



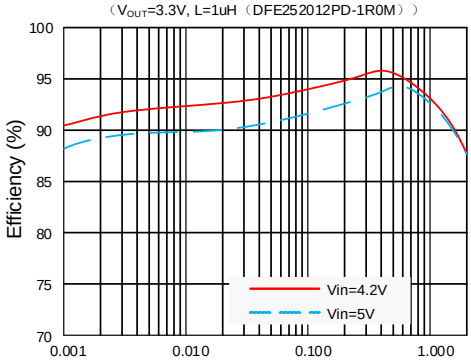
Efficiency vs Output Current

(V_{OUT}=1.8V，L=1μH（DFE252012PD-1R0M））



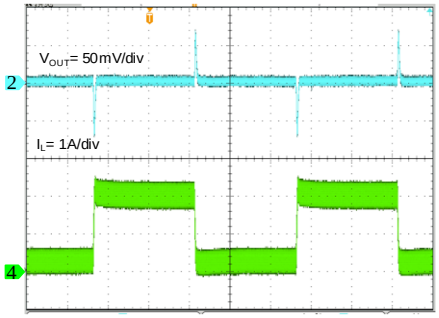
Efficiency vs Output Current

(V_{OUT}=3.3V, L=1uH（DFE252012PD-1R0M））



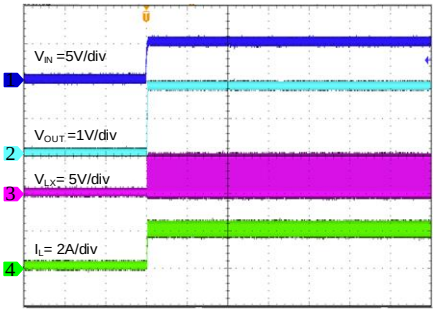
Load Transient Response

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0.2~2A)



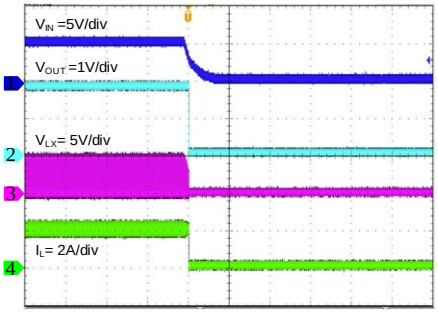
Startup from VIN

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



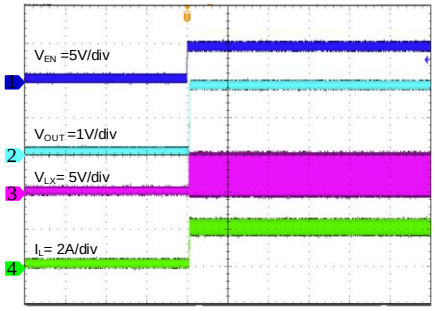
Shutdown from VIN

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Startup from VEN

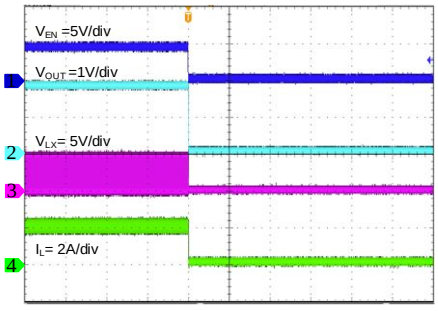
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (10ms/div)

Shutdown from VEN

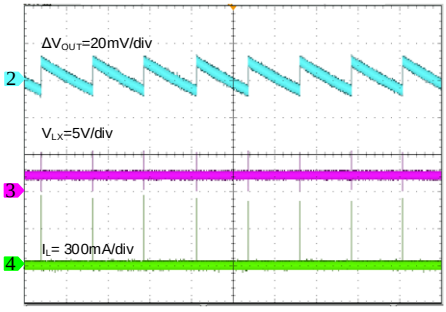
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (10ms/div)

Output Ripple

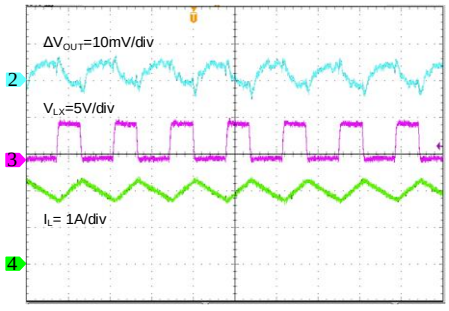
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)



Time (40ms/div)

Output Ripple

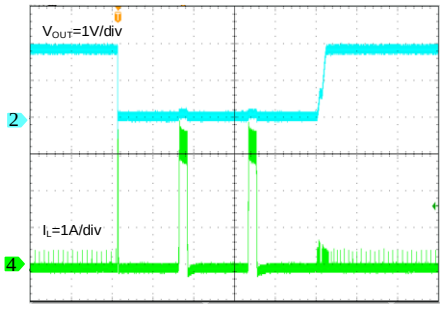
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (400ns/div)

Output Short Circuit

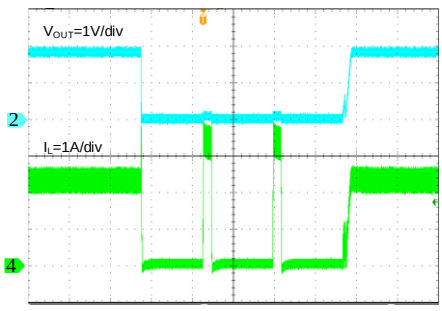
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)



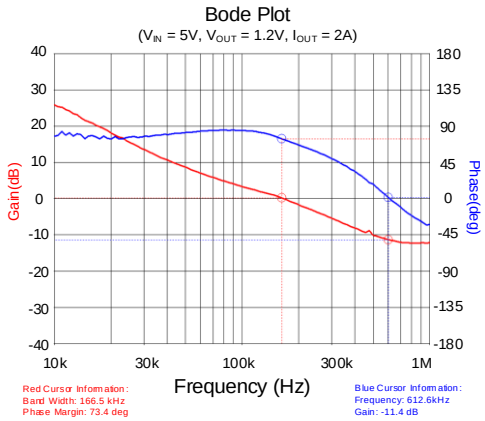
Time (2ms/div)

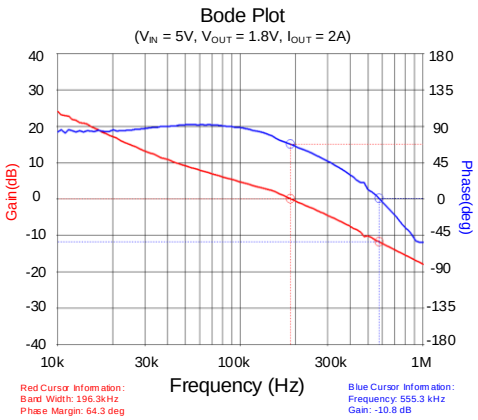
Output Short Circuit

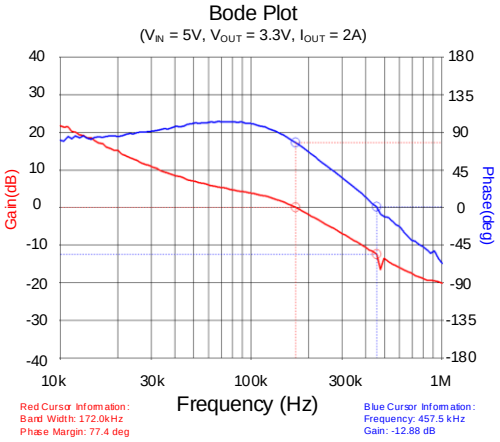
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (2ms/div)







Detailed Description

General Description

The SA23002B high efficiency 2.35MHz synchronous buck converter operates over an input voltage range of 2.8V to 5.5V and can deliver an output current up to 2A. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss. The 2.35MHz constant switching frequency reduces the required external inductor and capacitor values.

The SA23002B also provides cycle-by-cycle current limit protection, output short-circuit protection, and overtemperature protection.

Peak Current Mode Control

The SA23002B uses a fixed frequency peak current mode control architecture. The peak current through the high side MOSFET is added to the slope compensation ramp and fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input. The output of the error amplifier is fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch by using the switch logic block. This forces a high signal on the gate of the high side MOSFET, and the high side MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the high side MOSFET turns off.

ON-OFF Sequence

The normal startup of the chip is determined by two factors: EN pin level is higher than the logic high level threshold and the VIN voltage is higher than the UVLO rising threshold value. After the EN pin level is set high, the voltage at the VIN pin determines whether the chip is turned on. Once the VIN voltage is higher than the UVLO rising threshold value, the internal reference voltage is enabled and the functional circuit begins operating. After a 300μs delay, the soft-start circuit begins operating and the SW node begins switching. After the fixed soft-start time, the output reaches the target value.

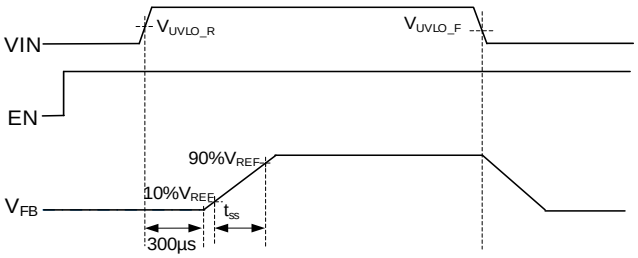


Figure 4. VIN ON/OFF Sequence

When the VIN pin voltage is higher than 2.7V (typical), the EN pin voltage determines whether the chip begins operating. When the EN pin voltage is above the logic high level threshold, the internal reference voltage is enabled and the device begins operating. After a 300μs delay, the soft-start circuit begins operating and the SW node begins switching. After the fixed soft-start time, the output reaches the target value.

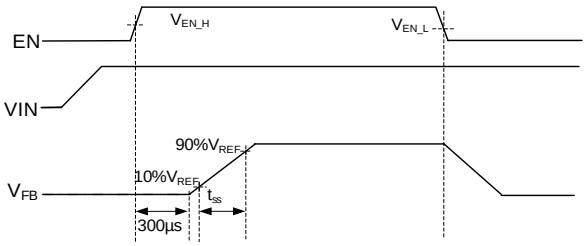


Figure 5. EN ON/OFF Sequence

Adaptive Frequency Foldback at Minimum T_{OFF} Operation (Dropout)

The SA23002B provides adaptive frequency reduction during large-duty-cycle operation when minimum T_{OFF} is reached. Unlike conventional peak current control, this approach ensures the stability of the circuit during dropout operation. When VIN voltage drops below the configured V_{OUT} voltage, the SA23002B will enter dropout mode, wherein its high side MOSFET will always be on. Normal operation resumes when VIN voltage exceeds the target V_{OUT} level.

Power Good

The SA23002B provides an external PG pin for power good indication. PG remains low until the internal soft-start is complete. When the FB pin voltage is between V_{PGTH_RG} and V_{PGTH_FG}, the PG pin open-drain MOSFET turns off, and the output is pulled high by the external resistor connected to the source. In addition, when the FB pin voltage exceeds V_{PGTH_FF} and V_{PGTH_RF}, the open-drain MOSFET turns on and the PG pin is pulled low.

A pullup resistor value of 2kΩ to 100kΩ connected to an external power source is recommended.

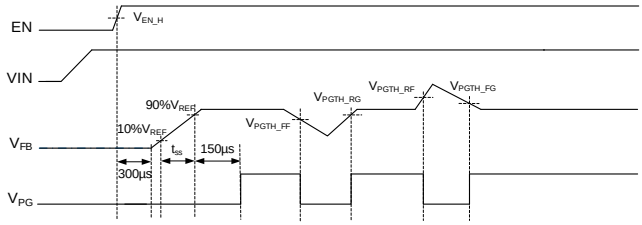


Figure 6. Power Good Logic

Soft-Start

The SA23002B features soft-start to ensure moderate inrush current and reduce output overshoot. The soft-start circuit charges a capacitor with a fixed current to ramp up the reference voltage. The soft-start time is fixed by an internal capacitor.

Table 1. Soft-Start

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Soft-Start Time	t_{SS}	Output from 10% to 90%		0.2		ms
Startup Delay Time	t_{DELAY}	Time from EN high to soft-start		300		μs

Fault Protection Modes

The SA23002B provides integrated output short-circuit protection, output overcurrent protection, and thermal shutdown protection.

Table 2. Fault Protection Modes

Protection	Threshold	Deglitch Time	Operation
Thermal Shutdown	Rising: 165°C Falling: 150°C	–	Shutdown when temperature >165°C. Restart when temperature <150°C.
Cycle-by-Cycle Current Limit	3.5A	–	Peak limit = valley limit. Valley foldback to 80% after 3 cycles.
Output SCP	V_{FB} < 30% V_{REF}	10μs	Hiccup time = 3.5ms.

Cycle-by-Cycle Current Limit Protection

The SA23002B features cycle-by-cycle current limit protection. The internal high side and low side MOSFET current sense signals and peak/valley current limit reference voltages are fed to the positive and negative ends of the current limiting comparator, respectively. When V_{FB} exceeds V_{SCP} and three consecutive peak current limits are detected, the valley current limiting reference will be reduced, thus avoiding minimum T_{ON} operation and reducing the power dissipation.

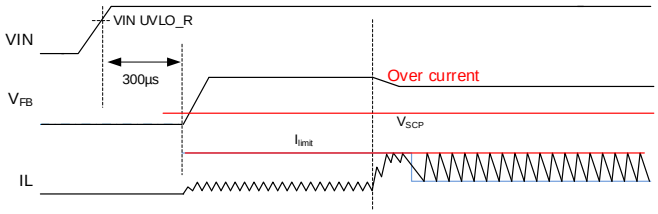


Figure 7. Cycle-by-Cycle Current Limit

Short-Circuit Protection

The SA23002B provides output short-circuit protection to prevent device damage. When the output is short-circuited and the FB voltage is lower than the short-circuit threshold voltage V_{SCP}, the chip will turn off the high side and low side MOSFETs and enter hiccup mode until the fault is removed.

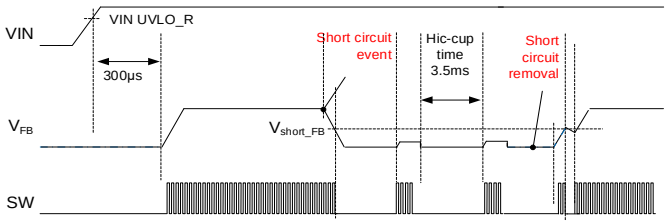


Figure 8. Short-Circuit Protection

Overtemperature Protection

The SA23002B enters thermal shutdown when the junction temperature exceeds 165°C (typical). In this mode, the high side and low side MOSFETs are turned off. When the junction temperature falls below 150°C (typical), the buck converter will automatically restart.

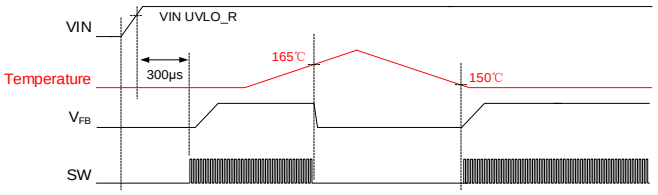


Figure 9. Overtemperature Protection

Application Information

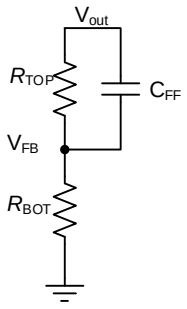
The following sections provide information to help select the external components required to meet the targeted application specifications.

Feedback Resistor Dividers R_{TOP} and R_{BOT}

Choose R_{TOP} and R_{BOT} to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R_{TOP} and R_{BOT} to minimize power consumption under light loads. In order to achieve better load transient performance and phase margin, refer to the Typical Application section for recommended feedback resistor values.

The output voltage can be configured using the following equation:

$$V_{OUT} = \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) \times V_{FB}$$



where V_{FB} has a value of 0.6V (typical).

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_S \times I_{OUT,MAX} \times 0.4}$$

where f_S is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SA23002B has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2f_S \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency. Choose an inductor with smaller DCR to achieve good overall efficiency.

Input Capacitor C_{IN}

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply, and to reduce EMI. When selecting the input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply, and a temperature rating above the system requirements. X7R series ceramic capacitors are most often selected due to their surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a long inductive cable may be susceptible to significant inductive ringing at the input of the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce input overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated as follows:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications, a single 10µF(0603) X7R capacitor is sufficient. Place the ceramic input capacitor as close to the device's VIN and GND pins as possible.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. It is recommended to use an X7R or better grade ceramic capacitor (refer to the Typical Application section for recommended capacitance values).

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

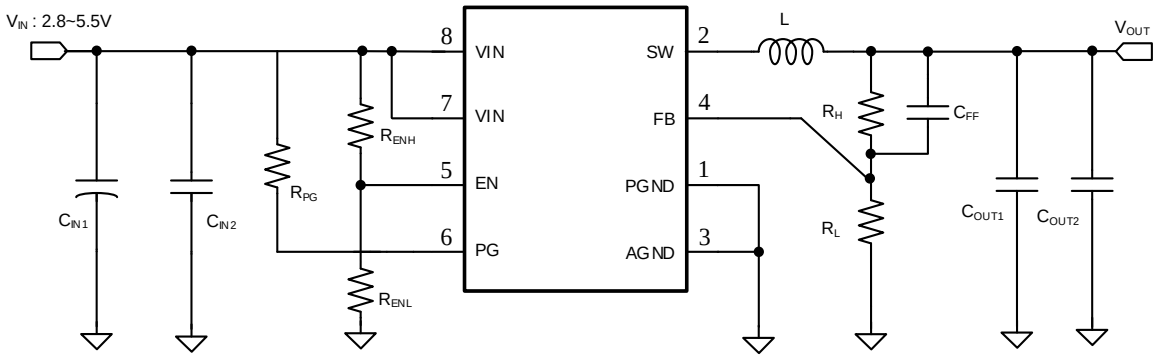
The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple may be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across their terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account. Refer to Table 3 and Table 4 for the recommended capacitor values for different design parameters.

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V Electrolytic Capacitor		
C_{IN2}, C_{OUT1}, C_{OUT2}	10μF/6.3V/X7T, 0603	GCM188D70J106ME36D	muRata
L	1μH/inductor,3.2A	DFE252012PD-1R0M	muRata
C_{FF}	47pF/50V/C0G, 0603		
R_H	100kΩ, 1%, 0603		
R_L	49.9kΩ, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommended Component Values for Typical Applications

Table 3. Setting the Output Voltage (C_{OUT} ≥ 20μF, V_{OUT} ≥ 0.6V)

V_{OUT} (V)	R_H (kΩ)	R_L (kΩ)	C_{FF} (pF)	L/Part Number	C_{OUT}
0.6	0	NC	NC	1.0μH/DFE252012PD-1R0M	10μF*3/6.3V, 0603, X7T
0.8	10	30	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
0.9	15	30	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.0	20	30	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.1	20	24	68	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.2	51	51	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.5	30	20	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.8	100	49.9	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
2.5	105	33	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
3.3	100	22.1	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T

Table 4. Setting the Output Voltage (C_{OUT} = 10μF, V_{OUT} ≥ 1.2V)

V_{OUT} (V)	R_H (kΩ)	R_L (kΩ)	C_{FF} (pF)	L/Part Number	C_{OUT}
1.2	10	10	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
1.5	30	20	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
1.8	30	15	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
2.5	47.5	15	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
3.3	100	22.1	10	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Input Capacitors:** Place the input capacitors as close as possible to the VIN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the VIN and GND pins using a wide copper area.
- **Output Capacitors:** Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of the output voltage.
- **Feedback Network:** Place the feedback components (R_H, R_L, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near SW or other high frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.
- **SW Connection:** Keep the SW area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.
- **EN Signal:** It is not recommended to connect the EN pin directly to VIN. A resistor in the range of 1kΩ to 1MΩ should be used if EN pin is pulled high to VIN voltage.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than the GND pad. Place multiple GND vias for heat dissipation.
- **PCB Board:** To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if possible. Connect the ground pad to a large copper area to enhance thermal performance.

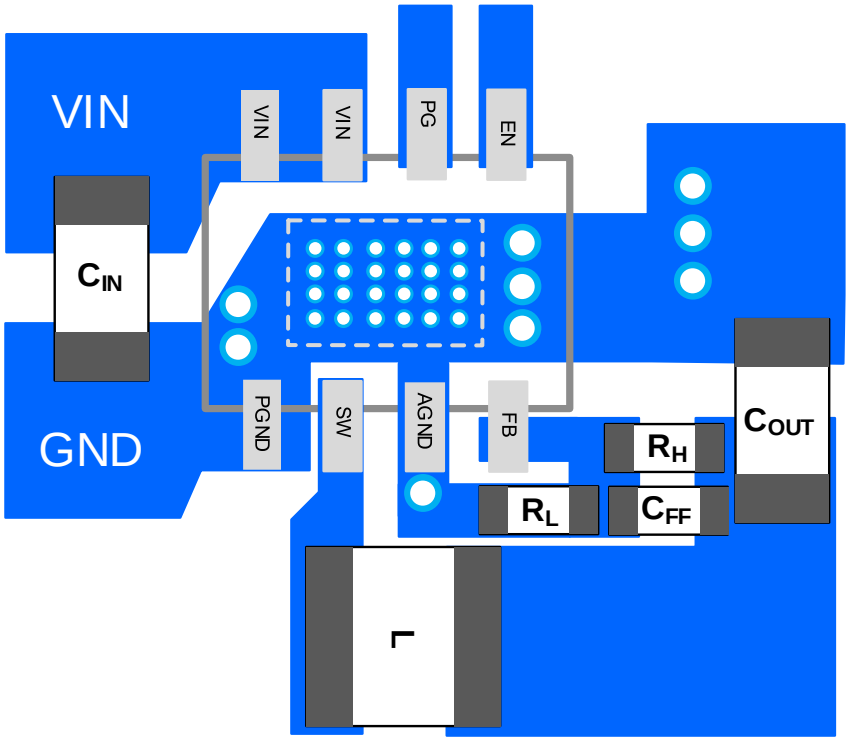
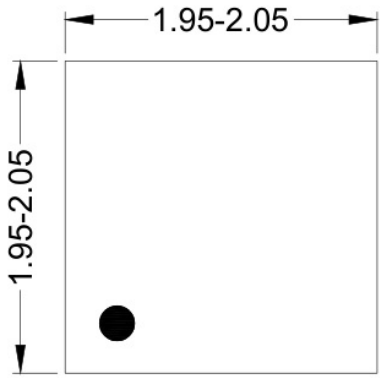
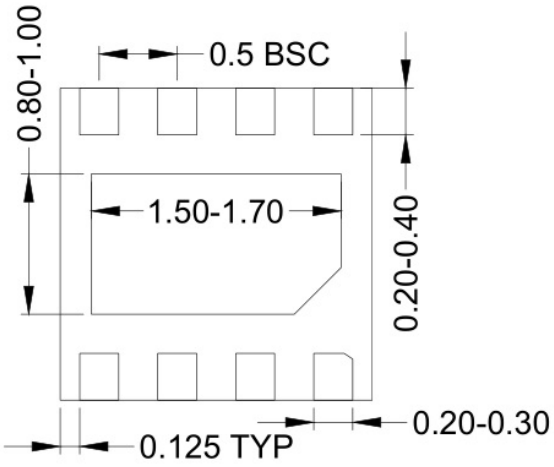


Figure 10. PCB Layout Suggestion

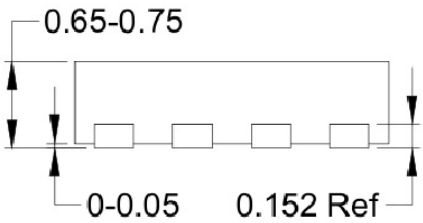
DFN2×2-8 Package Outline Drawing



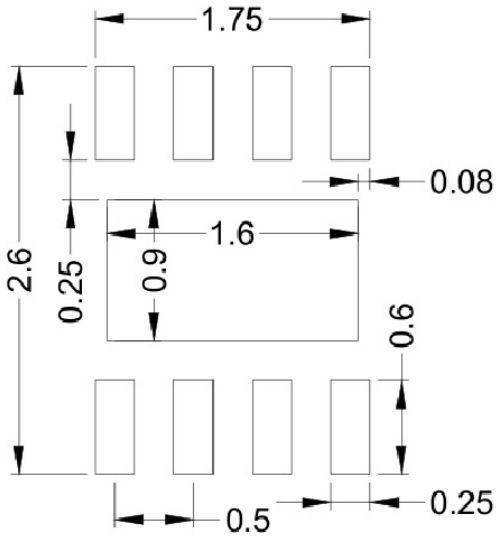
Top View



Bottom View



Side View

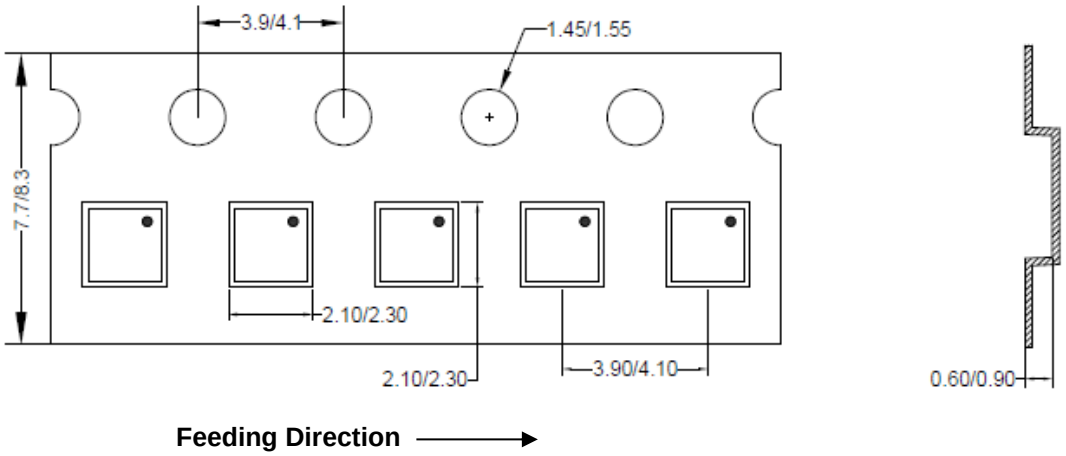


Recommended PCB Layout
(Reference only)

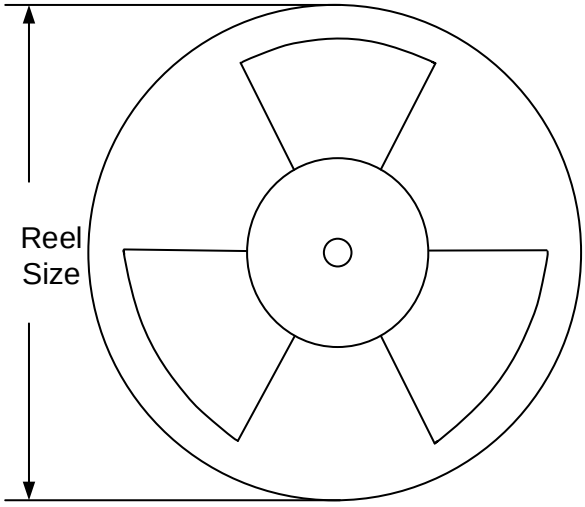
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Tape and Reel Specification

DFN2×2 Taping Orientation



Carrier Tape and Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer * Length (mm)	Leader * Length (mm)	Qty per Reel (pcs)
DFN2×2-8	8	4	7"	280	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Mar. 21, 2024	Revision 1.0	Initial Release	-

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