

VERSATILE SINGLE CHIP TELEPHONE

FEATURES

- Speech circuit, LD/MF Dialler and Tone Ringer on one 28 pin CMOS chip
- Soft clip to avoid harsh distortion
- Line Loss Compensation selectable by pin option
- Power down mode
- Versatile applications for different PTT demands
- 31 digit last number redial
- Sliding Cursor protocol with comparison
- 2 Flash keys, 100 ms and 280 ms (option 600 ms)
- Pause key for 3 sec Auto Pause or Wait Function
- Ring frequency discrimination
- Operating range from 13 to 100 mA (down to 5 mA with reduced performance)
- Low noise (max. -72dBmp)
- Real or Complex impedance on chip programmable
- LD/MF switchable dialling
- On chip MF filter (CEPT CS 203 compatible)
- 3-tone melody generator with selectable repetition rates

GENERAL DESCRIPTION

The SA2532 is a CMOS integrated circuit that contains all the functions needed to form a high performance electronic telephone.

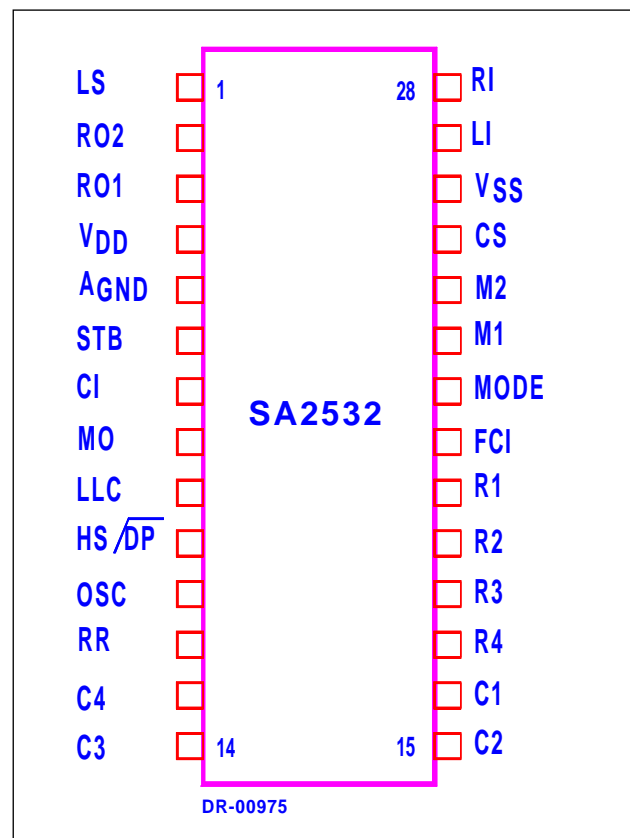
The device incorporates LD/MF dialling, melody generation, ring frequency discrimination and a high quality speech circuit.

A RAM is on chip for a 31 digit last number redial. The sliding cursor procedure makes Last Number Redial easy behind a PABX.

The versatility of the circuit is provided by on chip programmability and a few external components. This allows easy adaption to different PTT requirements without changing the PCB of the telephone.

PACKAGE

Available in 28 pin DIP and SOIC



PIN DESCRIPTION

Pin#	Symbol	Function								
23 24	M1 M2	Microphone Inputs Differential inputs for the microphone (electret).								
3 2	RO1 RO2	Receiver Outputs These are the outputs for driving a dynamic earpiece with an impedance of 100 to 300Ω								
5	A _{GND}	Analog Ground This is the analog ground for the amplifiers.								
28	RI	Receive Input This is the input for the receive signal.								
6	STB	Side Tone Balance Input This is the input for side tone cancellation.								
1	LS	Line Current Sense Input This is the input for sensing the line current.								
27	LI	Line Input This input is used for power extraction and line current sensing.								
25	CS	Current Shunt Control Output This N-channel open drain output controls the external high power shunt transistor for the modulation of the line voltage and for shorting the line during make period of pulse dialling.								
4	V _{DD}	Positive Voltage Supply This is the supply pin for the circuit.								
26	V _{SS}	Negative Power Supply								
8	MO	Melody Output Pulse Density Modulated output of the melody generator for tone ringer. At high impedance when not active.								
21	FCI	Frequency Comparator Input This is a Schmitt trigger input for ring frequency discrimination. Disabled during off-hook.								
10	HS/DP	Hook Switch Input and Dial Pulse Output This is an I/O that is pulled high by the hook switch when off-hook. An open drain pulls it low during break periods of pulse dialling and flash.								
11	OSC	Oscillator Input Oscillator pin for Xtal or ceramic resonator (3.58 MHz).								
9	LLC	Line Loss Compensation Select pin for line loss compensation.								
12	RR	Repetition Rate Select pin for repetition rate of melody.								
22	MODE	Signalling Mode Select Input <table border="1" data-bbox="384 1509 1185 1637"> <thead> <tr> <th>Mode pin</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>High</td> <td>LD default mode, make/break = 33/66 ms</td> </tr> <tr> <td>Open</td> <td>MF only</td> </tr> <tr> <td>Low</td> <td>LD default mode, make/break = 40/60 ms</td> </tr> </tbody> </table>	Mode pin	Function	High	LD default mode, make/break = 33/66 ms	Open	MF only	Low	LD default mode, make/break = 40/60 ms
Mode pin	Function									
High	LD default mode, make/break = 33/66 ms									
Open	MF only									
Low	LD default mode, make/break = 40/60 ms									
20 19 18 17	R1 R2 R3 R4	Keyboard Rows								
16 15 14 13	C1 C2 C3 C4	Keyboard Columns								
7	CI	Complex Impedance Input Input pin for the capacitor in the complex impedance								

FUNCTIONAL DESCRIPTION

Power On Reset

The on chip power on reset circuit monitors the supply voltage (V_{DD}). When V_{DD} rises above approx. 1.2V, a power on reset occurs to assure correct start-up and the RAM is cleared.

DC Conditions

The normal operating range is from 13mA to 100 mA. Operating range with reduced performance is from 5mA to 13mA. In the operating range all functions are operational.

In the line hold range from 0 to 5 mA the device is in a power down mode and the voltage at LI is reduced to maximum 3.5V.

The dc characteristic (excluding diode bridge and Pulsing transistors) is determined by the voltage at LI and the resistor R1 as follows:

$$VLS = VLI + I_{Line} \cdot R1$$

The voltage at LI is 4.5V.

During pulse dialling the speech circuit and other parts of the device not required are in a power down mode to save current. The CS pin is pulled to V_{SS} in order to turn the external shunt transistor on to keep a low voltage drop at the LS pin during make periods.

AC Impedance

The Characteristic or Output impedance of the SA2532 is set within the IC and adjusted by Mask Options. Available options are for 600Ω and 1000Ω. When the 1000Ω option is selected then a capacitor may be added to the circuit at pin CI to add a reactive element and make the output impedance complex.

Oscillator

All the Timing Functions of the SA2532 are based on a Clock Frequency of 3.58MHz. A crystal or ceramic resonator of this frequency should be connected to the OSC pin. In practise minor deviations from the nominal frequency may occur due to the characteristics of the frequency reference device used and so it is recommended that care is taken in the selection of components.

In some cases a small value capacitor ($\leq 47\text{pF}$) may have to be connected in parallel with the Frequency Reference to ensure start-up and/or operation at the nominal frequency.

Speech Circuit

The speech circuit consists of a transmit and a receive path with soft clip, mute, line loss compensation and side tone cancellation.

Transmit

The gain of the transmit path is 35 dB for M1/M2 to LS (see test circuit figure 5). The microphone input is differential with an input impedance of 25 kΩ.

The soft clip circuit limits the output voltage at LI to $2.0V_{PEAK}$. The attack time is 30μs/6dB and the decay time is 20 ms/6 dB. When mute is active, during dialling or after pressing the MUTE key, the gain is reduced by > 60 dB.

Receive

The receive input is the differential signal of RI and STB. The gain of the receive path is 2 dB (test circuit figure 5) with differential outputs, RO1/RO2 (0dB on SA2532C/U). When mute is active during dialling the gain is reduced by > 60dB. During DTMF dialling a MF comfort tone is applied to the receiver. The comfort tone is the DTMF signal with a level that is -30dB relative to the line signal.

Side Tone

Side Tone is controlled along with Return Loss by a Double Balance Bridge as shown in

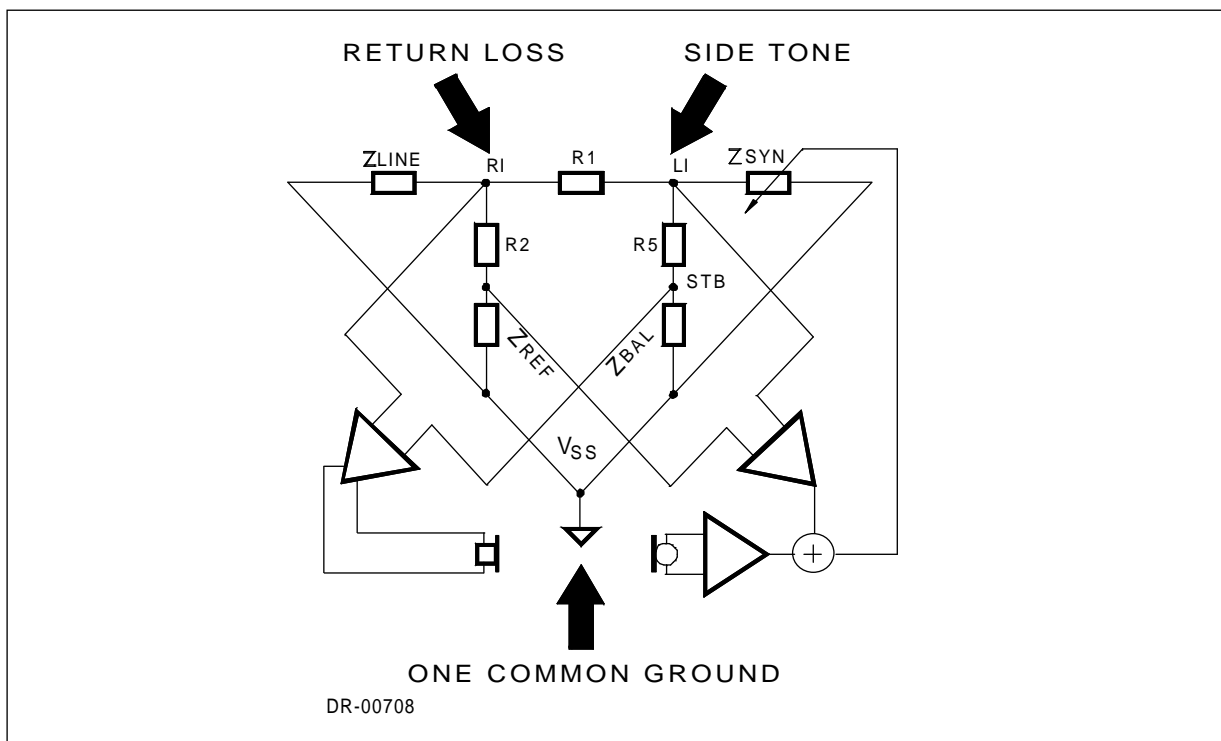


Fig. 1.

Figure 1

Double balance bridge (return loss and side tone) with one common ground

A good side tone cancellation is achieved by using the following equation:

$$\frac{ZBAL}{ZLINE} = \frac{R5}{R1}$$

The side tone cancellation signal is applied to the STB input.

Line Loss Compensation

When Line Loss Compensation is active the gain of the Transmit and Receive amplifiers are changed by 6dB in accord with the DC conditions as measured at Pins LI and LS. When the LLC Pin is Low this adjustment in gain occurs over the range $I_{LINE} = 20$ to 50 mA. When LLC is High the range is 45 to 75mA. Note that these figures apply for $R1 = R30\Omega$. When the LLC Pin is open the amplifier gains remain fixed regardless of the Line Current.

Dialling Functions

Valid Keys

The keypad of the SA2532 comprises a maximum of 20 keys (of which 3 have no function). A Bi-polar scan technique is used so that the 20 keys are scanned in a 4 x 5 matrix using only 8 pins.

A valid key is detected when one and only one contact closure is detected between a Row and Column Pin. Key contacts are debounced to avoid incorrect detection.

Dial Mode Selection

The default mode (LD or MF) can be selected by the Mode pin. When default LD mode is selected, a temporary change to MF can be invoked by pressing the * key. The circuit will revert to LD by pressing the **R** (or **R2**) key or by next on-hook.

When MF mode is selected by the mode pin, the circuit can not be changed temporarily to LD but will remain in MF.

Last Number Redial

LNR is a facility that allows resignalling of the last manually dialled number without keying in all the digits again. The LNR is repeatable.

The current contents of the RAM are overwritten by new entries.

A manually entered number is automatically stored in the LNR RAM. The capacity of the RAM is 31 digits. If a number greater than 31 digits is entered, the LNR facility will be inhibited (Until new entries < 32 digits) and further entries will be buffered in a First In First Out Memory (FIFO).

Post dialled digits, i.e. digits manually entered after LNR has been invoked, are not stored in RAM but buffered in FIFO.

During dialling, one or more pauses can be inserted by pressing the PAUSE KEY. Each pause is 3 secs (optionally 6 secs) when inserted within the first 5 digits. Otherwise a Wait Function will halt dialling until the LNR Key is pressed.

Recall Function

A Recall (**R** key or **R2** key) activation will invoke a Flash (Timed Loop Break).

If Recall is the first entry in a digit string, it will be stored in LNR RAM when digit(s) are entered after the Recall.

If the recall key is depressed after a digit string has been entered or dialled out, the recall will not be stored but buffered in the FIFO together with subsequently entered digits.

If pressing the recall key is not followed by digit entries, the LNR RAM remains intact.

After a recall, a 3 second pause will automatically be executed.

Mute Function

The MUTE key is enabled in speech mode only. Depressing the MUTE key mutes the microphone amplifier. Repeating the MUTE key deactivates the mute (toggle function). Any key entry overwrites a mute activated by the MUTE key and mute will be deactivated.

When privacy mute is activated a reminder tone is applied to the earpiece every 3 seconds.

Sliding Cursor Procedure

To accommodate easy and uncomplicated redialling (LNR) behind a PABX, a sliding cursor protocol is implemented. If new entries match the previous RAM contents, pressing the **LNR** key will dial out the remaining digits.

If there is an error in matching, the LNR will be inhibited until next on-hook, and the RAM will contain the new number.

Tone Generator

The tone generator incorporates the DTMF tones and 3 basic frequencies for the tone ringer.

DTMF Tones

The DTMF Tone Generator creates 12 Tones in compliance with CCITT Recommendation Q23. Signal levels are altered by Mask Option. High group frequencies have a level 2.6dB higher than those of the Low Group.

Details of the DTMF Tones are:

Low group

Digit 1-2-3	697Hz	(Error = -.074%)
Digit 4-5-6	770Hz	(Error = -.679%)
Digit 7-8-9	852Hz	(Error = -.621%)
Digit *-0-#	941Hz	(Error = +.139%)

High group

Digit 1-4-7-*	1209Hz	(Error = +.533%)
Digit 2-5-8-0	1336 Hz	(Error = +.176%)
Digit 3-6-9-#	1477Hz	(Error = -.141%)

Errors are calculated with reference to a base clock of 3.58MHz and at ambient temperature of 24°C. They exclude tolerance errors in the base frequency.

KEYBOARD ARRANGEMENT

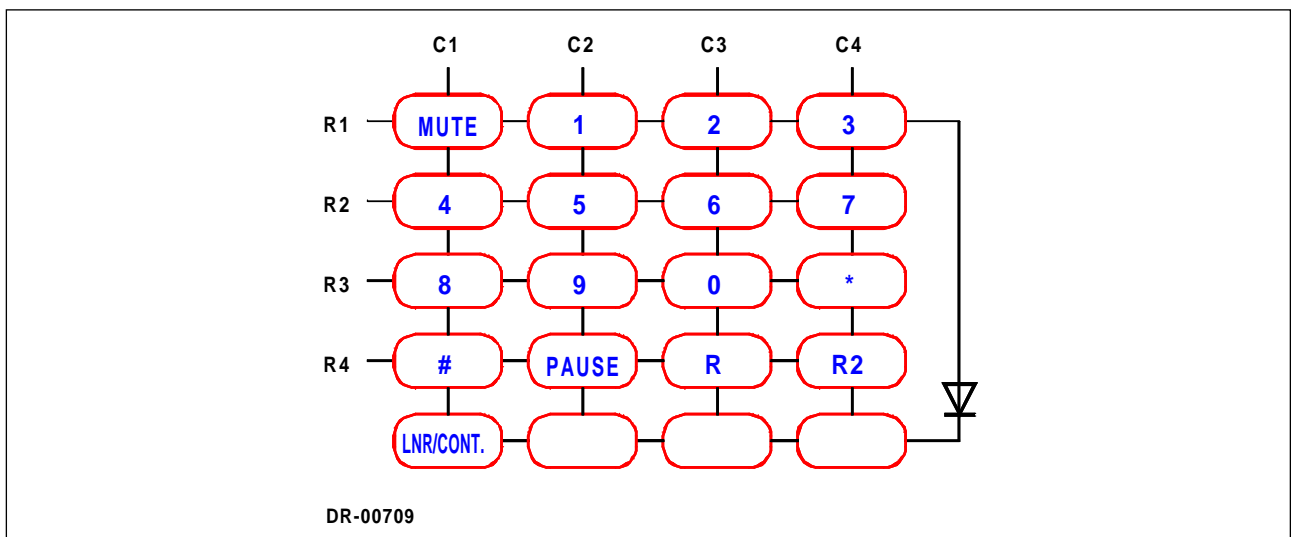


Figure 2

Microcontroller Interface

The keypad Row and Column Pins can readily be driven by a Microcontroller Interface. When configured in this way the SA2532 inputs and dials the corresponding digits in either LD or DTMF. The LNR store can be used to buffer digits to allow high speed data entry. See Application Note AN3002A for details.

Tone Ringer

The Tone Ringer of the SA2532 incorporates a Discriminator Circuit and adjustable Melody Generator

Ring Frequency Discrimination

The Ring Frequency Discriminator assures that only signals with a frequency between 20Hz and 60Hz (option 13 Hz to 60 Hz) are regarded as valid ring signals.

When a valid ring signal is present for 73ms continuously, the melody generator is activated and remains active as long as the ring signal is present.

Once the melody generator has been started, the ring signal is continuously monitored and the melody generator is instantly turned on or off according to the momentary presence of a valid or invalid ring signal respectively (until next POR or off-hook).

Melody Generator

When a Valid Ring Signal is detected the Melody generator is activated and creates a ringing Signal comprising 3 frequencies F1 (1065Hz), F2 (1420Hz) and F3 (1734Hz).

These frequencies are repeated in a sequence of 6 time slots constructed by the frequencies

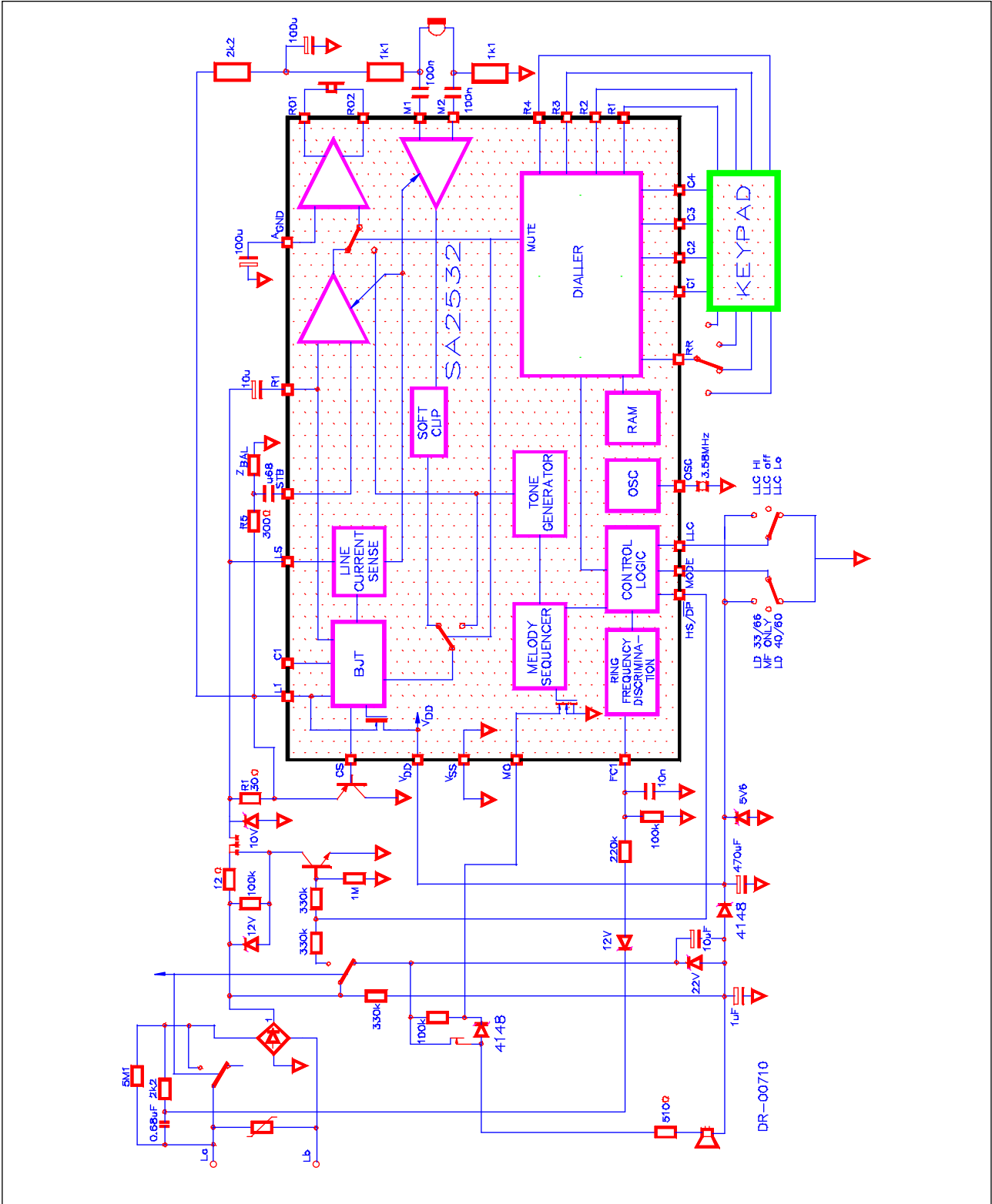
F1 F2 F3 F1 F2 F3

This sequence is repeated 1, 4, 7 or 10 times per second as indicated by the connection of the RR Pin to one of the four rows of the keyboard.

TYPICAL APPLICATION

Only the components necessary for presenting the complete functions of the SA2532 are included.

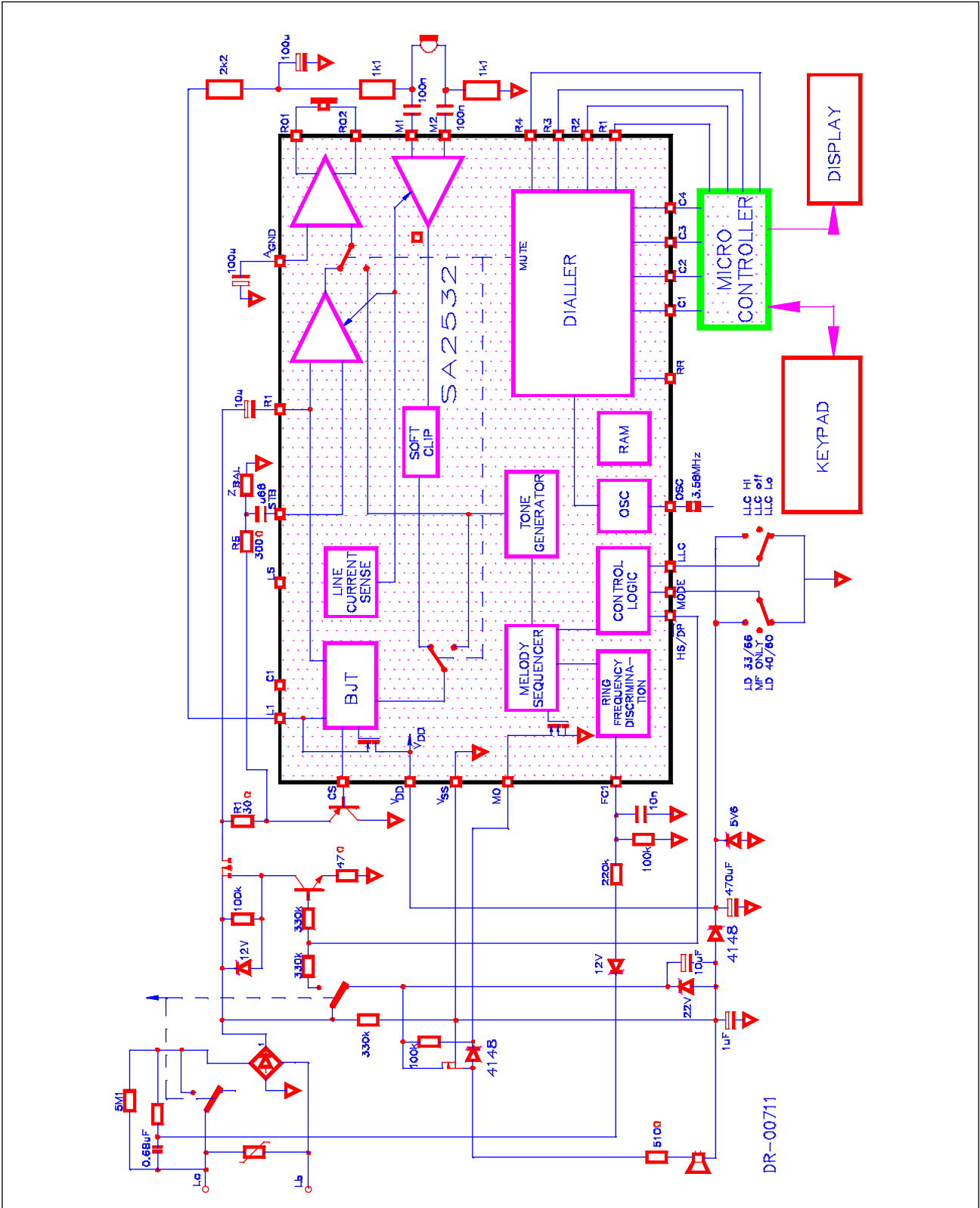
FIGURE 3



FEATURE PHONE APPLICATION

Only the components necessary for presenting the complete functions of the SA2532 are included.

FIGURE 4






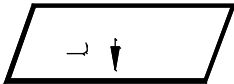
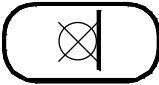

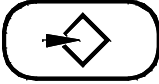
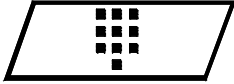
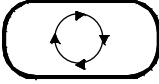

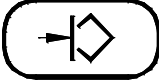

OPERATING PROCEDURES

Procedure Principles

The procedures for utilizing the features of the SA2532 are optimized out of consideration for the human factor in order to:

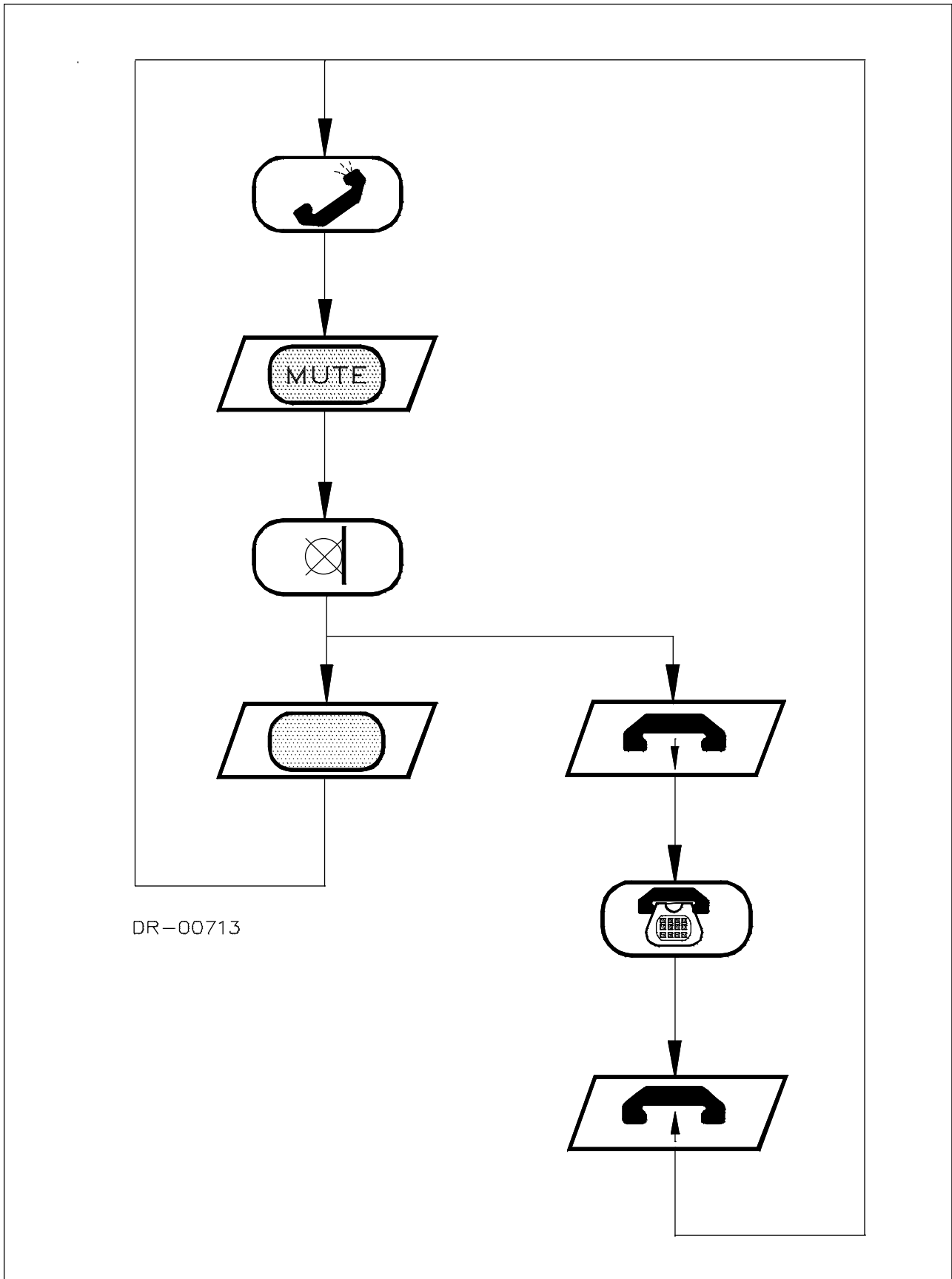
- meet the user's expectations
- be easy to learn and relearn
- not invoke any automatic functions which the user doesn't expect
- protect the user from committing critical errors, e.g. dialling wrong numbers, deleting stored numbers, etc.
- be consistent, simple and usable

SYMBOLS

<u>STATES</u>	<u>ENTRIES</u>
 IDLE (ON HOOK, NO RINGING)	
 SPEECH MODE	
 PRIVACY MUTE	
 PROGRAMMING	
 FALSE PROGRAMME ENTRY	
 INVALID ENTRY	
 STATE ACCORDING TO TEXT	

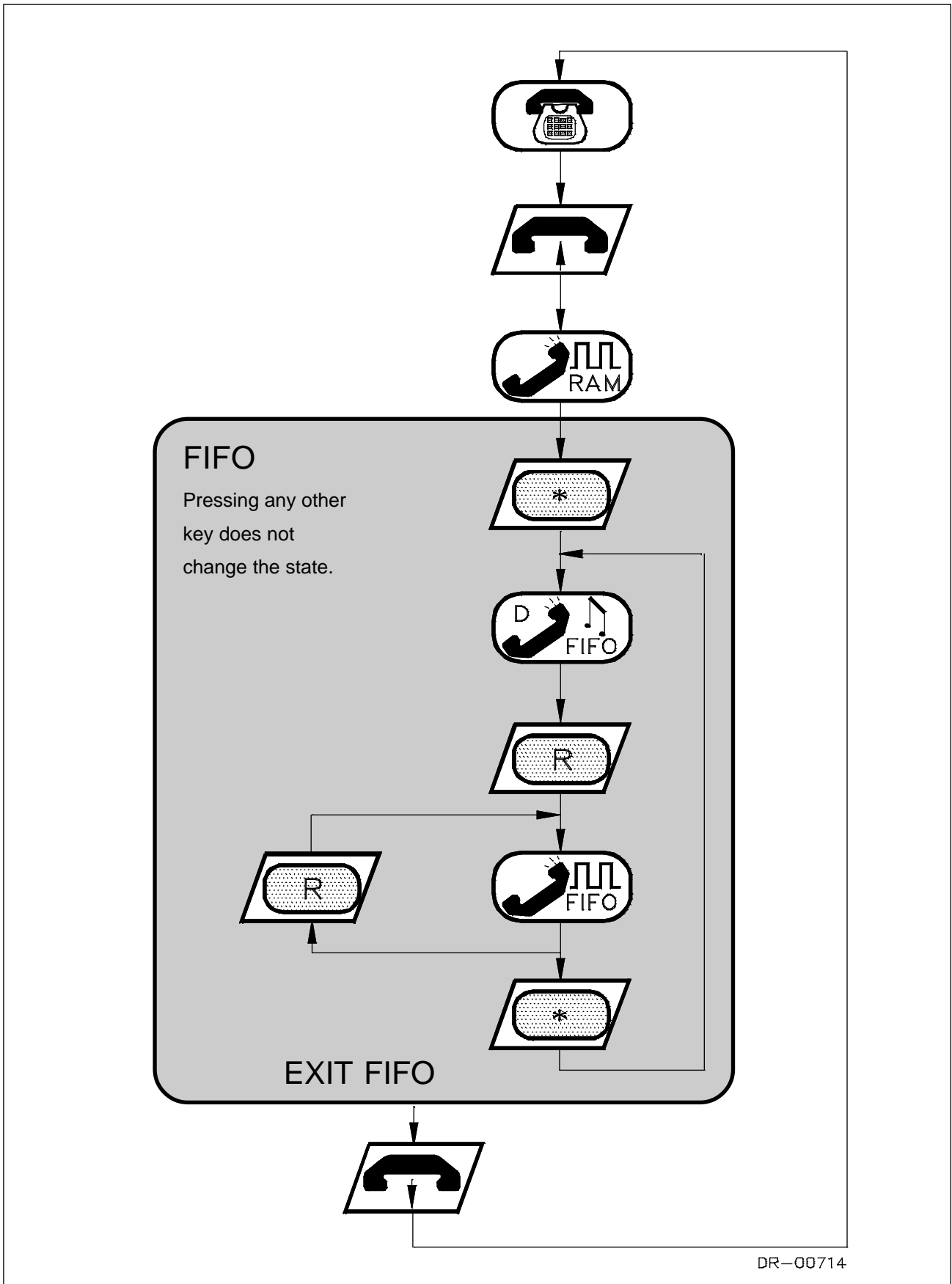
DR-00712

Privacy Mute



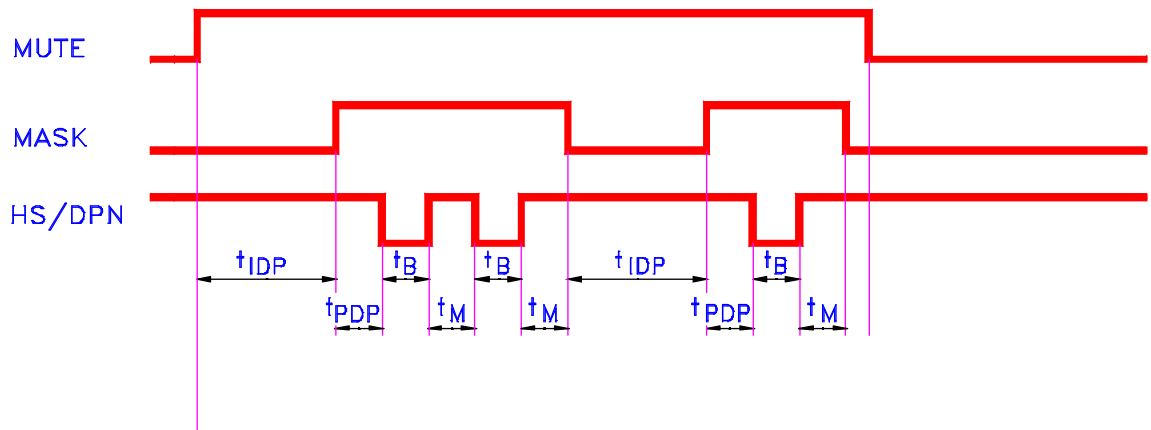
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Temporary MF

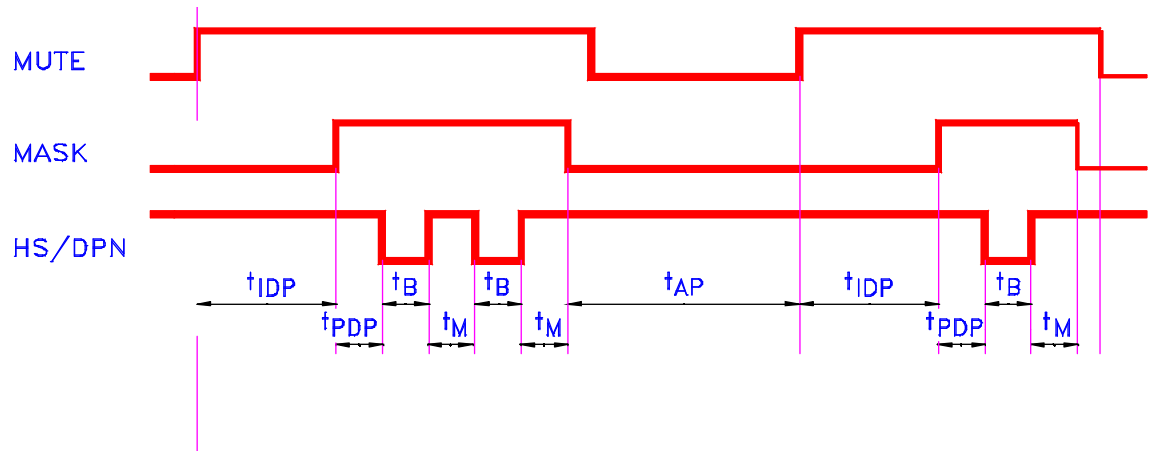


TIMING DIAGRAMS

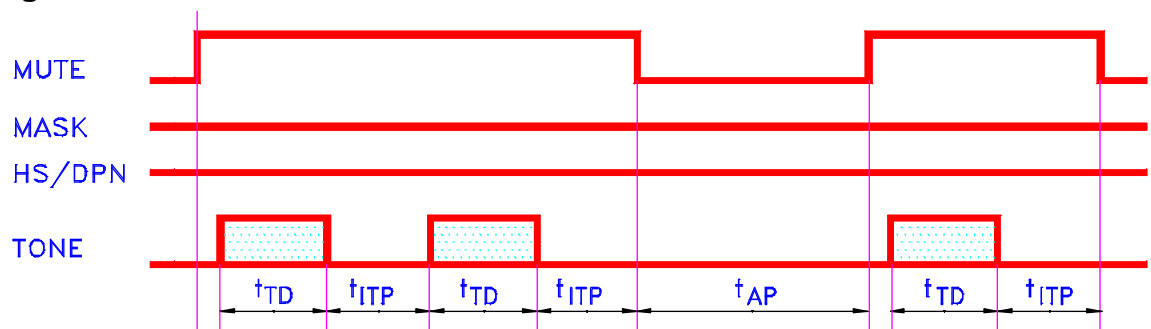
LD Dialling



LD Dialling with Access Pause

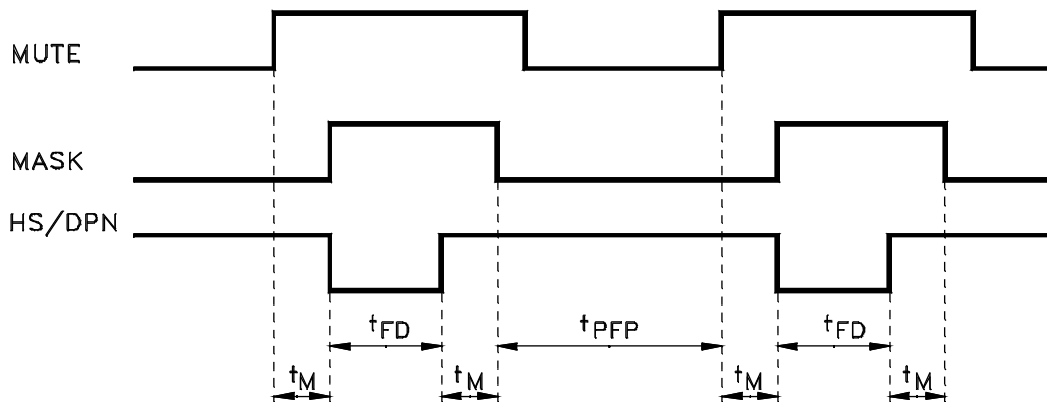


MF Dialling



DR-00715

Flash



DR-00716

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Positive Supply Voltage	$-0.3V \leq V_{DD} \leq 7V$
Input current	$\pm 25mA$
Input Voltage (LS)	$-0.3V \leq V_{IN} \leq 10V$
Input Voltage (LI, CS)	$-0.3V \leq V_{IN} \leq 8V$
Input Voltage (STB, RI)	$-2V \leq V_{IN} \leq V_{DD} + 0.3V$
Input Voltage (MO)	$-0.3V \leq V_{IN} \leq 35V$
Digital Input Voltage	$-0.3V \leq V_{IN} \leq V_{DD} + 0.3V$
Electrostatic Discharge	$\pm 800V$
Storage Temperature	$-65^{\circ}C$ to $+125^{\circ}C$

Recommended Operating Conditions

Supply Voltage * (Speech Mode)	$4V \leq V_{DD} \leq 5V$
Oscillator Frequency (Resonator: Murata CSA 3.58M G312AM)	3.58 MHz
Operating Temperature	$-25^{\circ}C$ to $+70^{\circ}C$

* This voltage is generated internally

DC Characteristics ($I_{LINE} = 15\text{ mA}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operating Current	Speech mode		3	5	mA
		MF dialling		4		mA
		LD dialling $V_{DD} = 2.5V$		200		μA
		Ring mode $V_{DD} = 2.5V$		300		μA
I_{DDO}	Retention Current	Idle mode $V_{DD} = 2V$, $T_{AMB} = 25^{\circ}C$		0.05		μA
V_{LI}	Line Voltage (default)	$13mA \leq I_{LINE} \leq 100mA$		4.5		V
I_{OL}	Output Current, Sink CS, HS/DP, MO	$V_{OL} = 0.4V$		1.5		mA

AC Characteristics ($I_{LINE}=15mA;f=800Hz$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TX	Transmit	Test Circuit Fig.5				
A_{TX}	Gain (M1/M2)	$Z_{RL}=600\Omega$ $Z_{RL} = 1000\Omega$	34	35 36.5	36	dB
$\Delta A_{TX/F}$	Variation with Frequency	$f=500Hz$ to 3.4kHz		± 0.8		dB
THD	Distortion	$V_{LI} \leq 0.5V_{RMS}$			2	%
V_{AGC}	Soft Clip Level	$V_{LI} =$		2		V_{PEAK}
A_{SCO}	Soft Clip Overdrive			20		dB
t_{ATTACK}	Attack Time			30		$\mu s/6dB$
t_{DECAY}	Decay Time			20		ms/6dB
Z_{IN}	Input Impedance (M1/M2)			20		k Ω
A_{MUTE}	Mute Attenuation	Mute activated	60			dB
V_{NO}	Noise Output Voltage				-72	dBmp
V_{FC}	Unwanted Frequency Components	50...300 Hz 4.3...28 kHz above 28 kHz			-43 note 1 -70	dBm dBm
V_{INMAX}	Input Voltage Range (M1/M2)	Differential Single Ended		± 1 ± 0.5		V_{PEAK} V_{PEAK}
BJT	Output Driver					
V_{INMAX}	Input Voltage Range (LI)			± 2		V_{PEAK}
V_{TX}	Dynamic Range			± 2		V_{PEAK}
RL	Return Loss	$Z_{RL} = 600\Omega$ SA2532A $Z_{RL} = 1000\Omega$ SA2532C/U	18			dB

Note 1: -37 dBm at 4.3 kHz and decreasing 12 dB/octave till 28 kHz.

AC Characteristics (cont'd) ($I_{LINE} = 15 \text{ mA}; f=800\text{Hz}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RX	Receive	Test Circuit Fig.5				
A_{RX}	Receive Gain (RO1/RO2)	$Z_{RL}=600\Omega$	1	2	3	dB
$\Delta A_{RX/F}$	Variation with Frequency	$Z_{RL}=1000\Omega$ $f=500 \text{ Hz to } 3.4 \text{ kHz}$		-0.2 ± 0.8		dB
THD	Distortion	$V_{RI} \leq 0.5V_{RMS}$			2	%
V_{AGC}	Soft Clip Level	$V_{RI} =$		1		V_{PEAK}
A_{SCO}	Soft Clip Overdrive			10		dB
t_{ATTACT}	Attact Time	$V_{RI} > 0.8V$		30		$\mu\text{s}/6\text{dB}$
t_{DECAY}	Decay Time			20		ms/6dB
V_{NO}	Noise Output Voltage				-72	dBmp
V_{FC}	Unwanted Frequency Components	50 Hz...20 kHz			-60	dBm
Z_{IN}	Input Impedance (RI)			8		k Ω
V_{INRI}	Input Voltage Range(RI)			± 2		V_{PEAK}
ST	Sidetone	Test Circuit Fig.5				
A_{ST}	Sidetone Cancellation	$V_{RI} \leq 0.5V_{RMS}$	26			dB
V_{INST}	Input Voltage Range (STB)			± 2		V_{PEAK}
Z_{IN}	Input Impedance (STB)			80		k Ω
	Keyboard					
t_D	Key Debounce Time			15		ms
	HS Input					
t_{HS-L}	Low to High Debounce	Going off-hook		15		ms
t_{HS-H}	High to Low Debounce	Line breaks/on-hook		240		ms
	DTMF					
ΔF	Frequency deviation	Note 5	-0.679		+0.533	%
V_{MF}	MF Tone Level(Low group)	Optionally	-12.5 -9.5	-11 -8	-9.5 -6.5	dB dB
V_{L-H}	Preemphasis Low to High		2.0	2.6	3.0	dB
THD	Distortion	Note 3			-30	dBr
t_{TD}	Tone Duration	Note 1	80	82.3	85	ms
t_{ITP}	Inter Tone Pause		80	82.3	85	ms

AC Characteristics Cont'd

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TR}	Tone Rise Time	Note 2			5	ms
t_{TF}	Tone Fall Time	Note 2			5	ms
t_{DR}	LD Dial Rate	$\pm 5\%$		10		pps
$t_{M/B}$	Make/Break Period	$\pm 5\%$, MODE=low $\pm 5\%$, MODE=high		40.8/61.2 33/66		ms ms
t_{PDP}	Pre-Digit Pause			35		ms
t_{IDP}	Inter Digit Pause		800	840	880	ms
t_{MO}	Mute Overhang			t_M		
t_{FD}	Flash Duration 1		100		102	ms
	Flash Duration 2	SA2532A/C	270		300	ms
	Flash Duration 2	SA2532U	600		650	ms
t_{PFP}	Post Flash Pause		2.9	3.0	3.1	sec.
t_{AP}	Access Pause Period	SA2532A/U	2.9	3.0	3.1	sec
		SA2532C	5.8	6.0	6.2	sec
V_{MO}	Tone Ringer Melody Output Level			PDM		
t_{MD}	Melody Delay				10	ms
F1	Frequency 1		1020	1064	1107	Hz
F2	Frequency 2		1363	1420	1477	Hz
F3	Frequency 3		1665	1734	1803	Hz
t_{DT}	Detection Time	Initial	70		80	ms
t_{TO}	Detection Time-out			note 4		ms
f_{MIN}	Min. Detection Frequency		19	20	21	Hz
f_{MIN}	Min. Detection Frequency	Optionally	12	13	14	Hz
f_{MAX}	Max. Detection Frequency		58	59	60	Hz
V_{RT}	Reminder Tone Level (RO1/RO2)	Relative to LS		-30		dBr
t_{RTD}	Duration			82.3		ms
t_{RTI}	Interval			3		sec
V_{CT}	Comfort Tone (DTMF) Level (RO1/RO2)	Relative to LS		-30		dBr

- Note 1: The values are valid during automatic dialling and are minimum values during manual dialling, i.e. the tones will continue as long as the key is depressed.
- Note 2: The rise time is the time from 10% of final value until the tone amplitude has reached 90% of its final value.
- Note 3: Relative to high group.
- Note 4: The FCI circuit is reset by POR and HS/DP pulled high (off-hook). After a reset the FCI circuit is in a standby state. A positive edge on FCI will start a 73ms timer and the frequency discrimination is initiated. Whenever a period of the ring signal is missing, the timer is reset. When a valid ring signal is present for $\geq 73\text{ms}$, the melody generator is started and is directly controlled by the ring signal. This condition will remain until a new reset.
- Note 5: This does not include the frequency deviation of the ceramic resonator.

Test Circuit

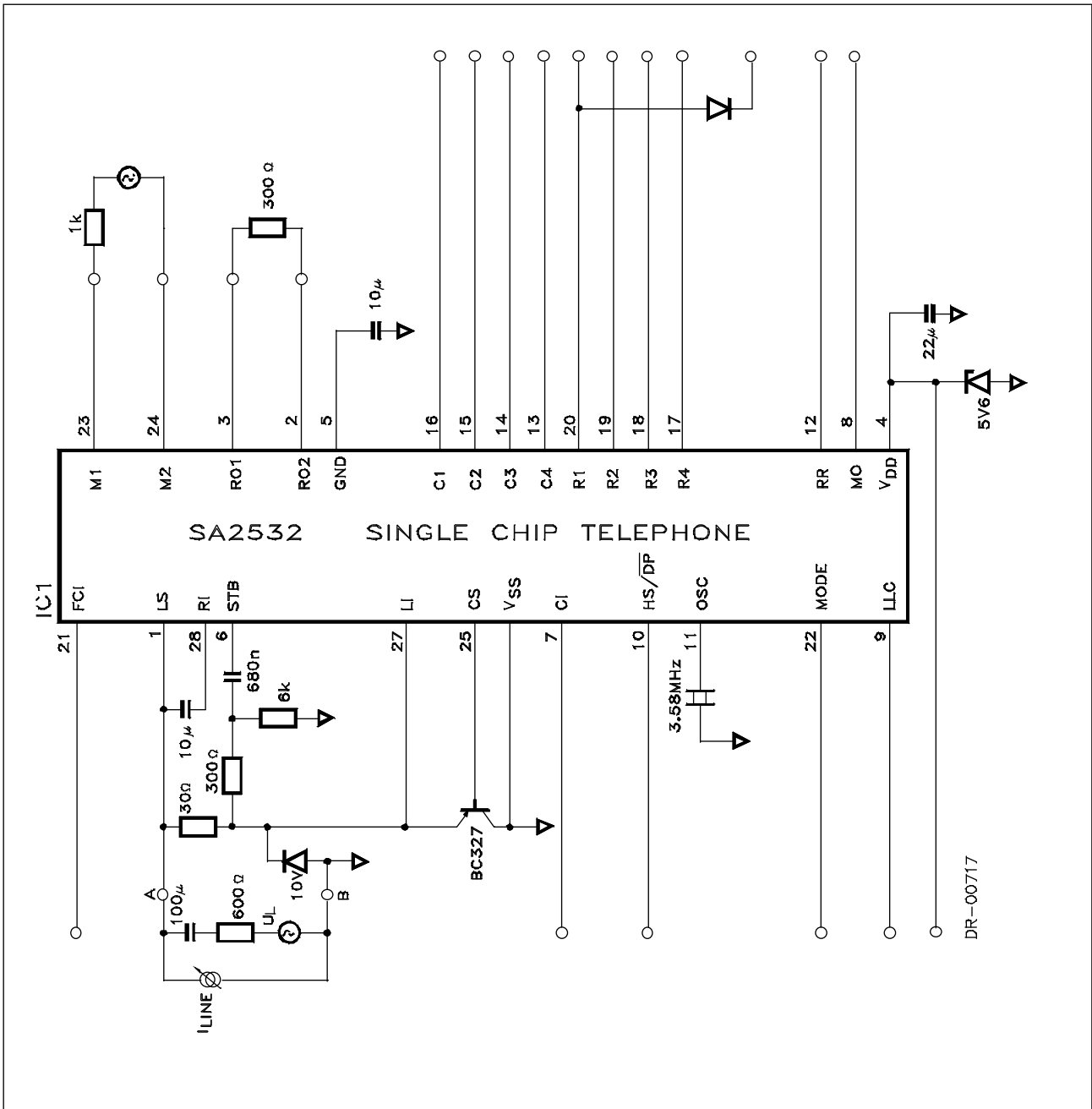


Figure 5

Ordering Information:

Versions	ZRL (ohm)	DTMF Level	R2 Period	Access Pause	Package
SA2532A P	600	-6/-8dBm	280ms	3s	28 pin DIP
SA2532A S	600	-6/-8dBm	280ms	3s	28 pin SOIC
SA2532C P	1000	-6/-8dBm	280ms	6s	28 pin DIP
SA2532C S	1000	-6/-8dBm	280ms	6s	28 pin SOIC
SA2532U P	1000	-9/-11dBm	600ms	3s	28 pin DIP
SA2532U S	1000	-9/-11dBm	600ms	3s	28 pin SOIC

NOTES:

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