SA4871

3W Mono Low-Voltage Audio Power Amplifier

Features

- Operating Voltage : 2.5V-5.5V
- Bridge-Tied Load (BTL) Mode Operation
- Supply Current – I_{DD}=7mA at V_{DD}=5V
- Low Shutdown Current – I_{DD}=0.1μA
- Low Distortion
  –2.5W, at V_{DD}=5V, BTL, R_L=3Ω
  THD+N=0.1%
  –2.1W, at V_{DD}=5V, BTL, R_L=4Ω
  THD+N=0.1%
- Output Power
  at 1% THD+N
  –2.6W, at V_{DD}=5V, BTL, R_L=3Ω
  –2.3W, at V_{DD}=5V, BTL, R_L=4Ω
  at 10% THD+N
  –3.3W at V_{DD}=5V, BTL, R_L=3Ω
  –2.7W at V_{DD}=5V, BTL, R_L=4Ω
- Depop Circuitry Integrated
- Thermal shutdown protection and over current protection circuitry
- High supply voltage ripple rejection
- Surface-Mount Packaging
  –MSOP-8-P (with enhanced thermal pad)
  –SOP-8-P (with enhanced thermal pad)
- Lead Free Available (RoHS Compliant)

General Description

The SA4871 is a bridged-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers. Operating with a 5V supply, the SA4871 can deliver 3.3W of continuous power into a BTL 3Ω load at 10% THD+N throughout voice band frequencies. Although this device is characterized out to 20kHz, its operation is optimized for narrow band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power sensitive applications with special depop circuitry to eliminate speaker noise when exiting shutdown mode. The SA4871 is available in a SOP-8-P or MSOP-8-P.

Applications

- Mobil Phones
- PDAs
- Portable Electronic Devices
- Desktop Computers

Ordering and Marking Information

SA4871 □□-□□ □ Lead Free Code Handling Code Temp. Range Package Code	Package Code KA : SOP-8-P XA : MSOP-8-P Operating Ambient Temp. Range I : -40 to 85°C Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device
SA4871 KA : SA4871 XXXXX	XXXXX - Date Code
SA4871 XA : SA4871 XXX XX	XXXXX - Date Code

Note: SUPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. SUPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

SUPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

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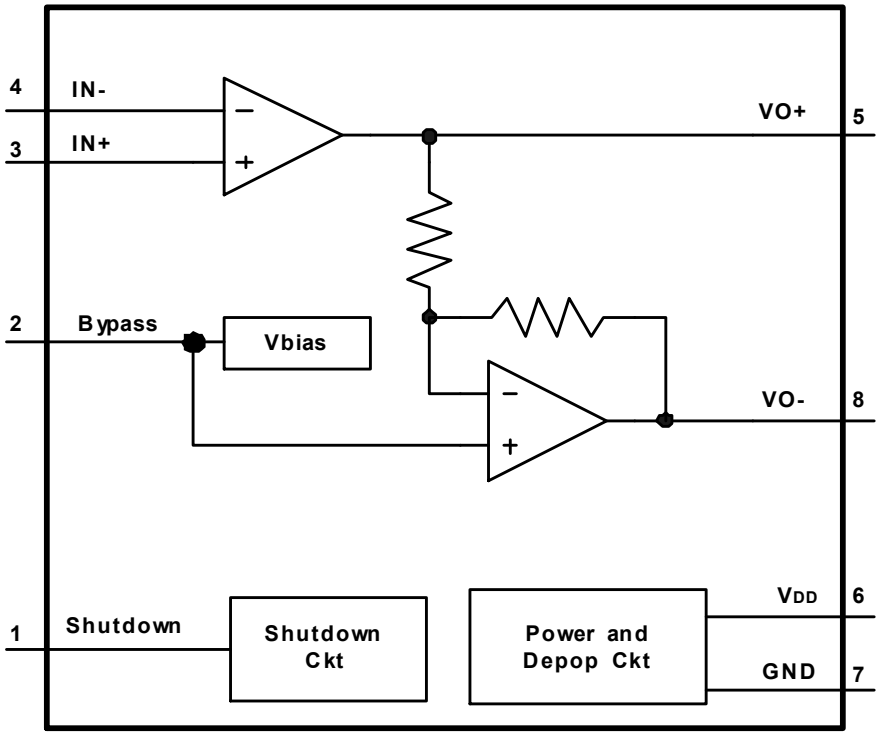
Block Diagram



Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 6	V
V_{IN}, V_O	Input Voltage Range, Shutdown, Bypass, V_O	-0.3 to V_{DD}+0.3	V
T_A	Operating Junction Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	Internally Limited	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature Range	260	°C
V_{ESD}	Electrostatic Discharge	-2000 to 2000 (Note1)	V
		-200 to 200 (Note2)	
P_D	Power Dissipation	Internally Limited	W

Notes:

1.Human body model: C=100pF, R=1500Ω, 3 positives pulses plus 3 negative pulses

2.Machine model: C=200pF, L=0.5μF, 3 positive pulses plus 3 negative pulses

Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		2.5	5.5	V
V_{IH}	High-Level Voltage	Shutdown	2.2		V
V_{IL}	Low-Level Voltage	Shutdown		0.4	V

Thermal Characteristics

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal Resistance - Junction to Ambient MSOP-8-P* SOP-8-P*	 50 56	°C/W

* Please refer to "Thermal Pad Consideration". 2 layered 5 in^2 printed circuit board with 2oz trace and copper through several thermal vias. The thermal pad is solder on the PCB.

Electrical Characteristics

Unless otherwise noted these specifications apply over full temperature V_{DD}= 5V, T_A= 25°C (unless otherwise noted)

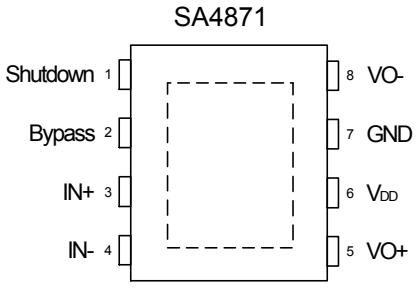
Symbol	Parameter	Test Conditions	SA4871			Unit
			Min.	Typ.	Max.	
V_{OO}	Output Offset Voltage	R_L=8Ω, Ri=R_F=20kΩ			20	mV
I_{DD}	Supply Current	I_O=0mA		7	14	mA
$I_{DD(SD)}$	Supply Current	Shutdown Mode		0.1		μA
|IH|		Shutdown, V_I=V_{DD}		0.1		μA
|IL|		Shutdown, V_I=0V		0.1		μA
Operating characteristic, V_{DD}=5V,T_A=25℃						
Po	Output Power	THD=1%, f=1kHz, R_L=3Ω R_L=4Ω R_L=8Ω		 2.6 2.3 1.3		W
		THD=10%, f=1kHz, R_L=3Ω R_L=4Ω R_L=8Ω		 3.3 2.7 1.7		

Electrical Characteristics (Cont.)

Unless otherwise noted these specifications apply over full temperature V_{DD}= 5V, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	SA4871			Unit
			Min.	Typ.	Max.	
THD+N	Total Harmonic Distortion Plus Noise	f=1kHz, Po=2W, RL=3Ω Po=1.6W, RL=4Ω Po=1W, RL=8Ω		 0.06 0.04 0.03		%
B1	Unity-Gain Bandwidth	Open Loop		2		MHz
PSRR	Power Supply Rejection Ratio	CB=1μF, RL=8Ω, f=120kHz		60		dB
Vn	Noise Output Voltage	Gain=2, CB=1μF, RL=8Ω		28		μV(rms)
Twu	Wake-Up Time	CB=1μF		380		ms

Pin Assignment

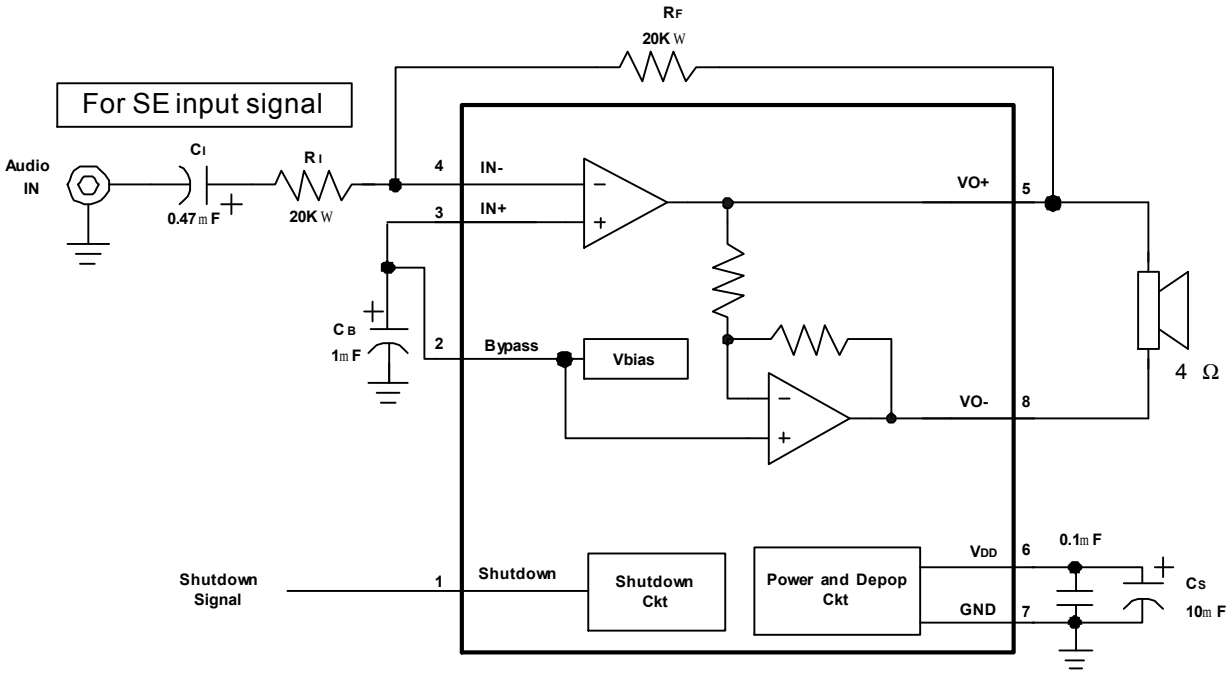


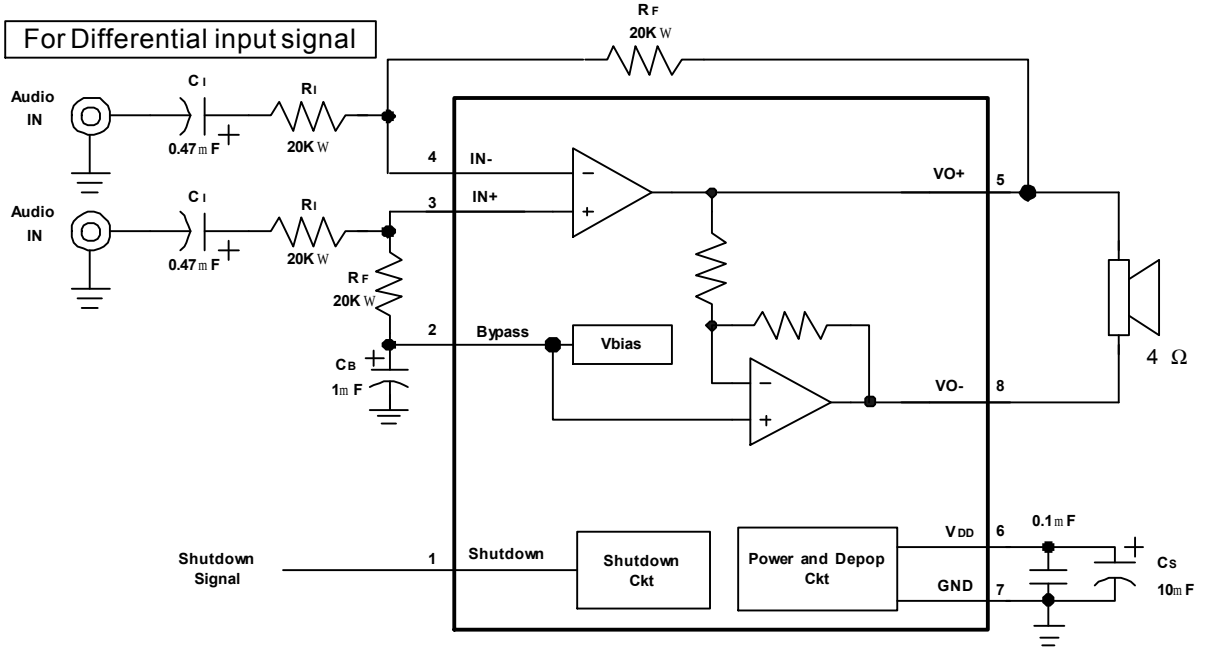
= Thermal Pad
(connected to GND plane for better heat dissipation)

Pin Function Description

Pin		I/O	Description
Name	No		
Shutdown (SA4871)	1	I	Shutdown mode control signal input, place entire IC in shutdown mode when held high in SA4871.
Bypass	2	I	Bypass pin
IN+	3	I	IN+ is the non-inverting input. IN+ is typically tied to the Bypass terminal.
IN-	4	I	IN- is the inverting input. IN- is typically used as the audio input terminal.
VO+	5	O	VO+ is the positive BTL output.
VDD	6		Supply voltage input pin.
GND	7		Ground connection for circuitry.
VO-	8	O	VO- is the negative BTL output.

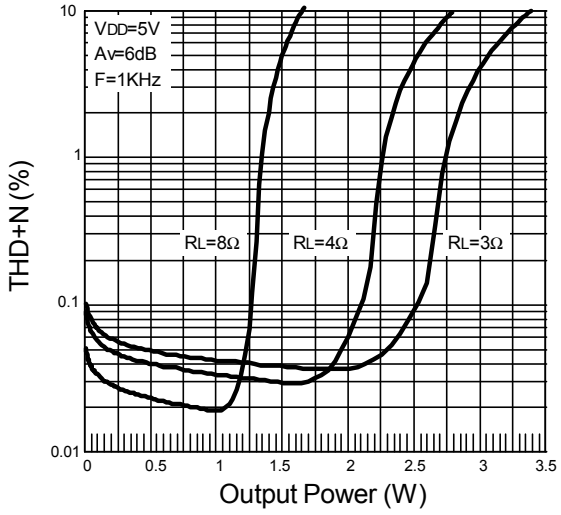
Typical Application Circuit



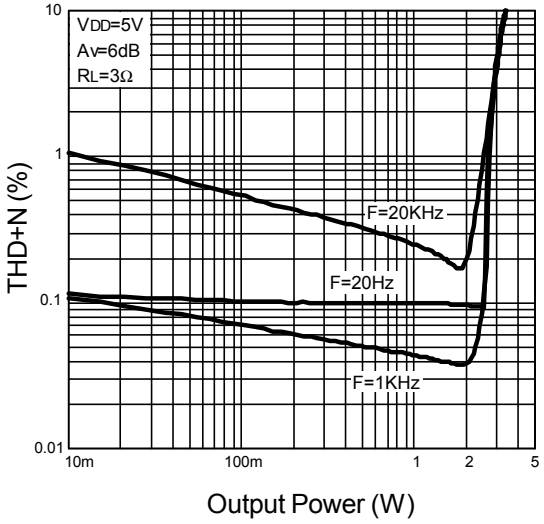


Typical Characteristics

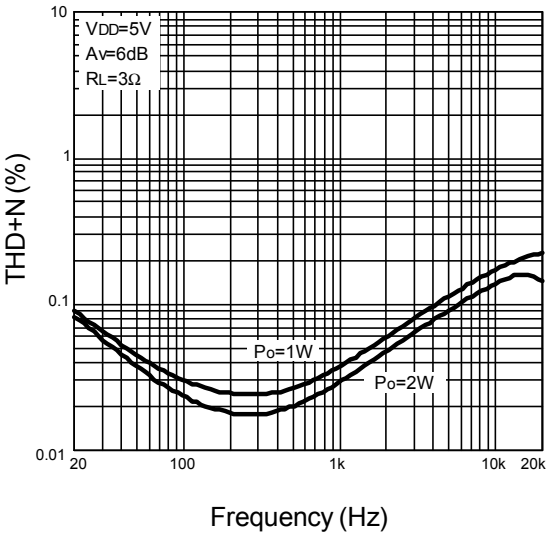
THD+N vs. Output Power



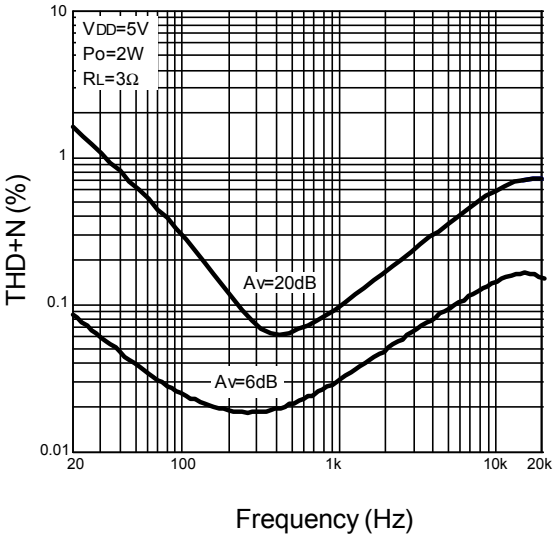
THD+N vs. Output Power



THD+N vs. Frequency

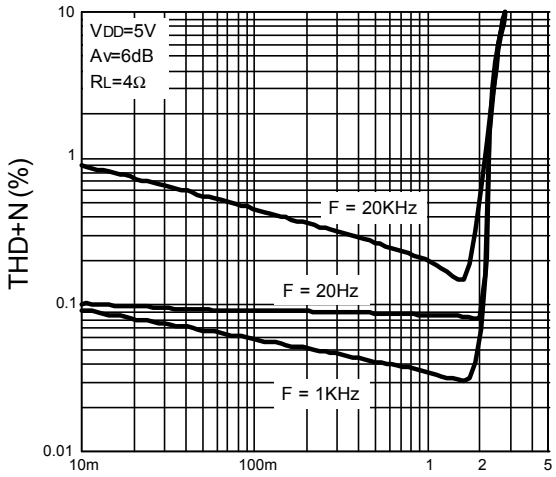


THD+N vs. Frequency



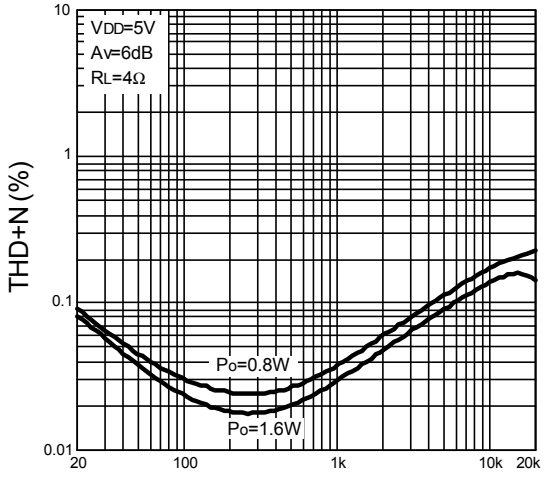
Typical Characteristics (Cont.)

THD+N vs. Output Power



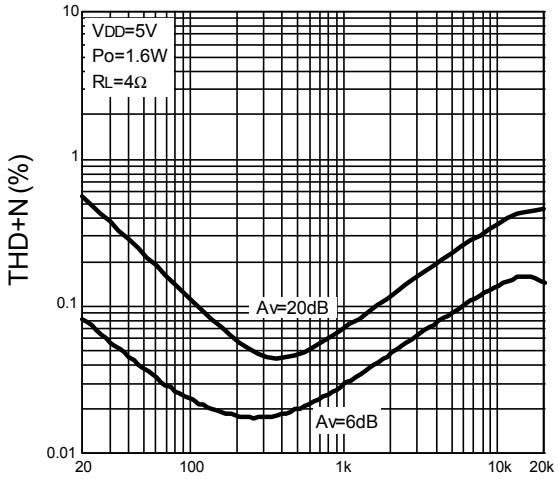
Output Power (W)

THD+N vs. Frequency



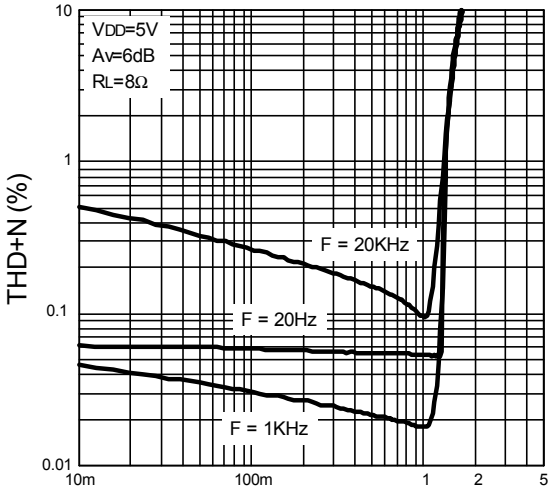
Frequency (Hz)

THD+N vs. Frequency



Frequency (Hz)

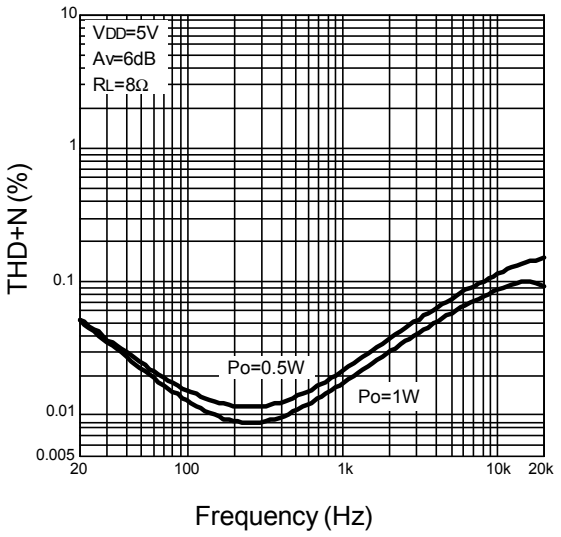
THD+N vs. Output Power



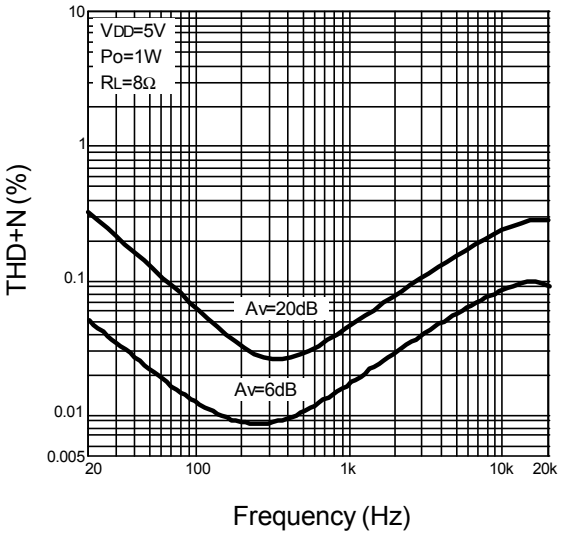
Output Power (W)

Typical Characteristics (Cont.)

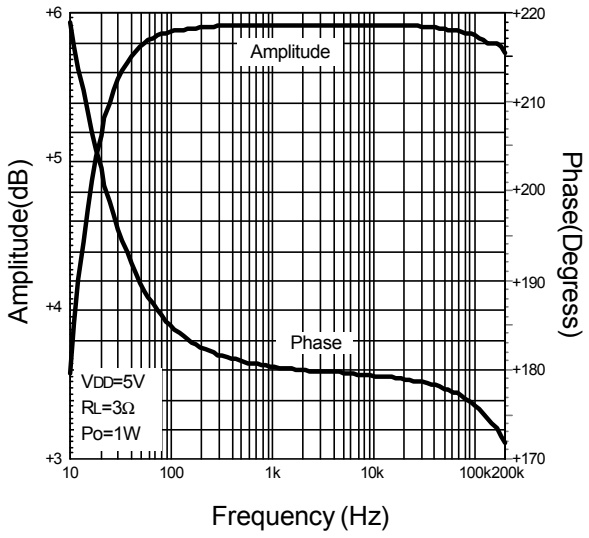
THD+N vs. Frequency



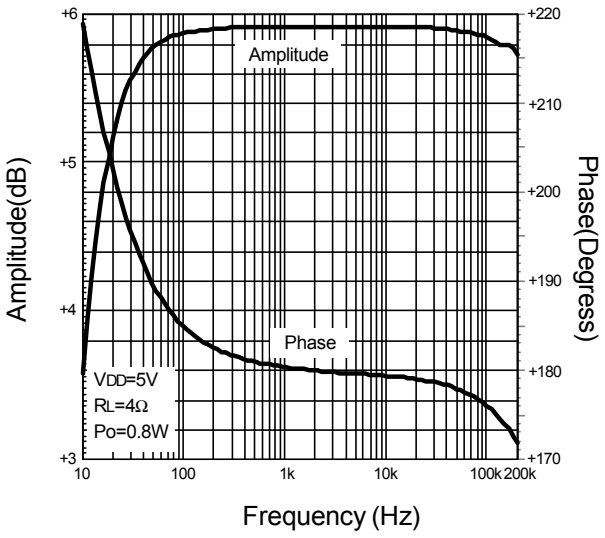
THD+N vs. Frequency



Frequency Response

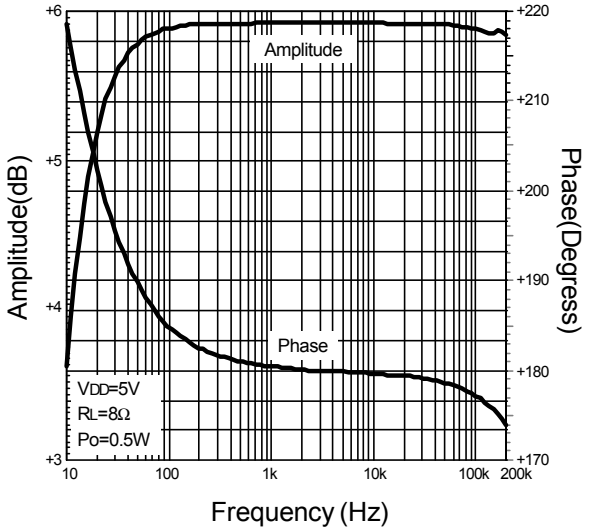


Frequency Response

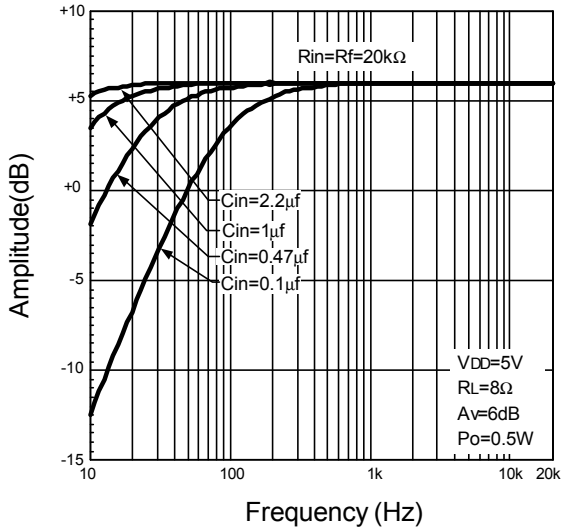


Typical Characteristics (Cont.)

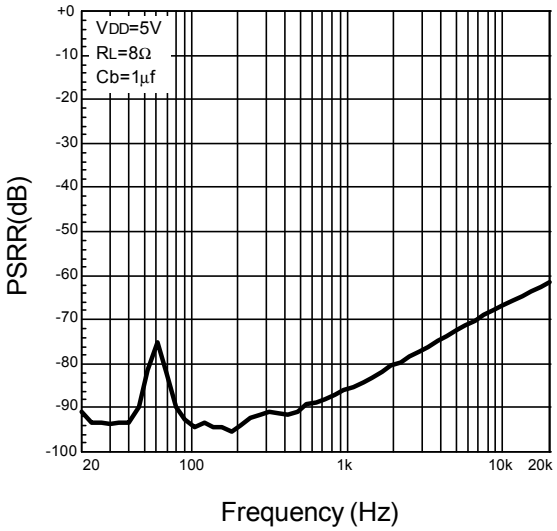
Frequency Response



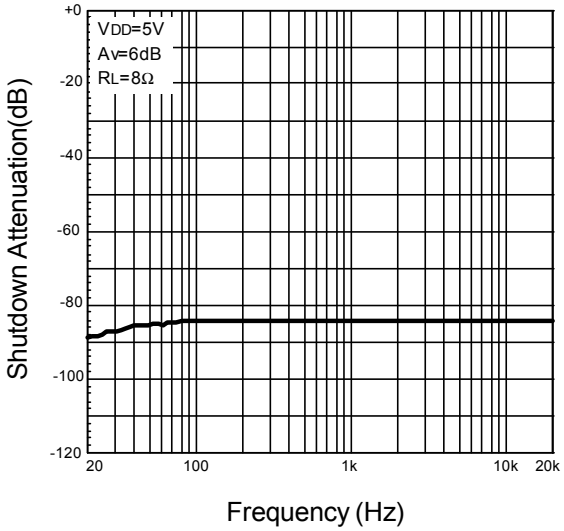
Input Capacitor vs.
Frequency Response



PSRR vs. Frequency

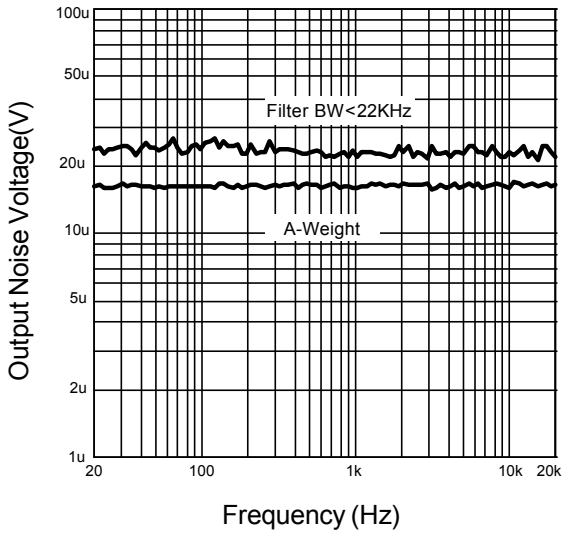


Shutdown Attenuation
vs. Frequency

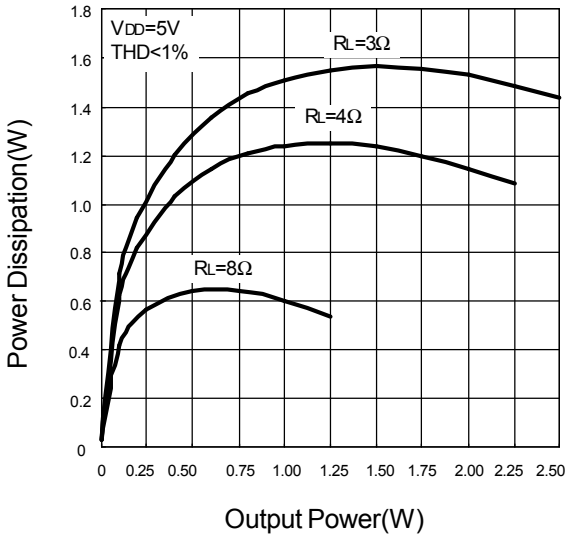


Typical Characteristics (Cont.)

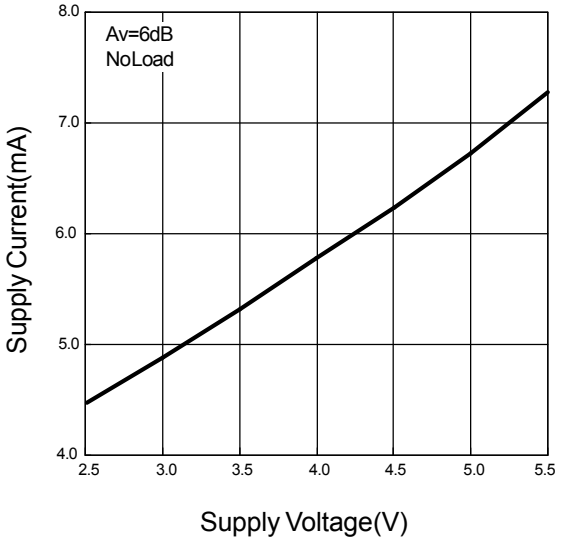
Output Noise Voltage vs.Frequency



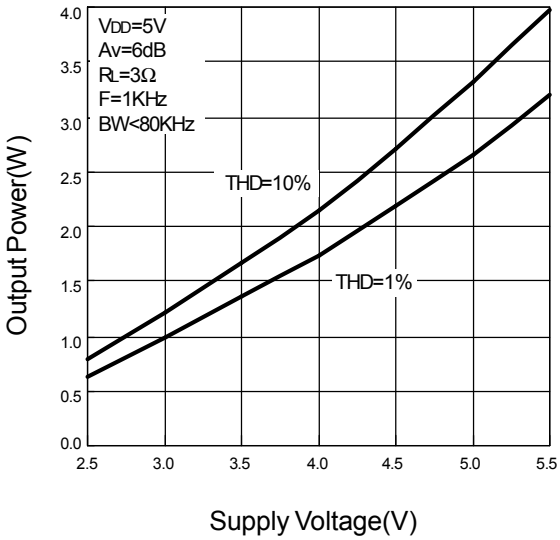
Power Dissipation vs. Output Power



Supply Current vs. Supply Voltage

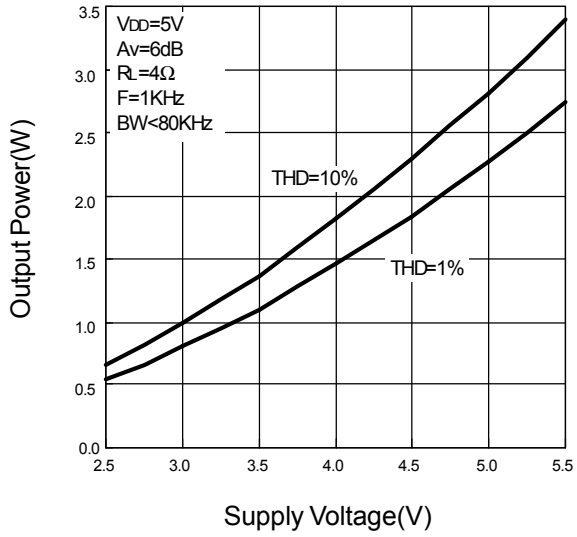


Supply Voltage vs. Output Power

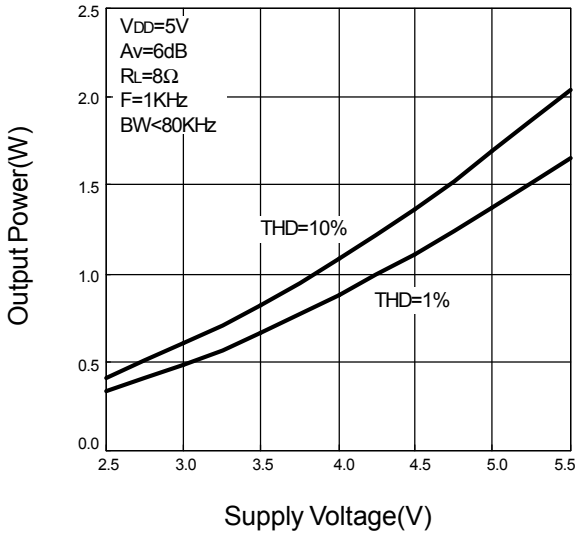


Typical Characteristics (Cont.)

Power Dissipation vs. Output Power



Supply Current vs. Supply Voltage



Application Descriptions

BTL Operation

The SA4871 output stage (power amplifier) has two pairs of operational amplifiers internally, allowed for different amplifier configurations.

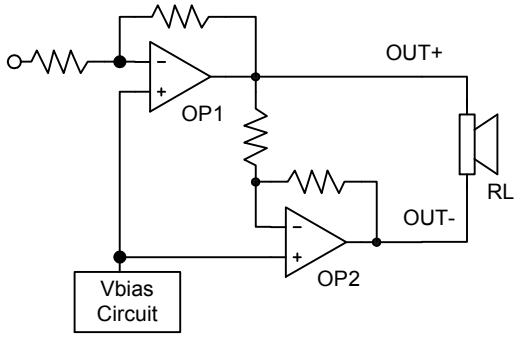


Figure 1: SA4871 internal configuration

The power amplifier's OP1 gain is setting by Ri and Rf, while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude, but out of phase 180°. Consequently, the differential gain for each channel is 2 x (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration commonly referred to as bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage.

Four times the output power is possible as compared toa SE amplifier under the same conditions. A BTL configuration, such as the one used in SA4871 , also creates a second advantage over SE amplifiers. Since the differential outputs, OUT+ and OUT- are biased

Application Descriptions (Cont.)

BTL Operation (Cont.)

at half-supply, no need DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Input Resistance, Ri

The gain for audio input of the SA4871 is set by the external resistors (Ri and Rf).

$$\text{BTL Gain} = -2 \times \frac{R_F}{Ri} \qquad (1)$$

BTL mode operation brings the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. The input resistance will affect the low frequency performance of audio signal.

Input Capacitor, Ci

In the typical application an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the input impedance Ri (20kΩ) form a high-pass filter with the corner frequency determined in the follow equation :

$$F_C(\text{highpass}) = \frac{1}{2\pi \times 20k\Omega \times Ci} \qquad (2)$$

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where Ri is 10kΩ and the specification calls for a flat bass response down to 50Hz. Equation is reconfigured as follow :

$$Ci = \frac{1}{2\pi \times 20k\Omega \times f_C} \qquad (3)$$

Ci is 0.16μF so one would likely choose a value in the range of 0.22μF to 1.0μF.

A further consideration for this capacitor is the leakage path from the input source through the input network (Ri+Rf, Ci) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at $V_{DD}/2$, which is likely higher that the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, Cbypass

As other power amplifiers, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitors located on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger bypass capacitor will improve PSRR due to increased supply stability. Typical applications employ a 5V regulator with 1.0μF and a 0.1μF bypass capacitor as supply filtering. This does not eliminate the need for bypassing the supply nodes of the SA4871. The selection of bypass capacitors, especially Cbypass, is thus dependent upon desired PSRR requirements, click and pop performance.

To avoid start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (4) should be maintained.

$$\frac{1}{Cbypass \times 125k\Omega} << \frac{1}{40k\Omega \times Ci} \qquad (4)$$

The bypass capacitor is fed thru from a 125kΩ resistor inside the amplifier and the 40kΩ is maximum input resistance of (Ri+ Rf). Bypass capacitor, Cb, values of 3.3μF to 10μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

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Application Descriptions (Cont.)

Effective Bypass Capacitor, Cbypass (Cont.)

The bypass capacitance also effects to the start up time. It is determined in the following equation :

$$T_{start\ up} = 5 \times (C_{bypass} \times 125K\Omega) \quad (5)$$

Power Supply Decoupling, Cs

The SA4871 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different type capacitors that target on different type of noise on the power supply leads.

For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

Optimizing Depop Circuitry

Circuitry has been included in the SA4871 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry.

The value of Ci will also affect turn-on pops. (Refer to Effective Bypass Capacitance) The bypass voltage ramp up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of Cbypass can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of Cbypass, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of Cbypass and the turn-on time.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. So it is advantageous to use low-gain configurations.

Shutdown Function

In order to reduce power consumption while not in use, the SA4871 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic high is placed on the SHUTDOWN pin. The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between ground and the supply V_{DD} to provide maximum device performance.

By switching the SHUTDOWN pin to high, the amplifier enters a low-current state, $I_{DD} < 0.1\mu A$. SA4871 is in shutdown mode. On normal operating, SHUTDOWN pin pull to low level to keeping the IC out of the shutdown mode. The SHUTDOWN pin should be tied to a definite voltage to avoid unwanted state changes.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load.

The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (6)$$

Where :

$$P_O = \frac{V_{ORMS} \times V_{ORMS}}{R_L} = \frac{V_P \times V_P}{2R_L}$$

$$V_{ORMS} = \frac{V_P}{\sqrt{2}} \quad (7)$$

$$P_{SUP} = V_{DD} \times I_{DDAVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (8)$$

Application Descriptions (Cont.)

BTL Amplifier Efficiency (Cont.)

Efficiency of a BTL configuration :

$$\frac{P_O}{P_{SUP}} = \left(\frac{V_P x V_P}{2R_L}\right) / \left(V_{DD} x \frac{2V_P}{\pi R_L}\right) = \frac{\pi V_P}{4V_{DD}} \qquad (9)$$

Table 1 calculates efficiencies for four different output power levels.

Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range.

Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Po (W)	Efficiency (%)	I_{DD}(A)	V_{PP}(V)	P_D (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

** High peak voltages cause the THD to increase.

Table 1. Efficiency Vs Output Power in 5-V/8Ω BTL Systems.

Power Dissipation

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \qquad (10)$$

Even with this substantial increase in power dissipation, the SA4871 does not require extra heatsink. The power dissipation from equation11, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation11 :

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \qquad (11)$$

For MSOP8-P package with thermal pad, the thermal resistance (θ_{JA}) is equal to 48°C/W.

Since the maximum junction temperature ($T_{J,MAX}$) of SA4871 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation11.

Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the SA4871 requires special attention on thermal design. If the thermal design issues are not properly addressed, the SA4871 4Ω will go into thermal shutdown when driving a 4Ω load.

The thermal pad must be connected to ground. The package with thermal pad of the SA4871 requires special attention on thermal design. If the thermal

Application Descriptions (Cont.)

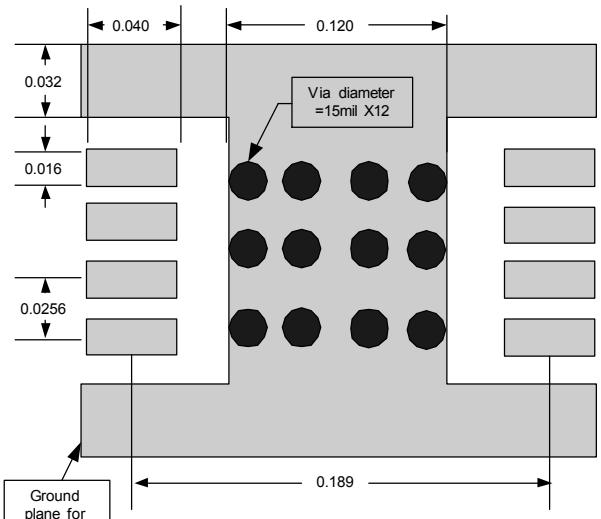
Thermal Pad Considerations (Cont.)

design issues are not properly addressed, the SA4871 4Ω will go into thermal shutdown when driving a 4Ω load.

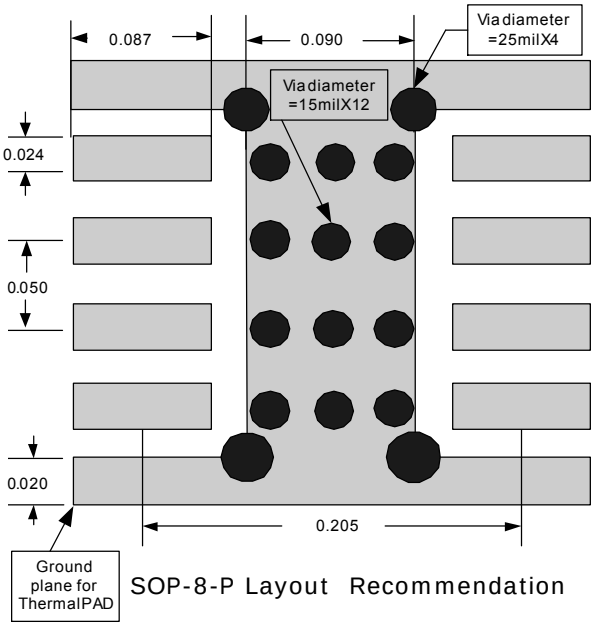
The thermal pad on the bottom of the SA4871 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 12 vias of 15 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the SA4871 junction temperature below the thermal shutdown temperature (150°C). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.



MSOP-8-P Layout Recommendation



SOP-8-P Layout Recommendation

Thermal Considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions.

To calculate maximum ambient temperatures, refer the **"Power Dissipation vs. Output Power"** graphs. Given θJA, the maximum allowable junction temperature (T_{JMAX}), and the total internal dissipation (P_D), the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the SA4871 is 150°C. The internal dissipation figures are taken from the **Power Dissipation vs. Output Power** graphs.

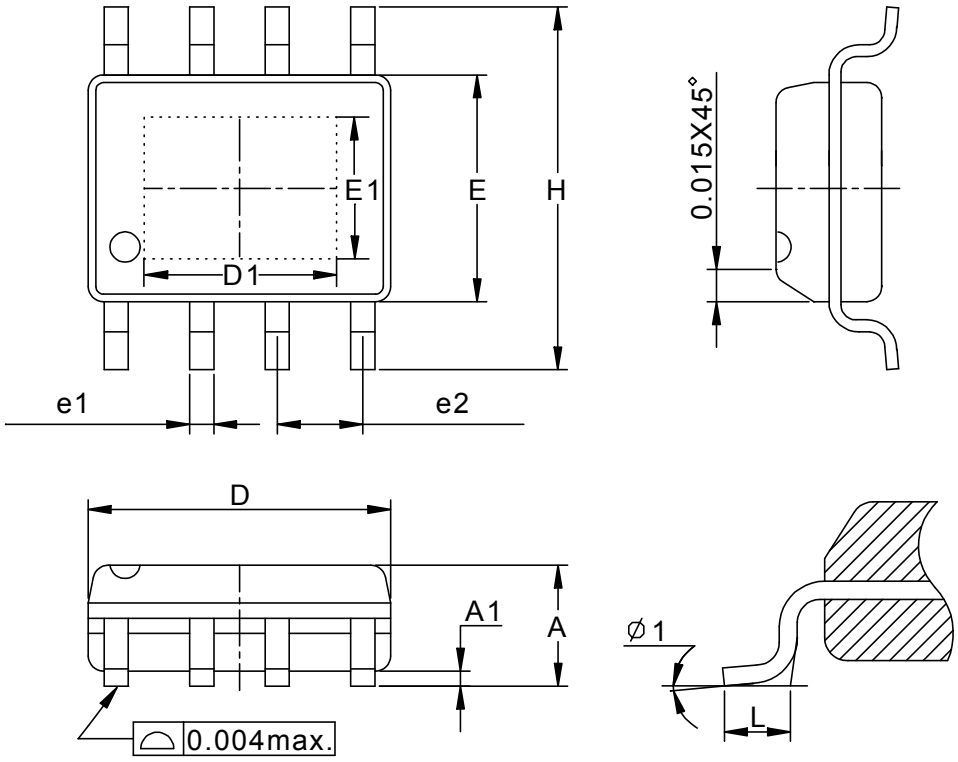
$$T_{AMax} = T_{JMax} - \theta_{JA} P_D \qquad (12)$$

150 - 50(1.3) = 85°C

The SA4871 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

Packaging Information

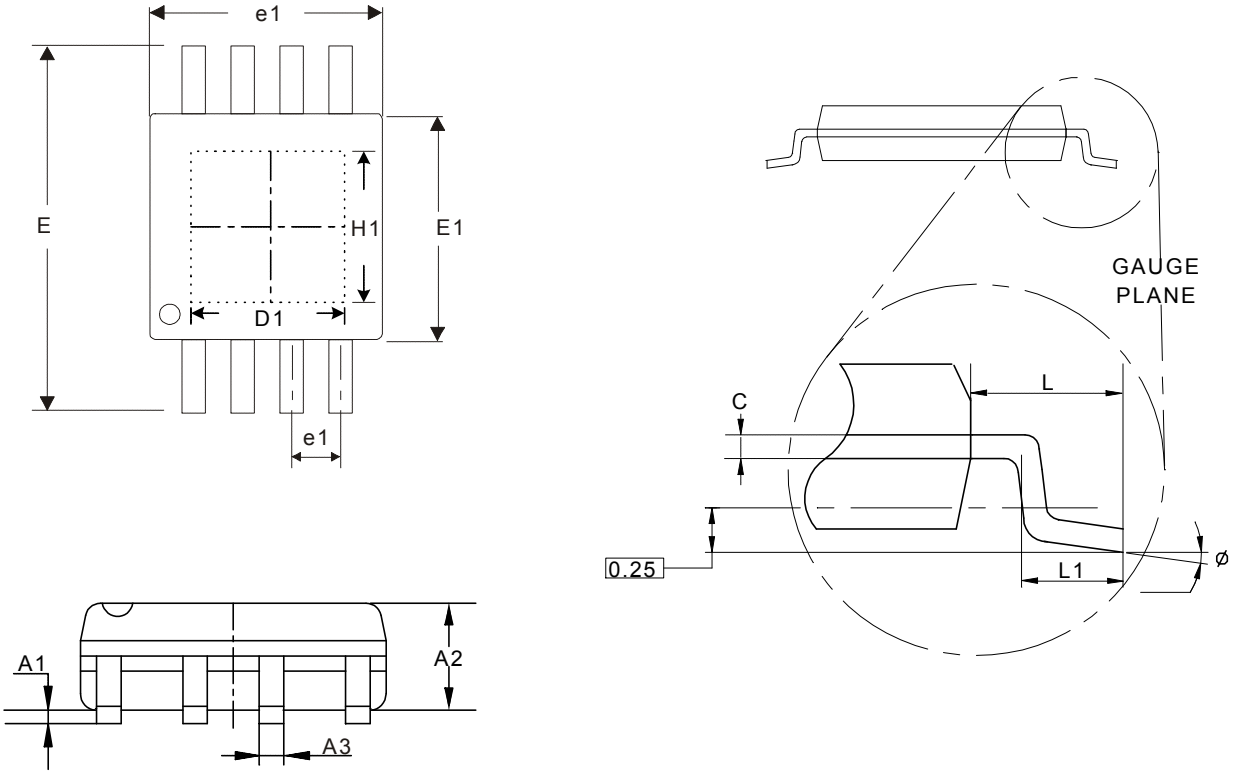
SOP-8-P pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0	0.15	0	0.006
D	4.80	5.00	0.189	0.197
D1	3.00REF		0.118REF	
E	3.80	4.00	0.150	0.157
E1	2.60REF		0.102REF	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

Packaging Information

MSOP-8-P

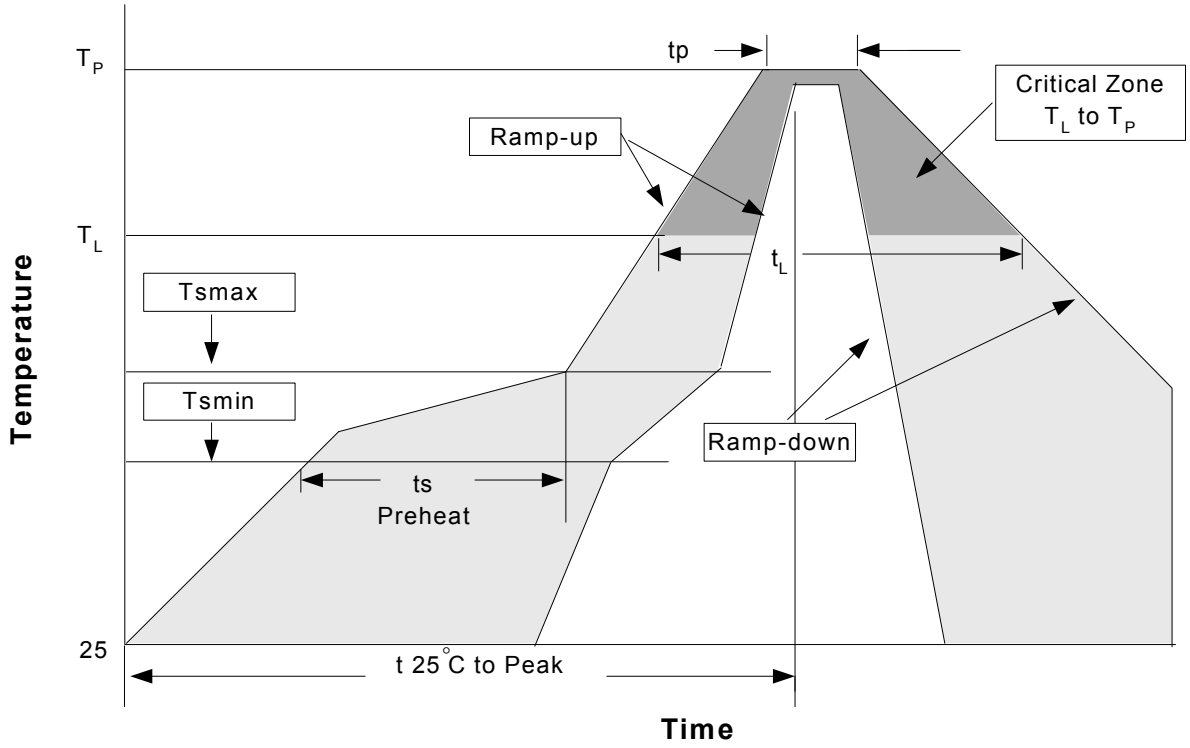


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A1	0.06	0.15	0.002	0.006
A2	0.86 TYP		0.34 TYP	
A3	0.25	0.4	0.01	0.0126
C	0.13	0.23	0.005	0.009
e	0.65 TYP		0.0256 TYP	
e1	2.90	3.1	0.114	0.122
E	4.8	5.0	0.189	0.197
E1	2.90	3.1	0.114	0.122
D1	2.146 REF		0.0845 REF	
H1	1.740 REF		0.0685 REF	
L	0.9	1.0	0.036	0.039
L1	0.45	0.65	0.018	0.026
ϕ	6°		6°	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

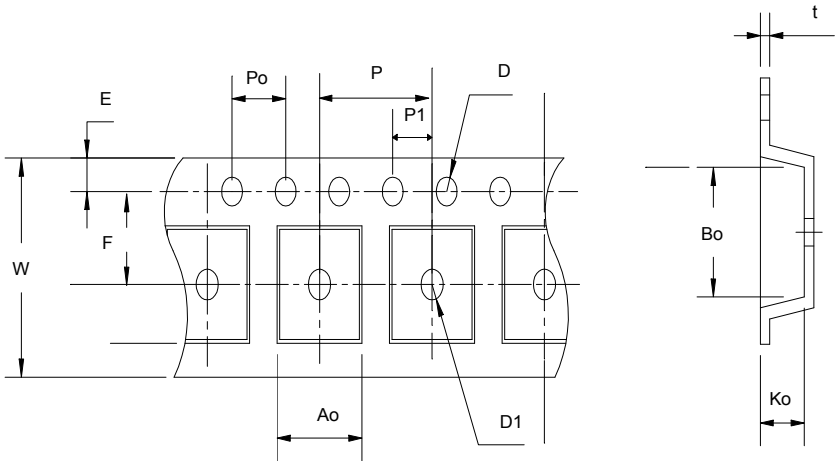
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

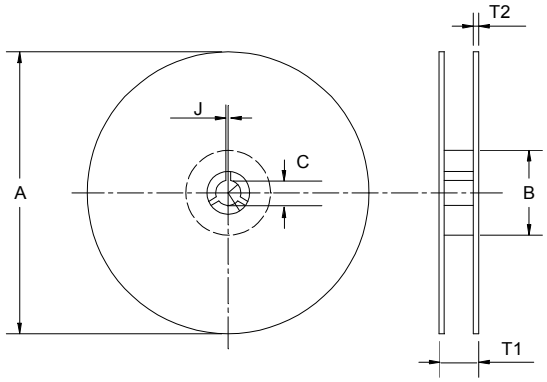
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimensions



Carrier Tape & Reel Dimensions (Cont.)



Carrier Tape & Reel Dimensions

Application	A	B	C	J	T1	T2	W	P	E
M/SOP-8-P	330±1	62 ± 1.5	12.75 + 0.1 5	2 + 0.5	12.4 +0.2	2± 0.2	12 + 0.3 - 0.1	8± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0.1	1.55±0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0.1	2.1± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8-P	12	9.3	2500
M/SOP- 8-P	12	9.3	3000

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