

### General Description

The SA52106 is a six half-bridge motor driver solution for automotive, industrial and other mechatronic applications. The half-bridges are fully controllable to achieve a forward, reverse, coasting and braking operation of motor. All the functions can be programmed through serial peripheral interface (SPI).

The SA52106 provides internal shutdown functions with an nFAULT output pin to alert the system when a fault occurs. Such as over current protection, open load detection, under voltage lockout, over voltage lockout and thermal shutdown. The device is packaged in TSSOP-24 with exposed pad.

### Features

- 6 Half-bridge Outputs
- 4.5V to 32V Operating Voltage
- Up to 1A Output Current for Each Output
- Low-power Sleep Mode
- Compatible with 5V/3.3V System
- Serial Peripheral Interface, up to 5MHz
- Daisy Chain Functionality
- PWM Capable Output for Frequency 80Hz, 100Hz, 200Hz and 2kHz with 8-Bit Duty Cycle Resolution
- Integrated Protection: Overcurrent Protection (OCP), Short Circuit Protection (SCP), Open Load Detection (OLD), Under Voltage Lockout (UVLO), Over Voltage Protection (OVP) and Thermal Shutdown (TSD)
- nFAULT Pin Output
- AEC-Q100 Qualified

### Applications

- Automotive
- HVAC
- DC Brushed Motors
- LED

### Typical Application

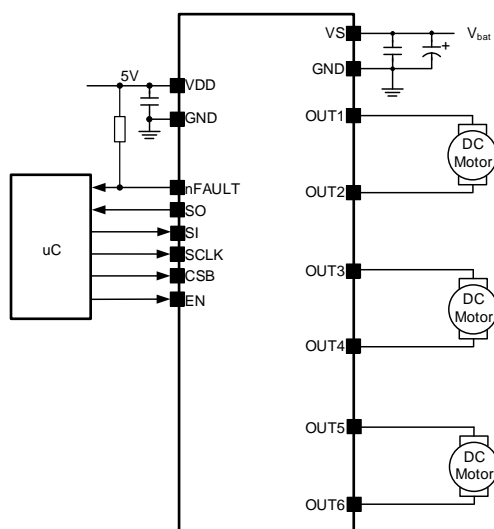


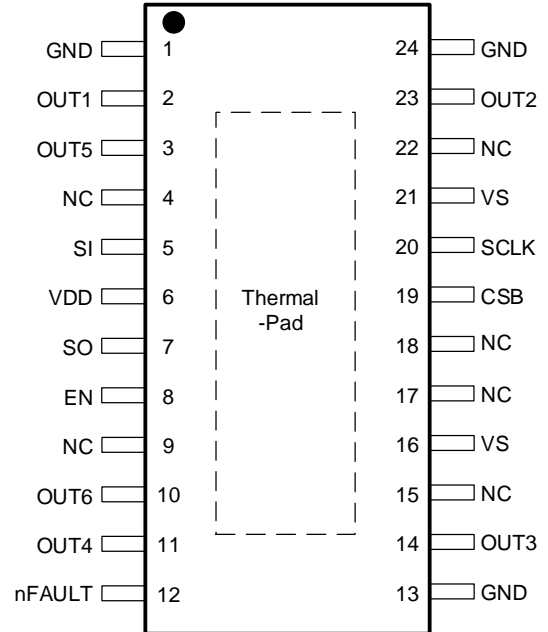
Figure 1. Typical Application Circuit

## Ordering Information

Ordering Part Number	Package Type	Top Mark
SA52106HHP	TSSOP24E RoHS Compliant and Halogen Free	HEJxyz

*x=year code, y=week code, z= lot number code*

## Pinout (Top View)



Pin Name	Pin No.	Pin Description
OUT3	14	Half-bridge Output 3.
VS	16,21	Main power supply.
OUT2	23	Half-bridge Output 2.
GND	1,13,24	Ground. Internal connection to lead frame.
NC	4,9,15,17,18,22	Not connected.
OUT1	2	Half-bridge Output 1
OUT5	3	Half-bridge Output 5.
EN	8	Drive enable pin. Logic high enables the IC. Internal pull-down.
SO	7	Serial data output. 16-bit serial communication output.
VDD	6	Power supply for internal logic.
nFAULT	12	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.
CSB	19	Chip select Bar. Active low serial port operation. Internal pull-up.
SCLK	20	Serial Clock input. Clock input for using SPI communication.
SI	5	Serial data input. 16-bit serial communication input.
OUT6	10	Half-bridge Output 6.
OUT4	11	Half-bridge Output 4.

## Function Block

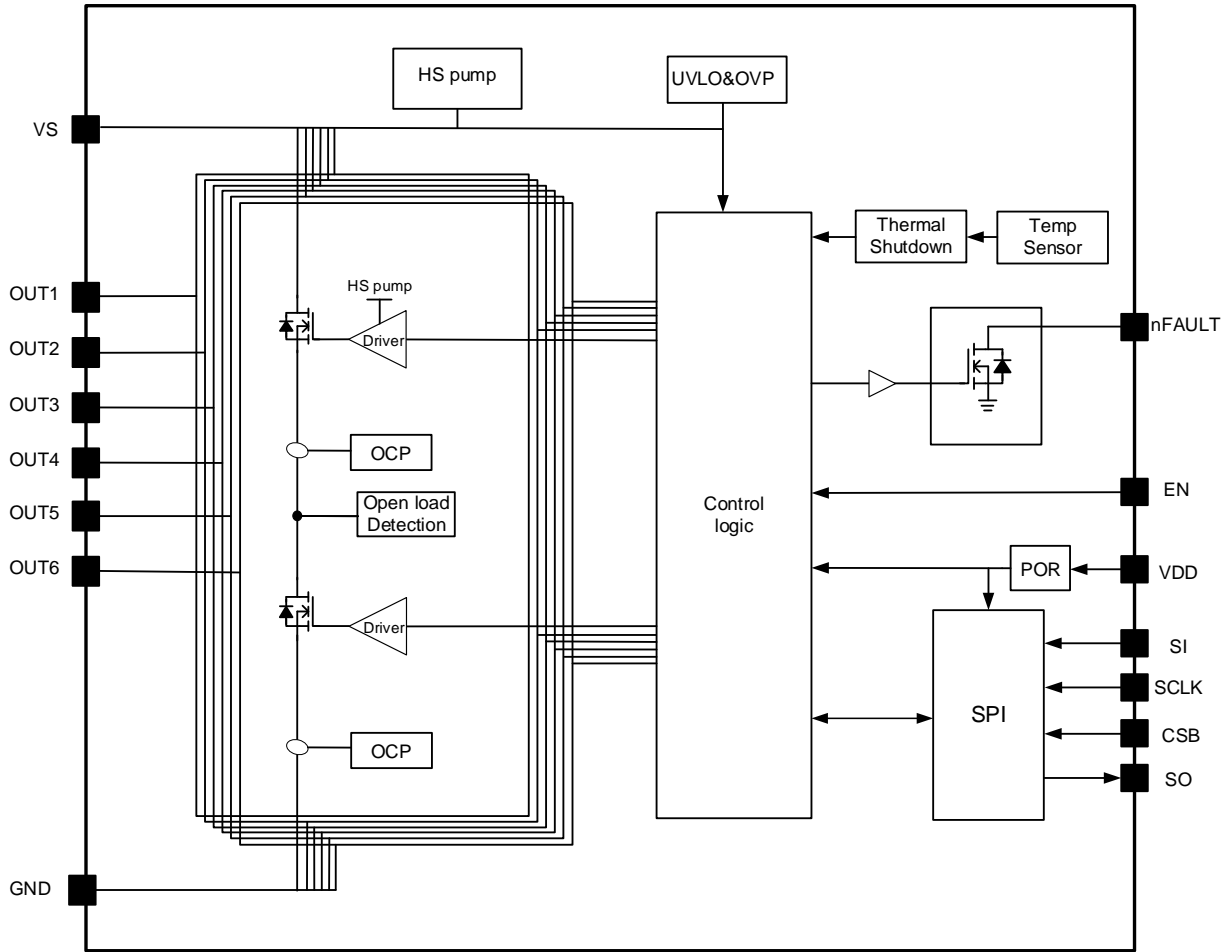


Figure 2. SA52106 Function Block Diagram

## Absolute Maximum Ratings (Note 1)

Parameter		Min	Max	Unit
VS (DC)		-0.3	40	V
OUTx(DC)		-0.3	VS+0.7	
Digital pin (SI, SCLK, CS, SO, EN, nFAULT)		-0.3	VDD+0.3	
VDD		-0.3	5.75	
Continuous Supply Current (VS pins) (Note 2)		0	6	A
Continuous Sink Current (GND pins) (Note 2)		0	6	
Junction Temperature (T <sub>J</sub> )		-40	150	°C
Storage Temperature		-65	150	
V <sub>ESD</sub> Electrostatic Discharge	Human body model (HBM), VS & OUTx pins per AEC-Q100-002		±4000	V
	Human body model (HBM), other pins per AEC-Q100-002		±2000	V
	Charged device model (CDM), per AEC-Q100-011		±750	V

## Thermal Information

Parameter (Note 3)	Typ.	Unit
θ <sub>JA</sub> Junction-to-ambient Thermal Resistance (TSSOP24E)	26	°C/W
θ <sub>JC TOP</sub> Junction-to-case Thermal Resistance (TSSOP24E)	15	

## Recommended Operating Conditions

Parameter	Min	Max	Unit
VS	4.5	32	V
VDD	3	5.5	
Digital pin	0	5.5	
nFAULT pull-up voltage	0	5.5	
nFAULT output current	0	5	mA
Operating Temperature Range (T <sub>A</sub> )	-40	125	°C
Junction Temperature (T <sub>J</sub> )	-40	150	

## Electrical Characteristics

(-40°C < T<sub>A</sub> < 125°C, 4.5V < V<sub>S</sub> < 32V, 3.15V < V<sub>DD</sub> < 5.5V, EN=V<sub>DD</sub>, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supplies						
VS Sleep Mode Current	I <sub>VS_sleep</sub>	VS =13.5V, EN=L, T <sub>A</sub> =25°C		0.35	1	μA
		VS =13.5V, EN=L, T <sub>A</sub> =125°C			3.5	μA
VS Standby Mode Current	I <sub>VS_standby</sub>	VS=13.5V, EN=H, Driver=OFF, T <sub>A</sub> =25°C		0.35	0.55	mA
		VS=13.5V, EN=H, Driver=OFF, T <sub>A</sub> =125°C			0.55	mA
VS Operating Mode Current	I <sub>VS</sub>	VS=13.5V, EN=H, All High-side FETs=ON, T <sub>A</sub> =25°C		2	3.5	mA
		VS=13.5V, EN=H, All High-side FETs=ON, T <sub>A</sub> =125°C			3.5	mA
VS Undervoltage Lockout Voltage	V <sub>UVLO_FALL</sub>	VS falling	3.8		4.3	V
	V <sub>UVLO_RISE</sub>	VS rising	4		4.5	V
	V <sub>UVLO_HYS</sub>			200		mV
VS Undervoltage Lockout Deglitch Time	t <sub>UVLO</sub>			10		μs
VS Overvoltage Protection	V <sub>OVP</sub>	VS rising, EXT_OVP=0b	21		25	V
		VS falling, EXT_OVP=0b	20		24	V
		VS rising, EXT_OVP=1b	32.6		35.1	V
		VS falling, EXT_OVP=1b	32		34.5	V
	V <sub>OVP_HYS</sub>	Rising to falling threshold, EXT_OVP=0b		1		V
		Rising to falling threshold, EXT_OVP=1b		0.7		V
VS Overvoltage Protection Deglitch Time	t <sub>OVP</sub>			10		μs
VDD Power On Reset Threshold	V <sub>POR_ON</sub>	Supply rising	2.75		3.05	V
VDD Power Off Reset Threshold	V <sub>POR_OFF</sub>	Supply falling	2.6		2.9	V
Logic Undervoltage Hysteresis	V <sub>POR_HYS</sub>	Rising to falling threshold		150		mV
VDD Operating Supply Current	I <sub>VDD</sub>	VS =13.5V, VDD=3.3V, EN=H, all low-side FETs=ON, SPI=ON, T <sub>A</sub> =25°C		3	4	mA
		VS =13.5V, VDD=3.3V, EN=H, all low-side FETs=ON, SPI=ON, T <sub>A</sub> =125°C			4	mA
VDD Standby Mode Current	I <sub>VDD_Standby</sub>	VS=13.5V, VDD=3.3V, EN=H, SPI=OFF, T <sub>A</sub> =25°C		2	3	mA
		VS=13.5V, VDD=3.3V, EN=H, SPI=OFF, T <sub>A</sub> =125°C			3	mA
VDD Sleep Mode Current	I <sub>VDD_SLEEP</sub>	VS=13.5V, VDD=3.3V, EN=L, T <sub>A</sub> =25°C		1.1	2	μA
		VS=13.5V, VDD=3.3V, EN=L, T <sub>A</sub> =125°C			2	μA
Logic Level Input (EN, SI, SCLK, CSB)						
Input Low Voltage	V <sub>IL</sub>		0		0.6	V
Input High Voltage	V <sub>IH</sub>		2			
Input Logic Hysteresis	V <sub>HYS</sub>		200			mV
Input Low Current	I <sub>IL</sub>	V <sub>IN</sub> =0V	-1		1	μA
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> =VDD		60	100	μA
Input Capacitance	C <sub>CAPIX</sub>	(Note 4)		-	15	pF
Open-Drain Output (nFAULT)						
Output Low Voltage	V <sub>OL</sub>	I <sub>sink</sub> =5mA	0		0.4	V
Output High Current	I <sub>OH</sub>	V <sub>OD</sub> =5V	-1		1	μA
Output Capacitance	C <sub>OD</sub>	(Note 4)	-	-	15	pF
Push-Pull Output (SO)						
Output Low Voltage	V <sub>OL</sub>	I <sub>out</sub> =-5mA	0		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>out</sub> =5mA	VDD-0.6		VDD	V
Output Capacitance	C <sub>OD</sub>	(Note 4)			30	pF

Output Low Current	I <sub>OL</sub>	V <sub>SO</sub> =0V	-1		1	μA	
Output High Current	I <sub>OH</sub>	V <sub>SO</sub> =V <sub>VDD</sub>	-1		1	μA	
Power MOSFETs							
High Side MOSFETs on Resistance	R <sub>DS(on)</sub>	I <sub>out</sub> =-300mA	VS=13.5V		0.75	1.6	Ω
Low Side MOSFETs on Resistance		I <sub>out</sub> =300mA	VS=13.5V		0.75	1.6	
Output Rise and Fall Time (HS and LS)	S <sub>L</sub> <sub>rise and fall</sub>	VS =13.5V, 10%-90% R <sub>LOAD</sub> =27Ω, HBx_SR=0b			1		V/μs
		VS =13.5V, 10%-90% R <sub>LOAD</sub> =27Ω, HBx_SR=1b			3.7		V/μs
Output Dead Time (H to L / L to H)	t <sub>DEAD</sub>	VS =13.5V, SR=0, HS/LS driver OFF to LS/HS driver ON		6	15	25	μs
		VS =13.5V, SR=1, HS/LS driver OFF to LS/HS driver ON		2	5	15	μs
Propagation Delay (HS and LS ON/OFF)	t <sub>PD</sub>	High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=0		3	6	15	μs
		High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=1		1	3	6	μs
Source Leakage Current	I <sub>source_LC</sub>	OUTx=0V, EN=H			6	10	μA
		OUTx=0V, EN=L				1	μA
Sink Leakage Current	I <sub>sink_LC</sub>	OUTx=13.5V, EN=H, SR=0b			13.5	20	μA
		OUTx=13.5V, EN=H, SR=1b			13.5	20	μA
		OUTx=13.5V, EN=L				1	μA
PWM Mode							
PWM Switching Frequency	f <sub>PWM</sub>	PWM_CHx_FREQ=00b		56	80	104	Hz
		PWM_CHx_FREQ=01b		70	100	130	Hz
		PWM_CHx_FREQ=10b		140	200	260	Hz
		PWM_CHx_FREQ=11b		1400	2000	2600	Hz
Protections							
Thermal Warning Temperature	T <sub>WARN</sub>	(Note 4)		120	140	170	°C
Thermal Warning Hysteresis	T <sub>WARN_HYS</sub>	(Note 4)			20		°C
Thermal Shutdown Temperature	T <sub>SD</sub>	(Note 4)		150	165	185	°C
Thermal Shutdown Hysteresis	T <sub>HYS</sub>	(Note 4)			20		°C
Over Current Shutdown (Source)	I <sub>OCSO</sub>	VDD=5V, VS=13.5V		-2.3	-1.8	-1.3	A
Over Current Shutdown (Sink)	I <sub>OCSI</sub>	VDD=5V, VS=13.5V		1.3	1.8	2.3	A
Over Current Shutdown Delay Time	t <sub>OC</sub>	OCP_DEG=000b		6	10	14	μs
		OCP_DEG=001b(Note 4)		2.6	5	7.9	μs
		OCP_DEG=010b(Note 4)		0.4	2.5	5.9	μs
		OCP_DEG=011b		0.1	1	3.4	μs
		OCP_DEG=100b		38.2	60	76.6	μs
		OCP_DEG=101b(Note 4)		23.1	40	51.9	μs
		OCP_DEG=110b(Note 4)		18.5	30	41.5	μs
		OCP_DEG=111b(Note 4)		8.4	20	31.6	μs
Open Load Detection Current	I <sub>OLD</sub>	High-side or Low-side		2	9	18	mA
Open Load Detection Current in Low Current OLD Mode	I <sub>OLD_LOW</sub>	Low side		0.2	0.8	2	mA
Open Load Detection Delay Time	t <sub>OL</sub>	Active OLD (Continuous Mode)		2	3	4	ms
		Active OLD (PWM Mode)		150	200	300	μs

## Serial Peripheral Interface

(-40°C < T<sub>A</sub> < 125°C, 4.5V < V<sub>S</sub> < 32V, 3.15V < V<sub>DD</sub> < 5.5V, EN = V<sub>DD</sub>, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCLK Frequency	f <sub>CLK</sub>	(Note 4)			5	MHz
SCLK High Time	t <sub>CLKH</sub>	(Note 4)	100			ns
SCLK Low Time	t <sub>CLKL</sub>	(Note 4)	100			ns
SI Setup Time	t <sub>SU_SI</sub>	(Note 4)	40			ns
SI Hold Time	t <sub>HD_SI</sub>	(Note 4)	60			ns
SO Output Data Delay Time	t <sub>DLY_SO</sub>	SCLK high to SO valid (Note 4)			60	ns
CSB Setup Time	t <sub>SU_CSB</sub>	(Note 4)	100			ns
CSB Hold Time	t <sub>HD_CSB</sub>	(Note 4)	100			ns
CSB Disable Delay Time	t <sub>DIS_CSB</sub>	CSB high to SO High-Z (Note 4)		30		ns
CSB Minimum High Time before Active Low	t <sub>HI_CSB</sub>	(Note 4)	600			ns
EN Low Valid Time	t <sub>ENL</sub>	V <sub>DD</sub> =5V, EN going low 50% to OUTx turning off 50% (Note 4)	10			μs
EN High to SPI Valid	t <sub>ENH_SPIV</sub>	(Note 4)			100	μs

**Note 1:** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.

**Note 2:** Power dissipation and thermal limits must be observed.

**Note 3:** θ<sub>JA</sub> are measured under the natural convention at T<sub>A</sub> = 25°C on a highly effective four layer thermal conductivity test board with thermal via.

**Note 4:** Guaranteed by design.

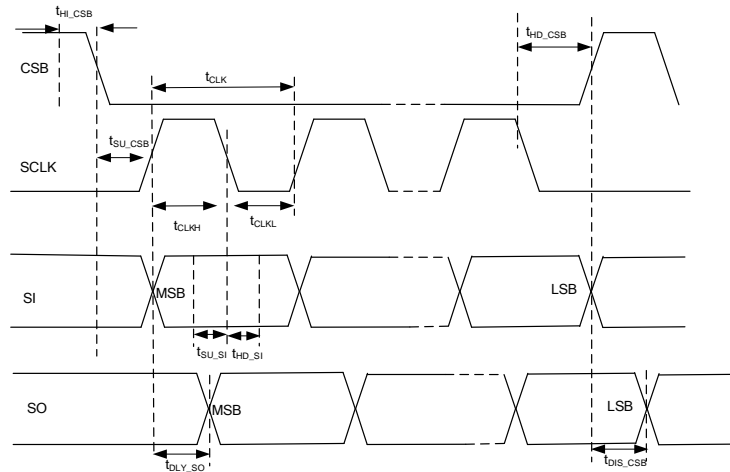
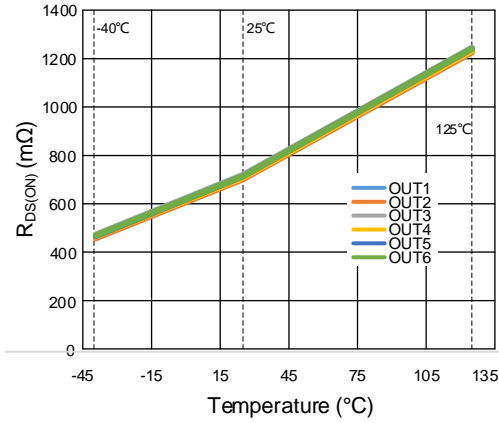


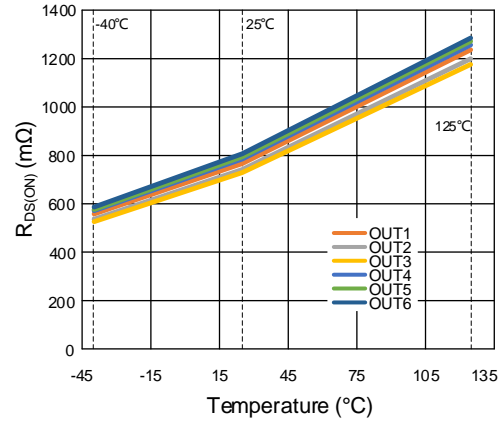
Figure 3. SPI Timing

## Typical Performance Characteristics

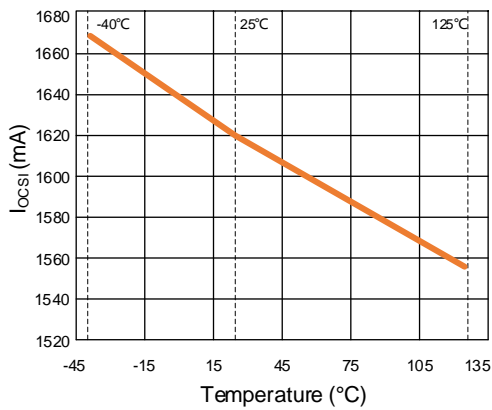
High Side MOSFETs on Resistance



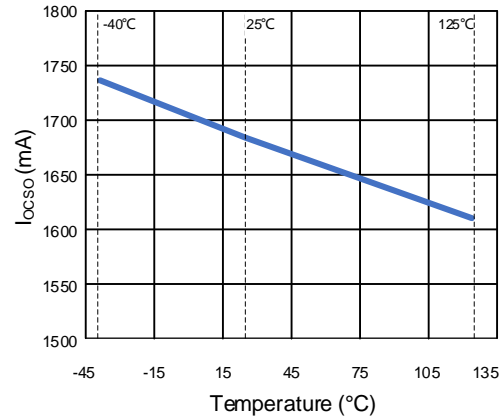
Low Side MOSFETs on Resistance



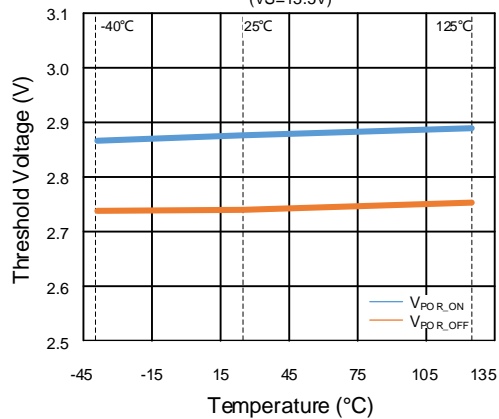
Low Side MOSFETs Over Current Limit  
( $V_S=13.5V$ )



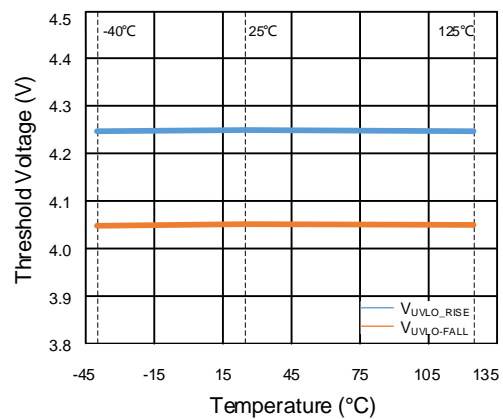
High Side MOSFETs Over Current Limit  
( $V_S=13.5V$ )



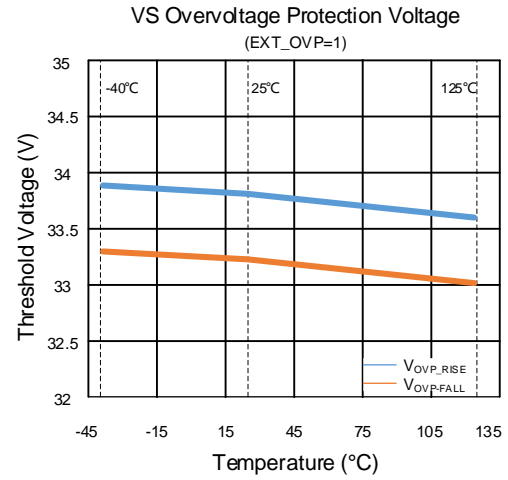
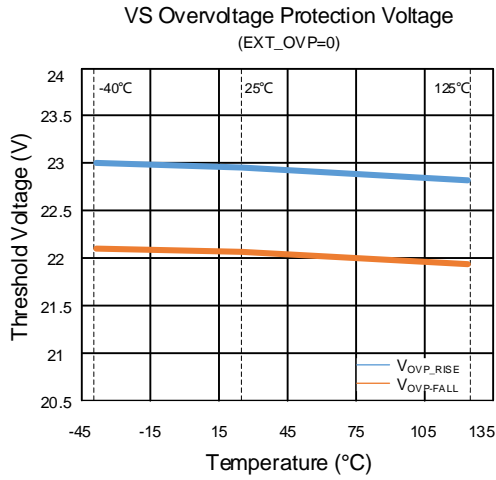
VDD Power On Reset and Power Off Reset  
( $V_S=13.5V$ )



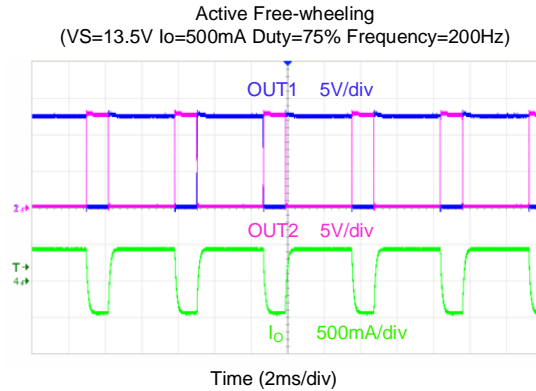
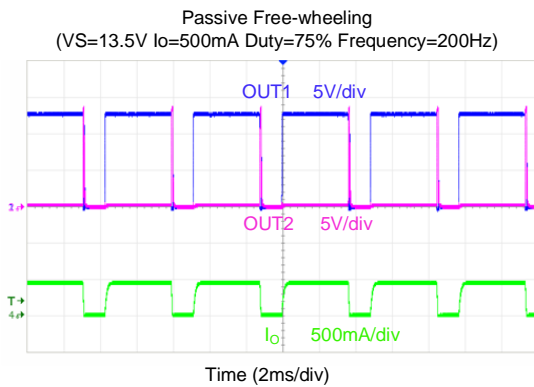
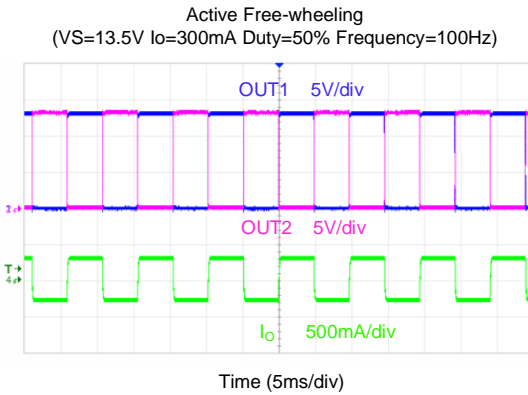
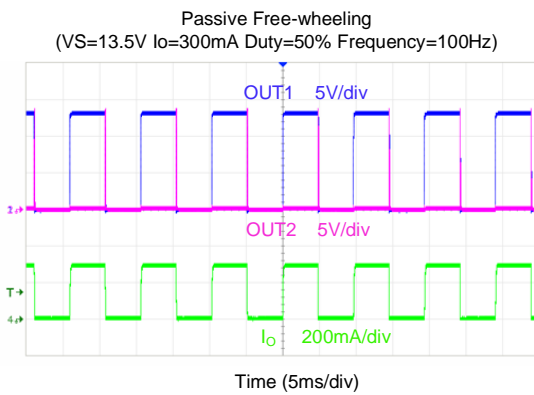
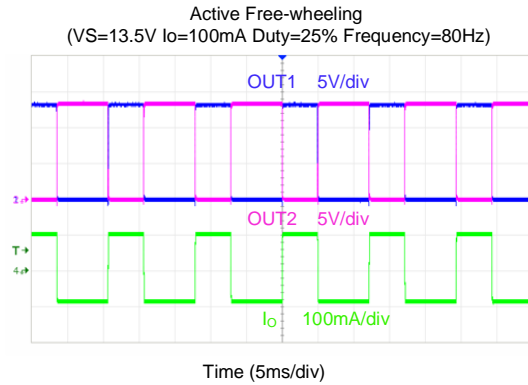
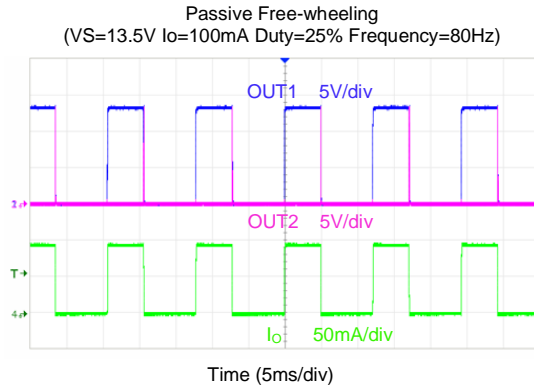
VS Undervoltage Lockout Voltage  
( $V_{DD}=5V$ )







## Operation Waveform



## Function Description

The SA52106 is a six half-bridge motor driver solution for automotive, industrial and other mechatronic applications. It can be configured as 3 independent H-bridges. The half-bridges are designed to support 1A per half-bridge and 6A maximum current from VS/GND pins.

The device supports a standard 16-bit, 5-MHz serial peripheral interface (SPI). The device is also equipped with a daisy-chain functionality which allows connecting multiple devices using a single CSB line and saving on multiple resources.

## Power Supply

VS powers the MOSFETs, and VDD powers the logic circuits. After the VS powers up, the drivers are allowed to turn on. All the drivers are initialized in the off condition, and remain off regardless of VDD status. VDD power up resets all the internal logic. All the internal registers are cleared on VDD POR.

## Driving Control

The device can be configured as H-bridge, high-side or low-side driver. The half-bridge outputs of the device are intended to drive motor or LEDs loads. The half-bridge drivers can be programmed to drive loads continuously (without PWM) or in chopping mode (with PWM) and in parallel operation for driving high current.

## Continuous Mode (Without PWM)

The half-bridge drivers can be programmed to drive loads continuously (without PWM). The device can set the high-side enable bits (HBx\_HS\_EN) and low-side enable bits (HBx\_LS\_EN) in operation control registers (OP\_CTRL\_1, OP\_CTRL\_2) to switch high-side or low-side individually. In addition, the device will stay in Hi-Z mode if high-side and low-side switch are set high of a particular half-bridge. An illustration is shown in Figure 4 and Figure 5, OUT1 and OUT2 driving a DC brush motor. With this configuration. The motor will work in forward direction with high-side FET of OUT1 and low-side FET of OUT2, and the motor current will flow from OUT1 into OUT2. Similarly, if it is switched on the high-side FET of OUT2 and low-side FET of OUT1, the motor will work in reverse, the motor current will flow from OUT2 into OUT1.

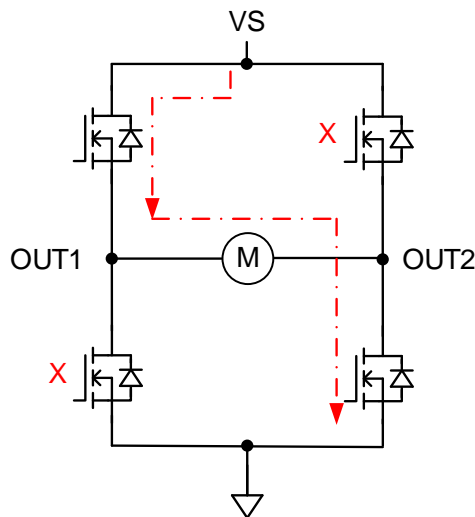


Figure 4. Continuous Mode (Forward)

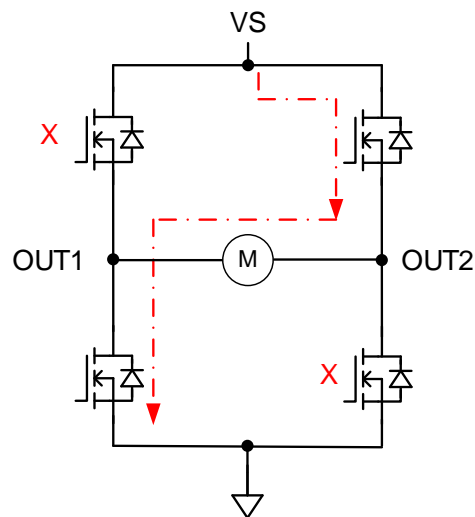


Figure 5. Continuous Mode (Reverse)

If the motor initially runs in forward or reverse direction, then switches high-side and low-side off, the H-bridge will operation in coast mode. Because of the inductance energy, the current will continue to flow in motor and take the path flow through the body diodes of FETs, shown in Figure 6 and Figure 7.

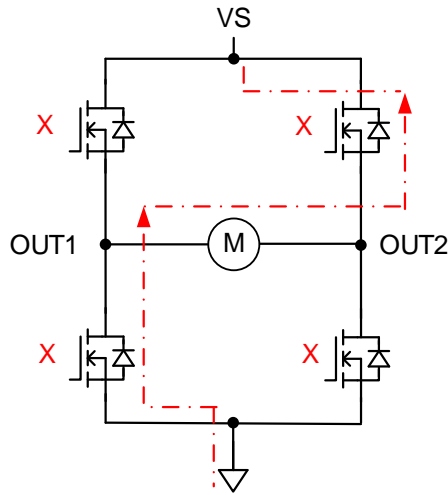


Figure 6. Coast-From Forward

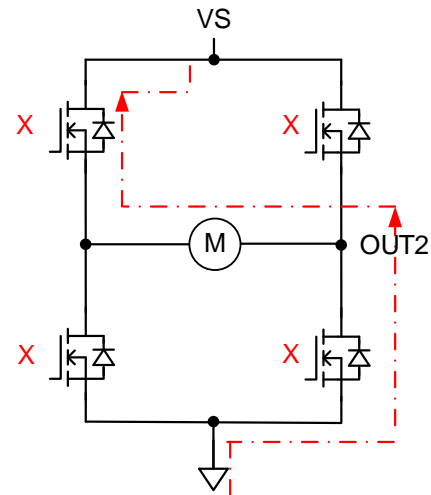


Figure 7. Coast-From Reverse

If the motor initially runs in forward or reverse direction, then switches either high-side or low-side on, the H-bridge will operation in brake mode. For the low-side braking, both low-side FETs of the driver are turned on. Similarly, both high-side FETs of the driver are turned on for the high-side braking, shown in Figure 8 and Figure 9.

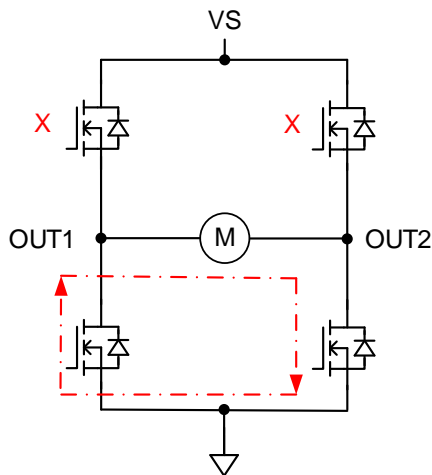


Figure 8. Brake-Low-Side

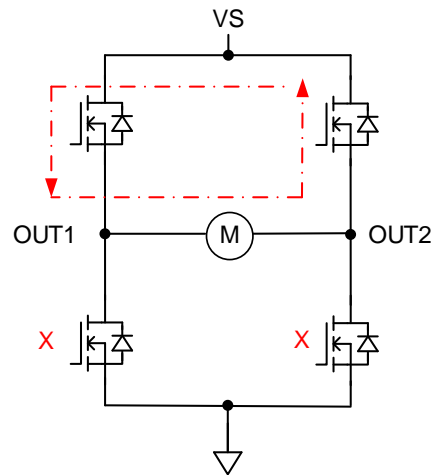


Figure 9. Brake-High-Side

## Chopping Mode (With PWM)

Each half-bridge can be configured into PWM mode to drive an inductive load (e.g., DC brush motor), and has been allocated eight PWM channels with individual duty cycle settings with 8-bit resolution. The device has four PWM frequency 80-Hz, 100-Hz, 200-Hz and 2-kHz for different application.

The PWM chopping mode operation is done in five steps as follows and explained in detail below:

1. PWM Configuration
2. Free-wheeling Mode (Synchronous Rectification) Disable/Enable
3. PWM Channels Mapping
4. PWM Channels Configuration (PWM Frequency and PWM Duty)
5. Half-bridge Enable

## PWM Configuration

Half-bridge can be configured into continuous mode or chopping mode (PWM mode) by using the PWM control register (PWM\_CTRL\_1). The HBx\_PWM bit = 1 is set to enable the PWM switching mode, otherwise it will operate in continuous mode. The PWM\_CHx\_DIS bit in PWM control register (PWM\_CTRL\_2) is set to enable the PWM generator.

## Free-Wheeling Mode (Synchronous Rectification) Disable/Enable

The device supports to select the synchronous rectification mode by setting the HBx\_FW bit in free-wheeling control registers (FW\_CTRL\_1 and FW\_CTRL\_2). Figure 10 shows when the HBx\_FW is disabled, the current path will go through the high-side diode during the PWM off time. If the HBx\_FW is enabled, it will open the FET to create a current path. Figure 11 shows example of the synchronous rectification, where the high-side FET of OUT2 half-bridge is turned on when the low-side FET of same half-bridge is turned off in a PWM cycle.

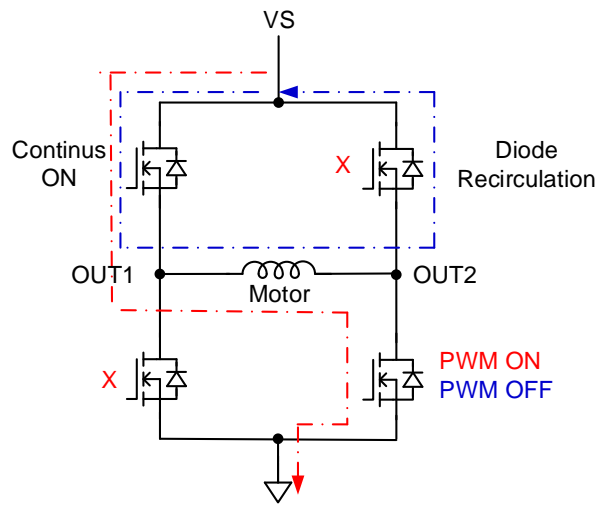


Figure 10. PWM Mode (Synchronous Rectification =OFF)

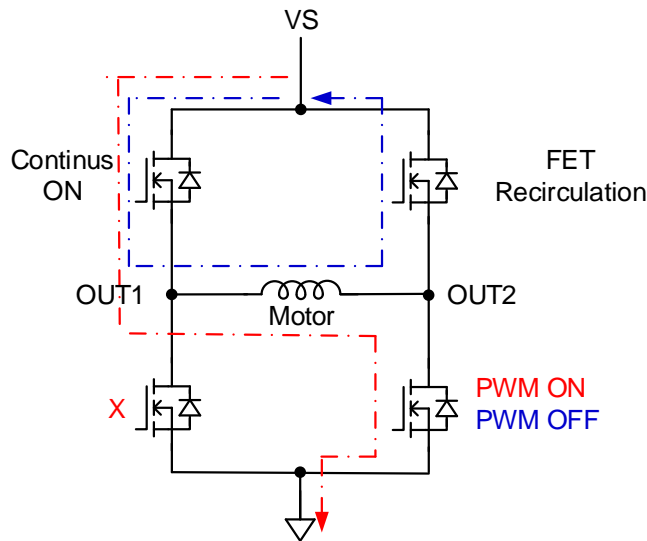


Figure 11. PWM Mode (Synchronous Rectification =ON)

## PWM Channels Mapping

By configuring the PWM map control registers (PWM\_MAP\_CTRL\_x), the any of the OUTx half bridge outputs can map different PWM generator, because the device includes 8 PWM generators. The HBx\_PWM\_MAP bits are used to map any of the 8 channels, as shown in Table 1.

Table 1. PWM Mapping

HBx_PWM_MAP BITS	PWM CHANNEL
HBx_PWM_MAP=000b	Channel 1 selected for OUTx
HBx_PWM_MAP=001b	Channel 2 selected for OUTx
HBx_PWM_MAP=010b	Channel 3 selected for OUTx
HBx_PWM_MAP=011b	Channel 4 selected for OUTx
HBx_PWM_MAP=100b	Channel 5 selected for OUTx
HBx_PWM_MAP=101b	Channel 6 selected for OUTx
HBx_PWM_MAP=110b	Channel 7 selected for OUTx
HBx_PWM_MAP=111b	Channel 8 selected for OUTx

## PWM Channels Configuration (PWM Frequency and PWM Duty)

Each PWM generator can be configured different frequency and duty independently. The PWM frequency of each channel is controlled by the PWM frequency control register (PWM\_FREQ\_CTRL\_x). The PWM\_DUTY\_CHx bit of the PWM duty control register (PWM\_DUTY\_CTRL\_x) is used to control PWM duty output, detailed shown in Table 2.

Table 2. PWM Frequency

HBx_PWM_MAP BITS	PWM CHANNEL
PWM_CHx_FREQ=00b	80Hz
PWM_CHx_FREQ =01b	100Hz
PWM_CHx_FREQ =10b	200Hz
PWM_CHx_FREQ =11b	2000Hz

Table 3. PWM Duty Control Channelx Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CHx	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxx) × 1/255

## Half-Bridge Enable

After the four steps, the last step is set high-side or low-side enabled. Once the half-bridge is configured for the PWM generation, the half-bridge is enabled by enabling either of the high-side or low-side switch. The HBx\_HS\_EN bit is used to set the high-side enabled, and the HBx\_LS\_EN bit is used to set the low-side enabled in operation control registers (OP\_CTRL\_1, OP\_CTRL\_2).

## Protection Circuits

This device has embedded protective functions such as undervoltage, overvoltage, overcurrent, power on reset, open load, thermal shutdown.

## Half-Bridge Enable

When voltage VS drops below the switch off voltage  $V_{UVLO\_FALL}$ , all output stages are switched off. However, the logic information remains intact and uncorrupted. The VS under-voltage error bit is also latched high in the IC status register (IC\_START), the nFAULT pin is driven low. If VS rises again and reaches the switch on voltage  $V_{UVLO\_RISE}$  threshold, the power stages will automatically be activated and the nFAULT pin will be released. The UVLO error bit remains set until it is cleared through the CLR\_FLT bit.

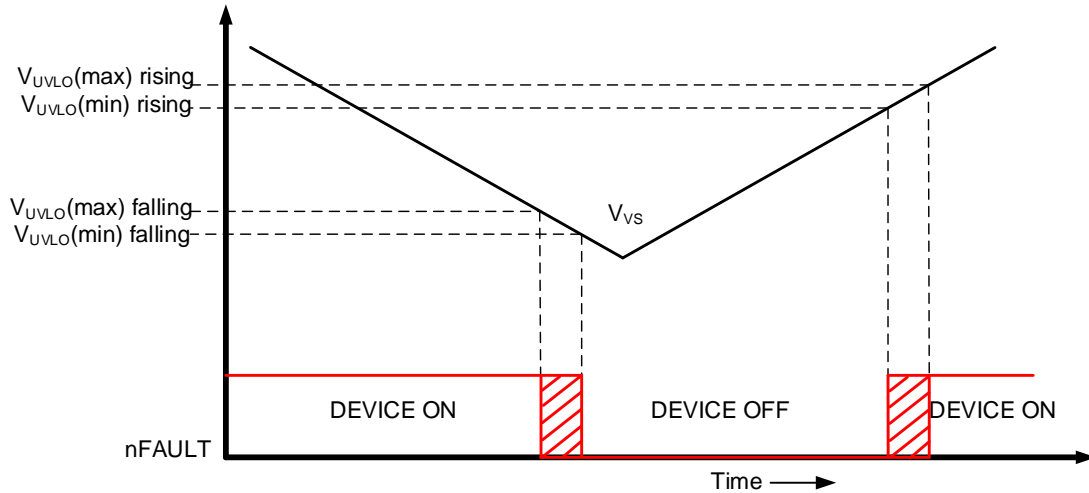


Figure 12. VS UVLO Operation

## Overvoltage Protection (OVP)

In the event the supply voltage  $V_S$  rises above the switch off voltage  $V_{OVP}$ , all output stages are switched off. The VS overvoltage error bit is also latched high in the IC status register (IC\_START), the  $nFAULT$  pin is driven low. If  $V_S$  falls again and reaches the switch-on voltage threshold ( $V_{OVP} - V_{OVP\_HYS}$ ), the power stages will automatically be activated and the  $nFAULT$  pin will be released. The OVP error bit remains set until it is cleared through the CLR\_FLT bit. The device supports an extended overvoltage operation for higher over-voltage range up to 33-V by enabling the EXT\_OVP bit in the configuration (CONFIG\_CTRL) register.

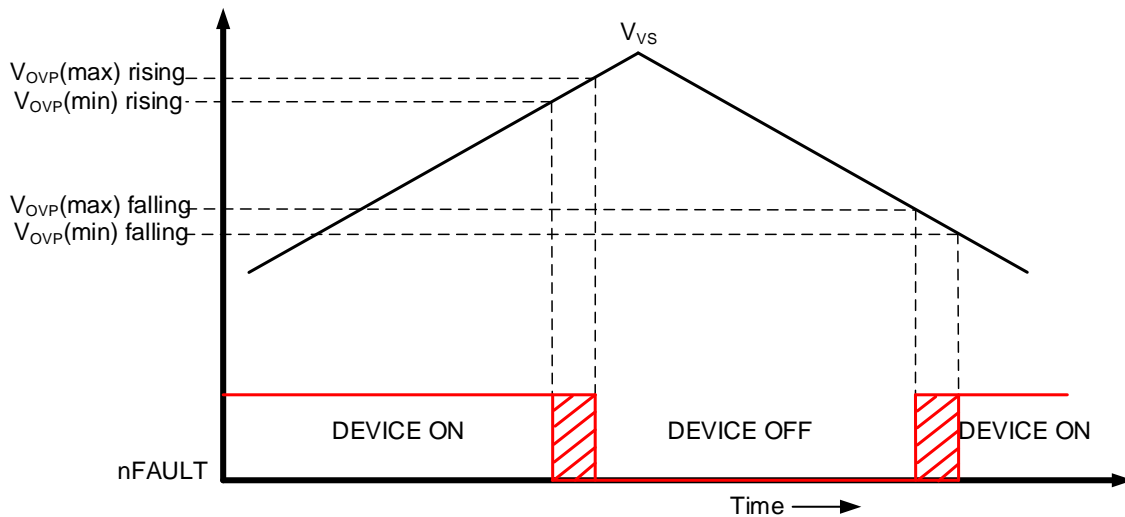


Figure 13. VS OVP Operation

## VDD Power on Reset (POR)

In the event the VDD logic supply decreases below the undervoltage threshold,  $V_{POR\_FALL}$ , the SPI interfaces shall no longer be functional and the device will enter reset mode. The digital block will be initialized and the output stages are switched off to high impedance. The undervoltage reset is released once VDD voltage levels are above the undervoltage threshold,  $V_{POR\_ON}$ . The reset event is reported in CONFIG\_CTRL register by the NPOR bit. The NPOR error bit remains reset and latched low until it is cleared through the CLR\_FLT bit.

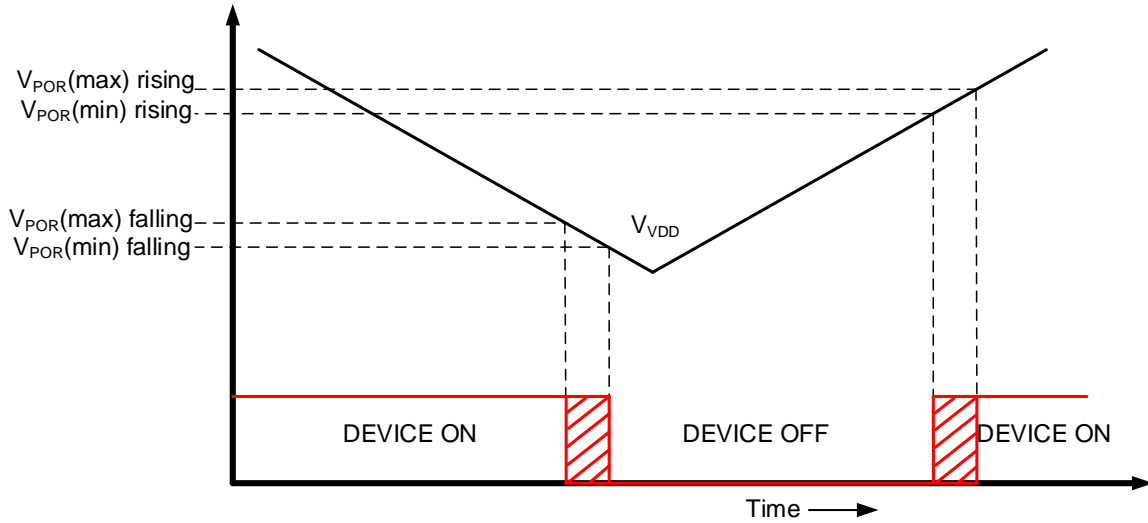


Figure 14. VDD UVLO Operation

## Overcurrent Protection (OCP)

The device offers over current protection. Monitoring the current on the high side and low side drivers at any time, once the current exceeds the overcurrent shutdown detection threshold, the corresponding HS or LS driver is latched off and the corresponding error bit, HBx\_HS\_OCP or HBx\_LS\_OCP is set and latched after the specified shutdown time,  $t_{OC}$ . To resume normal functionality of the power switch (in the event the overcurrent condition disappears or to verify if the failure still exists), user could disable the OCP fault on the nFAULT pin by setting the OCP\_REP bit in the CONFIG\_CTRL register.

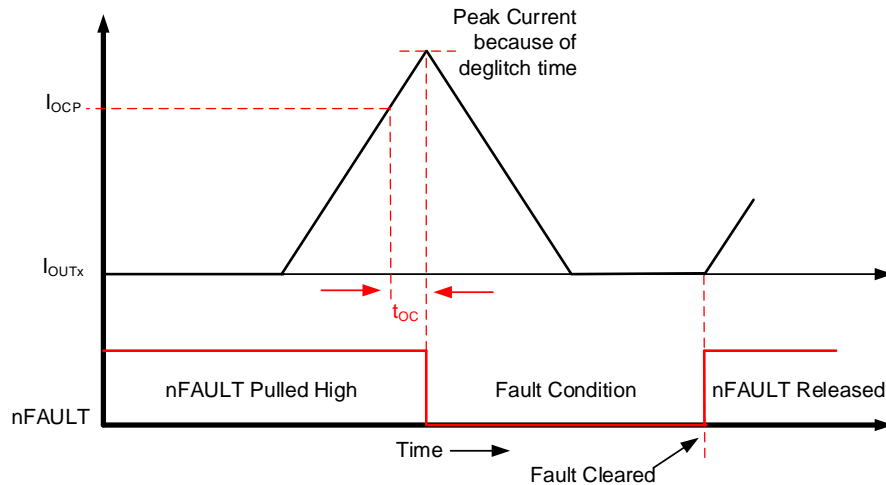


Figure 15. Over Current Protection

## Open Load Detection (OLD)

The open-load detection (OLD) function ensures the proper load connection. The device support active OLD and low-current OLD.

### Active OLD

Active OLD can identify an open-load condition on the OUTx pins while driving a load. As shown in Figure 16, If the motor current  $I_{OUTx}$  is lower than the open-load current threshold ( $I_{OLD}$ ) and the duration of fault condition longer than the open-load deglitch time ( $t_{OLD}$ ). The device will identify an active open-load fault condition. If the active OLD happen, the nFAULT



pin will go down. When the open-load condition is removed and set the CLR\_FLT bit to 1, the nFAULT pin release. The controller also can read the register to know whether there is an open-load condition. The OLD bit in the IC status (IC\_STAT) register will be set to 1 and HBx\_HS\_OLD or HBx\_LS\_OLD bit in the open-load status register (OLD\_STAT\_x) will be set to 1. There are two OLD control registers (OLD\_CTRL\_1 and OLD\_CTRL\_2) are used to configure OLD function. The HBx\_OLD\_DIS bit in OLD\_CTRL\_1 register allows the user to disable OLD on the OUTx pins, OLD on the devices is enabled by default. The OLD\_REP bit in the OLD\_CTRL\_2 register determines whether report on the nFAULT pin. The OLD\_OP bit determines the response of the device to an active OLD fault. If OLD\_OP = 0, the OUTx pins go to the Hi-Z state to stop driving the outputs. Otherwise, the OUTx pins will stay in their previous state and do not react to the OLD fault unless the controller takes action.

## Low-Current OLD

The device also includes a low-current OLD mode which is similar with active open-load detection. The difference between low-current open-load and active open-load is the current detection threshold. The current detection threshold is around 10x lower than the active open-load detection scheme. In addition, the low-current open-load only work in the low-side MOSFET. Enable the low-current OLD mode will also disable the high-side OLD for the particular half-bridge. As shown in Figure 17, If the motor current  $I_{OUTx}$  is lower than the open-load current threshold ( $I_{OLD\_LOW}$ ) and the duration of fault condition longer than the open-load deglitch time ( $t_{OLD}$ ). The device will identify a low-current open-load fault condition. If the low-current OLD happen, the nFAULT pin will go down. When the open-load condition is removed and set the CLR\_FLT bit to 1, the nFAULT pin release. The controller also can read the register to know whether there is an open-load condition. The OLD bit in the IC status (IC\_STAT) register will be set to 1 and HBx\_LS\_OLD bit in the open-load status register (OLD\_STAT\_x) will be set to 1.

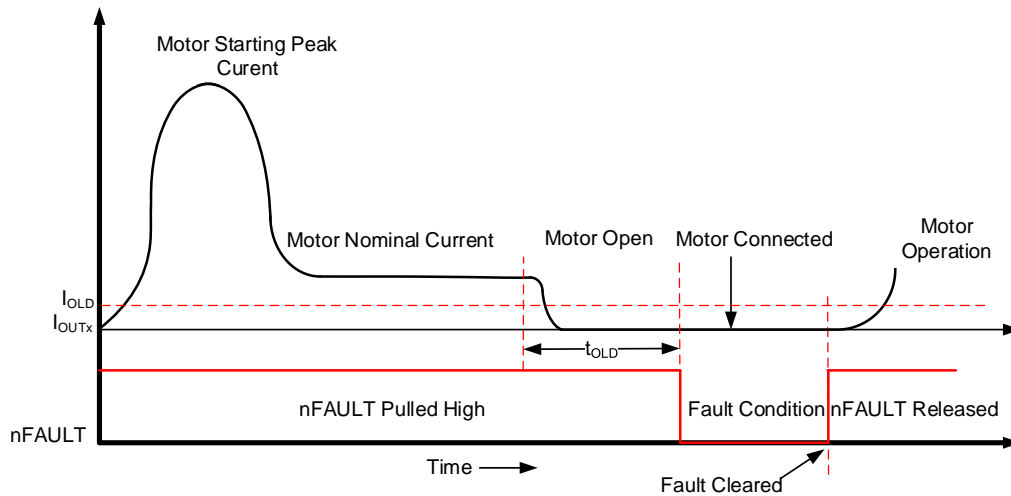


Figure 16. Active Open-load Detection

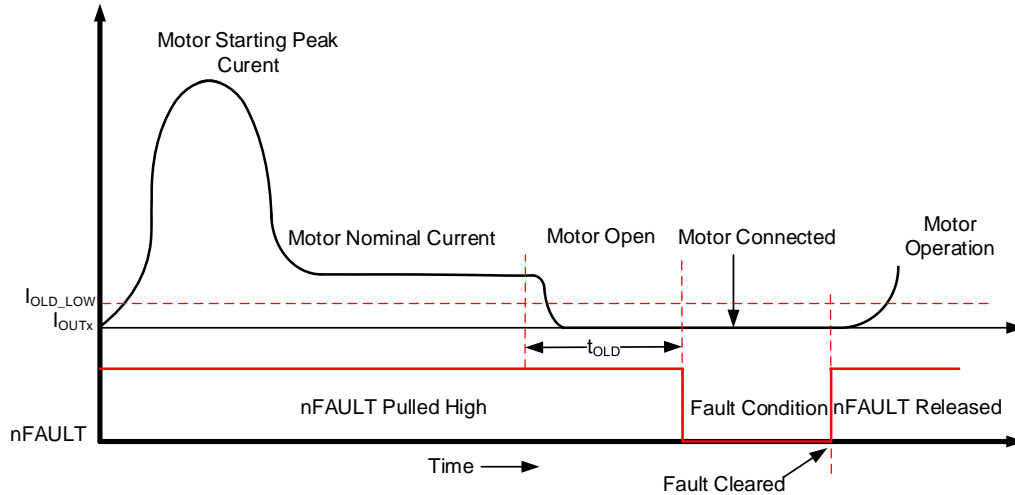


Figure 17. Low-current OLD

## Thermal Warning (OTW)

The device offers temperature warning and shutdown protection. If one or more temperature sensors reach the warning temperature, the temperature pre-warning bit, OTW is set in the IC status (IC\_START) register. This bit is latched and can only be cleared via SPI, but the outputs stages remain activated. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW\_REP) bit in the configuration control (CONFIG\_CTRL) register. The nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning ( $T_{WARN\_HYS}$ ).

## Thermal Shutdown (TSD)

If one or more temperature sensors reach the shut-down temperature threshold, all outputs are latched off and the nFAULT pin is driven low. The OTSD bit is set in the IC status (IC\_START) register. All outputs will be activated and the nFAULT pin is released when the overtemperature shutdown condition is removed and die temperature decreases below the hysteresis point of the thermal warning ( $T_{HYS}$ ). The OTSD bit remains latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR\_FLT bit. This protection feature cannot be disabled.

## Programming Configuration

### SPI

The device supports standard 16-bit SPI to be controlled. The commutation is performed by MSB clocked in first. The SPI interface is a synchronous serial interface for address and data transfer at bit rates of up to 5MHz. It is configured in 8-bit bytes designed to interface with a standard SPI bus. Four pins are used to communicate on the SPI: SCLK (synchronous clock), CSB (chip select, active low), SI (data input to the device for write operations,) and SO (data output from the device for read operations). As shown in Figure 18.

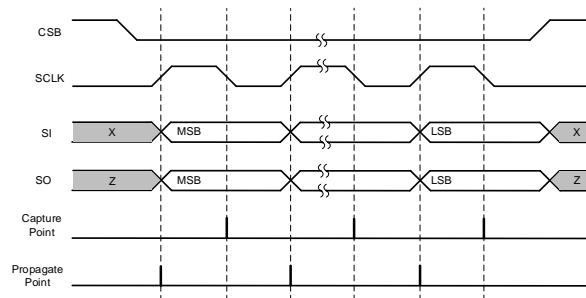


Figure 18. SPI Data Frame

A valid frame must meet the following conditions:

- 1). When the CSB pin is pulled high, any signals at the SCLK and SI pins are ignored and the SO pin is placed in the Hi-Z state
- 2). Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK
- 3). The most significant bit (MSB) is shifted in and out first
- 4). A full 16 SCLK cycles must occur for transaction to be valid
- 5). Data word sent to the SI pin should not be less than or more than 16 bits
- 6). For a write command, the existing data in the register being written to is shifted out on the SO pin following the 8-bit command data

## SPI Format

Each SPI communication starts with one address byte followed by one data byte. The SPI function of the device has 1 R/W bit in bit14, 6 address bits and 8 data bits. The control registers are READ/WRITE registers. To set the control register to READ, bit 14 of the address must be programmed to '1', otherwise '0' for WRITE. While the microcontroller sends the address byte on SI, SO shifts out the IC Status Register data. A further data byte (bit7-bit0) is allocated to either configure the half-bridges or retrieve status information of the device. The SPI Registers have been mapped as shown in Table 6 respectively.

Table 4. SI Input Data Word Format

		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 5. SO Output Data Word Format

			Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	OTSD	OLD	OCF	UVLO	OVP	NPOR	D7	D6	D5	D4	D3	D2	D1	D0

## Daisy Chain

The device supports daisy chain operation with devices with the same SPI protocol shown in Figure 20. The master output (MO) is connected to a slave SI and the first slave SO is connected to the next slave SI to form a chain. The SO of the final slave in the chain will be connected to the master input (MI) to close the loop of the SPI communication frame. In daisy chain configuration, a single chip selects, CSB, and clock signal, SCLK, connected in parallel to each slave device, are used by the microcontroller to control or access the SPI devices. Figure 19 shows the topology when 3 devices are connected in series with waveforms.

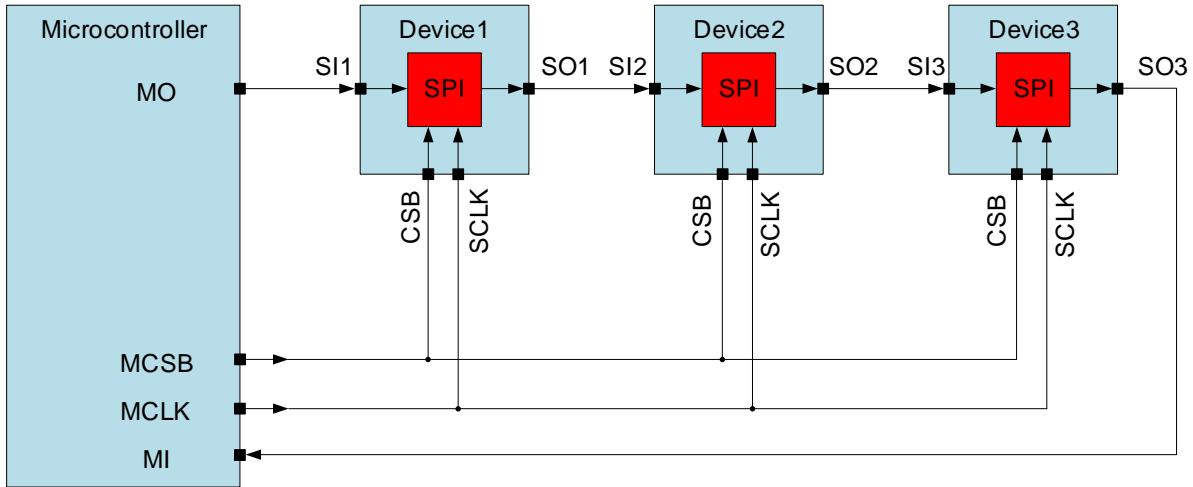


Figure 19. SPI Daisy Chain

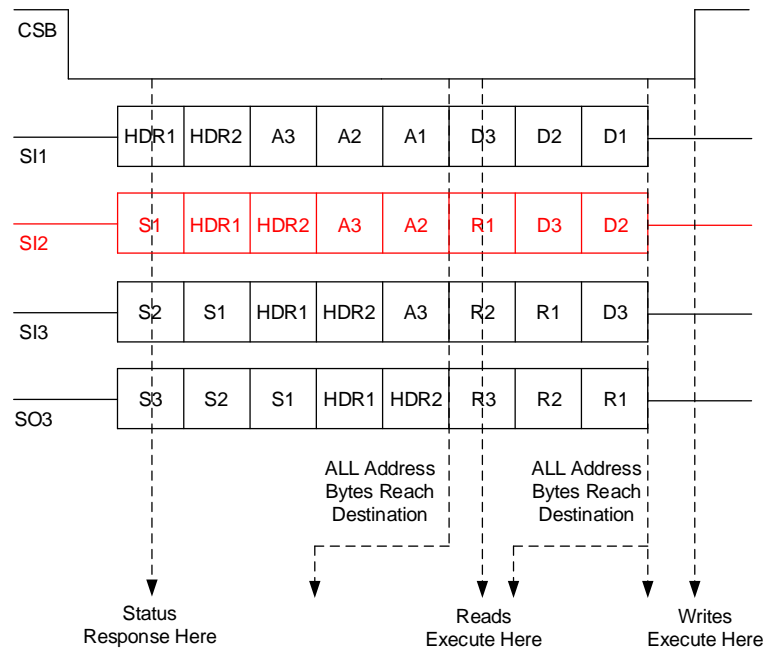


Figure 20. Daisy Chain SPI Operation

The first device in the chain shown above receives data from the master controller in the following format. See SI1 in Figure 20.

- 1). 2 bytes of Header
- 2). 3 bytes of Address
- 3). 3 bytes of Data

After the data has been transmitted through the chain, the master controller receives it in the following format. See SO3 in Figure 20.

- 1). 3 bytes of Status
- 2). 2 bytes of Header (should be identical to the information controller sent)
- 3). 3 bytes of Report

There are two Header bytes containing information of the number of devices and a global clear fault. The N5 to N0 in Header1 shows up to  $2^6-1$  devices can be connected in series per daisy chain connection. The CLR bit in Header2 is a global clear fault command that will clear the fault registers of all the devices. Both two Header bytes must start with 1 and 0.

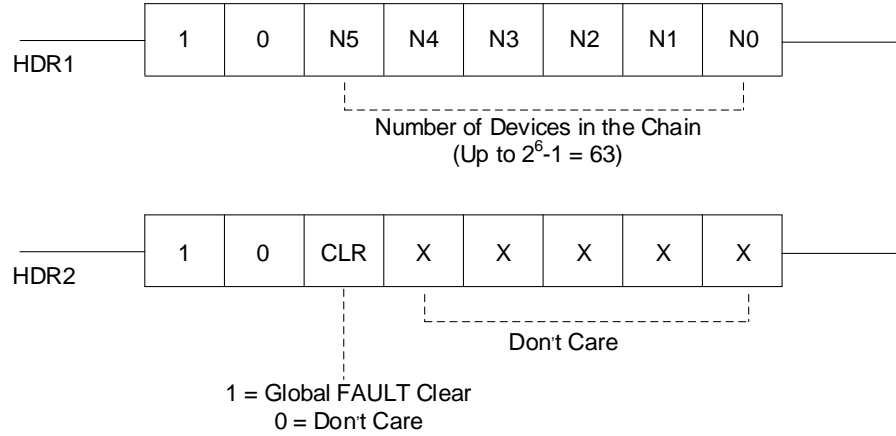


Figure 21. Header Bits

All the device will feedback fault status register in the status byte shown in Figure 22. It will be very convenient for the controller to read fault status and for the device to work efficiently.

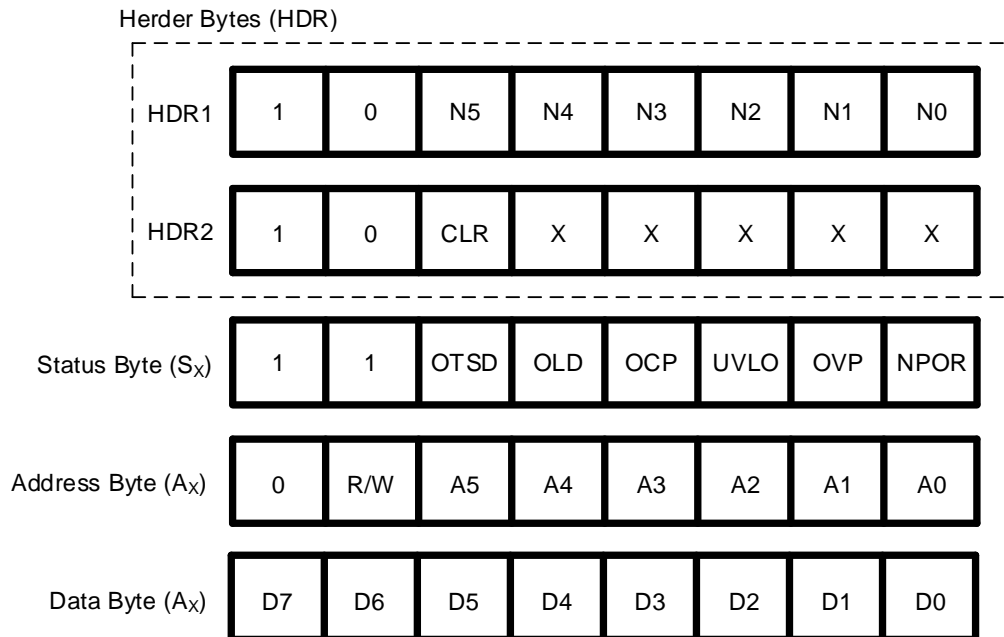


Figure 22. Daisy Chain Read Registers

The device can count the number of Status bytes behind the Header byte to recognize its position. As shown in Figure 20, the device 2 has One Status bytes ( $S_1$ ) behind the Header byte and the device 3 has Two Status bytes ( $S_1$ ,  $S_2$ ) behind the Header byte. When the device knows about its position and the number of devices connected in the chain, the device could load the relevant address and data byte in its buffer and bypasses the other bits. In this way, even the chain has 63 devices, the device still works fleetly.

Table 6. SA52106 Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCF	UVLO	OVP	NPOR	R	00h
OCF_STAT_1	HB4_HS_OCF	HB4_LS_OCF	HB3_HS_OCF	HB3_LS_OCF	HB2_HS_OCF	HB2_LS_OCF	HB1_HS_OCF	HB1_LS_OCF	R	01h
OCF_STAT_2		Reserved			HB6_HS_OCF	HB6_LS_OCF	HB5_HS_OCF	HB5_LS_OCF	R	02h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2		Reserved			HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
CONFIG_CTRL		Reserved			OCF_REP	OTW_REP	EXT_OVP	CLR_FLT	R/W	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	R/W	08h
OP_CTRL_2		Reserved			HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	R/W	09h
OP_CTRL_3					Reserved				R/W	0Ah
PWM_CTRL_1	Reserved		HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	R/W	0Bh
PWM_CTRL_2	Reserved		PWM_CH6_DIS	PWM_CH5_DIS	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	R/W	0Ch
FW_CTRL_1	Reserved		HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	R/W	0Dh
FW_CTRL_2					Reserved				R/W	0Eh
PWM_MAP_CTRL_1	Reserved			HB2_PWM_MAP			HB1_PWM_MAP		R/W	0Fh
PWM_MAP_CTRL_2	Reserved			HB4_PWM_MAP			HB3_PWM_MAP		R/W	10h
PWM_MAP_CTRL_3	Reserved			HB6_PWM_MAP			HB5_PWM_MAP		R/W	11h
PWM_MAP_CTRL_4					Reserved				R/W	12h
PWM_FREQ_CTRL_1	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		R/W	13h
PWM_FREQ_CTRL_2	PWM_CH8_FREQ		PWM_CH7_FREQ		PWM_CH6_FREQ		PWM_CH5_FREQ		R/W	14h
PWM_DUTY_CTRL_1					PWM_DUTY_CH1				R/W	15h
PWM_DUTY_CTRL_2					PWM_DUTY_CH2				R/W	16h
PWM_DUTY_CTRL_3					PWM_DUTY_CH3				R/W	17h
PWM_DUTY_CTRL_4					PWM_DUTY_CH4				R/W	18h
PWM_DUTY_CTRL_5					PWM_DUTY_CH5				R/W	19h
PWM_DUTY_CTRL_6					PWM_DUTY_CH6				R/W	1Ah
PWM_DUTY_CTRL_7					PWM_DUTY_CH7				R/W	1Bh
PWM_DUTY_CTRL_8					PWM_DUTY_CH8				R/W	1Ch
SR_CTRL_1	Reserved		HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	R/W	1Dh
SR_CTRL_2					Reserved				R/W	1Eh
OLD_CTRL_1	Reserved		HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	R/W	1Fh
OLD_CTRL_2	OLD_REP	OLD_OP			Reserved				R/W	20h
OLD_CTRL_3		OCF_DEG			Reserved				R/W	21h
OLD_CTRL_4	Reserved		HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	R/W	22h

## SPI Status Registers

The Status Register are used to report warning and fault conditions. The status registers are read-only registers.

### IC\_STAT

IC\_Status Register (Address =0x00) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	D7	r	
OTSD	D6	r	Temperature shutdown error detection 0 <sub>B</sub> Junction temperature below temperature shutdown threshold 1 <sub>B</sub> Junction temperature has reached temperature shutdown threshold
OTW	D5	r	Temperature pre-warning error detection 0 <sub>B</sub> Junction temperature below temperature pre-warning threshold 1 <sub>B</sub> Junction temperature has reached temperature pre-warning threshold.
OLD	D4	r	Open Load error detection 0 <sub>B</sub> No Open Load 1 <sub>B</sub> Open load
OCP	D3	r	Over current error detection 0 <sub>B</sub> No Over current 1 <sub>B</sub> Over current
UVLO	D2	r	VS Undervoltage error detection 0 <sub>B</sub> No undervoltage on VS detected 1 <sub>B</sub> Undervoltage on VS detected
OVP	D1	r	VS Overvoltage error detection 0 <sub>B</sub> No overvoltage on VS detected 1 <sub>B</sub> Overvoltage on VS detected
NPOR	D0	r	Not Power on Reset (NPOR) detection 0 <sub>B</sub> POR on EN or VDD supply rail 1 <sub>B</sub> No POR

### OCP\_STAT\_1

Overcurrent Error Status of Half-bridge Outputs 1-4 (Address =0x01) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB4_HS_OC	D7	r	High-side (HS) switch of half-bridge 4 overcurrent detection 0 <sub>B</sub> No error on HS4 switch 1 <sub>B</sub> Overcurrent detected on HS4 switch
HB4_LS_OC	D6	r	Low-side (LS) switch of half-bridge 4 overcurrent detection 0 <sub>B</sub> No error on LS4 switch 1 <sub>B</sub> Overcurrent detected on LS4 switch
HB3_HS_OC	D5	r	High-side (HS) switch of half-bridge 3 overcurrent detection 0 <sub>B</sub> No error on HS3 switch 1 <sub>B</sub> Overcurrent detected on HS3 switch
HB3_LS_OC	D4	r	Low-side (LS) switch of half-bridge 3 overcurrent detection

			0 <sub>B</sub> No error on LS3 switch 1 <sub>B</sub> Overcurrent detected on LS3 switch
HB2_HS_OC	D3	r	High-side (HS) switch of half-bridge 2 overcurrent detection 0 <sub>B</sub> No error on HS2 switch 1 <sub>B</sub> Overcurrent detected on HS2 switch
HB2_LS_OC	D2	r	Low-side (LS) switch of half-bridge 2 overcurrent detection 0 <sub>B</sub> No error on LS2 switch 1 <sub>B</sub> Overcurrent detected on LS2 switch
HB1_HS_OC	D1	r	High-side (HS) switch of half-bridge 1 overcurrent detection 0 <sub>B</sub> No error on HS1 switch 1 <sub>B</sub> Overcurrent detected on HS1 switch
HB1_LS_OC	D0	r	Low-side (LS) switch of half-bridge 1 overcurrent detection 0 <sub>B</sub> No error on LS1 switch 1 <sub>B</sub> Overcurrent detected on LS1 switch

## OCP\_STAT\_2

Overcurrent Error Status of Half-bridge Outputs 5-6 (Address =0x02) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	D7:D4	r	Reserved. Always reads as '0'
HB6_HS_OC	D3	r	High-side (HS) switch of half-bridge 6 overcurrent detection 0 <sub>B</sub> No error on HS6 switch 1 <sub>B</sub> Overcurrent detected on HS6 switch
HB6_LS_OC	D2	r	Low-side (LS) switch of half-bridge 6 overcurrent detection 0 <sub>B</sub> No error on LS6 switch 1 <sub>B</sub> Overcurrent detected on LS6 switch
HB5_HS_OC	D1	r	High-side (HS) switch of half-bridge 5 overcurrent detection 0 <sub>B</sub> No error on HS5 switch 1 <sub>B</sub> Overcurrent detected on HS5 switch
HB5_LS_OC	D0	r	Low-side (LS) switch of half-bridge 5 overcurrent detection 0 <sub>B</sub> No error on LS5 switch 1 <sub>B</sub> Overcurrent detected on LS5 switch

## OLD\_STAT\_1

Open Load Error Status of Half-bridge Outputs 1-4 (Address =0x04) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OL	HB4_LS_OL	HB3_HS_OL	HB3_LS_OL	HB2_HS_OL	HB2_LS_OL	HB1_HS_OL	HB1_LS_OL
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB4_HS_OL	D7	r	High-side (HS) switch of half-bridge 4 open load detection 0 <sub>B</sub> No error on HS4 switch (default value) 1 <sub>B</sub> Open load detected on HS4 switch
HB4_LS_OL	D6	r	Low-side (LS) switch of half-bridge 4 open load detection 0 <sub>B</sub> No error on LS4 switch (default value) 1 <sub>B</sub> Open load detected on LS4 switch
HB3_HS_OL	D5	r	High-side (HS) switch of half-bridge 3 open load detection 0 <sub>B</sub> No error on HS3 switch (default value) 1 <sub>B</sub> Open load detected on HS3 switch
HB3_LS_OL	D4	r	Low-side (LS) switch of half-bridge 3 open load detection 0 <sub>B</sub> No error on LS3 switch (default value) 1 <sub>B</sub> Open load detected on LS3 switch



HB2_HS_OL	D3	r	High-side (HS) switch of half-bridge 2 open load detection 0 <sub>B</sub> No error on HS2 switch (default value) 1 <sub>B</sub> Open load detected on HS2 switch
HB2_LS_OL	D2	r	Low-side (LS) switch of half-bridge 2 open loadt detection 0 <sub>B</sub> No error on LS2 switch (default value) 1 <sub>B</sub> Open load detected on LS2 switch
HB1_HS_OL	D1	r	High-side (HS) switch of half-bridge 1 open load detection 0 <sub>B</sub> No error on HS1 switch (default value) 1 <sub>B</sub> Open load detected on HS1 switch
HB1_LS_OL	D0	r	Low-side (LS) switch of half-bridge 1 open load detection 0 <sub>B</sub> No error on LS1 switch (default value) 1 <sub>B</sub> Open load detected on LS1 switch

## OLD\_STAT\_2

Open Load Error Status of Half-bridge Outputs 5-6 (Address =0x05) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				HB6_HS_OL	HB6_LS_OL	HB5_HS_OL	HB5_LS_OL
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	D7:D4	r	Reserved. Always reads as '0'
HB6_HS_OL	D3	r	High-side (HS) switch of half-bridge 6 open load detection 0 <sub>B</sub> No error on HS6 switch 1 <sub>B</sub> Open load detected on HS6 switch
HB6_LS_OL	D2	r	Low-side (LS) switch of half-bridge 6 open load detection 0 <sub>B</sub> No error on LS6 switch 1 <sub>B</sub> Open load detected on LS6 switch
HB5_HS_OL	D1	r	High-side (HS) switch of half-bridge 5 open load detection 0 <sub>B</sub> No error on HS5 switch 1 <sub>B</sub> Open load detected on HS5 switch
HB5_LS_OL	D0	r	Low-side (LS) switch of half-bridge 5 open load detection 0 <sub>B</sub> No error on LS5 switch 1 <sub>B</sub> Open load detected on LS5 switch

## SPI Control Registers

The Control Register are used to configure the device. The control registers are read and write capable.

### CONFIG\_CTRL

Configuration Register (Address =0x07) [reset =0x30]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	OCP_REG	OTW_REG	EXT_OVP	CLR_FLT
r	r	r	r	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7	r	Bit reserved. Always reads '0'.
Reserved	D6	r	Bit reserved. Always reads '0'.
Reserved	D5	r	Bit reserved. Always reads '1'.
Reserved	D4	r	Bit reserved. Always reads '1'.
OCP_REG	D3	r/w	0 <sub>B</sub> Overcurrent condition is reported in nFAULT pin 1 <sub>B</sub> Overcurrent condition warning is not reported in nFAULT pin
OTW_REG	D2	r/w	0 <sub>B</sub> Overtemperature warning is not reported in nFAULT pin 1 <sub>B</sub> Overtemperature warning is reported in nFAULT pin
EXT_OVP	D1	r/w	0 <sub>B</sub> Overvoltage protection threshold is at 21V min.

CLR_FLT	D0	r/w	1 <sub>B</sub> Overvoltage protection threshold is at 32.7V min. 0 <sub>B</sub> Faults not cleared 1 <sub>B</sub> Clear all faults
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## OP\_CTRL\_1

Half-bridge Output Control 1 (Address =0x08) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB4_HS_EN	D7	r/w	Half-bridge output 4 High side switch enable 0 <sub>B</sub> HS4 OFF 1 <sub>B</sub> HS4 ON
HB4_LS_EN	D6	r/w	Half-bridge output 4 Low side switch enable 0 <sub>B</sub> LS4 OFF 1 <sub>B</sub> LS4 ON
HB3_HS_EN	D5	r/w	Half-bridge output 3 High side switch enable 0 <sub>B</sub> HS3 OFF 1 <sub>B</sub> HS3 ON
HB3_LS_EN	D4	r/w	Half-bridge output 3 Low side switch enable 0 <sub>B</sub> LS3 OFF 1 <sub>B</sub> LS3 ON
HB2_HS_EN	D3	r/w	Half-bridge output 2 High side switch enable 0 <sub>B</sub> HS2 OFF 1 <sub>B</sub> HS2 ON
HB2_LS_EN	D2	r/w	Half-bridge output 2 Low side switch enable 0 <sub>B</sub> LS2 OFF 1 <sub>B</sub> LS2 ON
HB1_HS_EN	D1	r/w	Half-bridge output 1 High side switch enable 0 <sub>B</sub> HS1 OFF 1 <sub>B</sub> HS1 ON
HB1_LS_EN	D0	r/w	Half-bridge output 1 Low side switch enable 0 <sub>B</sub> LS1 OFF 1 <sub>B</sub> LS1 ON

## OP\_CTRL\_2

Half-bridge Output Control 2 (Address =0x09) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D4	r/w	Reserved. Always reads as '0'
HB6_HS_EN	D3	r/w	Half-bridge output 6 High side switch enable 0 <sub>B</sub> HS6 OFF 1 <sub>B</sub> HS6 ON
HB6_LS_EN	D2	r/w	Half-bridge output 6 Low side switch enable 0 <sub>B</sub> LS6 OFF 1 <sub>B</sub> LS6 ON
HB5_HS_EN	D1	r/w	Half-bridge output 5 High side switch enable 0 <sub>B</sub> HS5 OFF 1 <sub>B</sub> HS5 ON
HB5_LS_EN	D0	r/w	Half-bridge output 5 Low side switch enable

			0 <sub>B</sub> LS5 OFF 1 <sub>B</sub> LS5 ON
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## OP\_CTRL\_3

Half-bridge output control 3 (Address =0x0A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D0	r/w	Reserved. Always reads as '0'

## PWM\_CTRL\_1

Half-bridge PWM Control 1 (Address =0x0B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D6	r/w	Reserved. Always reads as '0'
HB6_PWM	D5	r/w	0 <sub>B</sub> Half-bridge 6 is operating in continuous mode 1 <sub>B</sub> Half-bridge 6 is operating in PWM mode
HB5_PWM	D4	r/w	0 <sub>B</sub> Half-bridge 5 is operating in continuous mode 1 <sub>B</sub> Half-bridge 5 is operating in PWM mode
HB4_PWM	D3	r/w	0 <sub>B</sub> Half-bridge 4 is operating in continuous mode 1 <sub>B</sub> Half-bridge 4 is operating in PWM mode
HB3_PWM	D2	r/w	0 <sub>B</sub> Half-bridge 3 is operating in continuous mode 1 <sub>B</sub> Half-bridge 3 is operating in PWM mode
HB2_PWM	D1	r/w	0 <sub>B</sub> Half-bridge 2 is operating in continuous mode 1 <sub>B</sub> Half-bridge 2 is operating in PWM mode
HB1_PWM	D0	r/w	0 <sub>B</sub> Half-bridge 1 is operating in continuous mode 1 <sub>B</sub> Half-bridge 1 is operating in PWM mode

## PWM\_CTRL\_2

Half-bridge PWM Control 2 (Address =0x0C) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		PWM_CH6_DIS	PWM_CH5_DIS	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D6	r/w	Reserved. Always reads as '0'
PWM_CH6_DIS	D5	r/w	0 <sub>B</sub> PWM Generator-6 is enabled 1 <sub>B</sub> PWM Generator-6 is disabled
PWM_CH5_DIS	D4	r/w	0 <sub>B</sub> PWM Generator-5 is enabled 1 <sub>B</sub> PWM Generator-5 is disabled
PWM_CH4_DIS	D3	r/w	0 <sub>B</sub> PWM Generator-4 is enabled 1 <sub>B</sub> PWM Generator-4 is disabled
PWM_CH3_DIS	D2	r/w	0 <sub>B</sub> PWM Generator-3 is enabled 1 <sub>B</sub> PWM Generator-3 is disabled
PWM_CH2_DIS	D1	r/w	0 <sub>B</sub> PWM Generator-2 is enabled 1 <sub>B</sub> PWM Generator-2 is disabled
PWM_CH1_DIS	D0	r/w	0 <sub>B</sub> PWM Generator-1 is enabled 1 <sub>B</sub> PWM Generator-1 is disabled

## FW\_CTRL\_1

Free-wheeling Configuration 1 (Address =0x0D) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		FW_HB6	FW_HB5	FW_HB4	FW_HB3	FW_HB2	FW_HB1
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D6	r/w	Reserved. Always reads as '0'
FW_HB6	D5	r/w	HB6 free-wheeling configuration 0 <sub>B</sub> Passive free-wheeling 1 <sub>B</sub> Active free-wheeling
FW_HB5	D4	r/w	HB5 free-wheeling configuration 0 <sub>B</sub> Passive free-wheeling 1 <sub>B</sub> Active free-wheeling
FW_HB4	D3	r/w	HB4 free-wheeling configuration 0 <sub>B</sub> Passive free-wheeling 1 <sub>B</sub> Active free-wheeling
FW_HB3	D2	r/w	HB3 free-wheeling configuration 0 <sub>B</sub> Passive free-wheeling 1 <sub>B</sub> Active free-wheeling
FW_HB2	D1	r/w	HB2 free-wheeling configuration 0 <sub>B</sub> Passive free-wheeling 1 <sub>B</sub> Active free-wheeling
FW_HB1	D0	r/w	HB1 free-wheeling configuration 0 <sub>B</sub> Passive free-wheeling 1 <sub>B</sub> Active free-wheeling

## FW\_CTRL\_2

Free-wheeling Configuration 2 (Address =0x0E) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D0	r/w	Reserved. Always reads as '0'

## PWM\_MAP\_CTRL\_1

Half-bridge Output PWM Map Control 1 (Address =0x0F) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB2_PWM_MAP			HB1_PWM_MAP		
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D6	r/w	Reserved. Always reads as '0'
HB2_PWM_MAP	D5:D3	r/w	Half-bridge output 2 mode select 000 <sub>B</sub> PWM control with PWM Channel 1 001 <sub>B</sub> PWM control with PWM Channel 2 010 <sub>B</sub> PWM control with PWM Channel 3 011 <sub>B</sub> PWM control with PWM Channel 4 100 <sub>B</sub> PWM control with PWM Channel 5 101 <sub>B</sub> PWM control with PWM Channel 6 110 <sub>B</sub> PWM control with PWM Channel 7

			111 <sub>B</sub> PWM control with PWM Channel 8
HB1_PWM_MAP	D2:D0	r/w	Half-bridge output 1 mode select 000 <sub>B</sub> PWM control with PWM Channel 1 001 <sub>B</sub> PWM control with PWM Channel 2 010 <sub>B</sub> PWM control with PWM Channel 3 011 <sub>B</sub> PWM control with PWM Channel 4 100 <sub>B</sub> PWM control with PWM Channel 5 101 <sub>B</sub> PWM control with PWM Channel 6 110 <sub>B</sub> PWM control with PWM Channel 7 111 <sub>B</sub> PWM control with PWM Channel 8

## PWM\_MAP\_CTRL\_2

Half-bridge Output PWM Map Control 2 (Address =0x10) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB4_PWM_MAP			HB3_PWM_MAP		
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D6	r/w	Reserved. Always reads as '0'
HB4_PWM_MAP	D5:D3	r/w	Half-bridge output 4 mode select 000 <sub>B</sub> PWM control with PWM Channel 1 001 <sub>B</sub> PWM control with PWM Channel 2 010 <sub>B</sub> PWM control with PWM Channel 3 011 <sub>B</sub> PWM control with PWM Channel 4 100 <sub>B</sub> PWM control with PWM Channel 5 101 <sub>B</sub> PWM control with PWM Channel 6 110 <sub>B</sub> PWM control with PWM Channel 7 111 <sub>B</sub> PWM control with PWM Channel 8
HB3_PWM_MAP	D2:D0	r/w	Half-bridge output 3 mode select 000 <sub>B</sub> PWM control with PWM Channel 1 001 <sub>B</sub> PWM control with PWM Channel 2 010 <sub>B</sub> PWM control with PWM Channel 3 011 <sub>B</sub> PWM control with PWM Channel 4 100 <sub>B</sub> PWM control with PWM Channel 5 101 <sub>B</sub> PWM control with PWM Channel 6 110 <sub>B</sub> PWM control with PWM Channel 7 111 <sub>B</sub> PWM control with PWM Channel 8

## PWM\_MAP\_CTRL\_3

Half-bridge Output PWM Map Control 3 (Address =0x11) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB6_PWM_MAP			HB5_PWM_MAP		
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D6	r/w	Reserved. Always reads as '0'
HB6_PWM_MAP	D5:D3	r/w	Half-bridge output 6 mode select 000 <sub>B</sub> PWM control with PWM Channel 1 001 <sub>B</sub> PWM control with PWM Channel 2 010 <sub>B</sub> PWM control with PWM Channel 3 011 <sub>B</sub> PWM control with PWM Channel 4 100 <sub>B</sub> PWM control with PWM Channel 5 101 <sub>B</sub> PWM control with PWM Channel 6 110 <sub>B</sub> PWM control with PWM Channel 7

HB5_PWM_MAP	D2:D0	r/w	111 <sub>B</sub> PWM control with PWM Channel 8 Half-bridge output 5 mode select 000 <sub>B</sub> PWM control with PWM Channel 1 001 <sub>B</sub> PWM control with PWM Channel 2 010 <sub>B</sub> PWM control with PWM Channel 3 011 <sub>B</sub> PWM control with PWM Channel 4 100 <sub>B</sub> PWM control with PWM Channel 5 101 <sub>B</sub> PWM control with PWM Channel 6 110 <sub>B</sub> PWM control with PWM Channel 7 111 <sub>B</sub> PWM control with PWM Channel 8
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## PWM\_MAP\_CTRL\_4

Half-bridge Output PWM Map Control 4 (Address =0x12) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D0	r/w	Reserved. Always reads as '0'

## PWM\_FREQ\_CTRL\_1

PWM Channel Frequency Select 1 (Address =0x13) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH4_FREQ	PWM_CH3_FREQ	PWM_CH2_FREQ	PWM_CH1_FREQ				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_CH4_FREQ	D7:D6	r/w	PWM Channel 4 frequency select 00 <sub>B</sub> PWM frequency: 80Hz 01 <sub>B</sub> PWM frequency: 100Hz 10 <sub>B</sub> PWM frequency: 200Hz 11 <sub>B</sub> PWM frequency: 2000Hz
PWM_CH3_FREQ	D5:D4	r/w	PWM Channel 3 frequency select 00 <sub>B</sub> PWM frequency: 80Hz 01 <sub>B</sub> PWM frequency: 100Hz 10 <sub>B</sub> PWM frequency: 200Hz 11 <sub>B</sub> PWM frequency: 2000Hz
PWM_CH2_FREQ	D3:D2	r/w	PWM Channel 2 frequency select 00 <sub>B</sub> PWM frequency: 80Hz 01 <sub>B</sub> PWM frequency: 100Hz 10 <sub>B</sub> PWM frequency: 200Hz 11 <sub>B</sub> PWM frequency: 2000Hz
PWM_CH1_FREQ	D1:D0	r/w	PWM Channel 1 frequency select 00 <sub>B</sub> PWM frequency: 80Hz 01 <sub>B</sub> PWM frequency: 100Hz 10 <sub>B</sub> PWM frequency: 200Hz 11 <sub>B</sub> PWM frequency: 2000Hz

## PWM\_FREQ\_CTRL\_2

PWM Channel Frequency Select 2 (Address =0x14) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH8_FREQ	PWM_CH7_FREQ	PWM_CH6_FREQ	PWM_CH5_FREQ				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_CH8_FREQ	D7:D6	r/w	PWM Channel 8 frequency select 00 <sub>B</sub> PWM frequency: 80Hz 01 <sub>B</sub> PWM frequency: 100Hz 10 <sub>B</sub> PWM frequency: 200Hz 11 <sub>B</sub> PWM frequency: 2000Hz
PWM_CH7_FREQ	D5:D4	r/w	PWM Channel 7 frequency select 00 <sub>B</sub> PWM frequency: 80Hz 01 <sub>B</sub> PWM frequency: 100Hz 10 <sub>B</sub> PWM frequency: 200Hz 11 <sub>B</sub> PWM frequency: 2000Hz
PWM_CH6_FREQ	D3:D2	r/w	PWM Channel 6 frequency select 00 <sub>B</sub> PWM frequency: 80Hz 01 <sub>B</sub> PWM frequency: 100Hz 10 <sub>B</sub> PWM frequency: 200Hz 11 <sub>B</sub> PWM frequency: 2000Hz
PWM_CH5_FREQ	D1:D0	r/w	PWM Channel 5 frequency select 00 <sub>B</sub> PWM frequency: 80Hz 01 <sub>B</sub> PWM frequency: 100Hz 10 <sub>B</sub> PWM frequency: 200Hz 11 <sub>B</sub> PWM frequency: 2000Hz

## PWM\_DUTY\_CTRL\_1

PWM Channel 1 Duty Cycle Configuration (Address =0x15) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH1							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH1	D7:D0	r/w	PWM Channel 1 Duty Cycle configuration 0000 0000 <sub>B</sub> 100% OFF xxxx xxxx <sub>B</sub> parts of 255 ON 1111 1111 <sub>B</sub> 100% ON

## PWM\_DUTY\_CTRL\_2

PWM Channel 2 Duty Cycle Configuration (Address =0x16) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH2							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH2	D7:D0	r/w	PWM Channel 2 Duty Cycle configuration 0000 0000 <sub>B</sub> 100% OFF xxxx xxxx <sub>B</sub> parts of 255 ON 1111 1111 <sub>B</sub> 100% ON

## PWM\_DUTY\_CTRL\_3

PWM Channel 3 Duty Cycle Configuration (Address =0x17) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH3							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH3	D7:D0	r/w	PWM Channel 3 Duty Cycle configuration 0000 0000 <sub>B</sub> 100% OFF xxxx xxxx <sub>B</sub> parts of 255 ON 1111 1111 <sub>B</sub> 100% ON

## PWM\_DUTY\_CTRL\_4

PWM Channel 4 Duty Cycle Configuration (Address =0x18) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH4							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH4	D7:D0	r/w	PWM Channel 4 Duty Cycle configuration 0000 0000 <sub>B</sub> 100% OFF xxxx xxxx <sub>B</sub> parts of 255 ON 1111 1111 <sub>B</sub> 100% ON

## PWM\_DUTY\_CTRL\_5

PWM Channel 5 Duty Cycle Configuration (Address =0x19) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH5							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH5	D7:D0	r/w	PWM Channel 5 Duty Cycle configuration 0000 0000 <sub>B</sub> 100% OFF xxxx xxxx <sub>B</sub> parts of 255 ON 1111 1111 <sub>B</sub> 100% ON

## PWM\_DUTY\_CTRL\_6

PWM Channel 6 Duty Cycle Configuration (Address =0x1A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH6							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH6	D7:D0	r/w	PWM Channel 6 Duty Cycle configuration 0000 0000 <sub>B</sub> 100% OFF xxxx xxxx <sub>B</sub> parts of 255 ON 1111 1111 <sub>B</sub> 100% ON

## PWM\_DUTY\_CTRL\_7

PWM Channel 7 Duty Cycle Configuration (Address =0x1B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH7							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH7	D7:D0	r/w	PWM Channel 7 Duty Cycle configuration 0000 0000 <sub>B</sub> 100% OFF xxxx xxxx <sub>B</sub> parts of 255 ON 1111 1111 <sub>B</sub> 100% ON



## PWM\_DUTY\_CTRL\_8

PWM Channel 8 Duty Cycle Configuration (Address =0x1C) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH8							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH8	D7:D0	r/w	PWM Channel 8 Duty Cycle configuration 0000 0000 <sub>B</sub> 100% OFF xxxx xxxx <sub>B</sub> parts of 255 ON 1111 1111 <sub>B</sub> 100% ON

## SR\_CTRL\_1

The Slew Rate Configuration 1 (Address =0x1D) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D6	r/w	Reserved. Always reads as '0'
HB6_SR	D5	r/w	HB6 slew rate configuration 0 <sub>B</sub> 1V/μs 1 <sub>B</sub> 3.7V/μs
HB5_SR	D4	r/w	HB5 slew rate configuration 0 <sub>B</sub> 1V/μs 1 <sub>B</sub> 3.7V/μs
HB4_SR	D3	r/w	HB4 slew rate configuration 0 <sub>B</sub> 1V/μs 1 <sub>B</sub> 3.7V/μs
HB3_SR	D2	r/w	HB3 slew rate configuration 0 <sub>B</sub> 1V/μs 1 <sub>B</sub> 3.7V/μs
HB2_SR	D1	r/w	HB2 slew rate configuration 0 <sub>B</sub> 1V/μs 1 <sub>B</sub> 3.7V/μs
HB1_SR	D0	r/w	HB1 slew rate configuration 0 <sub>B</sub> 1V/μs 1 <sub>B</sub> 3.7V/μs

## SR\_CTRL\_2

The slew rate configuration 2 (Address =0x1E) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D0	r/w	Reserved. Always reads as '0'

## OLD\_CTRL\_1

The Open Load Detect Control 1 (Address =0x1F) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D6	r/w	Reserved. Always reads as '0'
HB6_OLD_DIS	D5	r/w	HB6 open load detect configuration 0 <sub>B</sub> Open-load detection on half-bridge 6 is enable 1 <sub>B</sub> Open-load detection on half-bridge 6 is disable
HB5_OLD_DIS	D4	r/w	HB5 open load detect configuration 0 <sub>B</sub> Open-load detection on half-bridge 5 is enable 1 <sub>B</sub> Open-load detection on half-bridge 5 is disable
HB4_OLD_DIS	D3	r/w	HB4 open load detect configuration 0 <sub>B</sub> Open-load detection on half-bridge 4 is enable 1 <sub>B</sub> Open-load detection on half-bridge 4 is disable
HB3_OLD_DIS	D2	r/w	HB3 open load detect configuration 0 <sub>B</sub> Open-load detection on half-bridge 3 is enable 1 <sub>B</sub> Open-load detection on half-bridge 3 is disable
HB2_OLD_DIS	D1	r/w	HB2 open load detect configuration 0 <sub>B</sub> Open-load detection on half-bridge 2 is enable 1 <sub>B</sub> Open-load detection on half-bridge 2 is disable
HB1_OLD_DIS	D0	r/w	HB1 open load detect configuration 0 <sub>B</sub> Open-load detection on half-bridge 1 is enable 1 <sub>B</sub> Open-load detection on half-bridge 1 is disable

## OLD\_CTRL\_2

The Open Load Detect Control 2 (Address =0x20) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OLD_REP	OLD_OP	Reserved					
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
OLD_REP	D7	r/w	0 <sub>B</sub> Report on nFAULT pin during OLD condition 1 <sub>B</sub> No report on nFAULT pin during OLD condition
OLD_OP	D6	r/w	0 <sub>B</sub> Half-bridge are not active after OLD condition detect 1 <sub>B</sub> Half-bridge are active after OLD condition detect
Reserved	D5:D0	r/w	Reserved. Always reads as '0'

## OLD\_CTRL\_3

The Open Load Detect Control 3 (Address =0x21) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OCP_DEG			Reserved				
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
OCP_DEG	D7:D5	r/w	000B OCP deglitch time is 10μs 001B OCP deglitch time is 5μs 010B OCP deglitch time is 2.5μs 011B OCP deglitch time is 1μs 100B OCP deglitch time is 60μs 101B OCP deglitch time is 40μs

			110B OCP deglitch time is 30μs 111B OCP deglitch time is 20μs
Reserved	D4:D0	r/w	Reserved. Always reads as '0'

## OLD\_CTRL\_4

The open load detect control 4 (Address =0x22) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	HB6_OLD_EN	HB5_OLD_EN	HB4_OLD_EN	HB3_OLD_EN	HB2_OLD_EN	HB1_OLD_EN	
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7:D6	r/w	Reserved. Always reads as '0'
HB6_OLD_EN	D5	r/w	HB6 low-current OLD detect configuration 0 <sub>B</sub> Low-current OLD detection on half-bridge 6 is disable 1 <sub>B</sub> Low-current OLD detection on half-bridge 6 is enable
HB5_OLD_EN	D4	r/w	HB5 low-current OLD detect configuration 0 <sub>B</sub> Low-current OLD detection on half-bridge 5 is disable 1 <sub>B</sub> Low-current OLD detection on half-bridge 5 is enable
HB4_OLD_EN	D3	r/w	HB4 low-current OLD detect configuration 0 <sub>B</sub> Low-current OLD detection on half-bridge 4 is disable 1 <sub>B</sub> Low-current OLD detection on half-bridge 4 is enable
HB3_OLD_EN	D2	r/w	HB3 low-current OLD detect configuration 0 <sub>B</sub> Low-current OLD detection on half-bridge 3 is disable 1 <sub>B</sub> Low-current OLD detection on half-bridge 3 is enable
HB2_OLD_EN	D1	r/w	HB2 low-current OLD detect configuration 0 <sub>B</sub> Low-current OLD detection on half-bridge 2 is disable 1 <sub>B</sub> Low-current OLD detection on half-bridge 2 is enable
HB1_OLD_EN	D0	r/w	HB1 low-current OLD detect configuration 0 <sub>B</sub> Low-current OLD detection on half-bridge 1 is disable 1 <sub>B</sub> Low-current OLD detection on half-bridge 1 is enable

## Application Example

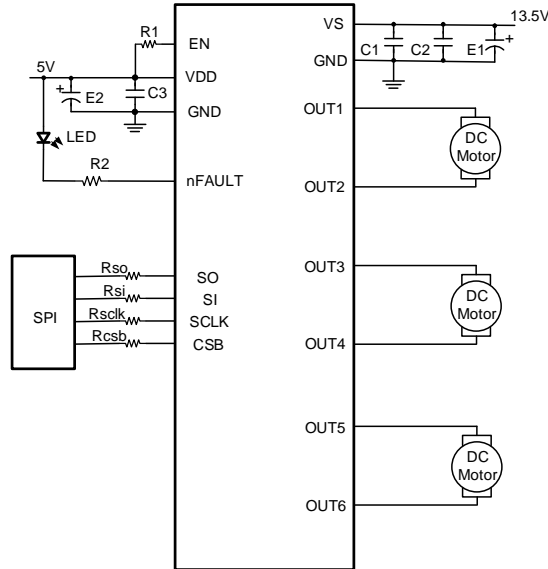


Figure 23. Typical Application of SA52106

## BOM List

Reference Designator	Description	Package Info
U1	SA52106	TSSOP24E
Rso, Rsc, Rsi, Rcsb, R1	100Ω	0603
E1	100uF/Ecap/50V	
E2	100uF/Ecap/25V	
C1, C2	1uF/50V	0603
C3	1uF/16V	0603
R2	10kΩ	0603
LED	Red LED	SMA

## PCB Layout Guide

The VS supplies power switches through a large current. Decoupling the VS pin to the GND pin with low ESR ceramic caps is recommended. These capacitors should be placed as close to the VS as possible with a thick trace or ground plane connection to the device's GND pin.

The thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should connect to a large bottom-layer ground plane. Large copper areas are recommended to improve thermal dissipation.

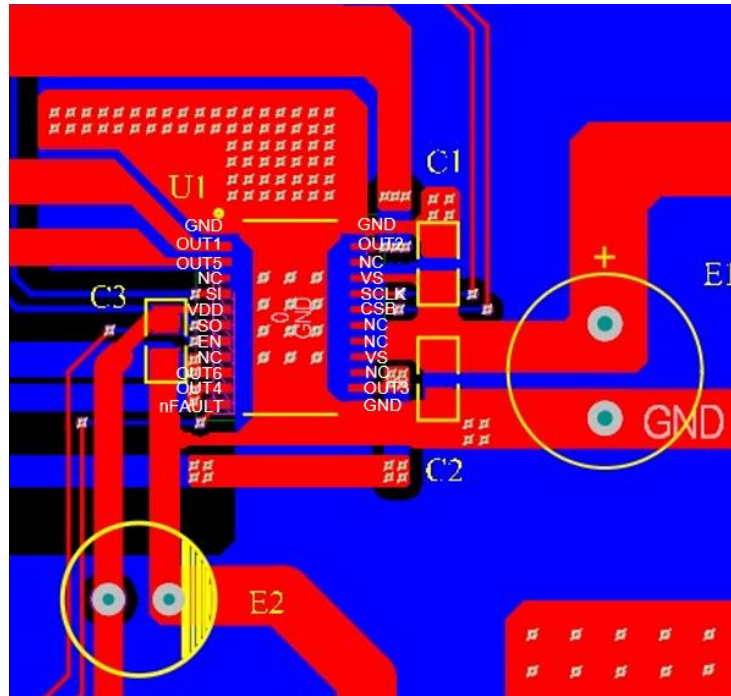
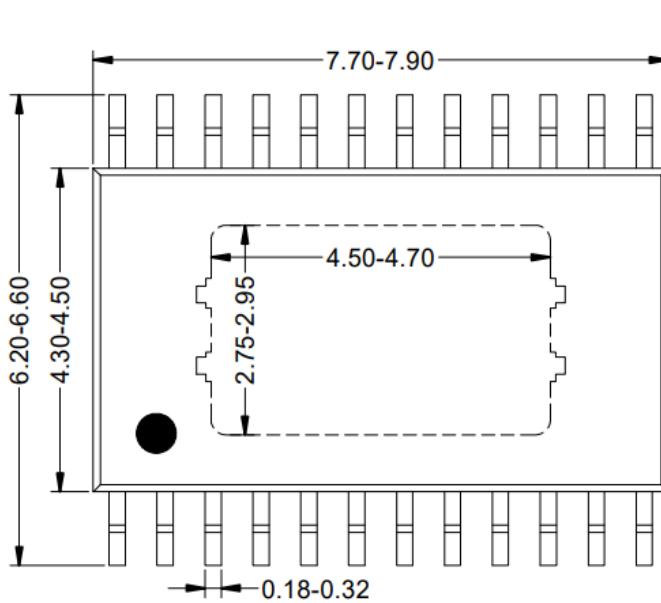
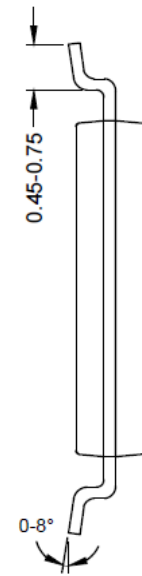


Figure 24. PCB Layout Details

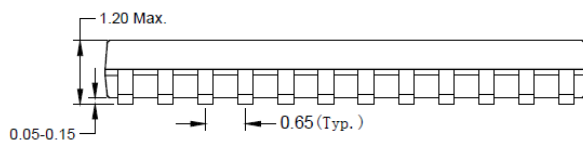
## TSSOP24E Package Outline Drawing



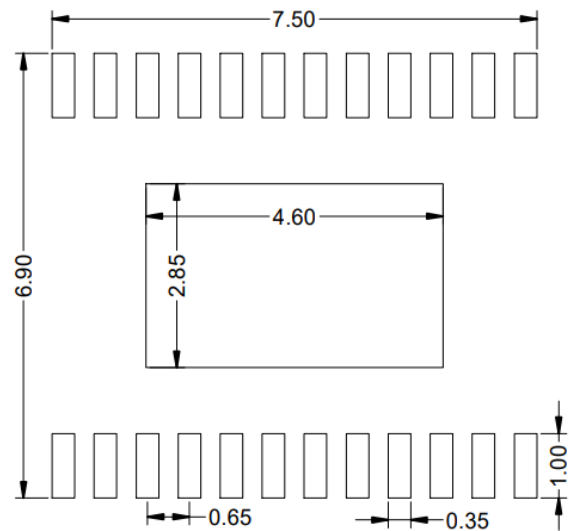
**Top View**



**Side View**



**Front View**

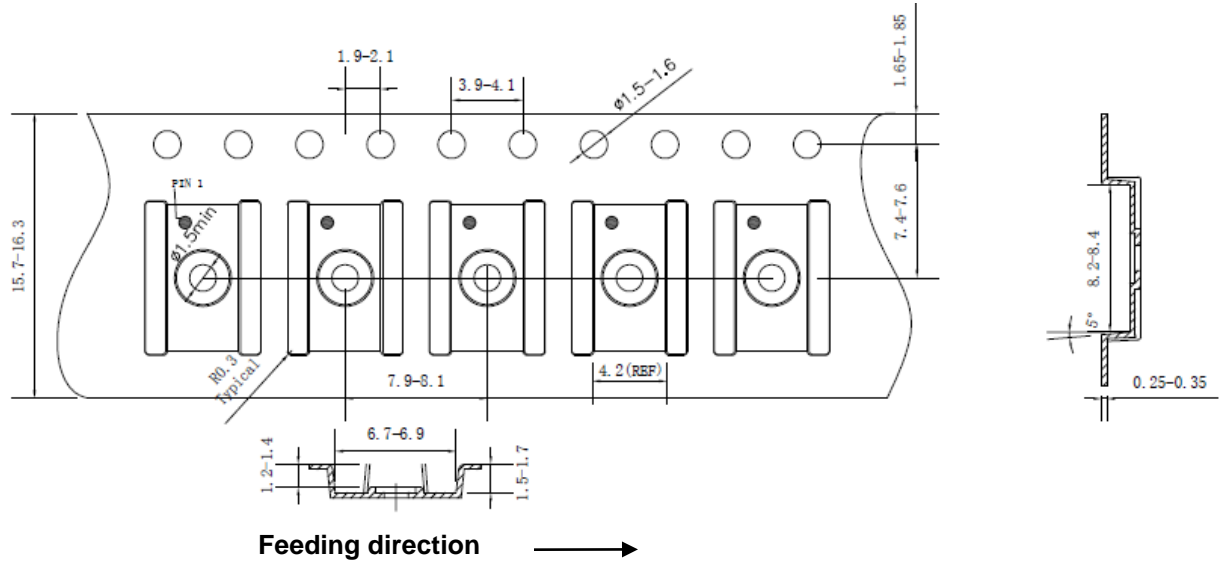


**Recommended PCB Layout  
(Reference only)**

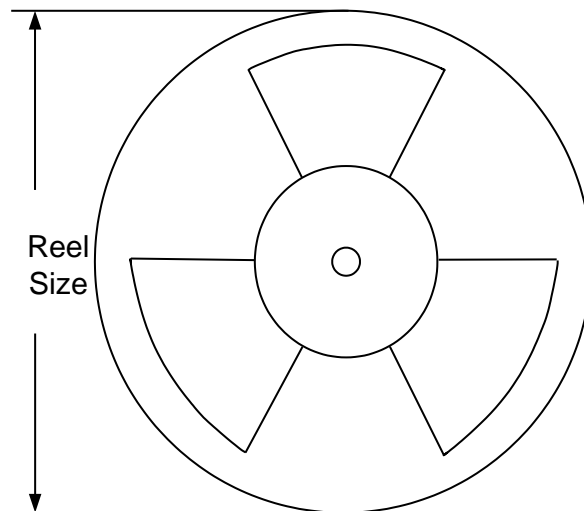
**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

## Taping & Reel Specification

## 1. Taping Orientation



## 2. Carrier Tape & Reel Specification for packages



Package Types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSSOP24E	16	8	13"	400	400	3000

### 3. Others: NA



## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description
1.0	Jan 05, 2024	Initial Release



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