

DATA SHEET

SA5753

Audio processor — filter and control
section

Product specification
Replaces data of 1995 July 7
IC17 Data Handbook

1997 Nov 07

Audio processor – filter and control section

SA5753

DESCRIPTION

The SA5753 is a high performance low power CMOS audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The SA5753 subsystem includes complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, digitally controlled attenuators for signal level and volume control, audio path mute switches, a programmable DTMF generator, power-down circuitry for low current standby, power-on reset capability, and an I²C interface. When the SA5753 is used with an SA5752 (companding function), the complete audio processing system of an AMPS, TACS, NAMPS or NTACS cellular telephone is easily implemented.

The system also meets the requirements of the proposed NAMPS or NTACS specification, and can be used in cordless telephone applications.

The SA5753 can be operated without the I²C bus interface by pulling DFT (Pin 13) HIGH.

BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5752

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

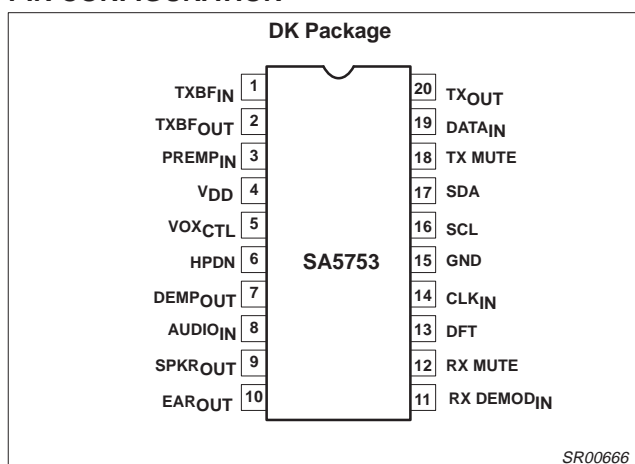


Figure 1. Pin Configuration

FEATURES

- Low 3V supply
- Miniature SSOP package
- Low power
- High performance
- Built-in programmable DTMF generator
- Built-in digitally controlled attenuators for modulation and volume control
- Built-in peak-deviation limiter
- I²C Bus controlled
- Power-on reset
- Power down capability
- Programmable mute control
- Meets AMPS/TACS/NAMPS/NTACS requirements

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA5753DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{DD}	Power supply voltage range	-0.3 to 6	V
V _{IN}	Voltage applied to any other pin	-0.3 to V _{DD} +0.3	V
	Storage temperature	-65 to +150	°C
T _A	Ambient operating temperature	-40 to +85	°C

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PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	TXBF _{IN}	Transmit bandpass filter input
2	TXBF _{OUT}	Transmit bandpass filter output
3	PREMP _{IN}	Pre-emphasis input
4	V _{DD}	Positive supply
5	VOX _{CTL}	Vox control output
6	HPDN	Power-down I/O
7	DEMP _{OUT}	De-emphasis output
8	AUDIO _{IN}	Audio input
9	SPKR _{OUT}	Audio output to speaker
10	EAR _{OUT}	Audio output to earpiece
11	RX DEMOD _{IN}	Rx demodulated audio signal input
12	RX MUTE	RX audio signal mute input
13	DFT	Default input, non-I ² C or stand-alone operation
14	CLK _{IN}	Clock input (1.2MHz)
15	GND	Ground
16	SCL	I ² C serial clock line
17	SDA	I ² C serial data line
18	TX MUTE	Tx audio signal mute input
19	DATA _{IN}	Data input
20	TX _{OUT}	Transmit output

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DC ELECTRICAL CHARACTERISTICST_A = 25°C, V_{DD} = +3.3V, unless otherwise specified. See test circuit, Figure 2.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V _{DD}	Power supply voltage		3.0	3.3	5.5	V
I _{DD}	Supply current	Operating IDLE Power Down (PVDN)		1.7 600 200		mA μA μA
I _{IH}	Input current high TX MUTE, RX MUTE, HPDN DFT	V _{IN} = V _{DD}	-10 0	0 +10	+10 +30	μA μA
I _{IL}	Input current low TX MUTE, RX MUTE, HPDN, DFT	V _{IN} = GND	-30 -10	-10 0	0 +10	μA μA
V _{IH}	Input voltage high		0.7V _{DD}		V _{DD}	V
V _{IL}	Input voltage low		0		0.3V _{DD}	V

AC ELECTRICAL CHARACTERISTICST_A = 25°C, V_{DD} = +3.3V. See test circuit, Figure 2. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = -20dBm, unless otherwise specified. All gain control blocks (Attenuators) = 0dB gain, NAMPS and VCO bits set to 0.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f = 1kHz		100		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-1.0	0	1.0	dB
	RX BPF gain with de-emphasis	f = 100Hz		-30		dBm0
	RX BPF gain with de-emphasis	f = 300Hz	8.5	9.6	11.5	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.5	-10.0	-8.5	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-58		dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz		200		μV _{RMS}
	RX dynamic range	with deemphasis		80		dB
	DEMP _{OUT} output impedance	f = 1kHz			40	Ω
	DEMP _{OUT} output swing (1%)	2kΩ to V _{DD} /2; f = 1kHz		2.4		V _{P-P}
	SPKR _{OUT} output swing (1%)	50kΩ to V _{DD} /2; f = 1kHz	V _{DD} -1	2.4		V _{P-P}
	EAR _{OUT} output swing (1%)	50kΩ to V _{DD} /2; f = 1kHz	V _{DD} -1	2.4		V _{P-P}
	SPKR _{OUT} noise / EAR _{OUT} noise			200		μV _{RMS}
	CLK _{IN} high		2.1		3.0	V
	CLK _{IN} low		0		1.0	V
	TX BPF anti alias rejection	f > 50kHz		40		dB
	TX BPF input impedance	f = 3kHz		100		KΩ
	TX BPF noise	300 - 3000kHz		200		μV _{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dBm0
	TX LPF gain with pre-emphasis	f = 1kHz, 0dBV		2.43		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-28		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-48		dBm0
	TX overall gain	1kHz		2.43		dB
	TX overall gain	100Hz		-58	-44	dBm0
	TX overall gain	300Hz	-11.5	-10.4	-8.5	dBm0

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AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF dynamic range			TBD		dB
	PREMP _{IN} input impedance	f = 3kHz		100		kΩ
	TX _{OUT} Slew rate	C _L = 15pF		0.75		V/μs
	Output impedance	f = 3kHz			40	Ω
	Output swing (limiting)			1.2		V _{P-P}
	Output swing (1% THD)	5kΩ load (25°C)		1.0		V _{P-P}
	Tx DTMF signal with TXLPF and pre-emphasis			0.45		V/kHz
	Rx DTMF sidetone		-0.8		5.2	dBm0
	Time delay to mute from RX MUTE or TX MUTE transition	V _{IN} = V _{IL} to V _{IH} V _{IN} = V _{IH} to V _{IL}		0.5		μs
				0.5		μs

Table 1. Gain Control Blocks (Bit 0 is Least Significant Bit)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB)	
			MIN	MAX
A1	4	-0.8	-12.0	0
A2a	5	±0.25	-3.75	+3.75
A2b	2	-6, (-12 on first)	-24.0	0
A3	4	-1.0	-17.0	-2.0
A4	4	±0.5	-3.5	+3.5
A6	4	-2.0	-30.0	0
A7	4	±0.5	-3.5	+3.5
NAMPS	1		+1.9 in A2b -7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

FUNCTIONAL DESCRIPTION

The SA5753 is an audio signal processor designed to meet the requirements of compact low voltage radio telephone equipment. It includes transmit and receive bandpass filters for voiceband (300-3000Hz) with pre-emphasis and de-emphasis respectively, a transmit peak deviation limiter, voice channel mute switches and a data path which can be summed into the transmit channel. An I²C interface is provided for software programmability of a DTMF generator, mute polarity, selection of different power down and operating modes and control of the gain in both the transmit and receive channels.

Software programmable gain control allows the device to be automatically optimized during equipment production and offers flexibility during normal operation.

Gain Blocks

The programmable gain blocks are shown in Table 1 and Figure 2. The purpose for each block is as follows:

- A1 compensates for microphone gain variations in the transmit path.
- A2a compensates for transmitter dynamic range variations due to manufacturing tolerances of the SA5753 and SA5752 compandor companion device. To meet AMPS requirements, the dynamic range between the zero crossing signal level of the compandor and the peak signal allowed by the deviation limiter is adjusted to 12.34dB.
- A2b allows coarse attenuation to be inserted in the transmit path to eliminate positive feedback effects in hands-free speaker applications. First step is 12dB followed by two steps of 6dB.
- A3 sets the gain between the DATA_{IN} pin (Pin 19) and the TX_{OUT} pin (Pin 20) and should be adjusted after A2a and A4 have been previously optimized. The SA5753 will interface directly with the UMA1000T data processor (which produces a 2Vpk data signal). For NAMPS applications an additional 10 to 14dB resistive divider must be added at the DATA_{IN} pin (Pin 19) for a 2V data signal.

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- e. A4 compensates for transmit gain variations due to manufacturing tolerances of the SA5753, SA5752 and VCO connected to TX_{OUT} (Pin 20). After A2a has been adjusted to set dynamic range then A4 is used to set the peak output voltage at TX_{OUT} (Pin 20) such that a nominal 10kHz/V VCO produces a peak deviation of 12kHz to meet AMPS specifications.
- f. A6 is the volume control for both the SPKR_{OUT} and EAR_{OUT}.
- g. A7 compensates for manufacturing tolerances in the SA5753 and preceding demodulator. For AMPS requirements, a 1kHz tone with 2.9kHz deviation should produce an output signal at DEMP_{OUT} (Pin 7) corresponding to the zero crossing signal level of the expander.

NAMPS and VCO Offsets

For NAMPS applications, a '1' programmed into R5B3 (register 5, bit 3) will offset the transmit gain for NAMPS applications. It is recommended that A2a and A4 be programmed after the NAMPS option is set to compensate for manufacturing tolerances in the NAMPS offset, itself.

When the VCO bit of R5B2 is a '1', an extra gain of 6dB is provided at TX_{OUT} for direct interface to VCOs with a nominal gain of 5kHz/V.

Operation Using the I²C Communications Bus

The SA5753 includes on-chip gain blocks and options which can be programmed through an I²C interface bus. To use this capability, the DFT pin (Pin 13) must be pulled LOW. In this mode, all signal level adjustments can be made through software with no external potentiometers required.

With DFT pulled LOW, the HPDN pin (Pin 6) is an OUTPUT having the same value as the program bit in register 5 bit 1 (R5B1) of the control register bit map. The value at the VOX_{CTL} output (Pin 5) is the same as the program bit in R8B7. The HPDN and VOX_{CTL} outputs can be used to control the state of the SA5752 companion device.

Power On Reset and Power Down Modes

In order to avoid undefined states of the SA5753 when power is initially applied, a power-on-reset circuit is incorporated which defaults RxP and TxP such that the receive and transmit paths are muted if a 'high' voltage is applied to RX MUTE and TX MUTE (Pins 12 and 18). RX MUTE and TX MUTE include on-chip pull up resistors so, during power up, the user may apply a logic '1' to these pins or leave them floating. After power up, the registers can be programmed and the mutes removed by a quick access write to R0.

Three software controlled low power modes are provided on the SA5753. These are POWER DOWN (PWDN), IDLE and DENA and can be selected by programming a '1' into R6B2, R6B1 or R6B0 as follows. In PWDN mode (R6B2=1) both the voice and data channels are powered down with the respective I/O pins at a high impedance. In DENA mode (R6B1=1) the voice channels are powered down, but the data channel (from DATA_{IN} and TX_{OUT}) is fully active. In IDLE mode (R6B1=1, R6B0=1) both voice and data channels are powered down. (See Table on page 8.)

The difference between selecting IDLE and PWDN is that the former maintains the normal operational bias voltages at all voice and data I/O pins and provides a glitch-free transfer from power down to a fully active mode and vice-versa.

Although the POWER DOWN mode exhibits lower power consumption, glitches may occur when transferring to an active mode because of the previous high impedance of the I/O pins.

The VOX_{CTL} and HPDN pins (Pins 5 and 6) still have the same value as R8B7 and R5B1 in all low power modes.

Operation Without Using the I²C Bus

The SA5753 can be operated in a default mode with the I²C bus bypassed. To use this mode, the DFT pin (Pin 13) is pulled HIGH, then the I²C bus is bypassed and the SA5753 operates as if all register bits in the I²C address map table are set to '0' except R1B2 (S13), R0B0 (S10) and R0B1 (S9), which are set to '1' to enable the receiver output. R6B2 (PWDN), which is controlled by the state of the HPDN pin (Pin 6), which is an input in DEFAULT mode.

When HPDN is pulled HIGH, the R6B2 bit is set to '0' and the SA5753 is placed in its normal operating mode with all Gain Control Blocks set to 0dB except A3, which is set to -2dB.

When HPDN is pulled LOW, the R6B2 bit is set to '1' and the SA5753 enters POWER DOWN.

There is no on-chip pull-up or pull-down structure on the HPDN pin and so it must not be allowed to float in DEFAULT mode since the operating mode of the SA5753 will then be undetermined.

The Tx MUTE and Rx MUTE pins must be pulled LOW to enable the transmit and receive paths, respectively.

The VOX_{CTL} pin (Pin 5) will follow the value of the control bit stored in R8B7 prior to pulling DFT HIGH.

The DTMF is disabled in the DEFAULT mode.

Programming Without the I²C Protocol

In the default mode, with DFT (Pin 13) and HPDN (Pin 6) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I²C bus by the negative edge of a shifting clock applied at the SCL pin of the I²C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are therefore required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value.

Summary: To use this capability, the DFT pin and the HPDN pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

NOTE: Default Mode is not tested in production.

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Cordless Telephone Applications

For cordless telephone applications, a switch S12 is provided (R5B0) to route data through the complete transmit path while inhibiting the voice channel. In the receive path, a quick access mode is provided through the I²C to disable both EAR_{OUT} and SPKR_{OUT}, by setting R0B0 and R0B1, when data is detected at the DEMP_{OUT} pin (Pin 7).

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. Data transfer may be initiated only when the bus is not busy (both lines HIGH).

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kb/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

For devices operating over a wide range of supply voltages, such as the SA5753, the following levels have been defined for a logical LOW and HIGH;

$$V_{ILMAX} = 0.3V_{DD} \text{ (max. input LOW voltage)}$$

$$V_{IHMIN} = 0.7V_{DD} \text{ (min. input HIGH voltage)}$$

Data Transfer

Data is transferred from a transmitting device to a receiving device with one data bit transferred during each clock pulse on the SCL line. The transmitter also generates the clock once arbitration has given it control of the SCL line. The data on the SDA line must remain stable during the HIGH period of the clock cycle, otherwise it may be interpreted as a control signal.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

Acknowledgement

Following each byte of data transferred, the receiver must acknowledge successful reception. To do this the transmitter releases the SDA line (allowing it to go HIGH) at the end of each transmitted byte, and it is pulled LOW by the receiver. If this condition is maintained during the next HIGH period of the clock pulse (called the acknowledge clock pulse) then data transfer is resumed. If the receiver does not pull the SDA line LOW, the transmitter will abort the transfer.

I²C Bus Data Configurations

The SA5753 is always a slave receiver in the I²C bus configuration). The slave address consists of eight bits in the serial mode and is internally fixed.

Control Registers

The control register bit map is shown below. Either a quick access or normal address mode can be used, determined by the two MSB bits in the first word following the SA5753 address word. If the quick access mode is used, the registers R0 or R1 can be updated by sending only two bytes of information (address plus update). If R0 or R1 are updated using the address mode, then B7 and B6 of the data word are ignored. In all access modes, incremental register addressing is supported with following words updating the next register until a 'stop' bit is sent.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

$$\text{High Frequency} = 1200\text{kHz}/6/\text{HD}$$

where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

$$\text{Low Frequency} = 1200\text{kHz}/14/\text{LD}$$

where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading DTC = 1 in R1, bit 5.

Single tones can be obtained by loading 2 into the unused tone register to silence it.

Loading a value of 1 or 0 into the registers will default the register value to 257 or 256 for high tone or low tone, respectively.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during continuous operation (DTC=1).

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I²C Address and Access

S	A7	A6	A5	A4	A3	A2	A1	A0	ACK	F7	F6	F5	F4	F3	F2	F1	F0	ACK	...	P
---	----	----	----	----	----	----	----	----	-----	----	----	----	----	----	----	----	----	-----	-----	---

S = start, A0 = 0, ACK = acknowledge, P = stop, A7–0 = SA5753 address fixed internally at 1000000. Access mode is determined by F7, F6.

All access modes support incremental addressing.

Mode	F7	F6	Action
quick access	0	0	Load F5–F0 to R0B5 – R0B0
quick access	0	1	Load F5–F0 to R1B5 – R1B0
test mode	1	0	For test only. DO NOT USE.
address mode	1	1	F3–F0 point to register

Address Map

REG	Address				Register Bits							
	F3	F2	F1	F0	B7	B6	B5	B4	B3	B2	B1	B0
R0	0	0	0	0	Y	Y	RxM	TxM	A2bb1	A2bb0	S9	S10
R1	0	0	0	1	Y	Y	DTC	S4	S8	S13	S7	S2
R2	0	0	1	0	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0
R3	0	0	1	1	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
R4	0	1	0	0	A1b3	A1b2	A1b1	A1b0	A4b3	A4b2	A4b1	A4b0
R5	0	1	0	1	A6b3	A6b2	A6b1	A6b0	NAMPS	VCO	HPDN	S12
R6	0	1	1	0	A2ab4	A2ab3	A2ab2	A2ab1	A2ab0	PWDN	IDLE 1	IDLE 0
R7	0	1	1	1	A3b3	A3b2	A3b1	A3b0	A7b3	A7b2	A7b1	A7b0
R8	1	0	0	0	VOX _{CTL}	S3	S5	S6	S11	RxP	TxP	S1

Y = ignored in address mode.

For all bits TRUE = '1'

A1b3–0	=	program bits for gain block A1	TxP	=	transmit mute polarity
A2ab4–0	=	program bits for gain block A2a	DTC	=	DTMF continuous
A2bb1–0	=	program bits for gain block A2b	S1	=	bypass TXBPF
A3b3–0	=	program bits for gain block A3	S2	=	bypass compressor in TX path, inhibit pre-emph input
A4b4–0	=	program bits for gain block A4	S3	=	bypass pre-emp and limiter in Tx path
A5b2–0	=	program bits for gain block A5	S4	=	enable DTMF to TX path and inhibit PREMP _{IN} and S2.
A6b3–0	=	program bits for gain block A6	S5	=	bypass RXBPF
A7b3–0	=	program bits for gain block A7	S6	=	bypass de-emph in RX path
HD7–0	=	high tone DTMF	S7	=	bypass expander in RX path, inhibit audio input
LD7–0	=	low tone DTMF	S8	=	enable DTMF to RX path and inhibit AUDIO _{IN} and S7.
NAMPS	=	program bit for NAMPS offset	S9	=	enable SPKR _{OUT}
VCO	=	6dB higher TX _{OUT}	S10	=	enable EAR _{OUT}
RxM	=	receive mute	S11	=	bypass TXLPF
TxM	=	transmit mute	S12	=	cordless data option established
RxP	=	receive mute polarity	S13	=	enable data path
VOX _{CTL}	=	enable VOX of compandor/expander circuit. This bit appears at the VOX _{CTL} pin (Pin 5) of the SA5753.			
HPDN	=	enable power down of compandor circuit. This bit appears at the HPDN pin (Pin 6) of the SA5753			
PWDN, IDLE1, IDLE0	=	see Table below			

Low Power Modes (R6B0 – R6B2)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I ² C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at V _{DD} /2, DATA _{IN} to TX _{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at V _{DD} /2, DATA _{IN} to TX _{OUT} disabled.
0	0	0	Normal operation.
0	0	1	DATA _{IN} to TX _{OUT} disabled.

X = don't care.

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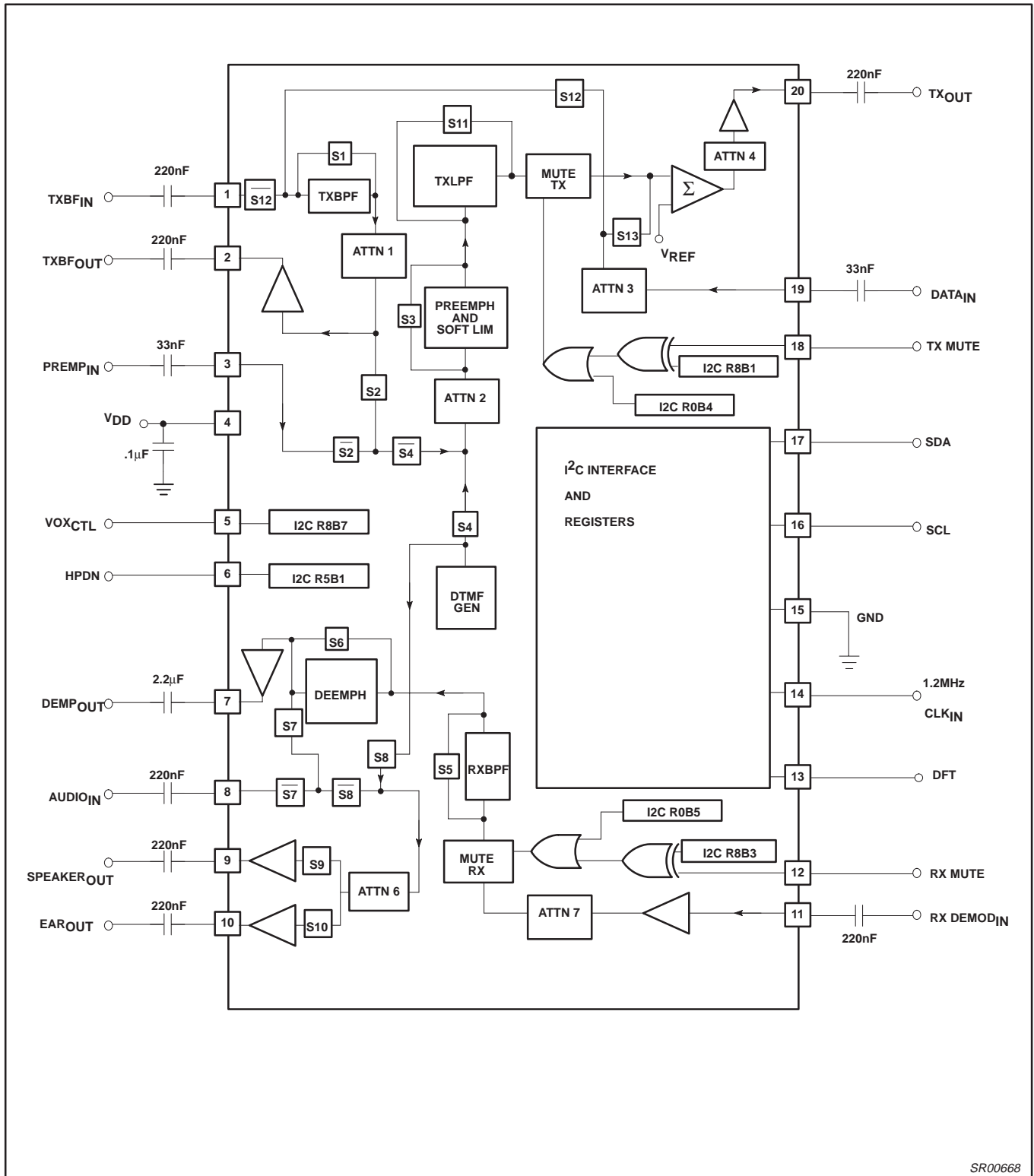


Figure 2. SA5753 Test and Application Circuit

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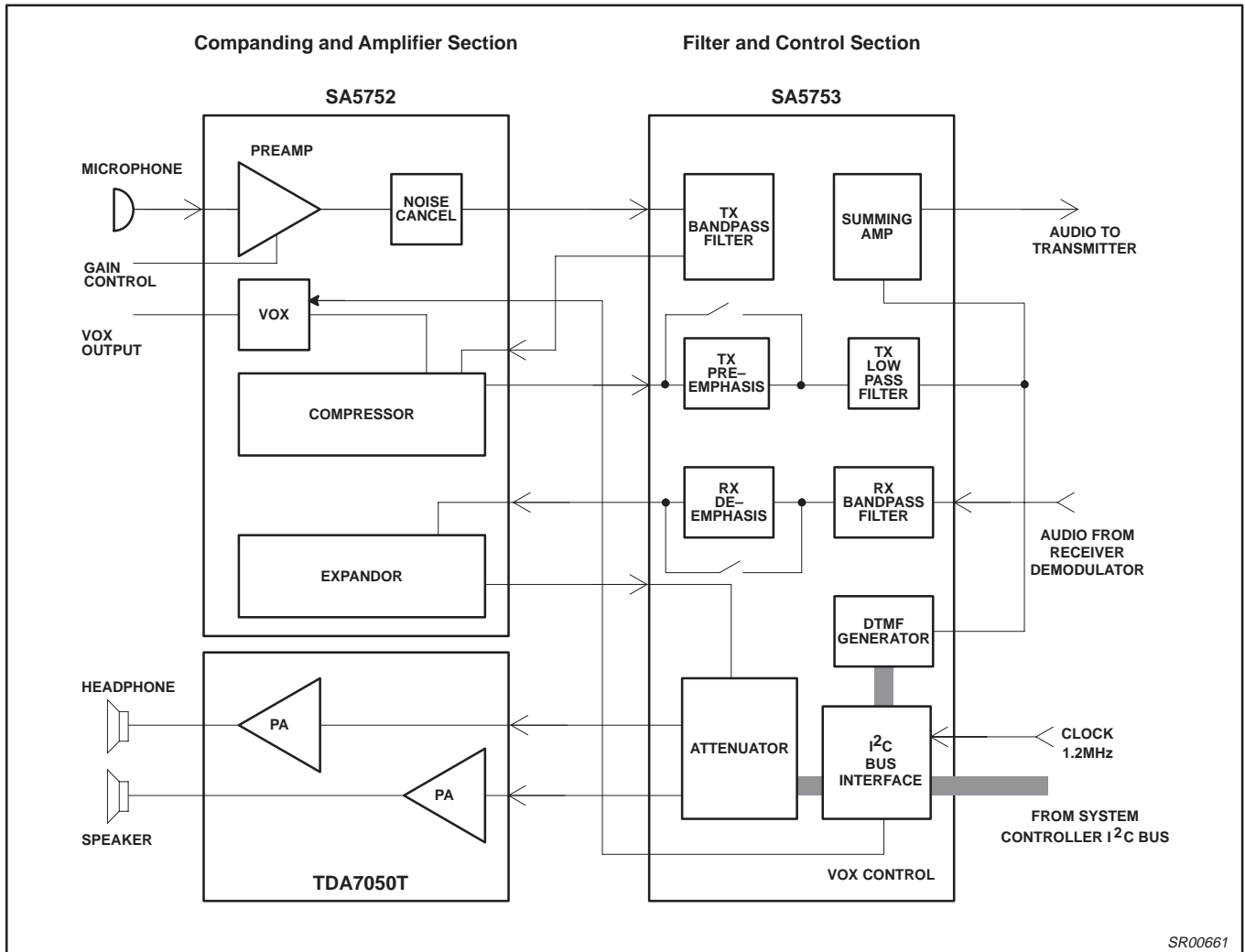


Figure 4. Typical Configuration of Audio Processor (APROC) System Chip Set

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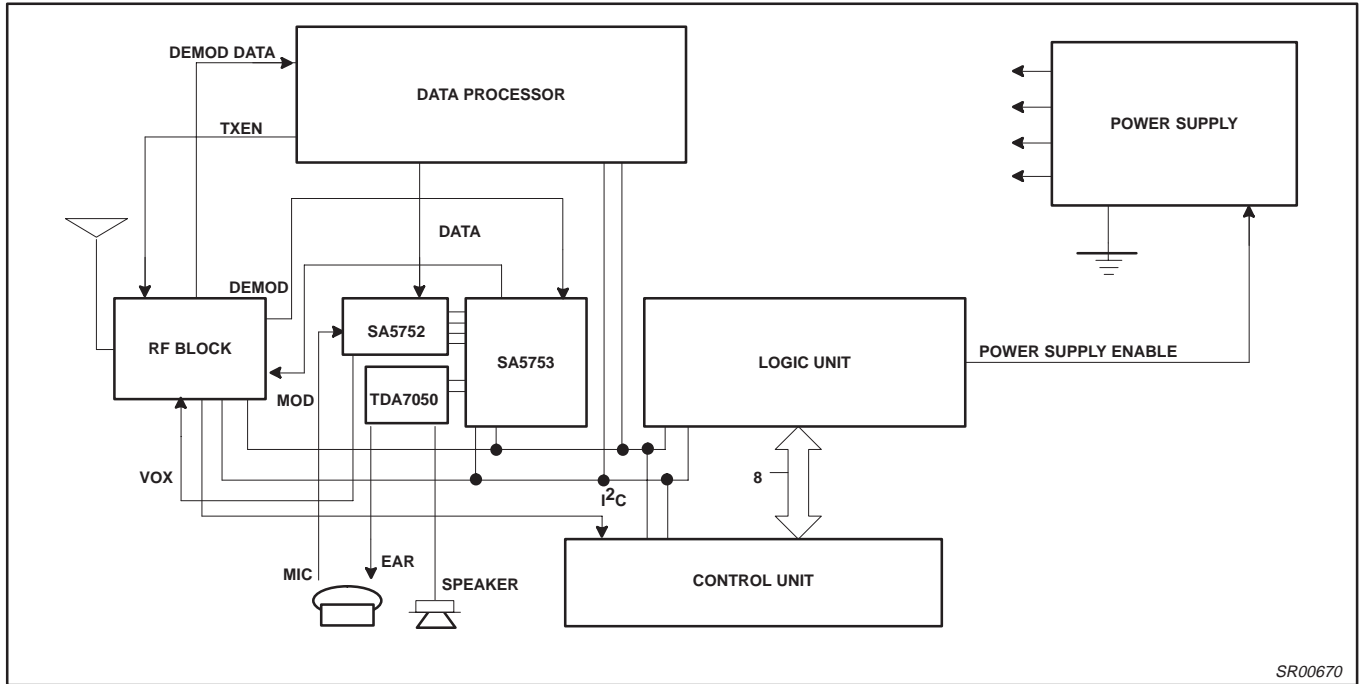


Figure 5. APROC Application Diagram

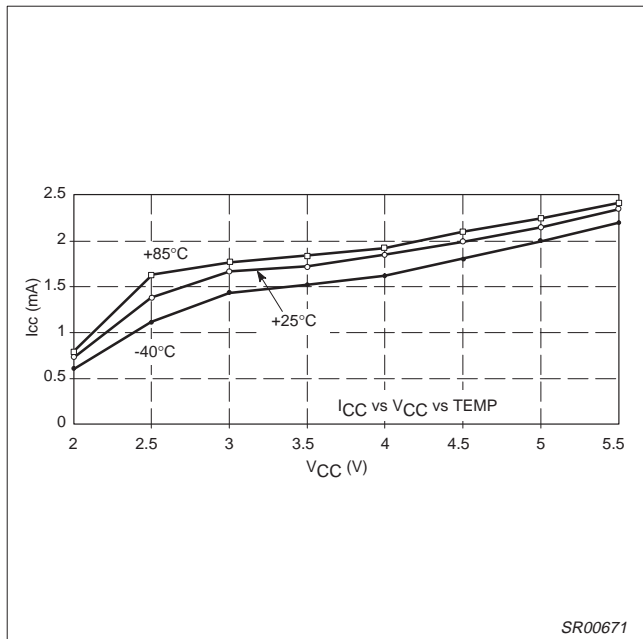


Figure 6. SA5753 Normal Operation

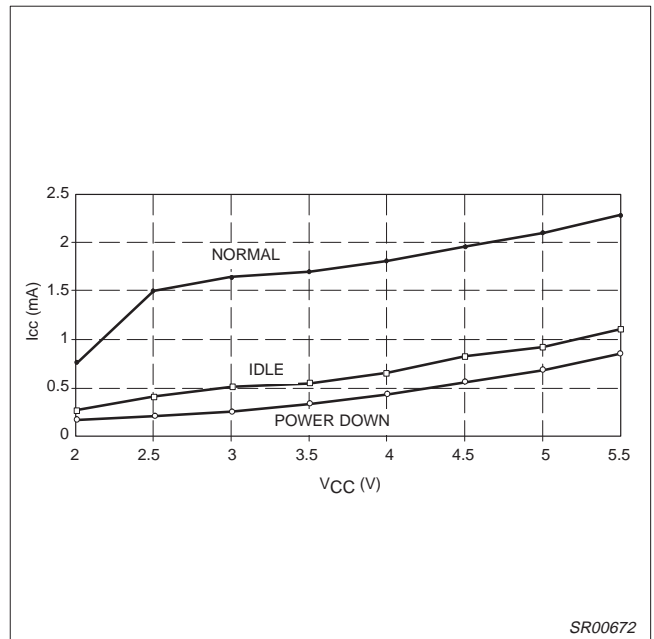


Figure 7. SA5753 Power Mode Comparison (I_{CC})

Audio processor – filter and control section

SA5753

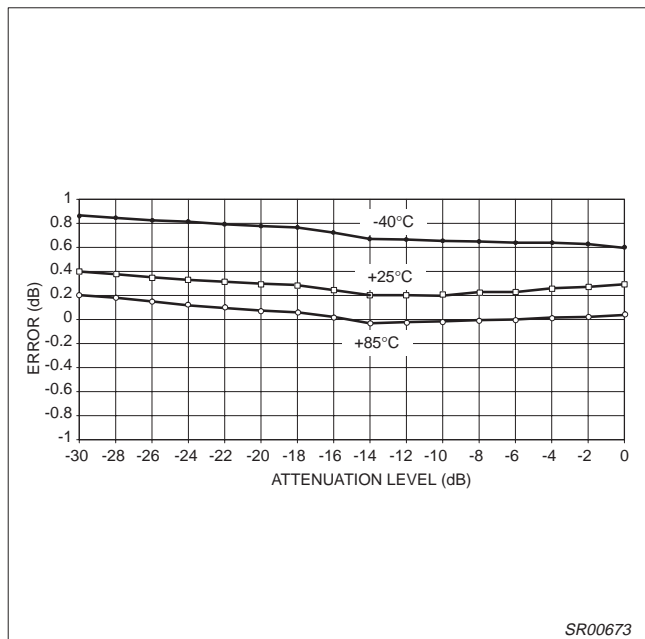


Figure 8. Gain Control, A6 Linearity

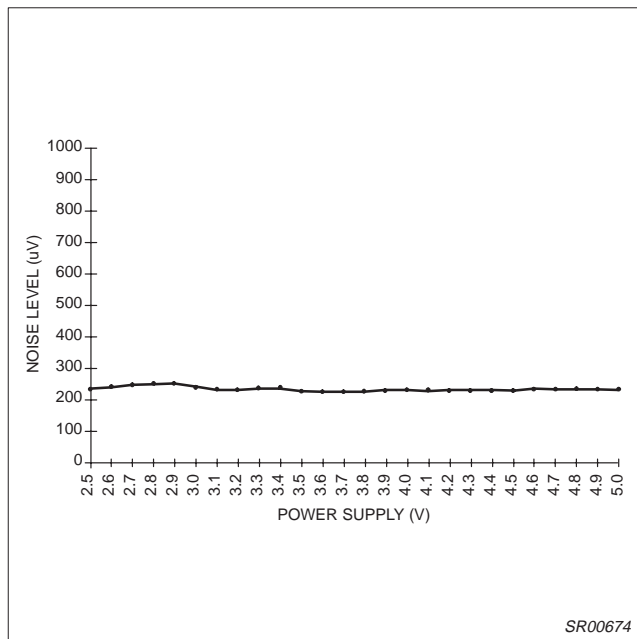


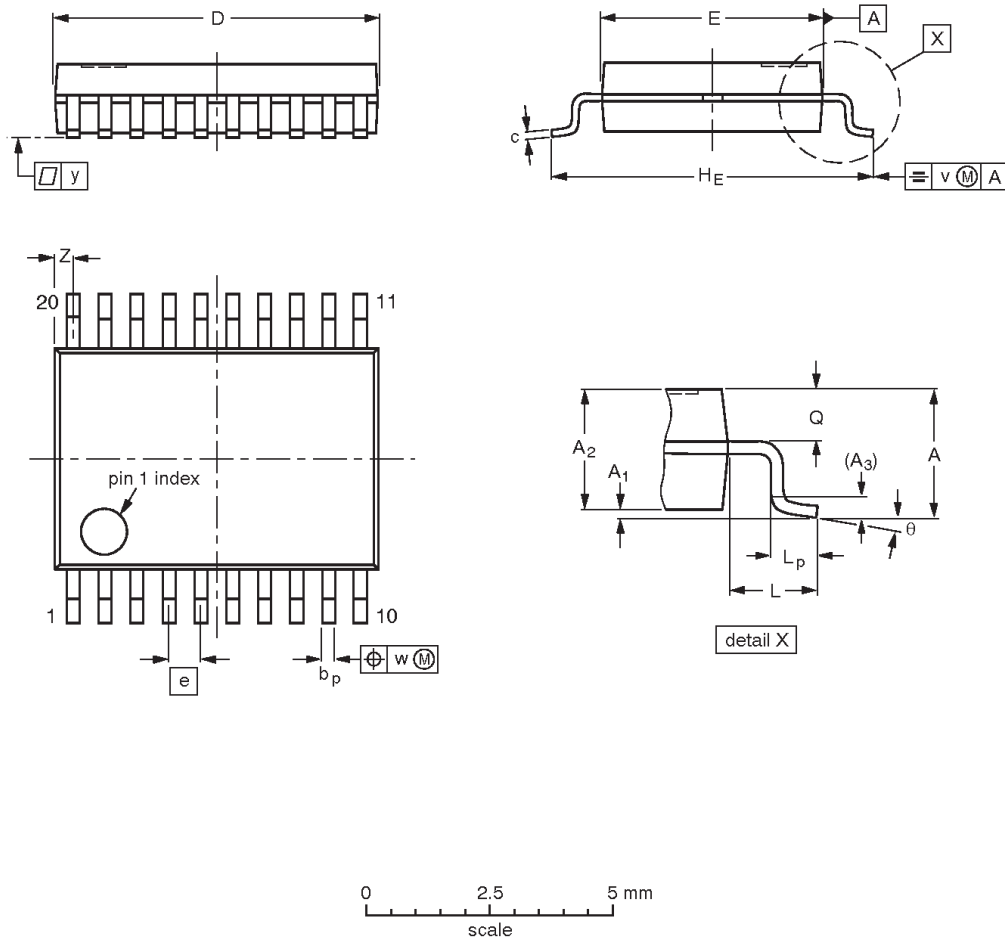
Figure 9. Power Supply vs Noise at TXBPF (25°C)

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SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT266-1						90-04-05 95-02-25

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SA5753

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Data Sheet Identification	Product Status	Definition
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