



BRAVO-DSD SA9227

Stereo In/Out
DSD64/ DSD128,
PCM 32Bit/ 384KHz
USB Audio Streaming Controller

Datasheet v1.3

SAVITECH Corporation



BRAVO-DSD/PCM SA9227

USB Audio Streaming Controller



Overview

The SA9227 is a high performance up to 32bit, 384KHz PCM and DSD64/128 streaming USB High-Speed compliant audio streaming controller. It features one stereo playback and recording pairs and one IEC60958 S/PDIF receive and transmit streaming pair. The SA9227 is ideal for both one stereo-in and one stereo-out professional digital audio interface applications. Its PCM resolution and sampling rate can be configurable with 16/24/32 bit and 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384KHz respectively.

Features

- SA9227 optional iAP1/iAP2, require MFi (Made for iDevice) license
- USB 2.0 High-Speed Compliant
- USB Audio Class v1.0 and v2.0 supported
- Incredible Bravo sound quality supported by Savitech innovative Bravo Tech*1
 - Bravo Tech*1 supporting Jitter-less outputs using local clock in Async-mode
- Isochronous input and output endpoints for recording and playback
- One interrupt endpoint for HID
- One DSD interface for connect with external DSD DAC
- Support resolutions up to 32-bit and sampling rates up to 384KHz
- Two I2S input pairs and four I2S output pairs for PCM
 - Independent sample rates for each pairs
 - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384 KHz sampling rates
 - 16/24/32 bit resolution
- Built in IEC60958 professional S/PDIF TX and S/PDIF RX,
 - AES/EBU supported*
 - SCMS for copyright supported
 - Stereo SPDIF Input and S/PDIF Output
 - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384 KHz sampling rates
 - 16/24 bit resolution
 - DSD with S/PDIF TX
- Control and I/O
 - I2C bus
 - GPIOs
- 64-pin TQFP packages

*AES : Audio Engineering Society
*EBU : European Broadcasting Union

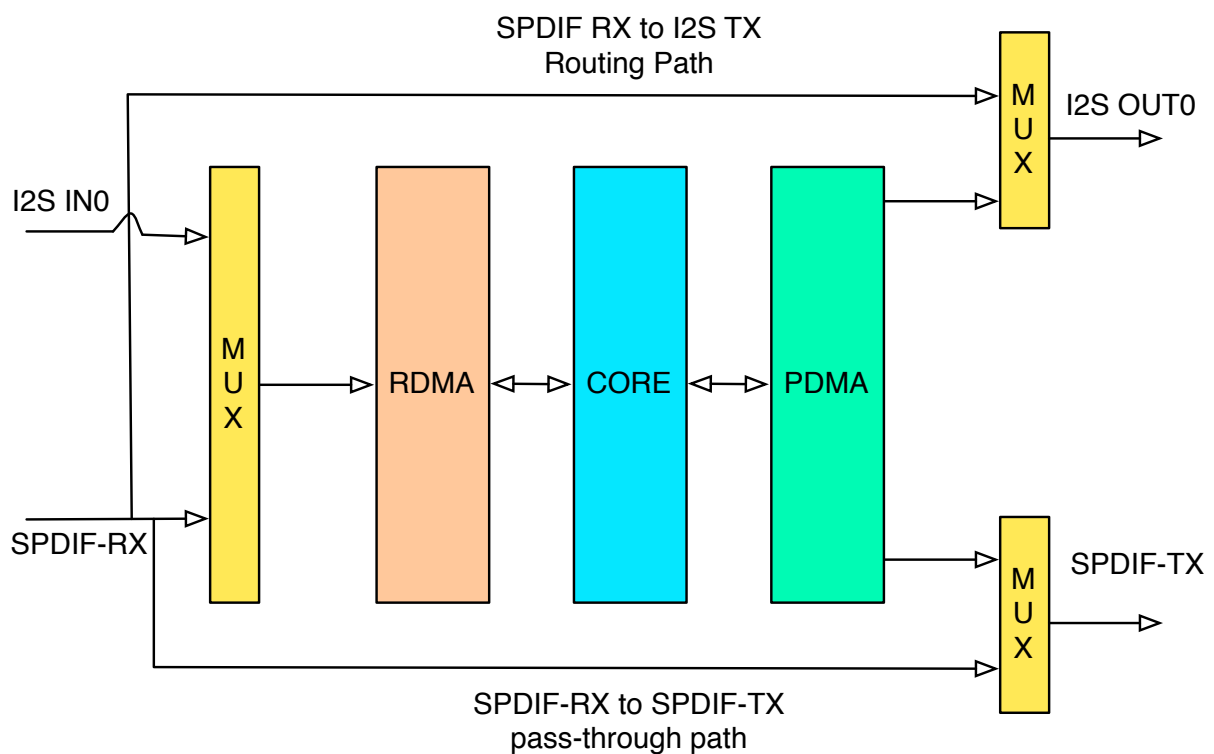
For iDevice, it is necessary to become a licensee of Apple Inc.

www.savitech-ic.com

Serial Audio Interfaces

■ Support 2-IN / 2-OUT

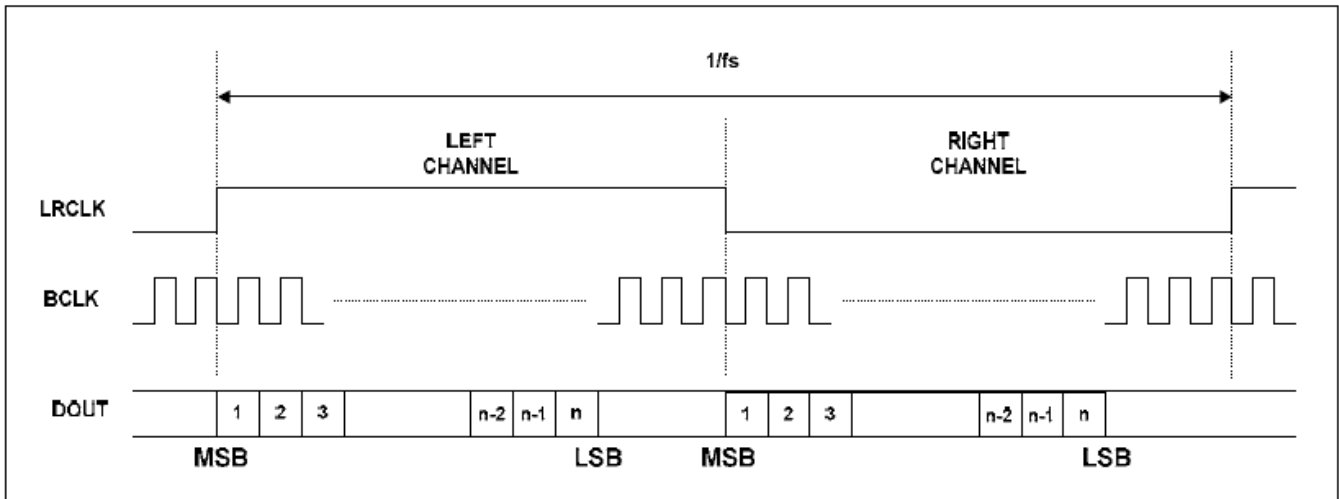
Two I2S input and four I2S output serial interfaces are supported to communicate with the external DACs / ADCs / CODECs. All the input channels share the same MCLK, SCLK and LRCLK and run at the same rate and same format. All the output channels share the same MCLK, SCLK and LRCLK and run at the same rate and same format.. Some internal routing capabilities are supported for audio stream switching, as shown in the following diagram.



Serial Audio Interfaces Formats

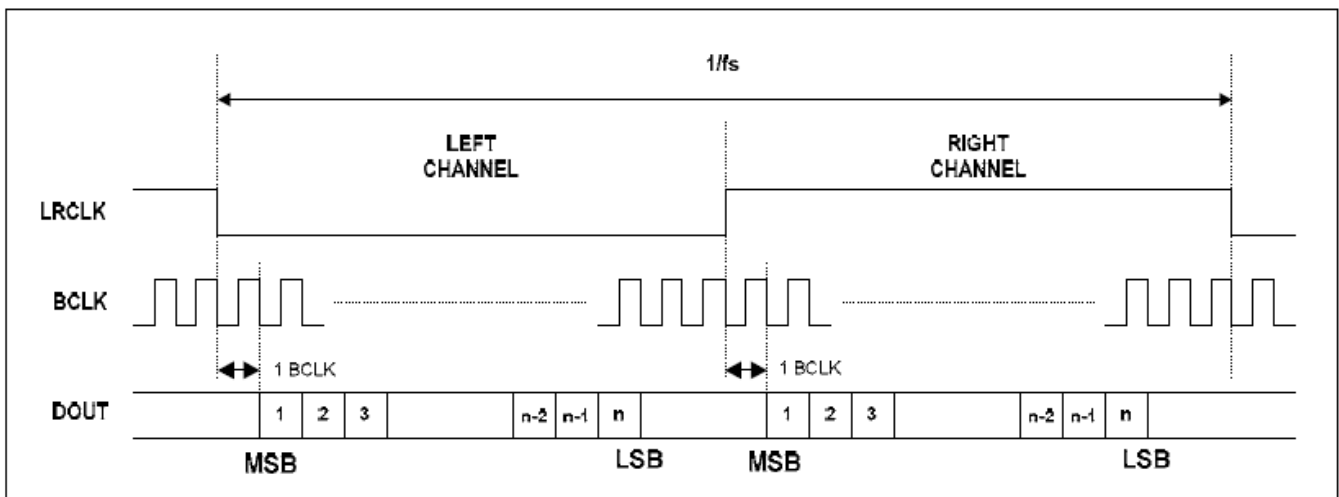
■ L-justified format:

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.



■ I2S format

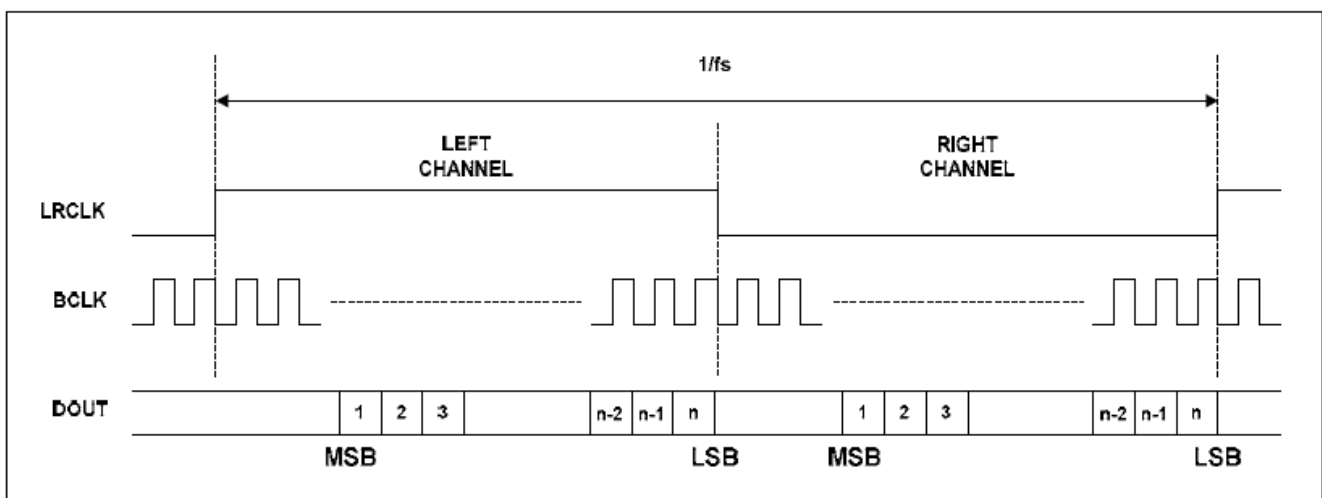
In I2S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.



Serial Audio Interfaces Formats

■ R-justified format

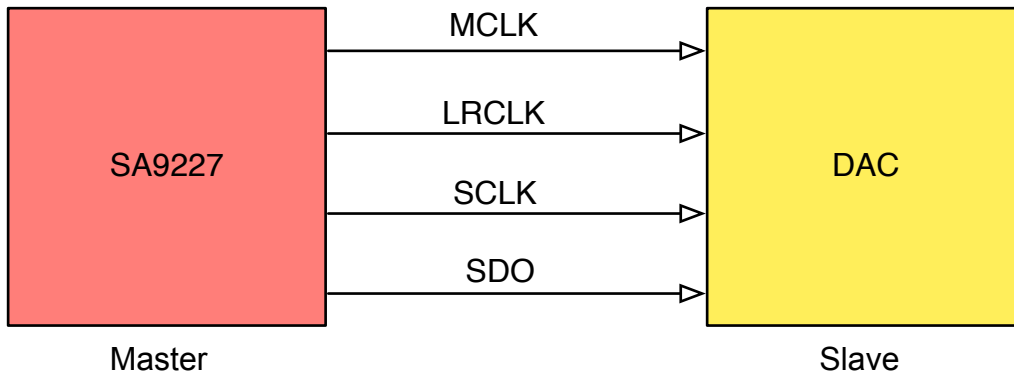
In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition. In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.



Serial Audio Interfaces Configuration-DAC

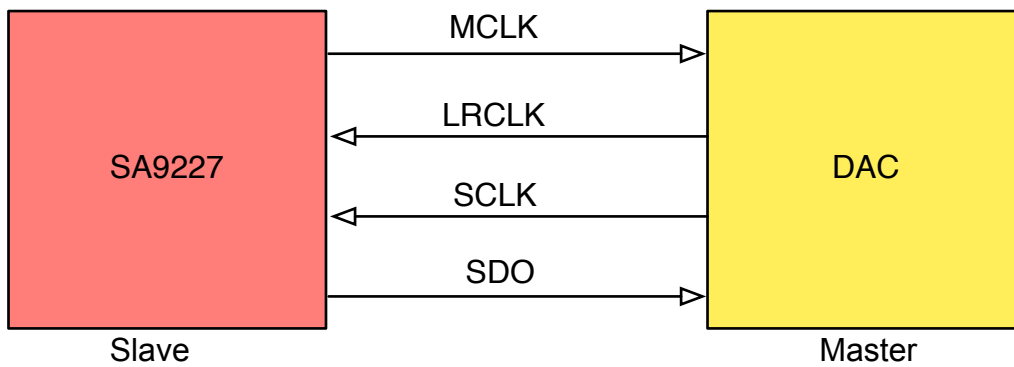
- SA9227 supports both master mode and slave mode for following configurations.

Master Mode



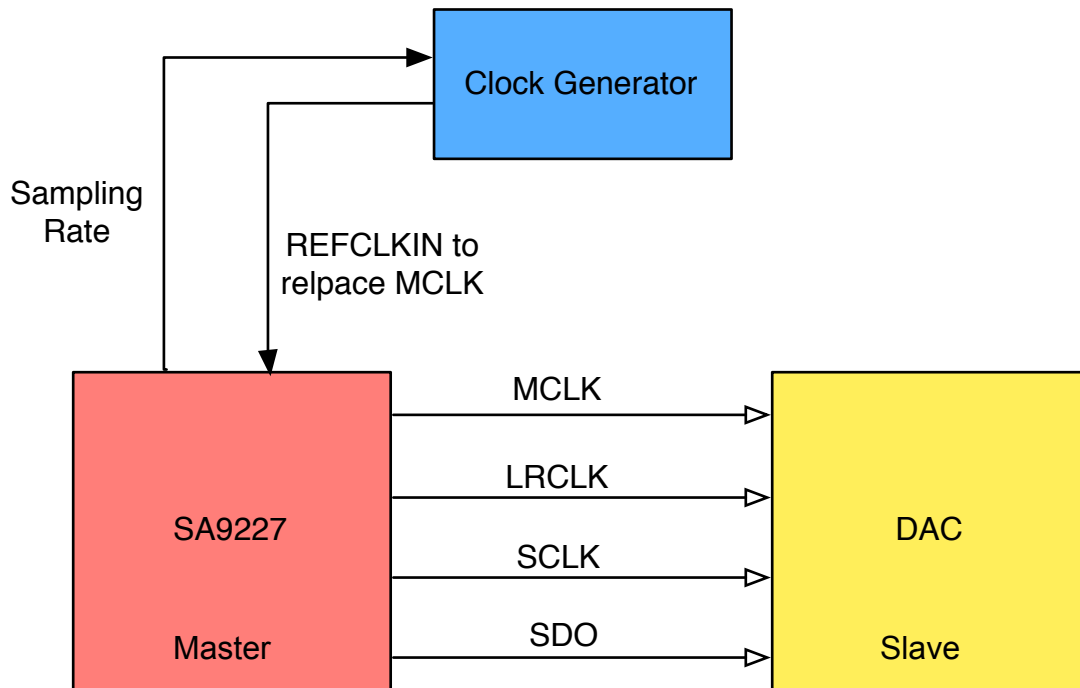
SA9227 I2S Master Mode connection

Slave Mode

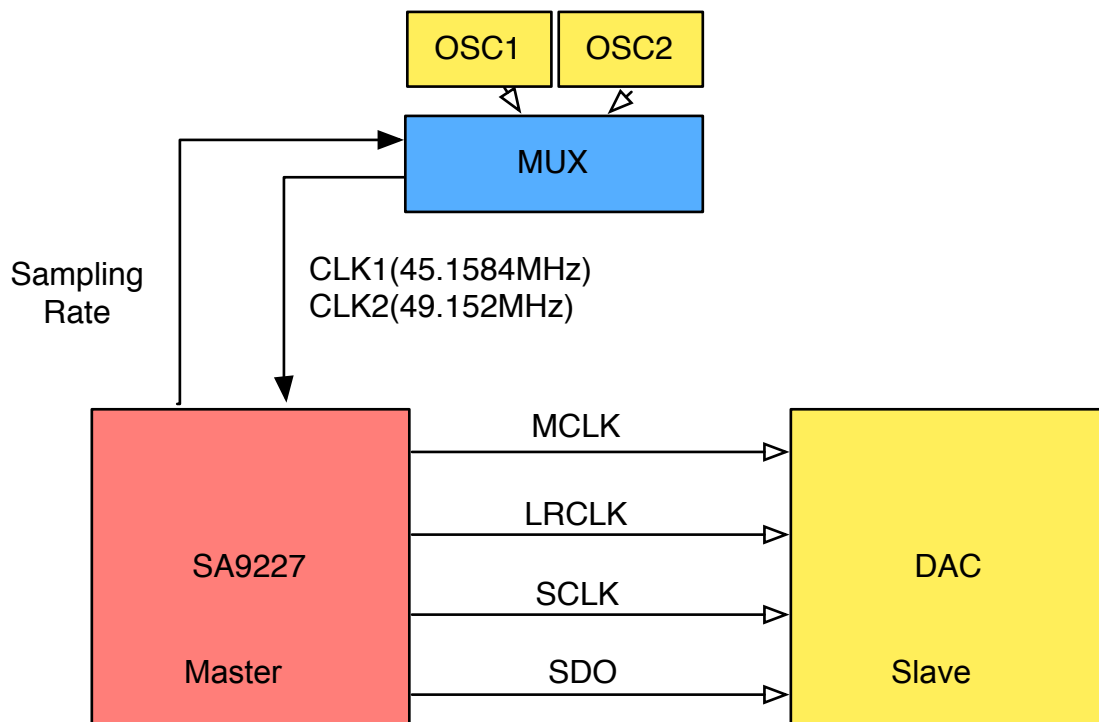


SA9227 I2S Slave Mode connection

Serial Audio Interfaces Configuration-DAC

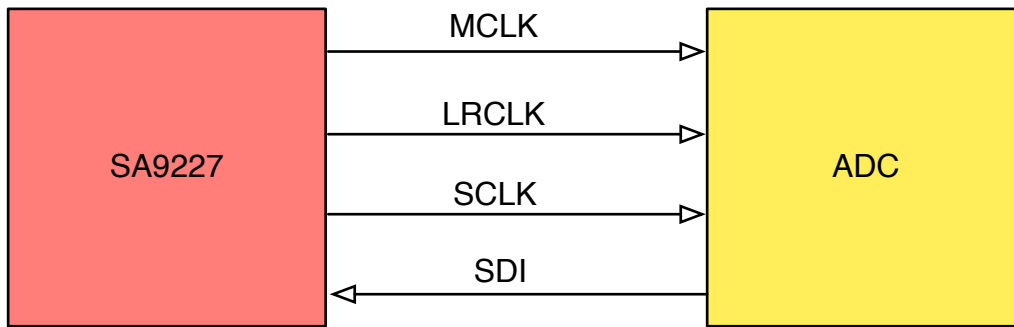


Master Mode (with external REFCLKIN), Mode 0



Master Mode (with external REFCLKIN), Mode 1

Serial Audio Interfaces Configuration-ADC



DSD Audio Data Interfaces

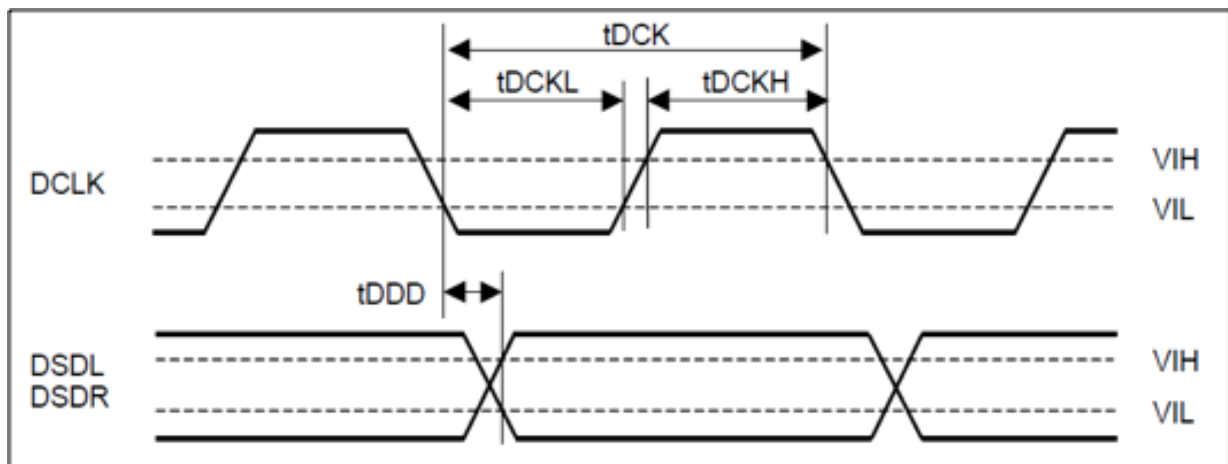
Playback:

SA9227 support three modes for playback DSD data over USB Audio stream

1. Sampling rate 88.2K and resolution 32-bits to transmit DSD data over USB streaming.
2. Sampling rate 176.4K and resolution 24-bits to transmit DSD64 data over USB streaming.
3. Sampling rate 352.8K and resolution 24-bits to transmit DSD128 data over USB streaming.

Summary these DSD formats:

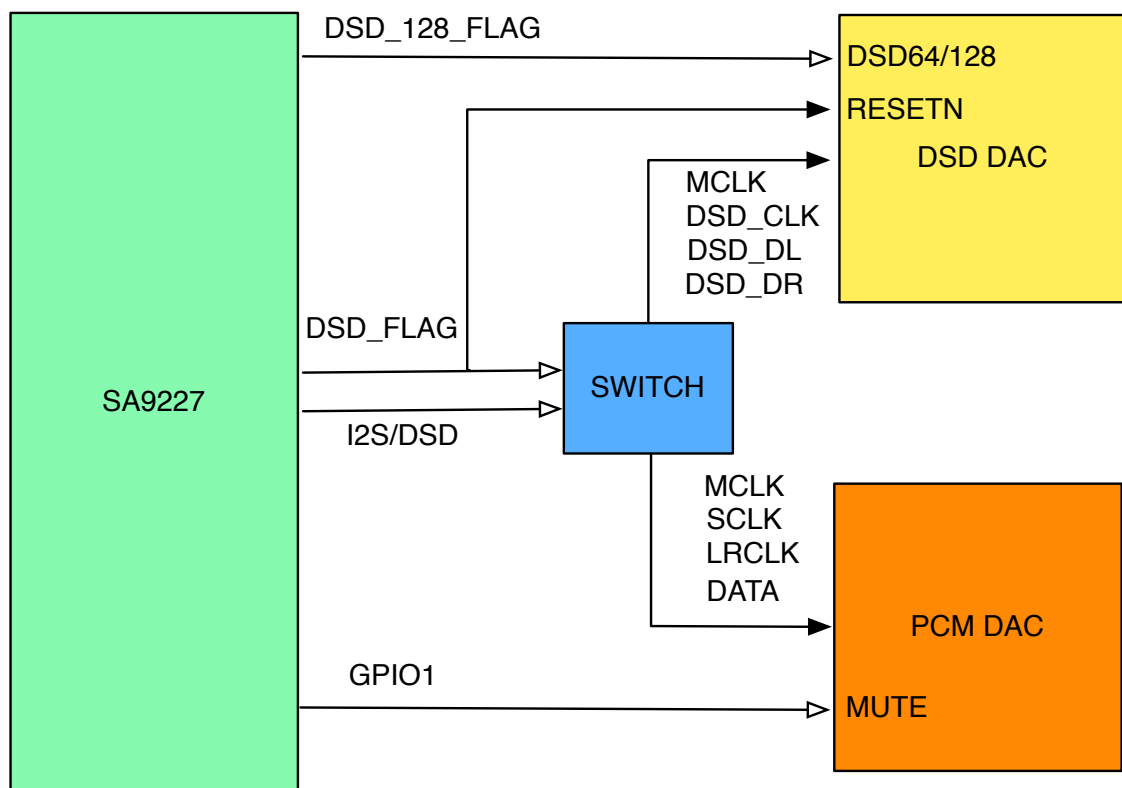
- | | | |
|-------------------------------------|-------------------|------------|
| ■ DSD format for 88.2K 32-bit: | DCLK (@2.8224MHz) | Direct-DSD |
| ■ DSD 64 format for 176.4K 24-bit: | DCLK (@2.8224MHz) | DoP/dCS |
| ■ DSD 128 format for 352.8K 24-bit: | DCLK (@5.6448MHz) | DoP/dCS |



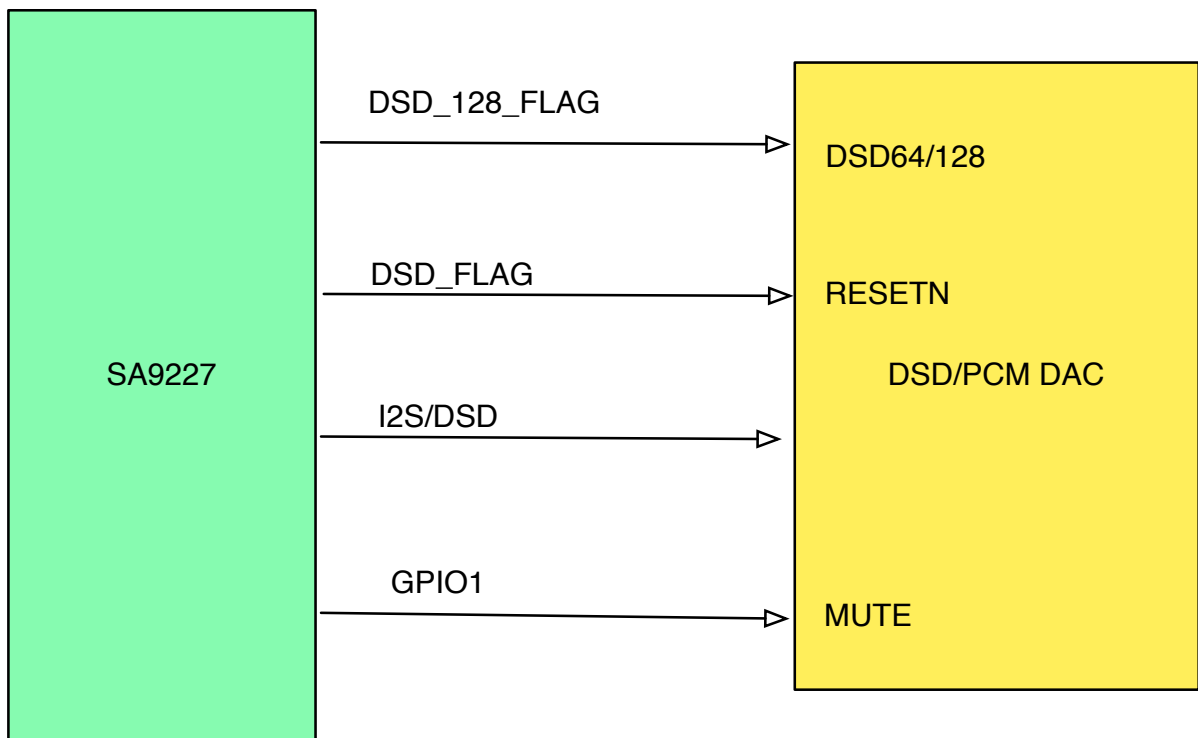
The DSDL and DSDR are all output by negative edge of DCLK. And DSD DAC will sample them by post edge of DCLK.

DSD External Control Signals

- DSD_FLAG : (0 : RESET, 1: Normal Operation in DSD format):
Used to RESETN DSD DAC.
- DSD_FLAG : (0 : in PCM mode, 1: in DSD mode):
used to switch DSD or PCM DAC.
- DSD_128 : (0 : in DSD 64 mode, 1: in DSD 128 mode):
used to switch DSD64 and DSD128 format for DSD DAC.



Application with PCM DAC and DSD DAC

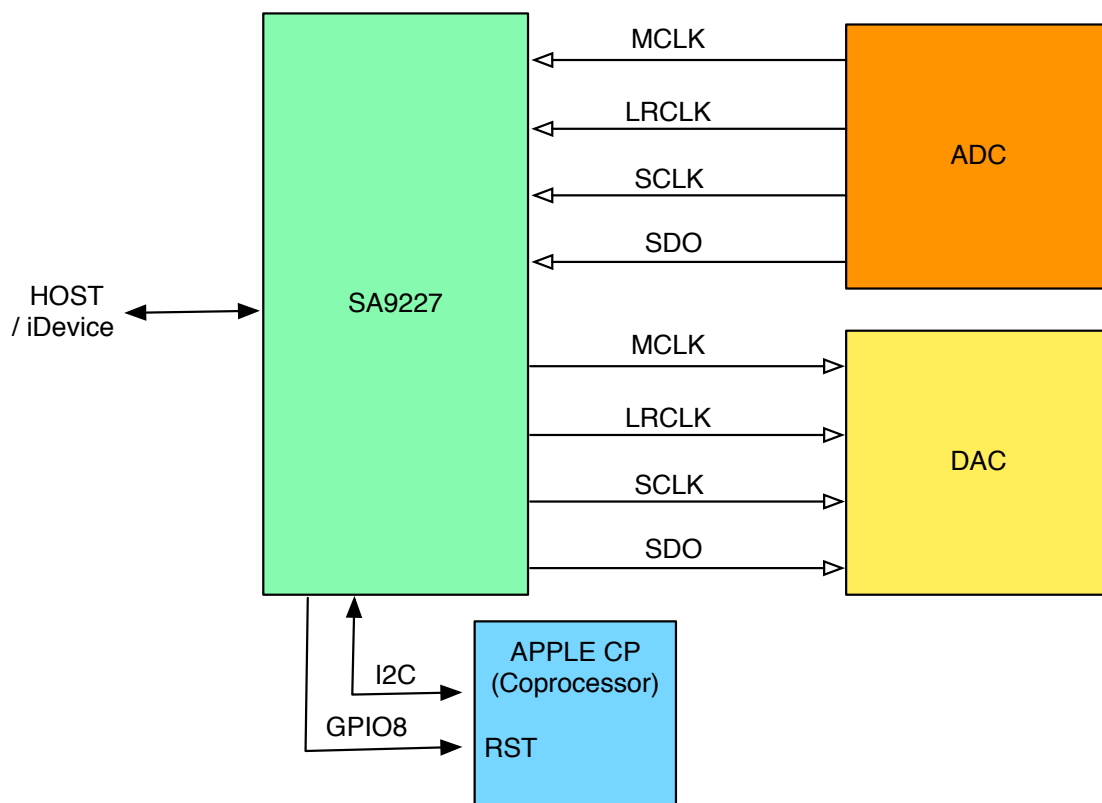


Application with PCM/DSD multi function DAC

iDevice support

Apple strongly recommends the use of digital audio paths to and from accessories. Apple device in USB Host Mode audio is the recommended approach. SA9227 will authenticate and identify itself to Apple device using iAP1/iAP2 CP before the iDevice will enumerate and start using USB Audio interface.

- Support 16 /24-bit linear PCM
- Support 44.1, 48KHz sampling rate and up to 384KHz for future.
- Support input and output audio interface
- Support Volume Control Feature Unit
- Support iAP1 and iAP2 by CP2.0B and CP2.0C.



Digital USB Audio Application for iDevice

For using of SA9227 on iDevice, It is necessary to become a licensee of Apple Inc. regarding "Made for iPod/iPhone/iPad License".

S/PDIF TX & RX Interfaces

SA9227 support one S/PDIF TX and one S/PDIF RX interfaces, each can support up to 24-bit 384K sampling rate. Built in IEC60958 professional S/PDIF TX and SPDIF RX,

- AES/EBU supported
- DSD stream output on S/PDIF TX
- 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384 KHz sampling rates
- 16/24 bit resolution
- DSD with SPDIF TX

I²C Master Interfaces

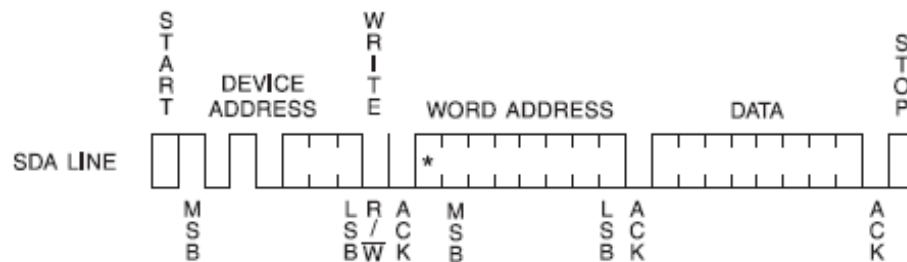
One serial I²C master is supported in SA9227 to control external peripheral devices (EEPROM). SA9227/SA9227i need an EEPROM to load Firmware code from it to SA9227. SA9227 support use I²C Master Interfaces to read/write CP to support Apple MFi.

I²C Slave Interfaces

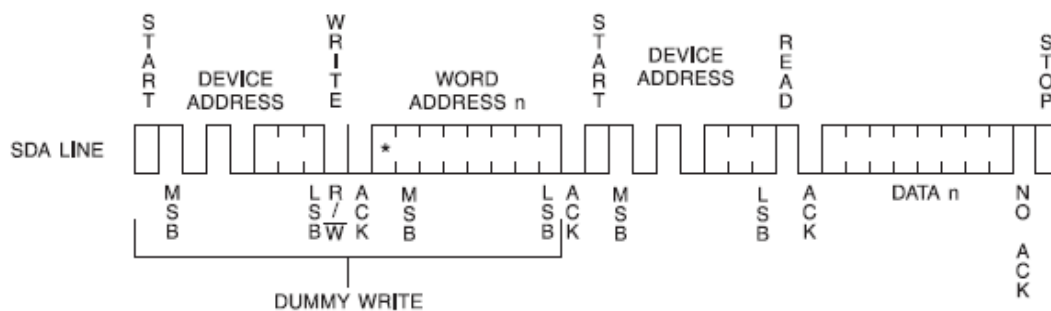
SA9227 have an I2C slave interface which is used for external uC to read status of SA9227. I2CS supports burst read /burst write.

Slave I2C

Byte Write



Random Read



Read Back Registers

SPDIF RX Read Back Registers:

S/PDIF RX Read Back Status Register 0

Offset 30

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|---|
| 7 | RO | 0 | Non-Audio Samples 1: Non-PCM audio samples 0: Linear PCM samples |
| 6 | RO | 0 | Copyright 1: Non-copyright 0: Copyright |
| 5 | RO | 0 | Pre-emphasis |
| 4 | RO | 0 | Lock Status 1: S/PDIF RX input is locked 0: S/PDIF RX input is unlocked |

S/PDIF RX Read Back Status Register 1

Offset 31

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|---------------|
| 7 | RO | 0 | Reserved |
| 6:0 | RO | 0 | Category code |

S/PDIF RX Read Back Status Register 3

Offset 32

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|---|
| 7 | RO | 0 | Reserved |
| 6 | RO | 0 | Professional mode 1: Professional mode 0: Consumer mode |
| 5 | RO | 0 | Validity |
| 4 | RO | 0 | Generation Level (L) |
| 3:0 | RO | 0s | S/PDIF Sample Rate reported from channel status bit 4'b0000: 44.1KHz 4'b0010: 48KHz 4'b0011: 32KHz 4'b1000: 88.2KHz 4'b1010: 96KHz |

SPDIF TX Read Back Registers :

S/PDIF TX Control Register 0

Offset 33

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|--|
| 7 | RO | 0 | Non-Audio Samples 1: Non-PCM audio samples 0: Linear PCM samples |
| 6 | RO | 0 | Copyright 1: Non-copyright 0: Copyright |
| 5 | RO | 0 | Pre-emphasis |
| 4 | RO | 0 | Reserved |
| 3:0 | RO | 0000 | Reserved |

S/PDIF TX Control Register 1

Offset 34

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|---------------|
| 7 | RO | 0 | Reserved |
| 6:0 | RO | 0 | Category code |

S/PDIF TX Control Register 2

Offset 35

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|---|
| 7 | RO | 0 | Reserved |
| 6 | RO | 0 | Professional mode 1: Professional mode 0: Consumer mode |
| 5 | RO | 0 | Validity |
| 4 | RO | 0 | Generation Level (L) |
| 3:0 | RO | 0s | S/PDIF Sample Rate reported from channel status bit 4'b0000: 44.1KHz 4'b0010: 48KHz 4'b0011: 32KHz 4'b1000: 88.2KHz 4'b1010: 96KHz |

S/PDIF TX Control Register 3

Offset 36

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|--------|--|
| 7 | R_W | 1'b0 | Integrated S/PDIF transmitter enable 1: enabled 0: disabled |
| 6 | R_W | 1'b0 | Companion I2S enable 1: Enabled. The data is duplicated on the I2S data output pin. 0: Disabled |
| 5 | R_W | 1'b0 | 1: Force TX data to 0 when Validity (bit 16) is 1 and bit 1 is 0 (PCM data) 0: Do not change data when Validity is 1. (default) This bit is for the SCMS compatibility issues sometimes found when interfacing with MD devices. |
| 4:2 | R/W | 3'b010 | S/PDIF TX data source select 3'b110: Data is from the track 0/1 of the 8-CH I2S input (input 0) 3'b100: 8-channel Turbo Mode enable. Data is from the 8-CH I2S streams (EP3) 3'b011: Data is from Stereo mixer output 3'b010: Data is from the track 0/1 of the 8-CH I2S streams (EP3) 3'b001: 8-channel Turbo Mode enable. Data is from the 8-CH I2S input (EP2) 3'b000: Data is from EP6 |
| 1 | RO | 1'b0 | Reserved |

Offset 36 ~ 3F

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------|
| 7:0 | R_O | 8'h0 | reserved |

Offset 40

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF RX channel status Byte0 |

Offset 40

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF RX channel status Byte0 |

Offset 41

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF RX channel status Byte1 |

Offset 42

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF RX channel status Byte2 |

Offset 43

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF RX channel status Byte3 |

Offset 44

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF RX channel status Byte4 |

Offset 45

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF RX channel status Byte5 |

Offset 46 ~ 4F

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------|
| 7:0 | R_O | 8'h0 | reserved |

Offset 50

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte0 |

Offset 51

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte1 |

Offset 52

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte2 |

Offset 53

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte3 |

Offset 54

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte4 |

Offset 55

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte5 |

Offset 56

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte6 |

Offset 57

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte7 |

Offset 58

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte8 |

Offset 59

Length: 1 byte

| Bit | Type | Reset | Description |
|-----|------|-------|-------------------------------|
| 7:0 | R_O | 8'h0 | SPDIF TX channel status Byte9 |

General Purpose Interface IN /OUT

Sixteen GPIO pins are supported that can be controlled by standard USB HID requests.

| GPIOs | Definition Playback only | Definition Playback and recording |
|-------------------------|--|--------------------------------------|
| GPIO1 | Use for reset DAC | |
| GPIO2 | High/Full speed selector, "1": Full-speed, "0": High-speed | |
| GPIO3 | Selection of 49MHz, 45MHz external clocks for reference input pin (57 pin), '0': 49Mhz, '1':45MHz | |
| GPIO6 GPIO5 GPIO4 | GPIO[6:5:4:3] 0010: 32KHz 0001: 44.1KHz 0000: 48KHz 1101: 88.1KHz 1100: 96KHz 1011: 176.4KHz 1010: 192KHz 1001: 352.8KHz 1000: 384KHz | |
| GPIO8 | Used for Apple CP reset | |

DSD External Control Signals

SA9227 provide these pins for DSD and special usage

| FLAGS | Definition |
|--------------|--|
| SOF_FLAG | User can check this pin to understand USB is in suspend or not 0: USB is in suspend 1: USB is in normal mode |
| DSD_FLAG | User can check this pin to understand DSD mode is detected or not 0: PCM mode 1: DSD mode |
| DSD_128_FLAG | User can check this pin to understand which DSD mode is played now (DSD64 or DSD128 mode) 0: DSD 64 mode 1: DSD 128 mode |

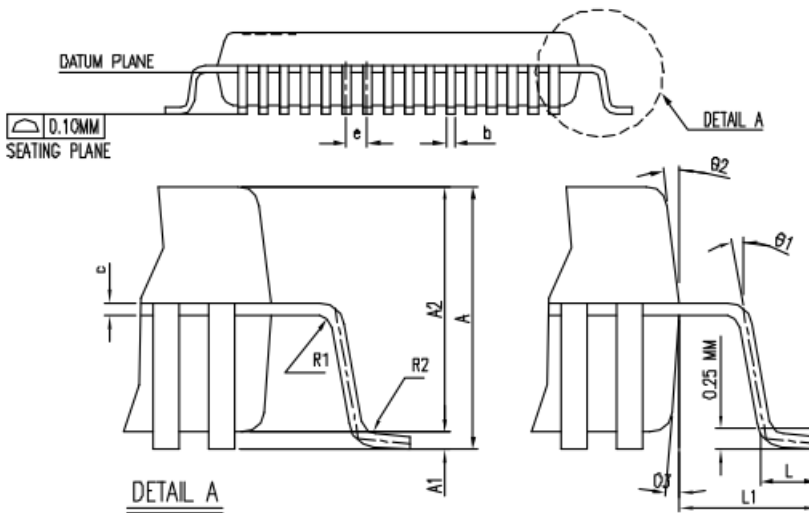
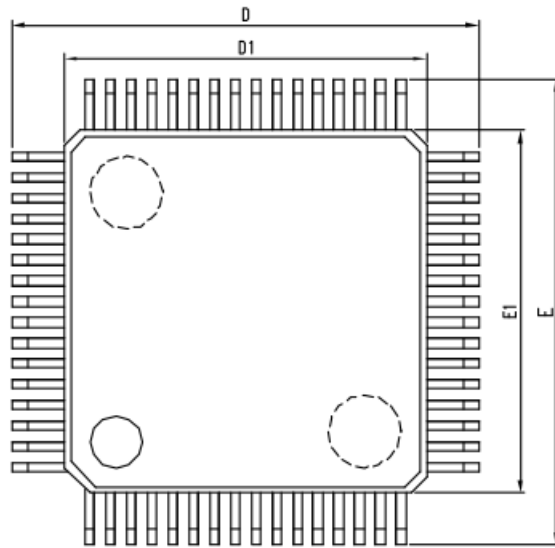
Pin Assignment

| Pin | Name | Pin | Name |
|-----|-------------------------|-----|-----------------|
| 1 | VDD | 33 | GPIO4 |
| 2 | GND | 34 | GPIO5 |
| 3 | VDD8OUT | 35 | GPIO6 |
| 4 | VDD | 36 | GPIO7 |
| 5 | GND | 37 | GPIO8 |
| 6 | SPDRX | 38 | RESETN |
| 7 | VDD | 39 | VDD |
| 8 | VDD18 | 40 | SCL |
| 9 | SOF_FLAG | 41 | SDA |
| 10 | DSD_FLAG | 42 | SCLK0/ DSD_CLK |
| 11 | DSD_128_FLAG | 43 | VDD18 |
| 12 | REXT | 44 | VDD |
| 13 | VDD | 45 | SDATA00/ DSD_DL |
| 14 | VDD | 46 | MCLK0 |
| 15 | DP | 47 | LRCLK0/ DSD_DR |
| 16 | DM | 48 | SPDTX |
| 17 | GND | 49 | SCLK1 |
| 18 | XI | 50 | SDATA10 |
| 19 | XO | 51 | MCLK1 |
| 20 | VDD18 | 52 | VDD |
| 21 | VDD | 53 | LRCLK1 |
| 22 | GND | 54 | SCL1 |
| 23 | GND | 55 | SDA1 |
| 24 | VDD | 56 | VDD |
| 25 | GND | 57 | REFCLKIN |
| 26 | VDD | 58 | VDD18 |
| 27 | GPIO0 | 59 | TEST1 |
| 28 | VDD18 | 60 | TEST2 |
| 29 | VDD | 61 | TEST3 |
| 30 | GPIO1 | 62 | TEST4 |
| 31 | GPIO2 / USB (HS/FS) SEL | 63 | TEST5 |
| 32 | GPIO3 | 64 | TEST6 |

Pin Description

| Pin | Name | I/O/P | Description |
|-----|-------------------------|-------|---|
| 1 | VDD | P | I/O power |
| 2 | GND | P | I/O ground |
| 3 | VDD8OUT | P | 1.8V OUT |
| 4 | VDD | P | SPDIF RX power |
| 5 | GND | P | SPDIF RX ground |
| 6 | SPDRX | I | S/PDIF RX input |
| 7 | VDD | P | I/O power |
| 8 | VDD18 | P | Core power |
| 9 | SOF_FLAG | O | USB SOF(Start Of Frame) indicator |
| 10 | DSD_FLAG | O | DSD/PCM indicator: 0: PCM 1: DSD |
| 11 | DSD_128_FLAG | O | DSD64/DSD128 indicator |
| 12 | REXT | I | USB2.0 PHY signals |
| 13 | VDD | P | USB2.0 PHY power |
| 14 | VDD | P | USB2.0 PHY power |
| 15 | DP | I/O | USB2.0 signals |
| 16 | DM | I/O | USB2.0 signals |
| 17 | GND | P | USB2.0 PHY ground |
| 18 | XI | I/O | 12MHz X'stal |
| 19 | XO | I/O | 12MHz X'stal |
| 20 | VDD18 | P | USB2.0 PHY power |
| 21 | VDD | P | PLL power |
| 22 | GND | P | PLL ground |
| 23 | GND | P | PLL ground |
| 24 | VDD | P | PLL power |
| 25 | GND | P | PLL ground |
| 26 | VDD | P | PLL power |
| 27 | GPIO0 | I/O | General purpose I/O |
| 28 | VDD18 | P | Core power |
| 29 | VDD | P | I/O power |
| 30 | GPIO1 | I/O | For DSD DAC reset |
| 31 | GPIO2 / USB (HS/FS) SEL | I/O | HID/ Pull-high for USB Full-speed or pull-low for High-speed select |
| 32 | GPIO3 | I/O | Audio stream sampling rate indicator 1 |

| Pin | Name | I/O/P | Description |
|-----|-----------------|-------|---|
| 33 | GPIO4 | I/O | Audio stream sampling rate indicator 1 |
| 34 | GPIO5 | I/O | Audio stream sampling rate indicator 2 |
| 35 | GPIO6 | I/O | Audio stream sampling rate indicator 3 |
| 36 | GPIO7 | I/O | Audio stream resolution indicator 1 |
| 37 | GPIO8 | I/O | For Apple CP reset |
| 38 | RESETN | I | Power-on reset signal (active low) |
| 39 | VDD | P | I/O power |
| 40 | SCL | I/O | Master I2C clock |
| 41 | SDA | I/O | Master I2C data |
| 42 | DASCLK/ DSD_CLK | I/O | I2S output SCLK/ DSD_CLK |
| 43 | VDD18 | P | Core power |
| 44 | VDD | P | I/O power |
| 45 | DADAT/ DSD_DL | O | I2S output data / DSD_DL |
| 46 | DAMCLK | I/O | I2S output MCLK |
| 47 | DASYNC/ DSD_DR | I/O | I2S output LRCLK/ DSD_DR |
| 48 | SPD TX | O | S/PDIF TX output |
| 49 | ADSCLK | I/O | I2S input SCLK |
| 50 | ADDAT | I | I2S input data pin |
| 51 | ADMCLK | I/O | I2S input MCLK |
| 52 | VDD | P | I/O power |
| 53 | ADSYNC | I/O | I2S input LRCLK |
| 54 | SCL1 | I/O | Slave I2C CLK |
| 55 | SDA1 | I/O | Slave I2C SDA |
| 56 | VDD | P | I/O power |
| 57 | REFCLKIN | I | Optional external reference clock input |
| 58 | VDD18 | P | Core power |
| 59 | TEST1 | I | For TEST, need pull-high |
| 60 | TEST2 | I | For TEST, need pull-down |
| 61 | TEST3 | I | For TEST, need pull-down |
| 62 | TEST4 | I | For TEST, need pull-down |
| 63 | TEST5 | I | For TEST, need pull-down |
| 64 | TEST6 | I | For TEST, need pull-down |



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|-----------------|------|------|-------------------|-------|--------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.0019 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0078 |
| e | 0.40 BASIC | | | 0.016 BASIC | | |
| D | 9.00 BASIC | | | 0.354 BASIC | | |
| D1 | 7.00 BASIC | | | 0.276 BASIC | | |
| E | 9.00 BASIC | | | 0.354 BASIC | | |
| E1 | 7.00 BASIC | | | 0.276 BASIC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF. | | | 0.039 REF. | | |
| R1 | 0.08 | | | 0.0031 | | |
| R2 | 0.08 | | 0.20 | 0.0031 | | 0.0078 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | | | 0° | | |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| JEDEC | MS-026 (BBD) | | | | | |

*NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE.
 " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

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