Signetics

SAB1256
1GHz Divide-by-256 Prescaler

Product Specification

02899d

Linear Products

DESCRIPTION

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70MHz up to 1GHz, for a supply voltage of 5V± 10% and an ambient temperature of 0 to 70°C. It features a high sensitivity and low harmonic contents of the output signal.

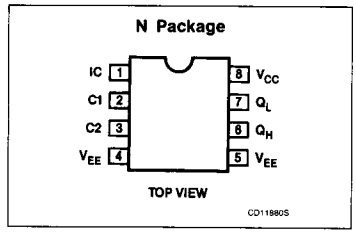
FEATURES

- **3mV (typ.) sensitivity**
- **AC input coupling, internally biased**
- **Outputs edge-controlled for low RFI**
- **235mV typical power dissipation**
- **Low output impedance ≈ 1kΩ**

APPLICATIONS

- **PLL or FLL tuning systems, FM/communications/TV**
- **Frequency counters**

PIN CONFIGURATION



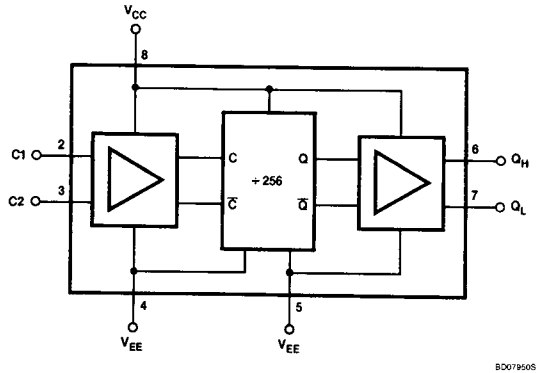
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97)	0 to 70°C	SAB1256N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (DC)	7	V
V_I	Input voltage	0 to V_{CC}	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Junction temperature	125	°C
θ_{CA}	Thermal resistance from crystal to ambient	120	°C/W

BLOCK DIAGRAM



NOTE:
Divide-by-256 = 8 binary dividers.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = 0V (ground); V_{CC} = 5V; T_A = 25°C, unless otherwise specified. The circuit has been designed to meet the DC specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{OH}	Output voltage HIGH level			V_{CC}	V
V_{OL}	LOW level			V_{CC} - 0.8	V
I_{CC}	Supply current		47	55	mA

AC ELECTRICAL CHARACTERISTICS

V_{EE} = 0V (ground); V_{CC} = 5V ± 10%; T_A = 0°C to +70°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$V_{I(RMS)}$	Input voltage RMS value (see Figure 2) Input frequency 70MHz 150MHz 300MHz 500MHz 900MHz 1GHz		 9 4 3 3 2 3	 17.5 10 10 10 10 17.5	 mV mV mV mV mV mV
$V_{I(RMS)}$	Input overload voltage RMS value input frequency range 70MHz to 1GHz			200	mV
$V_{O(P-P)}$	Output voltage swing	0.8	1		V
R_O	Output resistance		1		kΩ
ΔV_O	Output unbalance			0.1	V
t_{TLH}	Output rise time[1] f_I = 1GHz		40		ns
t_{THL}	Output fall time f_I = 1GHz		40		ns

NOTE:
1. Between 10% and 90% of observed waveform.

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70MHz up to 1GHz, for a supply voltage of 5V ± 10% and an ambient temperature of 0 to 70°C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

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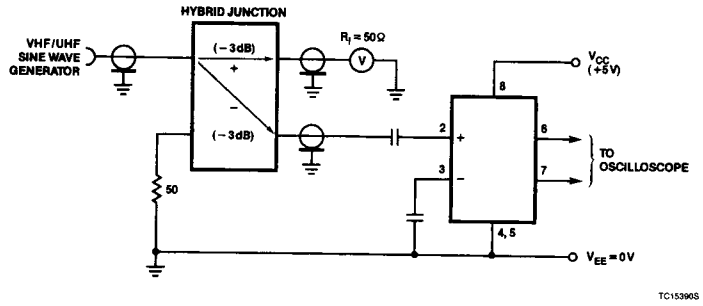

NOTES:
Cables must be 50Ω coaxial.
The capacitors are leadless ceramic (multi-layer capacitors) of 10nF.
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Hybrid junction is ANZAC H-183-4 or similar.

Figure 1. Test Circuit for Defining Input Voltage

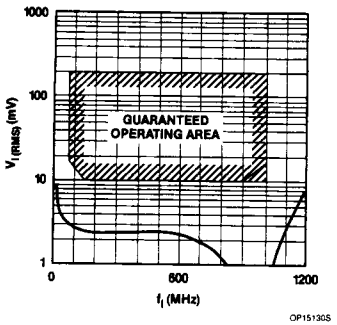
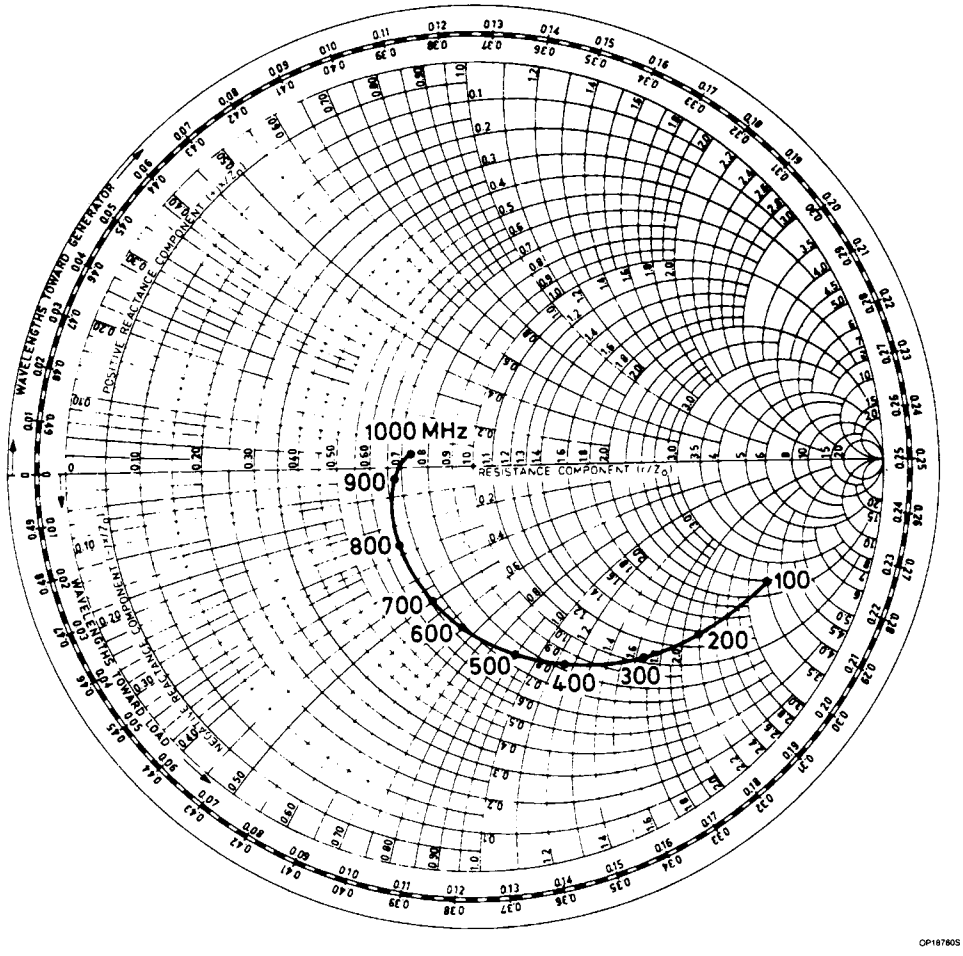


Figure 2. Typical Sensitivity Curve Under Nominal Conditions



NOTE:
$V_{I(RMS)}$ = 25mV; V_{CC} = 5V; reference value = 50Ω

Figure 3. Smith Chart of Typical Input Impedance

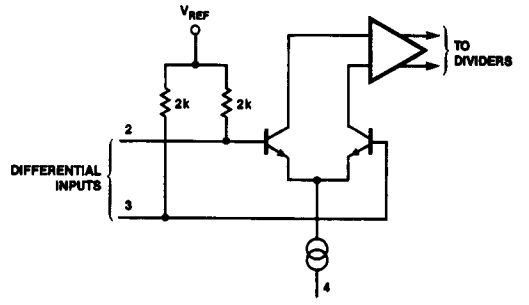
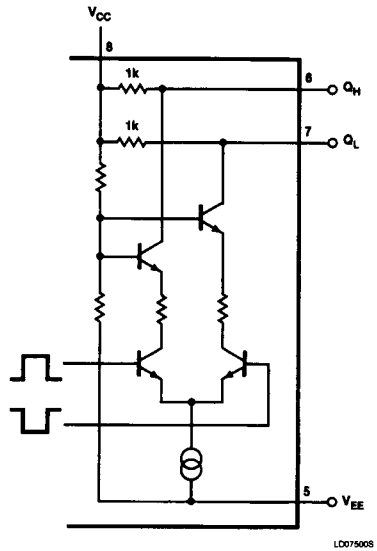
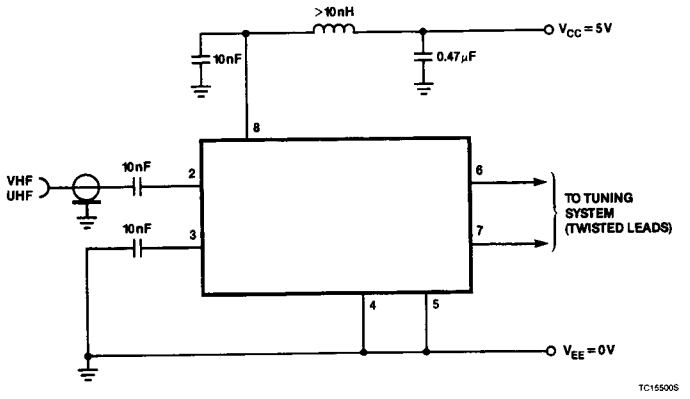


Figure 4. Input Stage



NOTE:
V_{CC} = 5V; I = 1mA.

Figure 5. Output Stage



NOTE:
Application in a television tuning system. The output peak-to-peak voltage is about 1V.

Figure 6. Circuit Diagram

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