



COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 4 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I²C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 4 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I²C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 13)	V _{P1}	typ.	12 V
(pin 19)	V _{P2}	typ.	13 V
(pin 14)	V _{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 13)	I _{P1}	typ.	30 mA
(pin 19)	I _{P2}	typ.	0,1 mA
(pin 14)	I _{P3}	typ.	0,6 mA
Total power dissipation	P _{tot}	typ.	380 mW
Operating ambient temperature range	T _{amb}		-20 to +70 °C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT 101A).

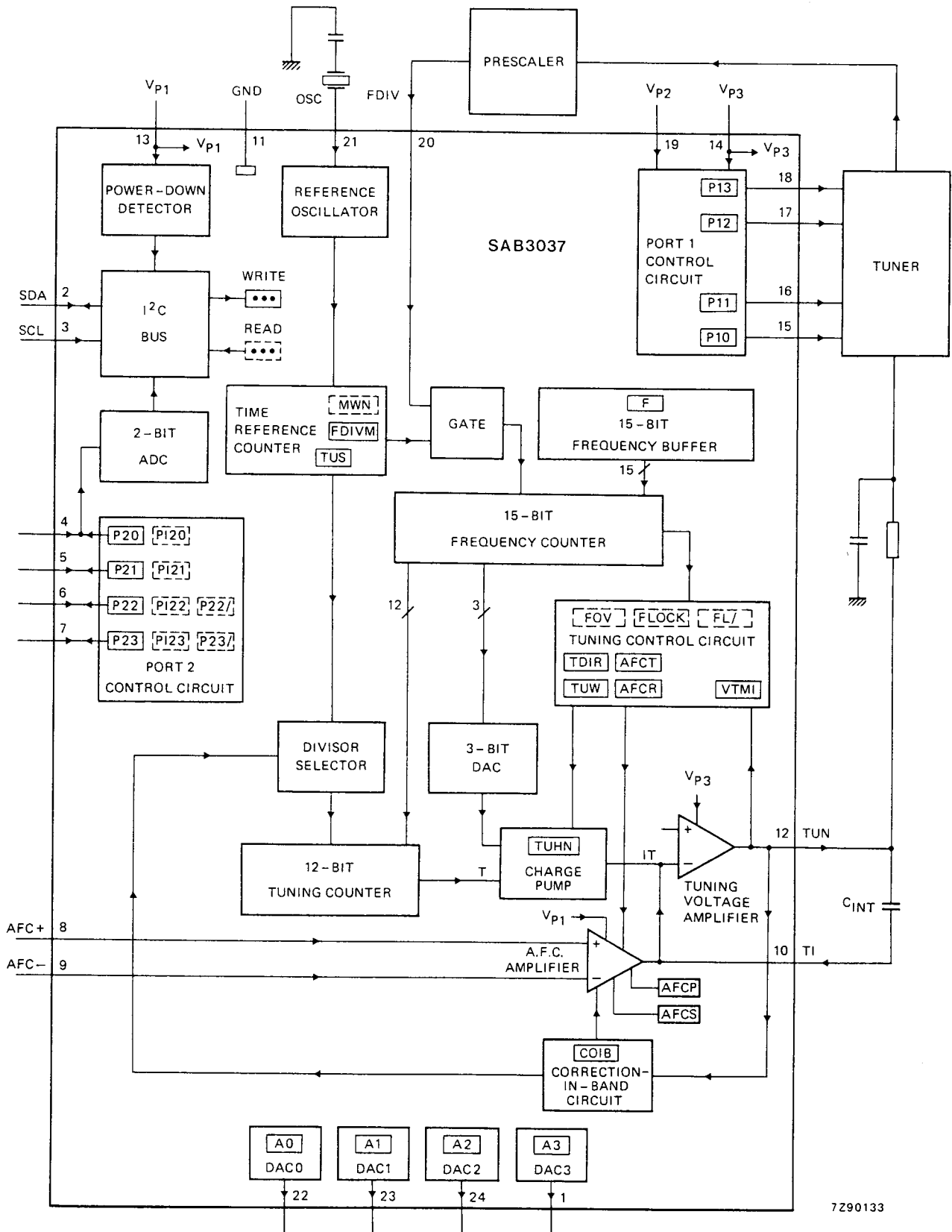


Fig. 1 Block diagram.

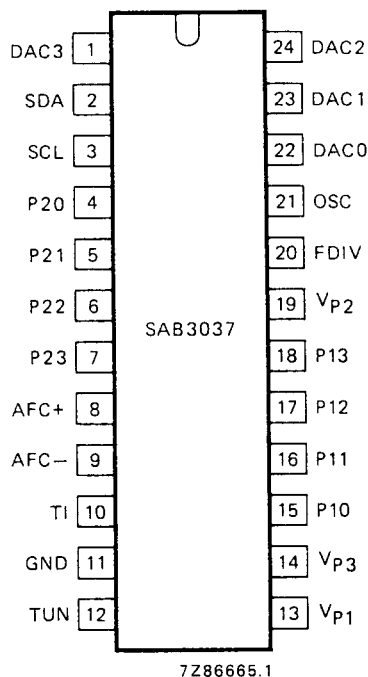
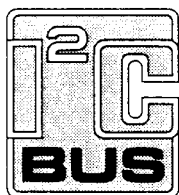


Fig. 2 Pinning diagram.

PINNING

1	DAC3	output of static DAC
2	SDA	} I ² C bus
3	SCL	
4	P20	} general purpose input/output ports
5	P21	
6	P22	
7	P23	} a.f.c. inputs
8	AFC+	
9	AFC-	
10	TI	tuning voltage amplifier inverting input
11	GND	ground
12	TUN	tuning voltage amplifier output
13	VP1	+ 12 V supply voltage
14	VP3	+ 32 V supply for tuning voltage amplifier
15	P10	} high-current band-selection output ports
16	P11	
17	P12	
18	P13	
19	VP2	positive supply for high-current band-selection output circuits
20	FDIV	input from prescaler
21	OSC	crystal oscillator input
22	DAC0	} outputs of static DACs
23	DAC1	
24	DAC2	



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I²C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50$ kHz equals $250 \mu A \mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50$ kHz equals $2^6 \times 2^3 \times 250 \mu A \mu s$ (typical).

The maximum tuning current I is $875 \mu A$ (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCT is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCT. If the frequency of the tuning oscillator does not remain within AFCT, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2} .

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analogue converters DAC0 to DAC3 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I²C bus; the I²C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/W bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

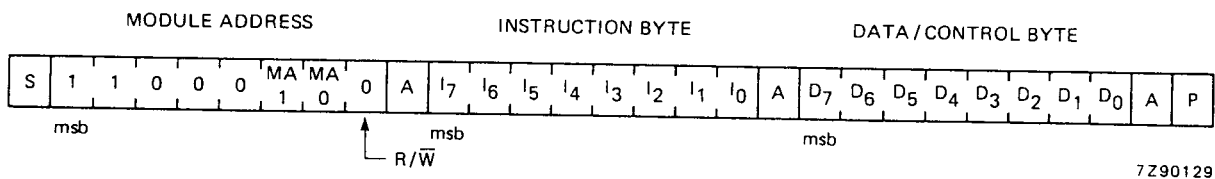


Fig. 3 I²C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

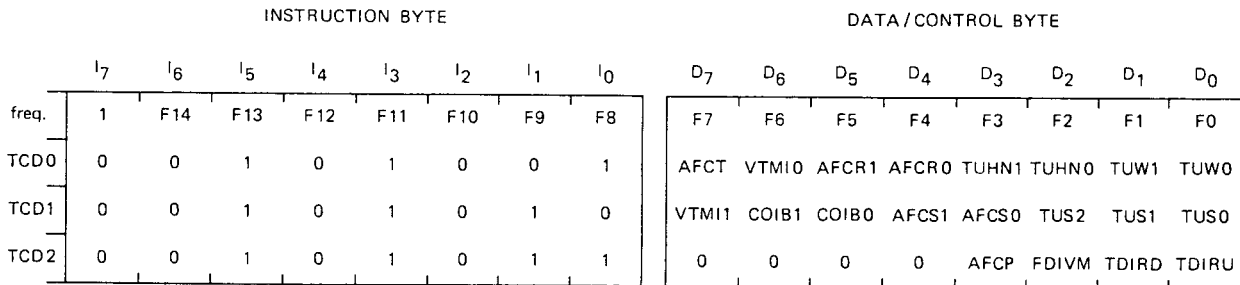


Fig. 4 Tuning control format.

7290125

Frequency

Frequency is set when bit I₇ of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I _{max} μA	typ. IT _{min} μA μs	typ. ΔVTUN _{min} at C _{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected. After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS $\Delta f = 50$ kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{\min} mA μ s	typ. $\Delta V_{TUN\min}$ at $C_{INT} = 1 \mu F$ mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$ \Delta f $ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCH (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCH1	AFCH0	$ \Delta f $ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance ($\mu A/V$)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFPC is at logic 0 (value after reset). At AFPC = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 Band select outputs. If a logic 1 is programmed on any of the POD bits D₃ to D₀, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D₇ to D₄, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

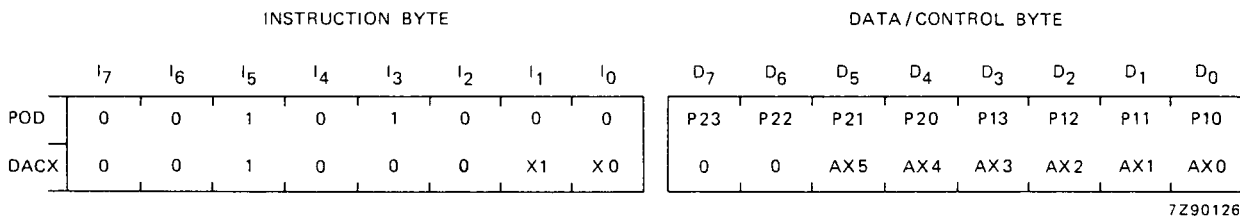


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/W bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

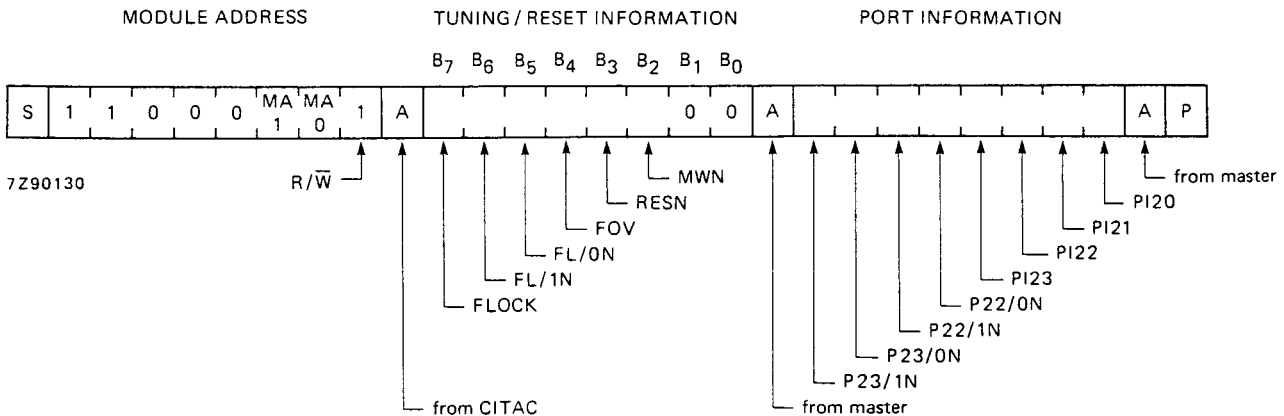


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

- FLOCK** Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
- FL/1N** Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
- FL/0N** As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
- FOV** Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
- RESN** Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
- MWN** MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured.

When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

- P23/1N, P22/1N** Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
- P23/0N, P22/0N** As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
- PI23, PI22, PI21, PI20** Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

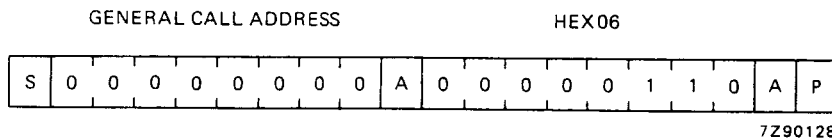


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:

(pin 13)	V_{P1}	-0,3 to +18 V
(pin 19)	V_{P2}	-0,3 to +18 V
(pin 14)	V_{P3}	-0,3 to +36 V

Input/output voltage ranges:

(pin 2)	V_{SDA}	-0,3 to +18 V
(pin 3)	V_{SCL}	-0,3 to +18 V
(pins 4 to 7)	V_{P2X}	-0,3 to +18 V
(pins 8 and 9)	$V_{AFC+}, AFC-$	-0,3 to V_{P1}^* V
(pin 10)	V_{TI}	-0,3 to V_{P1}^* V
(pin 12)	V_{TUN}	-0,3 to V_{P3}^* V
(pins 15 to 18)	V_{P1X}	-0,3 to V_{P2}^{**} V
(pin 20)	V_{FDIV}	-0,3 to V_{P1}^* V
(pin 21)	V_{OSC}	-0,3 to +5 V
(pins 1 and 22 to 24)	V_{DACX}	-0,3 to V_{P1}^* V

Total power dissipation

 P_{tot} max. 1000 mW

Storage temperature range

 T_{stg} -55 to +125 °C

Operating ambient temperature range

 T_{amb} -20 to +70 °C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$; V_{P1} , V_{P2} , V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	18	30	45	mA
	I_{P2}	0	—	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A) (note 1)	I_{P2A}	-2	—	I_{OHP1X}	mA
	I_{P3A}	0,2	—	2	mA
Total power dissipation	P_{tot}	—	380	—	mW
Operating ambient temperature	T_{amb}	-20	—	+70	$^{\circ}\text{C}$
I²C bus inputs/outputs					
SDA input (pin 2); SCL input (pin 3)					
Input voltage HIGH (note 2)	V_{IH}	3	—	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	-0,3	—	1,5	V
Input current HIGH (note 2)	I_{IH}	—	—	10	μA
Input current LOW (note 2)	I_{IL}	—	—	10	μA
SDA output (pin 2, open collector)					
Output voltage LOW at $I_{OL} = 3\text{ mA}$	V_{OL}	—	—	0,4	V
Maximum output sink current	I_{OL}	—	5	—	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 4 to 7, open collector)					
Input voltage HIGH	V_{IH}	2	—	16	V
Input voltage LOW	V_{IL}	-0,3	—	0,8	V
Input current HIGH	I_{IH}	—	—	25	μA
Input current LOW	$-I_{IL}$	—	—	25	μA
Output voltage LOW at $I_{OL} = 2\text{ mA}$	V_{OL}	—	—	0,4	V
Maximum output sink current	I_{OL}	—	4	—	mA

parameter	symbol	min.	typ.	max.	unit	
A.F.C. amplifier						
Inputs AFC+, AFC- (pins 8, 9)						
Transconductance for input voltages up to 1 V differential:						
AFCS1	AFCS2					
0	0	900	100	250	800	nA/V
0	1	901	15	25	35	μ A/V
1	0	910	30	50	70	μ A/V
1	1	911	60	100	140	μ A/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used						
	ΔM_g	-20	-	+20		%
Input offset voltage						
	V_{Ioff}	-75	-	+75		mV
Common mode input voltage						
	V_{com}	3	-	$V_{P1-2,5}$		V
Common mode rejection ratio						
	CMRR	-	50	-		dB
Power supply (V_{P1}) rejection ratio						
	PSRR	-	50	-		dB
Input current						
	I_I	-	-	500		nA
Tuning voltage amplifier						
Input TI, output TUN (pins 10, 12)						
Maximum output voltage at $I_{load} = \pm 1,5$ mA						
	V_{TUN}	$V_{P3-1,6}$	-	$V_{P3-0,4}$		V
Minimum output voltage at $I_{load} = \pm 1,5$ mA:						
VTM11	VTM10					
0	0	V_{TM00}	300	-	500	mV
1	0	V_{TM10}	450	-	650	mV
1	1	V_{TM11}	650	-	900	mV
Maximum output source current						
	$-I_{TUNH}$	2,5	-	8		mA
Maximum output sink current						
	I_{TUNL}	-	40	-		mA
Input bias current						
	I_{TI}	-5	-	+5		nA
Power supply (V_{P3}) rejection ratio						
	PSRR	-	60	-		dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit	
Tuning voltage amplifier (continued)						
Minimum charge I_T to tuning voltage amplifier						
TUHN1	TUHN0					
0	0	CH00	0,4	1	1,7	$\mu A \mu s$
0	1	CH01	4	8	14	$\mu A \mu s$
1	0	CH10	15	30	48	$\mu A \mu s$
1	1	CH11	130	250	370	$\mu A \mu s$
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used						
		ΔCH	-20	-	+20	%
Maximum current i into tuning amplifier						
TUHN1	TUHN0					
0	0	I_{T00}	1,7	3,5	5,1	μA
0	1	I_{T01}	15	29	41	μA
1	0	I_{T10}	65	110	160	μA
1	1	I_{T11}	530	875	1220	μA
Correction-in-band						
Tolerance of correction-in-band levels 12 V, 18 V and 24 V						
		ΔV_{CIB}	-15	-	+15	%
Band-select output ports						
P10, P11, P12, P13 (pins 15 to 18)						
Output voltage HIGH at $-I_{OH} = 50 \text{ mA}$ (note 3)						
		V_{OH}	$V_{P2}-0,6$	-	-	V
Output voltage LOW at $I_{OL} = 2 \text{ mA}$						
		V_{OL}	-	-	0,4	V
Maximum output source current (note 3)						
		$-I_{OH}$	-	130	200	mA
Maximum output sink current						
		I_{OL}	-	5	-	mA
FDIV input (pin 20)						
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leq 40 \text{ ns}$)						
		$V_{FDIV(p-p)}$	0,1	-	2	V
Duty cycle						
		-	40	-	60	%
Maximum input frequency						
		f_{max}	14,5	-	-	MHz
Input impedance						
		Z_i	-	8	-	$k\Omega$
Input capacitance						
		C_i	-	5	-	pF

parameter	symbol	min.	typ.	max.	unit	
OSC input (pin 21)						
Crystal resistance at resonance (4 MHz)	R_X	—	—	150	Ω	
DAC outputs 0 to 3 (pins 22 to 24 and pin 1)						
Maximum output voltage (no load) at $V_{P1} = 12$ V (note 4)	V_{DH}	10	—	11,5	V	
Minimum output voltage (no load) at $V_{P1} = 12$ V (note 4)	V_{DL}	0,1	—	1	V	
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	—	350	mV	
Deviation from linearity	—	—	—	0,5	V	
Output impedance at $I_{load} = \pm 2$ mA	Z_o	—	—	70	Ω	
Maximum output source current	$-I_{DH}$	—	—	6	mA	
Maximum output sink current	I_{DL}	—	8	—	mA	
Power-down-reset						
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	—	9,5	V	
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	—	—	μs	
Voltage level for valid module address						
Voltage level at P20 (pin 4) for valid module address as a function of MA1, MA0						
MA1	MA0					
0	0	V_{VA00}	-0,3	—	16	V
0	1	V_{VA01}	-0,3	—	0,8	V
1	0	V_{VA10}	2,5	—	$V_{P1}-2$	V
1	1	V_{VA11}	$V_{P1}-0,3$	—	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X} , the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1} .

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:

4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t _{BUF}	4	—	—	μs
Start condition set-up time	t _{SU,STA}	4	—	—	μs
Start condition hold time	t _{HD,STA}	4	—	—	μs
SCL, SDA LOW period	t _{LOW}	4	—	—	μs
SCL HIGH period	t _{HIGH}	4	—	—	μs
SCL, SDA rise time	t _R	—	—	1	μs
SCL, SDA fall time	t _F	—	—	0,3	μs
Data set-up time (write)	t _{SU,DAT}	1	—	—	μs
Data hold time (write)	t _{HD,DAT}	1	—	—	μs
Acknowledge (from CITAC) set-up time	t _{SU,CAC}	—	—	2	μs
Acknowledge (from CITAC) hold time	t _{HD,CAC}	0	—	—	μs
Stop condition set-up time	t _{SU,STO}	4	—	—	μs
Data set-up time (read)	t _{SU,RDA}	—	—	2	μs
Data hold time (read)	t _{HD,RDA}	0	—	—	μs
Acknowledge (from master) set-up time	t _{SU,MAC}	1	—	—	μs
Acknowledge (from master) hold time	t _{HD,MAC}	2	—	—	μs

Note

Timings t_{SU,DAT} and t_{HD,DAT} deviate from the I²C bus specification .

After reset has been activated, transmission may only be started after a 50 μs delay.

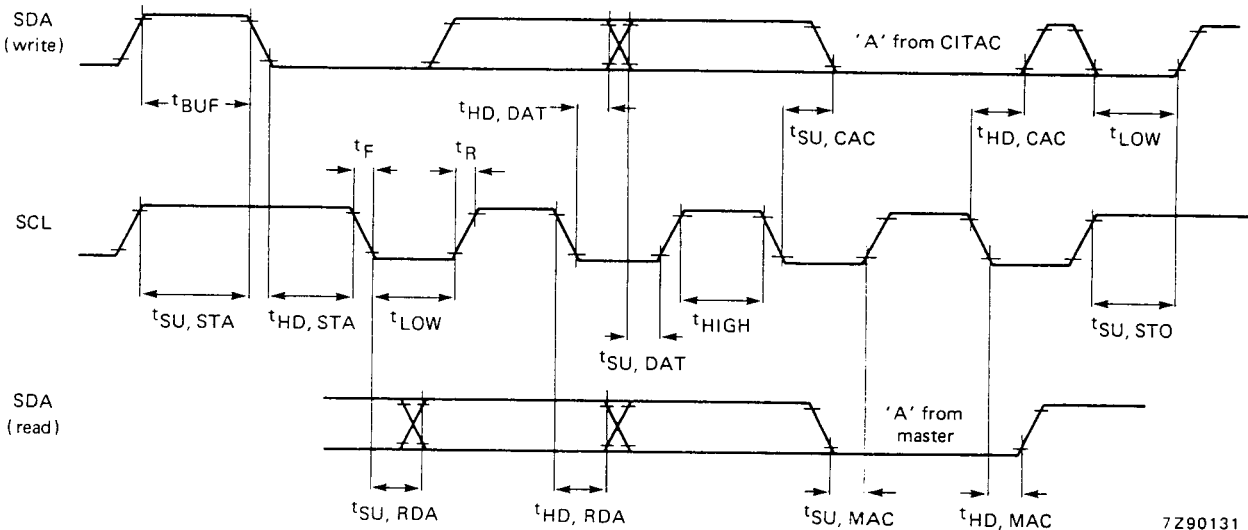


Fig. 8 I²C bus timing SAB3037.