8-Bit Single-Chip Microcontroller

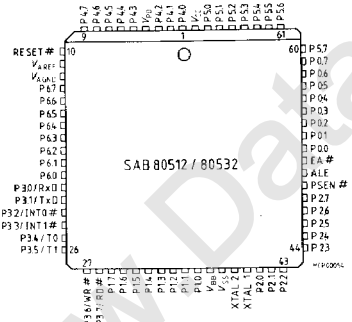
SAB 80512/80532

Obsolescent Type

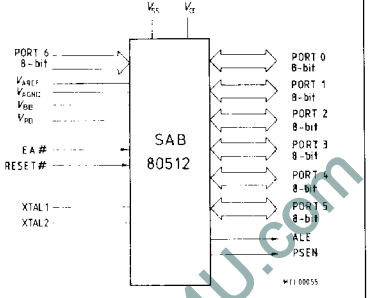
SAB 80512-N	Microcontroller with factory-maskprogrammable ROM
SAB 80532-N	Microcontroller for external ROM

- 4 K × 8 ROM (SAB 80512 only)
- 128 × 8 RAM
- Full backward compatibility to SAB 8051A/8031A
- Seven 8-bit ports
- Two 16-bit timers/event counters
- High performance full duplex serial channel with own baud rate generator
- 8-bit A/D converter with eight multiplexed inputs, reference voltages externally adjustable
- Six interrupt sources (2 external, 4 internal), two priority levels programmable
- Boolean processor
- 1 µs instruction cycle time (at 12 MHz osc. frequency)
- 4 µs multiply and divide (at 12 MHz osc. frequency)
- External program and data memory expandable up to 64 Kbyte each
- PL-CC-68 package

Pin Configurations



Logic Symbol



The SAB 80512/80532 is a new member of the Siemens SAB 8051 family of 8-bit microcontrollers. Maintaining all features of the SAB 8051A/8031A, it is fully backward compatible to the SAB 8051A/8031A. Furthermore the SAB 80512/80532 incorporates several enhancements that significantly increase design flexibility and cost effectiveness. Compared to the SAB 8051A/8031A the SAB 80512/ 80532 additionally contains an 8-bit A/D converter with 8 multiplexed inputs (these inputs can also be used as digital inputs), an own baud rate generator for the serial interface and two more I/O ports.The SAB 80532 is identical with the SAB 80512, except that it lacks the on-chip ROM.
The SAB 80512/80532 is fabricated in + 5 V advanced N-channel, silicon gate MYMOS technology of Siemens and supplied in a PL-CC-68 package. For the industrial temperature range – 40 to + 85°C, the SAB 80512/80532-T40/85 is available.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors.
V_{PD}	4	–	Power down supply voltage. If V_{PD} is held within its specifications while V_{CC} drops below the specification, V_{PD} will providestandby power to 40 byte of internal RAM (addr. 58H to 7FH).During normal operation of the SAB 80512, the RAM's current is supplied by V_{CC}, when V_{PD} is low.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80512. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11	–	Reference voltage for the A/D converter
V_{AGND}	12	–	Reference ground for the A/D converter
P6.7-P6.0	13-20	I	Port 6, 8-bit unidirectional input port. Port pins can be used for digital input if voltage levels meet the specified input high/low voltages and for the eight multiplexed analog inputs of the A/D converter, simultaneously.
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 3 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input/timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input/timer 1 gate control – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0

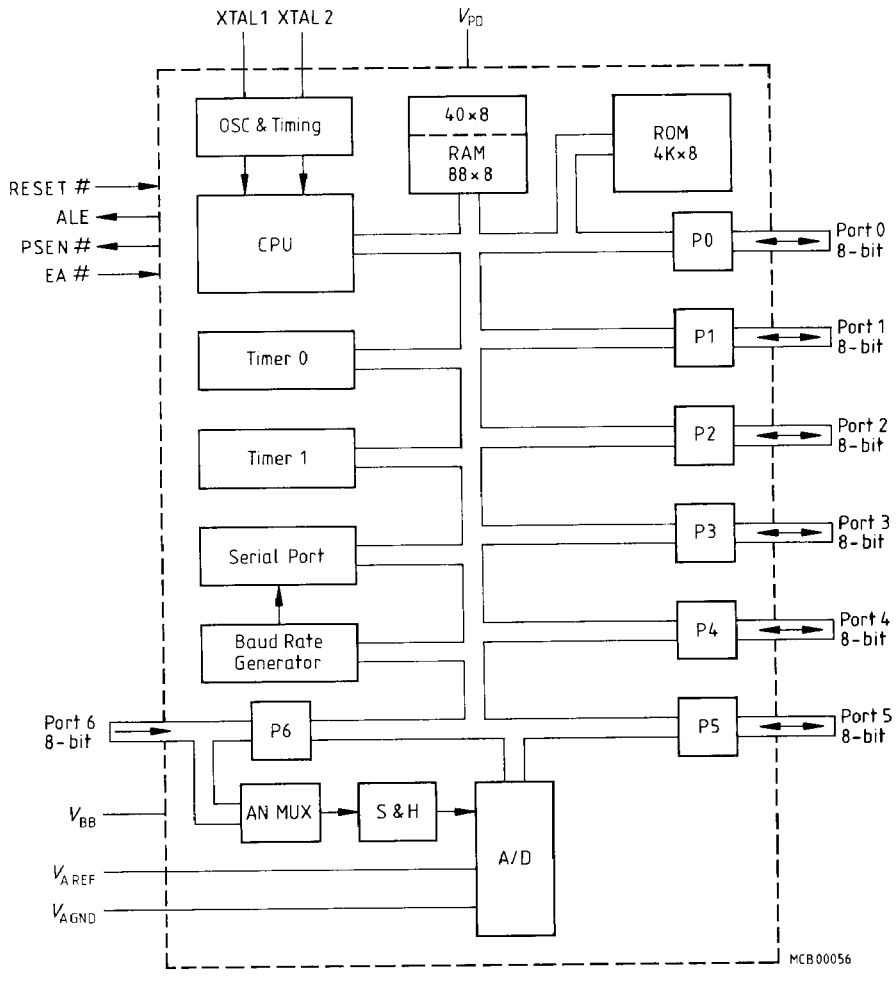
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0	29-36	I/O	Port 1 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 1 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. The port is also used for the low order address byte during program verification.
V_{BB}	37	–	Substrate pin. Must be connected to V_{SS} with a capacitor (100 nF to 1000 nF) for proper operation of the A/D converter.
XTAL2 XTAL1	39 40	– –	XTAL2 Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is pulled low. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed: XTAL1 Input to the inverting oscillator amplifier. Required when a crystal or ceramic resonator is used.
P2.0-P2.7	41-48	I/O	Port 2 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 2 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{EA}$	51	I	When held at a TTL high level, the SAB 80512 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 80512 fetches all instructions from external program memory. For the SAB 80532 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification. External pullup resistors are required during program verification.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 5 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors.
V_{CC}	68	–	Supply voltage during normal operation and program verification.
V_{SS}	38	–	Ground (0 V)

Block Diagram



Functional Description

The SAB 80512/80532 is based on the architecture of the SAB 8051 microcontroller family. The SAB 80512 includes all features of the SAB 8051 and additionally offers peripheral extensions in three items:

- bit A/D converter with adjustable reference voltage
- two more ports
- dedicated baud rate generator

Different to the SAB 8051 is the inverted reset-input and the RAM power-down supply by a special pin (V_{PD}), which supplies 40 byte with a typical current of 2 mA. Beside the backward compatibility to the SAB 8051 (all SAB 8051 software runs on the SAB 80512 without any changes) the SAB 80512 is also upwardly compatible to the SAB 80515. The SAB 80512 is packed into the PL-CC-68 package and has got the same pinning as the SAB 80515.

A/D Converter

The 8-bit A/D converter of the SAB 80512 has 8 multiplexed analog inputs and uses the successive approximation method. The sampling of an analog signal takes 5 machine cycles, the total conversion time is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous, at the end of a conversion an interrupt can be generated. The SAB 80512 provides variable external reference voltages V_{AGND} and V_{AREF} adjustable in a wide range. A compressed reference voltage range allows to increase the resolution of the converted analog input. The lower reference voltage (V_{AGND}) can be varied within V_{SS} – 0.2 V and 4 V, the higher (V_{AREF}) within 1 V and V_{CC} + 5%. For proper operation of the A/D converter a minimum of 1 V difference is required between the external voltages:

$(V_{SS} - 0.2\ V) \leq V_{AGND} \leq (V_{AREF} - 1\ V)$

$(V_{AGND} + 1\ V) \leq V_{AREF} \leq (V_{CC} + 5\%)$

Special Function Register

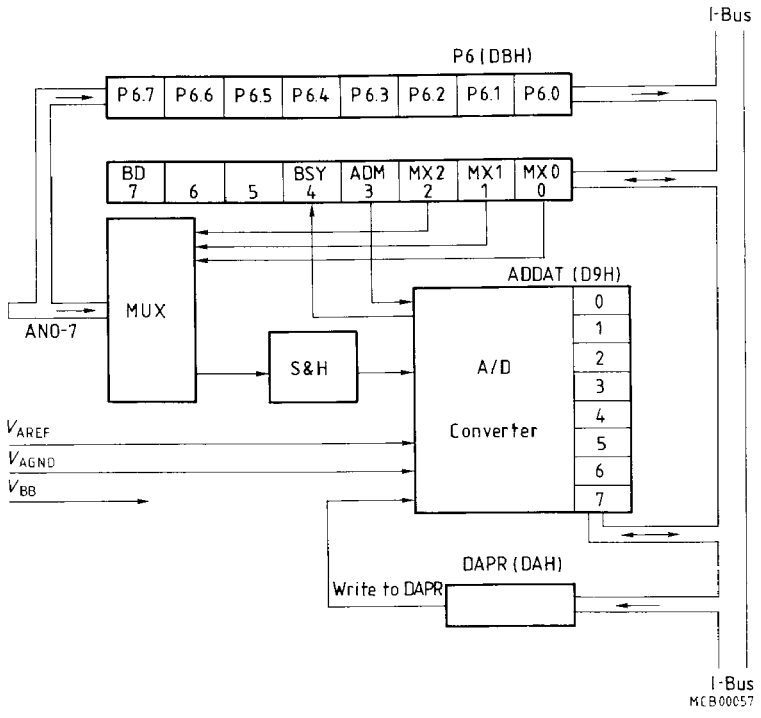
All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 28 special function registers (SFRs) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area

I/O Ports

The SAB 80512 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullups. That means, when configured as inputs, ports 1 to 5 will pull high and will source current when externally pulled low. Port 0 will float when configured as input. Port 6 is an input port only and can be used as digital input port, if the values meet the specified high/low voltages and as analog input for the A/D-converter.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

Block Diagram of A/D Converter



Special Function Registers

Address	Symbol	Name	bit-addressable
80H	P0	Port 0 Register	yes
81H	SP	Stack Pointer	–
82H	DPL	Data Pointer, low-byte	–
83H	DPH	Data Pointer, high-byte	–
87H	PCON	Power Control Register	–
88H	TCON	Timer Control Register	yes
89H	TMOD	Timer Mode Register	–
8AH	TL0	Timer 0, low-byte	–
8BH	TL1	Timer 1, low-byte	–
8CH	TH0	Timer 0, high-byte	–
8DH	TH1	Timer 1, high-byte	–
90H	P1	Port 1 Register	yes
98H	SCON	Serial Port Control Register	yes
99H	SBUF	Serial Port Buffer Register	–
0A0H	P2	Port 2 Register	yes
0A8H	IE	Interrupt Enable Register	yes
0B0H	P3	Port 3 Register	yes
0B8H	IP	Interrupt Priority Register	yes
0C0H	IRCON	Interrupt Request Control	yes
0D0H	PSW	Program Status Word Register	yes
0D8H	ADCON	A/D Converter Control Register	yes
0D9H	ADDAT	A/D Converter Data Register	–
0DAH	DAPR	D/A Converter Start Register	–
0DBH	P6	Port 6 Register	–
0E0H	ACC	Accumulator Register	yes
0E8H	P4	Port 4 Register	yes
0F0H	B	B-Register	yes
0F8H	P5	Port 5 Register	yes

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	1
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct, A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct, A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Data transfer

MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

Boolean variable manipulation

CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn	–	Working register R0-R7
direct	–	128 internal RAM locations, any I/O port, control or status register
@Ri	–	Indirect internal or external RAM location addressed by register R0 or R1
#data	–	8-bit constant included in instruction
#data 16	–	16-bit constant included as bytes 2 and 3 of instruction
bit	–	128 software flags, any I/O pin, control or status bit
A	–	Accumulator

Notes on program addressing modes:

addr 16	–	Destination address for LCALL and LJMP may be anywhere within the 64-Kbyte program memory address space.
addr 11	–	Destination address for ACALL and AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.
rel	–	SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	addr. 11
02	3	LJMP	addr. 16
03	1	RR	A
04	1	INC	A
05	2	INC	direct
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit,rel*
11	2	ACALL	addr. 11
12	3	LCALL	addr. 16
13	1	RRC	A
14	1	DEC	A
15	2	DEC	direct
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit,rel*
21	2	AJMP	addr. 11
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,direct
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit,rel*
31	2	ACALL	addr. 11
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#data
35	2	ADDC	A,direct
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	*rel*
41	2	AJMP	addr. 11
42	2	ORL	direct,A
43	3	ORL	direct,#data
44	2	ORL	A,#data
45	2	ORL	A,direct
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*rel*
51	2	ACALL	addr. 11
52	2	ANL	direct,A
53	3	ANL	direct,#data
54	2	ANL	A,#data
55	2	ANL	A,direct
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*rel*
61	2	AJMP	addr. 11
62	2	XRL	direct,A
63	3	XRL	direct,#data
64	2	XRL	A,#data
65	2	XRL	A,direct
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*rel*
71	2	ACALL	*addr. 11*
72	2	ORL	C,*bit*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*direct*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*rel*
81	2	AJMP	*addr. 11*
82	2	ANL	C,*bit*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*direct, direct*
86	2	MOV	*direct*,@R0
87	2	MOV	*direct*,@R1
88	2	MOV	*direct*,R0
89	2	MOV	*direct*,R1
8A	2	MOV	*direct*,R2
8B	2	MOV	*direct*,R3
8C	2	MOV	*direct*,R4
8D	2	MOV	*direct*,R5
8E	2	MOV	*direct*,R6
8F	2	MOV	*direct*,R7
90	3	MOV	DPTR,#*data 16*
91	2	ACALL	*addr. 11*
92	2	MOV	*bit*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*direct*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	A,*bit* #
A1	2	AJMP	*addr. 11*
A2	2	MOV	C,*bit*
A3	1	INC	DPTR
A4	1	MUL	AB
A5	2	reserved	
A6	2	MOV	@R0,*direct*
A7	2	MOV	@R1,*direct*
A8	2	MOV	R0,*direct*
A9	2	MOV	R1,*direct*
AA	2	MOV	R2,*direct*
AB	2	MOV	R3,*direct*
AC	2	MOV	R4,*direct*
AD	2	MOV	R5,*direct*
AE	2	MOV	R6,*direct*
AF	2	MOV	R7,*direct*
B0	2	ANL	C,/*bit*
B1	2	ACALL	*addr. 11*
B2	2	CPL	*bit*
B3	1	CPL	C
B4	3	CJNE	A,#*data,rel*
B5	3	CJNE	A,*direct,rel*
B6	3	CJNE	@R0,#*data,rel*
B7	3	CJNE	@R1,#*data,rel*
B8	3	CJNE	R0,#*data,rel*
B9	3	CJNE	R1,#*data,rel*
BA	3	CJNE	R2,#*data,rel*
BB	3	CJNE	R3,#*data,rel*
BC	3	CJNE	R4,#*data,rel*
BD	3	CJNE	R5,#*data,rel*
BE	3	CJNE	R6,#*data,rel*
BF	3	CJNE	R7,#*data,rel*
C0	2	PUSH	*direct*
C1	2	AJMP	*addr. 11*
C2	2	CLR	*bit*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*direct*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*direct*
D1	2	ACALL	*addr. 11*
D2	2	SETB	*bit*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*direct,rel*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*rel*
D9	2	DJNZ	R1,*rel*
DA	2	DJNZ	R2,*rel*
DB	2	DJNZ	R3,*rel*
DC	2	DJNZ	R4,*rel*
DD	2	DJNZ	R5,*rel*
DE	2	DJNZ	R6,*rel*
DF	2	DJNZ	R7,*rel*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*addr. 11*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*direct**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*addr. 11*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*direct,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Temperature under bias	0 to + 70°C for the SAB 80512/80532
	– 40 to + 85°C for the SAB 80512/80532-T40/85
storage temperature	– 65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ±10%; V_{SS} = 0 V;
T_A = 0 to 70°C; for SAB 80512/80532
T_A = – 40 to + 85°C for SAB 80512/80532-T40/85

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except $\overline{\text{RESET}}$ and XTAL2)	2.0	V_{CC} + 0,5	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to $\overline{\text{RESET}}$	3.0	–	V	–
V_{PD}	Power-down voltage	3	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage, port 0, ALE, $\overline{\text{PSEN}}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	I_{IOH} = – 80 µA
V_{OH1}	Output high voltage, port 0, ALE, $\overline{\text{PSEN}}$	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logic 0 input current, XTAL2	–	– 2.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IL3}	Input low current to $\overline{\text{RESET}}$ for reset	–	– 500	µA	V_{IL} = 0.45 V
I_{LI}	Input leakage current to port 0, $\overline{\text{EA}}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 80512/80532 SAB 80512/80532-T40/85	–	175	mA	all outputs disconnected
I_{PD}	Power-down current	–	3	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

A/D Converter Characteristics

V_{CC} = 5 V ±10%; V_{SS} = 0 V;
(V_{SS} – 0.2 V) ≤ V_{AGND} ≤ (V_{AREF} – 1 V); (V_{AGND} +1 V) ≤ V_{AREF} ≤ (V_{CC} +5%);
T_A = 0 to 70°C for SAB 80512/80532
T_A = – 40 to + 85°C for SAB 80512/80532-T40/85

Symbol	Parameter	Limit Values			Unit	Test condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	V_{AGND} – 0.2	–	V_{AREF} + 0.2	V	–
C_I	Analog input capacitance	–	25	70	pF	1)
t_L	Load time	–	–	2 t_{CY}	µs	
t_S	Sample time (incl. load time)	–	–	5 t_{CY}	µs	
t_C	Conversion time (incl. sample time)	–	–	15 t_{CY}	µs	
DNLE	Differential non-linearity	–	± 1/4	± 1/2	LSB	V_{AREF} = V_{CC} V_{AGND} = V_{SS}
INLE	Integral non-linearity	–	± 1/4	± 1/2		
	Offset error	–	± 1/4	± 1/2		
	Gain error	–	± 1/4	± 1/2		
TUE	Total unadjusted error	–	± 1	± 1/2		1) 2)
I_{REF}	V_{AREF} supply current	–	–	5	mA	2)

1) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

2) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V
T_A = 0 to 70°C for SAB 80512/80532
T_A = – 40 to + 85°C for SAB 80512/80532-T40/85
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock 1/ t_{CLCL} = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	12 t_{CLCL}	–	ns
t_{LHLL}	ALE pulse width	127	–	2 t_{CLCL} – 40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL} – 30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL} – 35	–	ns
t_{LLIV}	Address to valid instr in	–	233	–	4 t_{CLCL} – 100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL} – 25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	3 t_{CLCL} – 35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instr in	–	150	–	3 t_{CLCL} – 100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL} – 20	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	75	–	t_{CLCL} – 8	–	ns
t_{AVIV}	Address to valid instr in	–	302	–	5 t_{CLCL} – 115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 80512 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

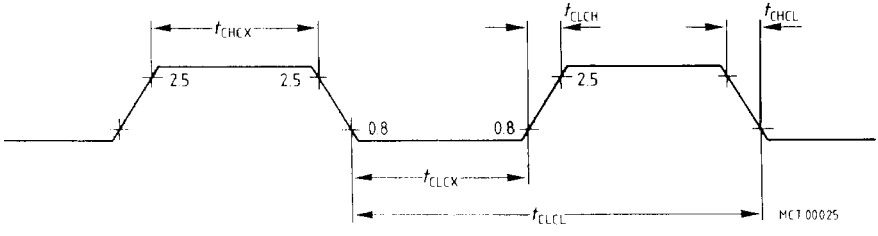
External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock 1/ t_{TCLCL} = 1.2 MHz to 12		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{WHLH}	$\overline{WR}$ pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	2 t_{CLCL} – 35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	250	–	5 t_{CLCL} – 165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	2 t_{CLCL} – 70	ns
t_{LLDV}	ALE to valid data in	–	517	–	8 t_{CLCL} – 150	ns
t_{AVDV}	Address to valid data in	–	585	–	9 t_{CLCL} – 165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	4 t_{CLCL} – 130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL} – 50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	7 t_{CLCL} – 150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL} – 50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

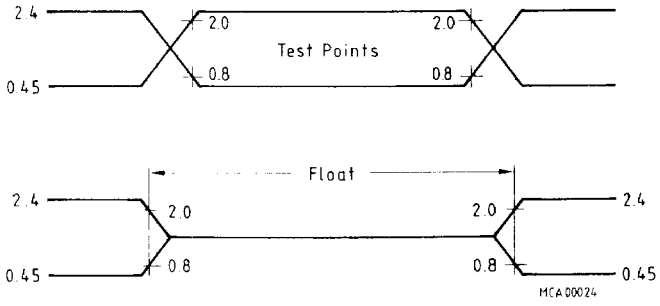
External Clock Drive XTAL2

Symbol	Parameter	Limit Values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz		
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCK}	Low time	20	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

External Clock Cycle



AC Testing Input, Output, Float Waveforms



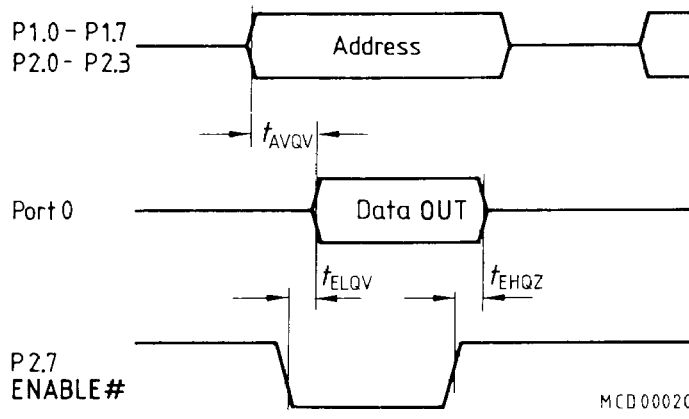
AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	ENABLE to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after ENABLE	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification

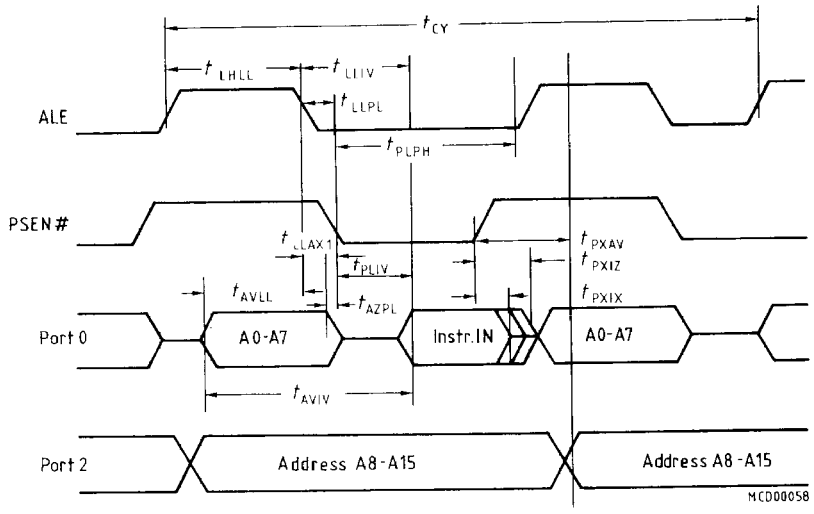


Data : P1.0-P1.7 = A0-A7
P2.0-P2.3 = A8-A11
Port 0 = D0-D7

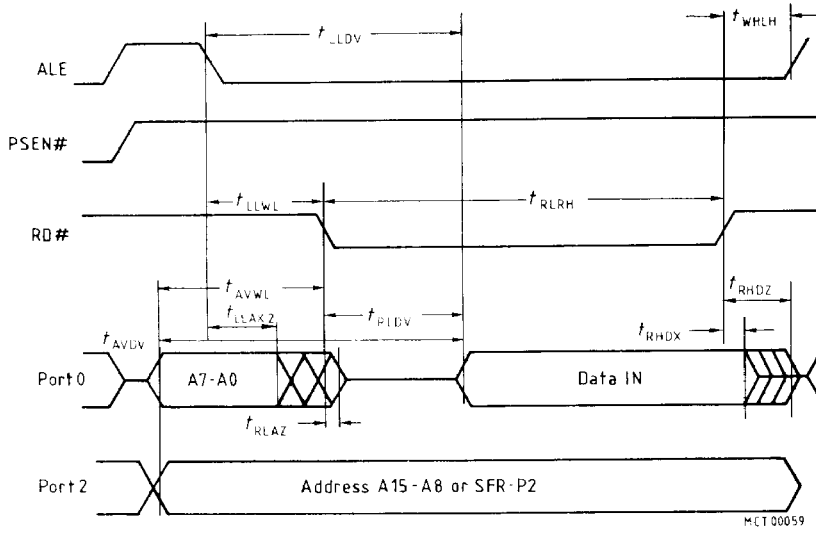
Inputs: P2.4-P2.6,$\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

Waveforms

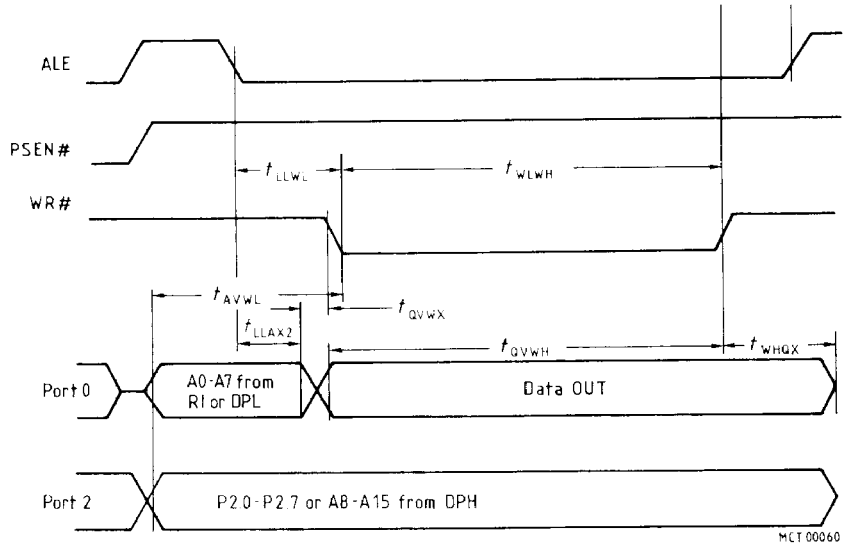
Program Memory Read Cycle



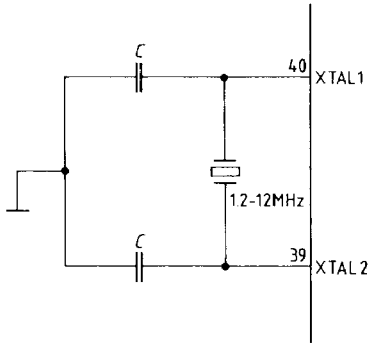
Data Memory Read Cycle



Program Memory Write Cycle

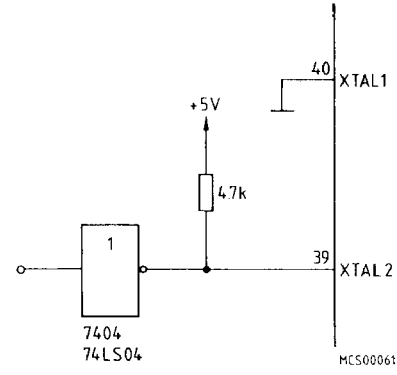


Recommended Oscillator Circuits



$C = 30pF \pm 10pF$

Crystal Oscillator Mode



Driving from External Source

Ordering Information

Type	Ordering code	Function
SAB 80512-N	Q67120-C336	8-bit single-chip microcontroller with ROM
SAB 80532-N	Q67120-C337	8-bit single-chip microcontroller for external ROM
SAB 80512-T40/85-N	Q67120-C353	like SAB 80512 but for – 40 to + 85 °C
SAB 80532-T40/85-N	Q67120-C354	like SAB 80532 but for – 40 to + 85 °C