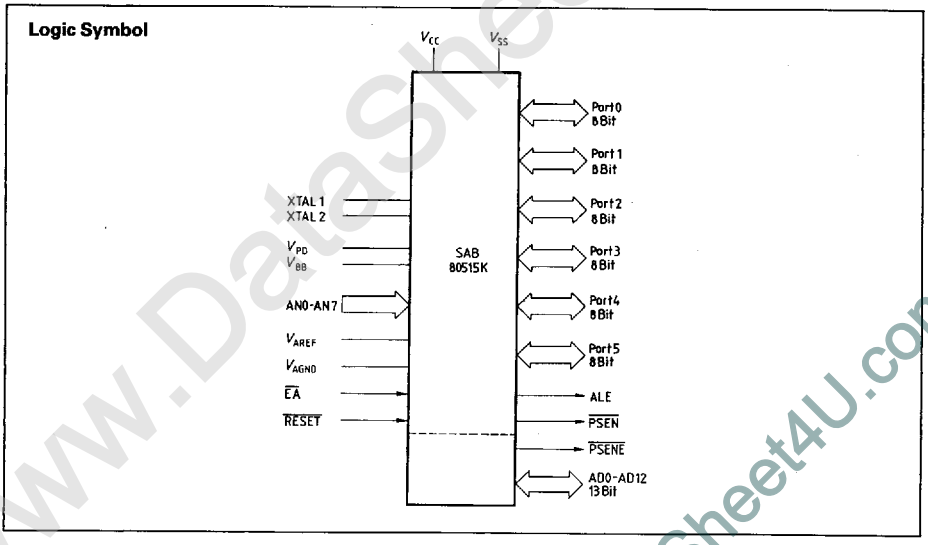
T-49-19-61

Preliminary

SAB 80515K
8-Bit Single-Chip Microcontroller
ROM-less Version

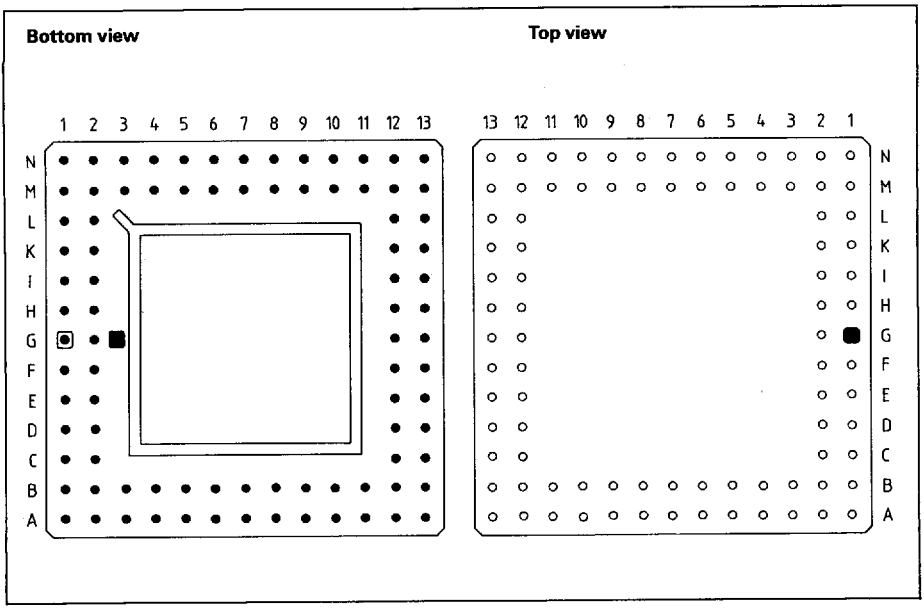
- Additional bus interface for external memory
- 256 × 8 RAM
- Six 8-bit ports
- Three 16-bit timer/event counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt sources, four priority levels
- 8-bit A/D converter with 8 multiplexed analog inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable to 128 Kbyte
- Pin grid array package, 88 pins (C-PGA-88)

Logic Symbol



The SAB 80515K is a special ROM-less version of the 8-bit microcontroller SAB 80515. The SAB 80515K contains an additional bus interface to connect an external program memory in place of the SAB 80515's on-chip ROM. Thereby, the SAB 80515K maintains the full I/O capability of the single-chip SAB 80515 while it permits connection of an external program memory. All other features of the SAB 80515K are identical with those of the SAB 80515.
The SAB 80515K is fabricated in +5 V advanced N-channel, silicon gate Siemens MYMOS technology, and supplied as pin grid array with 88 pins (C-PGA-88).

Pin Configuration



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12	J 13 J 12 K 13 K 12 L 13 M 13 L 12 N 13 N 8 M 7 N 7 M 6 N 6	I/O	Multiplexed address/data bus for the program memory. This bus is used for connecting an external memory in place of the 8-Kbyte internal ROM of the SAB 80515. Pins AD0 to AD12 can sink/source 5 LS-TTL loads.
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	A 8 B 8 A 7 B 7 A 6 B 6 A 5 B 5	I	Multiplexed analog inputs of the A/D converter.
P0.0 P0.1 P0.2 P0.3 P0.4 P0.5 P0.6 P0.7	N 1 M 2 L 2 M 1 K 2 L 1 K 1 J 2	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external program and data memory. Port 0 can sink/source 8 LS-TTL loads.
P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7	F 13 F 12 E 13 E 12 D 13 C 13 D 12 B 13	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). Port 1 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the port 1 pins, as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input/compare 0 output/ capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/compare 1 output/ capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/compare 2 output/ capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/compare 3 output/ capture 3 input – $\overline{\text{INT2}}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input.

T-49-19-61

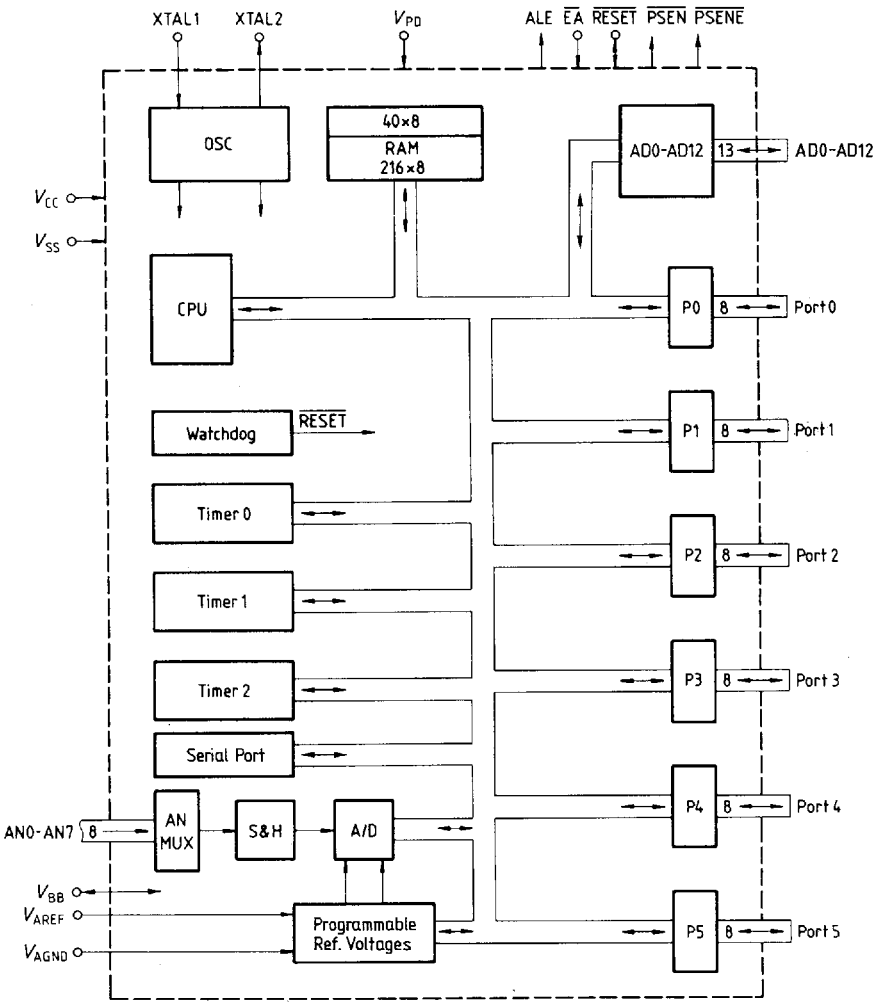
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	M 11 N 12 M 10 N 11 N 10 M 9 N 9 M 8	I/O	Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application, port 2 employs strong internal pullup resistors when issuing 1 s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register. Port 2 can sink/source 4 LS-TTL loads.
P3.0 P3.1 P3.2 P3.3 P3.4 P3.5 P3.6 P3.7	A 9 B 9 A 10 B 10 A 11 A 12 B 12 C 12	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{INT0}$ (P3.2): interrupt 0 input/timer 0 gate control input – $\overline{INT1}$ (P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0.
P4.0 P4.1 P4.2 P4.3 P4.4 P4.5 P4.6 P4.7	D 1 D 2 C 1 C 2 A 1 B 2 B 3 A 2	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source 4 LS-TTL loads.
P5.0 P5.1 P5.2 P5.3 P5.4 P5.5 P5.6 P5.7	E 1 F 1 F 2 G 1 G 2 H 1 H 2 J 1	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
XTAL2 XTAL1	H 12 H 13		XTAL2 Output of the inverting oscillator amplifier. To drive the device from en external clock source, XTAL2 should be driven, while XTAL1 is pulled low. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flipflop. Minimum and maximum high and low times specified in the AC characteristics must be observed. XTAL1 Input to the inverting oscillator amplifier. Required when a crystal or ceramic resonator is used.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{RESET}}$	B 4	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80515K. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
ALE	N 2	O	Provides ADDRESS LATCH ENABLE output used for latching the address into external memories at port 0 and 2, and AD0-AD12. It is activated every six oscillator periods except during external data memory accesses.
$\overline{\text{PSEN}}$	N 3	O	The PROGRAM STORE ENABLE output is a control signal that enables the external program memory at port 0 and 2 to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during program execution from program memory at AD0-AD12.
$\overline{\text{PSENE}}$	M 12	O	This output is a control signal that enables the program memory at AD0-AD12 during instruction fetch operations. It is activated every six oscillator periods.
$\overline{\text{EA}}$	M 3	I	When $\overline{\text{EA}}$ is held at a TTL high level, the SAB 80515K executes instructions from the program memory that is connected to AD0-AD12 when the PC is less than 8192. When $\overline{\text{EA}}$ is held at a TTL low level, the SAB 80515K executes all instructions from external program memory.
V_{AREF}	A 3		Reference voltage for the A/D converter
V_{AGND}	A 4		Reference ground for the A/D converter
V_{CC}	E 2		POWER SUPPLY (+5 V power supply during normal operation and program verification)
V_{SS}	G 13		GROUND (0 V)
V_{PD}	B 1		POWER DOWN SUPPLY. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 bytes of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
V_{BB}	G 12		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 1000 nF) for proper operation of the A/D converter.
NC	A 13 B 11 M 4 M 5 N 4 N 5		No connection.

Figure 1
Block Diagram



T-49-19-61

Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80515 with factory mask-programmable 8 Kbyte on-chip ROM
- SAB 80535 ROM-less version of the SAB 80515
- SAB 80515K ROM-less version of the SAB 80515 with additional bus interface.

In this data sheet the term "SAB 80515" is used to refer generally to all members of the SAB 80515 family, except where specifically stated otherwise.

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- instruction set
- external memory expansion interface (port 0 and port 2)
- full-duplex serial port
- timer/counters 0 and 1
- alternate functions on port 3
- the lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

Different to the SAB 8051 are the RAM power-down supply, which supplies 40 byte with a typical current of 2 mA, and the powerful interrupt structure with 12 sources and 4 priority levels.
The SAB 80515 additionally contains 128 byte of internal RAM and 4 Kbyte of internal ROM, that means a total of 256 byte RAM and 8 Kbyte ROM (SAB 80515 only) on-chip. The SAB 80515 has a 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with 8 analog inputs and programmable reference voltages, two additional quasi-bidirectional 8-bit ports, and a programmable clock output ($f_{osc}/12$).
The SAB 80515K is a special ROM-less version of the SAB 80515. In place of the 8 Kbyte on-chip ROM there is an additional bus interface for an 8 Kbyte program memory which can be connected externally.

Figure 2 shows a detailed block diagram of the SAB 80515K.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities of binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described below.

Program memory

The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbyte. If the $\overline{EA}$ pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this device.

The SAB 80515K has the same function as the SAB 80515; the difference is that fetches from the internal ROM are executed from a program memory via the additional bus interface (AD0-AD12).

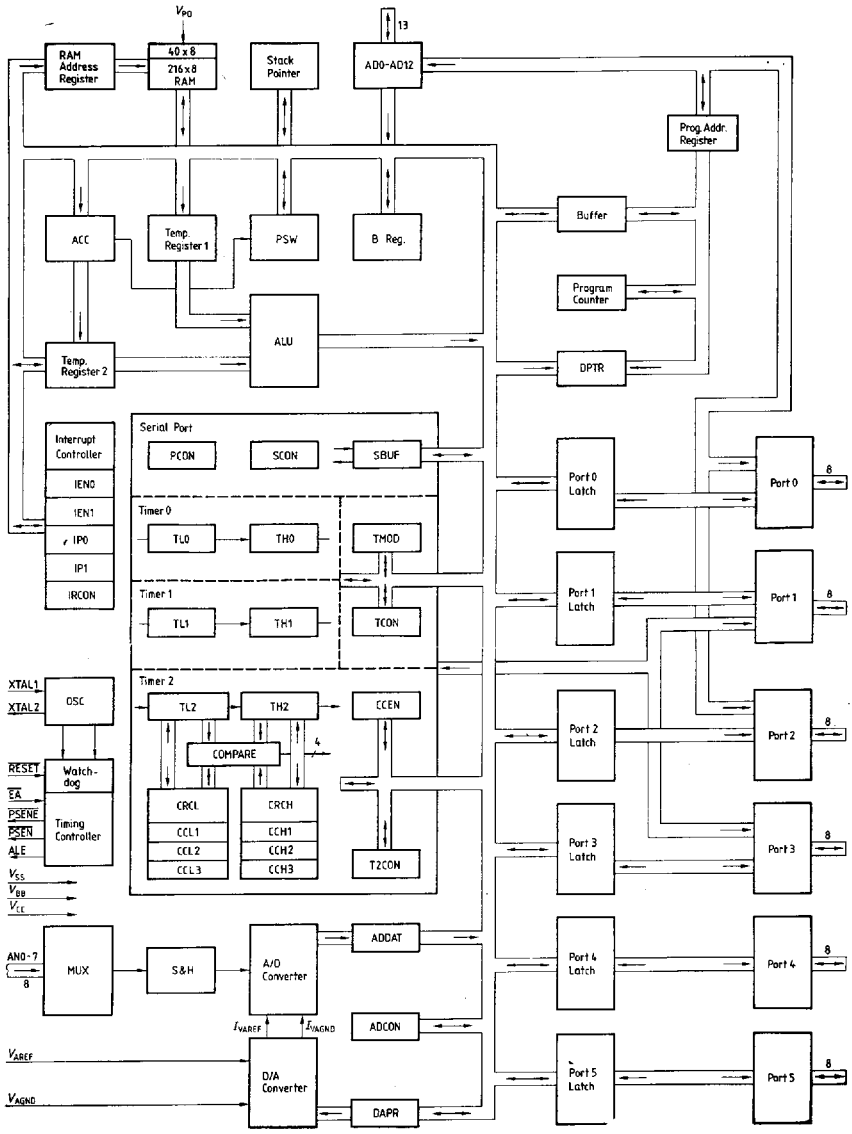
Data memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 byte of RAM; the upper 128 byte of RAM; and the 128-byte special function register (SFR) area. While the upper 128 byte of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 byte of data memory can be accessed through direct or register-indirect addressing; the upper 128 byte of RAM can be accessed through register-indirect addressing; and the special function registers are accessed through direct addressing.

Four 8-register banks occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depths can be expanded up to 256 byte.

The external data memory can be expanded up to 64 Kbyte and can be accessed by instructions that use a 16-bit or an 8-bit address.

Figure 2
Detailed Block Diagram

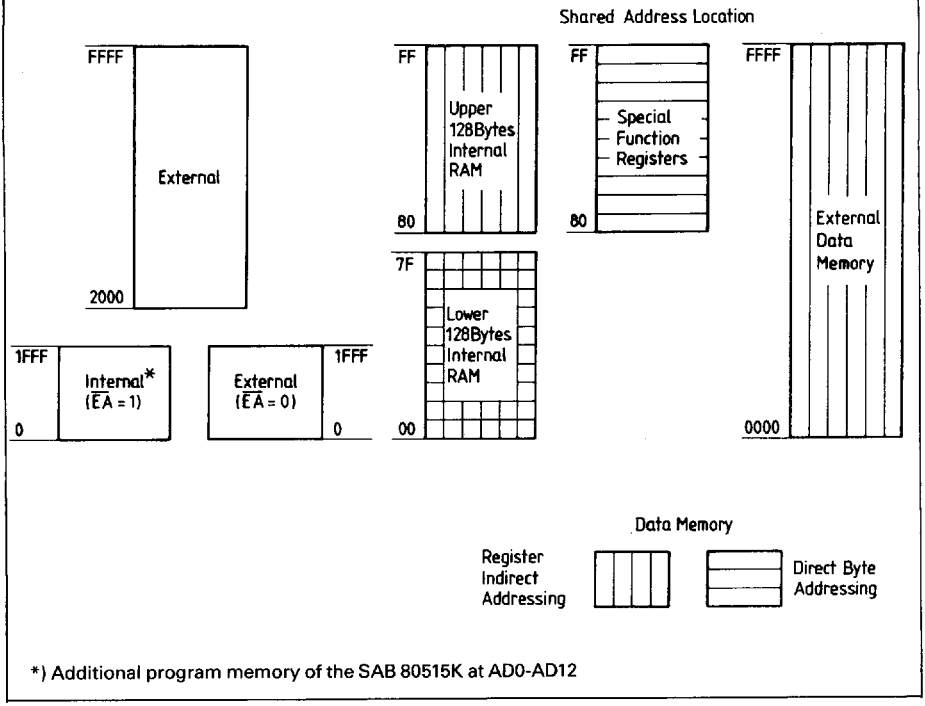


All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

Symbol	Name	Address
* P0	Port 0	80H
SP	Stack pointer	81H
DPL	Data pointer, low byte	82H
DPH	Data pointer, high byte	83H
PCON	Power control register	87H
* TCON	Timer control register	88H
TMOD	Timer mode register	89H
TL0	Timer 0, low byte	8AH
TL1	Timer 1, low byte	8BH
TH0	Timer 0, high byte	8CH
TH1	Timer 1, high byte	8DH
* P1	Port 1	90H
* SCON	Serial port control register	98H
SBUF	Serial port buffer register	99H
* P2	Port 2	0A0H
* IEN0	Interrupt enable register 0	0A8H
IP0	Interrupt priority register 0	0A9H
* P3	Port 3	0B0H
* IEN1	Interrupt enable register 1	0B8H
IP1	Interrupt priority register 1	0B9H
* IRCON	Interrupt request control register	0C0H
CCEN	Compare/capture enable register	0C1H
CCL1	Compare/capture register 1, low byte	0C2H
CCH1	Compare/capture register 1, high byte	0C3H
CCL2	Compare/capture register 2, low byte	0C4H
CCH2	Compare/capture register 2, high byte	0C5H
CCL3	Compare/capture register 3, low byte	0C6H
CCH3	Compare/capture register 3, high byte	0C7H
* T2CON	Timer 2 control register	0C8H
CRCL	Compare/reload/capture register, low byte	0CAH
CRCH	Compare/reload/capture register, high byte	0CBH
TL2	Timer 2, low byte	0CCH
TH2	Timer 2, high byte	0CDH
* PSW	Program status word register	0D0H
* ADCON	A/D converter control register	0D8H
ADDAT	A/D converter data register	0D9H
DAPR	D/A converter program register	0DAH
* ACC	Accumulator	0E0H
* P4	Port 4	0E8H
* B	B register	0F0H
* P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are both bit and byte-addressable.
Figure 3 illustrates the memory address spaces of the SAB 80515.

Figure 3
Memory Address Spaces



*) Additional program memory of the SAB 80515K at AD0-AD12

I/O Ports

The SAB 80515 has six 8-bit ports. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-ups. That means, when configured as inputs, ports 1 to 5 will pull high, and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

T-49-19-61

Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{INT3}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{INT2}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial input port
P3.1	TXD	Serial output port
P3.2	$\overline{INT0}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{INT1}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{WR}$	External data memory write strobe
P3.7	$\overline{RD}$	External data memory read strobe

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

–Timer/counters 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler
Mode 1: 16-bit timer/counter
Mode 2: 8-bit timer/counter with 8-bit auto-reload
Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

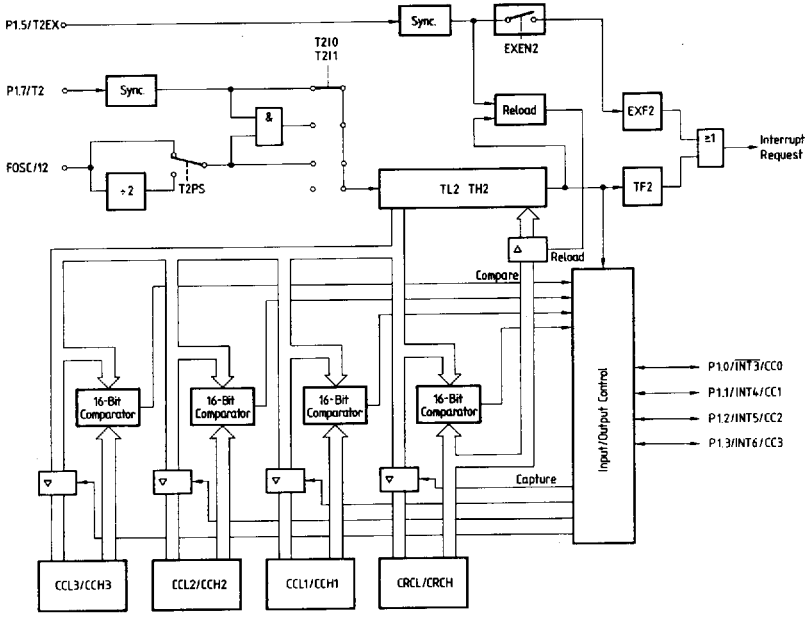
External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

–Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin on port 1 for capture input/compare output.

Figure 4 shows a block diagram of timer/counter 2.

Figure 4
Block Diagram of Timer/Counter 2



Reload

With the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH, a 16-bit reload can be performed. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Serial Port

The serial port of the SAB 80515 permits the full duplex communication between microcontrollers or between microcontrollers and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

The variable baud rates can be generated by timer 1 or an internal baud rate generator.

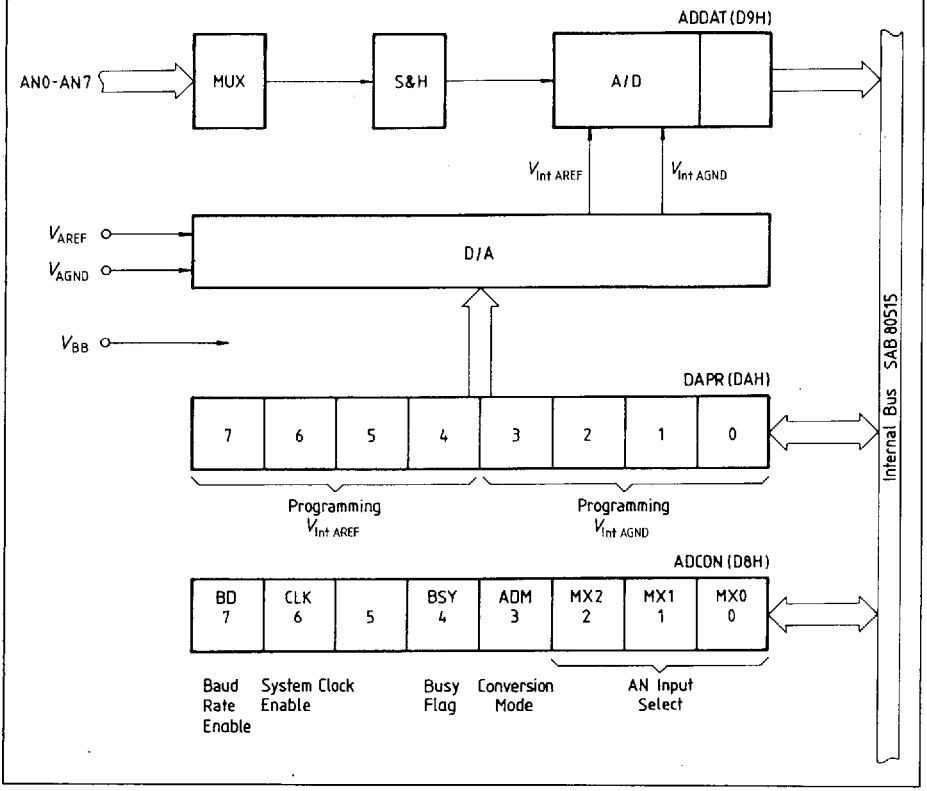
A/D Converter

The 8-bit A/D converter of the SAB 80515 has 8 multiplexed analog inputs and is using the successive approximation method. The sampling of an analog signal takes 5 machine cycles, the total conversion time is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous, at the end of a conversion an interrupt can be generated.

The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter are programmable in 16 steps with respect to the external reference voltages. This feature permits a second conversion with changed internal reference voltages to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog voltage range. Takes 7 machine cycles each (7 µs at 12 MHz oscillator frequency).

Figure 5 shows a block diagram of the A/D converter of the SAB 80515.

Figure 5
A/D Converter Block Diagram



Interrupt Structure

The 12 interrupt sources of the SAB 80515 are organized in 6 pairs:

External interrupt 0	–	A/D converter interrupt
Timer 0 interrupt	–	External interrupt 2
External interrupt 1	–	External interrupt 3
Timer 1 interrupt	–	External interrupt 4
Serial port interrupt	–	External interrupt 5
Timer 2 interrupt	–	External interrupt 6

Each interrupt source has its own vector address. It can be programmed to one of four priority levels and can individually be enabled/disabled. The minimum interrupt response time is 3 to 8 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed to be activated by a negative or a positive transition. The external interrupts 4 to 6 are activated by a positive transition. The interrupts 3 to 6 can be combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

Figure 6 shows the interrupt request sources, and figure 7 illustrates the priority level structure of the SAB 80515.

T-49-19-61

Figure 6
Interrupt Request Sources

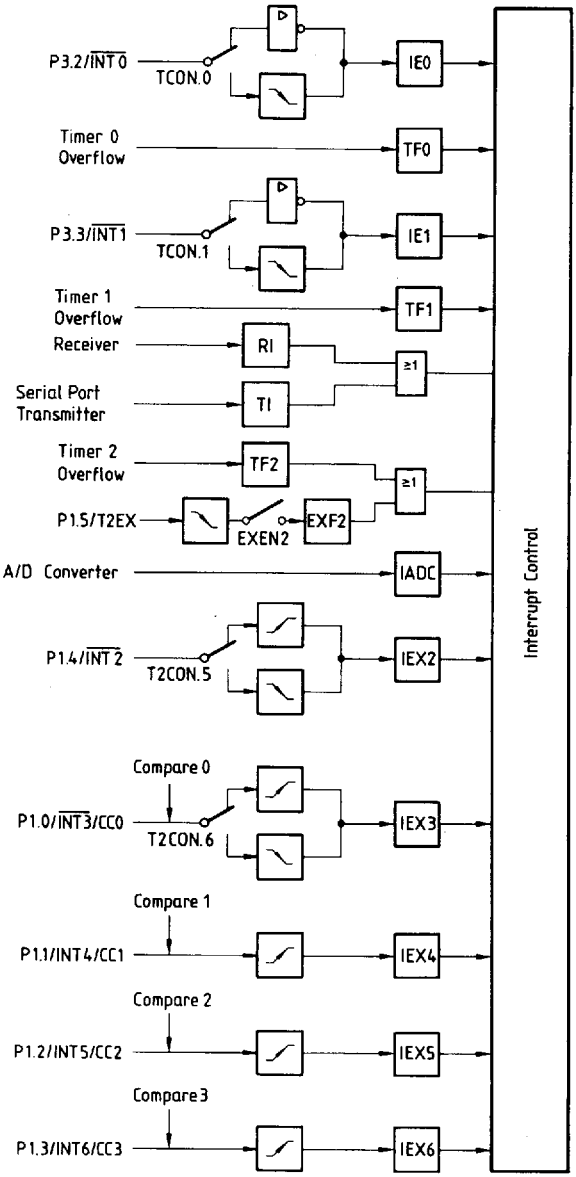
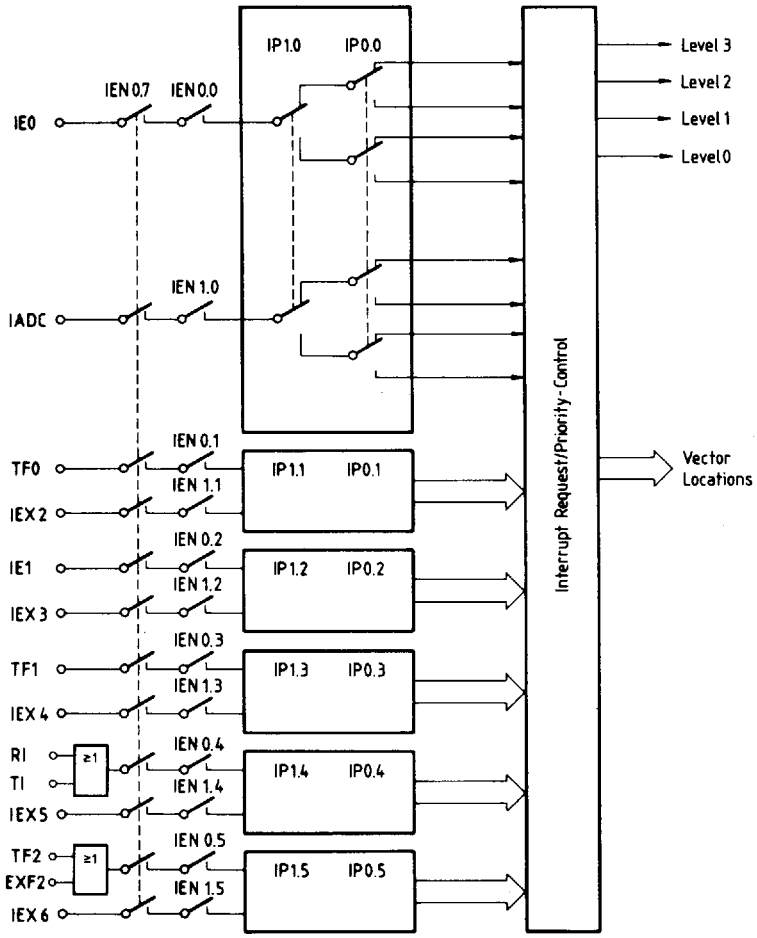


Figure 7
Priority Level Structure



Watchdog Timer

This feature is provided as a means of graceful recovery from software upset. After a reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65536 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), a hardware reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions. This is done to prevent the watchdog from being cleared by unexpected op codes.

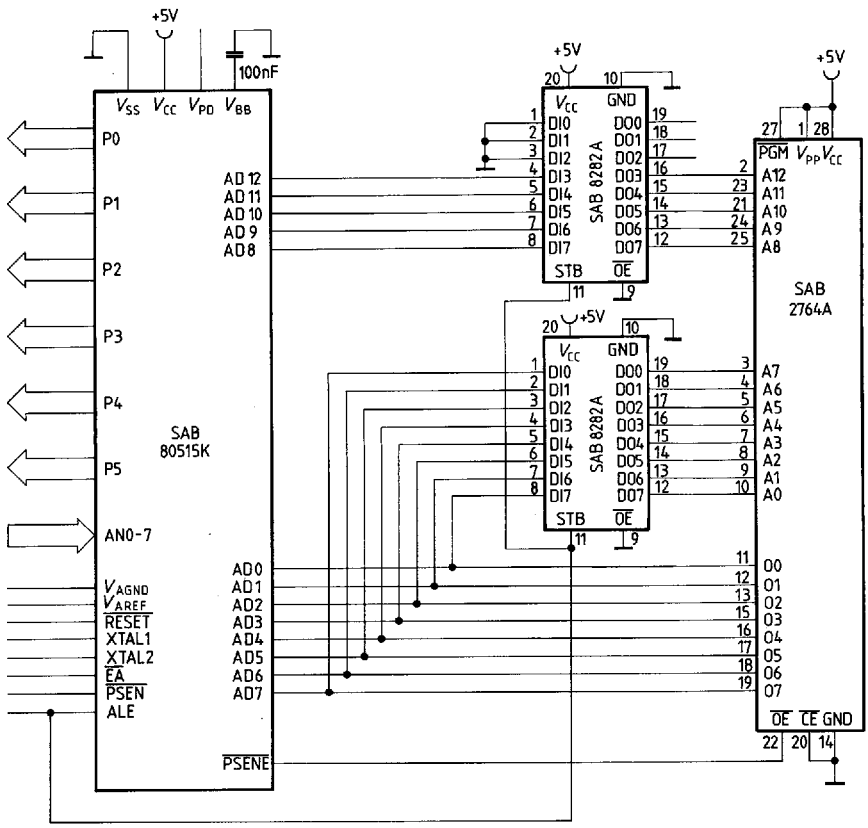
T-49-19-61

Connecting an External Program Memory to the SAB 80515K

The ROM-less chip SAB 80515K allows emulating the SAB 80515's internal ROM via the additional bus interface. The multiplexed bus AD0 to AD12 emits the address and reads the instruction at pins AD0 to AD7. Observe that the higher address lines AD8 to AD12 are also multiplexed. The control signals for the emulation memory are ALE and $\overline{\text{PSENE}}$.

When pin $\overline{\text{EA}}$ is high, the SAB 80515K executes instructions read from AD0-AD12 if the PC is less than 8192, otherwise it will execute from external program memory at port 0 and 2. When pin $\overline{\text{EA}}$ is low, the SAB 80515K executes all instructions from external program memory. Figure 8 shows a typical circuitry for connection of a program memory to AD0-AD12 of the SAB 80515K.

Figure 8
Connecting an External Program Memory



T-49-19-61

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

T-49-19-61

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	2
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate accumulator right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Data transfer

MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct *)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

*) MOV A,ACC is not a valid instruction

T-49-19-61

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

Boolean variable manipulation

CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64-Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

T-49-19-61

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to + 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	−0.5 to + 7 V
Power dissipation	2 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$; $T_A = 0$ to 70°C

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage (except $\overline{RESET}$ and XTAL2)	2.0	V_{CC}+0.5	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	V_{CC}+0.5	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to $\overline{RESET}$	3.0	–	V	–
V_{PD}	Power-down voltage	3	5.5	V	$V_{CC} = 0\,V$
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	$I_{OL} = 1.6$ mA
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$, $\overline{PSENE}$	–	0.45	V	$I_{OL} = 3.2$ mA
V_{OL2}	Output low voltage, AD0 to AD12	–	0.45	V	$I_{OL} = 2$ mA
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	$I_{OH} = -80\,\mu A$
V_{OH1}	Output high voltage, port 0, ALE, $\overline{PSEN}$, $\overline{PSENE}$	2.4	–	V	$I_{OH} = -400\,\mu A$
V_{OH2}	Output high voltage, AD0 to AD12	2.4	–	V	$I_{OH} = -2$ mA
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	−800	µA	$V_{IL} = 0.45\,V$
I_{IL2}	Logic 0 input current, XTAL2	–	−2.5	mA	XTAL1 = V_{SS} $V_{IL} = 0.45\,V$
I_{IL3}	Input low current to $\overline{RESET}$ for reset	–	−500	µA	$V_{IL} = 0.45\,V$
I_{LI}	Input leakage current to port 0, $\overline{EA}$, AD0 to AD12	–	±10	µA	$0\,V < V_{IN} < V_{CC}$
I_{CC}	Power supply current	–	210	mA	all outputs disconnected
I_{PD}	Power-down current	–	3	mA	$V_{CC} = 0\,V$
C_{IO}	Capacitance of I/O buffer	–	10	pF	$f_c = 1$ MHz

A/D Converter Characteristics

$V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$; $V_{AREF} = V_{CC} \pm 5\%$; $V_{AGND} = V_{SS} \pm 0.2V$; $V_{IntAREF} - V_{IntAGND} \geq 1V$;
$T_A = 0$ to $+70°C$ for SAB 80515K

Symbol	Parameter	Limit values			Unit	Test condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	$V_{AGND}-$ 0.2	–	$V_{AREF}+$ 0.2	V	–
C_I	Analog input capacitance	–	25	–	pF	1)
t_L	Load time	–	–	$2t_{CY}$	µs	–
t_S	Sample time (incl. load time)	–	–	$5t_{CY}$	µs	–
t_C	Conversion time (incl. sample time)	–	–	$15t_{CY}$	µs	–
DNLE	Differential non-linearity	–	±1/2	±1	LSB	$V_{IntAREF} =$
INLE	Integral non-linearity	–	±1/2	±1	LSB	$V_{AREF} = V_{CC}$
	Offset error	–	±1/2	±1	LSB	$V_{IntAGND} =$
	Gain error	–	±1/2	±1	LSB	$V_{AGND} = V_{SS}$
TUE	Total unadjusted error	–	±1	±2	LSB	1)
I_{REF}	V_{AREF} supply current	–	–	5	mA	2)
$V_{IntREFERR}$	Internal reference error	–	–	TBD	mV	2)

1) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

2) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics

$T_A = 0$ to 70°C; $V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$
(C_L for port 0, ALE, $\overline{PSEN}$ and $\overline{PSENE}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics at Port 0/Port 2

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	$12t_{CLCL}$	–	ns
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL1}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV1}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$-100	ns
t_{LLPL1}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH1}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}$-35	–	ns
t_{PLIV1}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}$-100	ns
t_{PXIX1}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ1} [4]	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV1} [4]	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV1}	Address to valid instruction in	–	302	–	$5t_{CLCL}$-115	ns
t_{AZPL1}	Address float to $\overline{PSEN}$	0	–	0	–	ns

External Data Memory Characteristics

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}$-100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}$-35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}$-165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}$-70	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}$-150	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}$-165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}$-130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns
t_{DVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL}-50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}$-150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL}-50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

[4] Interfacing the SAB 80515K to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

T-49-19-61

Program Memory Characteristics at AD0-AD12

Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	$12t_{CLCL}$	–	ns
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$-40	–	ns
t_{AVLL2}	Address setup to ALE	53	–	t_{CLCL}-30	–	ns
t_{LLAX3}	Address hold after ALE	48	–	t_{CLCL}-35	–	ns
t_{LLIV2}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$-100	ns
t_{LLPL2}	ALE to $\overline{PSENE}$	58	–	t_{CLCL}-25	–	ns
t_{PLPH2}	$\overline{PSENE}$ pulse width	215	–	$3t_{CLCL}$-35	–	ns
t_{PLIV2}	$\overline{PSENE}$ to valid instruction in	–	150	–	$3t_{CLCL}$-100	ns
t_{PXIX2}	Input instruction hold after $\overline{PSENE}$	0	–	0	–	ns
t_{PXIZ2} [5]	Input instruction float after $\overline{PSENE}$	–	63	–	t_{CLCL}-20	ns
t_{PXAV2} [5]	Address valid after $\overline{PSENE}$	75	–	t_{CLCL}-8	–	ns
t_{AVIV2}	Address to valid instruction in	–	302	–	$5t_{CLCL}$-115	ns
t_{AZPL2}	Address float to $\overline{PSENE}$	0	–	0	–	ns

External Clock Drive XTAL2

Symbol	Parameter	Limit values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	t_{CLCL}-t_{CLCX}	ns
t_{CLCK}	Low time	20	t_{CLCL}-t_{CHCX}	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

System Clock Timing

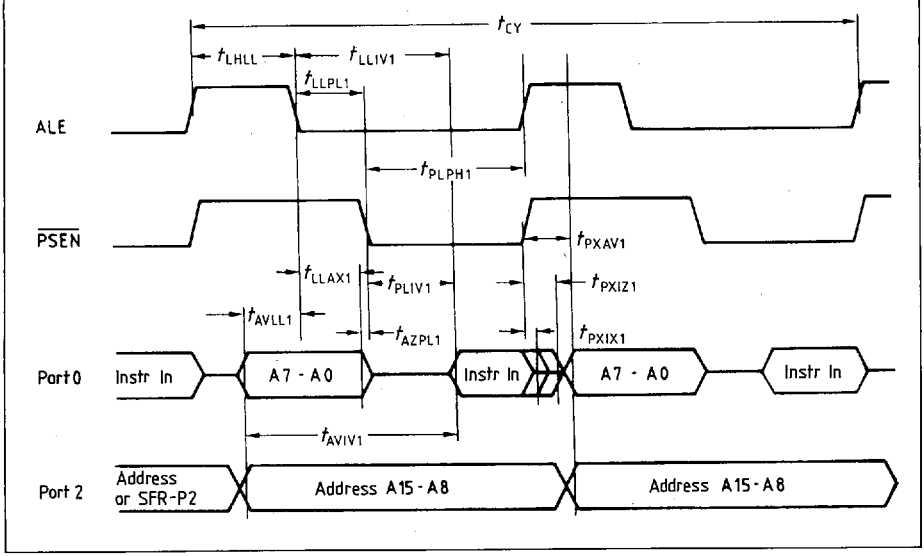
Symbol	Parameter	Limit values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LLSH}	ALE to CLKOUT	543	–	$7t_{CLCL}$-40	–	ns
t_{SHSL}	CLKOUT high time	127	–	$2t_{CLCL}$-40	–	ns
t_{SLSH}	CLKOUT low time	793	–	$10t_{CLCL}$-40	–	ns
t_{SLLH}	CLKOUT low to ALE high	43	123	t_{CLCL}-40	t_{CLCL}+40	ns

[5] Interfacing the SAB 80515K to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to AD0–AD7 drivers.

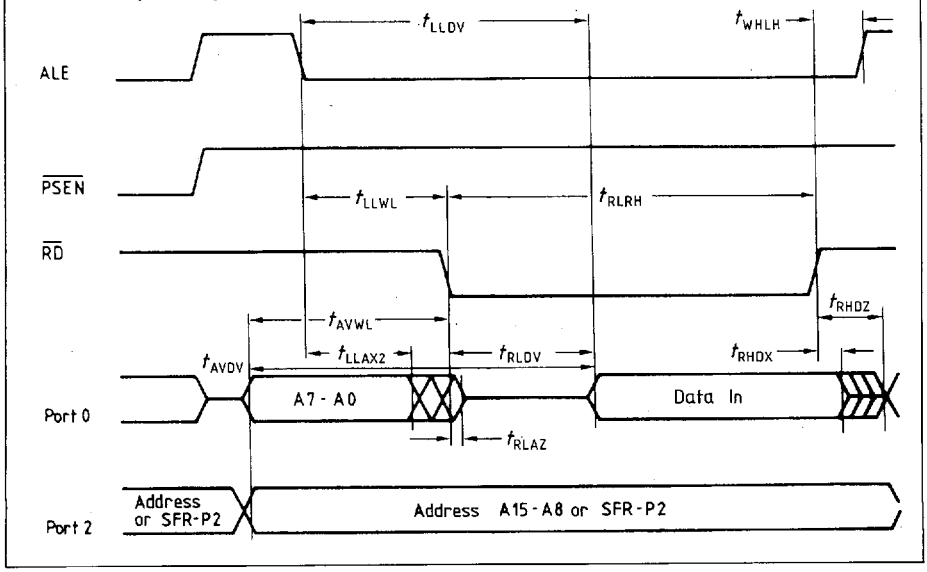
Waveforms

T-49-19-61

Program Memory Read Cycle at Port 0 / Port 2

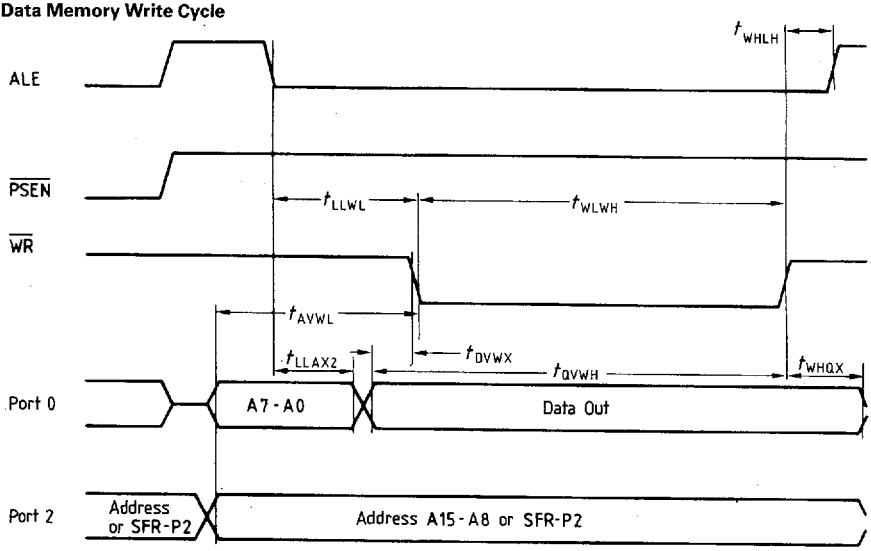


Data Memory Read Cycle

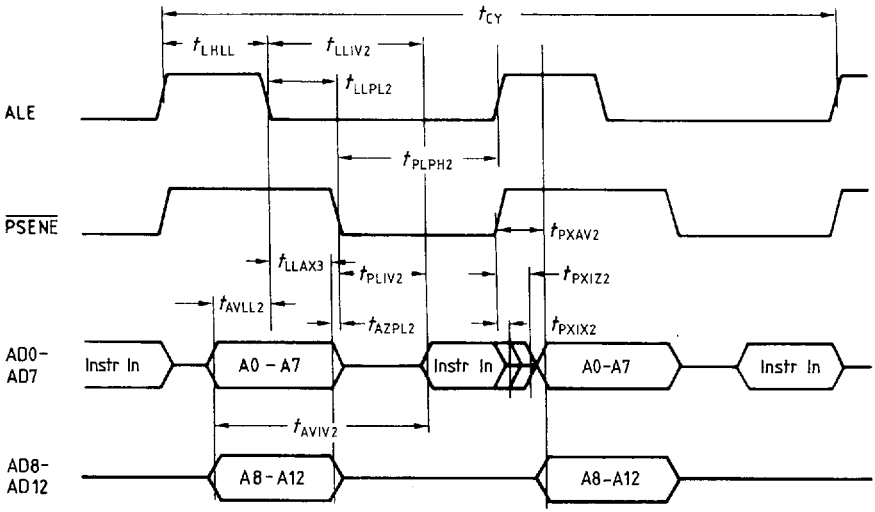


T-49-19-61

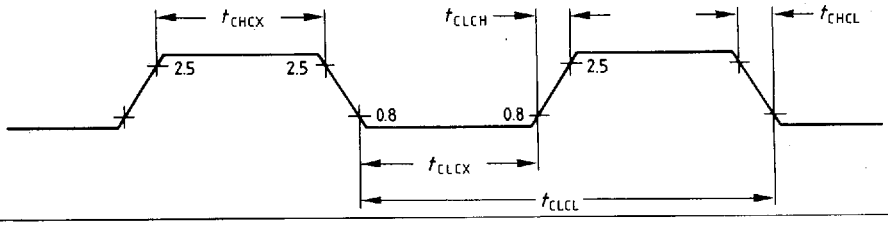
Data Memory Write Cycle



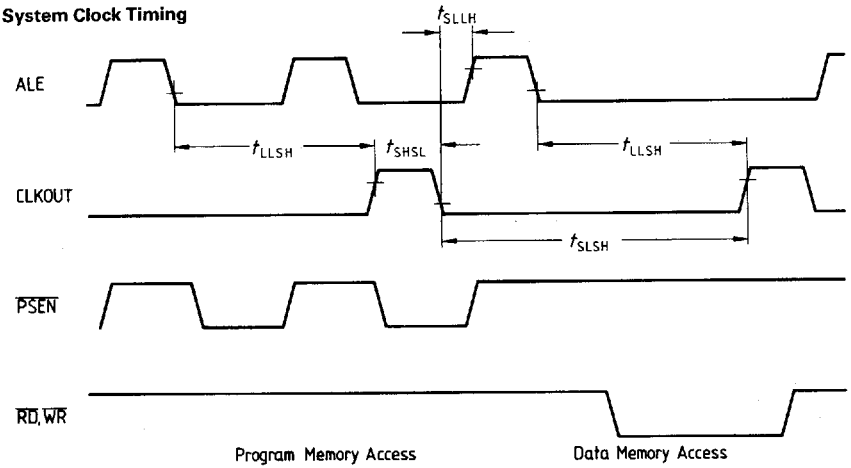
Emulation Memory Read Cycle at AD0-AD12



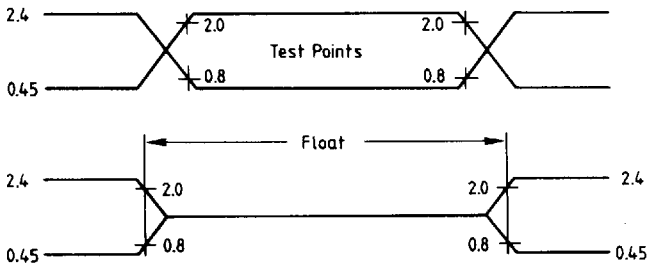
External Clock Cycle



System Clock Timing

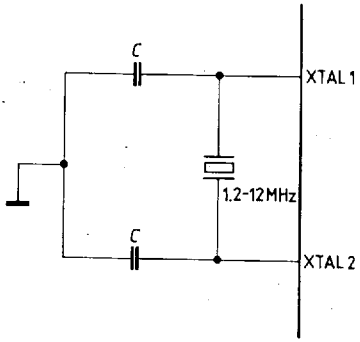


AC Testing Input, Output, Float Waveforms



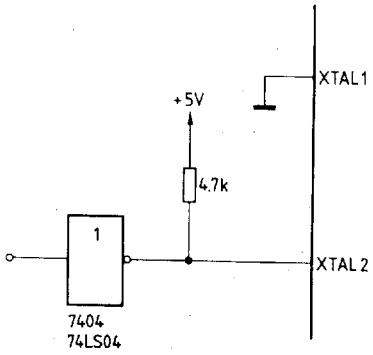
AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pins sinks 3.2 mA or sources 400 µA at voltage test levels.

Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode

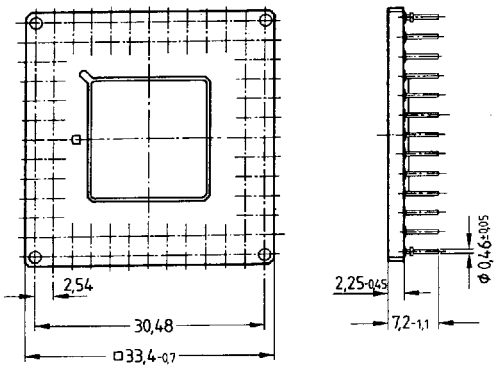


Driving from External Source

Package Outlines

T-49-19-61

Pin Grid Array, C-PGA-88



Dimensions in mm

Ordering Information

Type	Ordering code	Function
SAB 80515K-A	Q67120-C267	8-bit single-chip microcontroller, ROM-less version