Preliminary Data **MOS IC**

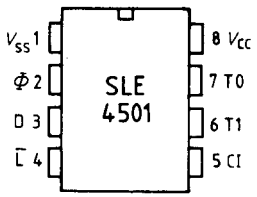
Type	Ordering Code	Package
SLE 4501 SLE 4501 K	Q67100-H8377 in preparation	P-DIP-8 MIKROPACK (SMD)

Features

- Internal generation of programming voltage
- Counting range 22 binary bits, nonvolatile storage
- Count output in serial binary code
- Counting operation is executed under on-chip control and cannot be influenced externally
- Disconnection of the operating voltage, even during a counting operation, has no effect on the stored count
- Once the fusible link has been blown, the count is protected against manipulation by internal safety logic.
- Additional 64x8 bit EEPROM area with serial access (byte organization)
- Non-volatile reprogramming of EEPROM area and count through on-chip control onto defined viewport, thus reliable data storage is ensured.
- Extended temperature range from −40 °C to +110 °C

Pin Configuration

(top view)



Pin Description

Pin	Symbol	Function
1	V_{SS}	Ground
2	Φ	Clock input
3	D	Data input/output
4	$\overline{L}$	Chip select for data input (active high) and indication of storage operation (active low)
5	CI	Count pulse input (active high)
6	T1	Fusible link
7	T0	Control input test operation and fusible link
8	V_{CC}	Operating range

Circuit Description

The nonvolatile counter (NC) has a counting range of 22 binary bits and retains its count even after the operating voltage has been disconnected. The safety logic of the device prevents any alteration other than the intended incrementing of the count, which might be caused by supply voltage failures, e.g. during a counting operation. Before the fusible link blows, a desired count can be preset in a test operation. After the fusible link has blown, the count can only be altered by a count request. Thus it is only possible to increment the counter.

The count is binary coded and can be serially sampled via a three-wire bus (section 4). A counting operation has priority in any case and will terminate any readout operation that has been started.

The 64x8 bit EEPROM area (NVM) is addressed serially by a 1-byte OP code (see programming and readout operation). Addresses 16 through 63 can no longer be reprogrammed after the fusible link is blown. Before the fusible link blows, test input T0 should be set low for normal operation.

An on-chip reset circuit ensures operational reliability. Its functioning is described on page 870.

Counting Operation (figure 1c)

The integrated circuit consists of a 22-step, asynchronous counter and a nonvolatile, electrically reprogrammable memory (EEPROM) for nonvolatile storage of the counter contents.

For reasons of operational reliability, the counting operation is executed entirely under on-chip control. The device includes the necessary sequence control for which it generates an internal clock of approx. 50 kHz. A pulse at input CI causes the asynchronous counter to be incremented by 1.

The new count is stored as nonvolatile information. This storage operation is indicated by low at input/output $\overline{L}$. During storage no other count events are registered, resulting in a dead time of max. 100 ms in the rated-voltage range. The operating voltage must be maintained in the rated-voltage range for at least another 10 ms after the start of a storage operation, or else the last count event might not be permanently stored (response time). Counts that have already been stored are not at all affected if the operating voltage is switched off during a storage operation and thus cannot be manipulated. If the operating voltage is reduced during the counting operation, the dead time and the response time will increase, but storage reliability is not affected due to the integrated programming-duration control. The device is inactive outside the operating-voltage window defined by the reset circuit.

The nonvolatile safety counter includes overflow protection. If all counter bits are 1, any further count pulses are ignored.

Count Readout (figure 1d)

For sampling the count, input/output $\overline{L}$ is first set low and then the two instruction bits B0, B1 are clocked in. Afterwards pin L is set high.again. With the trailing edge of any further clock pulse Φ the bits appear consecutively at pin D, starting with the most significant bit. The entire count is read out with 22 clock pulses. A low pulse at input/output L switches pin D back to high impedance.

A storage operation (nonvolatile counter or 64x8 bit EEPROM) indicated by a low level at pin $\overline{L}$ has always priority. During this time the device cannot be addressed. A count request will terminate any readout operation that has already been started.

Programming of NVM (figure 1a)

The input/output $\overline{L}$ must be set low. Then the 8-bit data word (D0 as the 1st bit) is first clocked in, followed by the 8-bit instruction word (consisting of six address bits A0 through A5 and two instruction bits B0, B1). After pin $\overline{L}$ has been set high again, the programming operation, indicated by low at the input/output $\overline{L}$, begins subsequently to another clock pulse Φ. When the internally controlled storage operation has been completed, $\overline{L}$ returns to high. In the rated-voltage range the maximum programming time t_p is 10 ms.

Readout of NVM (figure 1b)

The input/output $\overline{L}$ must be set low. Then the 8-bit instruction word (consisting of 6 address bits A0 through A5 and two instruction bits B0, B1) is clocked in. After pin $\overline{L}$ has been set high again, one bit (beginning with D0) of the respective data word appears at pin D with the trailing edge of any further clock pulse Φ. The entire data word is read out with eight clock pulses. A low pulse at input/output $\overline{L}$ switches pin D back to high impedance.

Fusible Link (figure 4)

Blowing of the fusible link has the following irreversible effects:

a) The count can now only be altered by count pulses at count input CI.
b) It is no longer possible to program the entire NVM in one operation.
c) Addresses 16 through 63 of the NVM can no longer be reprogrammed.

In order to blow the fusible link, the following conditions must prevail at the inputs (cf. **figure 4**):

a) Test input T0 to 17 V
b) Test input T1 to 17 V with max. 1 µs edge rise time.

The fusible link melts within 100 ms. At test input T0 there is a temporary peak current of up to 100 mA which can be taken from a storage capacitor, for instance.

For the blowing process, test input T0 must be connected according to **figure 4b**, otherwise the device might be destroyed.

Test Operation (figure 2a, 2b, 2c)

Provided the fusible link has not blown the following test operations are possible (T1 must always be kept low and T0 high):

a) Presetting of count **(figure 2a)**

The input/output $\overline{L}$ is set low and then the 22 bits constituting the required count are clocked in, starting with the most significant bit. Here it should be noted that the counter bits CB0 through CB3 can only be programmed uniformly as 0 or 1. After the two bits of the instruction code have been clocked in, pin $\overline{L}$ is set high again.

Differing values for CB0 through CB3 will lead to undefined counts.

A high on count input CI starts the programming operation, which is indicated by a low at pin $\overline{L}$. In order to activate the safety logic for the preset count, T0 must then be set low and the supply voltage switched off briefly.

b) Erasure of entire NVM **(figure 2b)**
Writing into entire NVM **(figure 2c)**

Input/output $\overline{L}$ is set low and the two bits B0, B1 of the instruction code are clocked in. After switching pin $\overline{L}$ to high, a high at input Φ will start the programming operation which is indicated by a low at input/output $\overline{L}$. Input Φ must be kept high for at least 50 ms because the internal timing control for the NVM is switched off and the programming duration (t_{gpr}) is defined for the length of the Φ pulse.

Instruction Codes

a) T0 low or after blowing the fusible link:

Function	B0	B1
Program NVM	1	0
Read out NVM	1	1
Read out counter	0	1

b) T0 high (test operation):

Started by pulse at CI

Function	B0	B1
Preset counter	0	0

Started by clock pulse Φ

Function	B0	B1
Erase entire NVM Write into entire NVM	1	0

Reset Function

For reasons of operational reliability the device contains an internal reset circuit that limits the active range to that of a voltage window. The lower limit is at a maximum of 4.5 V and the upper limit at a minimum of 5.5 V.

If the supply voltage is outside the window, even if only because of spikes, the device will reset. As soon as the prescribed voltage window has been reached again, a reset routine runs automatically, this being indicated by a low at input/output $\overline{L}$ resulting in a dead time of max. 100 ms in the rated-voltage range.

Maximum Ratings

Description	Symbol	min	typ	max	Unit
Supply voltage Input voltage	V_{CC} V_I	−0.3 −0.3		6 6	V V
Power dissipation	P_D		40		mW
Storage temperature	T_{stg}	−55		125	°C
Thermal resistance system – air	$R_{th\ SA}$		100		K/W

Operating Range

Supply voltage	V_{CC}	4.75		5.25	V
Ambient temperature	T_A	−40		110	°C

Characteristics

Description	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.75		5.25	V
Supply current	I_{CC}		7	10	mA
Inputs[1])	V_I		0.5	0.8	V
(Φ, $\overline{L}$, CI, D, T1)	V_H	2.2		V_{CC}	V
(T0)	V_H	4.95		V_{CC}	V
(Φ, $\overline{L}$, CI, D, T1)	I_H			10	µA
(T0)	I_H			100	µA
Outputs (D, $\overline{L}$)	I_L	1			mA
(open drain, $V_I = 0.5$ V)	I_H			10	A
Counting dead time	t_{dead}			100	ms
Counting response time	t_{resp}			10	ms
Clock Φ	t_H	5		1000	µs
	t_L	5			µs
	t_f	1			µs
Interval start pulse/ trailing edge $\overline{L}$	t_{ST}	5			µs
Count input CI	t_{CI}	5			µs
Programming time NVM (per byte)	t_{pr}			10	ms
Programming time NVM (total memory)	t_{gpr}	50		100	ms
Blowing of fusible link:					
T0	V_H	16.7		17.3	V
	I_H			100	mA
T1	V_H	16.7		17.3	V
	I_H			10	µA
	t_f			1	µs
	t_s	100			ms

[1]) The following particular level conditions apply to the input Φ in case of test operating modes:

Φ (test operation)	V_L		0.5	0.6	V
	V_H	3.0		V_{CC}	V

Block Diagram

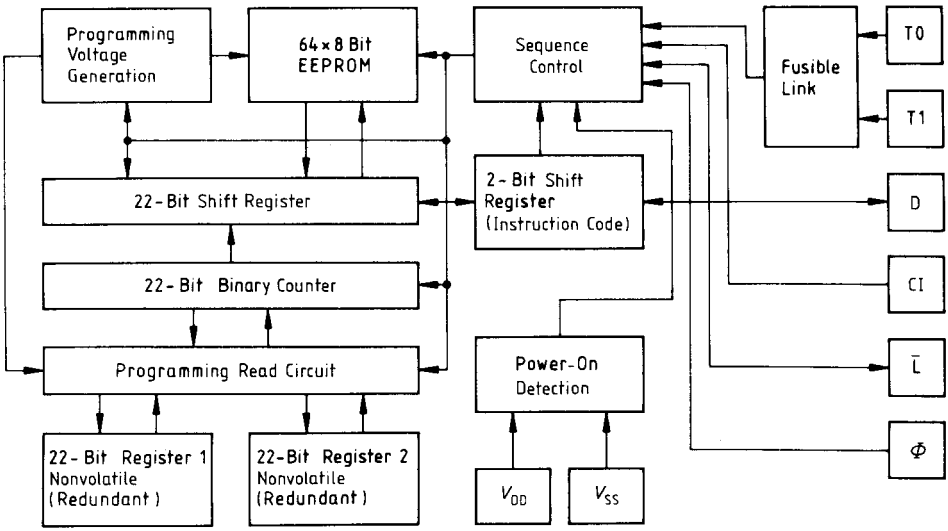


Figure 1a Programming of NVM

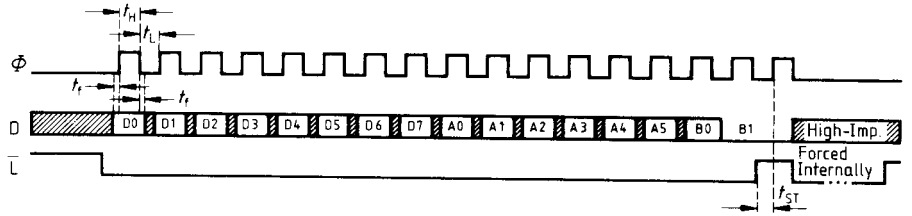


Figure 1b Readout of NVM

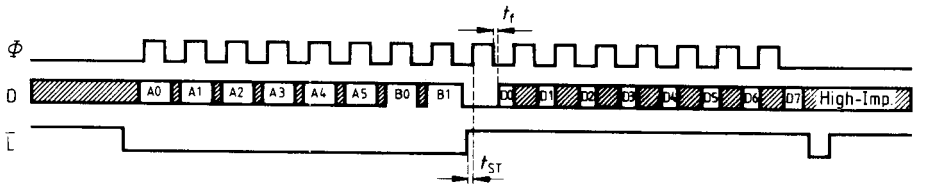


Figure 1c Counting Operation

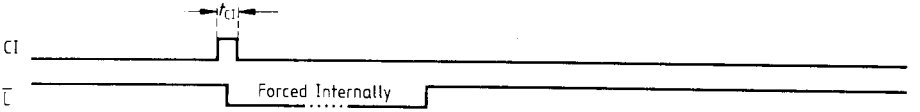


Figure 1d Reading Out Count

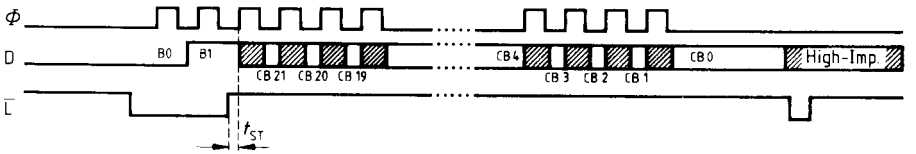


Figure 2a Presetting Count on NC

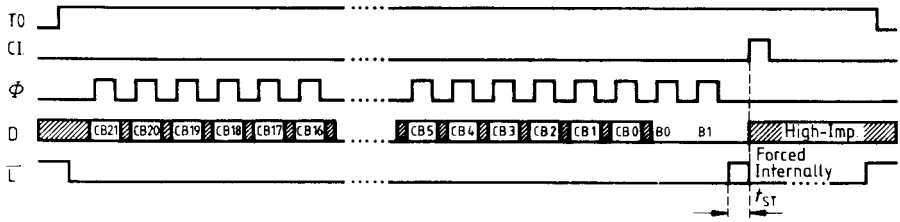


Figure 2b Erasure of Entire NVM

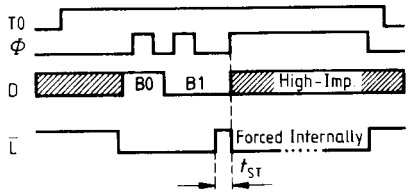


Figure 2c Writing into Entire NVM

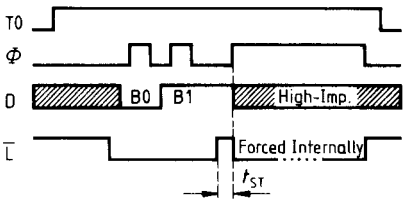


Figure 3
Application Circuit

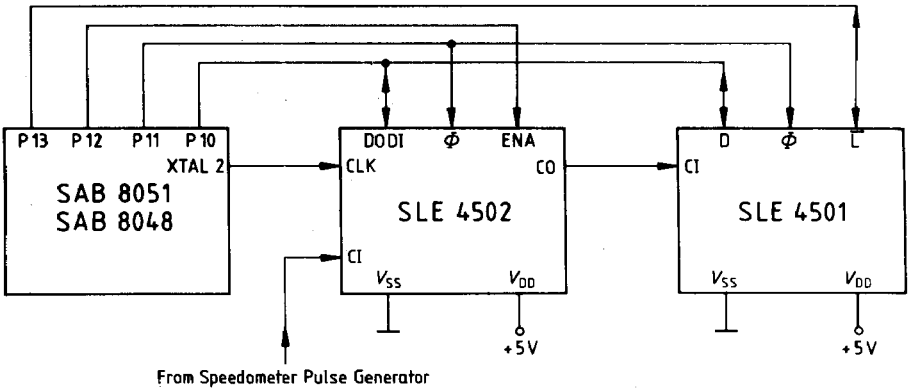


Figure 4
Blowing Fusible Link