

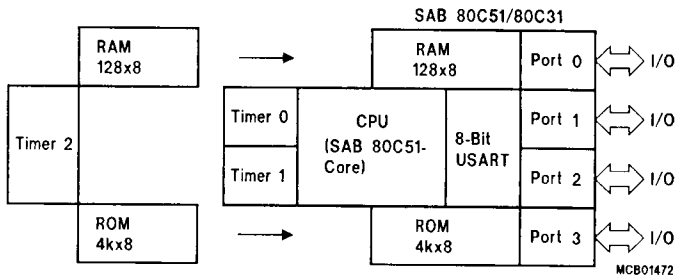
High-Performance 8-Bit CMOS Microcontroller

SAB 80C52/80C32

Preliminary

SAB 80C52 CMOS microcontroller with factory-maskprogrammable ROM
SAB 80C32 CMOS microcontroller for external ROM

- Versions for 12 MHz /16MHz /20 MHz operating frequency
- 8 K × 8 ROM (SAB 80C52 only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Boolean processor
- Most instructions execute in 1 μs /750 ns /666 ns
- Multiply and divide in 4 μs /3 μs /2.7 μs
- Six interrupt sources, two priority levels
- Idle and power-down operation
- Fully functionally compatible with SAB 8052A/8032A
- Three temperature ranges available:
 - 0 to 70°C,
 - 40 to +85°C,
 - 40 to +110°C
- P-DIP-40 and P-LCC-44 package



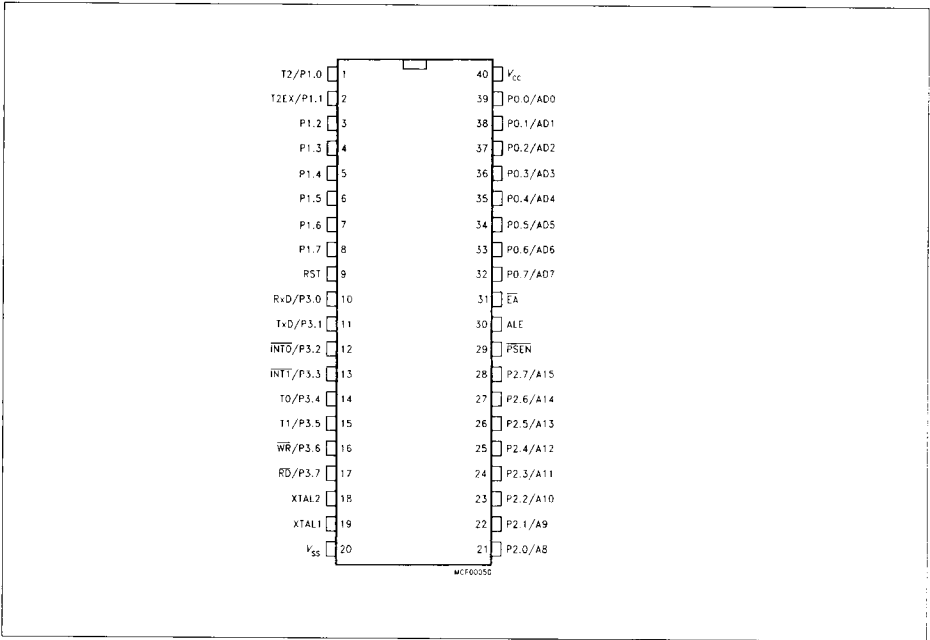
The SAB 80C52/80C32 is a standalone, high-performance CMOS single-chip microcontroller, designed in Siemens ACMOS technology. It is functionally compatible with the SAB 8052A/8032A devices in MYMOS technology.

Furthermore, it is backwardly compatible with the SAB 80C51/80C31. The low-power properties of ACMOS technology allow applications where power consumption and dissipation are critical. In addition, the SAB 80C52/80C32 has two software-selectable modes of reduced activity for further power reduction – idle and power-down.

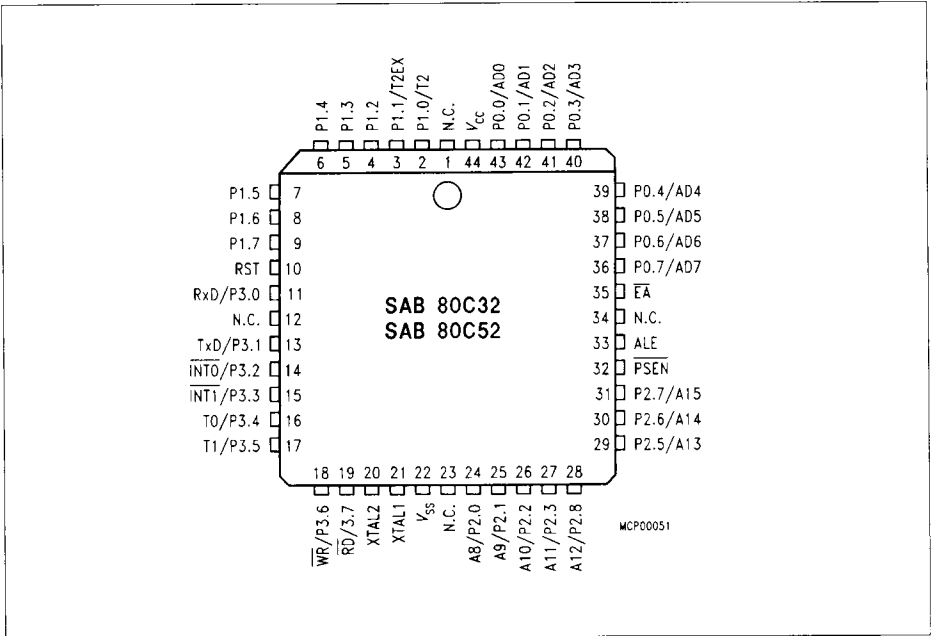
The SAB 80C52 contains a non-volatile 8 K × 8 read-only program memory, a volatile 256 K × 8 read/write data memory, 32 I/O lines, three 16-bit timer/counters, a six-source, two-priority-level interrupt structure, a serial I/O port, an on-chip oscillator, and clock circuits. The SAB 80C32 is identical, except that it lacks the program memory on the chip.

Ordering Information

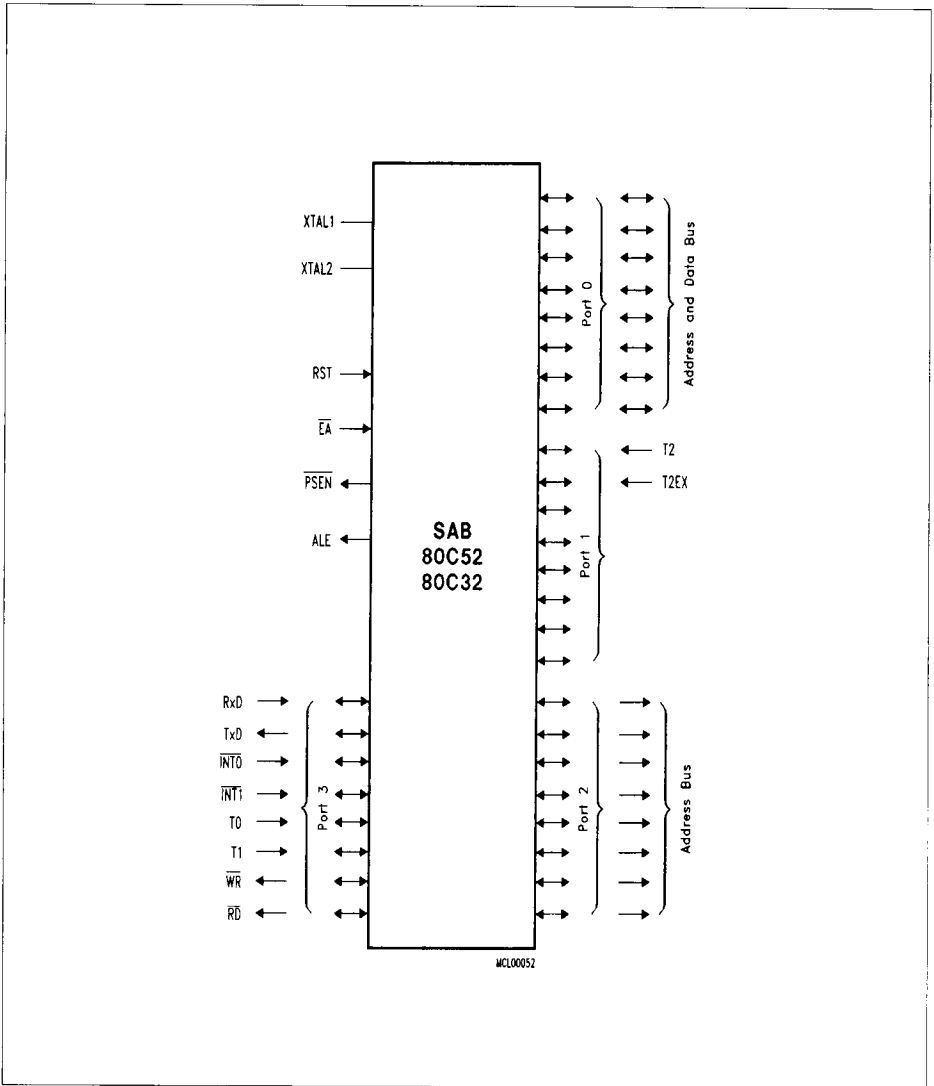
| Type | Ordering code | Package | Description 8-bit CMOS microcontroller |
|----------------------------------|----------------------------|----------------------|---|
| SAB 80C52-N SAB 80C52-P | Q67120-C396 Q67120-C379 | P-LCC-44 P-DIP-40 | with factory mask-programmable ROM, 12 MHz |
| SAB 80C32-N SAB 80C32-P | Q67120-C395 Q67120-C378 | P-LCC-44 P-DIP-40 | for external memory, 12 MHz |
| SAB 80C52-P-T40/85 | Q67120-C521 | P-DIP-40 | with factory mask-programmable ROM, 12 MHz, ext. temp. – 40 to 85 °C |
| SAB 80C32-P-T40/85 | Q67120-C520 | P-DIP-40 | for external memory, 12 MHz, ext. temp. – 40 to 85 °C |
| SAB 80C52-16-N SAB 80C52-16-P | Q67120-C503 Q67120-C501 | P-LCC-44 P-DIP-40 | with factory mask-programmable ROM, 16 MHz |
| SAB 80C32-16-N SAB 80C32-16-P | Q67120-C502 Q67120-C500 | P-LCC-44 P-DIP-40 | for external memory, 16 MHz |
| SAB 80C52-16-P-T40/85 | Q67120-C563 | P-DIP-40 | with factory mask-programmable ROM, 16 MHz, ext. temp. – 40 to 85 °C |
| SAB 80C32-16-P-T40/85 | Q67120-C527 | P-DIP-40 | for external memory, 16 MHz ext. temp. -40 to 85 °C |
| SAB 80C52-20-N SAB 80C52-20-P | Q67120-C710 Q67120-C708 | P-LCC-44 P-DIP-40 | with factory mask-programmable ROM, 20 MHz |
| SAB 80C32-20-N SAB 80C32-20-P | Q67120-C711 Q67120-C709 | P-LCC-44 P-DIP-40 | for external memory, 20 MHz |



Pin Configuration (P-DIP-40)



Pin Configuration
(P-LCC-44)



Logic Symbol

Pin Definitions and Functions

| Symbol | Pin Number | | I/O ^{*)} | Function |
|-----------|------------|----------|-------------------|--|
| | P-DIP-40 | P-LCC-44 | | |
| P1.0-P1.7 | 1-8 | 2-9 | I/O | <p>Port 1 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 1 also receives the low-order address bytes during program verification. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows:</p> <ul style="list-style-type: none"> – T2 (P1.0): Input to counter 2. – T2 EX (P1.1): Capture/Reload trigger of timer 2. |
| RST | 9 | 10 | I | A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC} . |

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | | I/O [*] | Function |
|-----------|------------|--------------|------------------|---|
| | P-DIP-40 | P-LCC-44 | | |
| P3.0-P3.7 | 10-17 | 11, 13-19 | I/O | <p>Port 3 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and \overline{RD} and \overline{WR} pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate.</p> <p>The secondary functions are assigned to the pins of port 3, as follows:</p> <ul style="list-style-type: none"> – R x D/data (P3.0): Serial port's receiver data input (asynchronous) or data input/output (synchronous). – T x D/clock (P3.1): Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2): Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3): Interrupt 1 input or gate control input for counter 1. – T0 (P3.4): Input to counter 0. – T1 (P3.5): Input to counter 1. – \overline{WR} (P3.6): The write control signal latches the data byte from port 0 into the external data memory. – (P3.7): The read control signal enables external data memory to port 0. |

* I = Input
O = Output

Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | | I/O *) | Function |
|----------------|------------|----------|--------|---|
| | P-DIP-40 | P-LCC-44 | | |
| XTAL1 XTAL2 | 19 18 | 21 20 | I/O | <p>XTAL 1 Input to the inverting oscillator amplifier and input to the internal clock generator circuits.</p> <p>XTAL 2 Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL1 should be driven, while XTAL 2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed.</p> |
| P2.0-P2.7 | 21-28 | 24-31 | I/O | <p>Port 2 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL} on the DC characteristics) because of the internal pullup resist. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.</p> |

* 1 = Input
0 = Output

Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | | I/O *) | Function |
|--------------------------|------------|----------|--------|--|
| | P-DIP-40 | P-LCC-44 | | |
| $\overline{\text{PSEN}}$ | 29 | 32 | O | Program Store Enable This output issues a control signal that enables the external program memory to access the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution. |
| ALE | 30 | 33 | O | Address Latch Enable Provides signal used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. |
| $\overline{\text{EA}}$ | 31 | 35 | I | External Access When held at a high level, the SAB 80C52 executes instructions from the internal ROM when the PC is less than 8192. When held at a low level, the SAB 80C52 fetches all instructions from the external program memory. For the SAB 80C32 this pin must be tied low. |

* I = Input
 O = Output

Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | | I/O ^{*)} | Function |
|-----------------|------------|------------------|-------------------|---|
| | P-DIP-40 | P-LCC-44 | | |
| | | | | <p>Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB 80C52. External pullup resistors are required during program verification.</p> |
| V _{CC} | 40 | 44 | | Supply voltage during normal, idle, and power-down operations. |
| V _{SS} | 20 | 22 | | Circuit ground potential. |
| NC | — | 1, 12, 23, 24 | — | No connection. |

* I = Input

O = Output

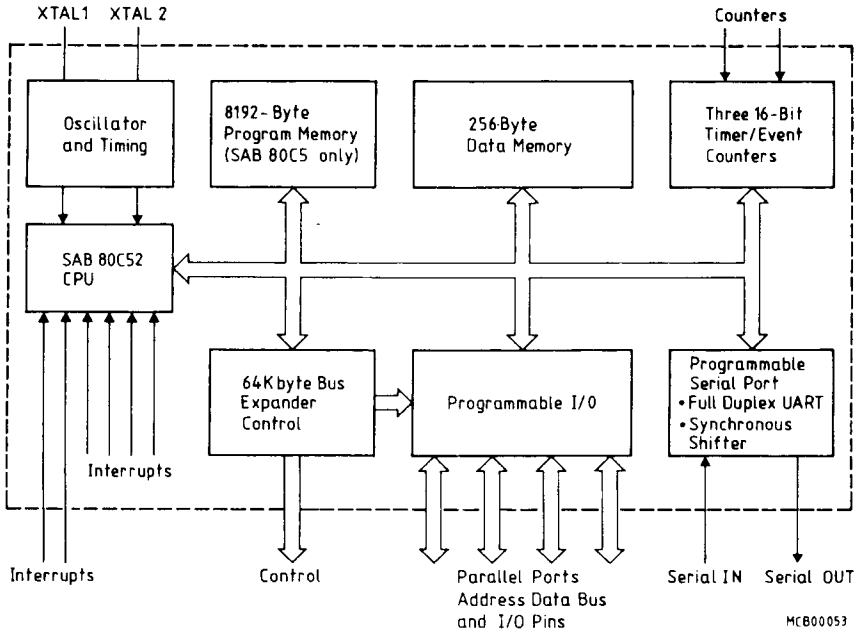


Figure 1
Block Diagram

Functional Description

The SAB 80C52/80C32 is functionally compatible with the SAB 8052A/8032A products that are designed in Siemens MYMOS technology. Furthermore, the SAB 80C52/80C32 is backwardly compatible with the SAB 80C51/80C31 devices.

In addition, instead of the RAM backup power supply of the SAB 8052A/8032A, the SAB 80C52/ 80C32 offers two additional power control modes, the idle mode and the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

Idle mode

In the idle mode, the CPU puts itself to sleep while all the on-chip peripherals stay active. The instruction that invokes the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The contents of the CPU, the on-chip RAM, and all the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor in the same way as a power-on reset.

Power-down mode

In the power-down mode the oscillator is stopped, and the instruction that invoke power-down is the last instruction executed. Only the contents of the on-chip RAM is preserved. A hardware reset is the only way to terminate power-down.

During power-down and idle mode the external pins will have the following status (see table 1):

Table 1
Status of the External Pins during Idle and Power-Down Modes

| Mode | Program Memory | ALE | PSEN | Port 0 | Port 1 | Port 2 | Port 3 |
|------------|----------------|-----|------|--------|---|---------|---|
| Idle | Internal | 1 | 1 | Data | Data/ Alternate Outputs | Data | Data/ Alternate Outputs |
| Idle | External | 1 | 1 | Float | Data/ Alternate Outputs | Address | Data/ Alternate Outputs |
| Power-Down | Internal | 0 | 0 | Data | Data/ Last Out- put of Alternate Function | Data | Data/ Last Out- put of Alternate Function |
| Power-Down | External | 0 | 0 | Float | Data/ Last Out- put of Alternate Function | Data | Data/ Last Out- put of Alternate Function |

Instruction Set

The SAB 80C52/80C32 has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function

Register, Interrupt Vectors and Assembler Directives.

Literature Information

| Title | Ordering No. |
|--|---------------------|
| Microcontroller Family SAB 8051 Pocket Guide | B158-B6229-X-X-7600 |

Absolute Maximum Ratings

| | |
|---|--|
| Ambient temperature under bias..... | 0 to 70 °C (SAB 80C52/80C32) – 40 to 85 °C (SAB 80C52/80C32-T40/85) – 40 to 110 °C (SAB 80C52/80C32-T40/110) |
| Storage temperature | – 65 to 150 °C |
| Voltage on any pin with respect to ground (V_{SS})..... | – 0.5 to V_{CC} 0.5 V |
| Voltage on V_{CC} to V_{SS} | – 0.5 to 6.5 V |
| Power dissipation..... | 1 W |

Note Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$V_{CC} = 5 V \pm 10\%$; $V_{SS} = 0 V$; $T_A = 0$ to 70 °C (SAB 80C52/80C32)
 $T_A = -40$ to 85 °C (SAB 80C52/80C32-T40/85)
 $T_A = -40$ to 110 °C (SAB 80C52/80C32-T40/110)

| Parameter | Symbol | Limit Values | | Unit | Test condition |
|---|-----------|-----------------------|--|------|--|
| | | min. | max. | | |
| Input low voltage (except EA) for SAB 80C52/80C32, 80C52/80C32-T40/85 for SAB 80C52/80C32, T40/110 | V_{IL} | – 0.5 – 0.5 | $0.2 V_{CC}$ – 0.1 $0.2 V_{CC}$ – 0.3 | V | – |
| Input low voltage ($\bar{E}A$) | V_{IL1} | – 0.5 | $0.2 V_{CC}$ – 0.3 | V | – |
| Input high voltage (except XTAL1, RST) | V_{IH} | $0.2 V_{CC}$ + 0.9 | $0.2 V_{CC}$ + 0.5 | V | – |
| Input high voltage (XTAL1, RST) | V_{IH1} | $0.7 V_{CC}$ | $V_{CC} + 0.5$ | V | – |
| Output low voltage (ports 1, 2, 3) | V_{OL} | – | 0.45 | V | $I_{OL} = 1.6 mA$ ¹⁾ |
| Output low voltage (port 0, ALE, PSEN) | V_{OL1} | – | 0.45 | V | $I_{OL} = 3.2 mA$ ¹⁾ |
| Output high voltage (ports 1, 2, 3) | V_{OH} | $2.4 V_{CC}$ 0.9 | – | V | $I_{OH} = -80 \mu A$ $I_{OH} = -10 \mu A$ |

Notes see page 367

DC Characteristics (cont'd)

| Parameter | Symbol | Limit Values | | Unit | Test condition |
|---|---------------|---------------------|----------|-----------|---|
| | | min. | max. | | |
| Output high voltage (port 0 in external bus mode, ALE, PSEN) | V_{OH1} | 2.4 V_{CC} 0.9 | – – | V V | $I_{OL} = -800 \mu A$ $I_{OL} = -80 \mu A^{2)}$ |
| Logical 0 input current (ports 1, 2, 3) | I_{IL} | – | – 50 | V | $V_{IN} = 0.45 V$ |
| Logical 1-to-0 transition current (ports 1, 2, 3) | I_{TL} | – | – 650 | V V | $V_{IN} = 2 V$ |
| Input leakage current (port 0, EA) | I_{\square} | – | ± 10 | μA | $0.45 < V_{IN} < V_{CC}$ |
| Reset pulldown resistor | R_{RST} | 40 | 150 | $k\Omega$ | – |
| Pin capacitance | C_{IO} | – | 10 | | $f \leq 1 \text{ MHz}$, $T_A = 25 \text{ }^\circ\text{C}$ |
| Power supply current: Active mode, 12 MHz ⁶⁾ | I_{CC} | – | 20 | mA | $V_{CC} = 5 V^{4)}$ |
| Active mode, 16 MHz ⁶⁾ | I_{CC} | – | 26 | mA | $V_{CC} = 5 V^{4)}$ |
| Idle mode, 12 MHz ⁶⁾ | I_{CC} | – | 6.8 | mA | $V_{CC} = 5 V^{5)}$ |
| Idle mode, 16 MHz ⁶⁾ | I_{CC} | – | 8.4 | mA | $V_{CC} = 5 V^{5)}$ |
| Power Down Mode | I_{PD} | – | 50 | μA | $V_{CC} = 2 \dots 5.5 V^{3)}$ |

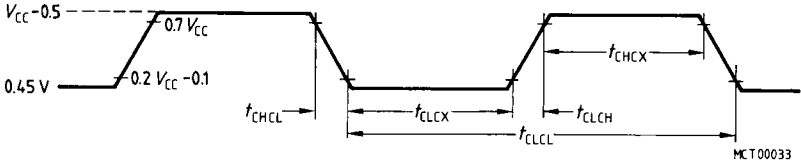
Notes see page 367

Notes for pages 365 and 366

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and \overline{PSEN} to momentarily fall below the $0.9 V_{CC}$ specification when the address lines are stabilizing.
- 3) Power-down I_{CC} is measured with: $\overline{EA} = \text{Port 0} = V_{CC}$; XTAL1 = V_{SS} ; XTAL2 = N.C.;
- 4) I_{CC} (active mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA} = \text{Port 0} = V_{CC}$; RST = V_{CC} ; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.
- 5) I_{CC} (idle mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; $\overline{EA} = V_{SS}$; Port 0 = V_{CC} ; RST = V_{SS} ; all other pins are disconnected.
- 6) $I_{CC \text{ Max}}$ at other frequencies is given by:

| | |
|--------------|--|
| active mode: | $I_{CC \text{ Max}} = 1.5 * f_{OSC} + 2.0$ |
| idle mode: | $I_{CC \text{ Max}} = 0.4 * f_{OSC} + 2.0$ |

 where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at $V_{CC} = 5 \text{ V}$ (see also notes 5 and 6)



Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode

AC Characteristics

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$;

$T_A = 0\text{ to }70\text{ }^\circ\text{C}$; (SAB 80C52/80C32)

$T_A = -40\text{ to }85\text{ }^\circ\text{C}$; (SAB 80C52/80C32 – T40/85)

$T_A = -40\text{ to }110\text{ }^\circ\text{C}$; (SAB 80C52/80C32 – T40/110)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

| Parameter | Symbol | Limit values | | | | Unit |
|-----------|--------|--------------|------|--|------|------|
| | | 12 MHz clock | | Variable clock $1/t_{CLCL} = 0.5\text{ MHz to }12\text{ MHz}$ | | |
| | | min | max. | min. | max. | |

Program Memory Characteristics

| | | | | | | |
|--|---------------|-----|-----|-------------------|-------------------|----|
| ALE pulse width | t_{LHLL} | 127 | – | $2 t_{CLCL} - 40$ | – | ns |
| Address setup to ALE | t_{AVLL} | 43 | – | $t_{CLCL} - 40$ | – | ns |
| Address hold after ALE | t_{LLAX} | 60 | – | $t_{CLCL} - 23$ | – | ns |
| Address to valid instruction in | t_{LLIV} | – | 233 | – | $4t_{CLCL} - 100$ | ns |
| ALE to $\overline{\text{PSEN}}$ | t_{LLPL} | 58 | – | $t_{CLCL} - 25$ | – | ns |
| $\overline{\text{PSEN}}$ pulse width | t_{PLPH} | 215 | – | $3 t_{CLCL} - 35$ | – | ns |
| $\overline{\text{PSEN}}$ to valid instruction | t_{PLIV} | – | 150 | – | $3t_{CLCL} - 100$ | ns |
| Input instruction hold after $\overline{\text{PSEN}}$ | t_{PXIX} | 0 | – | 0 | – | ns |
| Input instruction float after $\overline{\text{PSEN}}$ | $t_{PXIZ}^*)$ | – | 63 | – | $t_{CLCL} - 20$ | ns |
| Address valid after $\overline{\text{PSEN}}$ | $t_{PXAV}^*)$ | 75 | – | $t_{CLCL} - 8$ | – | ns |
| Address to valid instruction in | t_{AVIV} | – | 302 | 0 | $5t_{CLCL} - 115$ | ns |
| Address float to $\overline{\text{PSEN}}$ | t_{PLAZ} | – | 0 | – | 0 | ns |

*) Interfacing the SAB 80C515A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

| Parameter | Symbol | Limit values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 12 MHz clock | | Variable clock 1/t _{CLCL} = 0.5 MHz to 12 MHz | | |
| | | min. | max. | min. | max. | |

External Data Memory Characteristics

| | | | | | | |
|---|--------------------|-----|-----|---------------------------|---------------------------|----|
| \overline{RD} pulse width | t _{RLRH} | 400 | – | 6 t _{CLCL} – 100 | – | ns |
| \overline{WR} pulse width | t _{WLWH} | 400 | – | 6 t _{CLCL} – 100 | – | ns |
| Address hold after ALE | t _{LLAX2} | 132 | – | 2 t _{CLCL} – 35 | – | ns |
| \overline{RD} to valid data in | t _{RLDV} | – | 252 | – | 5 t _{CLCL} – 165 | ns |
| Data hold after \overline{RD} | t _{RHDX} | 0 | – | 0 | – | ns |
| Data float after \overline{RD} | t _{RHDZ} | – | 97 | – | 2 t _{CLCL} – 70 | ns |
| ALE to valid data in | t _{LLDV} | – | 517 | – | 8 t _{CLCL} – 150 | ns |
| Address to valid data in | t _{AVDV} | – | 585 | – | 9 t _{CLCL} – 165 | ns |
| ALE to \overline{WR} or \overline{RD} | t _{LLWL} | 200 | 300 | 3 t _{CLCL} – 50 | 3 t _{CLCL} + 50 | ns |
| \overline{WR} or \overline{RD} high to ALE high | t _{WHLH} | 43 | 123 | t _{CLCL} – 40 | t _{CLCL} + 40 | ns |
| Address valid to \overline{WR} or \overline{RD} | t _{AVWL} | 203 | – | 4 t _{CLCL} – 130 | – | ns |
| Data valid to \overline{WR} transition | t _{QVWX} | 33 | – | t _{CLCL} – 50 | – | ns |
| Data setup before \overline{WR} | t _{QVWX} | 433 | – | 7 t _{CLCL} – 150 | – | ns |
| Data hold after \overline{WR} | t _{WHQX} | 33 | – | t _{CLCL} – 50 | – | ns |
| Address float after \overline{RD} | t _{RLAZ} | – | 0 | – | 0 | ns |

AC Characteristics (cont'd)

| Parameter | Symbol | Limit values | | Unit |
|-----------|--------|--|------|------|
| | | Variable clock Frequ. = 0.5 MHz to 12 MHz | | |
| | | min | max. | |

External Clock Drive XTAL1

| | | | | |
|-------------------|------------|------|-----------------------|----|
| Oscillator period | t_{CLCL} | 83.3 | 2000 | ns |
| High time | t_{CHCX} | 20 | $t_{CLCL} - t_{CHCX}$ | ns |
| Low time | t_{CLCX} | 20 | $t_{CLCL} - t_{CHCX}$ | ns |
| Rise time | t_{CLCH} | - | 20 | ns |
| Fall time | t_{CHCL} | - | 20 | ns |

AC Characteristics (cont'd)

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$;

$T_A = 0\text{ to }70\text{ }^\circ\text{C}$; (SAB 80C52-16/80C32-16)

$T_A = -40\text{ to }85\text{ }^\circ\text{C}$; (SAB 80C52-16/80C32-16 – T40/85)

$T_A = -40\text{ to }110\text{ }^\circ\text{C}$; (SAB 80C52-16/80C32-16 – T40/110)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

| Parameter | Symbol | Limit values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 16 MHz clock | | Variable clock $1/t_{\text{CLCL}} = 0.5\text{ MHz to }16\text{ MHz}$ | | |
| | | min | max. | min. | max. | |

Program Memory Characteristics

| | | | | | | |
|--|----------------------|-----|-----|--------------------------|---------------------------|----|
| ALE pulse width | t_{LHLL} | 85 | – | $2 t_{\text{CLCL}} - 40$ | – | ns |
| Address setup to ALE | t_{AVLL} | 23 | – | $t_{\text{CLCL}} - 40$ | – | ns |
| Address hold after ALE | t_{LLAX} | 40 | – | $t_{\text{CLCL}} - 23$ | – | ns |
| Address to valid instruction in | t_{LLIV} | – | 233 | – | $4 t_{\text{CLCL}} - 100$ | ns |
| ALE to $\overline{\text{PSEN}}$ | t_{LLPL} | 38 | – | $t_{\text{CLCL}} - 25$ | – | ns |
| $\overline{\text{PSEN}}$ pulse width | t_{PLPH} | 153 | – | $3 t_{\text{CLCL}} - 35$ | – | ns |
| $\overline{\text{PSEN}}$ to valid instruction in | t_{PLIV} | – | 150 | – | $3 t_{\text{CLCL}} - 100$ | ns |
| Input instruction hold after $\overline{\text{PSEN}}$ | t_{PXIX} | 0 | – | 0 | – | ns |
| Input instruction float after $\overline{\text{PSEN}}$ | t_{PXIZ} | – | 63 | – | $t_{\text{CLCL}} - 15$ | ns |
| Address valid after $\overline{\text{PSEN}}$ | $t_{\text{PXAV}^*)}$ | 60 | – | $t_{\text{CLCL}} - 3$ | – | ns |
| Address to valid instruction in | $t_{\text{AVIV}^*)}$ | – | 302 | 0 | $5 t_{\text{CLCL}} - 90$ | ns |
| Address float to $\overline{\text{PSEN}}$ | t_{PLAZ} | – | 0 | – | 0 | ns |

*) Interfacing the SAB 80C52-16/80C32-16 to devices with float times up to 45 ns permissible.

This limited bus contention will not cause any damage to port 0 drivers

AC Characteristics (cont'd)

| Parameter | Symbol | Limit values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 16 MHz clock | | Variable clock 1/ t_{CLCL} = 0.5 MHz to 16 MHz | | |
| | | min. | max. | min. | max. | |

External Data Memory Characteristics

| | | | | | | |
|---|-------------|-----|-----|--------------------|--------------------|----|
| \overline{RD} pulse width | t_{RLRH} | 275 | – | 6 t_{CLCL} – 100 | – | ns |
| \overline{WR} pulse width | t_{WLWH} | 275 | – | 6 t_{CLCL} – 100 | – | ns |
| Address hold after ALE | t_{LLAX2} | 90 | – | 2 t_{CLCL} – 35 | – | ns |
| \overline{RD} to valid data in | t_{RLDV} | – | 148 | – | 5 t_{CLCL} – 165 | ns |
| Data hold after \overline{RD} | t_{RHDX} | 0 | – | 0 | – | ns |
| Data float after \overline{RD} | t_{RHDZ} | – | 55 | – | 2 t_{CLCL} – 70 | ns |
| ALE to valid data in | t_{LLDV} | – | 350 | – | 8 t_{CLCL} – 150 | ns |
| Address to valid data in | t_{AVDV} | – | 398 | – | 9 t_{CLCL} – 165 | ns |
| ALE to \overline{WR} or \overline{RD} | t_{LLWL} | 138 | 238 | 3 t_{CLCL} – 50 | 3 t_{CLCL} + 50 | ns |
| Address valid to \overline{WR} or \overline{RD} | t_{AVWL} | 120 | – | 4 t_{CLCL} – 130 | – | ns |
| \overline{WR} or \overline{RD} high to ALE high | t_{WHLH} | 23 | 103 | t_{CLCL} – 40 | t_{CLCL} + 40 | ns |
| Data valid to \overline{WR} transition | t_{QVWX} | 13 | – | t_{CLCL} – 50 | – | ns |
| Data setup before \overline{WR} | t_{QVWX} | 288 | – | 7 t_{CLCL} – 150 | – | ns |
| Data hold after \overline{WR} | t_{WHQX} | 13 | – | t_{CLCL} – 50 | – | ns |
| Address float after \overline{RD} | t_{RLAZ} | – | 0 | – | 0 | ns |

AC Characteristics (cont'd)

| Parameter | Symbol | Limit values | | Unit |
|-----------|--------|--|------|------|
| | | Variable clock Frequ. = 0.5 MHz to 16 MHz | | |
| | | min | max. | |

External Clock Drive XTAL1

| | | | | |
|-------------------|------------|------|-----------------------|----|
| Oscillator period | t_{CLCL} | 62.5 | 2000 | ns |
| High time | t_{CHCX} | 15 | $t_{CLCL} - t_{CHCX}$ | ns |
| Low time | t_{CLCX} | 15 | $t_{CLCL} - t_{CHCX}$ | ns |
| Rise time | t_{CLCH} | - | 15 | ns |
| Fall time | t_{CHCL} | - | 15 | ns |

AC Characteristics (cont'd)

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$;

$T_A = 0\text{ to }70\text{ }^\circ\text{C}$; (SAB 80C52-20/80C32-20)

$T_A = -40\text{ to }85\text{ }^\circ\text{C}$; (SAB 80C52-20/80C32-20 – T40/85)

$T_A = -40\text{ to }110\text{ }^\circ\text{C}$; (SAB 80C52-20/80C32-20 – T40/110)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

| Parameter | Symbol | Limit values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 20 MHz clock | | Variable clock 1/ $t_{CLCL} = 0.5\text{ MHz to }20\text{ MHz}$ | | |
| | | min | max. | min. | max. | |

Program Memory Characteristics

| | | | | | | |
|--|---------------|-----|-----|-------------------|--------------------|----|
| ALE pulse width | t_{LHLL} | 60 | – | $2 t_{CLCL} - 40$ | – | ns |
| Address setup to ALE | t_{AVLL} | 20 | – | $t_{CLCL} - 30$ | – | ns |
| Address hold after ALE | t_{LLAX} | 20 | – | $t_{CLCL} - 30$ | – | ns |
| Address to valid instruction in | t_{LLIV} | – | 100 | – | $4 t_{CLCL} - 100$ | ns |
| ALE to $\overline{\text{PSEN}}$ | t_{LLPL} | 25 | – | $t_{CLCL} - 25$ | – | ns |
| $\overline{\text{PSEN}}$ pulse width | t_{PLPH} | 115 | – | $3 t_{CLCL} - 35$ | – | ns |
| $\overline{\text{PSEN}}$ to valid instruction in | t_{PLIV} | – | 75 | – | $3 t_{CLCL} - 75$ | ns |
| Input instruction hold after $\overline{\text{PSEN}}$ | t_{PXIX} | 0 | – | 0 | – | ns |
| Input instruction float after $\overline{\text{PSEN}}$ | t_{PXIZ} | – | 40 | – | $t_{CLCL} - 10$ | ns |
| Address valid after $\overline{\text{PSEN}}$ | $t_{PXAV}^*)$ | 47 | – | $t_{CLCL} - 3$ | – | ns |
| Address to valid instruction in | $t_{AVIV}^*)$ | – | 190 | 0 | $5 t_{CLCL} - 60$ | ns |
| Address float to $\overline{\text{PSEN}}$ | t_{PLAZ} | – | 10 | – | 0 | ns |

*) Interfacing the SAB 80C52-20/80C32-20 to devices with float times up to 45 ns permissible.

This limited bus contention will not cause any damage to port 0 drivers

AC Characteristics (cont'd)

| Parameter | Symbol | Limit values | | | | Unit |
|-----------|--------|--------------|------|--|------|------|
| | | 20 MHz clock | | Variable clock 1/ $t_{CLCL} = 0.5 \text{ MHz to } 20 \text{ MHz}$ | | |
| | | min | max. | min. | max. | |

External Data Memory Characteristics

| | | | | | | |
|---|-------------|-----|-----|--------------------|--------------------|----|
| \overline{RD} pulse width | t_{RLRH} | 200 | - | $6 t_{CLCL} - 100$ | - | ns |
| \overline{WR} pulse width | t_{WLWH} | 200 | - | $6 t_{CLCL} - 100$ | - | ns |
| Address hold after ALE | t_{LLAX2} | 65 | - | $2 t_{CLCL} - 35$ | - | ns |
| \overline{RD} to valid data in | t_{RLDV} | - | 85 | - | $5 t_{CLCL} - 165$ | ns |
| Data hold after \overline{RD} | t_{RHDX} | 0 | - | 0 | - | ns |
| Data float after \overline{RD} | t_{RHDZ} | - | 40 | - | $2 t_{CLCL} - 60$ | ns |
| ALE to valid data in | t_{LLDV} | - | 250 | - | $8 t_{CLCL} - 150$ | ns |
| Address to valid data in | t_{AVDV} | - | 285 | - | $9 t_{CLCL} - 165$ | ns |
| ALE to \overline{WR} or \overline{RD} | t_{LLWL} | 100 | 200 | $3 t_{CLCL} - 50$ | $3 t_{CLCL} + 50$ | ns |
| Address valid to \overline{WR} or \overline{RD} | t_{AVWL} | 70 | - | $4 t_{CLCL} - 130$ | - | ns |
| \overline{WR} or \overline{RD} high to ALE high | t_{WHLH} | 20 | 80 | $t_{CLCL} - 30$ | $t_{CLCL} + 30$ | ns |
| Data valid to \overline{WR} transition | t_{QVWX} | 5 | - | $t_{CLCL} - 45$ | - | ns |
| Data setup before \overline{WR} | t_{QVWX} | 200 | - | $7 t_{CLCL} - 150$ | - | ns |
| Data hold after \overline{WR} | t_{WHQX} | 10 | - | $t_{CLCL} - 40$ | - | ns |
| Address float after \overline{RD} | t_{RLAZ} | - | 0 | - | 0 | ns |

AC Characteristics (cont'd)

| Parameter | Symbol | Limit values | | Unit |
|-----------|--------|--|------|------|
| | | Variable clock Frequ. = 0.5 MHz to 20 MHz | | |
| | | min | max. | |

External Clock Drive XTAL1

| | | | | |
|-------------------|------------|----|-----------------------|----|
| Oscillator period | t_{CLCL} | 50 | 2000 | ns |
| High time | t_{CHCX} | 12 | $t_{CLCL} - t_{CHCX}$ | ns |
| Low time | t_{CLCX} | 12 | $t_{CLCL} - t_{CHCX}$ | ns |
| Rise time | t_{CLCH} | - | 12 | ns |
| Fall time | t_{CHCL} | - | 12 | ns |

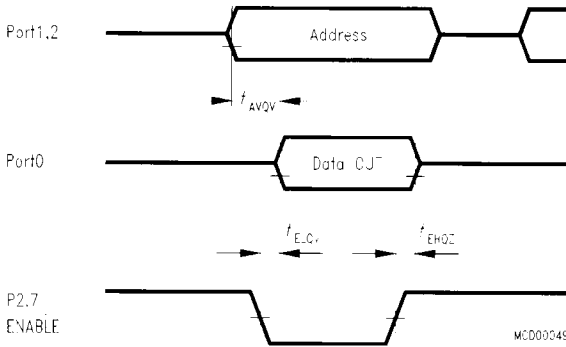
ROM Verification Characteristics

$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$; $V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Limit values | | Unit |
|-----------|--------|--------------|------|------|
| | | min | max. | |

ROM Verification

| | | | | |
|---|--------------|---|---------------|-----|
| Address to valid data | t_{AVQV} | – | $48 t_{CLCL}$ | ns |
| $\overline{\text{ENABLE}}$ to valid data | t_{ELQV} | – | $48 t_{CLCL}$ | ns |
| Data float after $\overline{\text{ENABLE}}$ | t_{EHOZ} | 0 | $48 t_{CLCL}$ | ns |
| Oscillator frequency | $1/t_{CLCL}$ | 4 | 6 | MHz |

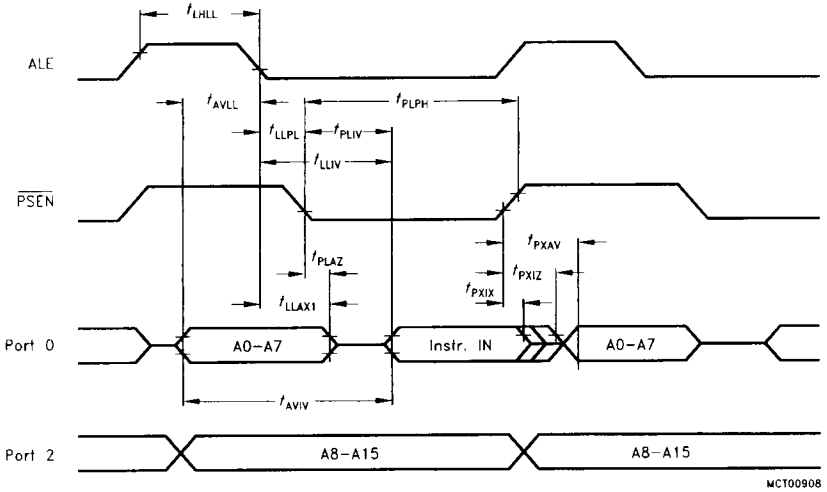


Address: P1.0–P1.7 = A0–A7
 P2.0–P2.4 = A8–A12
 Data: Port 0 = D0–D7

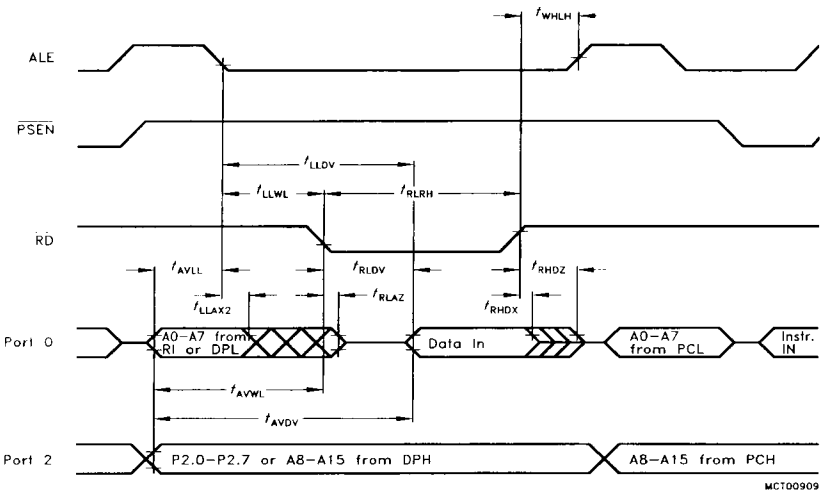
Inputs: P2.5–P2.6, $\overline{\text{PSEN}}$ = V_{SS}
 ALE, $\overline{\text{EA}}$ = V_{IH}
 RST = V_{IH1}

ROM Verification

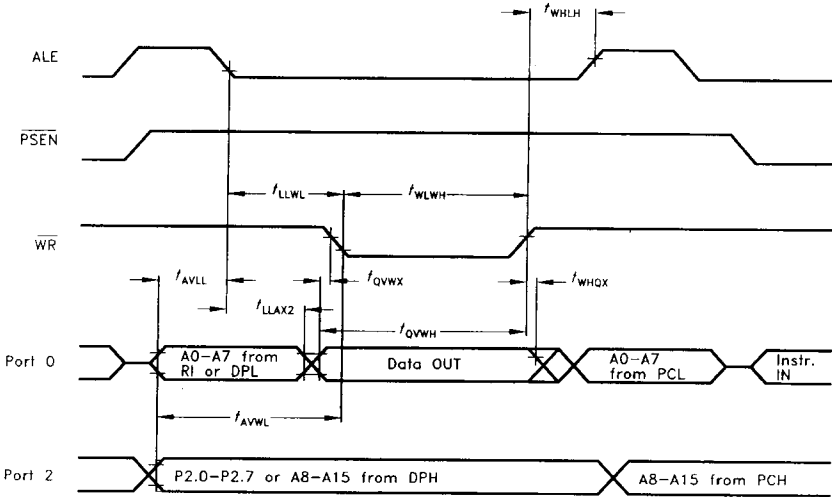
Waveforms



Program Memory Read Cycle

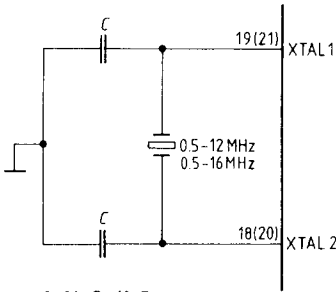


Data Memory Read Cycle



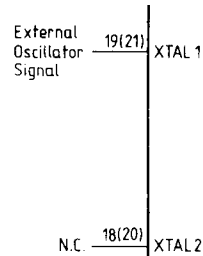
MCT00910

Data Memory Write Cycle



$C = 30 \text{ pF} \pm 10 \text{ pF}$

Crystal Oscillator Mode

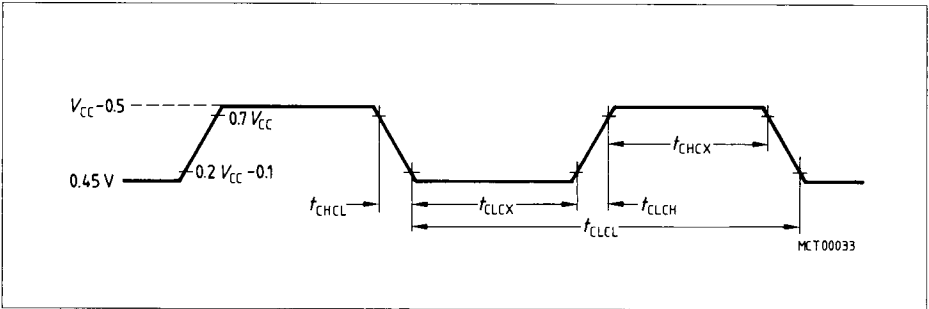


MCS00911

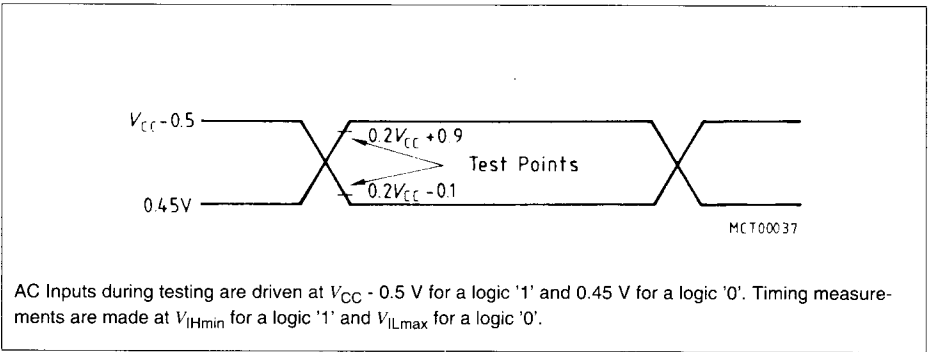
Driving from External Source

Pin numbers in (. .) are for PL-CC-44 package

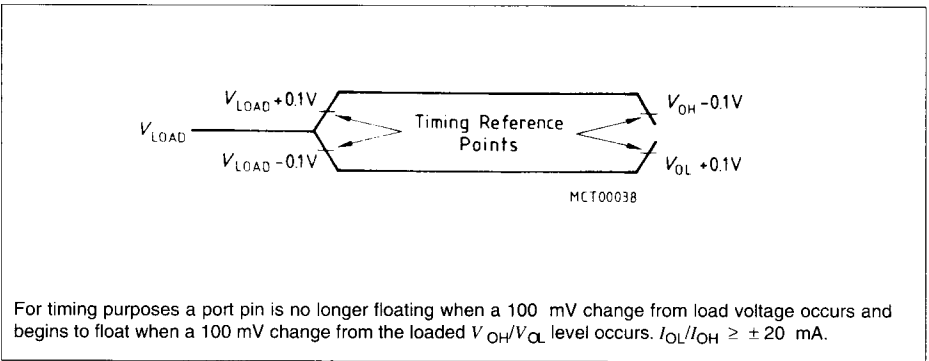
Recommended Oscillator Circuits



External Clock Cycle



AC Testing: Input, Output Waveforms



AC Testing: Float Waveforms