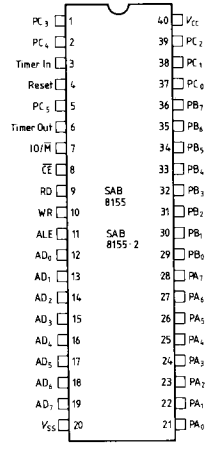
SIEMENS

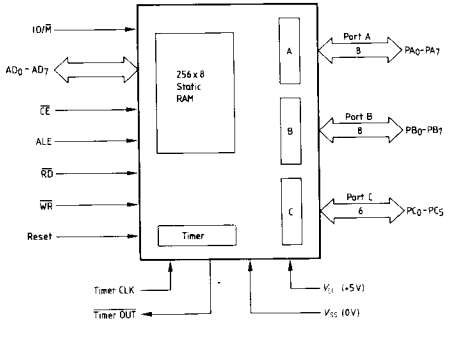
SAB 8155, SAB 8155-2 2048 Bit Static MOS RAM with I/O Ports and Timer

- 256 Word × 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8-Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with SAB 8085A and SAB 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

Pin Configuration



Block Diagram



The SAB 8155 is a RAM and I/O chip to be used in the SAB 8085A and SAB 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256×8. They have a maximum access time of 400ns to permit use with no wait states in SAB 8085A CPU. The SAB 8155-2 has a maximum access time of 330ns for use with the SAB 8085A-2 and the full speed 5MHz SAB 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
PC$\emptyset$–PC5	1, 2, 5, 37–39	I/O	PORT C – These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC$\emptyset$-PC5 are used as control signals, they will provide the following: PC$\emptyset$ – A INTR (Port A Interrupt) PC1 – ABF (Port A Buffer Full) PC2 – $\overline{\text{A STB}}$ (Port A Strobe) PC3 – B INTR (Port B Interrupt) PC4 – B BF (Port B Buffer Full) PC5 – $\overline{\text{B STB}}$ (Port B Strobe)
TIMER IN	3	I	TIMER INPUT – Input to the counter/timer.
RESET	4	I	RESET – Pulse provided by the SAB 8085A to initialize the system (connect to SAB 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two SAB 8085A clock cycle times.
$\overline{\text{TIMER OUT}}$	6	O	TIMER OUTPUT – This output can be either a square wave or a pulse, depending on the timer mode.
IO/$\overline{\text{M}}$	7	I	I/O MEMORY – Selects memory if low and I/O and command/status registers if high.
$\overline{\text{CE}}$	8	I	CHIP ENABLE – On this SAB 8155, this pin is $\overline{\text{CE}}$ and is ACTIVE LOW.
$\overline{\text{RD}}$	9	I	READ CONTROL – Input low on this line with the Chip Enable active enables and AD$\emptyset$–AD7 buffers. If IO/$\overline{\text{M}}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{\text{WR}}$	10	I	WRITE CONTROL – Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{\text{M}}$.
ALE	11	I	ADDRESS LATCH ENABLE – This control signal latches both the address on the AD$\emptyset$–AD7 lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.
AD$\emptyset$–AD7	12–19	I/O	ADDRESS/DATA – 3-state Address/Data lines that interface with the CPU lower 8-bit Address-Data Bus. The 8-bit address is latched into the address latch inside the SAB 8155 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{\text{M}}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{\text{WR}}$ or $\overline{\text{RD}}$ input signal.

Symbol	Number	Input (I) Output (O)	Function
PAØ–PA7	21–28	I/O	PORT A – These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PBØ–PB7	29–36	I/O	PORT B – These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
V_{CC}	40		POWER SUPPLY (+5V)
V_{SS}	20		GROUND (0 V)

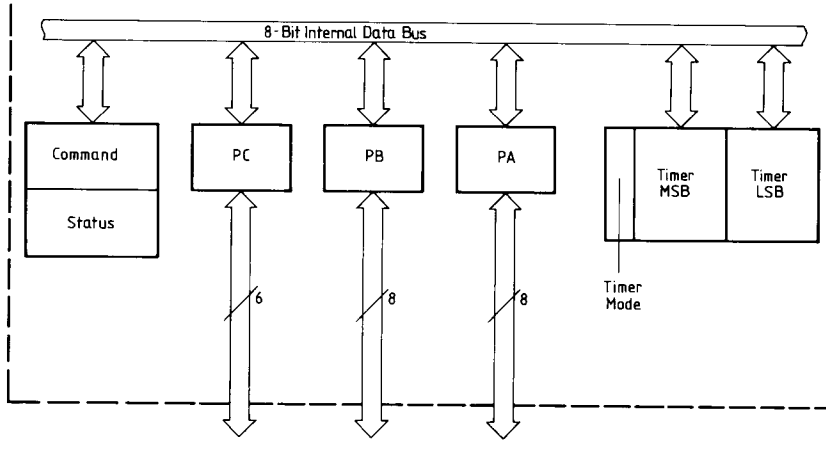
Functional Description

The SAB 8155 contains the following:

- 2Kbit Static RAM organized as 256×8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA0–PA7, PB0–PB7, PC0–PC5) or the memory (RAM) portion.

SAB 8155 Internal Registers



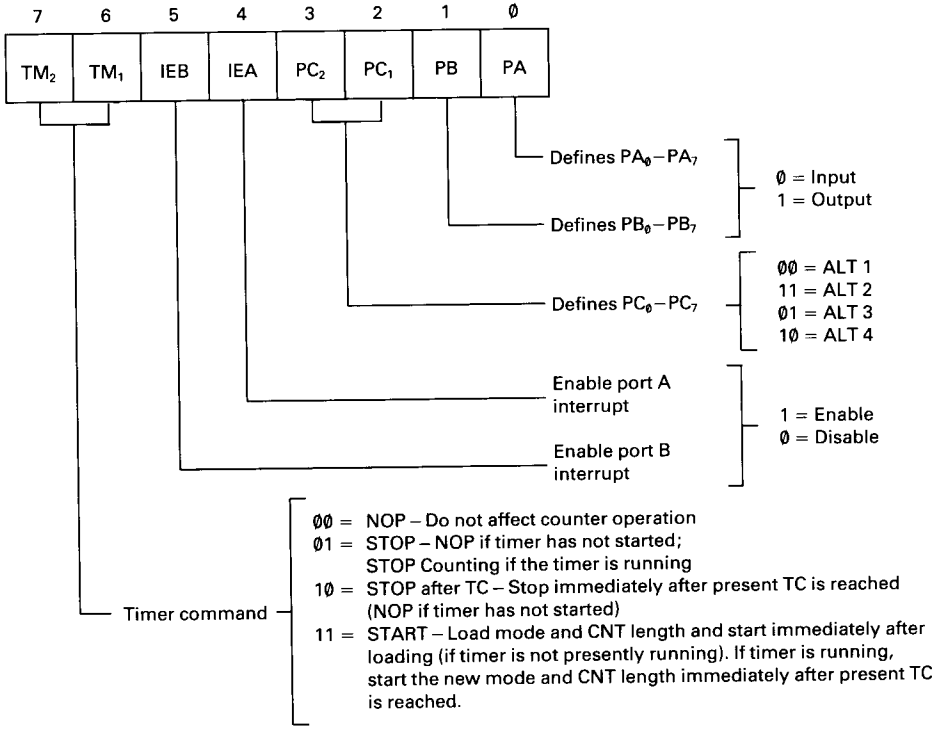
The 8-bit address on the Address/Data lines, Chip Enable input $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

Programming of the Command Register

The command register consists of eight latches. Four bits (Ø–3) define the mode of the ports, two bits (4–5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6–7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXXØØØ during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in the following figure. The contents of the command register may never be read.

Command Register Bit Assignment

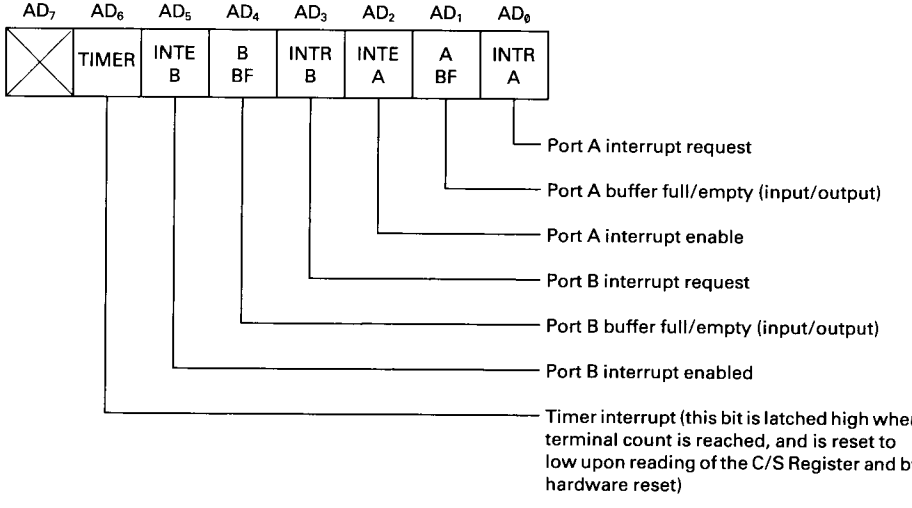


Reading the Status Register

The status register consists of seven latches, one for each bit; six (Ø–5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polles by reading the Status Register (Address XXXXXØØØ). Status word format is shown in the following figure. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

Status Register Bit Assignment



Input/Output Section

The I/O section of the SAB 8155 consists of five registers (see following figure):

- **Command/Status Register (C/S)** – Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are **not** accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD0–AD7 lines.

- **PA Register** – This register can be programmed to be either input or – output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (see timing diagram). The I/O pins assigned in relation to this register are PA0–PA7. The address of this register is XXXXX001.

- **PB Register** – This register functions the same as PA Register. The I/O pins assigned are PB0–PB7. The address of this register is XXXXX010.

- **PC Register** – This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA und PB by properly programming the AD2 and AD3 bits of the C/S register.

  When PC0–PC5 is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the SAB 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode (see table Port Control Assignment).

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

Control	Input Mode	Output Mode
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

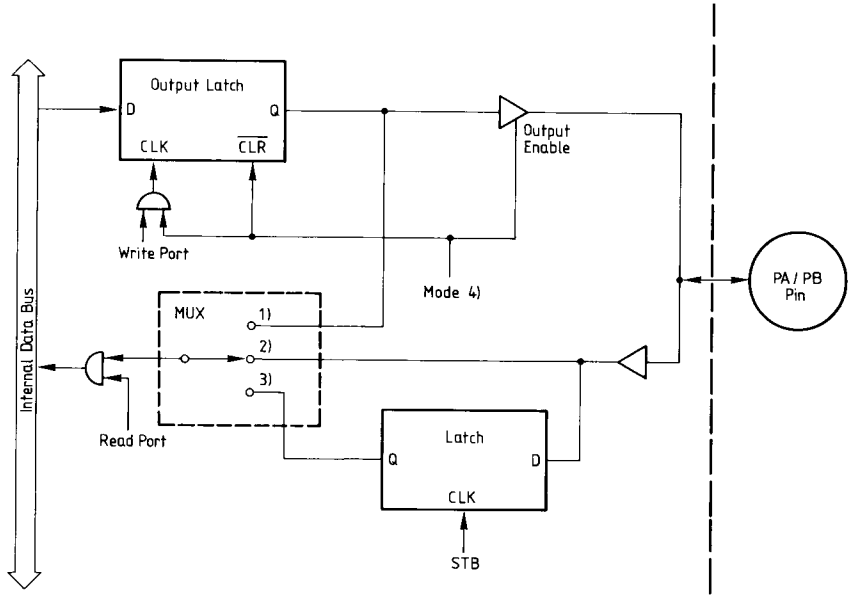
I/O Port and Timer Addressing Scheme

I/O Address *								Selection
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Interval Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	Port C – General Purpose I/O or Control
X	X	X	X	X	1	0	0	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	0	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care.
*: I/O Address must be qualified by $\overline{CE}$ = 0 and IO/$\overline{M}$ = 1 in order to select the appropriate register.

The following figure shows how I/O PORTS A and B are structured within the SAB 8155:

SAB 8155 Port Functions



Control

Notes:

1) Output Mode
2) Simple Input
3) Strobed Input

} Multiplexer Control

4) = 1 for Output Mode
= Ø for Input Mode

Read Port = (IO/$\overline{M}$ = 1) × ($\overline{RD}$ = Ø) × (CE Active) × (Port Address selected)
Write Port = (IO/$\overline{M}$ = 1) × ($\overline{WR}$ = Ø) × (CE Active) × (Port Address selected)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the SAB 8155 are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the SAB 8155 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

Port Control Assignment

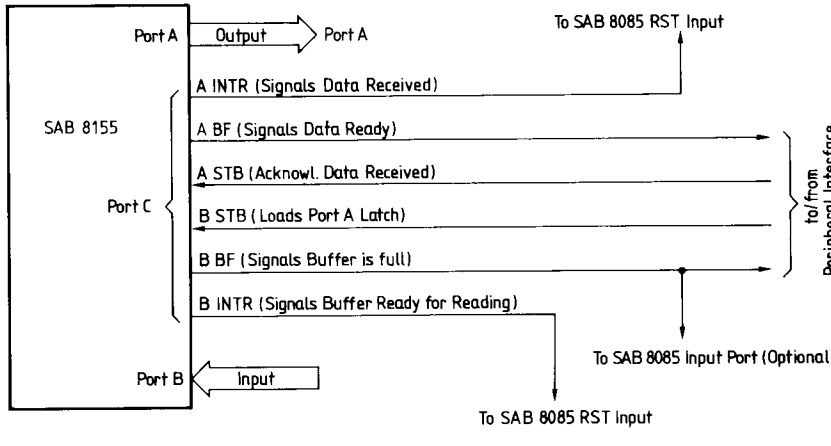
Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{\text{STB}}$ (Port A Strobe)	A $\overline{\text{STB}}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{\text{STB}}$ (Port B Strobe)

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Next figure shows how the SAB 8155 I/O ports might be configured in a typical SAB 8085 system.

Example: Command Register = 00111001



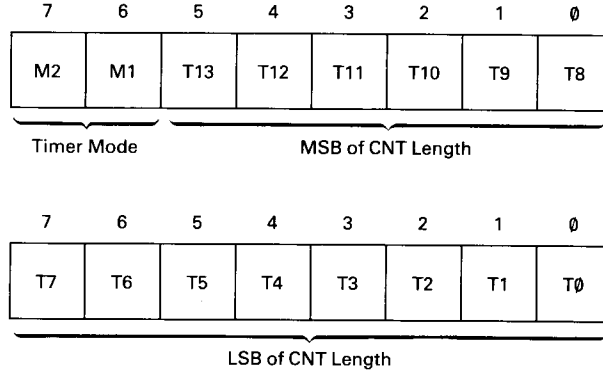
Timer Section

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register (see figure I/O Port and Timer Addressing Scheme).

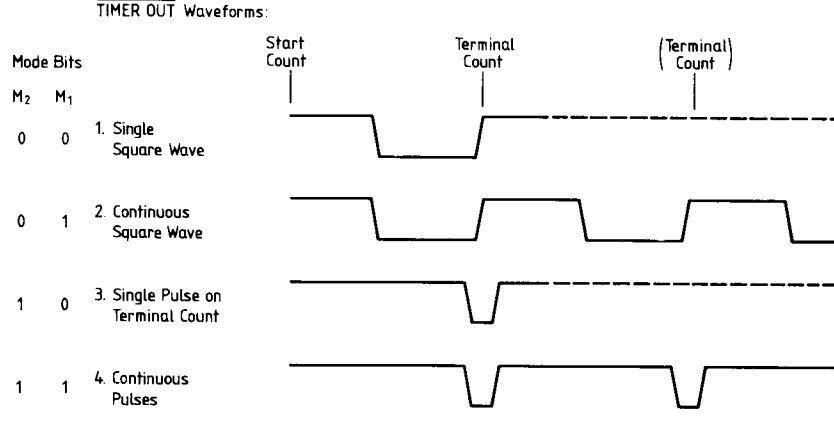
To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0–13 of the high order count register will specify the length of the next count and bits 14–15 of the high order register will specify the timer output mode (see next figure). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0–13.

Timer Format



There are four modes to choose from: M2 and M1 define the timer mode, as shown in following figure.

Timer Modes



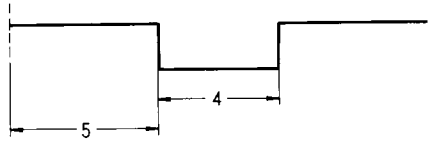
Bits 6–7 (TM2 and TM1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM2	TM1	Function
Ø	Ø	NOP – Do not affect counter operation
Ø	1	STOP – NOP if timer has not startet; stop counting if the timer is running
1	Ø	STOP AFTER TC – Stop immediately after present TC is reached (NOP if timer has not startet)
1	1	START – Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you **must** issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in next figure.

Asymmetrical Square-Wave Output Resulting from Count of 9



Note: 5 and 4 refer to the number of clocks in that time period

The counter in the SAB 8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the SAB 8155 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the SAB 8085A be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To abtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set. add ½ of the full original count (½ full count – 1 if full count is odd)

Note:
If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts have occured. Regardless of this, the SAB 8155 always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

Absolute maximum ratings *)

Temperature Under Bias	0 to +70°C
Storage Temperature	−65 to +150°C
Voltage on any Pin with Respect to Ground	−0.5 to +7V
Power Dissipation	1.5 Watt

D.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5V ±5%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5		
V_{OL}	Output Low Voltage	–	0.45		I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH} = −400 µA
I_{IL}	Input Leakage	–	±10	µA	$V_{IN} = V_{CC}$ to 0V
I_{LO}	Output Leakage				0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	–
I_{IL} (CE)	Chip Enable Leakage		+100	µA	$V_{IN} = V_{CC}$ to 0V

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

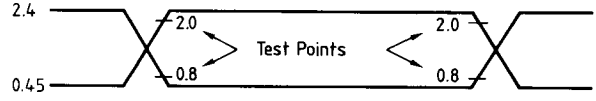
A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 5%

Symbol	Parameter	Limit Values				Units
		SAB 8155		SAB 8155-2		
		Min.	Max.	Min.	Max.	
t_{AL}	Address to Latch Set Up Time	50				
t_{LA}	Address Hold Time after Latch	80	–	30	–	
t_{LC}	Latch to READ/WRITE Control	100		40		
t_{RD}	Valid Data Out Delay from READ Control	–	170	–	140	
t_{AD}	Address Stable to Data Out Valid		400		330	
t_{LL}	Latch Enable Width	100	–	70	–	
t_{RDF}	Data Bus Float After READ	0	100	0	80	
t_{CL}	READ/WRITE Control to Latch Enable	20		10		
t_{CC}	READ/WRITE Control Width	250		200		
t_{DW}	Data In to WRITE Set Up Time	150	–	100	–	
t_{WD}	Data In Hold Time After WRITE	0		0		
t_{RV}	Recovery Time Between Controls	300		200		
t_{WP}	WRITE to Port Output	–	400	–	300	ns
t_{PR}	Port Input Setup Time	70	–	50	–	
t_{RP}	Port Input Hold Time	50	–	10	–	
t_{SBF}	Strobe to Buffer Full	–	400	–	300	
t_{SS}	Strobe Width	200	–	150	–	
t_{RBE}	READ to Buffer Empty					
t_{SI}	Strobe to INTR ON	–	400	–	300	
t_{RDI}	READ to INTR Off					
t_{PSS}	Port Setup Time to Strobe Strobe	50	–	0	–	
t_{PHS}	Port Hold Time After Strobe	120		100		
t_{SBE}	Strobe to Buffer Empty					
t_{WBF}	WRITE to Buffer Full					
t_{WI}	WRITE to INTR Off	–	400	–	300	
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low					
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High					
t_{RDE}	Data Bus Enable from READ Control	10		10		
t_1	TIMER-IN Low Time	80	–	40	–	
t_2	TIMER-IN High Time	120		70		

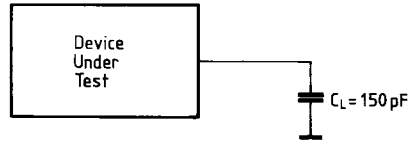
A.C. Testing

Input/Output Waveform



A.C. Testing: Input are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0".
Timing Measurements are made at 2.0 V for Both a Logic "1" and 0.8 V for a Logic "0".

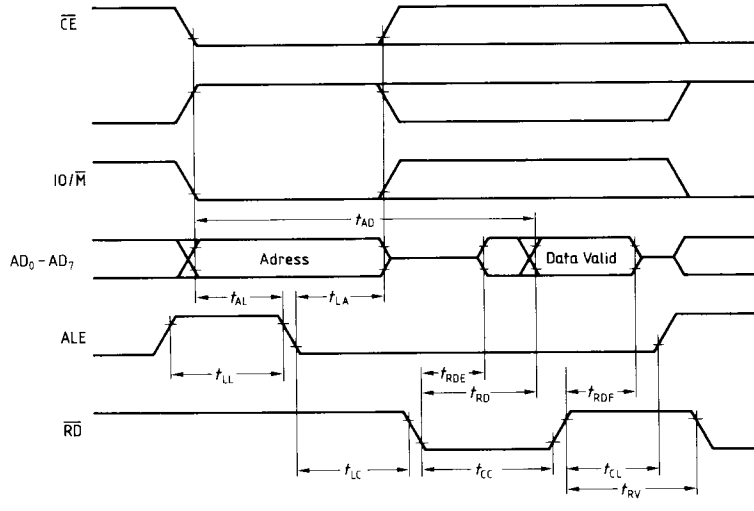
Load Circuit



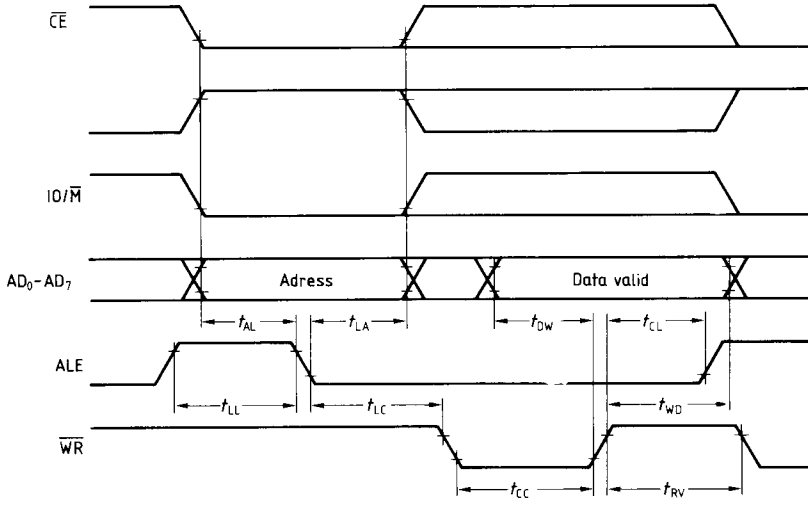
C_L = 150 pF
C_L = Includes JIG Capacitance

Waveforms

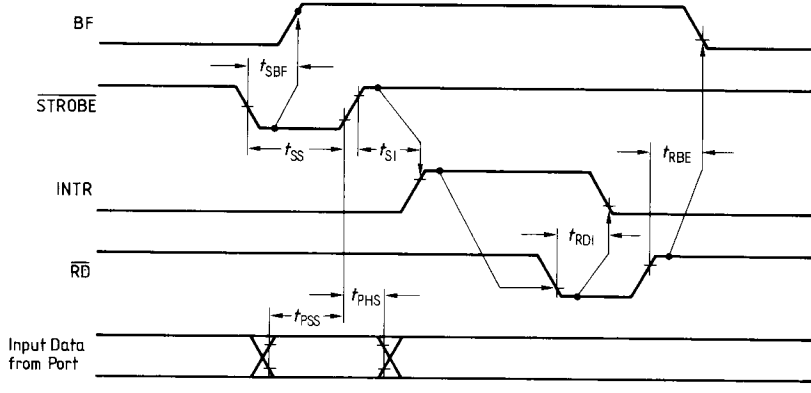
Read Cycle



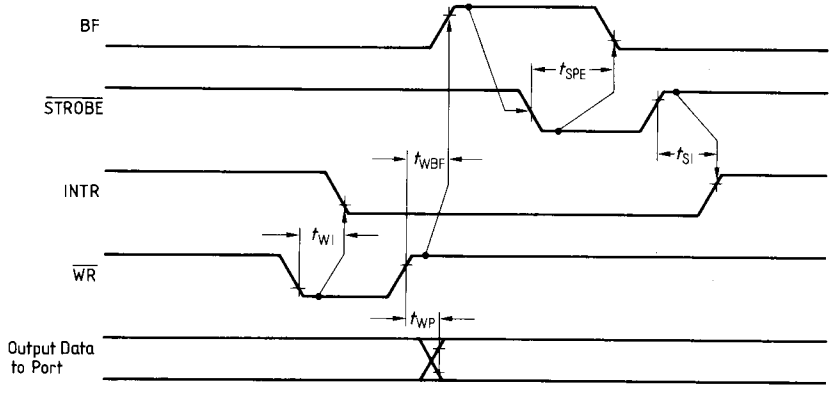
Write Cycle



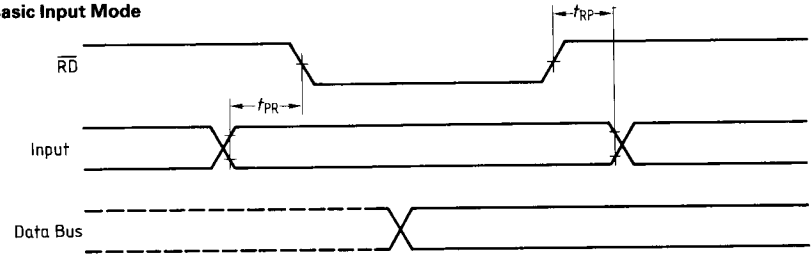
Strobed Input Mode



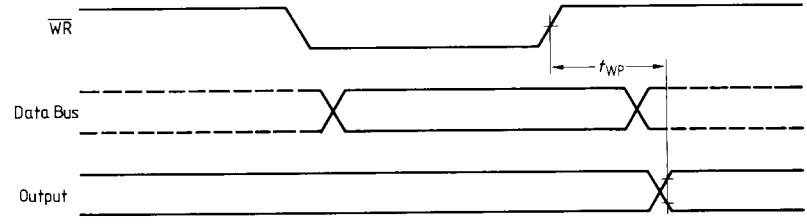
Strobed Output Mode



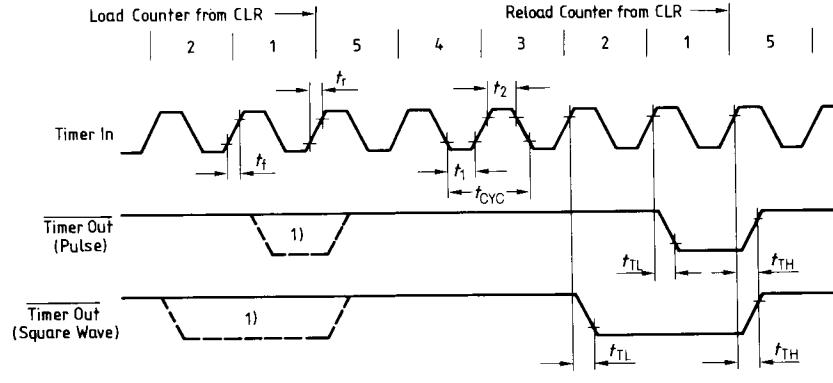
Basic Input Mode



Basic Output Mode



Timer Output Countdown from 5 to 1



1) The Timer Output is periodic if an automatic reload Mode (M1 Mode Bit = 1)

Ordering Description

Type	Description	Ordering Number
	RAM with I/O Port and Timer	
SAB 8155-C	Ceramic	Q 67120–Q 43
SAB 8155-P	Plastic	Q 67120–Q 42
SAB 8155-2-C	Ceramic	Q 67120–Q 85
SAB 8155-2-P	Plastic	Q 67120–Q 86