SIEMENS

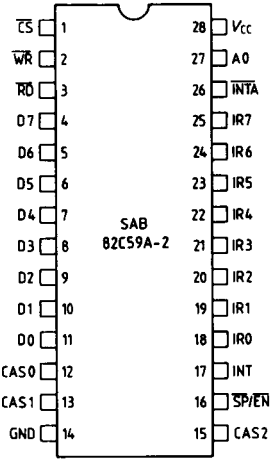
CMOS Programmable Interrupt Controller

SAB 82C59A-2

Preliminary

- Compatible with NMOS and CMOS 8085A, SAB 8086/8088, SAB 80186/80188, SAB 80286 and 80386 processor families
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Fully static design
- Low standby power dissipation
- Compatible with the industry standard NMOS SAB 8259A-2

Pin Configuration



Pin Names

D7-D0	Data Bus (bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS2-CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Program/Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0-IR7	Interrupt Request Inputs

The SAB 82C59A-2 Programmable Interrupt Controller is a high-performance CMOS version of the NMOS SAB 8259A-2. The SAB 82C59A-2 is fabricated in Siemens ACMOS technology and compatible with the industry standard 8259A.
The SAB 82C59A-2 handles up to 8 vectored interrupts to the CPU. It is designed to minimize the software and real-time overhead in handling multilevel priority interrupts. It offers several modes, permitting optimization for a variety of system requirements. Packaged in a 28-pin plastic dual-in-line package, the SAB 82C59A-2 as a static CMOS circuit insures low operating power.

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Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{CS}$	1	I	$\overline{CHIP\ SELECT}$ A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the SAB 82C59A-2. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	$\overline{WRITE}$ A low on this pin, when $\overline{CS}$ is low, enables the SAB 82C59A-2 to accept command words from the CPU.
$\overline{RD}$	3	I	$\overline{READ}$ A low on this pin, when $\overline{CS}$ is low, enables the SAB 82C59A-2 to release status onto the data bus for the CPU.
D7-D0	4-11	I/O	BIDIRECTIONAL DATA BUS Control, status, and interrupt vector information is transferred via this bus.
CAS0-CAS2	12, 13, 15	I/O	CASCADE LINES The CAS lines form a private SAB 82C59A-2 bus to control a multiple SAB 82C59A-2 structure. These pins are outputs for a master SAB 82C59A-2 and inputs for a slave SAB 82C59A-2.
$\overline{SP}/\overline{EN}$	16	I/O	$\overline{SLAVE\ PROGRAM}/\overline{ENABLE\ BUFFER}$ This is a dual-function pin. When in buffered mode it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in buffered mode it is used as an input to designate a master ($\overline{SP}$ = 1) or slave ($\overline{SP}$ = 0).
INT	17	O	INTERRUPT This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU and is, therefore, connected to the CPU's interrupt pin.
IR0-IR7	18-25	I	INTERRUPT REQUESTS These are asynchronous inputs. An interrupt request can be generated by raising an IR input (low to high) and holding it high until it is acknowledged (edge-triggered mode), or just by a high level on an IR input (level-triggered mode).
$\overline{INTA}$	26	I	$\overline{INTERRUPT\ ACKNOWLEDGE}$ This pin is used to enable SAB 82C59A-2 interrupt vector data onto the data bus. This is done by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	A0 ADDRESS LINE This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. It is used by the SAB 82C59A-2 to distinguish between various command words written by the CPU and the status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for SAB 8086/80186/80286).
V_{CC}	28	–	POWER SUPPLY (+5 V)
GND	14	–	GROUND (0 V)

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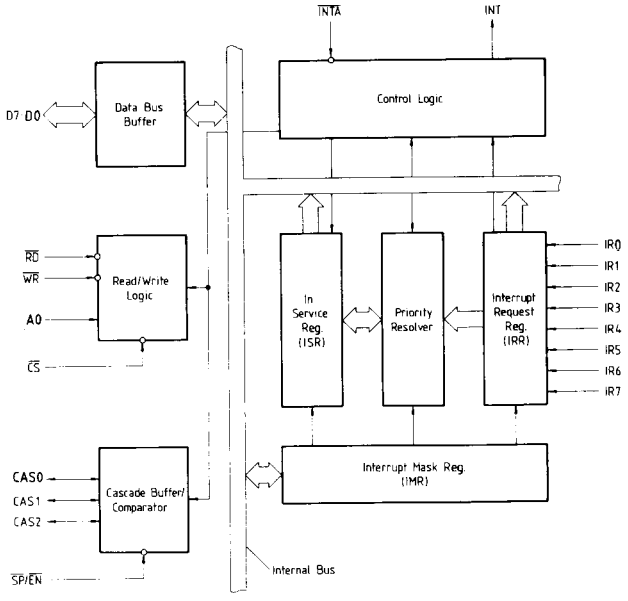
Functional Block Diagram



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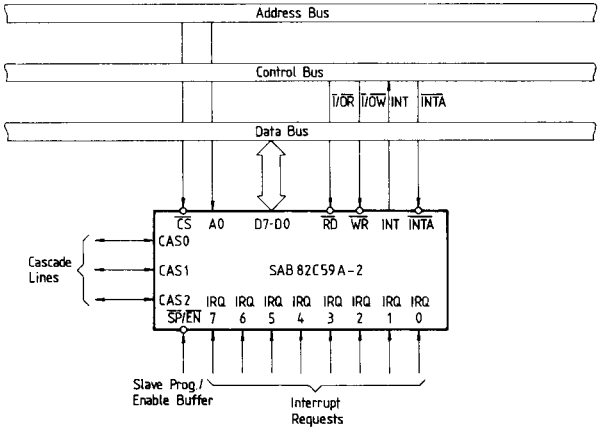
Interface to Standard System Bus



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Functional Description

General

The SAB 82C59A-2 is a device specifically designed for use in real-time, interrupt-driven microcomputer systems. It manages eight levels of requests and has built-in features for expandability to other SAB 82C59A-2 devices (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the SAB 82C59A-2 can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two cascaded registers: the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced.

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Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during an $\overline{INTA}$ pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines. The IMR operation is based on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the SAB 8085A/8086/8088/80186/80188/80286 and 80386.

$\overline{INTA}$ (Interrupt Acknowledge)

$\overline{INTA}$ pulses will cause the SAB 82C59A-2 to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the SAB 82C59A-2.

Data Bus Buffer

This tristate, bidirectional 8-bit buffer is used to interface the SAB 82C59A-2 to the system data bus. Control words and status information are transferred through the data bus buffer.

Read/Write Control Logic

The function of this block is to accept output commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the SAB 82C59A-2 to be transferred onto the data bus.

$\overline{CS}$ (Chip Select)

A low on this input enables the SAB 82C59A-2. No reading or writing of the chip will occur unless the device has been selected.

$\overline{WR}$ (Write)

A low on this input enables the CPU to write control words (ICWs and OCWs) to the SAB 82C59A-2.

$\overline{RD}$ (Read)

A low on this input enables the SAB 82C59A-2 to send the status of the Interrupt Request Register (IRR), the In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the data bus.

A0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as to read the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all SAB 82C59A-2 devices used in the system. The associated three I/O pins (CAS0-2) are outputs when the SAB 82C59A-2 is used as a master and are inputs when the SAB 82C59A-2 is used as a slave. As a master, the SAB 82C59A-2 sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the data bus during the next one or two consecutive $\overline{INTA}$ pulses.

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Interrupt Sequence

The powerful features of the SAB 82C59A-2 in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

In an SAB 8085A system the events occur as follows:

1. One or more of the interrupt request lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The SAB 82C59A-2 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The SAB 82C59A-2 will also release a "call" instruction code (11001101) onto the 8-bit data bus through its D7-0 pins.
5. This "call" instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the SAB 82C59A-2 from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the SAB 82C59A-2 to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte "call" instruction released by the SAB 82C59A-2. In the AEOI (automatic end of interrupt) mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an SAB 8086/8088/80186/80188/80286 or 80386 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The SAB 82C59A-2 does not drive the data bus during this cycle.
5. The CPU will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the SAB 82C59A-2 releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request duration was too short), the SAB 82C59A-2 will issue an interrupt level 7. Both, the vectoring bytes and the CAS lines will look as if an interrupt level 7 was requested.

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Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to V_{CC}+0.5 V
Supply voltage with respect to ground	−0.5 to 7.0 V
Power dissipation	1 W

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; GND = 0V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage	2.2	V_{CC} +0.5	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} −0.4	–	V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{LI}	Interrupt leakage current	–	±1	µA	0 V < V_{IN} < V_{CC}
I_{LOL}	Output leakage current	–	±10	µA	0 V < V_{OUT} < V_{CC}
I_{LIR}	IR input leakage current	–	−300 +10	µA	V_{IN} = 0 V V_{IN} = V_{CC}
I_{CC}	Operating supply current	–	5	mA	[2]
I_{CCS}	Standby supply current	–	10	µA	V_{CC} = 5.5 V, outputs unloaded, V_{IN} = V_{CC} or GND All IR inputs = V_{CC}

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Capacitance

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	f_C = 1 MHz Unmeasured pins returned to GND
C_{IO}	I/O capacitance	–	20	pF	
C_{OUT}	Output capacitance	–	15	pF	

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Repeated data input with 8086-2 timings.

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AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; GND = 0 V

Timing Requirements

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AHRL}	A0/$\overline{CS}$ setup to $\overline{RD}$/$\overline{INTA}$↓	0	–	ns	–
t_{RHAX}	A0/$\overline{CS}$ hold after $\overline{RD}$/$\overline{INTA}$↑	0	–	ns	–
t_{RLRH}	$\overline{RD}$ pulse width	160	–	ns	–
t_{AHWL}	A0/$\overline{CS}$ setup to $\overline{WR}$↓	0	–	ns	–
t_{WHAX}	A0/$\overline{CS}$ hold after $\overline{WR}$↑	0	–	ns	–
t_{WLWH}	$\overline{WR}$ pulse width	190	–	ns	–
t_{DVWH}	Data setup to $\overline{WR}$↑	160	–	ns	–
t_{WHDX}	Data hold after $\overline{WR}$↑	0	–	ns	–
t_{JLJH} [1]	Interrupt request width (low)	100	–	ns	–
t_{CVIAL}	Cascade setup to second or third $\overline{INTA}$↓ (slave only)	40	–	ns	–
t_{RHRL}	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160	–	ns	–
t_{WHRL}	End of $\overline{WR}$ to next $\overline{WR}$	190	–	ns	–
t_{CHCL} [2]	End of command to next command (not same command type)	180	–	ns	–
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	400	–	ns	–

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Timing Responses

Symbol	Parameter	Limit values		Unit	Test condition [3]
		min.	max.		
t_{RLDV}	Data valid from $\overline{RD}$/$\overline{INTA}$↓	–	120	ns	1
t_{RHDZ}	Data float after $\overline{RD}$/$\overline{INTA}$↑	10	85	ns	2
t_{JHIH}	Interrupt output delay	–	300	ns	1
t_{IALCV}	Cascade valid from first $\overline{INTA}$↓ (master only)	–	360	ns	1
t_{RLEL}	Enable active from $\overline{RD}$↓ or $\overline{INTA}$↓	–	100	ns	1
t_{RHEH}	Enable inactive from $\overline{RD}$↑ or $\overline{INTA}$↑	–	150	ns	1
t_{AHDV}	Data valid from stable address	–	200	ns	1
t_{CVDV}	Cascade valid to valid data	–	200	ns	1

[1] This is the low time required to clear the input latch in the edge-triggered mode.

[2] Worst-case timing for t_{CHCL} in an actual microprocessor system is typically much greater than 400 ns.

[3] See diagrams on next page.

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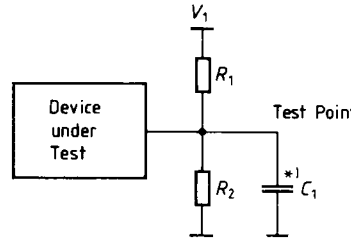
AC Testing

Load Circuit



*) Includes Stray and Jig Capacitance

Test Condition Definition

Test Condition	V_1	R_1	R_2	C_1
1	1.7 V	523 Ω	Open	100 pF
2	4.5 V	1.8 kΩ	1.8 kΩ	30 pF

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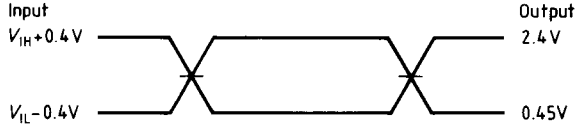
I/O Waveform



AC testing: All input signals must switch between V_{IL} −0.4 V and V_{IH} + 0.4 V. Input rise and fall times must be ≤15 ns.
All timing measurements are made at 2.4 V and 0.45 V.

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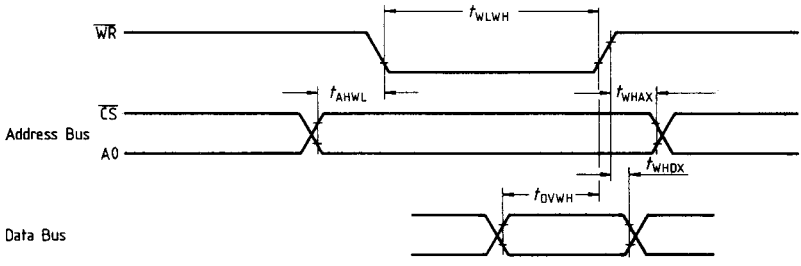
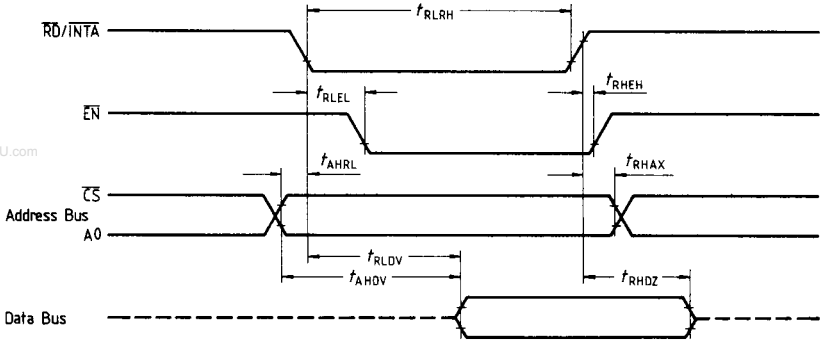
Waveforms

Write



Read/$\overline{INTA}$



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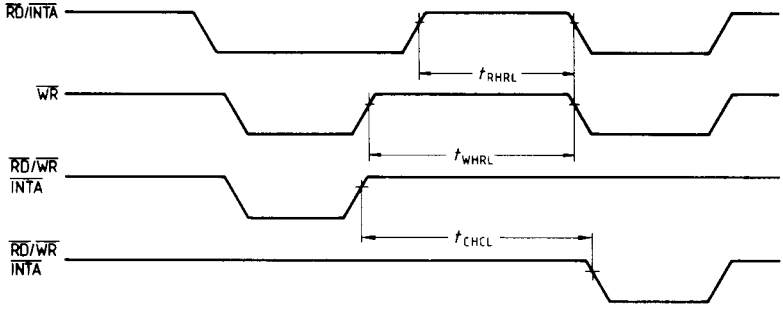
Other Timings



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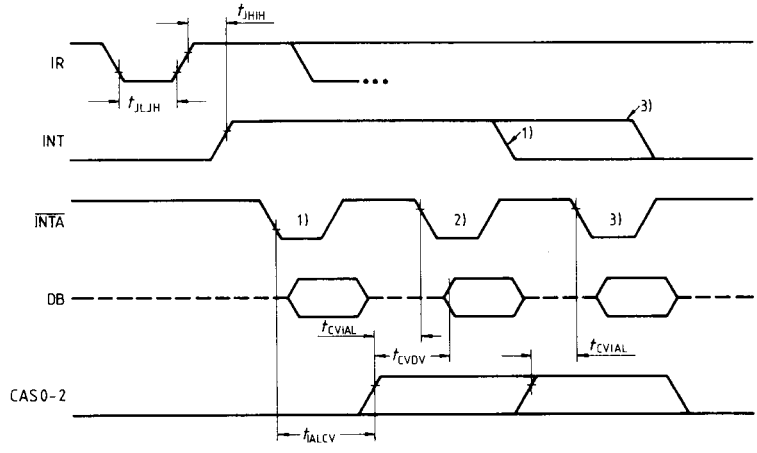
$\overline{\text{INTA}}$ Sequence



Interrupt output must remain high at least until leading edge of first $\overline{\text{INTA}}$.
[1]) Cycle 1 in SAB 8086/8088/80186/80188/80286 and 80386 systems, the data bus is not active.
[2]) Cycle 2.
[3]) Cycle 3 in SAB 8085 systems only.

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Ordering Information

Type	Ordering code	Description
SAB 82C59A-2-P	Q67120-P238	Programmable interrupt controller, 8 MHz, plastic package

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