DATA SHEET

SAB9077H
Picture-In-Picture (PIP) controller

Preliminary specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

FEATURES

Display

- 50/60 Hz PIP modes possible
- Twin PIP in interlaced mode at 8-bit resolution
- Sub-title mode features built in
- Large display fine positioning area, both channels independent
- Only 2 Mbit needed as external VDRAM (2 × 1 Mbit or 1 × 2 Mbit)
- Four 8-bit Analog-to-Digital Converters (ADCs; > 7-bit performance) with clamp circuit
- Most PIP modes handle interlaced pictures without joint line error
- Two PLLs which generate the line-locked clocks for the acquisition channels
- Display PLL to generate line-locked clock for the display
- Three 8-bit Digital-to-Analog Converters (DACs)
- 4 : 1 : 1 data format
- Data reduction factors 1 to 1, 1 to 2, 1 to 3 and 1 to 4, horizontal and vertical independent.

I^2C-bus programmable

- Single and double PIP modes can be set
- Full field still mode available
- Several aspect ratios can be handled
- Reduction factors can be set freely
- Selection of vertical filtering type
- Freeze of live pictures
- Fine tuned display position, H (8-bit), V (8-bit), both channels independent
- Fine tuned acquisition area, H (4-bit), V (8-bit), both channels independent
- Eight main borders, sub-borders and background colours available
- Border and background brightness adjustable, 30%, 50%, 70% and 100% IRE
- Several type of decoder input signals can be set.

GENERAL DESCRIPTION

The SAB9077H is a picture-in-picture controller for multi-standard TV-sets. The circuit contains ADCs, reduction circuitry, memory control, display control and DACs.

It inserts one or two live video signals with original or reduced sizes into a live video signal. All video signals are expected to be analog base band signals. The conversion into the digital environment and back to the analog environment is done on chip. Internal clocks are generated by two acquisition PLLs and a display PLL.

The two PIP channels and a large external memory offer a wide range of PIP modes. The emphasis is put on single PIP, double PIP, split-screen mode and many multi-PIP modes.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current		–	200	–	mA
f_{sys}	system frequency	note 1	–	27	–	MHz
f_{loop}	PLL loop bandwidth frequency		4	–	–	kHz
t_{jitter}	PLL short term stability time	jitter during 1 line (64 µs)	–	–	4	ns
ς	PLL damping factor		–	0.7	–	–

Note

1. The internal system frequency is 1728 times the H_{Sync} input frequency for both the acquisition and display PLLs.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAB9077H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

BLOCK DIAGRAM

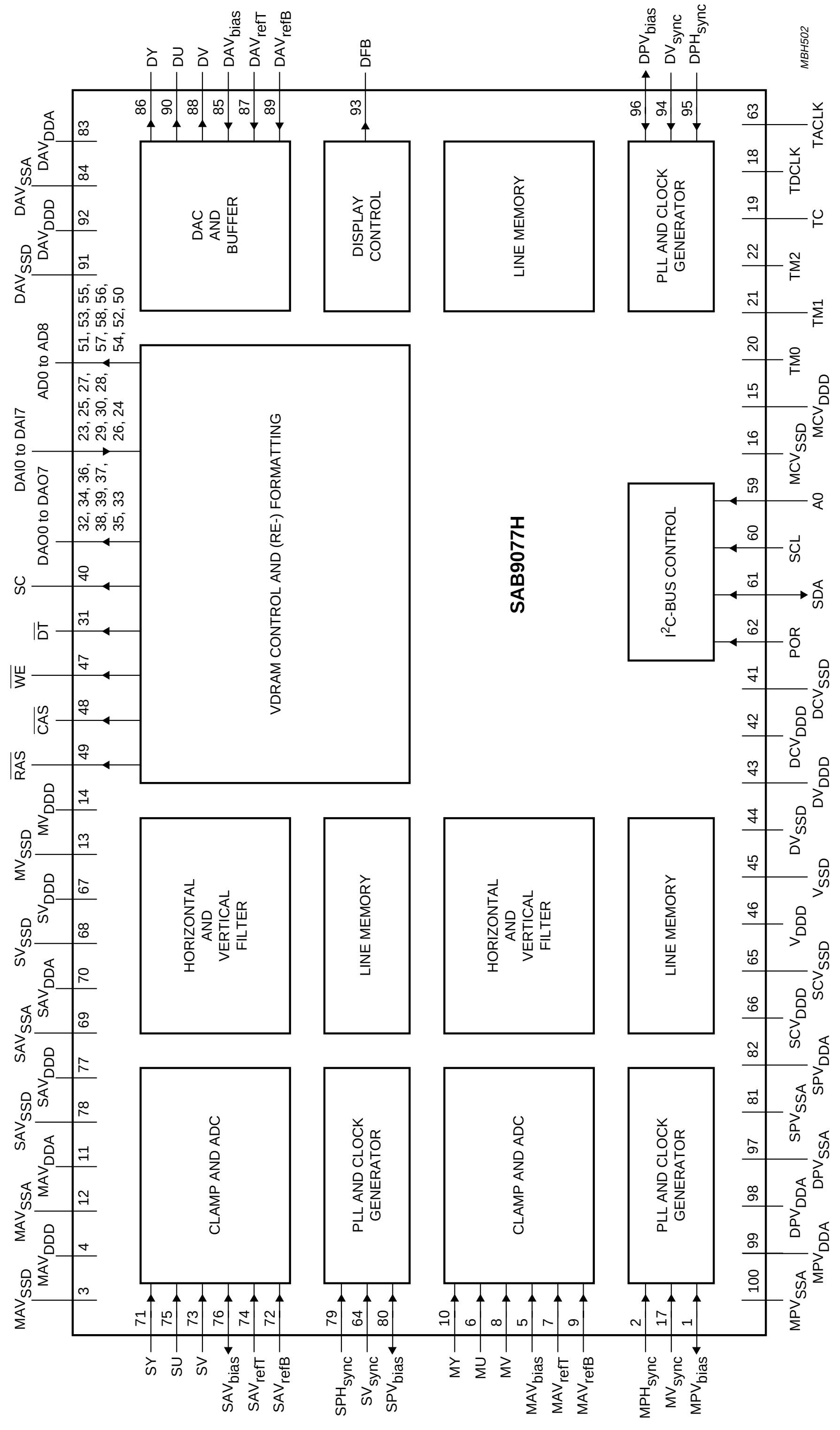


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
MPV_{bias}	1	I/O	E027	analog bias reference for main channel
MPH_{sync}	2	I	HPP01	horizontal synchronization for main channel
MAV_{SSD}	3	I/O	E009	digital ground for main channel ADCs and PLLs
MAV_{DDD}	4	I/O	E030	digital positive power supply for main channel ADCs and PLLs
MAV_{bias}	5	I	E027	analog bias reference for main channel ADCs
MU	6	I	E027	analog U input for main channel
MAV_{refT}	7	I	E027	analog top reference voltage for main channel ADCs
MV	8	I	E027	analog V input for main channel
MAV_{refB}	9	I	E027	analog bottom reference voltage for main channel ADCs
MY	10	I	E027	analog Y input for main channel
MAV_{DDA}	11	I/O	E030	analog positive power supply for main channel ADCs
MAV_{SSA}	12	I/O	E009	analog ground for main channel ADCs
MV_{SSD}	13	I/O	E009	digital ground for main-channel core
MV_{DDD}	14	I/O	E030	digital positive power supply for main-channel core
MCV_{DDD}	15	I/O	E030	digital positive power supply for main-clock buffer
MCV_{SSD}	16	I/O	E009	digital ground for main-clock buffer
MV_{sync}	17	I	HPP01	vertical synchronization for main channel
TDCLK	18	I	HPP01	test clock for display
TC	19	I	HPP01	test control
TM0	20	I	HPP01	test mode 0
TM1	21	I	HPP01	test mode 1
TM2	22	I	HPP01	test mode 2
DAI0	23	I	HPP04	data bus input from memory; bit 0
DAI7	24	I	HPP04	data bus input from memory; bit 7
DAI1	25	I	HPP04	data bus input from memory; bit 1
DAI6	26	I	HPP04	data bus input from memory; bit 6
DAI2	27	I	HPP04	data bus input from memory; bit 2
DAI5	28	I	HPP04	data bus input from memory; bit 5
DAI3	29	I	HPP04	data bus input from memory; bit 3
DAI4	30	I	HPP04	data bus input from memory; bit 4
$\overline{DT}$	31	O	OPF20	memory data transfer output; active LOW
DAO0	32	O	OPF20	data bus output to memory; bit 0
DAO7	33	O	OPF20	data bus output to memory; bit 7
DAO1	34	O	OPF20	data bus output to memory; bit 1
DAO6	35	O	OPF20	data bus output to memory; bit 6
DAO2	36	O	OPF20	data bus output to memory; bit 2
DAO5	37	O	OPF20	data bus output to memory; bit 5
DAO3	38	O	OPF20	data bus output to memory; bit 3
DAO4	39	O	OPF20	data bus output to memory; bit 4
SC	40	O	OPF20	memory shift clock output

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
DCV_{SSD}	41	I/O	E009	digital ground for display-clock buffer
DCV_{DDD}	42	I/O	E030	digital positive power supply for display-clock buffer
DV_{DDD}	43	I/O	E030	digital positive power supply for display core
DV_{SSD}	44	I/O	E009	digital ground for display core
V_{SSD}	45	I/O	E009	digital ground for peripherals
V_{DDD}	46	I/O	E030	digital positive power supply for peripherals
$\overline{WE}$	47	O	OPF20	memory write enable output; active LOW
$\overline{CAS}$	48	O	OPF20	memory column address strobe output; active LOW
$\overline{RAS}$	49	O	OPF20	memory row address strobe output; active LOW
AD8	50	O	OPF20	memory address bus output; bit 8
AD0	51	O	OPF20	memory address bus output; bit 0
AD7	52	O	OPF20	memory address bus output; bit 7
AD1	53	O	OPF20	memory address bus output; bit 1
AD6	54	O	OPF20	memory address bus output; bit 6
AD2	55	O	OPF20	memory address bus output; bit 2
AD5	56	O	OPF20	memory address bus output; bit 5
AD3	57	O	OPF20	memory address bus output; bit 3
AD4	58	O	OPF20	memory address bus output; bit 4
A0	59	I	HPF01	I^2C-bus address 0 selection input
SCL	60	I	HPP01	shift clock input for I^2C-bus
SDA	61	I/O	IOI41	shift I^2C-bus input data; acknowledge I^2C-bus output data
POR	62	I	HUP07	power-on reset input
TACLK	63	I	HPP01	test clock for acquisition
SV_{sync}	64	I	HPP01	vertical synchronization input for sub-channel
SCV_{SSD}	65	I/O	E009	digital ground for sub-clock buffer
SCV_{DDD}	66	I/O	E030	digital positive power supply for sub-clock buffer
SV_{DDD}	67	I/O	E030	digital positive power supply for sub-channel core
SV_{SSD}	68	I/O	E009	digital ground for sub-channel core
SAV_{SSA}	69	I/O	E009	analog ground for sub-channel ADCs
SAV_{DDA}	70	I/O	E030	analog positive power supply for sub-channel ADCs
SY	71	I	E027	analog Y input for sub-channel
SAV_{refB}	72	I	E027	analog bottom reference voltage for sub-channel ADCs
SV	73	I	E027	analog V input for sub-channel
SAV_{refT}	74	I	E027	analog top reference voltage for sub-channel ADCs
SU	75	I	E027	analog U input for sub-channel
SAV_{bias}	76	I/O	E027	analog bias reference for sub-channel ADCs
SAV_{DDD}	77	I/O	E030	digital positive power supply for sub-channel ADCs and PLLs
SAV_{SSD}	78	I/O	E009	digital ground for sub-channel ADCs and PLLs
SPH_{sync}	79	I	HPP01	horizontal synchronization input for sub-channel
SPV_{bias}	80	I/O	E027	analog bias reference for sub-channel
SPV_{SSA}	81	I/O	E009	analog ground for sub-channel PLL

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
SPV_{DDA}	82	I/O	E030	analog positive power supply for sub-channel PLL
DAV_{DDA}	83	I/O	E030	analog positive power supply for DACs
DAV_{SSA}	84	I/O	E009	analog ground for DACs
DAV_{bias}	85	I	E027	analog bias voltage reference for DACs
DY	86	O	E027	analog Y output of DAC
DAV_{refT}	87	I	E027	analog top reference voltage for DACs
DV	88	O	E027	analog V output of DAC
DAV_{refB}	89	I	E027	analog bottom reference voltage for DACs
DU	90	O	E027	analog U output of DAC
DAV_{SSD}	91	I/O	E009	digital ground for DACs
DAV_{DDD}	92	I/O	E030	digital positive power supply for DACs
DFB	93	O	OPF20	fast blanking control output signal
DV_{sync}	94	I	HPP01	vertical synchronization input for display channel
DPH_{sync}	95	I	HPP01	horizontal synchronization input for display PLL
DPV_{bias}	96	I/O	E027	analog bias voltage reference for display PLL
DPV_{SSA}	97	I/O	E009	analog ground for display PLL
DPV_{DDA}	98	I/O	E030	analog positive power supply for display PLL
MPV_{DDA}	99	I/O	E030	analog positive power supply for main channel PLL
MPV_{SSA}	100	I/O	E009	analog ground for main channel PLL

Table 1 Pin type explanation

PIN TYPE	DESCRIPTION
E030	V_{DD} pin; diode to V_{SS}
E009	V_{SS} pin; diode to V_{DD}
E027	analog input pin; diode to V_{DD} and V_{SS}
HPF01	digital input pin; CMOS levels, diode to V_{SS}
HPP01	digital input pin; CMOS levels, diode to V_{DD} and V_{SS}
HUP07	digital input pin; CMOS levels with hysteresis, pull-up resistor to V_{DD}, diode to V_{DD} and V_{SS}
HOU21	digital IO pin; CMOS levels with hysteresis, pull-up to V_{DD}, diode to V_{DD} and V_{SS}
IOI41	I^2C-bus pull-down output stage; CMOS input levels, diode to V_{SS}
OPF20	digital output pin; CMOS levels

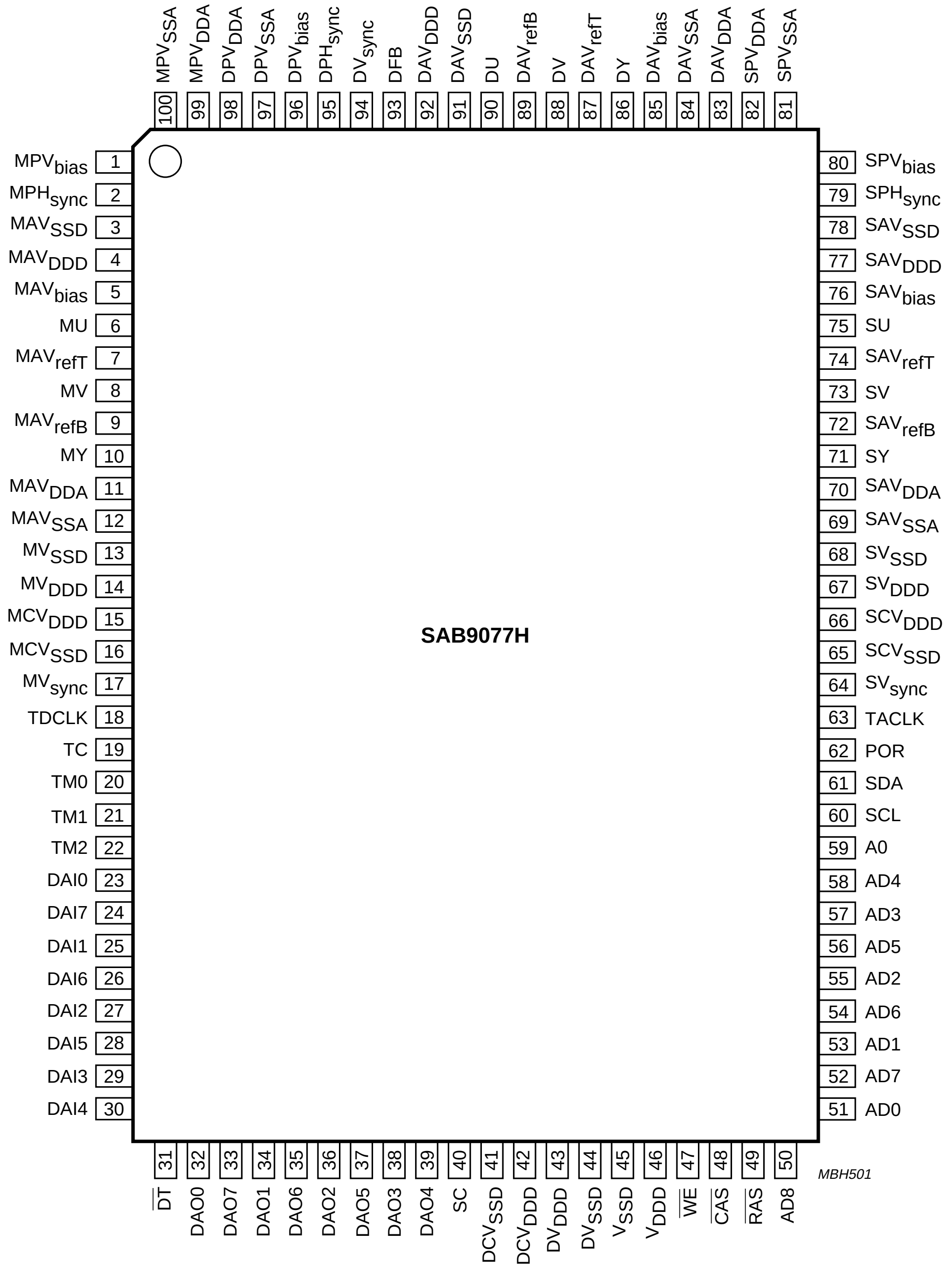


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Pixel rate

The internal chrominance format used is 4 : 1 : 1. It is expected that the bandwidth of the input signals is limited to 4.5 MHz for the Y input and 1.125 MHz for the U/V inputs.

The Y input is sampled with a $1728 \times H_{sync}$ (≈27.0 MHz) clock and is filtered and down sampled to the internal $864 \times H_{sync}$ (≈13.5 MHz) pixel rate.

The U and V inputs are multiplexed and sampled with a $432 \times H_{sync}$ clock and down sampled to the internal $216 \times H_{sync}$ (≈3.375 MHz) pixel rate.

Acquisition area

Synchronization is done via the acquisition H_{Sync} and V_{Sync} pins. With the acquisition fine positioning added to a system constant the starting point of the acquisition can be controlled.

The acquisition area is 672 pixels/line and 228 lines/field for NTSC and 276 lines/field for PAL. Both main and sub-channel are equivalent in handling the data.

Display mode

The internal display pixel rate is $864 \times DPH_{sync}$ which is 13.5 MHz. This pixel rate is upsampled by interpolation to $1728 \times DPH_{sync}$ before the DAC stage.

Display area

The display background is an area of 696 pixels for both PAL and NTSC, 238 lines for NTSC and 286 lines for PAL. This can be put on/off by the BGON bit independent of the PIPON bits. This area can be moved by the display background fine positioning (BGHFP and BGVFP).
Its colour is determined by the BGCOL and BGBRT bits.

Within this area PIPs are defined dependent on the PIP mode. The PIP sizes are determined by the display reduction factors as is shown in Table 2. Whether a PAL or NTSC fixed number is used is depends on the DPAL bit.

The display fine positioning determines the location of the PIPs with respect to the background. sub and main-channel both have their independent PIP size and location control, which is shown in Fig.3.

Table 2 PIP sizes

REDUCTION	H/1	H/2	H/3	H/4	V/1	V/2	V/3	V/4
Pixels	672	336	224	168	–	–	–	–
NTSC-lines	–	–	–	–	228	114	76	57
PAL-lines	–	–	–	–	276	138	92	69

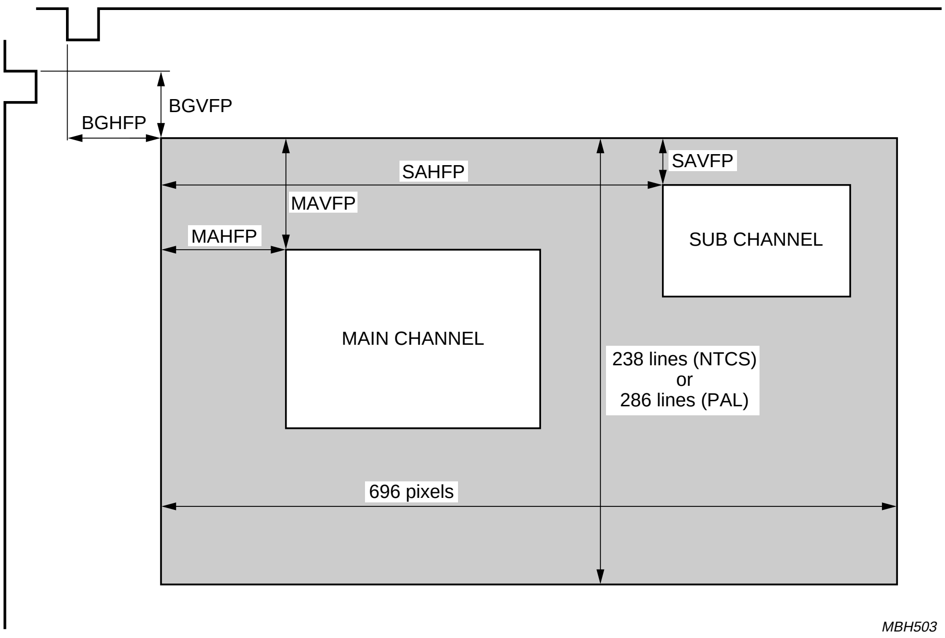


Fig.3 Display fine positioning.

PIP modes

The two independent acquisition channels can also be controlled independently on the display side. A wide variety of modes is possible but a subset of 7 modes is fixed and can be set easily by the I^2C-bus. An overview of the preconditioned modes is given in Table 3. For all PIP modes the main and sub-display fine positioning must be set to obtain a display configuration.

DATA TRANSFER

The internal data path has an 8-bit resolution and 4 : 1 : 1 data format. The communication to the external VDRAM takes place at 864 × H_{sync} (both display and acquisition).

Approximately 800 8-bit words can be fetched from the external VDRAM in one display line which is not enough to display one complete display line with true 8-bit resolution.

Two methods of reducing data are available. One is simply skipping the 8-bit to 6-bit (SKIP6, I^2C-bus bit) and the other is a small form of data reduction to come from 8-bit to 6-bit (SMART6, I^2C-bus bit). If both bits are set to logic 0 the device is in true 8-bit resolution mode. For the twin PIP mode the main channel is not placed in the VDRAM but in an internal buffer, 8 bit resolution is then possible for both PIPs.

Table 3 PIP modes

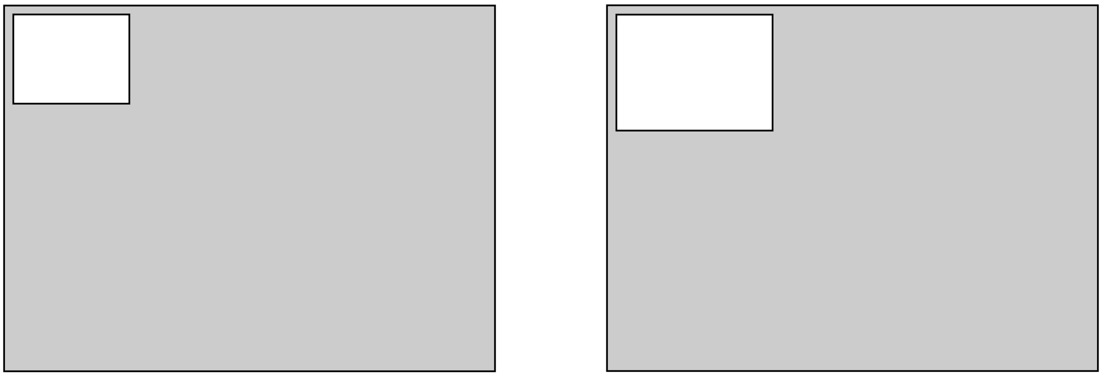
PIP MODES			SUB-CHANNEL		MAIN CHANNEL		SUB-CHANNEL		MAIN CHANNEL	
NAME	**FIGURE**	**MODE**	**REDH**	**REDV**	**REDH**	**REDV**	**HFP**	**VFP**	**HFP**	**VFP**
SP	SP small	0000	$\frac{1}{4}$	$\frac{1}{4}$	–	–	–	–	–	–
SP	SP medium	0000	$\frac{1}{3}$	$\frac{1}{3}$	–	–	–	–	–	–
SP	SP large	0000	$\frac{1}{2}$	$\frac{1}{2}$	–	–	–	–	–	–
SP	SP small	0000	–	–	$\frac{1}{4}$	$\frac{1}{4}$	–	–	–	–
SP	SP medium	0000	–	–	$\frac{1}{3}$	$\frac{1}{3}$	–	–	–	–
SP	SP large	0000	–	–	$\frac{1}{2}$	$\frac{1}{2}$	–	–	–	–
DP	DP	0000	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	03H	46H	57H	46H
DP	twin PIP	1001	$\frac{1}{2}$	$\frac{1}{1}$	$\frac{1}{2}$	$\frac{1}{1}$	03H	05H	57H	05H
MP3L	POP-left	0010	$\frac{1}{4}$	$\frac{1}{4}$	–	–	08H	10H	–	–
MR3R	POP-right	0010	–	–	$\frac{1}{4}$	$\frac{1}{4}$	–	–	72H	10H
MR3D	POP-double	0010	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{4}$	08H	10H	72H	10H
MP7	POP-double	0011	$\frac{1}{4}$	$\frac{1}{4}$	–	–	03H	05H	–	–
MP8	MP7	0011	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{2}$	$\frac{1}{2}$	03H	05H	44H	20H
MP4	Quatro	0001	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	03H	05H	03H	77H
MP9	MP9	0100	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	03H	05H	51H	3BH
MP16	MP16	0101	$\frac{1}{4}$	$\frac{1}{4}$	–	–	03H	05H	–	–
MP16	MP16 mix	0110	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{4}$	03H	05H	03H	77H
FFS	full field still	0000	$\frac{1}{1}$	$\frac{1}{1}$	–	–	03H	05H	–	–
FFL	full field live	1000	–	–	$\frac{1}{1}$	$\frac{1}{1}$	–	–	03H	05H
MAN	manual	X111	X	X	X	X	X	X	X	X

PIP COMBINATIONS

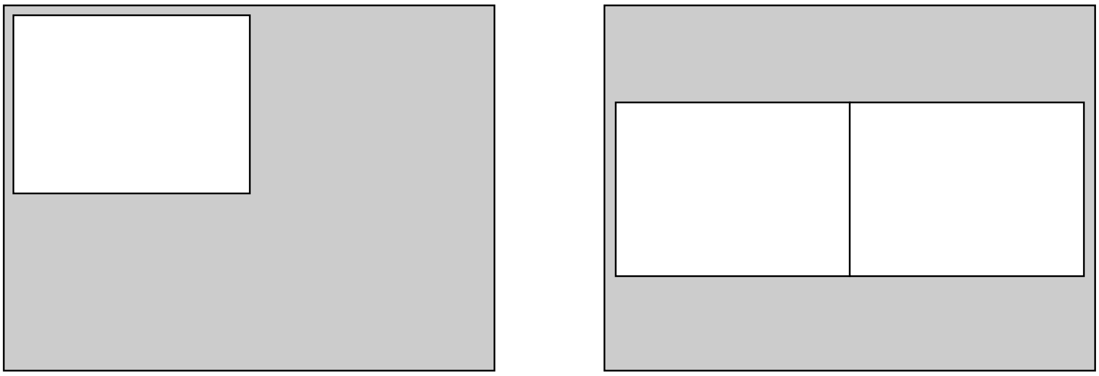
Figures 4, 5 and 6 provide an overview of possible combinations as they can be shown on the screen.
An example of fine positioning is given in the right four columns of Table 3.

More PIP modes can be obtained by varying the horizontal and vertical reduction factors to meet correct aspect ratios when using 16 : 9 screens.

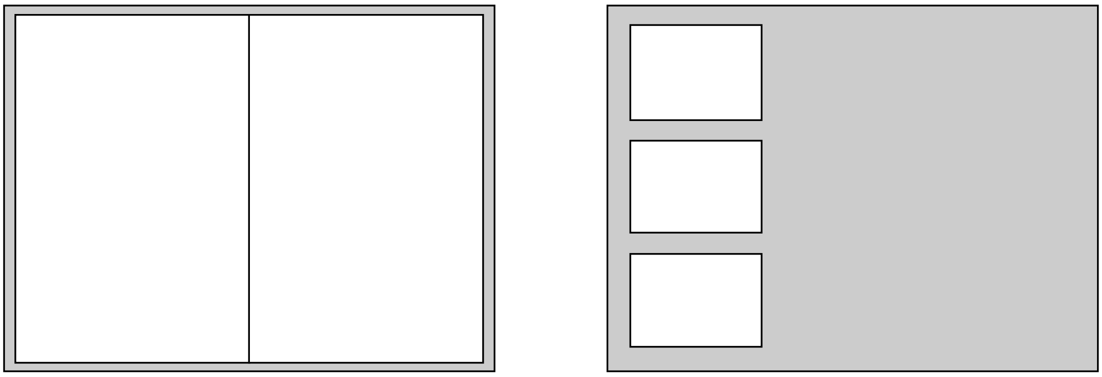
In manual mode more PIP modes become available. Table 6 with associating text describes how to setup a PIP mode.



SP-Small **SP-Medium**

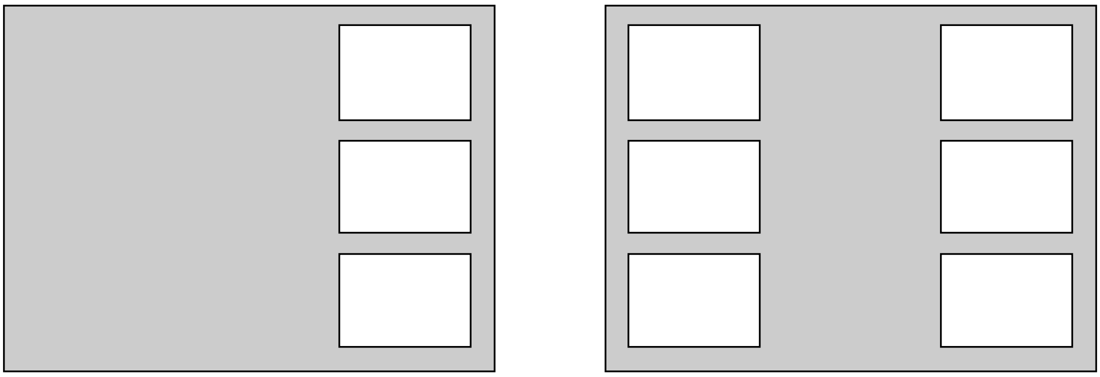


SP-Large **DP**



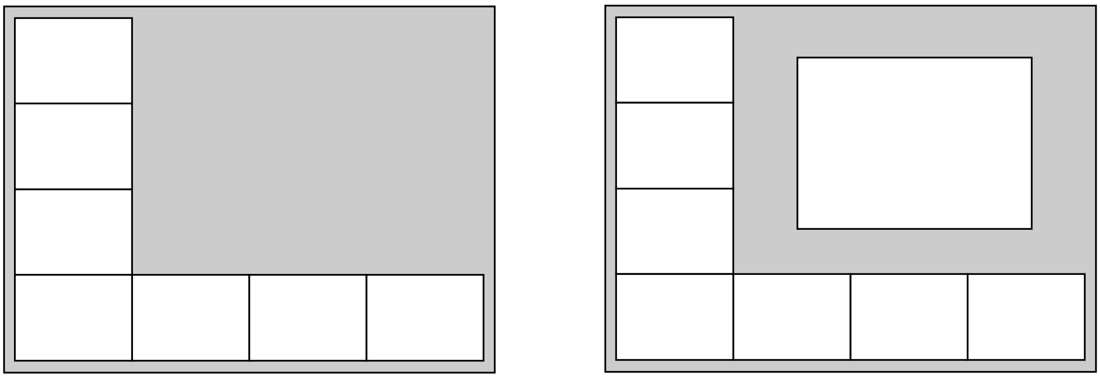
Twin-PIP **POP-Left**

Fig.4 PIP Modes.



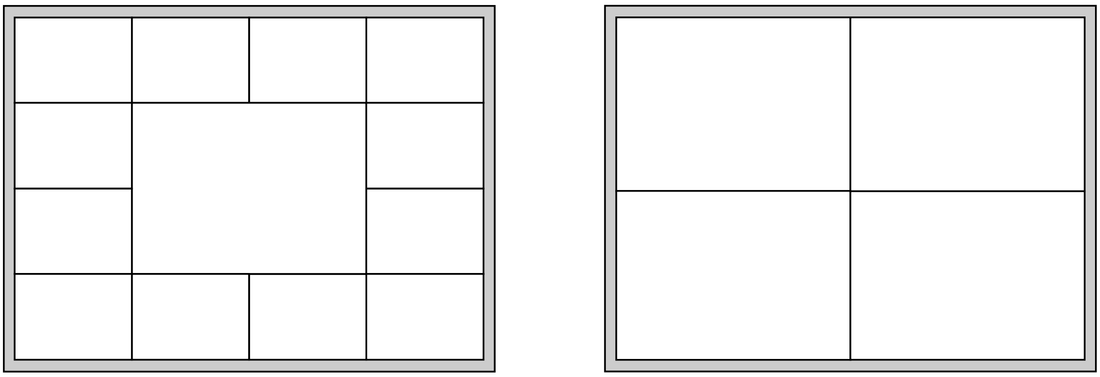
POP-Right MGD589

POP-Double MGD590



MP7 MGD591

MP8 MGD592



MP13 MGD593

Quatro MGD584

Fig.5 PIP Modes.

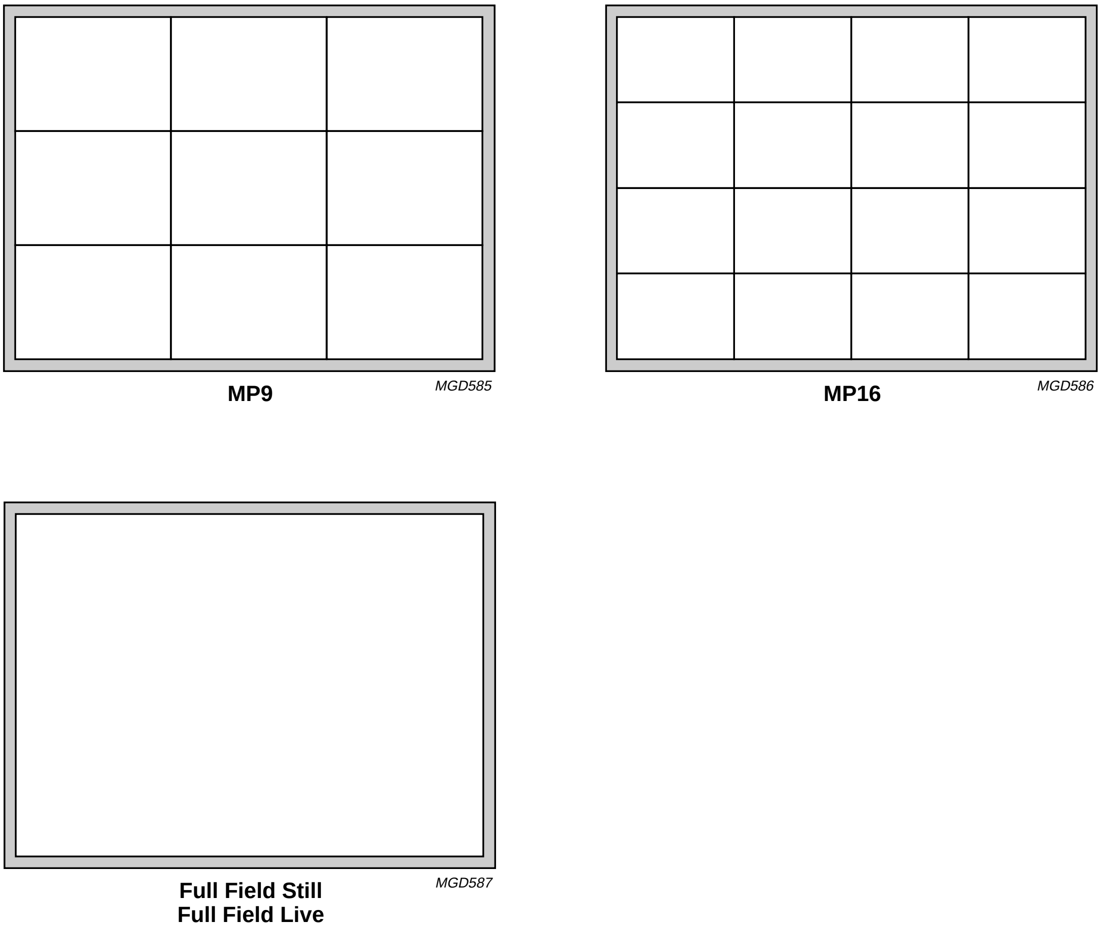


Fig.6 PIP Modes.

I^2C-bus description

The I^2C-bus provides bidirectional 2-line communication between different ICs. The SDA line is the serial data line and SCL serves as serial clock line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

The SAB9077H has the I^2C-bus addresses 2C and 2E, switchable by the pin A0. Valid subaddresses are 00H to 18H (Table 4) and 20H to 32H (Table 6).

I^2C-bus control is in accordance with the I^2C-bus protocol.

First a START sequence must be put on the I^2C-bus, then the I^2C-bus address of the circuit must be send, followed by a subaddress. After this sequence the data of the subaddresses must be sent. An auto-increment function gives the option to send data of the incremented subaddresses until a STOP sequence is send.
Table 4 gives an overview of the I^2C-bus addresses.

Table 4 Overview of I^2C-bus addresses

SA	DATA BYTE							
	BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
00H	MPIPON	SPIPON	MFREEZE	SFREEZE	MCOPY	PIPMODE2	PIPMODE1	PIPMODE0
01H	note 1	note 1	M1FLD	S1FLD	NIPCOFF	DNONINT	MNONINT	SNONINT
02H	DFILT	FILLOFF	SMART6	SKIP6	YTH3	YTH2	YTH1	YTH0
03H	BGHFP3	BGHFP2	BGHFP1	BGHFP0	BGVFP3	BGVFP2	BGVFP1	BGVFP0
04H	SDHFP7	SDHFP6	SDHFP5	SDHFP4	SDHFP3	SDHFP2	SDHFP1	SDHFP0
05H	SDVFP7	SDVFP6	SDVFP5	SDVFP4	SDVFP3	SDVFP2	SDVFP1	SDVFP0
06H	MDHFP7	MDHFP6	MDHFP5	MDHFP4	MDHFP3	MDHFP2	MDHFP1	MDHFP0
07H	MDVFP7	MDVFP6	MDVFP5	MDVFP4	MDVFP3	MDVFP2	MDVFP1	MDVFP0
08H	MDREDH1	MDREDH0	MDREDV1	MDREDV0	SDREDH1	SDREDH0	SDREDV1	SDREDV0
09H	MAREDH1	MAREDH0	MAREDV1	MAREDV0	SAREDH1	SAREDH0	SAREDV1	SAREDV0
0AH	MAHFP3	MAHFP2	MAHFP1	MAHFP0	SAHFP3	SAHFP2	SAHFP1	SAHFP0
0BH	SAVFP7	SAVFP6	SAVFP5	SAVFP4	SAVFP3	SAVFP2	SAVFP1	SAVFP0
0CH	MAVFP7	MAVFP6	MAVFP5	MAVFP4	MAVFP3	MAVFP2	MAVFP1	MAVFP0
0DH	MLSEL3	MLSEL2	MLSEL1	MLSEL0	SLSEL3	SLSEL2	SLSEL1	SLSEL0
0EH	MBSEL3	MBSEL2	MBSEL1	MBSEL0	SBSEL3	SBSEL2	SBSEL1	SBSEL0
0FH	BHSIZE3	BHSIZE2	BHSIZE1	BHSIZE0	BVSIZE3	BVSIZE2	BVSIZE1	BVSIZE0
10H	note 1	SBON	SBBRT1	SBBRT0	note 1	SBCOL2	SBCOL1	SBCOL0
11H	note 1	SBSON	SBSBRT1	SBSBRT0	note 1	SBSCOL2	SBSCOL1	SBSCOL0
12H	note 1	MBON	MBBRT1	MBBRT0	note 1	MBCOL2	MBCOL1	MBCOL0
13H	note 1	MBSON	MBSBRT1	MBSBRT0	note 1	MBSCOL2	MBSCOL1	MBSCOL0
14H	note 1	BGON	BGBRT1	BGBRT0	note 1	SBGCOL2	SBGCOL1	SBGCOL0
15H	note 1	note 1	note 1	SVFILT	SUVPOL	SVSPOL	SHSYNC	SFPOL
16H	note 1	note 1	note 1	MVFILT	MUVPOL	MVSPOL	MHSYNC	MFPOL
17H	note 1	FBDEL2	FBDEL1	FBDEL0	DUVPOL	DVSPOL	DHSYNC	DFPOL
18H	PEDESTV3	PEDESTV2	PEDESTV1	PEDESTV0	PEDESTU3	PEDESTU2	PEDESTU1	PEDESTU0

Note

1. The data bits which are not used should be set to zero.

SA 00H PIP REGISTER

MPIPON and SPIPON bits switch respectively the main and sub PIPs of the SAB9077H on or off. The MFREEZE and SFREEZE bits make the current live pictures for the Main and Sub frozen. The writing to the VDRAM is stopped.

The MCOPY bit copies the Main data direct to the output. This mode should only be set when MREDV is 1/1. Table 2 gives more information when to set this bit. The PIPMODE bits set the PIP mode in accordance with Table 3.

SA 01H DISPLAY REGISTER

M1FLD and S1FLD(1) bits control the use of the reserved second field in the VDRAM. If this bit is set to logic 0 then address spaces are reserved for both fields in the VDRAM. This avoids joint line errors. Whether these address spaces are used is dependent on the interlacing of the input signals and the NONINT bits. If a 1FLD bit is set to logic 1 then only 1 address space is used in the VDRAM for both fields. In some PIP modes the use of a second field is not possible since there is not enough space in the VDRAM, in these modes the 1FLD bit must be set to logic 1. The DNONINT bit controls the interlace mode of the display part. If set to logic 1 then data is only read from one field in the VDRAM. If set to logic 0 then both fields (if available) are used for display.

MNONINT and SNONINT bits control the interlace mode of the acquisition blocks. If set to logic 1 then data is only written to one field in the VDRAM (two fields remain allocated). If set to logic 0 then both fields (if available) are used for acquisition.

The NIPCOFF bit determines whether a grey bar is inserted in case a NTSC PIP is displayed in a PIP with PAL PIP size. The missing lines are equally divided between the top part and the bottom part of the PIP window and made 30% grey. If this bit is set to logic 0 the grey bar is displayed, if this bit is set to logic 1 the grey bar is omitted and the PIP data is shifted up.

SA 02H DISPLAY REGISTER

The DFILT bit controls an interpolating filter that changes the internal 864 pixels data rate to the output data rate of 2 × 864 pixels. If DFILT is set to logic 1 then the filter is on.

The FILLOFF bit controls filling of PIPs when the PIP mode is switched. If FILLOFF is set to logic 0 then all PIPs are filled with a 30% gray until their channel has been updated. If FILLOFF is set to logic 1 then the VDRAM content is always visible. This is useful when a new, ‘similar’ to the previous one, PIP mode is set. The previous data can then be displayed.

The SMART6 and SKIP6 bits control the data transfer mode to the external VDRAM. For modes which display a complete line (672 pixels) a form of data reduction has to be carried out.
Two transfer modes are available. One is simply skipping the 8-bit data path to 6-bit (SKIP6). The other is carry out an intelligent data reduction which keeps an 8-bit resolution (SMART6).

The YTH bits control the video output. If the current Y-value is less then YTH × 16 then the fast blank is switched off, the original live background will be visible. This feature can be used to pick up sub-titles and display them as On-Screen Display (OSD) anywhere on the screen.

SA 03H DISPLAY BACKGROUND FINE POSITIONING REGISTER

The BGHFP bits control the horizontal display positioning of the background. The resolution is 16 steps of 4 pixels. The BGVFP bits control the vertical display positioning of the background. The resolution is 16 steps of 2 lines/field. The background fine positioning moves the complete display. It is a general offset of all the PIP pictures and background, It is only meant to adjust once the centring of all PIP modes (see Fig.3).

SA 04H AND SA 05H DISPLAY SUB-CHANNEL FINE POSITIONING REGISTERS

These registers control the horizontal and vertical fine positioning of the display sub-channel with respect to the display background. This is the actual fine positioning (see Fig.3). The horizontal resolution is 256 steps of 4 pixels and the vertical resolution is 256 steps of 1 line/field.

SA 06H AND SA 07H DISPLAY MAIN-CHANNEL FINE POSITIONING REGISTERS

These registers control the horizontal and vertical fine positioning of the display main-channel with respect to the display background. This is the actual fine positioning (see Fig.3). The horizontal resolution is 256 steps of 4 pixels and the vertical resolution is 256 steps of 1 line/field.

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(1) If the 1 FLD bits are set to logic 1 the NONINT bits of the corresponding channel must also be set to logic 1.

SA 08H DISPLAY REDUCTION FACTORS REGISTER

This register sets the display reduction factors, independent of the acquisition reduction factors.
It sets the PIP size to a certain default value in such a way that the border drawn around the PIP is just fitting.

SA 09H ACQUISITION REDUCTION FACTORS REGISTER

This register sets the acquisition reduction factors, independent of the display reduction factors. If the HRED is 1 to 1 then the VRED must also be 1 : 1.

Restrictions are:

- The DREDH and AREDH must be the same
- The DREDV is equal or smaller than the AREDV (e.g DREDV is 1 to 2 and AREDV is 1 : 1).

SA 0AH AND SA 0CH ACQUISITION FINE POSITIONING REGISTERS

These registers determine the start of the acquisition area. Horizontal fine positioning can be adjusted with 16 steps of 2 pixels, vertical fine positioning can be adjusted with 256 steps of 1 line/field.

SA 0DH AND SA 0EH SELECTION REGISTERS

The MLSEL and SLSEL bits control which PIP is live. Both main channel and sub-channel can have one live PIP. Counting is done from upper-left to lower-right.

The MBSEL and SBSEL bits control which PIP border has a different colour. Both main and sub-channel can have a different PIP channel border selection. Counting is done from upper-left to lower-right.

SA 0FH BORDER SIZE REGISTER

This register controls the border size. The minimum horizontal border is 2 pixels. The minimum vertical border is 1 line. The vertical border size is multiplied by the FH mode number before it is displayed on the screen.

SA 10H AND SA 11H BORDER COLOUR AND BORDER SELECT COLOUR OF SUB-CHANNEL REGISTERS (see Table 5)

If SBON is set to logic 1 then the border of the sub-channel is visible.The SBBRT and SBCOL bits control the brightness and colour of the sub-channel border colour.

If SBSON is set to logic 1 then one sub-PIP border can have a different colour. This border is selected by the SBSEL bits.

The SBSBRT and SBSCOL bits control the brightness and colour of the sub-border selection colour.

SA 12H AND SA 13H BORDER COLOUR AND BORDER SELECTION COLOUR OF MAIN CHANNEL REGISTERS (see Table 5)

If MBON is set to logic 1 then the border of the main channel is visible.

The MBBRT and MBCOL bits control the brightness and colour of the main-channel border colour. If MBSON is set to logic 1 then one main PIP border can have a different colour. This PIP is selected by the MBSEL bits, the function can be switched on if MBSON is set to logic 1.

The MBSBRT and MBSCOL bits control the brightness and colour of the main-border selection colour.

SA 14H BACKGROUND CONTROL REGISTER (see Table 5)

If BGON is set to logic 1 then the background is visible.

The BGBRT and BGCOL bits control the brightness and colour of the background colour.

Table 5 Colour types and brightness levels

COLOUR TYPE		BRIGHTNESS LEVEL			
COLOUR	**VALUE**	**4H**	**5H**	**6H**	**7H**
Black	0H	0%	10%	30%	50%
Blue	1H	30%	50%	70%	100%
Red	2H	30%	50%	70%	100%
Magenta	3H	30%	50%	70%	100%
Green	4H	30%	50%	70%	100%
Cyan	5H	30%	50%	70%	100%
Yellow	6H	30%	50%	70%	100%
White	7H	60%	70%	80%	100%

Table 5 indicates how I^2C-bus register settings control the colour and brightness. All colour registers are similar, they contain one on/off bit, two brightness bits and three colour type bits. To determine which colour is visible in the event two or more colours being displayed on the same position, the next priority scheme is followed:

1. Sub-select colour (SBS)
2. Sub-border colour (SB)
3. Main-select colour (MBS)
4. Main-border colour (MB)
5. Background colour (BG).

SA 15H AND SA 16H DECODER REGISTERS

The MVFILT and SVFILT bits can set the type of vertical filtering. The MUVPOL and SUVPOL bits invert the UV polarity of the incoming signals. The MVSPOL and SVSPOL bits determine the active edge of the V_{sync} (see Fig.7). The MHSYNC and SHSYNC bits determine the timing of the H_{sync} pulse (burstkey or H_{sync} timing).
The MFPOL and SFPOL bits can invert the field identification (ID) of the incoming fields (see Fig.7).

SA 17H DISPLAY SETTINGS REGISTER

The FBDEL bits can adjust the fast blank delay in 8 steps of $\frac{1}{2}$ a clock cycle (–8 to +7). 0H is mid-scale.
The DUVPOL bit inverts the UV polarity of the border colours.

The DVSPOL bit determines the active edge of the V_{sync} (see Fig.7). The DHSYNC bit determines the timing of the H_{sync} pulse (burstkey or H_{sync}). The DFPOL bit can invert the field ID of the incoming fields (see Fig.7).

SA 18H PEDESTAL SETTINGS REGISTER

The PEDESTU and PEDESTV bits give the U and V DAC outputs an offset of –8 to +7 LSB when the FBL is switched off. This can be used to adjust the White point of the system.

Additional I^{2}C-bus settings

Table 6 Overview of additional I^{2}C-bus sub-addresses

SA	DATA BYTE							
	BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
20H	PRIO	DPAL	MPAL	SPAL	MVRPN1	MVRPN0	SVRPN1	SVRPN0
21H	MHRPO31	MHRPO30	MHRPO21	MHRPO20	MHRPO11	MHRPO10	MHRPO1	MHRPO0
22H	MHRPN31	MHRPN30	MHRPN21	MHRPN20	MHRPN11	MHRPN10	MHRPN1	MHRPN0
23H	MHPIC7	MHPIC6	MHPIC5	MHPIC4	MHPIC3	MHPIC2	MHPIC1	MHPIC0
24H	MVPIC7	MVPIC6	MVPIC5	MVPIC4	MVPIC3	MVPIC2	MVPIC1	MVPIC0
25H	MHDIS07	MHDIS06	MHDIS05	MHDIS04	MHDIS03	MHDIS02	MHDIS01	MHDIS00
26H	MHDIS17	MHDIS16	MHDIS15	MHDIS14	MHDIS13	MHDIS12	MHDIS11	MHDIS10
27H	MHDIS27	MHDIS26	MHDIS25	MHDIS24	MHDIS23	MHDIS22	MHDIS21	MHDIS20
28H	MHDIS37	MHDIS36	MHDIS35	MHDIS34	MHDIS33	MHDIS32	MHDIS31	MHDIS30
29H	MVDIS7	MVDIS6	MVDIS5	MVDIS4	MVDIS3	MVDIS2	MVDIS1	MVDIS0
2AH	SHRPO31	SHRPO30	SHRPO21	SHRPO20	SHRPO11	SHRPO10	SHRPO01	SHRPO00
2BH	SHRPN31	SHRPN30	SHRPN21	SHRPN20	SHRPN11	SHRPN10	SHRPN01	SHRPN00
2CH	SHPIC7	SHPIC6	SHPIC5	SHPIC4	SHPIC3	SHPIC2	SHPIC1	SHPIC0
2DH	SVPIC7	SVPIC6	SVPIC5	SVPIC4	SVPIC3	SVPIC2	SVPIC1	SVPIC0
2EH	SHDIS07	SHDIS06	SHDIS05	SHDIS04	SHDIS03	SHDIS02	SHDIS01	SHDIS00
2FH	SHDIS17	SHDIS16	SHDIS15	SHDIS14	SHDIS13	SHDIS12	SHDIS11	SHDIS10
30H	SHDIS27	SHDIS26	SHDIS25	SHDIS24	SHDIS23	SHDIS22	SHDIS21	SHDIS20
31H	SHDIS37	SHDIS36	SHDIS35	SHDIS34	SHDIS33	SHDIS32	SHDIS31	SHDIS30
32H	SVDIS7	SVDIS6	SVDIS5	SVDIS4	SVDIS3	SVDIS2	SVDIS1	SVDIS0

Additional I^{2}C-bus register and PIP modes become available in sub addresses 20H to 32H.
An overview of these I^{2}C-bus registers is given in Table 6.

The meaning and relation of the I^{2}C-bus registers is shown in Fig.8. The background has a fixed size and can be fine positioned with BGHFP and BGVFP bits. The shown PIPs are only for one channel (main or sub), the other channel has the same control and can be displayed at the same time. The SDHFP and MDHFP bits determine the most left shown pixel for this channel in 256 steps of 4 pixels.
The SDVFP and MDVFP bits determine the most upper shown pixel for this channel in 256 steps of 1 line.
The SHPIC and MHPIC bits determine the horizontal picture size in 256 steps of 4 pixels, the minimum value is 4 pixels. The SVPIC and MVPIC bits determine the vertical picture size in 256 steps of 1 line, the minimum value is 1 line. The PIP mode is built-up of a maximum of four horizontal rows. The minimum is one row, more rows can be displayed by setting the vertical repetition rate number VRPN bits.
The distance between the rows can be set by the SVDIS and MVDIS bits. Every row is built-up of a maximum of four PIPs. The minimum is one PIP, additional PIPs can be added with the HRPN values. The SHRPO and MHRPO bits determine the offset distance between the starting points of the first PIP. The distances between the starting points of the PIPs on a row are determined by the SHDIS and MHDIS bits.

SA 20H CONTROL REGISTER

The PRIO bit sets the priority between main and sub channel. If PRIO is set to logic 0 priority is given to the sub channel which means that the sub channel PIPs, if present, are placed on top of the main PIPs. If PRIO is set to logic 1 it places the main PIPs on top of the sub PIPs.
The DPAL bit sets the correct default values for PAL on the display side. The background is enlarged from 238 lines/field to 288 lines/field.

The MPAL and SPAL bits set the acquisition area. When set to logic 1 the acquisition area is enlarged from 228 lines/field (NTSC) to 276 lines/field (PAL).

The MVRPN and SVRPN bits determine the number of repeated PIP rows. There is always one row visible of each channel. If no PIPs should be visible the PIP channel must be switched off (SA 00, bit 7 or bit 6).

SA 21H AND SA 2AH: HORIZONTAL REPETITION OFFSET REGISTERS FOR ROW 0 TO 3

The horizontal repetition offsets (MHRPO and SHRPO) are strongly related to the horizontal distance (MHDIS and SHDIS bits). These bits set for each row a certain grid of possible starting points for the PIPs in that row. Every grid point has a number 0 (the most left PIP), 1, 2 or 3.
The SHRPO and MHRPO bits determine the first grid number which will be displayed. This mechanism can be set for each row.

SA 22H AND SA 2BH: HORIZONTAL REPETITION NUMBER REGISTERS FOR ROW 0 TO 3

The horizontal repetition numbers (MHRPO and SHRPO) determine how many times the PIPs are repeated in a row, once the first PIP is displayed. The repeated PIPs stay in the grid determined by the SHDIS and MHDIS bits for that row. This mechanism can be set for each row independently.

SA 23H AND SA 24H; SA 2CH AND SA 2DH: PICTURE SIZE REGISTERS

The MHPIC and SHPIC bits determine the horizontal PIP size in 256 steps of 4 pixels. The MVPIC and SVPIC bits determine the vertical PIP size line in 256 steps of 1 line for NTSC or 256 steps of 2 lines for PAL.

SA 25H TO SA 29H; SA 2EH TO SA 32H: PICTURE DISTANCE REGISTERS

For each row the distance between starting points of PIPs can be set with the MHDIS and SHDIS bits in 256 steps of 4 pixels. The distance between two rows can be set with the MVDIS and SVDIS bits in 256 steps of 1 line.

Acquisition channel ADCs

Both channels convert the analog input signals to digital signals by means of two ADCs for each channel.
The internal input levels of the ADCs of each channel are equal and can be set by the AV_{refT} and AV_{refB} pins.
The reference levels are made internally by means of a resistor network which divides the analog voltage to a default set of preferred levels. External capacitors are needed to filter AC components on the reference levels.
The resolution of the ADCs is 8-bit; Differential Non-Linearity (DNL) is 7-bit; Integral Non-Linearity (INL) is 6-bit, and the sampling is done at the system frequency of 27 MHz for the Y-input. The U/V inputs are multiplexed and sampled at 13.5 MHz. The analog input signals are amplified to make maximum use of the dynamic range of the ADCs. A bias voltage V_{bias} is used for decoupling AC components on internal references. The inputs should be AC-coupled and an internal clamp circuit will clamp the input to AV_{refB} for the luminance channels and to $\frac{AV_{refT} - AV_{refB}}{2}$ for the chrominance channels.

The clamping starts at the leading edge of the burst key pulse.

Output DACs

The digitally processed signals are converted to analog signals by means of three 8-bit DACs. The output voltages of these DACs are default set by the DAV_{refT} pin for the top level and DAV_{refB} pin for the bottom level. Default values are 1.5 V.

External memory

For the external memory two VDRAMs of type Mitsubishi M5M442256 are foreseen. They have a storage capacity of 262144 words of 4-bit each and will be used in parallel.

It is also possible to use one 2 Mbit VDRAM of 262144 words of 8-bit. An overview of the timing diagrams is given in Fig.9.

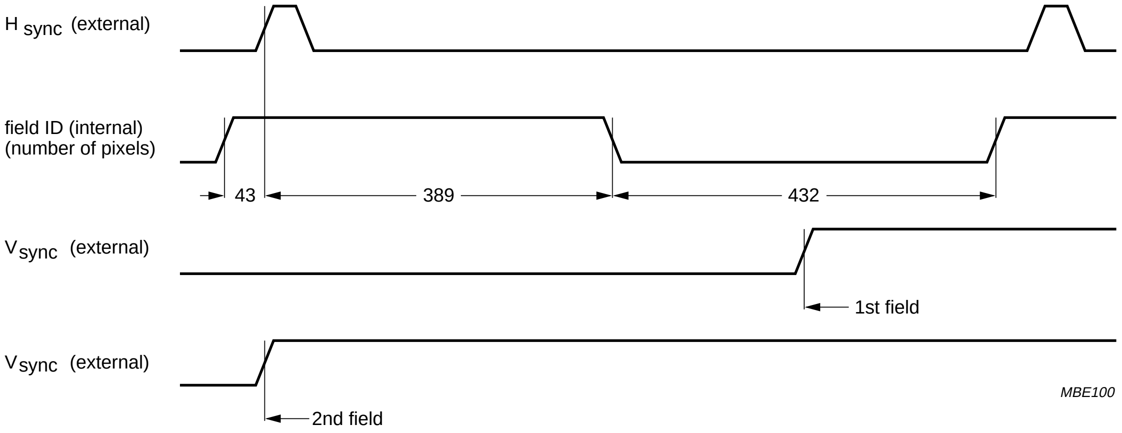


Fig.7 Vertical synchronization timing and field identification.

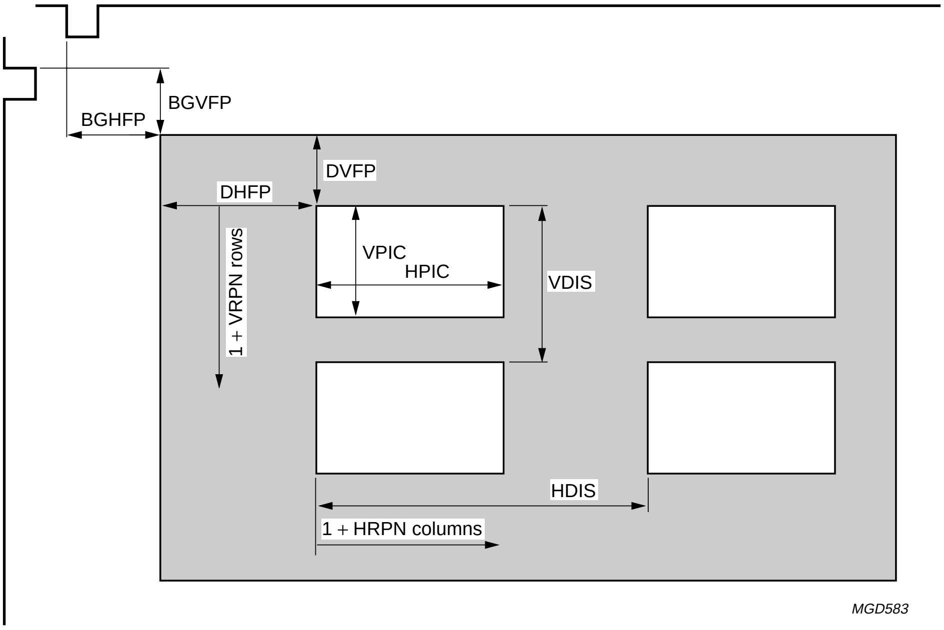
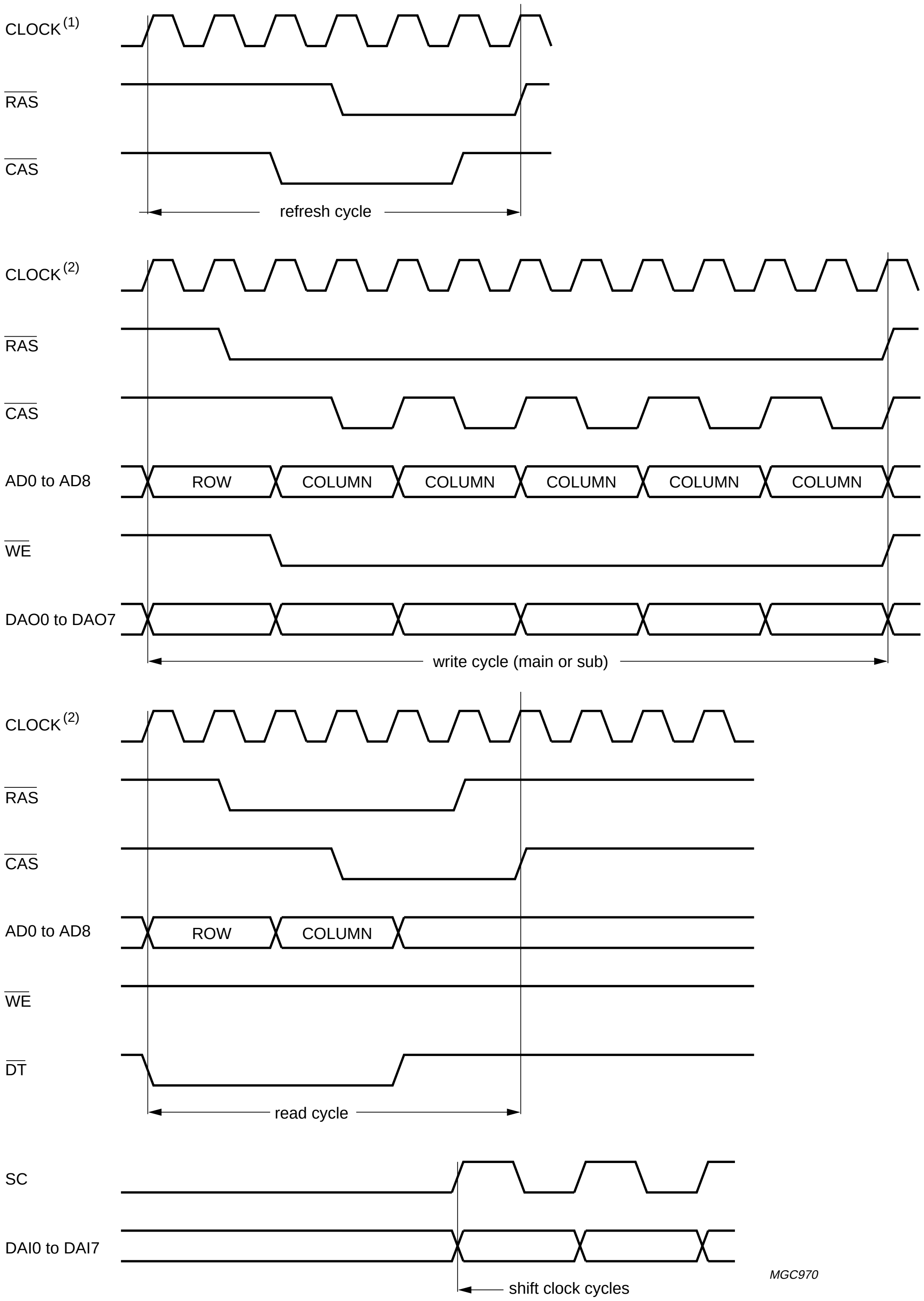


Fig.8 Relation of display I^{2}C-bus register.



(1) CLOCK = 13.5 MHz.
(2) CLOCK = 27 MHz.

Fig.9 VDRAM timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
P_{max}	maximum power dissipation	–	1.5	W
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	–25	+70	°C
V_{esd}	electrostatic discharge handling			
	Human body model		3000(1)	V
	Machine model		300(2)	V

Notes

1. Human body model: see *“UZW-B0/FQ-B302”*; The numbers of the quality specification can be found in the *“Quality Reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.
2. Machine model: see *“UZW-B0/FQ-A302”*; The numbers of the quality specification can be found in the *“Quality Reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	34	K/W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611 part E”*. The numbers of the quality specification can be found in the *“Quality Reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

CHARACTERISTICS

V_{DD} = 5.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	all positive supply voltages		4.5	5.0	5.5	V
V_{SS}	all ground voltages		–	0	–	V
$\Delta V_{DD(max)}$	maximum difference between supply voltages		–	0	100	mV
$\Delta V_{SS(max)}$	maximum difference between ground voltages		–	0	100	mV
I_{DDDQ}	quiescent current of digital supply voltages	note 1	–	0		μA
I_{MPVDDA}	main PLL supply current		–	5	–	mA
I_{SPVDDA}	sub PLL supply current		–	5	–	mA
I_{DPVDDA}	display PLL supply current		–	5	–	mA
I_{MAVDDA}	main ADCs supply current		–	40	–	mA
I_{SAVDDA}	sub ADCs supply current		–	40	–	mA
I_{DAVDDA}	display DACs supply current		–	20	–	mA
$I_{DDA(tot)}$	total analog supply current		–	115	–	mA
$I_{DDD(tot)}$	total digital supply current		–	tbf	–	mA
Analog-to-digital converter and clamping						
V_{refT}	top reference voltage	note 2	1.9	2.1	2.3	V
V_{refB}	bottom reference voltage	note 2	0.3	0.4	0.5	V
$V_{i(Y)(p-p)}$	input signal amplitude (peak-to-peak value)	$TM_2 = V_{SS}$; note 2	0.80	1.00	1.10	V
$V_{i(V)(p-p)}$	input signal amplitude (peak-to-peak value)	$TM_2 = V_{SS}$; note 2	0.84	1.05	1.16	V
$V_{i(U)(p-p)}$	input signal amplitude (peak-to-peak value)	$TM_2 = V_{SS}$; note 2	1.06	1.33	1.50	V
$V_{i(Y, U, V)(p-p)}$	input signal amplitude (peak-to-peak value)	note 2	1.2	1.5	1.6	V
I_i	input current	clamping off	–	0.1	–	μA
		clamping on	–	100	–	μA
C_i	input capacitance		–	5	–	pF
f_s	sample frequency rate	note 3	–	$1728H_{sync}$	–	MHz
RES	resolution		6	8	–	bit
DNL	differential non-linearity		–2.0	–	+2.0	LSB
INL	integral non-linearity		–4.0	–	+4.0	LSB
α_{cs}	channel separation		–	48	–	dB
PSRR	power supply rejection ratio		–	48	–	dB
V_{clampY}	clamping voltage level Y	note 4	–	V_{refB}	–	V
$V_{clampUV}$	clamping voltage level U/V	note 4	–	note 5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital-to-analog converter and output stage						
V_{refT}	top reference voltage		2.1	2.3	2.5	V
V_{refB}	bottom reference voltage		0.3	0.4	0.5	V
$V_{o(Y, U, V)}$	output signal amplitude	note 6	–	1.5	1.6	V
R_L	load resistance	note 6	75	220	10×10^3	Ω
C_L	load capacitance		0	–	50	pF
f_s	sample frequency rate	note 3	–	1728Hsync	–	MHz
RES	resolution		6	8	8	bit
DNL	differential non-linearity		–1.0	–	+1.0	LSB
INL	integral non-linearity		–1.0	–	+1.0	LSB
α_{cs}	channel separation		–	48	–	dB
PSRR	power supply rejection ratio		–	48	–	dB
PLL and clock generation acquisition						
$f_{i(PLL)}$	input frequency	note 3	14	15.75	18	kHz
PLL and clock generation display						
$f_{i(PLL)}$	input frequency	note 3	14	15.75	18	kHz

Notes

1. Digital clocks are silent, POR and TM_2 are connected to V_{DD}.
2. The V_{refT} and V_{refB} are made by a resistor division of the V_{DD}. They can be calculated with the formulas

$$V_{refT} = AV_{DD} \times \left(\frac{2.0}{5.0}\right) \text{V and } V_{refB} = AV_{DD} \times \left(\frac{0.4}{5.0}\right) \text{V}$$

3. The internal system frequency is 1728 times the H_{sync} input frequency for both the acquisition and display PLLs.
4. The Y-channel is clamped to the V_{refB} of the ADCs.
5. The UV-channel is clamped to $^1/_2(V_{refT} + V_{refB} + V_{LSB})$.
6. The gain of the SAB9077H is 1 under the condition that the R_L is 220 Ω.

DC CHARACTERISTICS FOR THE DIGITAL PART

All V_{DDD} pins = 4.5 to 5.5 V; T_{amb} = –20 to +75 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH level input voltage	HPF01	70	–	–	$\%V_{DD}$
		HPP01	70	–	–	$\%V_{DD}$
		HUP07	80	–	–	$\%V_{DD}$
		IOI41	70	–	–	$\%V_{DD}$
		HOU21	70	–	–	$\%V_{DD}$
V_{IL}	LOW level input voltage	HPF01	–	–	30	$\%V_{DD}$
		HPP01	–	–	30	$\%V_{DD}$
		HUP07	–	–	20	$\%V_{DD}$
		IOI41	–	–	30	$\%V_{DD}$
		HOU21	–	–	30	$\%V_{DD}$
V_{hys}	hysteresis voltage	HUP07	–	33	–	$\%V_{DD}$
V_{OH}	HIGH level output voltage	OPF20; I_{OL} = –2 mA; V_{DDD} = 4.5 V	4.1	–	–	V
		SPF20; I_{OL} = –2 mA; V_{DDD} = 4.5 V	4.1	–	–	V
V_{OL}	LOW level output voltage	IOI41; I_{OL} = +2 mA; V_{DDD} = 4.5 V	–	–	0.4	V
		OPF20; I_{OL} = +2 mA; V_{DDD} = 4.5 V	–	–	0.4	V
		SPF20; I_{OL} = +2 mA; V_{DDD} = 4.5 V	–	–	0.4	V
$\lvert I_{LI} \rvert$	input leakage current	HPF01; V_{DDD} = 5.5 V;	–	0.1	1	µA
		HPP01; V_{DDD} = 5.5 V;	–	0.1	1	µA
$\lvert I_{OZ} \rvert$	3-state output leakage current	IOI41; V_{DDD} = 5.5 V	–	0.2	5	µA
R_{pu}	internal pull-up resistor	HUP07	17	–	134	kΩ

Note

1. V_{in} is attached to the V_{DDD} or V_{SSD}.

AC CHARACTERISTICS FOR THE DIGITAL PART

V_{DDD} = 4.5 to 5.5 V (all V_{DDD} pins); T_{amb} = –20 to +75 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{sys}	system frequency	acquisition; note 1	–	27	30	MHz
		display; note 1	–	27	30	MHz
t_r	rise time		–	6	25	ns
t_f	fall time		–	6	25	ns

Notes

1. The internal system frequency is1728 times the H_{sync} input frequency for both the acquisition and display PLLs.

TEST AND APPLICATION INFORMATION

The application diagram for 1 FH mode in a standard configuration is shown in Fig.10. Two input signals MCVBS and SCVBS of different sources are processed by the SAB9077H and inserted by the YUV/RGB switch.

The synchronization of the display PLL is derived from the deflection circuit. The main signals are also led to the deflection circuit and the YUV/RGB switch where the SAB9077H signals can be inserted. The signals for deflection can also be taken from the main channel or sub-channel decoder.

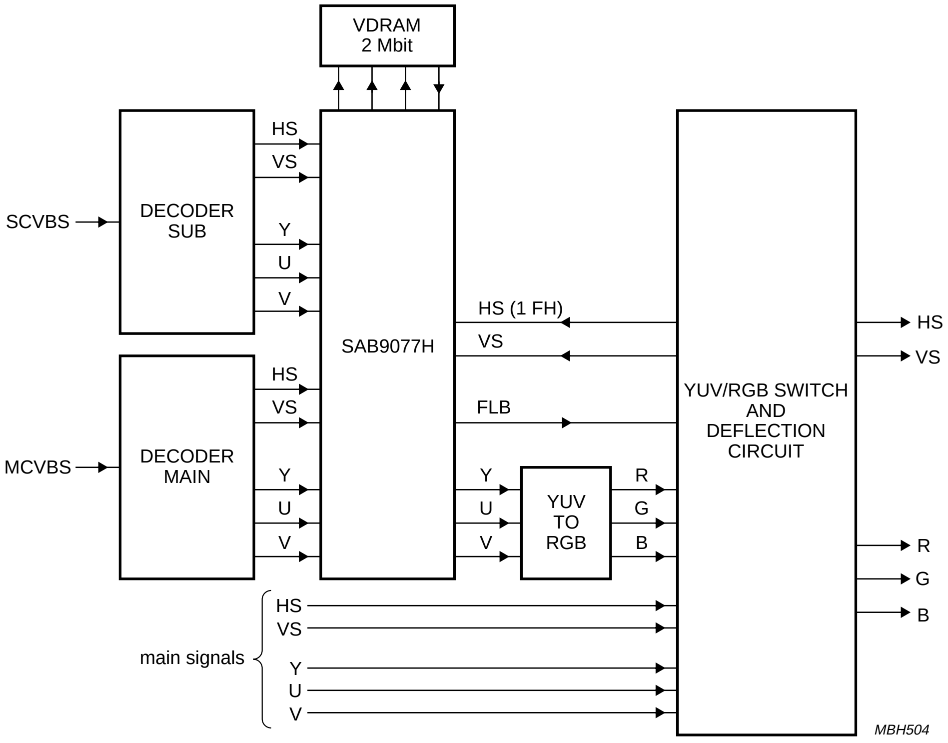
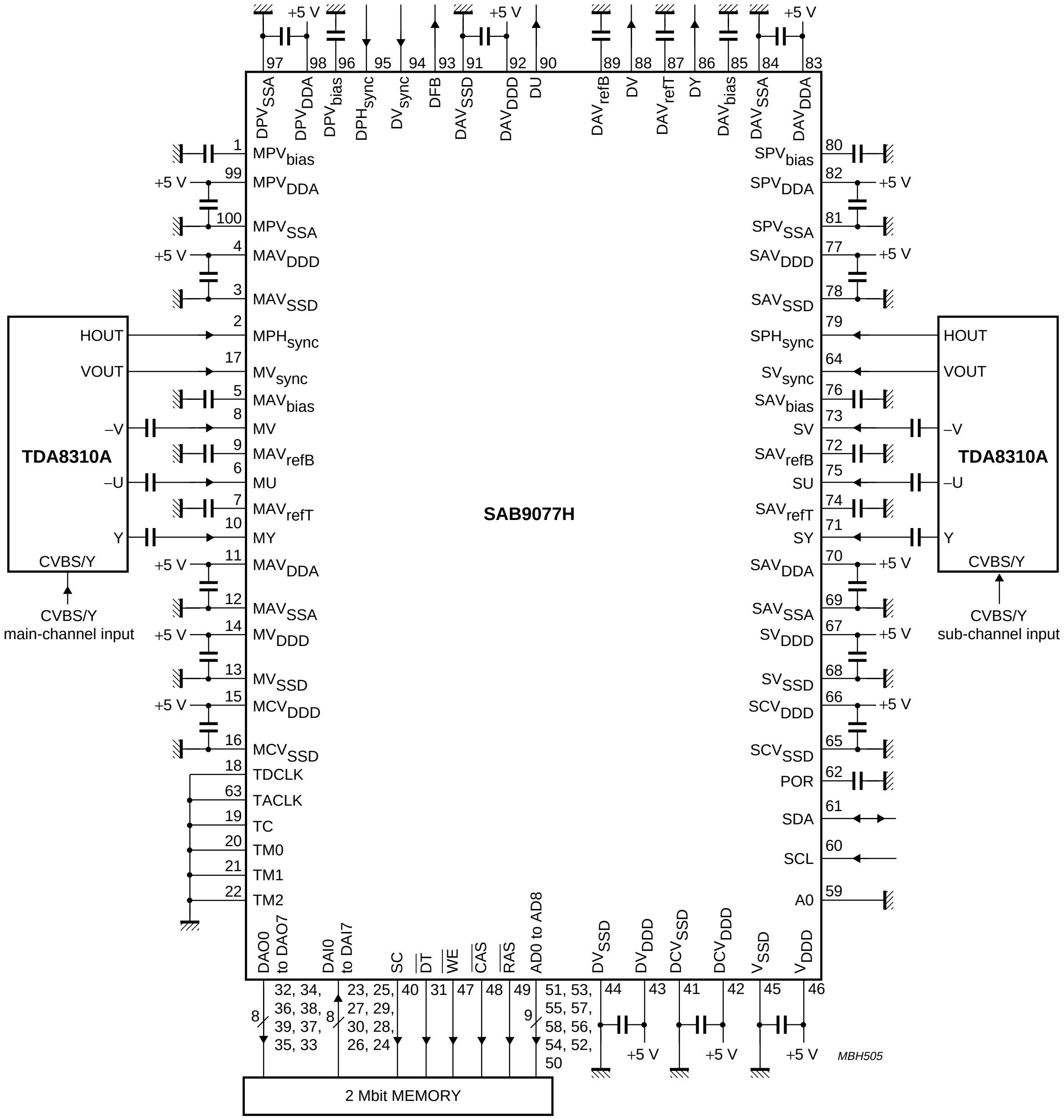


Fig.10 Application diagram for 1 FH mode.



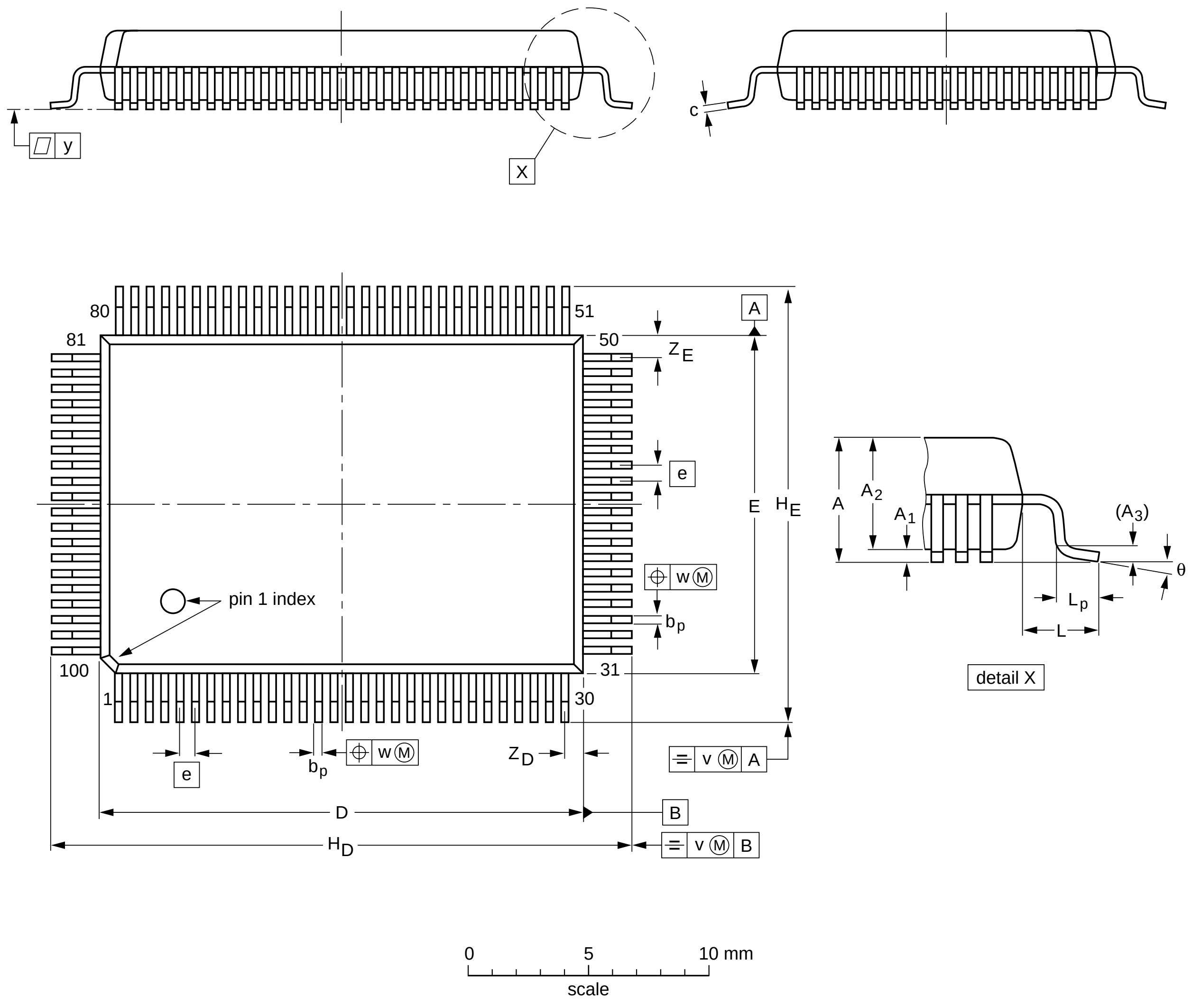
All capacitors are 100 nF.

On the application board a ground plane should be used.

Fig.11 Application diagram.

PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *“Quality Reference Handbook”* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

<table>
<tr><th colspan="2">Data sheet status</th></tr>
<tr><td>Objective specification</td><td>This data sheet contains target or goal specifications for product development.</td></tr>
<tr><td>Preliminary specification</td><td>This data sheet contains preliminary data; supplementary data may be published later.</td></tr>
<tr><td>Product specification</td><td>This data sheet contains final product specifications.</td></tr>
<tr><th colspan="2">Limiting values</th></tr>
<tr><td colspan="2">Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.</td></tr>
<tr><th colspan="2">Application information</th></tr>
<tr><td colspan="2">Where application information is given, it is advisory and does not form part of the specification.</td></tr>
</table>

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