TIME BASE CORRECTION DELAY LINE (TBC)

GENERAL DESCRIPTION

The SAD7630 is a charge-coupled device (CCD) dual variable delay line. It is designed for fault correction of composite video signals in compact disc video (CDV) applications. One line can be used to correct the time error of the composite video signal and the other line to correct the time error of the analogue audio carriers.

Features

- Variable clock frequency range of 13 to 24 MHz
- Separate power supply (V_{DDA} and V_{DDD}) to prevent interference between digital and analogue circuits
- Applicable for either PAL or NTSC players

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range						
analogue		V_{DDA}	4.75	5.0	5.5	V
digital		V_{DDD}	4.75	5.0	5.5	V
substrate bias		$-V_{SB}$	3.5	3.0	2.5	V
Supply current range	I_I = 0 mA; f_{CLK} = 16.6 MHz					
analogue		I_{DDA}	1	2	4	mA
digital		I_{DDD}	8	12	16	mA
substrate bias		$\|I_{SB}\|$	–	–	100	μA
Inputs						
V_{ref1}; V_{ref2}						
DC input voltage		V_{ref}	0	–	1.5	V
Input current level		I_{ref}	–	–	10	μA
V_{I1}; V_{I2}						
Signal amplitude	$V_I = V_{ref}$	V_I	0	1	1.6	V
Outputs						
V_{O1}; V_{O2}	R_{FZ} to V_{SB} = 47 kΩ					
DC output voltage	V_I to V_{ref} = 0 V	V_O	0.25	0.5	0.75	V
Operating ambient temperature range		T_{amb}	−25	–	+ 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38D).

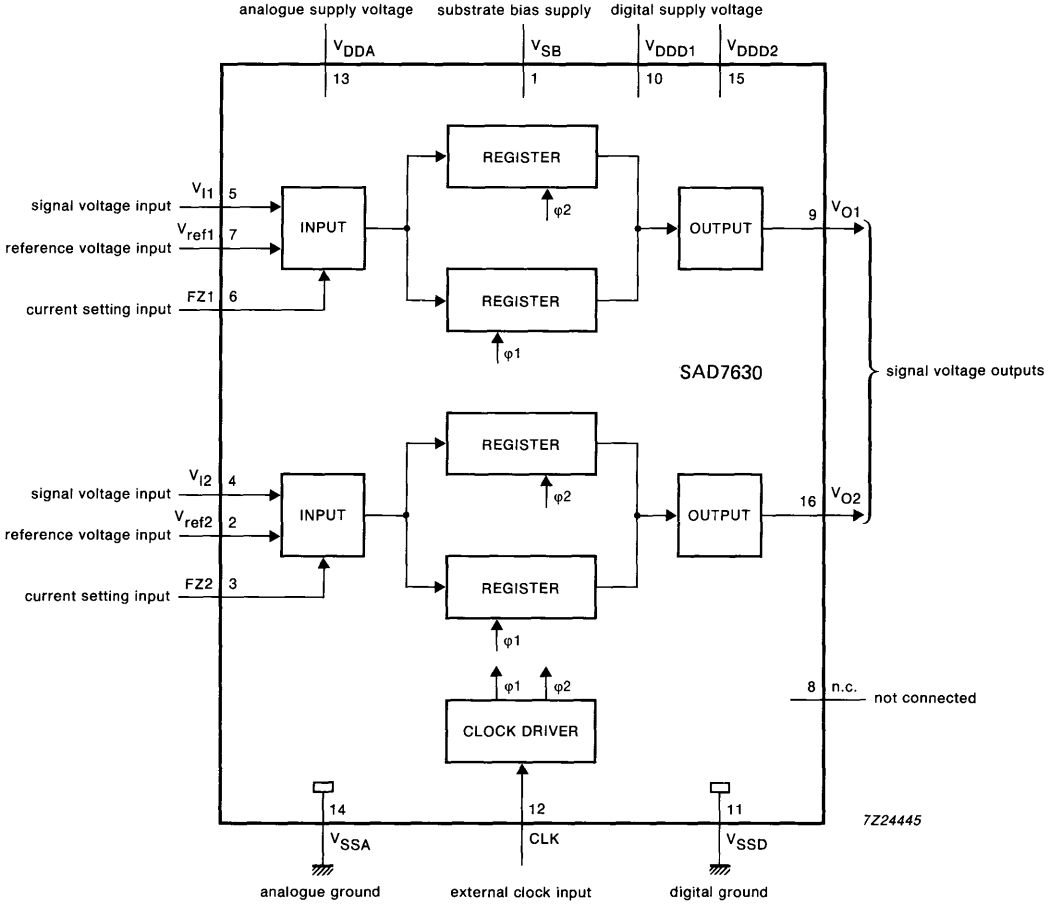


Fig.1 Block diagram.

PINNING

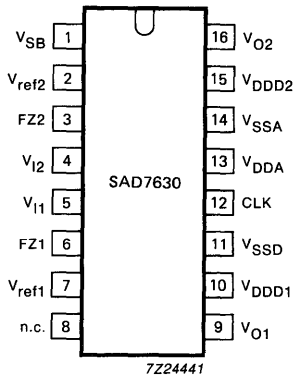


Fig.2 Pinning diagram.

DEVELOPMENT DATA

Power supply

V_{DDA}	analogue supply voltage
V_{SSA}	analogue ground
V_{DDD1}, V_{DDD2}	digital supply voltage
V_{SSD}	digital ground
V_{SB}	substrate bias supply

Input

CLK	external clock input

Inputs (analogue)

V_{ref1}, V_{ref2}	reference voltage inputs
V_{I1}, V_{I2}	signal voltage inputs
FZ1, FZ2	input stage current setting inputs

Outputs (analogue)

V_{O1}, V_{O2}	signal voltage outputs

FUNCTIONAL DESCRIPTION

Principle of variable delay

The input signal is sampled by clock pulses. At each pulse the samples are shifted one step in a 526 stage register. Two parallel multiplexed registers form one delay line. Each register is clocked by two clock pulses $\varphi 1$ and $\varphi 2$ which have a phase difference of 180°.

Effectively the two parallel multiplexed registers operate as a 1052 stage single line at the double clock frequency. This provides sufficient video bandwidth and delay range for CDV applications.

The delay time is inversely proportional to the clock frequency. Thus for a frequency range of 13 to 24 MHz the following values apply:

- Maximum delay time $1052 \div 13.10^6 = 80.92\ \mu s$
- Minimum delay time $1052 \div 24.10^6 = 43.83\ \mu s$
- Delay range $80.92 - 43.83 = 37.09\ \mu s$

Video input circuit

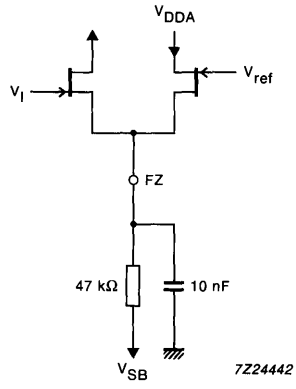


Fig.3 Video input circuit.

Each line has two inputs V_I and V_{ref}. The input signal amplitude is defined as $V_I - V_{ref}$.

Within the specified limits V_{ref} can be used to set the required DC input range for V_I. The FZ input can be used to set the current in the input stage.

In the nominal situation FZ is connected to V_{SB} (−3 V typ.) via a 47 kΩ resistor.

DEVELOPMENT DATA

Video input signal

PAL

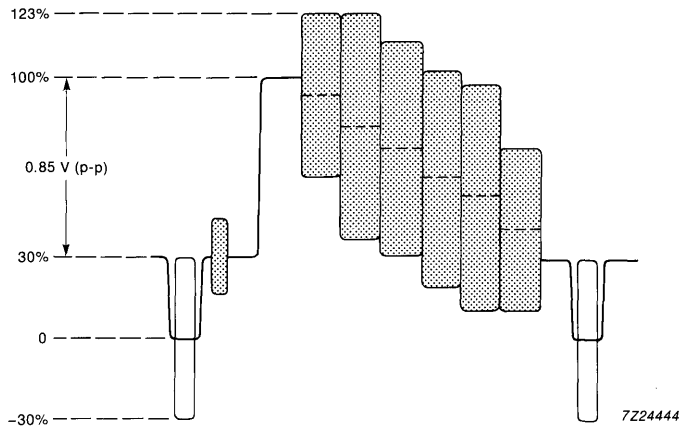


Fig.4 Video input signal for PAL.

The PAL line waveform of 100% saturated colour bars with special burst.
Tip sync to top-white = 100% ≙ 0.85 V (p-p).
Thus the maximum signal amplitude can become 150% x 0.85 V (p-p) = 1.3 V (p-p).

NTSC

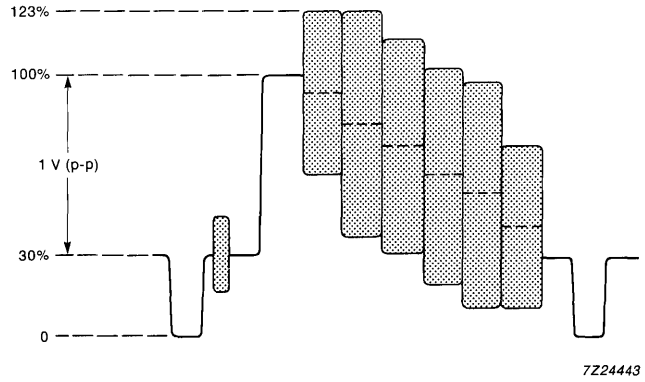


Fig.5 Video input signal for NTSC.

The NTSC line waveform of 100% saturated colour bars.
Tip sync to top-white = 100% ≙ 1.0 V (p-p).
Thus the maximum signal amplitude can become 123% x 1.0 V (p-p) = 1.23 V (p-p).

FUNCTIONAL DESCRIPTION (continued)

Supplies

Separate supply voltages (V_{DDA} and V_{DDD} are provided to prevent interference between analogue and digital circuits. However, it is still necessary to connect decoupling capacitors as near as possible to the respective ground pins. At decreasing V_{DDD} the transfer loss for high input frequencies at maximum f_{CLK} is increasing, therefore care must be taken not to exceed the specification limits of V_{DDD} (4.75 V to 5.5 V).

Clock circuit

The externally applied clock signal is internally converted to a squarewave. Flipflops generate two antiphase signals ($\varphi 1$ and $\varphi 2$) at half the clock frequency which operate the registers.

Output circuit

The output signals of the two multiplexed registers are demultiplexed and stored in a hold capacitor. A buffer stage following the hold capacitor is non-inverting and has a low output impedance (100 Ω typ.).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range					
analogue		V_{DDA}	−0.5	+7.0	V
digital		V_{DDD}	−0.5	+7.0	V
Input voltage	note 1	V_I	−0.5	V_{DD} + 0.5	V
Output voltage	note 1	V_O	−0.5	V_{DD} + 0.5	V
Maximum input current		I_{IM}	–	± 10	mA
Maximum output current		I_{OM}	–	± 10	mA
Maximum supply current in V_{SSA}; V_{SSD}		I_{SS}	–	−30	mA
Maximum supply current in V_{DDA}; V_{DDD}		I_{DD}	–	+ 30	mA
Total power dissipation		P_{tot}	–	500	mW
Storage temperature range		T_{stg}	−55	+ 150	°C
Operating ambient temperature range		T_{amb}	−25	+ 70	°C

Note to the Ratings

1. Input voltage should not exceed 7 V unless otherwise specified.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

T_{amb} = −25 to + 70 °C, unless otherwise specified; all parameters measured with the test circuit of Fig.6.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range						
analogue		V_{DDA}	4.75	5.0	5.5	V
digital		V_{DDD}	4.75	5.0	5.5	V
substrate bias		$-V_{SB}$	3.5	3.0	2.5	V
Supply current range	I_I = 0 mA; f_{CLK} = 16.6 MHz					
analogue		I_{DDA}	1	2	4	mA
digital		I_{DDD}	8	12	16	mA
substrate bias		$\|I_{SB}\|$	–	–	100	μA
Inputs						
V_{ref1}; V_{ref2}						
DC input voltage		V_{ref}	0	–	1.5	V
Input current level		I_{ref}	–	–	10	μA
V_{I1}; V_{I2}						
Signal amplitude	$V_I = V_{ref}$	V_I	0	1	1.6	V
Input impedance		R_I	1	–	–	MΩ
		C_I	–	–	10	pF
CLK						
Input voltage amplitude (peak-to-peak value)		$V_{AC(p-p)}$	0.30	0.60	0.90	V
DC output voltage		V_{DC}	1.5	–	3.5	V
Input current		I_{DC}	–	–	150	μA
Input frequency		f_{CLK}	13	–	24	MHz
FZ1; FZ2						
DC input voltage	w.r.t. V_{ref}	$-V_{DC}$	1.5	–	0.5	V
Outputs						
V_{O1}; V_{O2}	R_{FZ} to V_{SB} = 47 kΩ					
DC output voltage	V_I to V_{ref} = 0 V	V_O	0.25	0.5	0.75	V
	V_I to V_{ref} = 1.6 V	V_O	2.0	2.5	3.0	V
DC output current		$\|I_O\|$	–	–	1	mA
Output impedance		R_O	–	–	250	Ω
Maximum load impedance		R_L	–	–	10	kΩ
		C_L	–	–	10	pF

AC CHARACTERISTICS

V_{DDD} = 4.75 to 5.5 V; T_{amb} = −25 to +70 °C, unless otherwise specified; all parameters measured with the test circuit of Fig.6.

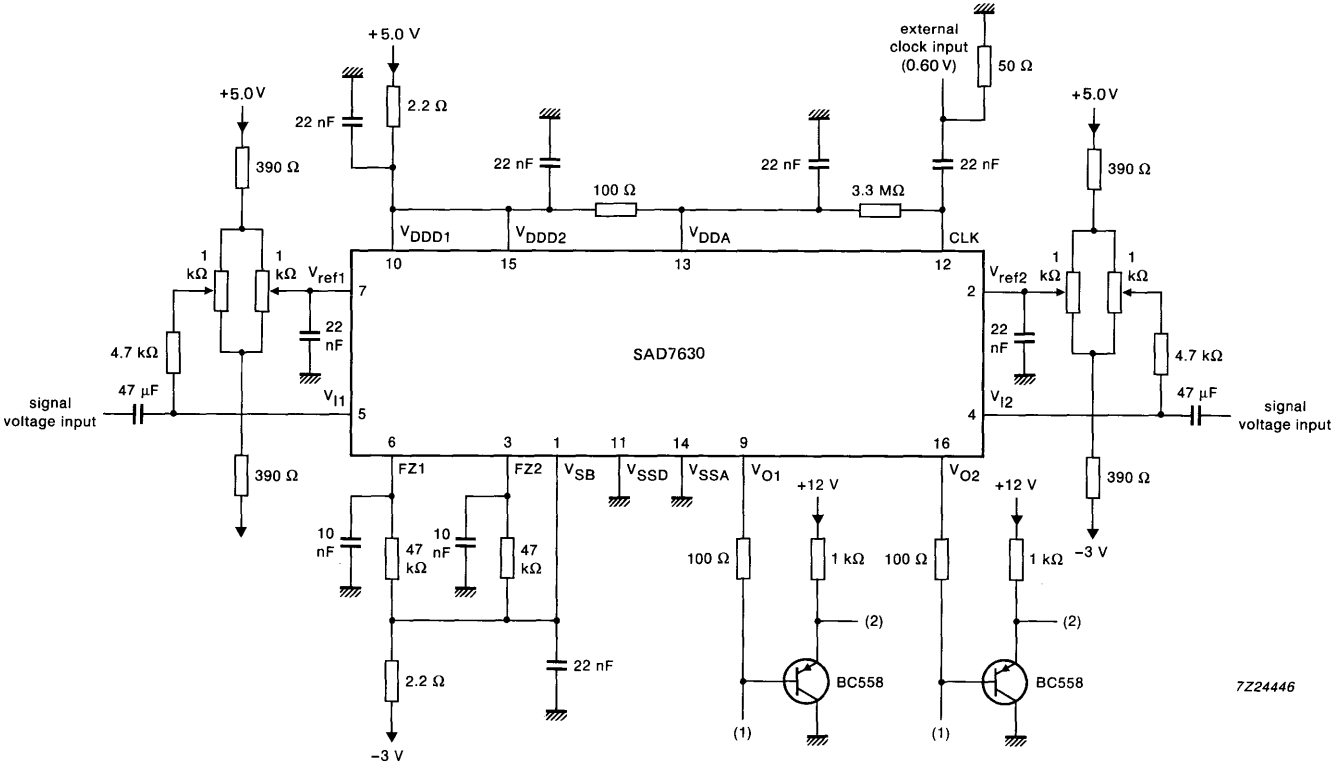
parameter	conditions	symbol	min.	typ.	max.	unit
Voltage gain	note 1	G_V	2	3	4	dB
Transfer loss at 5 MHz (w.r.t. 1 kHz)	f_{CLK} = 13 and 24 MHz	H_d	1.0	2.5	4.5	dB
Linearity error	note 2	L_e	–	–	6	%
Differential gain	note 2	G_d	–	–	5	%
Differential phase	note 2	α_d	–	–	5	deg.
DC output voltage		V_O	–	30	70	mV
Clock leakage voltage (RMS value)	f_{CLK} = 13 to 24 MHz					
6.5 MHz		V_{LCLK}	–	–	8	mV
13 MHz		V_{LCLK}	–	–	20	mV
19.5 MHz		V_{LCLK}	–	–	20	mV
Noise output voltage (RMS value)	B = 5 MHz (unweighted)	$V_{on(rms)}$	–	–	*	mV
Crosstalk attenuation between lines	note 3	a_x	–	–	*	dB
Distortion	note 4	d	–	–	10	%

DEVELOPMENT DATA

Notes to the AC characteristics

1. V_I to V_{ref} = 1 V(p-p); f_i = 1 kHz; f_{CLK} = 16.6 MHz.
2. V_I to V_{ref} = 1 V(p-p); f_{CLK} = 16.6 MHz.
3. V_I to V_{ref} = 1 V(p-p); f_i = 2 MHz; f_{CLK} = 16.6 MHz.
4. V_I to V_{ref} = 1.6 V(p-p); f_i = 1 kHz; f_{CLK} = 16.6 MHz.

* Value to be fixed.



(1) DC measurements.
(2) AC measurements.

Fig.6 Measuring circuit.