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SAF7115

Multistandard video decoder with super-adaptive comb filter, scaler and VBI data read-back via I²C-bus

Rev. 01 — 15 October 2008 Product data sheet

1. General description

The SAF7115 is a video capture device that, due to its improved comb filter performance and 10-bit video output capabilities, is suitable for various applications such as In-car video reception, In-car entertainment or In-car navigation.

The SAF7115 is a combination of a two channel analog preprocessing circuit and a high performance scaler.

The two channel analog preprocessing circuit includes source-selection, an anti-aliasing filter and Analog-to-Digital Converter (ADC) per channel, an automatic clamp and gain control, two Clock Generation Circuits (CGC1 and CGC2) and a digital multi standard decoder that contains two-dimensional chrominance/luminance separation utilizing an improved adaptive comb filter.

The high performance scaler has variable horizontal and vertical up and down scaling and a brightness/contrast/saturation control circuit.

The decoder is based on the principle of line-locked clock decoding and is able to decode the color of PAL, SECAM and NTSC signals into *ITU-601* compatible color component values. The SAF7115 accepts CVBS or S-video (Y/C) from TV or VCR sources as analog inputs, including weak and distorted signals.

The expansion port (X-port) for digital video (bi-directional half duplex, D1 compatible) can be used to either output unscaled video using 10-bit or 8-bit dithered resolution or to connect to other external digital video sources for reuse of the SAF7115 scaler features.

The enhanced image port (I-port) of the SAF7115 supports 8-bit and 16-bit wide output data with auxiliary reference data for interfacing, e.g. with VGA controller applications. It is also possible to output video in square pixel formats accompanied by a square pixel clock of the appropriate frequency.

The SAF7115 also incorporates provisions for capturing the serially coded data in the Vertical Blanking Interval (VBI-data) of several standards in parallel. Three basic options are available to transfer the VBI data to other devices:

- Capturing raw video samples, after interpolation to the required output data rate, using the scaler and transferring the data to a device connected to the I-port
- Slicing the VBI data using the built-in VBI data slicer (data recovery unit) and transferring the data to a device connected to the I-port
- Slicing the VBI data using the built-in VBI data slicer and reading out the sliced data through the I²C-bus (for several slow VBI data type standards only)

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The SAF7115 incorporates a frame locked audio clock generation. This function ensures that there is always the same number of audio samples associated with a frame, or a set of fields. This prevents the loss of synchronization between video and audio, during capture or playback. Furthermore, there is an option to use a second analog onboard PLL to enhance this audio clock to a low jitter frame locked audio clock.

The SAF7115 is controlled through the I^2C-bus with full write/read capability for all programming registers and a bit-rate of up to 400 kbit/s. See Ref. 1 for a detailed register description, pin strapping and applications.

2. Features

2.1 Video acquisition

- Six analog inputs, internal analog source selectors, e.g. (6 × CVBS) or (2 × Y/C and 2 × CVBS) or (1 × Y/C and 4 × CVBS)
- Two differential (bi-phase) video inputs as an alternative
- Two built-in analog anti-alias filters
- Two improved 9-bit CMOS ADCs in differential CMOS style at two-fold *ITU-656* oversampling (27 MHz)
- Fully programmable static gain or Automatic Gain Control (AGC) for the selected CVBS or Y/C channel
- Automatic Clamp Control (ACC) for CVBS, Y and C
- Switchable white peak control. Two 9-bit video CMOS ADCs, digitized CVBS or Y/C
- Signals are available on the expansion port (X-port)
- Requires only one crystal (32.11 MHz or 24.576 MHz) for all standards
- Independent gain and offset adjustments for raw data path

2.2 Comb filter video decoder

- Digital PLL for synchronization and clock generation from all standard and non-standard video sources e.g. consumer grade Video Tape Recorders (VTR)
- Automatic detection of 50 Hz and 60 Hz field frequencies
- Automatic recognition of all common broadcast standards
- Enhanced horizontal and vertical sync detection
- Luminance and chrominance signal processing for:
  - PAL BGDHIN
  - Combination-PAL N
  - PAL M
  - NTSC M
  - NTSC-Japan
  - NTSC 4.43
  - SECAM (50 Hz/60 Hz)
- PAL delay line for correcting PAL phase errors
- Improved 2/4-line comb filter for two dimensional chrominance/luminance-separation operating with adaptive comb filter parameters.
  - Increased luminance and chrominance bandwidth for all PAL and NTSC-standards
  - Reduced cross color and cross luminance artefacts

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- Independent Brightness Contrast Saturation (BCS) - adjustment for decoder part
- User programmable sharpness control
- Detection of copy protected input signals:
  - According to Macrovision standard
  - Indicating the level of protection
- Automatic TV/VCR detection
- 10-bit wide video output at comb filter video decoder
- X-port video output either as:
  - Noise shaped 8-bit *ITU-656* video or
  - Full 10-bit *ITU-656* interface (DC-performance 9-bit)

2.3 Video scaler

- Horizontal and vertical down-scaling and up-scaling to randomly sized windows
- Horizontal and vertical scaling range: variable zoom to 1/64 (icon) (note: H and V zoom are restricted by the transfer data rates)
- Vertical scaling with linear phase interpolation and accumulating filter for anti-aliasing (6-bit phase accuracy)
- Conversion to square pixel format
- Generation of a video output stream with improved synchronization grid at the I-port
- Two independent programming sets for scaler part, to define two regions (e.g. for different scaling for VBI and active picture) per field or sequences over frames
- Fieldwise switching between decoder part and expansion port (X-port) input
- Brightness, contrast and saturation controls for scaled outputs

2.4 VBI data slicer

- Versatile VBI-data decoder, slicer, clock regeneration and byte synchronization, e.g.:
  - WST525/WST625 (CCST)
  - VPS
  - US/European Close Caption (CC)
  - WSS525 (CGMS), WSS625
  - US NABTS
  - VITC 525/VITC 625
  - Gemstar 1x
  - Gemstar 2x
  - Moji
- I^2C-bus read-back of the following decoded data types:
  - US Close Caption (CC)
  - European Close Caption (CC)
  - WSS525 (CGMS)
  - WSS625 (CGMS)
  - Gemstar 1x
  - Gemstar 2x

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2.5 Clock generation

- On-chip line locked clock generation according *ITU-601*
- Generation of a frame locked audio master clock to support a constant number of audio clocks per video field
- Second onboard analog Phase-Locked Loop (PLL) to be used for:
  - On-chip line locked square pixel clock generation for PAL and NTSC square pixel video output or
  - The generation of a low jitter frame locked audio clock from the audio master clock through reuse of the analog square pixel PLL. The audio clock frequencies supported are $256 \times f_s$, $384 \times f_s$ and $512 \times f_s$ (f_s = 32 kHz, 44.1 kHz or 48 kHz)

2.6 General features

- CMOS 3.3 V device with 5 V tolerant digital inputs and I/O ports
- Programming through serial I^2C-bus, full read-back ability by an external controller, bit-rate up to 400 kbit/s
- Software controlled power saving stand-by modes
- Boundary Scan Test circuit complies to the *IEEE Std. 1149.b1-1994*

3. Applications

- General industrial video applications
- In-car TV reception
- In-car entertainment
- In-car navigation platforms

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SAF7115HW	HTQFP100	plastic thermal enhanced thin quad flat package; 100 leads; body $14 \times 14 \times 1$ mm; exposed die pad	SOT638-1
SAF7115ET	TFBGA160	plastic thin fine-pitch ball grid array package; 160 balls	SOT1016-1

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5. Block diagram

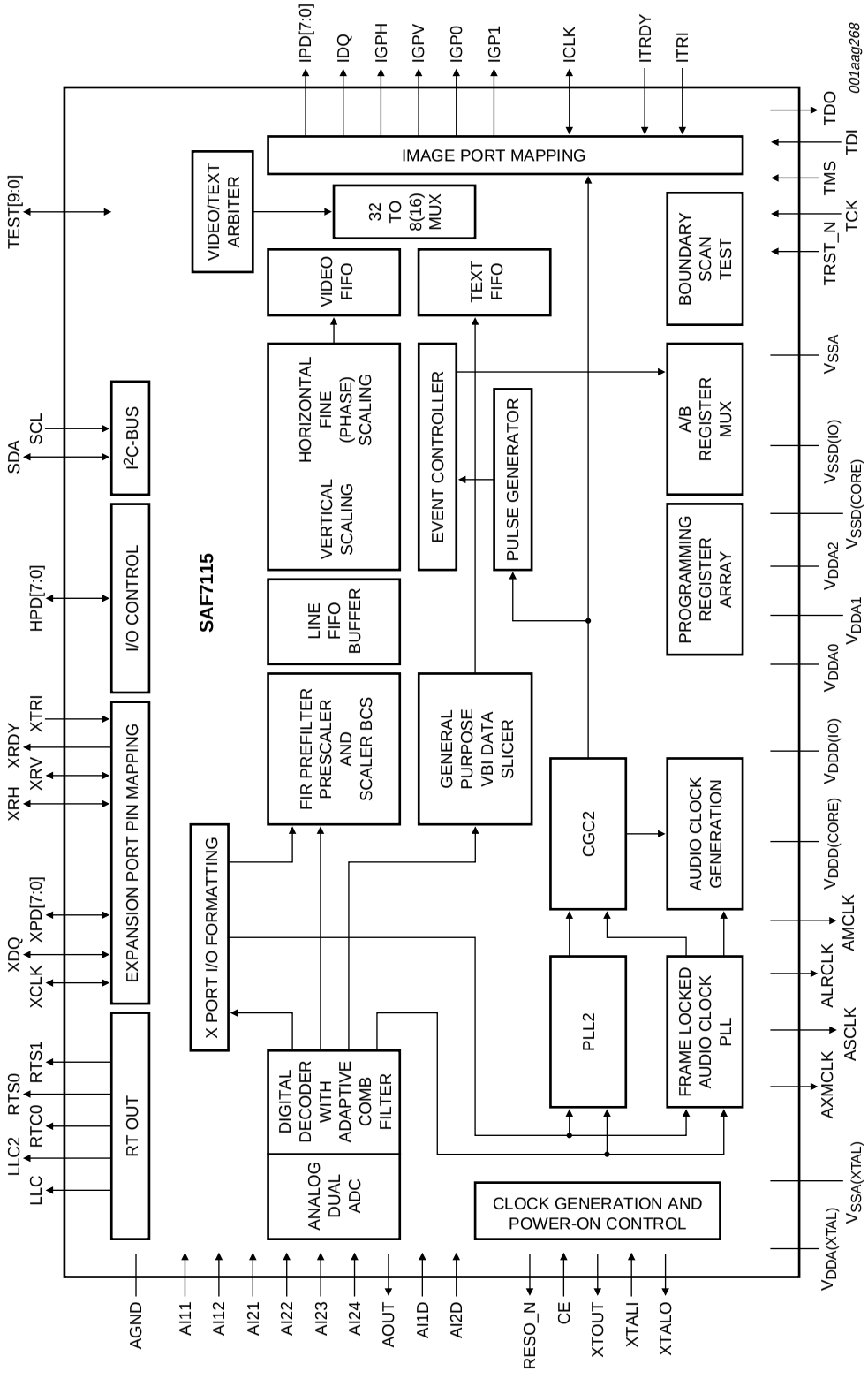

Fig 1. Block diagram

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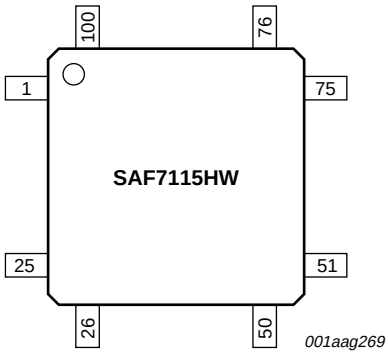
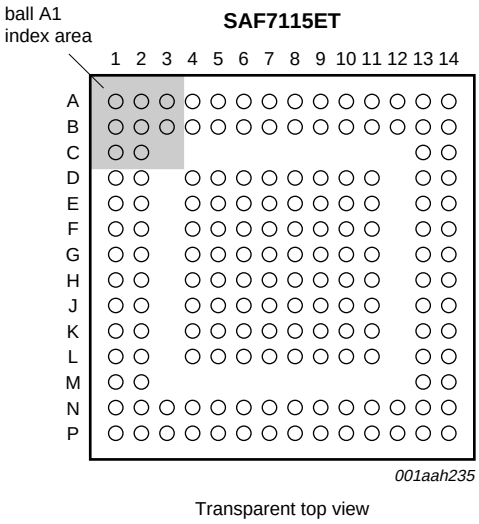
6. Pinning information

6.1 Pinning



a. HTQFP100



Transparent top view

b. TFBGA160

Fig 2. Pin configuration

Table 2. Pin allocation table (HTQFP100)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	$V_{DDD(IO)}$	2	TDO[1]	3	TDI[1]	4	XTOUT
5	$V_{SSA(XTAL)}$	6	XTALO	7	XTALI	8	$V_{DDA(XTAL)}$
9	V_{SSA}	10	AI24	11	V_{DDA2}	12	AI23
13	AI2D	14	AI22	15	V_{SSA}	16	AI21
17	V_{DDA1}	18	AI12	19	AI1D	20	AI11
21	AGND	22	AOUT	23	V_{DDA0}	24	V_{SSA}
25	$V_{DDD(IO)}$	26	$V_{SSD(IO)}$	27	CE	28	LLC
29	LLC2	30	RESO_N	31	SCL	32	SDA
33	$V_{DDD(CORE)}$	34	RTS0	35	RTS1	36	RTCO[1]
37	AMCLK	38	$V_{SSD(CORE)}$	39	ASCLK	40	ALRCLK
41	AMXCLK	42	ITRDY	43	$V_{DDD(CORE)}$	44	TEST0
45	ICLK	46	IDQ	47	ITRI	48	IGP0
49	IGP1	50	$V_{SSD(IO)}$	51	$V_{DDD(IO)}$	52	IGPV
53	IGPH	54	IPD7	55	IPD6	56	IPD5
57	IPD4	58	$V_{DDD(CORE)}$	59	IPD3	60	IPD2
61	IPD1	62	IPD0	63	$V_{SSD(CORE)}$	64	HPD7
65	HPD6	66	HPD5	67	HPD4	68	$V_{DDD(CORE)}$
69	HPD3	70	HPD2	71	HPD1	72	HPD0
73	TEST1	74	TEST2	75	$V_{DDD(IO)}$	76	$V_{SSD(IO)}$

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Table 2. Pin allocation table (HTQFP100) *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
77	TEST3	78	TEST4	79	TEST5	80	XTRI
81	XPD7	82	XPD6	83	$V_{DDD(CORE)}$	84	XPD5
85	XPD4	86	XPD3	87	XPD2	88	$V_{SSD(CORE)}$
89	XPD1	90	XPD0	91	XRV	92	XRH
93	$V_{DDD(CORE)}$	94	XCLK	95	XDQ	96	XRDY
97	TRST_N[1]	98	TCK[1]	99	TMS[1]	100	$V_{SSD(IO)}$

[1] See Table 4.

Table 3. Pin allocation table (TFBGA160)[1]

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
A1	$V_{DDD(IO)}$	A2	TMS[2]	A3	TRST_N[2]	A4	XRDY
A5	XCLK	A6	XRH	A7	XPD0	A8	$V_{SSD(CORE)}$
A9	XPD3	A10	XPD5	A11	XPD6	A12	XTRI
A13	TEST4	A14	$V_{DDD(IO)}$	-	-	-	-
Row B							
B1	XTOUT	B2	TDO[2]	B3	TCK[2]	B4	XDQ
B5	$V_{DDD(CORE)}$	B6	XRV	B7	XPD1	B8	XPD2
B9	XPD4	B10	$V_{DDD(CORE)}$	B11	XPD7	B12	TEST5
B13	TEST2	B14	TEST3	-	-	-	-
Row C							
C1	XTALO	C2	TDI[2]	C13	HPD0	C14	TEST1
Row D							
D1	XTALI	D2	$V_{SSA(XTAL)}$	D4	$V_{SSD(IO)}$	D5	$V_{SSD(IO)}$
D6	$V_{SSD(IO)}$	D7	$V_{SSD(IO)}$	D8	$V_{SSD(IO)}$	D9	$V_{SSD(IO)}$
D10	$V_{SSD(IO)}$	D11	$V_{SSD(IO)}$	D13	HPD2	D14	HPD1
Row E							
E1	$V_{DDA(XTAL)}$	E2	V_{SSA}	E4	$V_{SSD(IO)}$	E5	$V_{SSD(IO)}$
E6	$V_{SSD(IO)}$	E7	$V_{SSD(IO)}$	E8	$V_{SSD(IO)}$	E9	$V_{SSD(IO)}$
E10	$V_{SSD(IO)}$	E11	$V_{SSD(IO)}$	E13	$V_{DDD(CORE)}$	E14	HPD3
Row F							
F1	V_{DDA2}	F2	AI24	F4	$V_{SSD(IO)}$	F5	$V_{SSD(IO)}$
F6	$V_{SSD(IO)}$	F7	$V_{SSD(IO)}$	F8	$V_{SSD(IO)}$	F9	$V_{SSD(IO)}$
F10	$V_{SSD(IO)}$	F11	$V_{SSD(IO)}$	F13	HPD5	F14	HPD4
Row G							
G1	AI23	G2	AI2D	G4	$V_{SSD(IO)}$	G5	$V_{SSD(IO)}$
G6	$V_{SSD(IO)}$	G7	$V_{SSD(IO)}$	G8	$V_{SSD(IO)}$	G9	$V_{SSD(IO)}$
G10	$V_{SSD(IO)}$	G11	$V_{SSD(IO)}$	G13	HPD7	G14	HPD6
Row H							
H1	AI22	H2	V_{SSA}	H4	$V_{SSD(IO)}$	H5	$V_{SSD(IO)}$
H6	$V_{SSD(IO)}$	H7	$V_{SSD(IO)}$	H8	$V_{SSD(IO)}$	H9	$V_{SSD(IO)}$

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Table 3. Pin allocation table (TFBGA160)[1] *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
H10	$V_{SSD(IO)}$	H11	$V_{SSD(IO)}$	H13	IPD0	H14	$V_{SSD(CORE)}$
Row J							
J1	AI21	J2	V_{DDA1}	J4	$V_{SSD(IO)}$	J5	$V_{SSD(IO)}$
J6	$V_{SSD(IO)}$	J7	$V_{SSD(IO)}$	J8	$V_{SSD(IO)}$	J9	$V_{SSD(IO)}$
J10	$V_{SSD(IO)}$	J11	$V_{SSD(IO)}$	J13	IPD2	J14	IPD1
Row K							
K1	AI12	K2	AI1D	K4	$V_{SSD(IO)}$	K5	$V_{SSD(IO)}$
K6	$V_{SSD(IO)}$	K7	$V_{SSD(IO)}$	K8	$V_{SSD(IO)}$	K9	$V_{SSD(IO)}$
K10	$V_{SSD(IO)}$	K11	$V_{SSD(IO)}$	K13	$V_{DDD(CORE)}$	K14	IPD3
Row L							
L1	AI11	L2	AGND	L4	TEST6	L5	TEST7
L6	$V_{SSD(IO)}$	L7	$V_{SSD(IO)}$	L8	$V_{SSD(IO)}$	L9	$V_{SSD(IO)}$
L10	TEST8	L11	TEST9	L13	IPD5	L14	IPD4
Row M							
M1	AOUT	M2	V_{DDA0}	M13	IPD7	M14	IPD6
Row N							
N1	V_{SSA}	N2	CE	N3	LLC2	N4	SCL
N5	$V_{DDD(CORE)}$	N6	RTS1	N7	AMCLK	N8	ASCLK
N9	AMXCLK	N10	$V_{DDD(CORE)}$	N11	ICLK	N12	ITRI
N13	IGP1	N14	IGPH	-	-	-	-
Row P							
P1	$V_{DDD(IO)}$	P2	LLC	P3	RESO_N	P4	SDA
P5	RTS0	P6	RTCO[2]	P7	$V_{SSD(CORE)}$	P8	ALRCLK
P9	ITRDY	P10	TEST0	P11	IDQ	P12	IGP0
P13	IGPV	P14	$V_{DDD(IO)}$	-	-	-	-

[1] i.c.: internally connected; do not connect

[2] See Table 4.

6.2 Pin description

Table 4. Pin description

Symbol	Pin		Type[1]	Description
	HTQFP100	TFBGA160		
Supplies (analog)				
V_{DDA0}	23	M2	P	analog supply voltage 0[2]
V_{DDA1}	17	J2	P	analog supply voltage 1[3]
V_{DDA2}	11	F1	P	analog supply voltage 2[4]
$V_{DDA(XTAL)}$	8	E1	P	crystal analog supply voltage
V_{SSA}	9, 15 and 24	E2, H2 and N1	P	analog ground supply voltage
$V_{SSA(XTAL)}$	5	D2	P	crystal analog ground supply voltage

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Table 4. Pin description *...continued*

Symbol	Pin		Type[1]	Description
	HTQFP100	TFBGA160		
Supplies (digital)				
$V_{DDD(IO)}$	1, 25, 51 and 75	A1, A14, P1 and P14	P	I/O digital supply voltage
$V_{DDD(CORE)}$	33, 43, 58, 68, 83 and 93	B5, B10, E13, K13, N5 and N10	P	core digital supply voltage
$V_{SSD(CORE)}$	38, 63 and 88	A8, H14 and P7	P	core digital ground supply voltage
$V_{SSD(IO)}$	26, 50, 76 and 100	D4 to D11, E4 to E11, F4 to F11, G4 to G11, H4 to H11, J4 to J11, K4 to K11 and L6 to L9	P	I/O digital ground supply voltage
Analog inputs				
AGND	21	L2	P	analog signal ground reference for all AIx inputs
AI21	16	J1	AI	analog input 21
AI22	14	H1	AI	analog input 22
AI23	12	G1	AI	analog input 23
AI24	10	F2	AI	analog input 24
AI2D	13	G2	AI	differential input for ADC channel 2 (pins AI24, AI23, AI22 and AI21)[5]
AI11	20	L1	AI	analog input 11
AI12	18	K1	AI	analog input 12
AI1D	19	K2	AI	differential input for ADC channel 1 (pins AI12 and AI11)[5]
Analog output				
AOUT	22	M1	AO	analog test output (do not connect)
I^2C-bus				
SCL	31	N4	I (/O)/od	serial clock input (/output) with inactive output path
SDA	32	P4	I (/O)/od	serial data input (/output)
General control				
CE	27	N2	I/pu	chip enable or reset input (with internal pull-up)
RESO_N	30	P3	O	reset output (active low)
Audio clock				
ALRCLK	40	P8	(I/) O/st/pd	audio left/right clock output: can be strapped to supply through a 3.3 kΩ resistor indicating that the default 24.576 MHz crystal (internal pull-down) has been replaced by a 32.11 MHz crystal
AMCLK	37	N7	O	audio master clock output
AMXCLK	41	N9	I	audio master external clock input
ASCLK	39	N8	O	audio serial clock output

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Table 4. Pin description *...continued*

Symbol	Pin		Type[1]	Description
	HTQFP100	TFBGA160		
Real time signals				
RTCO	36	P6	(I/) O/st/pd	real time control output[6]
RTS1	35	N6	O	real time status or sync information, controlled by subaddresses 11h and 12h
RTS0	34	P5	O	real time status or sync information, controlled by subaddresses 11h and 12h
Clocks				
LLC	28	P2	O	line-locked system clock output (27 MHz nominal), for backward compatibility; use pin XCLK for new applications
LLC2	29	N3	O	line locked 1/2 clock output (13.5 MHz nominal) for backward compatibility; do not use for new applications
XTALI	7	D1	I	input terminal for 24.576 MHz (32.11 MHz) crystal oscillator or connection of external oscillator with TTL compatible square wave clock signal
XTALO	6	C1	O	24.576 MHz (32.11 MHz) crystal oscillator output; not connected if pin XTALI is driven by an external single-ended oscillator
XTOUT	4	B1	O	crystal oscillator output signal, auxiliary signal
Boundary scan test				
TCK	98	B3	I/pu	test clock for boundary scan test (with internal pull-up)[7]
TDI	3	C2	I/pu	test data input for boundary scan test (with internal pull-up)[7]
TDO	2	B2	O	test data output for boundary scan test[7]
TMS	99	A2	I/pu	test mode select for boundary scan test or scan test (with internal pull-up)[8]
TRST_N	97	A3	I/pu	test reset for boundary scan test (active LOW with internal pull-up); for board design without boundary scan connect TRST_N to 'ground', e.g. through $V_{SSD(CORE)}$ or $V_{SSD(IO)}$[8]
Test interface				
TEST9	-	L11	I/pd	do not connect, reserved for future extensions and for testing
TEST8	-	L10	AI	do not connect, reserved for future extensions and for testing
TEST7	-	L5	AI	do not connect, reserved for future extensions and for testing
TEST6	-	L4	I/pu	do not connect, reserved for future extensions and for testing
TEST5	79	B12	I/pu	do not connect, reserved for future extensions and for testing
TEST4	78	A13	O	do not connect, reserved for future extensions and for testing
TEST3	77	B14	I/pu	do not connect, reserved for future extensions and for testing
TEST2	74	B13	I/pu	do not connect, reserved for future extensions and for testing
TEST1	73	C14	I/pu	do not connect, reserved for future extensions and for testing
TEST0	44	P10	O	do not connect, reserved for future extensions and for testing
Image port (I-port)				
ICLK	45	N11	I/O	clock output signal for image port or optional asynchronous back end clock input
IDQ	46	P11	O	output data qualifier for image port (optional: gated clock output)
IGP1	49	N13	O	general purpose output signal 1; image port (controlled by subaddresses 84h and 85h); same functions as pin IGP0

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Table 4. Pin description *...continued*

Symbol	Pin		Type[1]	Description
	HTQFP100	TFBGA160		
IGP0	48	P12	O	general purpose output signal 0; image port (controlled by subaddresses 84h and 85h)
IGPH	53	N14	O	multipurpose horizontal reference output signal; image port (controlled by subaddresses 84h and 85h)
IGPV	52	P13	O	multipurpose vertical reference output signal; image port (controlled by subaddresses 84h and 85h)
IPD7	54	M13	O	MSB of image port data output
IPD6	55	M14	O	MSB – 1 of image port data output
IPD5	56	L13	O	MSB – 2 of image port data output
IPD4	57	L14	O	MSB – 3 of image port data output
IPD3	59	K14	O	MSB – 4 of image port data output
IPD2	60	J13	O	MSB – 5 of image port data output
IPD1	61	J14	O	MSB – 6 of image port data output
IPD0	62	H13	O	LSB of image port data output
ITRDY	42	P9	I/pu	target ready input, image port (with internal pull-up)
ITRI	47	N12	I (/O)/pd	image port output control signal, affects all I-port pins including ICLK, enable and active polarity is under software control (bits IPE in subaddress 87h) output path used for testing: scan output
Expansion port (X-port)				
XCLK	94	A5	I/O	clock I/O expansion port
XDQ	95	B4	I/O	data qualifier I/O expansion port
XPD7	81	B11	I/O	MSB of expansion-port data: in 8-bit video output mode: this signal represents the video bit 7; in 10-bit video output mode: this signal represents the video bit 9
XPD6	82	A11	I/O	MSB – 1 of expansion-port data: in 8-bit video output mode: this signal represents the video bit 6; in 10-bit video output mode: this signal represents the video bit 8
XPD5	84	A10	I/O	MSB – 2 of expansion-port data: in 8-bit video output mode: this signal represents the video bit 5; in 10-bit video output mode: this signal represents the video bit 7
XPD4	85	B9	I/O	MSB – 3 of expansion-port data: in 8-bit video output mode: this signal represents the video bit 4; in 10-bit video output mode: this signal represents the video bit 6
XPD3	86	A9	I/O	MSB – 4 of expansion-port data: in 8-bit video output mode: this signal represents the video bit 3; in 10-bit video output mode: this signal represents the video bit 5
XPD2	87	B8	I/O	MSB – 5 of expansion-port data: in 8-bit video output mode: this signal represents the video bit 2; in 10-bit video output mode: this signal represents the video bit 4
XPD1	89	B7	I/O	MSB – 6 of expansion-port data: in 8-bit video output mode: this signal represents the video bit 1; in 10-bit video output mode: this signal represents the video bit 3
XPD0	90	A7	I/O	expansion-port data: in 8-bit video output mode: this signal represents the video bit 0 (LSB); in 10-bit video output mode: this signal represents the video bit 2

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Table 4. Pin description *...continued*

Symbol	Pin		Type[1]	Description
	HTQFP100	TFBGA160		
XRDY	96	A4	O	task flag or read signal from scaler, controlled by bit XRQT (subaddress 83h)
XRH	92	A6	I/O	horizontal reference I/O expansion-port: in 10-bit video output mode: this signal represents the video bit 1
XRV	91	B6	I/O	vertical reference I/O expansion-port: in 10-bit video output mode: this signal represents the video bit 0 (LSB)
XTRI	80	A12	I/pd	X-port output control signal, affects all X-port pins (XPD[7:0], XRH, XRV, XDQ and XCLK) enable and active polarity is under software control (bits XPE in subaddress 83h)
Host port (H-port)				
HPD7	64	G13	I/O	MSB of host port data I/O, carries CbCr chrominance information in 16-bit video I/O modes
HPD6	65	G14	I/O	MSB – 1 of host port data I/O, carries CbCr chrominance information in 16-bit video I/O modes
HPD5	66	F13	I/O	MSB – 2 of host port data I/O, carries CbCr chrominance information in 16-bit video I/O modes
HPD4	67	F14	I/O	MSB – 3 of host port data I/O, carries CbCr chrominance information in 16-bit video I/O modes
HPD3	69	E14	I/O	MSB – 4 of host port data I/O, carries CbCr chrominance information in 16-bit video I/O modes
HPD2	70	D13	I/O	MSB – 5 of host port data I/O, carries CbCr chrominance information in 16-bit video I/O modes
HPD1	71	D14	I/O	MSB – 6 of host port data I/O, carries CbCr chrominance information in 16-bit video I/O modes
HPD0	72	C13	I/O	LSB of host port data I/O, carries CbCr chrominance information in 16-bit video I/O modes

[1] A = analog, I = input, O = output, P = power, st = strapping, pu = pull-up, pd = pull-down, od = open-drain.

[2] For CGC1 and CGC2.

[3] For analog inputs AI1x.

[4] For analog inputs AI2x.

[5] For normal operation connect pins AI1D and AI2D to ground through a capacitor. In principle both analog input stages can operate in differential mode, too, depending on the application. This may be interesting for differential video (CVBS). Please contact NXP for more information.

[6] This contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier phase and frequency and PAL sequence (according to RTC level 3.1, refer to external document *RTC Functional Specification* for details), can be strapped to supply through a 3.3 kΩ resistor to change the default I^2C-bus read and write addresses from 42h and 43h (internal pull-down) to 40h and 41h.

[7] According to the *IEEE1149.b1-1994* standard pins TDI and TMS are input pins with an internal pull-up transistor and TDO is a 3-state output pin. Pins TCK and TRST_N are also built with internal pull-up.

[8] This pin provides easy initialization of BST circuitry. Pin TRST_N can be used to force the Test Access Port (TAP) controller to the test-logic-reset state (normal operation) at once.

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7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
All ground pins connected together and grounded (0 V); all supply pins connected together.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDA0}	analog supply voltage 0	for CGC1 and CGC2		–0.5	+4.6	V
V_{DDA1}	analog supply voltage 1	for analog inputs AI1x		–0.5	+4.6	V
V_{DDA2}	analog supply voltage 2	for analog inputs AI2x		–0.5	+4.6	V
$V_{DDA(XTAL)}$	crystal analog supply voltage			–0.5	+4.6	V
$V_{DDD(CORE)}$	core digital supply voltage			–0.5	+4.6	V
$V_{DDD(IO)}$	I/O digital supply voltage			–0.5	+4.6	V
$V_{I(a)}$	analog input voltage			–0.5	+4.6	V
V_i	input voltage	at pins XTALI, SDA and SCL		–0.5	V_{DDx} + 0.5	V
$V_{I(D)}$	digital input voltage	outputs in 3-state		–0.5	+4.6	V
			[1]	–0.5	+5.5	V
ΔV_{SS}	ground supply voltage difference			-	100	mV
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
V_{esd}	electrostatic discharge voltage	human body model, all pins	[2]	-	±2000	V
		charged device model, corner pins	[3]	-	±750	V
		charged device model, all other pins	[3]	-	±500	V

[1] Condition for maximum voltage at digital inputs or I/O pins: 3.0 V < V_{DDD} < 3.6 V.

[2] Class 2 according to *EIA/JESD22-114*.

[3] Class C3B according to *AEC-Q100-011*.

8. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air			
		SAF7115ET	[1]	23	K/W
		SAF7115HW	[2]	35	K/W

[1] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly and use maximum areas for power and ground planes in the application PCB.

In order to meet the specified $R_{th(j-a)}$ value the exposed die pad of the package has to be soldered directly to the ground layer of the application PCB.

[2] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly and use maximum areas for power and ground planes in the application PCB.

The $R_{th(j-a)}$ value is calculated for a 4 layer PCB (100 × 100 mm^2) with at least 50 plated through-hole-vias at the center of the package (large ground area). This calculation assumes 80 % coverage for power and ground metal layers and a natural convection flow at top and bottom sides of the PCB.

Maximum ball temperature then is 110 °C, assuming ambient temperature $T_{amb(max)}$ = 85 °C.

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9. Characteristics

Table 7. Characteristics

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 25 °C; timings and levels refer to drawings and conditions illustrated in Figure 3 and Figure 4; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DDA0}	analog supply voltage 0	for CGC1 and CGC2		3.1	3.3	3.5	V
V_{DDA1}	analog supply voltage 1	for analog inputs AI1x		3.1	3.3	3.5	V
V_{DDA2}	analog supply voltage 2	for analog inputs AI2x		3.1	3.3	3.5	V
$V_{DDA(XTAL)}$	crystal analog supply voltage			3.1	3.3	3.5	V
$V_{DDD(CORE)}$	core digital supply voltage			3.0	3.3	3.6	V
$V_{DDD(IO)}$	I/O digital supply voltage			3.0	3.3	3.6	V
I_{DDA}	analog supply current	V_{DDAx} = 3.3 V; bits AOSL1 and AOSL0 = 0b	[1]				
		CVBS mode		-	81	-	mA
		Y/C mode		-	142	-	mA
I_{DDD}	digital supply current	X-port 3-state; 8-bit I-port out		-	108	-	mA
P	power dissipation	digital part; open pin AOUT		-	356	-	mW
		analog part; V_{DDAx} = 3.3 V					
		CVBS mode		-	267	-	mW
		Y/C mode		-	468	-	mW
		analog and digital parts					
		CVBS mode		-	623	-	mW
		Y/C mode		-	825	-	mW
		power-down mode	[2]	-	7	-	mW
		power-save mode	[3]	-	115	-	mW
Analog part							
$V_{i(p-p)}$	peak-to-peak input voltage	for normal video levels 1 V (p-p), –3 dB termination 18 Ω to 56 Ω and AC coupling required; coupling capacitor is 47 nF		-	0.7	-	V
I_{CL}	clamping current	V_I = 1 V DC		-	±8	-	µA
$\|Z_i\|$	input impedance	clamping current off		200	-	-	kΩ
C_i	input capacitance			-	-	10	pF
α_{cs}	channel separation	f_i < 5 MHz		-	-	–50	dB
9-bit analog-to-digital converters							
B	bandwidth	at –3 dB		-	7	-	MHz
φ_{dif}	differential phase	amplifier plus anti-alias filter bypassed		-	2	-	deg

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Table 7. Characteristics *...continued*

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 25 °C; timings and levels refer to drawings and conditions illustrated in Figure 3 and Figure 4; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_{dif}	differential gain	amplifier plus anti-alias filter bypassed		-	2	-	%
$f_{clk(ADC)}$	ADC clock frequency			25.4	–	28.6	MHz
DLE_{DC}	DC differential linearity error			-	0.7	-	LSB
ILE_{DC}	DC integral linearity error			-	1	-	LSB
ΔG_{ADC}	ADC gain difference		[4]	-	3	-	%
Digital inputs							
V_{IL}	LOW-level input voltage	pins SCL and SDA	[5]	–0.5	-	$+0.3 \times V_{CC(I2C\text{-}bus)}$	V
		any other pin, including pin XTALI	[5]	–0.3	-	+0.8	V
V_{IH}	HIGH-level input voltage	pins SCL and SDA	[5]	$0.7 \times V_{CC(I2C\text{-}bus)}$	-	$V_{CC(I2C\text{-}bus)} + 0.5$	V
		pin XTALI		2.0	-	$V_{DDA(XTAL)} + 0.3$	V
		any other pin		2.0	-	5.5	V
I_{LI}	input leakage current			-	-	1	µA
$I_{L(I/O)}$	leakage current (I/O)			-	-	10	µA
C_i	input capacitance	I/O at high-impedance		-	-	8	pF
Digital outputs[6]							
V_{OL}	LOW-level output voltage	pin SDA at 3 mA sink current		-	-	0.4	V
		all digital clocks		0	-	0.6	V
		for all other digital outputs		0	-	0.4	V
V_{OH}	HIGH-level output voltage	all digital output pins		2.4	-	$V_{DDD(IO)} + 0.5$	V
Clock output timing (LLC and LLC2)[7]							
$C_{o(L)}$	output load capacitance			15	-	50	pF
T_{cy}	cycle time	pin LLC		35	-	39	ns
		pin LLC2		70	-	78	ns
δ	duty cycle	for t_{CLKH}/T_{cy}; C_L = 40 pF		40	-	60	%
t_r	rise time	0.2 V to $V_{DDD(IO)}$ – 0.2 V		-	-	5	ns
t_f	fall time	$V_{DDD(IO)}$ – 0.2 V to 0.2 V		-	-	5	ns
t_d	delay time	between LLC and LLC2: measured at 1.5 V; C_L = 25 pF		–4	+1	+8	ns
Horizontal PLL							
$f_{hl(nom)}$	nominal horizontal line frequency	50 Hz field		-	15625	-	Hz
		60 Hz field		-	15734	-	Hz
$\Delta f_{hl}/f_{hl(nom)}$	horizontal line frequency deviation			-	-	5.7	%

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Table 7. Characteristics *...continued*

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 25 °C; timings and levels refer to drawings and conditions illustrated in Figure 3 and Figure 4; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Subcarrier PLL							
$f_{subc(nom)}$	nominal subcarrier frequency	PAL BGHI		-	4433619	-	Hz
		NTSC M		-	3579545	-	Hz
		PAL M		-	3575612	-	Hz
		PAL N		-	3582056	-	Hz
$\Delta f_{subc(lock-in)}$	subcarrier lock-in frequency			±400	-	-	Hz
Expansion port (X-port) output timing with XCLK clock output							
$C_{o(L)}$	output load capacitance			15	-	50	pF
T_{cy}	cycle time	XCLK output		35	-	39	ns
δ	duty cycle	for t_{XCLKH}/T_{cy}		35	-	65	%
t_r	rise time	0.6 V to 2.6 V		-	-	5	ns
t_f	fall time	2.6 V to 0.6 V		-	-	5	ns
Data and control signal output timing X-port including RT-port, related to XCLK output (for XPCK[1:0] 83h[5:4] = 01b)[7]							
$C_{o(L)}$	output load capacitance			15	-	50	pF
$t_{h(Q)}$	data output hold time		[8]	2	-	-	ns
t_{PD}	propagation delay	from positive edge of XCLK output	[8]	-	-	23	ns
Expansion port (X-port) input timing with XCLK clock input							
T_{cy}	cycle time	XCLK input		31	-	45	ns
δ	duty cycle	for t_{XCLKH}/T_{cy}		40	50	60	%
t_r	rise time			-	-	5	ns
t_f	fall time			-	-	5	ns
Data and control signal input timing X-port, related to XCLK input (for XPCK[1:0] 83h[5:4] = 11b);							
$t_{su(D)}$	data input set-up time		[9]	6	-	-	ns
$t_{h(D)}$	data input hold time		[9]	-	-	6	ns
$t_{h(Q)}$	data output hold time		[10]	-	3	-	ns
t_{PD}	propagation delay	from positive edge of XCLK input	[10]	-	23	-	ns
Image port (I-port) output timing with ICLK clock output							
$C_{o(L)}$	output load capacitance			15	-	50	pF
T_{cy}	cycle time			31	-	90	ns
δ	duty cycle	for t_{ICLKH}/T_{cy}; C_L = 40 pF		35	-	65	%
t_r	rise time	0.6 V to 2.6 V		-	-	5	ns
t_f	fall time	2.6 V to 0.6 V		-	-	5	ns
Image port (I-port) output timing with ICLK clock input							
T_{cy}	cycle time			31	-	100	ns
δ	duty cycle	for t_{ICLKH}/T_{cy}		40	50	60	%

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Table 7. Characteristics *...continued*

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 25 °C; timings and levels refer to drawings and conditions illustrated in Figure 3 and Figure 4; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	0.6 V to 2.6 V		-	-	5	ns
t_f	fall time	2.6 V to 0.6 V		-	-	5	ns
Data and control signal output timing I-port, related to ICLK output (for IPCK[1:0] 87h[5:4] = 11b)							
$C_{o(L)}$	output load capacitance	at all outputs		15	-	50	pF
$t_{h(Q)}$	data output hold time		[11]	3	-	-	ns
t_{PD}	propagation delay		[11]	-	-	23	ns
Data and control signal input timing I-port, related to ICLK output (for IPCK[1:0] 87h[5:4] = 11b)							
$t_{su(D)}$	data input set-up time		[12]	18	-	-	ns
$t_{h(D)}$	data input hold time		[12]	-	-	–2	ns
Data and control signal output timing I-port, related to ICLK input (for IPCK[1:0] 87h[5:4] = 11b)							
$C_{o(L)}$	output load capacitance	at all outputs		15	-	50	pF
$t_{h(Q)}$	data output hold time		[11]	3	-	-	ns
t_{PD}	propagation delay	from positive edge of LLC output	[11]	-	-	23	ns
Data and control signal input timing I-port, related to ICLK input (for IPCK[1:0] 87h[5:4] = 01b)							
$t_{su(D)}$	data input set-up time		[12]	12	-	-	ns
$t_{h(D)}$	data input hold time		[12]	-	-	2	ns
AMCLK clock output							
$C_{o(L)}$	output load capacitance			15	-	50	pF
t_r	rise time	0.6 V to 2.6 V		-	-	5	ns
t_f	fall time	2.6 V to 0.6 V		-	-	5	ns

[1] This setting connects pin AOUT to ground.

[2] Controlled through chip enable input (CE) from normal operation mode at typical supply voltage of $V_{DDD} = V_{DDA} = 3.3$ V.

[3] I^2C-bus controlled through subaddress 88h set to xx00 1011b.

[4] The ADC gain difference is $\Delta G_{ADC} = \left(\frac{\text{maximum deviation}}{\text{minimum deviation}} - 1\right) \times 100$.

[5] $V_{CC(I2C\text{-}bus)}$ is the external supply voltage of the I^2C-bus (3.3 V or 5 V).

[6] The levels must be measured with load circuits; 1.2 kΩ at 3 V (TTL load); C_L = 50 pF.

[7] The effects of rise and fall times are included in the calculation of $t_{h(Q)}$ and t_{PD}. Timings and levels refer to drawings and conditions illustrated in Figure 3 and Figure 4.

[8] Valid for outputs: XPD [7:0], XRH, XRV, XDQ, RTS0, RTS1, RTCO

[9] Valid for inputs: XPD [7:0], HPD [7:0], XRH, XRV, XDQ

[10] Valid for output: XRDY

[11] Valid for outputs: IPD [7:0], HPD [7:0], IGPH, IGPV, IDQ, IGP1, IGP0

[12] Valid for input: ITRDY

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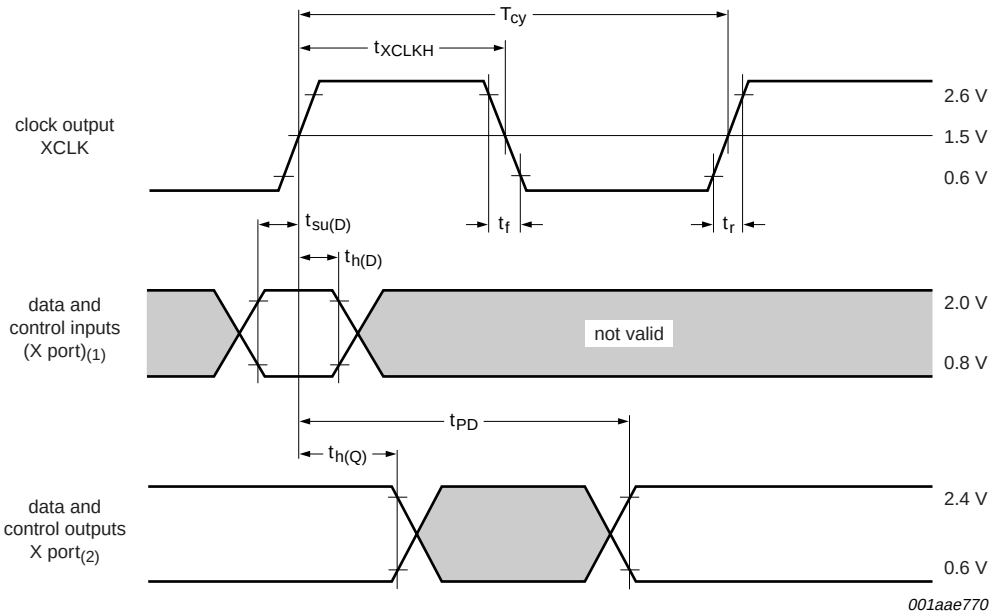
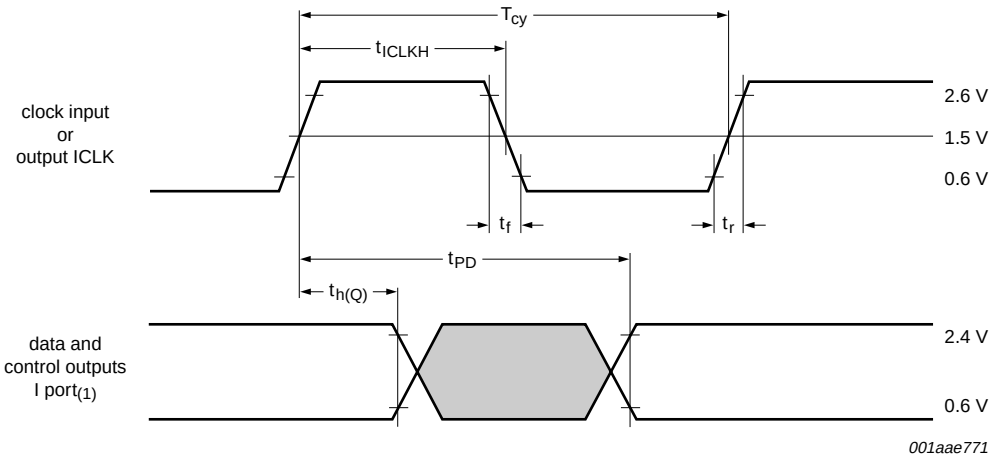


(1) See Table 7.

(2) See Table 7.

Fig 3. X-port input and output timing



(1) See Table 7.

Fig 4. I-port output timing, also valid for IX-port and H-port

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Table 8. Typical external fundamental crystal characteristics (see Section 10.1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Crystal oscillator for 32.11 MHz[1]							
$f_{xtal(nom)}$	nominal crystal frequency	3rd harmonics		-	32.11	-	MHz
$\Delta f/f_{xtal(nom)}$	nominal crystal frequency deviation			-	-	±100	ppm
Crystal specification (X1)							
C_L	load capacitance	3rd harmonics	[2]	-	-	8	pF
		fundamental	[2]	-	-	8	pF
R_S	series resistance	3rd harmonics		-		50	Ω
		fundamental		-	-	60	Ω
C_0	shunt capacitance	3rd harmonics		-	-	4.3	pF
		fundamental		-	-	3.3	pF
Crystal oscillator for 24.576 MHz[1]							
$f_{xtal(nom)}$	nominal crystal frequency	3rd harmonics		-	24.576	-	MHz
$\Delta f/f_{xtal(nom)}$	nominal crystal frequency deviation			-	-	±70	ppm
Crystal specification (X1)							
C_L	load capacitance	3rd harmonics	[2]	-	-	10	pF
		fundamental	[2]	-	-	20	pF
R_S	series resistance	3rd harmonics		-	40	80	Ω
		fundamental		-	-	60	Ω
C_0	shunt capacitance	3rd harmonics		-	-	3.5	pF
		fundamental		-	-	7	pF

[1] The crystal oscillator drive level is typical 0.28 mW.

[2] Effect from C_0 excluded.

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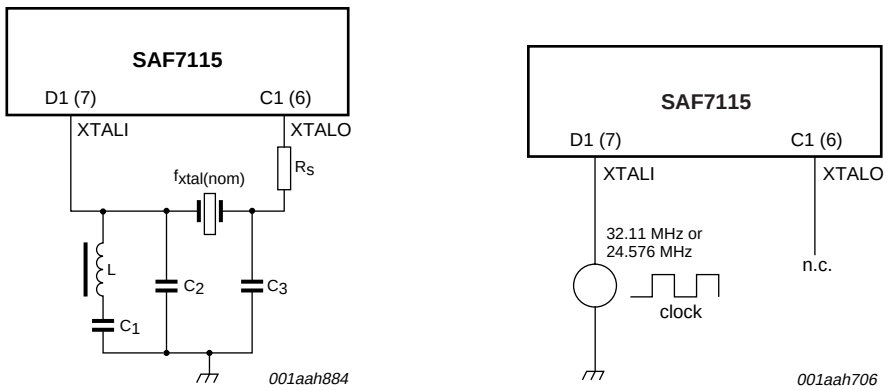
10. Application information

10.1 Oscillator applications

10.1.1 Generic oscillator applications

Figure 5 shows the generic oscillator circuit with quartz crystals and with direct clock input. Table 9 shows configuration examples for different quartz crystals.



a. Generic oscillator circuit

b. With direct clock.

Fig 5. Oscillator applications (see Table 9)

Table 9. Configuration examples quartz crystal (see Figure 5)

Example	Quartz crystal[1]			Oscillator circuit				
	Type	$f_{xtal(nom)}$ (MHz)	C_L (pF)	L (µH)	C_1 (nF)	C_2 (pF)	C_3 (pF)	R_S (Ω)[2]
1	3rd harmonic	32.11	8	4.7	1	15	15	0
2	3rd harmonic	24.576	8	4.7	1	18	18	0
3	fundamental	32.11	20	none	none	33	33	0
4	fundamental	32.11	8	none	none	10	10	0
5	fundamental	24.576	8	none	none	15	15	0

[1] See Table 8.

[2] See Section 10.1.2.

10.1.2 Fundamental quartz crystals with restricted drive level

Leave out L and C_1 when using fundamental quartz crystal and restricted drive level (see Section 10.1.1). Use a series resistance R_S at pin XTALO, when the internal oscillator of the SAF7115 provides too much power P_{drive} to the selected quartz crystal. Note that the decreased crystal amplitude results in a lower drive level, but on the other hand the jitter performance will decrease.

10.2 PCB layout guidelines for oscillator applications

Place the quartz crystal on the PCB as close to pins XTALI and XTALO as possible to minimize susceptibility to noise from current loops. Minimize parasitic capacitances.

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11. Test information

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

11.2 Boundary scan test

The SAF7115 has built-in logic and 5 dedicated pins to support boundary scan testing which allows board testing without special hardware (nails). The SAF7115 follows the *IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture* set by the Joint Test Action Group (JTAG).

The 5 dedicated pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset (TRST_N), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported (see Table 10). Details about the JTAG BST-TEST can be found in specification *IEEE Std. 1149.1*.

Table 10. BST instructions supported by the SAF7115

Instruction	Description
BYPASS	this mandatory instruction provides a minimum length serial path (1-bit) between TDI and TDO when no test operation of the component is required
EXTEST	this mandatory instruction allows testing of off-chip circuitry and board level interconnections
SAMPLE	this mandatory instruction can be used to take a sample of the inputs during normal operation of the component; it can also be used to preload data values into the latched outputs of the boundary scan register
CLAMP	this optional instruction is useful for testing when not all ICs have BST; this instruction addresses the bypass register while the boundary scan register is in external test mode
IDCODE	this optional instruction will provide information on the components manufacturer, part number and version number

11.2.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in the functional mode. The reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To compensate for the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the TRST_N pin LOW.

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11.2.2 Device identification codes

A device identification register is specified in *IEEE Std. 1149.1b-1994*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and the determination of the version number of ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between TDI and TDO of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller and this code can be subsequently shifted out. This code can be used at board level to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO); see Figure 6.

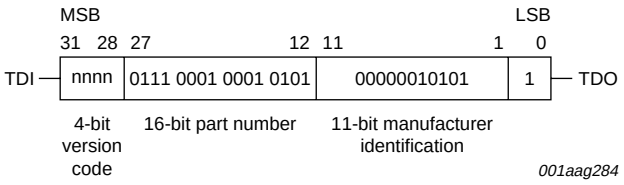

Fig 6. 32 bits of identification code

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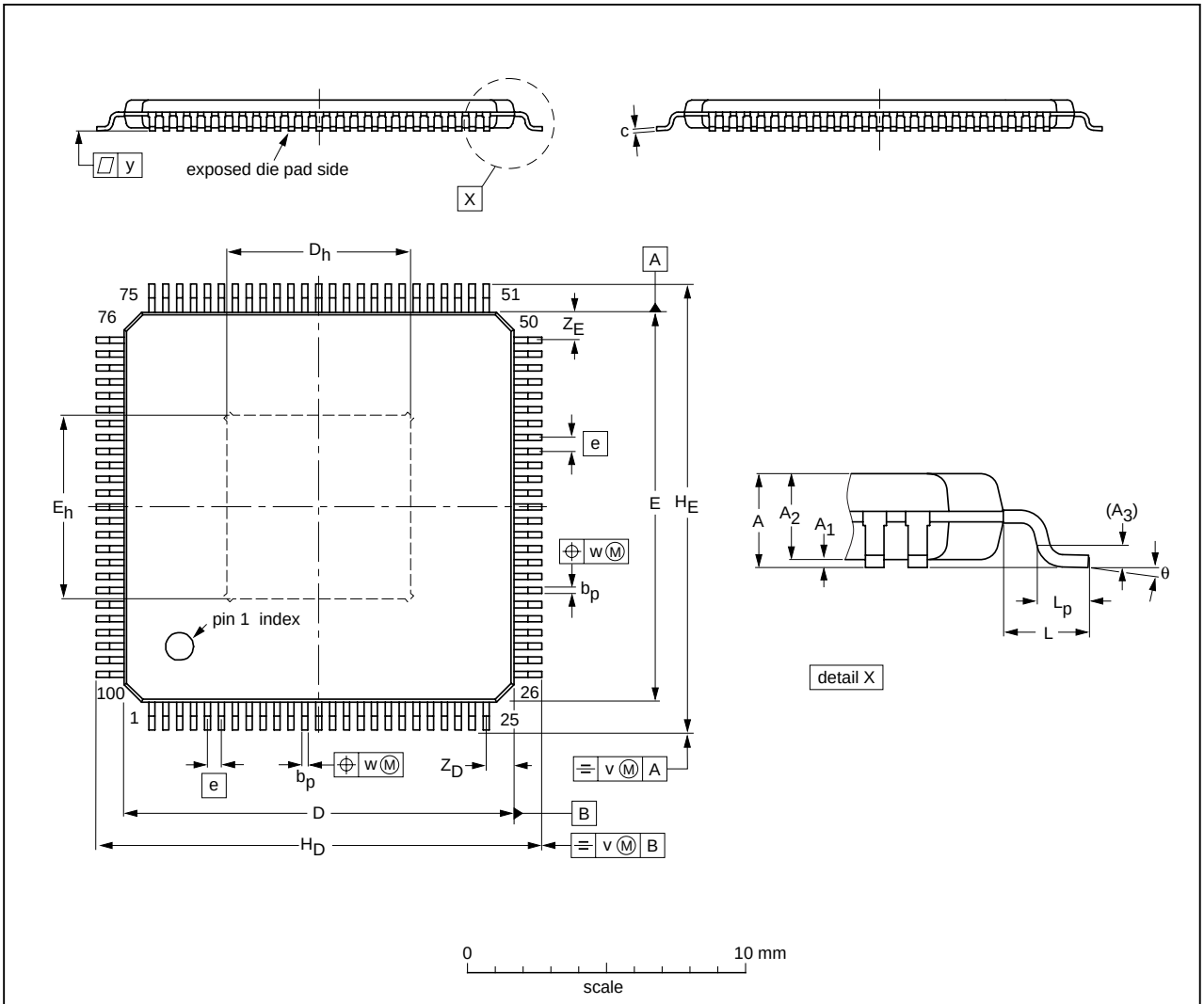
12. Package outline

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed die pad

SOT638-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-1		MS-026				~~03-04-07~~ 05-02-02

Fig 7. Package outline HTQFP100 (SOT638-1)

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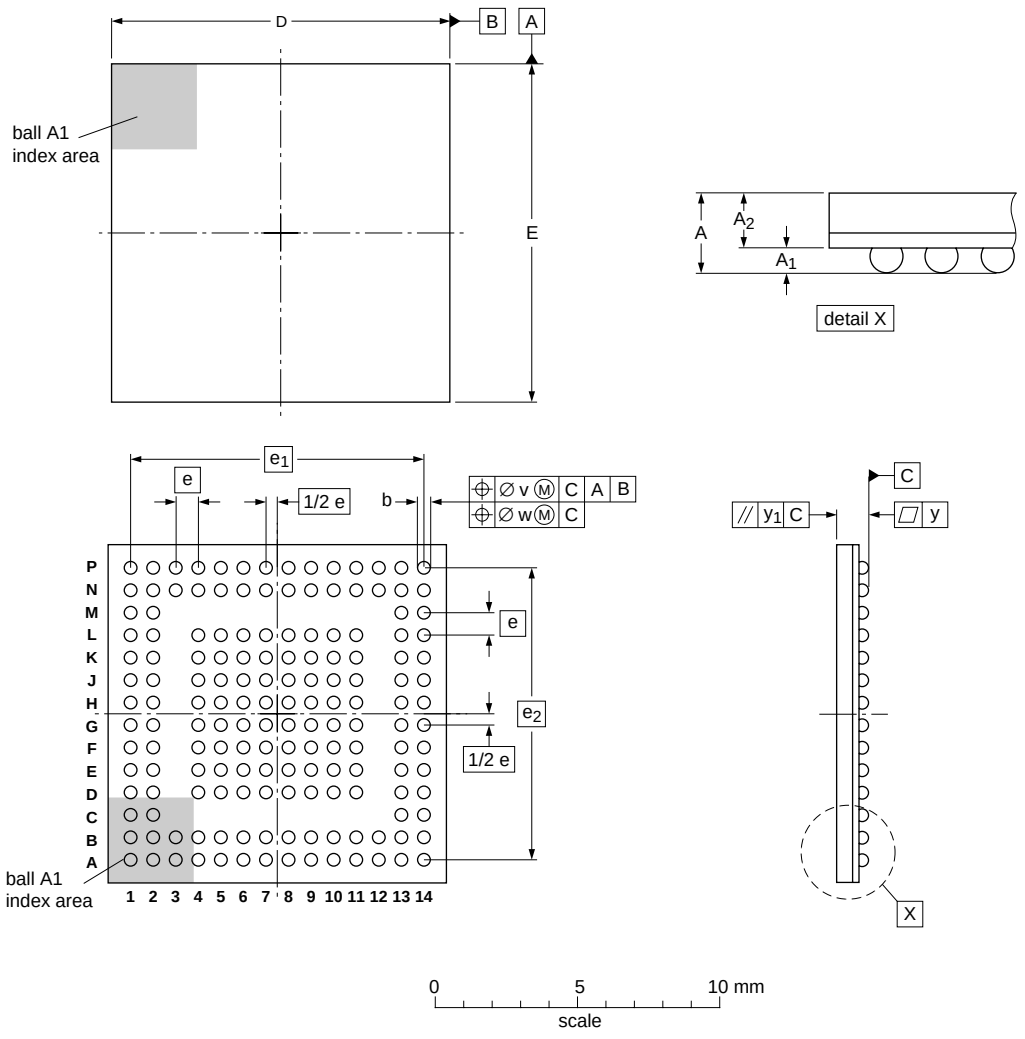
TFBGA160: plastic thin fine-pitch ball grid array package; 160 balls **SOT1016-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.80 0.65	0.5 0.4	12.1 11.9	12.1 11.9	0.8	10.4	10.4	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1016-1		- - -				~~07-06-20~~ 07-07-27

Fig 8. Package outline TFBGA160 (SOT1016-1)

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13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 9.

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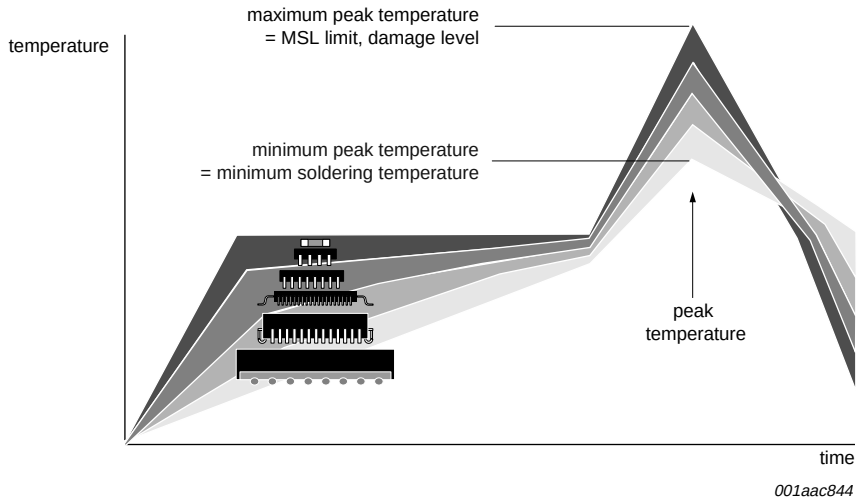

MSL: Moisture Sensitivity Level

Fig 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
ACC	Automatic Clamp Control
ADC	Analog-to-Digital Converter
AEC	Automotive Electronic Council
AGC	Automatic Gain Control
BCS	Brightness Contrast Saturation
CC	Close Caption
CCST	Chinese Character System Teletext
CGC	Clock Generation Circuit
CGMS	Copy Generation Management System
CMOS	Complementary MOS
CVBS	Composite Video Blanking Sync[1]
DC	Directed Current
EIA	Electronic Industries Alliance
ESD	ElectroStatic Discharge
FIFO	First In First Out
IC	Integrated Circuit
I^2C-bus	Inter-IC-bus
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output

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Table 13. Abbreviations *...continued*

Acronym	Description
ITU	International Telecommunication Union
JTAG	Joint Test Action Group
LLC	Line-Locked Clock
LSB	Least Significant Bit
MOS	Metal-Oxide-Semiconductors
MSB	Most Significant Bit
MUX	MUltipleXer
NABTS	North-American Broadcast Text System
NTSC	National Television Systems Committee
PAL	Phase Alternating Line
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
RT	Real Time
RTC	Real Time Control
SECAM	Systeme Electronique Coleur Avec Mémoire (French color TV standard)
SMD	Surface Mount Device
TAP	Test Access Port
TTL	Transistor-Transistor Logic
TV	TeleVision
US	United States of america
VBI	Vertical Blanking Interval
VCR	Video Cassette Recorder
VGA	Video Graphics Array
VITC	Vertical Interval Time Code
VPS	Video Program System
VTR	Video Tape Recorder
WSS	Wide Screen Signalling
WST	World System Teletext

[1] CVBS is also known as “composite video signal”.

15. Glossary

Arbiter — Electronic means to allocate access to shared resources.

H-port — Digital host port for CbCr video input or output.

I-port — Digital image port for scaled video data output.

Macrovision copy protection — The SAF7115 includes Macrovision detection only.

Moji — Japanese teletext. Moji means character.

X-port — Digital video expansion port (X-port), for unscaled digital video input and output.

Y/C — Luminance and separated modulated chrominance video signal.

YCbCr — Digital color coding format.

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16. References

[1] *SAF7115 User Manual*; please contact your local sales office (see Section 19).

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAF7115_1	20081015	Product data sheet	-	-

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18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 15 October 2008
Document identifier: SAF7115_1

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