

# Silicon-Based Technology

*Ultra High Speed and Low Power Memory*

**SB61L256C**

**32,768 x 8-Bits**

**STATIC CMOS RAM**

**PRELIMINARY**

## Description:

The SB61L256C series products are 32,768-words by 8-bits static RAMs fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the SB61L256C series products exhibit very high-speed performance with single +2.7-volt power supply while requiring very low power and no clock or refreshing to operate. The SB61L256C is packed in a standard 28-pin 300mil TSOP/SOJ.

## Features:

- 32,768-word x 8-bit organization
- Single +2.7-volt power supply
- Fully static operation — no clock or refreshing required
- LVTTL-compatible inputs and outputs
- Common I/O capability
- Low power consumption
  - Active: 105/95/85 mA (Max.)
  - Standby: 1 mA
- Very high speed access: 6.5/7/8 ns (Max.)
- 28-pin plastic 300 mil TSOP/SOJ package
- Output Enable (  $\overline{\text{OE}}$  ) available for very fast access

## Ordering Information:

Part Number	Package	Word Organization	Access Time ns(Max.)	Supply Voltage (Typ.)	Supply Current mA (Max.)	
					Operating	Standby
SB61L256C-6.5	28-Pin TSOP/SOJ (300 mil)	32Kx 8 bits	6.5	2.7V± 5%	105	1
SB61L256C-7			7		95	
SB61L256C-8			8		85	

The information in this document is subject to change without notice



**Silicon-Based Technology Corporation**

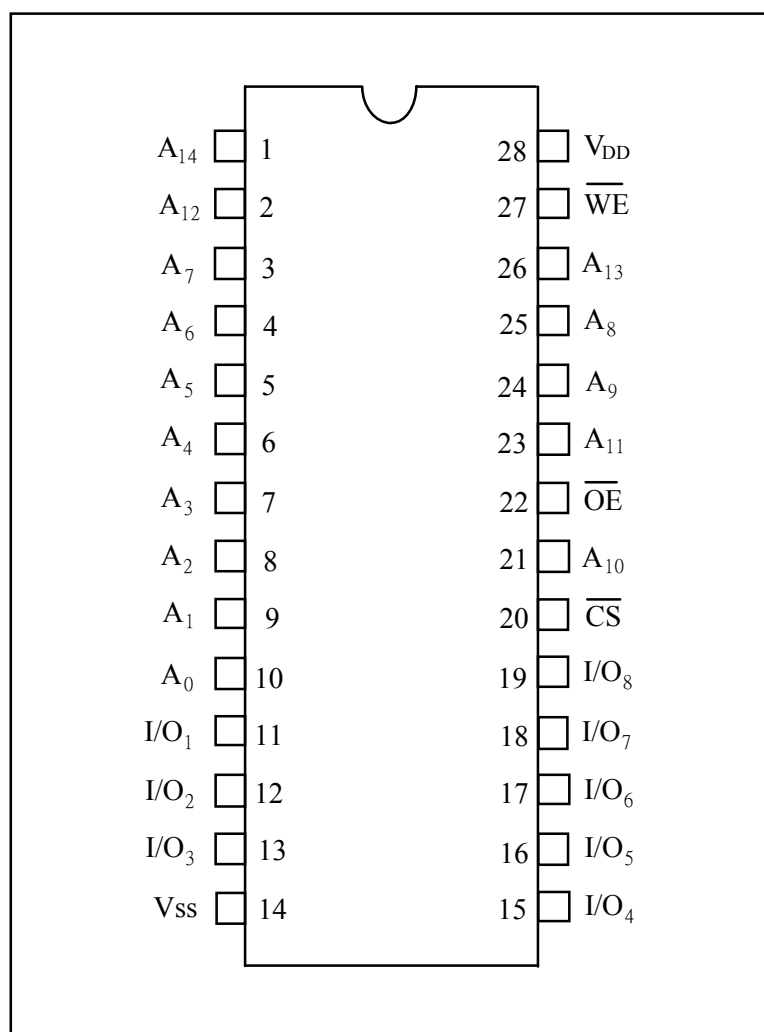
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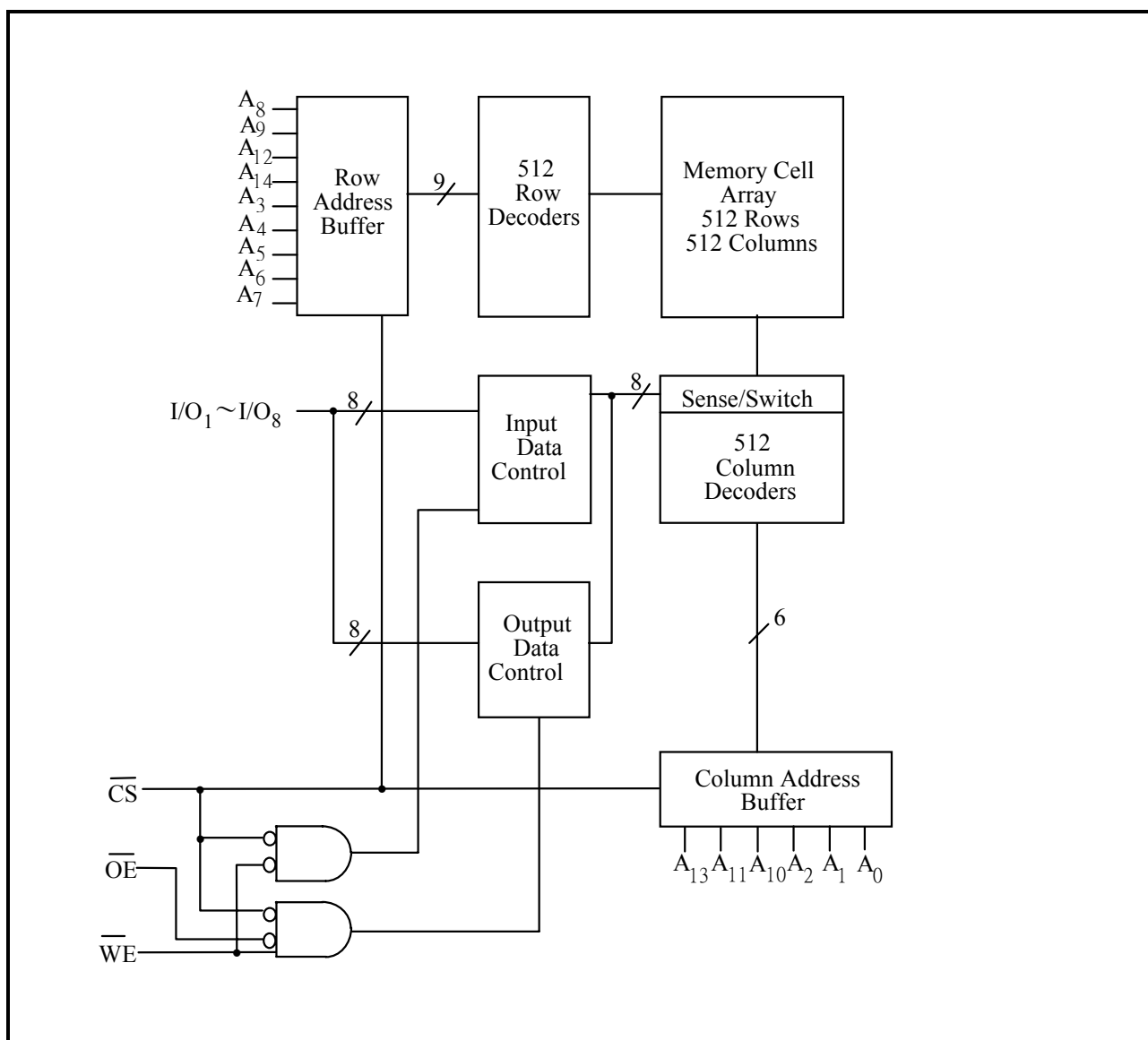
Pin Configuration: 28-Pin 300 mil SOJ



Symbols	Functions
A <sub>0</sub> ~ A <sub>14</sub>	Address Inputs
I/O <sub>1</sub> ~ I/O <sub>8</sub>	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V <sub>DD</sub>	Power Supply
V <sub>SS</sub>	Ground



## Block Diagram:



## Truth Table:

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O <sub>1</sub> ~I/O <sub>8</sub>	V <sub>DD</sub> Current
H	X	X	Not Selected	High Z	I <sub>SB</sub> , I <sub>SB1</sub>
L	H	H	Output Disable	High Z	I <sub>DD</sub>
L	L	H	Read	Data Out	I <sub>DD</sub>
L	X	L	Write	Data In	I <sub>DD</sub>



## DC Characteristics:

## Absolute Maximum Ratings

Parameters	Rating	Unit
Supply Voltage to V <sub>SS</sub>	-0.5 to +4.6	V
Input/Output to V <sub>SS</sub>	-0.5 to V <sub>DD</sub> +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

## Operating Characteristics:

(V<sub>DD</sub> = 2.7V ± 5%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameters	Symbols	Test Conditions	Min.	Typ.	Max.	Unit	
Input Low Voltage	V <sub>IL</sub>	-	-0.3	-	+0.8	V	
Input High Voltage	V <sub>IH</sub>	-	+1.7	-	V <sub>DD</sub> +0.3	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>	-5	-	+5	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>DD</sub> , $\overline{CS}$ = V <sub>IH</sub> or $\overline{OE}$ = V <sub>IH</sub> or $\overline{WE}$ = V <sub>IL</sub>	-5	-	+5	μA	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = +8.0mA	-	-	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	1.8	-	-	V	
Operating Power Supply Current	I <sub>DD</sub>	$\overline{CS}$ = V <sub>IL</sub> , I/O = 0 mA	6.5	-	-	100	mA
		Cycle = MIN	7	-	-	90	mA
		Duty = 100%	8	-	-	80	mA
Standby Power Supply Current	I <sub>SB</sub>	$\overline{CS}$ = V <sub>IH</sub> , Cycle = MIN Duty = 100%	-	-	10	mA	
	I <sub>SB1</sub>	$\overline{CS} \geq V_{DD} - 0.2V$	-	-	1.0	mA	

Note: Typical characteristics are measured at V<sub>DD</sub> = 2.7V, T<sub>a</sub> = 25°C



## AC Characteristics:

## Capacitances

(V<sub>DD</sub> = 2.7V, T<sub>a</sub> = 25°C, f = 1 MHz)

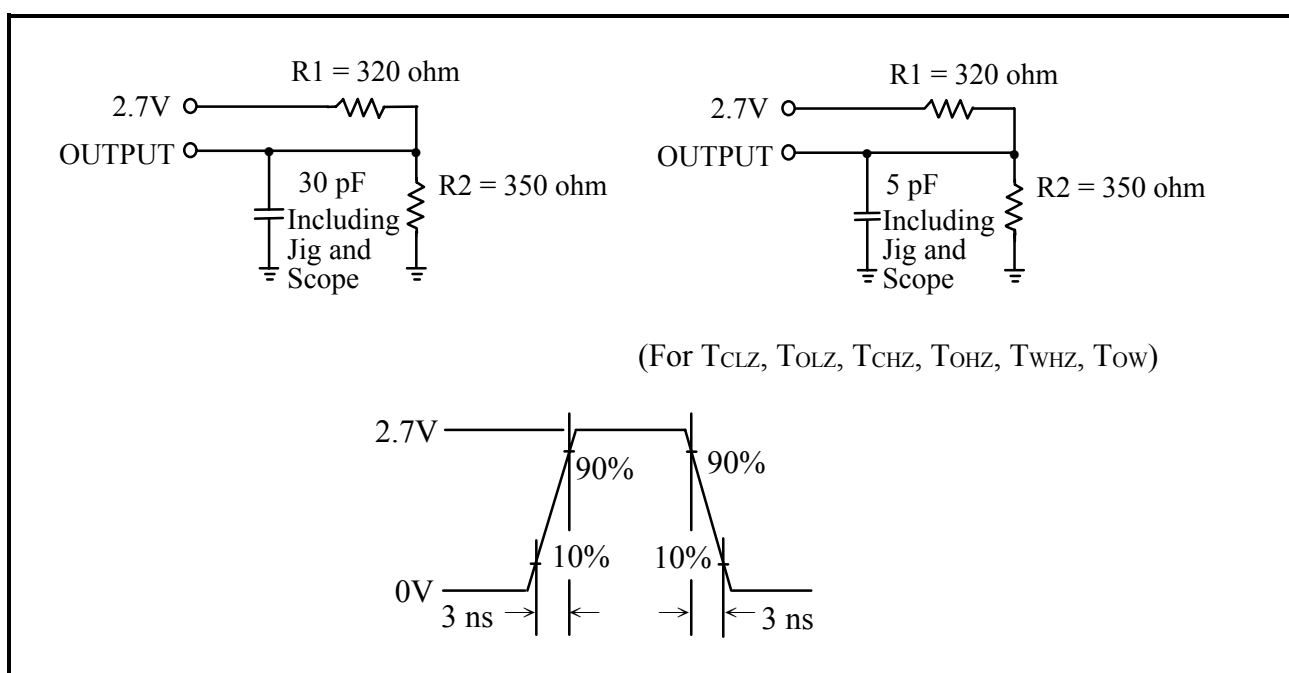
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>OUT</sub> = 0V	8	pF

Note: These parameters are sampled but not 100% tested.

## AC Test Conditions

Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	C <sub>L</sub> = 30 pF, I <sub>OH</sub> /I <sub>OL</sub> = -4 mA/8 mA

## AC Test Loads and Waveforms





## AC Performances:

( $V_{DD} = 2.7V \pm 5\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0$  to  $70^\circ C$ )

## (1) Read Cycle

Parameters	Symbols	SB61L256C-6.5		SB61L256C-7		SB61L256C-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T <sub>RC</sub>	6.5	-	7	-	8	-	ns
Address Access Time	T <sub>A</sub> A	-	6	-	7	-	8	ns
Chip Select Access Time	T <sub>A</sub> C <sub>S</sub>	-	6	-	7	-	8	ns
Output Enable to Output Valid	T <sub>A</sub> O <sub>E</sub>	-	4	-	4.5	-	5	ns
Chip Selection to Output in Low Z	T <sub>C</sub> L <sub>Z</sub> *	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	T <sub>O</sub> L <sub>Z</sub> *	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	T <sub>C</sub> H <sub>Z</sub> *	-	3	-	3.5	-	4	ns
Output Disable to Output in High Z	T <sub>O</sub> H <sub>Z</sub> *	-	3	-	3.5	-	4	ns
Output Hold from Address Change	T <sub>O</sub> H	3	-	3	-	3	-	ns

\*These parameters are sampled but not 100% tested

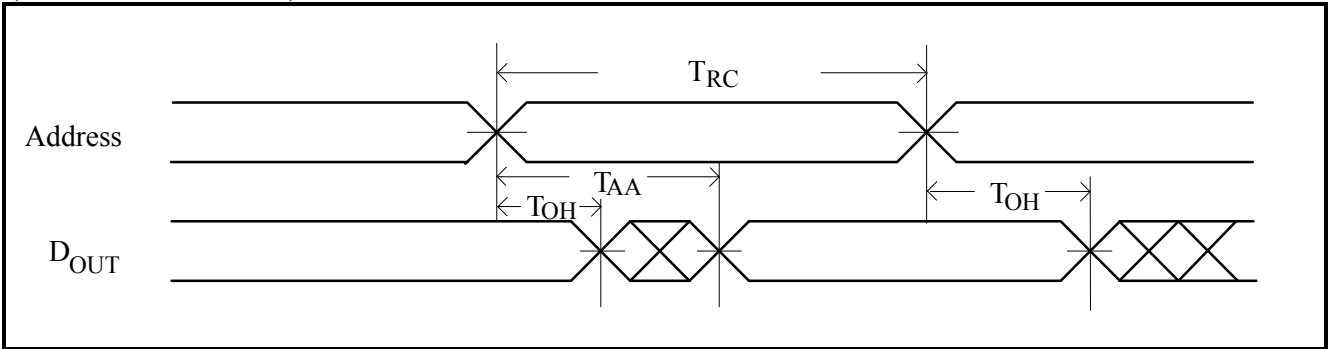
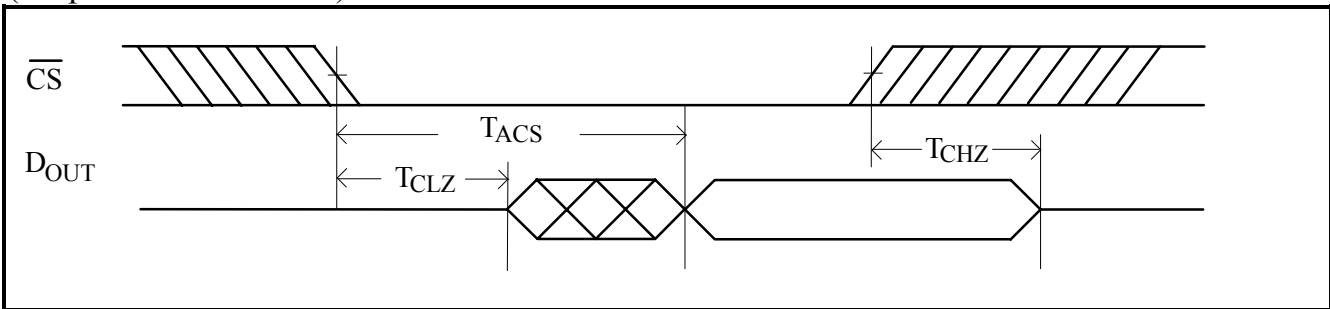
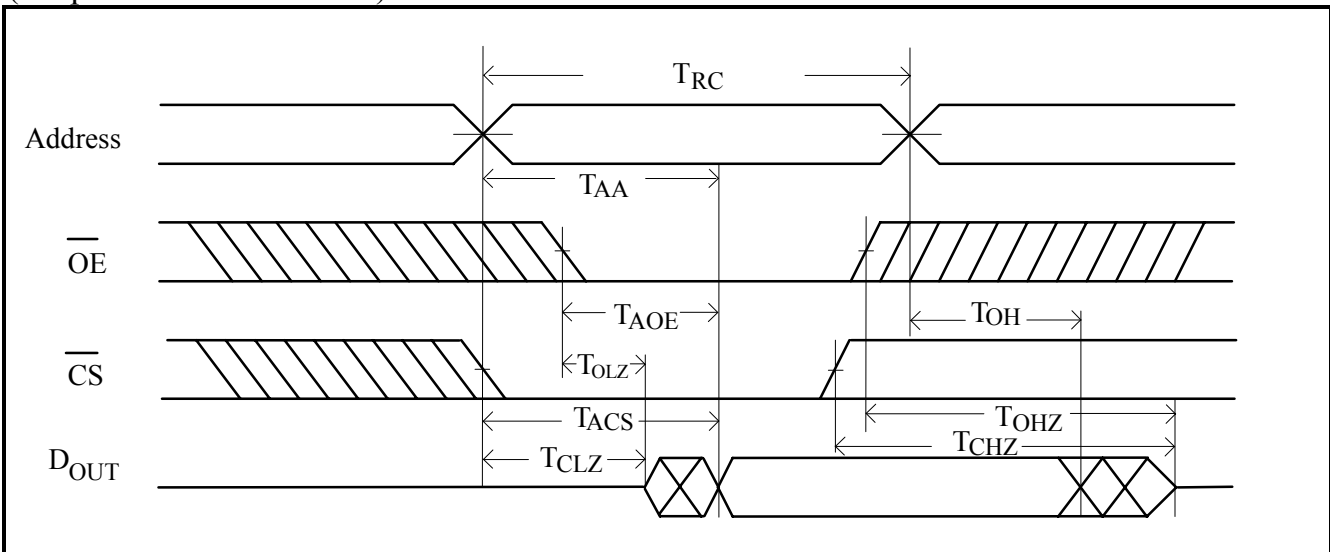
## (2) Write Cycle

Parameters	Symbols	SB61L256C-6.5		SB61L256C-7		SB61L256C-8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T <sub>W</sub> C	6.5	-	7	-	8	-	ns
Chip Selection to End of Write	T <sub>C</sub> W	4	-	5	-	6	-	ns
Address Valid to End of Write	T <sub>A</sub> W	4	-	5	-	6	-	ns
Address Setup Time	T <sub>A</sub> S	0	-	0	-	0	-	ns
Write Pulse Width	T <sub>W</sub> P	4	-	5	-	6	-	ns
Write Recovery Time	T <sub>W</sub> R	0	-	0	-	0	-	ns
Data Valid to End of Write	T <sub>D</sub> W	4	-	4.5	-	5	-	ns
Data Hold from End of Write	T <sub>D</sub> H	0	-	0	-	0	-	ns
Write to Output in High Z	T <sub>W</sub> H <sub>Z</sub> *	-	3	-	3.5	-	4	ns
Output Disable to Output in High Z	T <sub>O</sub> H <sub>Z</sub> *	-	3	-	3.5	-	4	ns
Output Active from End of Write	T <sub>O</sub> W	0	-	0	-	0	-	ns

\* These parameters are sampled but not 100% tested

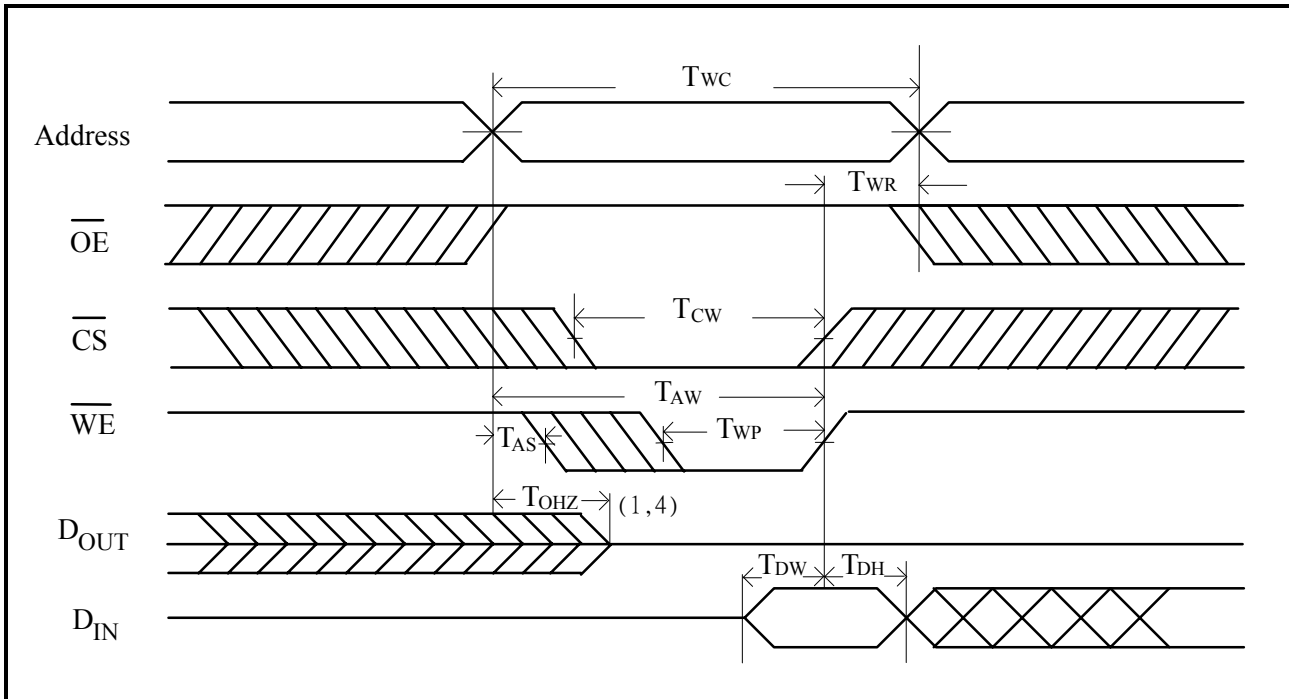


## Timing Waveforms

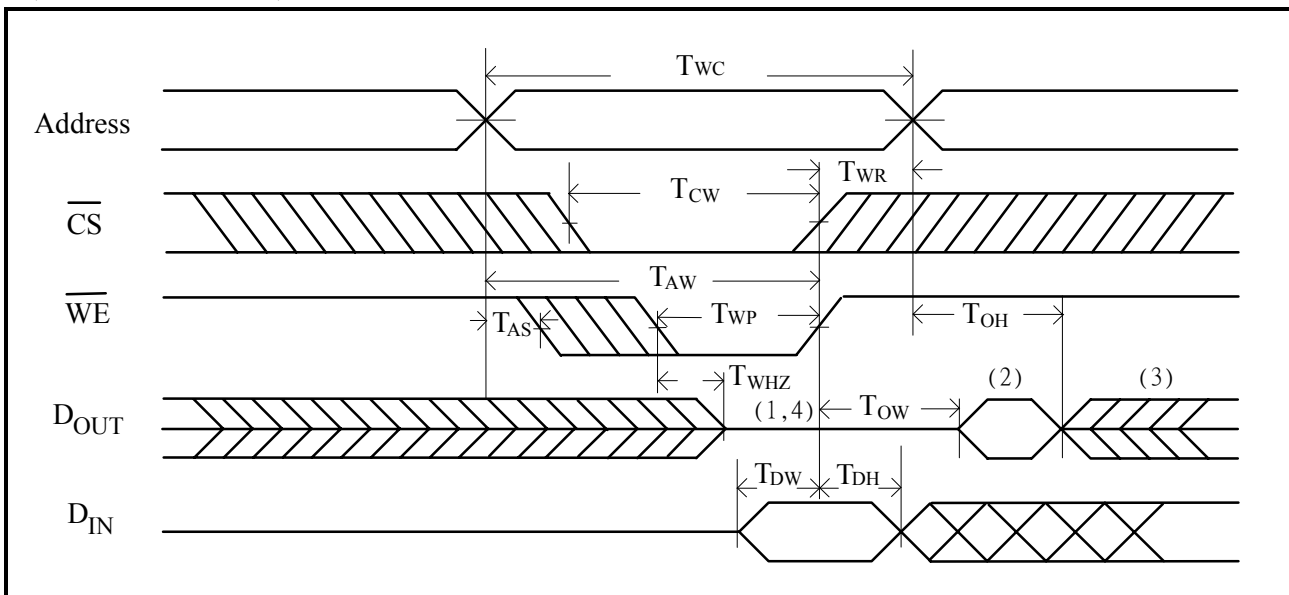
Read Cycle 1  
(Address Controlled)Read Cycle 2  
(Chip Select Controlled)Read Cycle 3  
(Output Enable Controlled)



### Write Cycle 1 ( $\overline{OE}$ Clock)



### Write Cycle 2 ( $\overline{OE} = V_{IL}$ Fixed)



#### Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from  $D_{OUT}$  are the same as the data written to  $D_{IN}$  during the write cycle.
3.  $D_{OUT}$  provides the read data for the next address.
4. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$ . This parameter is guaranteed but not 100% tested.





SB61L256B

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**Preliminary**