

4. Absolute Maximum Ratings (Ta=25°C)

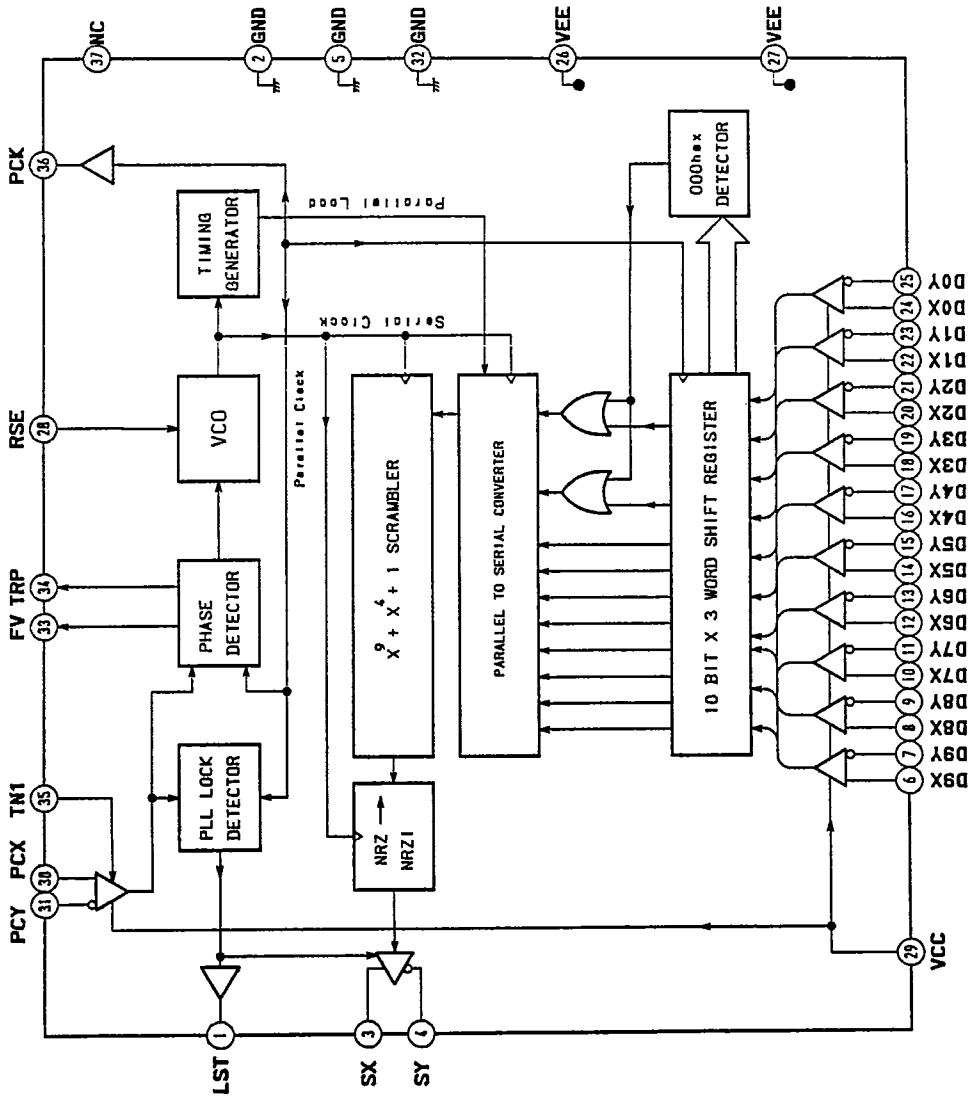
Item	Symbol	Ratings	Unit
Supply voltage	V _{EE}	-6	V
	V _{CC}	6	V
Input voltage	V _{IN}	V _{EE} to V _{CC}	V
Output current	I _{OUT}	-30	mA
Operating temperature	T _{OP}	0 to 65	°C
Storage temperature	T _{STG}	-50 to +125	°C
Allowable power dissipation	P _D	2.0	W

5. Recommended Operating Conditions

Item	Symbol	Ratings	Unit
Supply voltage	V _{EE}	-4.8 to -5.2	V
Supply voltage Note)	V _{CC}	4.8 to 5.2	V
Operating temperature	T _{OP}	0 to 65	°C

Note) Above conditions are for TTL input.
 Voltages are given with respect to the GND potential.

6. Block Diagram



Block diagram of SBX-1601A

7. Pin Description

Pin No.	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
1	LST		PLL lock detection. Turns to H during PLL lock. At unlock becomes irregular. At free run (TN1 H) turns to L.	O				
			H L	-1.0		-4.0	V V	
36	PCK		Clock output frequency divided to 1/10 VCO output. Utilized to check VCO free run frequency.	O				
			H L		-0.8 -1.6		V V	
3	SX		Input parallel data is converted to serial. Moreover, scramble, NRZ to NRZI converted data is differentially output.	H L				
4	SY					-1.6 -2.4	V V	

Pin No.	Symbol	Equivalent circuit	Description	I/O	Standard				
					Min.	Typ.	Max.	Unit	
29	Vcc		<p>Power supply for clock and parallel data input buffers:</p> <p>Give +5V for TTL input or -5V for ECL input.</p>	—					
6	D9X		<p>Parallel input ports:</p> <p>D9 is MSB D0 is LSB X is for signal. Y is for return.</p> <p>For TTL input (Vcc=+5V)</p> <p>For ECL input (Vcc=0V)</p>	I					
7	D9Y								
8	D8X								
9	D8Y								
10	D7X								
11	D7Y								
12	D6X								
13	D6Y								
14	D5X								
15	D5Y					2.0		0.8	V V
16	D4X								
17	D4Y								
18	D3X								
19	D3Y								
20	D2X								
21	D2Y								
22	D1X								
23	D1Y								
24	D0X								
25	D0Y								

Pin No.	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
28	RSE		Selection of VCO oscillation range: H: High range 140 to 270MHz L: Low range 100 to 145MHz	O	-0.4		-4.0	V
30	PCK		Parallel clock input (PCX) and its return (PCY): For ECL input (Vcc=0V) For TTL input (Vcc=+5V)	I	-1.0		-1.6	V
31	PCY					2.0		0.8
2 5 32	GND		GND	—				
26	VEE		-5V power supply for I/O buffers PLL	—	-5.2	-5.0	-4.8	V
27	VEE		-5V power supply for Logic block	—	-5.2	-5.0	-4.8	V

Pin No.	Symbol	Equivalent circuit	Description	I/O	Standard				
					Min.	Typ.	Max.	Unit	
33	FV		Adjustment of VCO free run frequency: The closer this pin is to V _{EE} , the lower the frequency. To adjust, TN1 pin shall be connected to GND.	I		-3.9		V	
34	TRP		Phase comparator out/VCO input: Connect to a trap in order to attenuate jitter.	O		-3.2		V	
35	TN1		Test node: At H: Input disabled (VCO free run condition). At L: Input through.	I		-1.0		V	
								-4.5	V

SONY

8. Electrical Characteristics

8-1. DC Characteristics

(V_{EE}=-5V, T_a=25°C)

Item	Symbol	Test conditions	Test circuit Fig.	Min.	Typ.	Max.	Unit
Supply current 1	I _{EE}	V _{EE} =-5V	Fig. 8-4		140		mA
Supply current 2	I _{CC}	V _{CC} =+5V				7	mA
Input voltage	V _{IH}	V _{CC} =GND		-1.0			V
	V _{IL}	Pin used PCX, PCY, DnX, DnY				-1.6	V
	V _{IH}	V _{CC} =+5V		2.0			V
	V _{IL}	Pin used PCX, PCY, DnX, DnY				0.8	V
Input current	I _{IH}	Pin used PCX, PCY, DnX, DnY	Fig. 8-5			+5.0	μA
	I _{IL}			-1.0		+1.0	μA
Input voltage	V _{IH}	Pin used RSE	Fig. 8-9	-0.4			V
	V _{IL}					-4.0	V
	V _{IH}	Pin used TN1	Fig. 8-8	-1.0			V
	V _{IL}					-4.5	V
Output voltage	V _{OH}	Pin used PCK R _P =1kΩ			-0.8		V
	V _{OL}				-1.6		V
	V _{OH}	Pin used LST I _{OH} =-10μA, I _{OL} =+10μA	Fig. 8-7	-1.0			V
	V _{OL}					-4.0	V
	V _{OH}	Pin used SX, SY R _P =220Ω			-1.6		V
	V _O				-2.4		V

8-2. AC Characteristics

PLL

Item	Symbol	Test conditions	Test circuit Fig.	Min.	Typ.	Max.	Unit
VCO Max. oscillation frequency 1	f _{MAX1}	RSE= "H"	Fig. 8-6	30.0			MHz
	f _{MIN1}					14.0	MHz
VCO Max. oscillation frequency 2	f _{MAX2}	RSE= "L"		15.0			MHz
	f _{MIN2}					10.0	MHz
PLL pull in range	f _{HP1}	f signal=270MHz RSE= "H"	Fig. 8-3	27.7			MHz
	f _{LP1}					25.5	MHz
	f _{HP2}	f signal=177MHz RSE= "H"		18.8			MHz
	f _{LP2}					16.5	MHz
	f _{HP3}	f signal=143MHz RSE= "L"		15.0			MHz
	f _{LP3}					13.0	MHz
Jitter	t _{jit}	f signal=270MHz RSE= "H"	Fig. 8-10			±0.25	nsec

Tested through PCK (Pin 36): 1/10 of serial clock.

Switching Characteristics

($V_{EE} = -5V, T_a = 25^\circ C$)

Item	Symbol	Test conditions	Test circuit Fig.	Min.	Typ.	Max.	Unit
rise time	t_r	Pins used PCK $R_P = 1k\Omega$			0.8		nsec
fall time	t_f				1.4		nsec
rise time	t_r	Pins used SX, SY $R_P = 220\Omega$			0.7		nsec
fall time	t_f				0.7		nsec

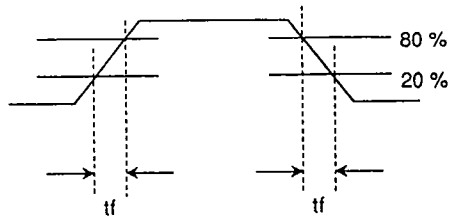


Fig. 8-1. Definition of t_r, t_f

Timing Relation of Input Clock and Data

($V_{EE} = -5V, T_a = 25^\circ C$)

Item	Symbol	Test conditions	Test circuit Fig.	Min.	Typ.	Max.	Unit
Pulse width	t_w	Pins used PCX, PCY	Fig. 8-3	$t_c/2$ -5		$t_c/2$ +5	nsec
Delay time	t_d	PCX-Dn		+5		+5	nsec

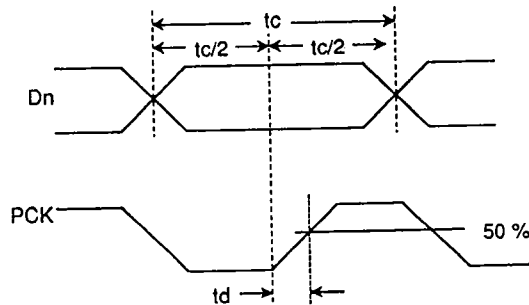


Fig. 8-2. Definition of t_d, t_w

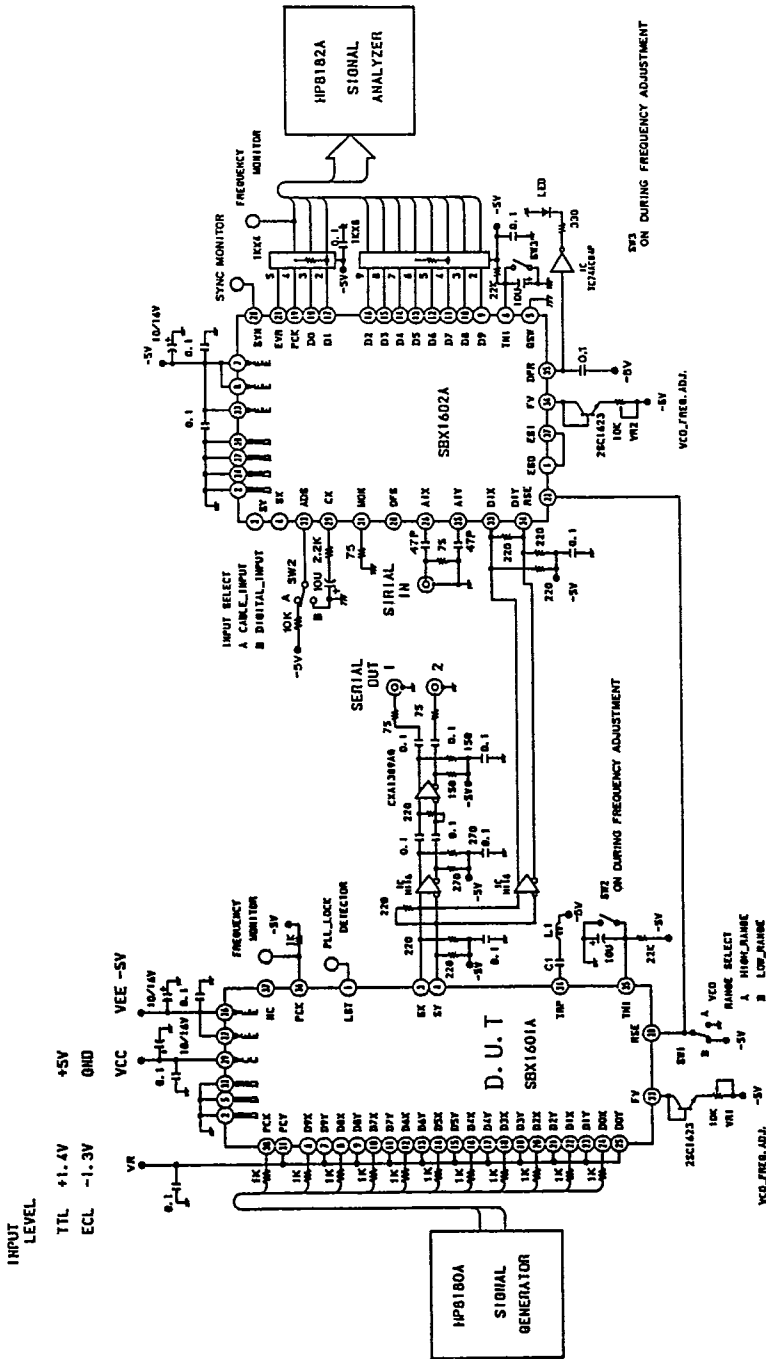


Fig. 8-3. Test circuit diagram

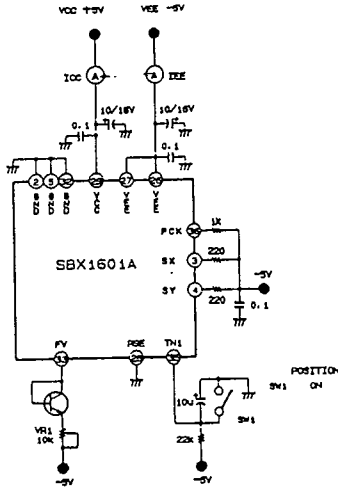


Fig. 8-4.

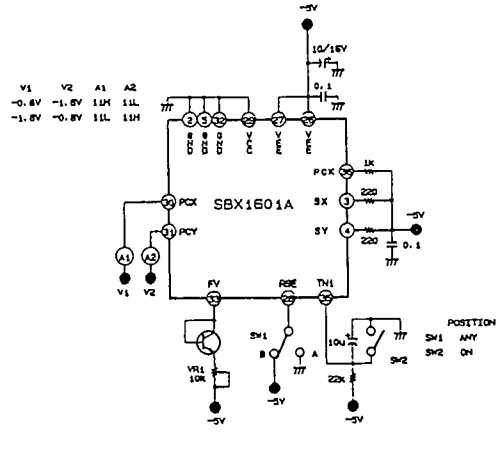


Fig. 8-5.

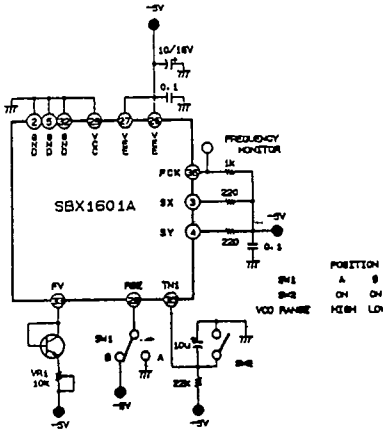


Fig. 8-6.

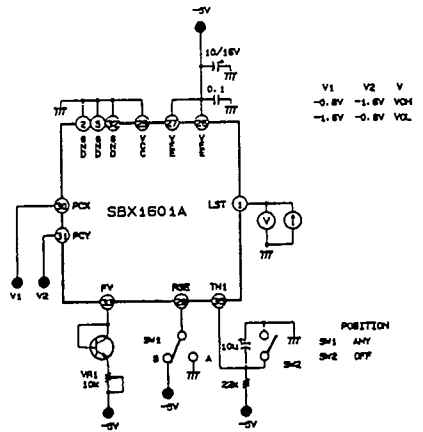


Fig. 8-7.

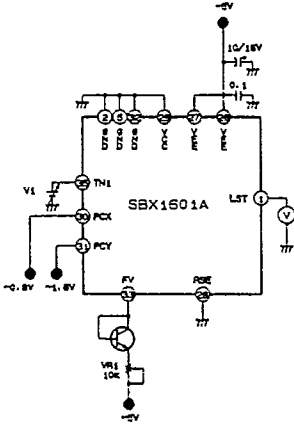


Fig. 8-8.

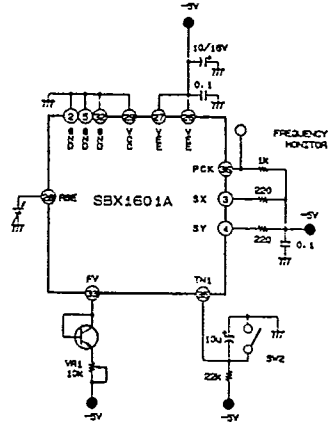


Fig. 8-9.

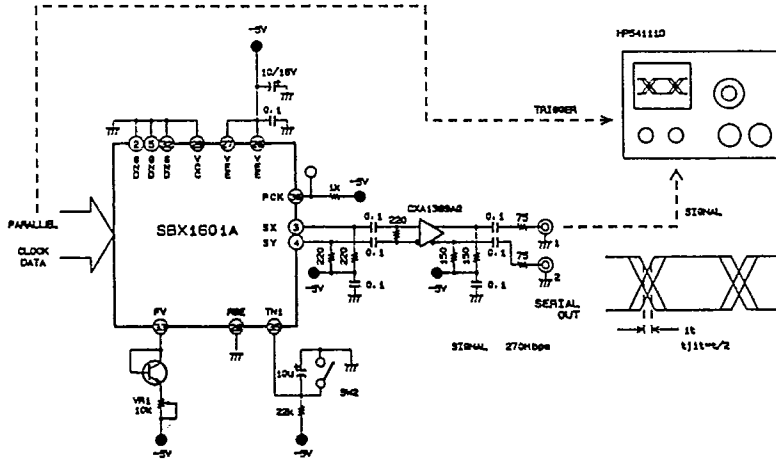


Fig. 8-10.

9. Description of Operation

SBX1601A internally generates a clock which is 10 times higher in frequency as that of parallel and locked to the input parallel clock in terms of a built-in PLL and converts input parallel data into serial data.

To facilitate clock extraction at the receiving end, serial data is being scrambled. To eliminate data polarity it is then converted to NRZI and output in differential form.

There is also a PLL lock detection circuit which enables the serial output circuit only when it is locked.

9-1 Phase Relation between Input Parallel Clock and Data

The phase relation between the parallel clock and data is shown in Fig. 9-1. Both clock and data are differentially input.

Parallel clock and data are input so that the rising edge of PCX be at the center of the data. A clock of almost the same phase as PCX is generated inside the IC to latch data inside the IC.

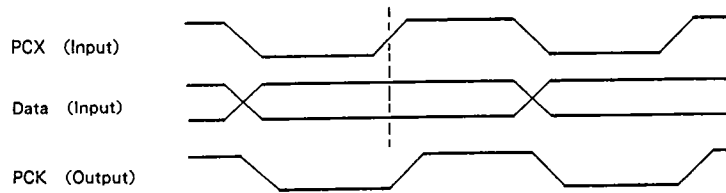


Fig. 9-1. Phase relation between clock and data

9-2. Input Circuit Requirements

Parallel clock and data can be given either by ECL or TTL logic. With ECL input every X or Y input can be used directly as an input for an ECL line receiver. To use with TTL input, Vcc (Pin 29) shall be connected to +5V. A fixed bias of +1.4V* shall be applied to PCY and DnY (n=0 to 9). TTL signals and its parallel clock shall be provided through 1 K ohm resistors to each "X" input. Those 1k Ω resistors are effective to minimize the influence of the TTL input signals to the jitter characteristics of the serial output signal. For 8 bit data, maintain unused LSBs to logical "0" state.

(* The fixed bias value can be higher, for example 2.5V in case of CMOS input).

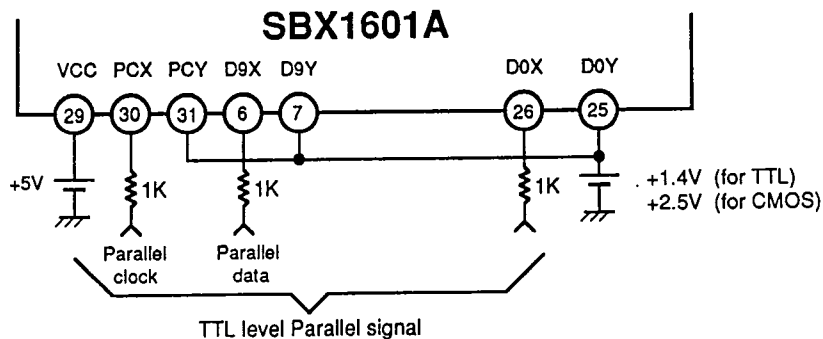


Fig. 9-2. Usage with TTL level input

9-3. Clock Generation

Fig. 9-3. shows a block diagram of PLL, PLL lock detection and the serial output control. When TN1 (pin 35) is set to "H" (connected to GND), the parallel clock input is disabled inside the IC. VCO turns to free run condition and adjustment of the free run frequency becomes possible through FV (pin 33).

Reducing the value of the resistance put between FV and V_{EE} lowers VCO oscillation frequency. Monitoring oscillation frequency is made through PCK (pin 36) which gives 1/10 frequency of VCO output. When PLL is locked, the phase of the PCK output coincides with that of the PCX input within a tolerance given. C-R time constant connected to TN1 serve to turn off the paralleled clock temporarily in order to avoid mislock problem. When supply voltage goes below $-4.3V$ approximately, the input parallel clock is automatically shut off to set VCO free run frequency.

The selection of VCO oscillation frequency range is made by RSE (pin 28): "H" stands at 140 to 270MHz and at "L", at 100 to 145MHz.

TRP (Pin 33) is the output of the phase comparator. To minimize jitter component, a trap circuit consisting of a series resonant circuit turned at the parallel clock frequency in use is necessary.

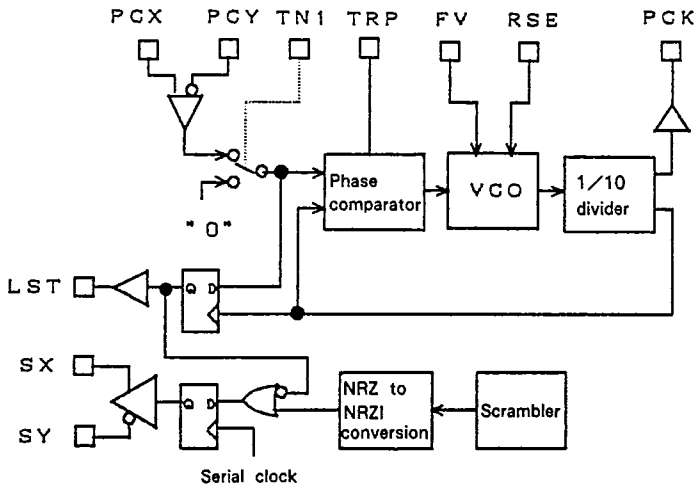


Fig. 9-3. PLL and serial output control block

9-4. PLL Lock Detection

LST signal is generated by latching the incoming parallel clock with the internal parallel clock which is 1/10 of the VCO frequency. LST serves as the PLL lock detection signal. The LST also controls serial output. If parallel clock input is disabled by means of TN1, LST turns to "L" and serial output turns to OFF condition (SX (3): "H", SY (4): "L") as described in the preceding section.

The involvement of LST in the control of serial output makes it possible to switch off the serial output signal at will by forcing the state of the input parallel clock to "L".

9-7. Scrambler

Fig. 9-6 (a) shows a basic scrambler block showing the modulo-2 division by $X^9 + X^4 + 1$. Fig. 9-6 (b) shows the actual form of the scrambler which is equivalent to (a) but fully pipelined.

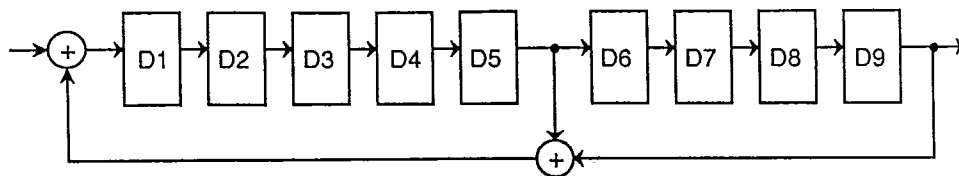


Fig. 9-6 (a). $X^9 + X^4 + 1$ scrambler

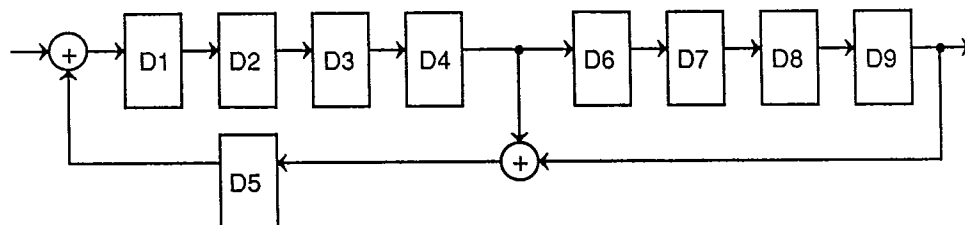


Fig. 9-6 (b). Actual $X^9 + X^4 + 1$ scrambler

9-8. NRZ to NRZI Conversion

To eliminate the signal polarity of scrambled data, conversion from NRZ to NRZI is employed.

Thanks to the nature of NRZI code, maintenance of the polarity of signal becomes unnecessary in design and manufacturing of equipment.

Further, if a differential output is used as two separate signal sources, their spurious radiation components tend to cancel out or lower to each other.

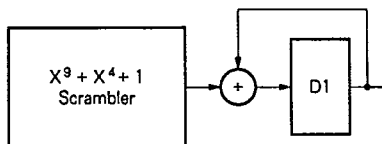


Fig. 9-7. NRZ to NRZI conversion

9-9. VCO Frequency Adjustment

VCO free-run frequency is adjusted generally at room temperature after the temperature of the IC reaches a steady state (5 to 10 minutes after power supply is ON). First, set VCO to free-run condition either by connecting TN1 node to ground or by maintaining parallel clock input (PCX) at logical "L" state. While monitoring PCK (Pin 36) output, adjust the frequency within $\pm 1\%$ of the desired parallel clock in terms of the variable resistor (VR1) shown in Fig. 9-8.

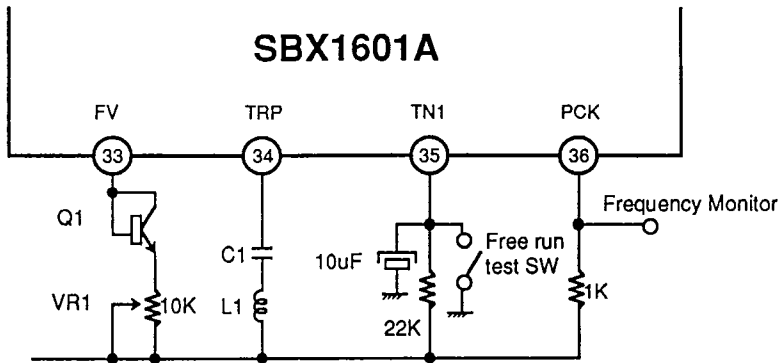


Fig. 9-8. VCO control area

9-10. Compensation on VCO Temperature Characteristics

A diode-connected transistor Q1 shown in Fig. 9-8. is effective to improve some residual frequency variation along the temperature change. Typical characteristics of the VCO are given in Fig. 9-9 (a) and 9-9 (b).

9-11. Jitter Trap

Since the internally generated serial clock is locked to the incoming parallel clock, there exists periodic jitter components which are generated from the phase comparison process of the PLL. A serial resonant circuit (trap) connected between TRP (Pin 34) and V_{EE} tuned at the parallel clock frequency reduces effectively the fundamental component of the jitter well below the specification ($\pm 0.25\text{nsec}$). Recommended values of C_1 and L_1 are given in Table 9-1.

Standard Component	D1	D2	
		PAL	NTSC
C ₁ (PF)	150	240	300
L ₁ (μH)	0.2	0.3	0.4

Table 9-1. Recommended values of the trap circuit

An important remark in a practical implementation is that TRP node is an input of a very sensitive voltage-frequency converter (VCO) which can be easily disturbed by any pick-up noise. Hence, the trap circuit should be carefully located and be kept as short as possible from the pin 34 in order to avoid a noise problem.

10. Recommended Circuit

Fig. 10-1 (a) and 10-1 (b) show recommended circuit for ECL input and that of TTL respectively.

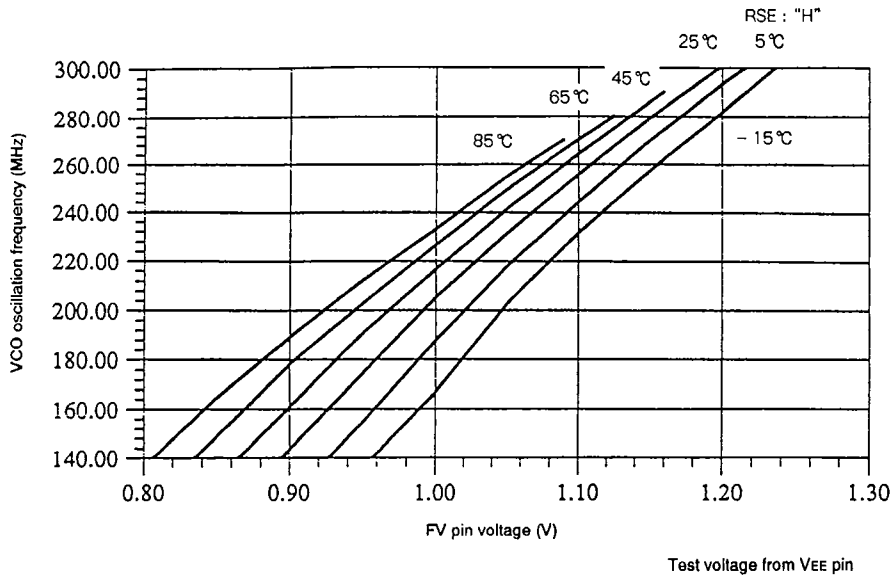


Fig. 9-9 (a). VCO oscillation frequency vs. FV pin voltage (High Rate)

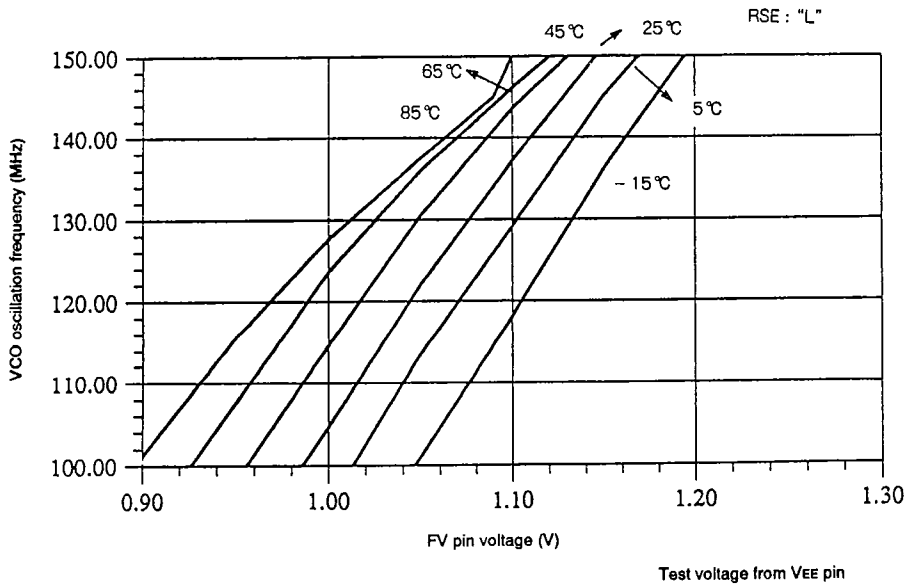
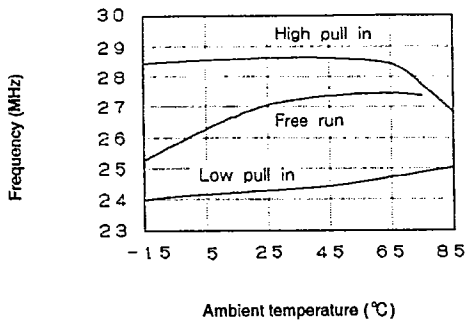
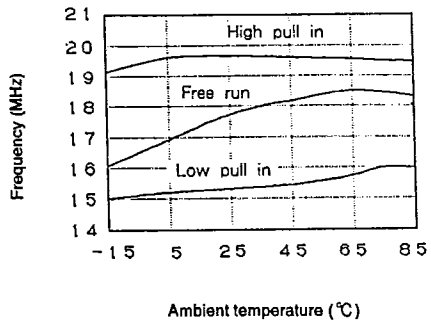


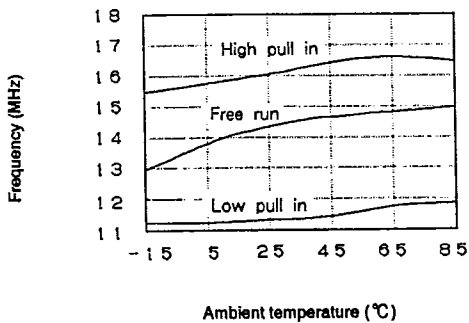
Fig. 9-9 (b). VCO oscillation frequency vs. FV pin voltage (Low Rate)



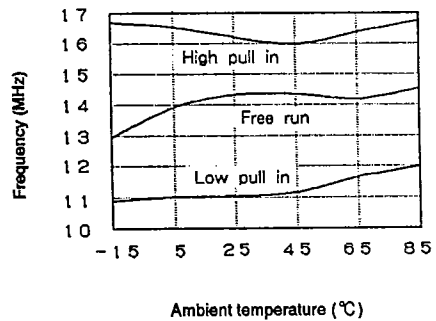
(a) at 270 Mb/sec (RSE="H")



(b) at 177 Mb/sec (RSE="H")



(c) at 143 Mb/sec (RSE="H")



(d) at 143 Mb/sec (RSE="L")

Fig. 9-10. Typical characteristics of pull-in range and free-run frequencies

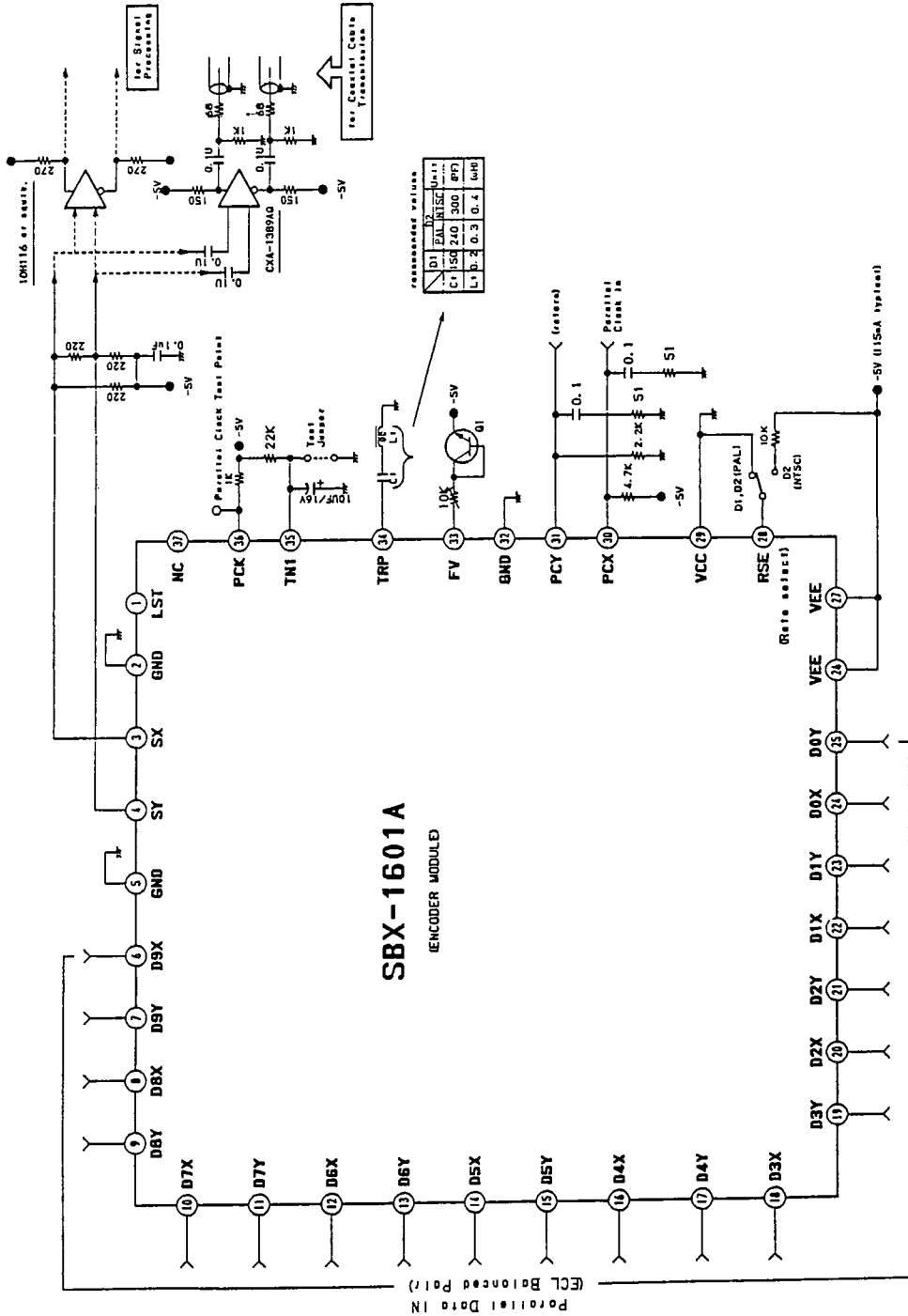


Fig. 10-1 (a). Recommended circuit for ECL input

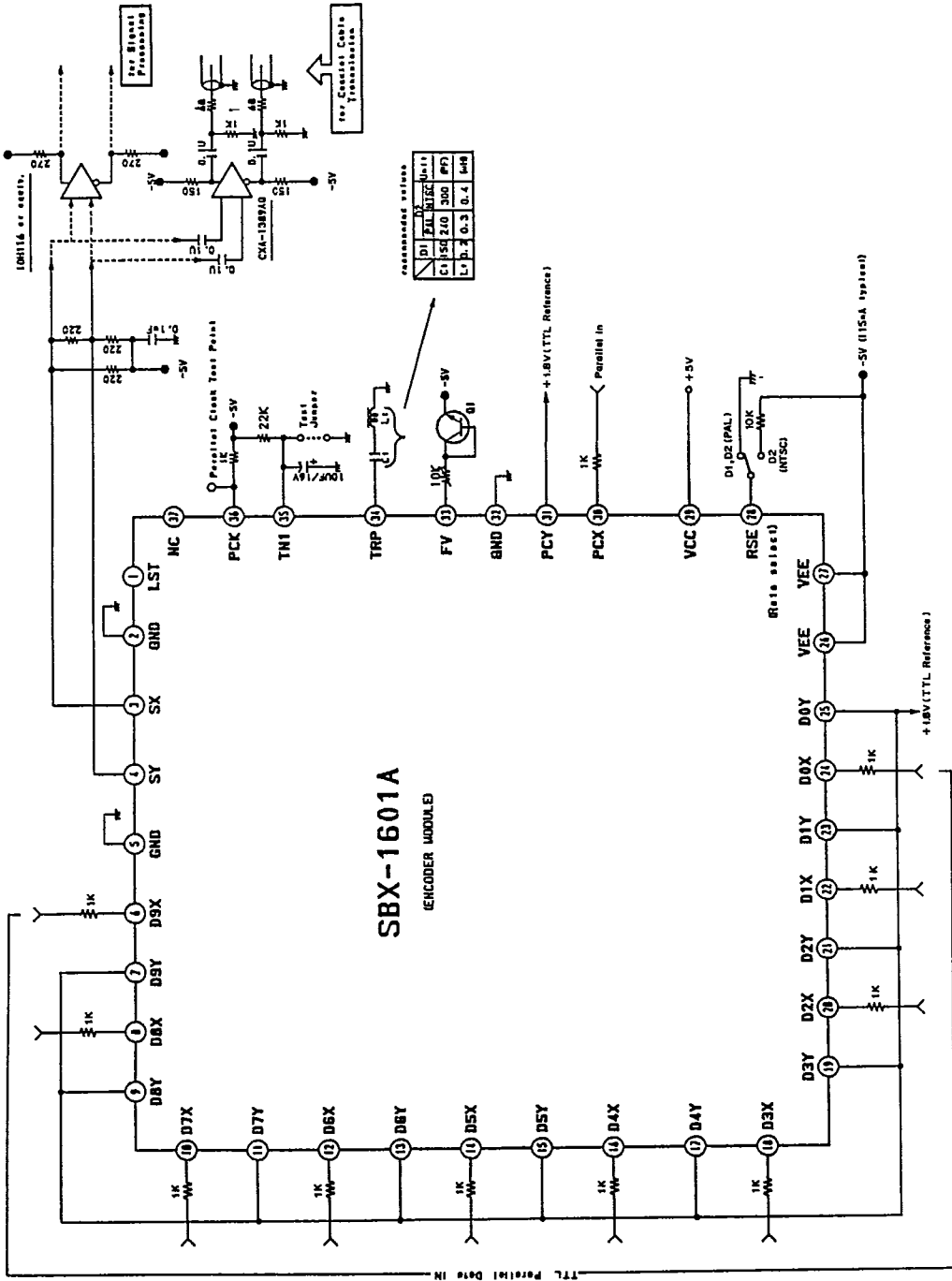


Fig. 10-1 (b). Recommended circuit for TTL input

11. Markings

Markings and their meanings are as shown below.

