SENSORY®

SC-604
Speech And Music Processor

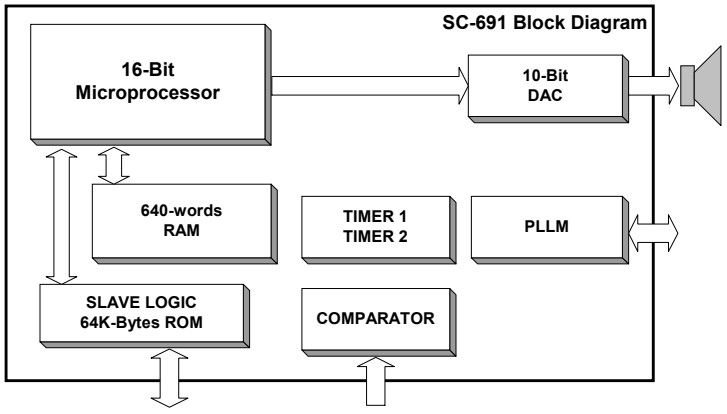
Data sheet

Features

- Advanced, Integrated Speech Synthesizer for High-Quality Sound
- Operates up to 12.32 MHz (Performs up to 12 MIPS)
- Slave Mode Enables Hours of Speech Using an External Processor and Memory
- Master Mode Allows 6.8 Minutes of Speech Onboard
- Supports High-Quality Synthesis Algorithms such as MX, CX, Simple CX, LX, ADPCM, and Polyphonic Music
- Simultaneous Speech Plus Music Capabilities
- Very Low-Power Operation, Ideal for Hand-Held Devices
- Low-Voltage Operation, Sustainable by Three (3) Batteries
- Reduced Power Standby Modes, Less Than 10 μA in Deep-Sleep Mode
- 16 General-Purpose I/O Pins (in Master Mode) or 4 General-Purpose I/O Pins (in Slave Mode)
- Resistor-Trimmed Oscillator or 32.768-kHz Crystal Reference Oscillator
- Slave Interface Logic Contains 64K Bytes-Words Onboard ROM (2K Words Reserved)
- 640-Word RAM
- Direct Speaker Drive, 32 Ω (PDM)
- One-Bit Comparator With Edge Detection Interrupt Service
- Serial Scan Port for In-Circuit Emulation, Monitor, and Test
- Available in Die Form or 64-Pin LQFP Package

Description

The SC-604 is a low-cost, mixed-signal processor that combines a speech synthesizer with a dedicated slave interface logic, general-purpose I/O, onboard ROM, and direct speaker-drive in a single package. The computational unit uses a powerful new DSP that gives the SC-604 unprecedented speed and computational flexibility compared with previous devices of its type. The SC-604 supports a variety of speech and audio coding algorithms, providing a range of options with respect to speech duration and sound quality.



The device consists of a micro-DSP core, embedded program and data memory, and a self-contained clock generation system. General-purpose periphery is comprised of 16 bits of partially configurable I/O.

The core processor is a general-purpose 16-bit microcontroller with DSP capability. The basic core block includes a computational unit (CU), data address unit, program address unit, two timers, eight-level interrupt processor, and several system and control registers. The core processor gives the SC-604break-point capability in emulation.

The processor is a Harvard type for efficient DSP algorithm execution, separating program and data memory blocks to permit simultaneous access. The ROM has a protection scheme to prevent third-party pirating. It is configured in 32K 17-bit words.

The total ROM space is divided into two areas:

1) The lower 2K words are reserved by Sensory, Inc. for a built-in self-test
2) The upper 30K is for user program and data space.

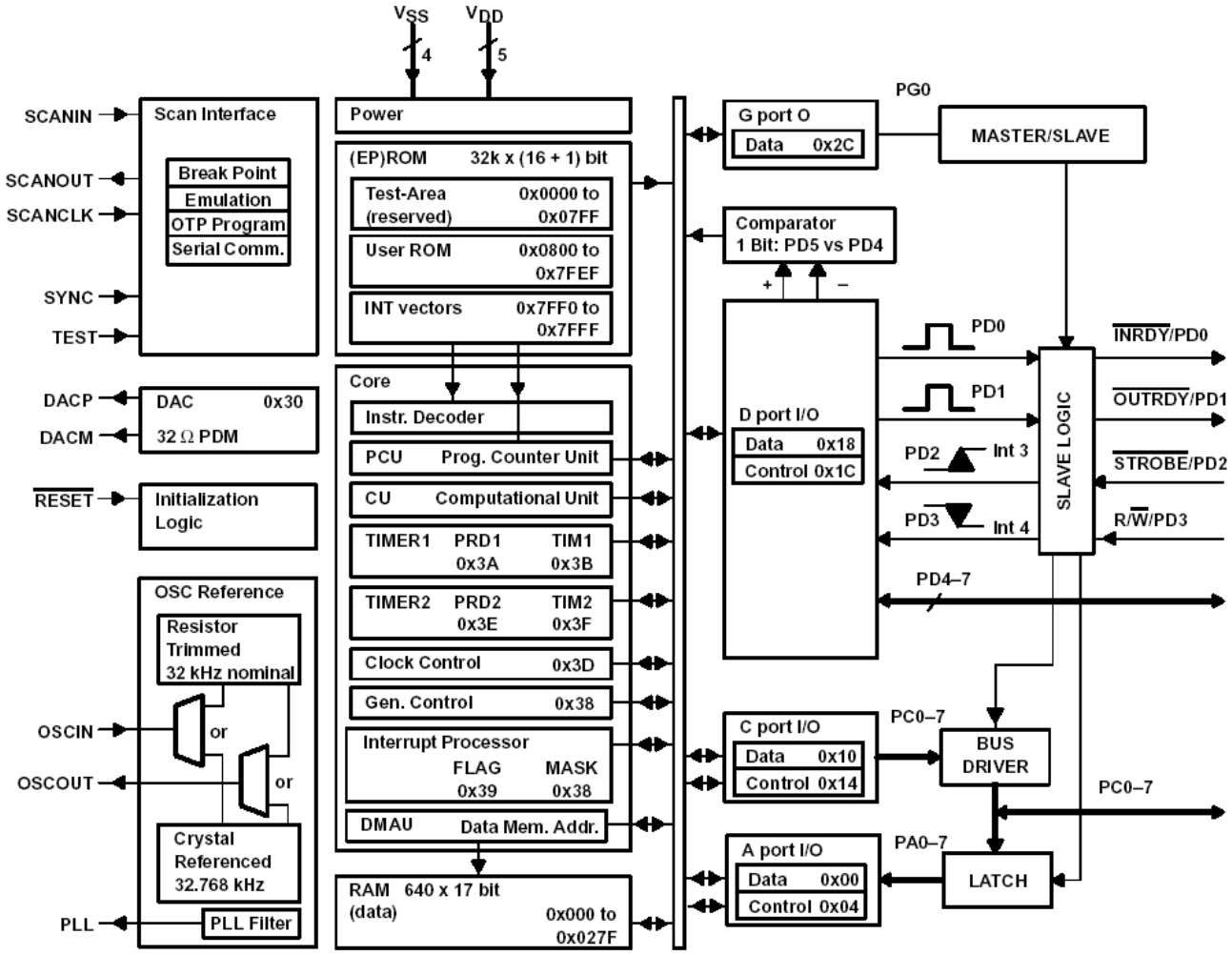
The data memory is internal static RAM. The RAM is configured in 640 17-bit words. All memories are designed to consume minimum power at a given system clock and algorithm acquisition frequency.

A flexible clock generation system enables the software to control the clock over a wide frequency range. The implementation uses a phase-locked loop (PLL) circuit that drives the processor clock at a selectable frequency between the minimum and maximum achievable. Selectable frequencies for the processor clock are spaced apart in 65.536-kHz steps. The PLL clock-reference is also selectable; either a resistor-trimmed oscillator or a crystal-referenced oscillator may be used. Internal and external clock sources are controlled separately to provide different levels of power management.

The periphery consists of two 8-bit-wide general-purpose I/O ports when operating in master mode, or four general-purpose I/O pins in slave mode. In the master mode, the bidirectional I/O can be configured under software control as either high-impedance inputs or as totem-pole output. They are controlled via addressable I/O registers. These features make the input port especially useful as a key-scan interface. Slave mode consists of four general-purpose I/O, four control pins, and eight bidirectional data pins.

A simple one-bit comparator is also included in the periphery. The comparator is enabled by a control register, and its access is shared with two pins in one general-purpose I/O port. Rounding out the SC-604 periphery is a built-in pulse-density-modulated DAC (digital-to-analog converter) with direct speaker-drive capability. The following block diagram gives an overview of the SC-604functionality.

Functional block diagram



Functional Description

The SC-604 is a member of the SC-6x family, which is based on the SC-614 core. For specific details about the core operations, instruction sets, register definitions, port configuration, etc., consult the SC-614 User's Guide (80-0212).

The SC-604 can be used as a slave synthesizer in slave mode or can operate stand-alone in master mode. The slave mode activates logic circuitry internal to the device that gives the device a dedicated slave interface. The slave or master mode is controlled by the bit 0 of the Port G (PG0). By default the device initially starts in slave mode. To change to master mode write a 0x01 to G port 0 (0x2C). To change back to slave mode write a 0x00 to port G bit 0 (0x2C).

Master Mode

In master mode, the slave logic circuitry is disabled and SC-604has 16 general-purpose I/Os. These 16 input/output pins are organized as 2-byte-wide ports (C and D), initialized as inputs. Each of the pins can be configured as a totem-pole output or as a high-impedance input by setting or clearing the appropriate bit in the appropriate control register (0x14, 0x1C). When configured as an output, the data driven by the output pin can be controlled by setting or clearing the appropriate bit in the appropriate data register (0x10, 0x18). Whether configured as input or as output, reading the data port reads the actual state of the pin.

External interrupts can be caused by transitions on pins PD2, PD3, PD4, and PD5 in the master mode. These interrupts are supported whether the pins are programmed as inputs or outputs.

Slave Mode

In slave mode, the slave logic circuitry is enabled allowing the device to have a dedicated slave interface. In this mode, only four pins of port D (PD4–PD7) are available as general-purpose I/O while the remaining pins (PD0–PD3) are redefined as INRDY, OUTRDY, STROBE and R/W. These pins are used to operate the slave interface. The SC-604controls the INRDY and OUTRDY pins to let the external microcontroller know when the slave is ready to accept or transmit data. The external microcontroller controls the R/W and STROBE pins of SC-604to sequence the read/write data flow. Each read or write sequence generates an interrupt that needs to be serviced by an interrupt service routine. These interrupt service routines need to be written by the code developer. The INT3 interrupt service routine indicates that the host has completed the write sequence, and the slave should read the data from port A. The INT4 interrupt service routine indicates the host has completed the read sequence. An interrupt is not generated when a read/write is done on port G bit 0 (PG0).

The slave interface consists of:

- 8-bit bidirectional data bus (PC0–PC7)
- 2 status outputs: INRDY/PD0, and OUTRDY/PD1
- 2 control inputs: STROBE/PD2, and R/W/PD3
- 4 general-purpose I/Os (PD4–PD7)

Port C is used as an 8-bit bidirectional data bus. When data is to be sent to the host, it needs to be written to port C data register (0x10). When data is read from the host, it needs to be read from port A data register (0x00). Port A pins are not physically brought outside the device but are internally connected with the pins of port C.

System Initialization Sequence In The Slave Mode

- Initialize the host processor first.
- The host must hold the slave RESET pin low until the slave STROBE pin can be held high by the host throughout the slave initialization process.

The INRDY and OUTRDY pins are set high by the slave on the rising edge of the slave RESET pin.

Slave Mode Software Initialization

- Write 0x00 to port A (0x00), port C (0x10), port D (0x18) data registers.
- Configure the port C (PC0–PC7), port D0, and port D1 as output ports. (Write 0xFF to port C (0x14) and 0x03 to port D (0x1C) control registers)

- Configure port A (PA0–PA7), PORT D2, and port D3 as input ports (default at reset). Write 0x00 to port A (0x04) and 0x03 to port D (0x1C) control registers.
- After the slave completes its initialization, the slave needs to inform the host that it is ready to read or write data.

Note: the default mode for the MSP50C604 is the slave mode. The MSP50C604 can be set to master mode by writing a 1 to port G bit 0. This is an internal bit that is not available on the MSP50C604 external pins.

Note: the initialization sequence given previously is a specific requirement for setting up the MSP50C604 in slave mode. For the basic initialization requirements of the device, please refer to the MSP50C614 user's guide (SPSU014).

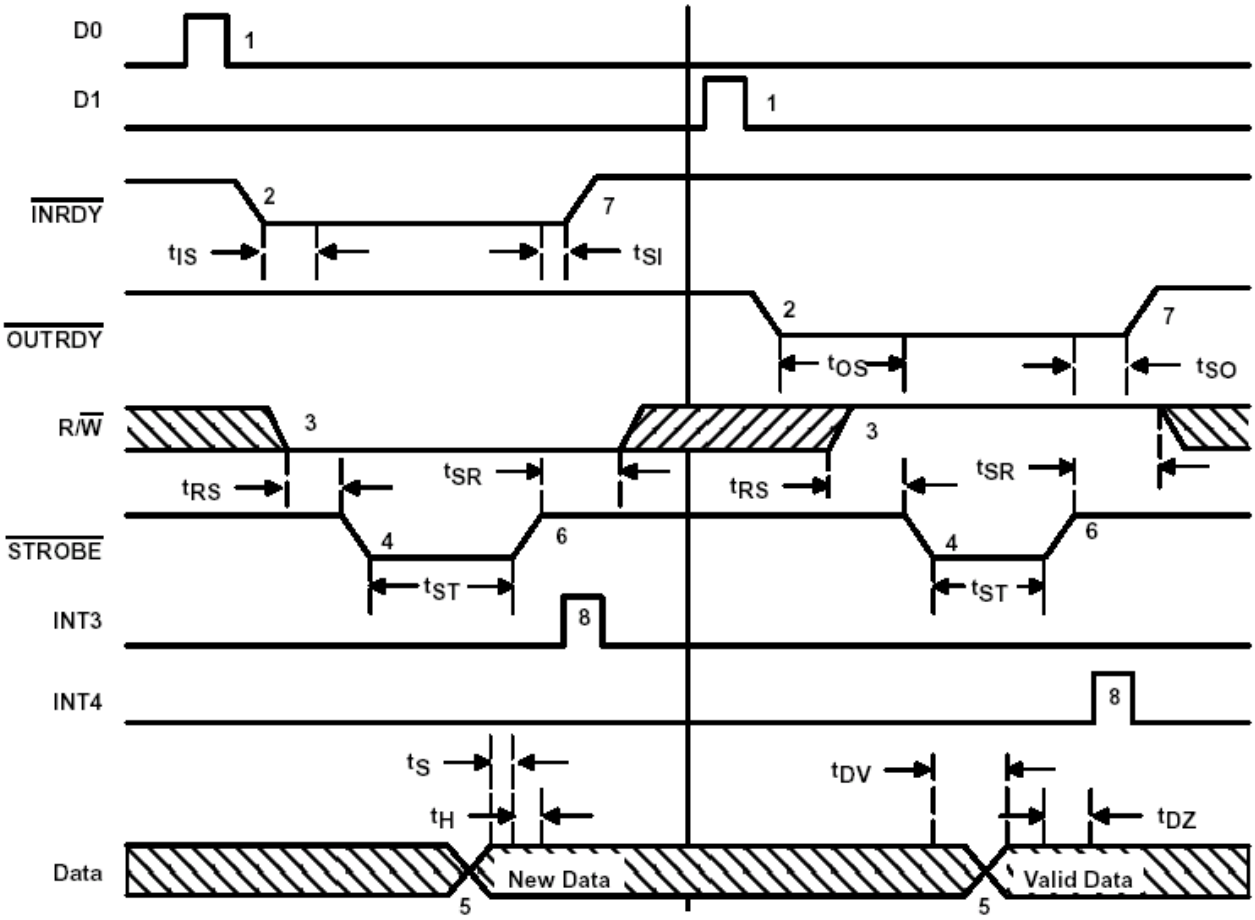
Write To Slave In The Slave Mode

- The slave indicates it is ready to receive data from the host by dropping INRDY low. This is done by writing low-high-low to port D (0x18) bit 0 (PD0).
- On the falling edge of the internal PD0 pulse, INRDY toggles low, notifying the host that the slave is ready to receive data.
- The host writes data to the slave by setting R/W low and then pulsing the STROBE high-low-high.
- The slave latches the data on the rising edge of the STROBE pulse and sets INRDY high.
- An INT3 interrupt is generated as INRDY goes high completing the write cycle.
- The latched data is read by the slave through port A (0x00) data register.

Read From Slave In The Slave Mode

- When the slave has data for the host, it places the data in port C (0x10).
- The slave then indicates that the data is ready by dropping OUTRDY low. This is done by writing low-high-low to port D (0x18) bit 1 (PD1).
- On the falling edge of the internal PD1 pulse, OUTRDY toggles low notifying the host that the slave is ready to send data.
- The host responds by setting R/W high and then pulsing STROBE high-low-high.
- The host should latch the data before raising STROBE high.
- This informs the slave that the data has been written to the host. The OUTRDY is pulled high by the slave at the rising edge of STROBE.
- An INT4 interrupt is generated as OUTRDY goes high completing the read cycle.

Timing Diagram

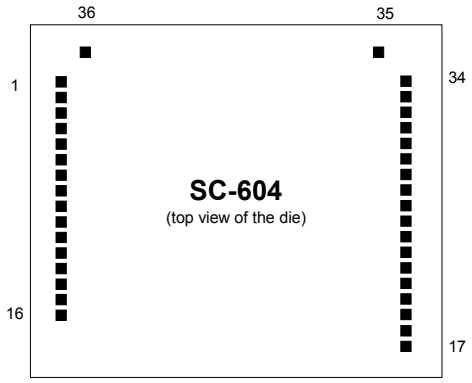


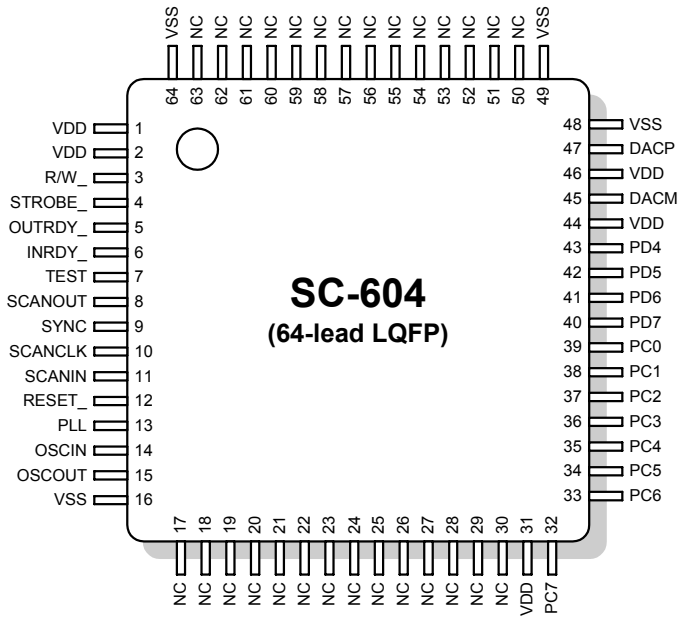
Write to Slave
1. Slave signals readiness to receive data from host.
2. Slave drops INRDY.
3. Host drops R/W to indicate a write.
4. Host drops STROBE.
5. Host places data on the bus.
6. Host raises STROBE indicating data is valid.
7. Slave raises INRDY, latching the data.
8. INT3 is triggered when INRDY rises.

Read from Slave
1. Slave signals readiness to send data to host.
2. Slave drops OUTRDY.
3. Host raises R/W to indicate a read.
4. Host drops STROBE.
5. Slave places data on the bus.
6. Host raises STROBE after reading the data.
7. Slave raises OUTRDY.
8. INT4 is triggered when OUTRDY rises.

Timing Constrains			
Write to Slave		**Read from Slave**	
INRDY low to STROBE low	$t_{IS\ (min)}$ = 5 ns	OUTRDY low to STROBE low	$t_{OS\ (min)}$ = 5 ns
R/W to STROBE low	$t_{RS\ (min)}$ = 75 ns	R/W to STROBE low	$t_{RS\ (min)}$ = 75 ns
STROBE low	$t_{ST\ (min)}$ = 100 ns	STROBE low	$t_{ST\ (min)}$ = 100 ns
STROBE high to R/W	$t_{SR\ (min)}$ = 25 ns	STROBE high to R/W	$t_{SR\ (min)}$ = 25 ns
STROBE high to INRDY high	$t_{SI\ (max)}$ = 75 ns	STROBE high to OUTRDY high	$t_{SO\ (max)}$ = 75 ns
Data setup	$t_{S\ (min)}$ = 15 ns	STROBE Low to data valid	$t_{DV\ (max)}$ = 90 ns
Data hold	$t_{H\ (min)}$ = 80 ns	STROBE High to data high Z	$t_{DZ\ (min)}$ = 90 ns

Pin/Pad Assignments





NAME	PIN NO.	PAD NO.	I/O	DESCRIPTION
PC0 – PC7	39 → 32	25 → 18	I/O	Port C general-purpose I/O (1 Byte)
PD4 – PD7	43 → 40	29 → 26	I/O	Port D general-purpose I/O (1 Byte)
PD0/INRDY	6	6	I/O	(Master) Port D general-purpose I/O
			O	(Slave) INRDY output to host
PD1/OUTRDY_	5	5	I/O	(Master) Port D general-purpose I/O
			O	(Slave) OUTRDY_ output to host
PD2/STROBE_	4	4	I/O	(Master) Port D general-purpose I/O
			O	(Slave) STROBE_ input from host
PD3/R/W_	3	3	I/O	(Master) Port D general-purpose I/O
			O	(Slave) Read/write input from host
Pins PD_4 and PD_5 may be dedicated to the comparator function, if the comparator enable bit is set.				
Scan Port Control Signals				
SCANIN	11	11	I	Scan port data input
SCANOUT	8	8	O	Scan port data output
SCANCLK	10	10	I	Scan port clock
SYNC	9	9	I	Scan port synchronization
TEST	7	7	I	Test modes
The scan port pins must be bonded out on any SC-604 production board.				
Reference Oscillator Signals				
OSCOUT	15	15	O	Resistor/crystal reference out
OSCIN	14	14	I	Resistor/crystal reference in
PLL	13	13	O	Phase-lock-loop filter
Digital-to-Analog Sound Output				
DACP	47	33	O	Digital-to-analog plus output (+)
DACM	45	31	O	Digital-to-analog minus output (–)
Initialization				
RESET_	12	12	I	Initialization
Power Signals				
V_{SS}	16, 48, 49†, 64	16, 34†, 35, 36	-	Ground
V_{DD}	1, 2, 31, 44, 46†	1, 2, 17, 30, 32†	-	Processor power (+)

† The V_{SS} and V_{DD} connections service the DAC circuitry. Their pins tend to sustain a higher current draw. A dedicated decoupling capacitor across these pins is therefore required.

Absolute Maximum Ratings

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	-0.3 to 7 V
Supply current, I_{DD} (see Note 2)	35 mA
Input voltage range, V_I (see Note 1)	-0.3 to V_{DD} + 0.3 V
Output voltage range, V_O (see Note 1)	-0.3 to V_{DD} + 0.3 V
Storage temperature range, T_A	-30°C to 125°C

***WARNING**:*
Stressing the SC-604 beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltages are measured with respect to V_{SS}.
2. The total supply current includes the current out of all the I/O pins as well as the operating current of the device.

Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage (with respect to V_{SS}), V_{DD}		3	5.2	V
CPU clock rate (as programmed), $f_{(CPU)}$		64	12,320	kHz
Load resistance between DAC_P and DAC_M, $R_{(DAC)}$		32		Ω
Operating free-air temperature, T_A	Device functionality	0	70	°C

Timing Requirements

		MIN	MAX	UNIT
$t_{(RESET)}$	Reset_ low pulse width, while V_{DD} is within specified limits	100		ns
$t1_{(WIDTH)}$	Pulse width required prior to a negative transition at pin PD3, PD5, or PF0 → PF7‡	2		$1/F_{CPU}$
$t2_{(WIDTH)}$	Pulse width required prior to a positive transition at pin PD2 or PD4†	2		$1/F_{CPU}$

‡ While these pins are being used as interrupt inputs.

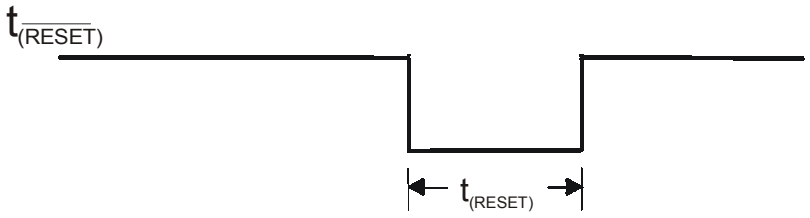


Figure 1: **Initialization Timing Diagram**

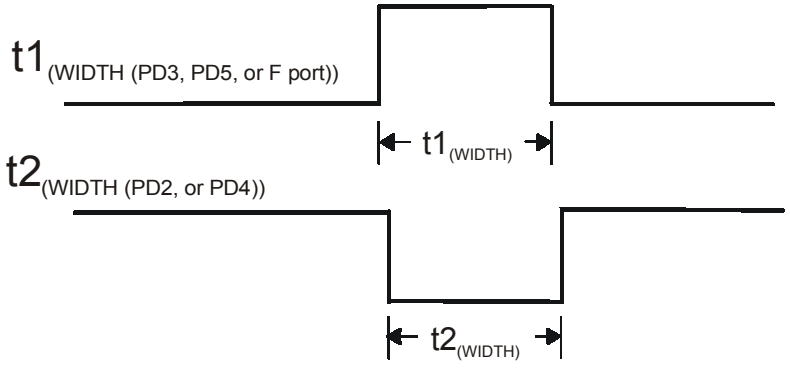


Figure 2: **External Interrupt Pin Pulse Width Requirements $t1_{WIDTH}$ and $t2_{WIDTH}$**

DC Electrical Characteristics, TA = 0 to 70°C

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
RESET_	Threshold changes	V_{DD} = 3 V	Positive going threshold		2.4		V
			Negative going threshold		1.8		
			Hysteresis		0.6		
		V_{DD} = 5.2 V	Positive going threshold		3.3		V
			Negative going threshold		2.9		
			Hysteresis		0.4		
V_{IH}	High-level input voltage	V_{DD} = 3 V		2		3	V
		V_{DD} = 4.5 V		3		4.5	
		V_{DD} = 5.2 V		3.5		5.2	
V_{IL}	Low-level input voltage	V_{DD} = 3 V		0		1	V
		V_{DD} = 4.5 V		0		1.5	
		V_{DD} = 5.2 V		0		1.7	
I_{OH}¶	High-level output current per pin of I/O port	V_{DD} = 4.5 V	V_{OH} = 4 V			–2	mA
I_{OL}¶	Low-level output current per pin of I/O port		V_{OL} = 0.5 V			5	mA
$I_{OH\ (DAC)}$	High-level output DAC current		V_{OH} = 4 V			–10	mA
$I_{OL\ (DAC)}$	Low-level output DAC current		V_{OL} = 0.5 V			20	mA
I_{lkg}	Input leakage current	Excludes OSC_{IN}				1	µA
$I_{(STANDBY)}$	Standby current	RESET is low			0.05	10	µA
I_{DD}†	Operating current	V_{DD} = 4.5 V, F_{CLOCK} = 12.32 MHz			15		mA
$I_{(SLEEP\text{-}deep)}$	Supply current	V_{DD} = 4.5 V, DAC off, ARM set, OSC disabled			0.05	10	µA
$I_{(SLEEP\text{-}mid)}$		V_{DD} = 4.5 V, DAC off, ARM set, OSC enabled			40	60	
$I_{(SLEEP\text{-}light)}$		V_{DD} = 4.5 V, DAC off, ARM clear, OSC enabled			60	100	
V_{IO}	Input offset voltage	V_{DD} = 4.5 V, V_{ref} = 1 to 4.25 V			25	50	mV
$R_{(PULLUP)}$	F port pullup resistance	V_{DD} = 5 V		70	150		KΩ
$\Delta f_{(RTO\text{-}trim)}$	Trim deviation	R_{RTO} = 470 KΩ, V_{DD} = 4.5 V, T_A = 25°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±1%	±3%	
$\Delta f_{(RTO\text{-}volt)}$	Voltage deviation	R_{RTO} = 470 KΩ, V_{DD} = 3.5 to 5.2 V, T_A = 25°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡				±1.5%	
$\Delta f_{(RTO\text{-}temp)}$	Temperature deviation	R_{RTO} = 470 KΩ, V_{DD} = 4.5 V, T_A = 0 to 70°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±0.03		%/°C
$\Delta f_{(RTO\text{-}res)}$	Resistance deviation	V_{DD} = 4.5 V, T_A = 25°C, $R_{(OSC)}$ = 470 KΩ at ±1%, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±1%		

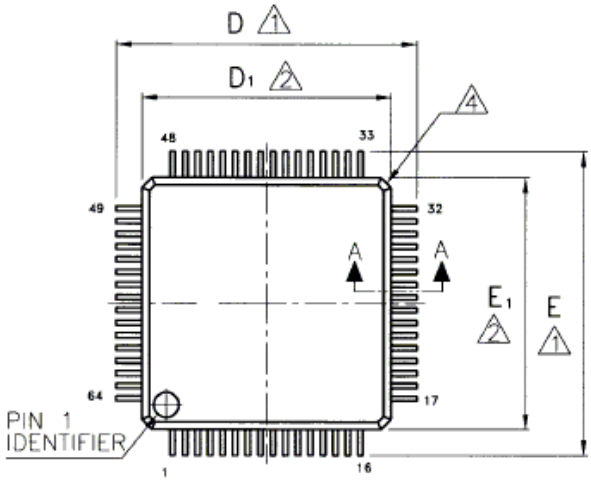
† Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.
‡ The best trim value is selected at nominal temperature and voltage but the deviation due to the trim error is ignored.
§ Typical voltage and current measurement taken at 25°C
¶ Cannot exceed 15 mA total per internal V_{DD} pin. Port A, B share 1 internal V_{DD} pin; Port C, D share 1 internal V_{DD}.

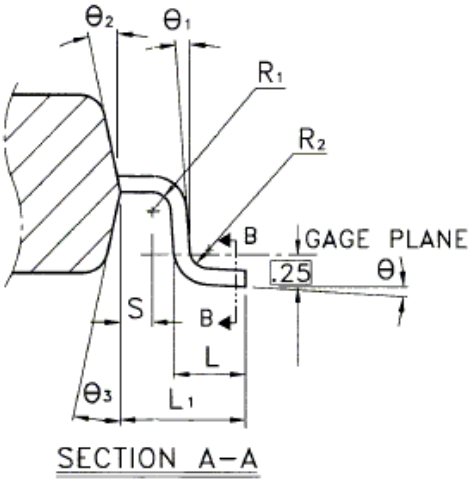
External Component Absolute Values

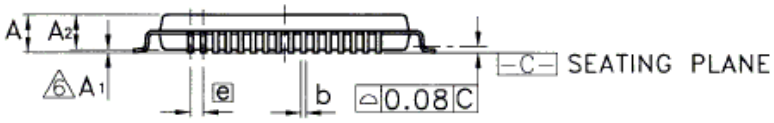
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{(RTO)}$	RTO external resistance	T_A = 25°C, 1% tolerance		470	KΩ
$C_{(PLL)}$	PLL external capacitance	T_A = 25°C, 10% tolerance		3300	pF

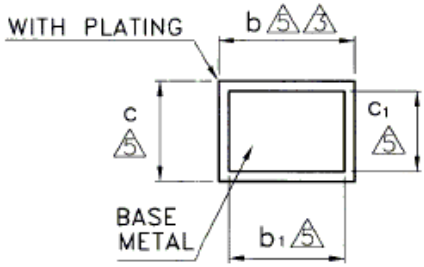
Mechanical Data

LQFP 64 PLASTICQUAD FLATPACK (10x10x1.4 mm)









Symbol Dimension in mm Dimension in inch	Min Nom Max Min Nom Max
A	- - 1.60 - - 0.063
A1	0.05 - 0.15 0.002 - 0.006
A2	1.35 1.40 1.45 0.053 0.055 0.057

Notes:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022

b
0.17
0.22
0.27
0.007
0.009
0.011

b1
0.17
0.20
0.23
0.007
0.008
0.009

c
0.09
-
0.20
0.004
-
0.008

c1
0.09
-
0.16
0.004
-
0.006

D
12.00 BSC
0.472 BSC

D1
10.00 BSC
0.394 BSC

E
12.00 BSC
0.472 BSC

E1
10.00 BSC
0.394 BSC

e
0.50 BSC
0.20 BSC

L
0.45
0.60
0.75
0.018
0.024
0.030

L1
1.00 REF
0.039 BSC

R1
0.08
-
-
0.003
-
-

R2
0.08
-
0.20
0.003
-
0.008

S
0.20
-
-
0.008
-
-

θ
0º
3.5º
7º
0º
3.5º
7º

θ**1**
0º
-
-
0º
-
-

θ**2**
12º TYP
12º TYP

θ**3**
12º TYP
12º TYP

Die Bond-out Coordinates

Die Size = **147.64 x 111.02 Mil**
Pad Size = **210 x 210 Mil**
Units = **Metric**

Pad	Pin	X-Axis Min	Y-Axis Min	X-Axis Max	Y- Axis Max
1	1	149.00	2122.80	235.00	2208.80
2	2	149.00	1961.45	235.00	2047.45
3	3	127.40	1805.45	213.40	1891.45
4	4	127.40	1651.45	213.40	1737.45
5	5	127.40	1497.45	213.40	1583.45
6	6	127.40	1343.45	213.40	1429.45
7	7	127.30	1191.05	213.30	1277.05
8	8	127.40	1077.95	213.40	1163.95
9	9	127.30	925.45	213.30	1011.45
10	10	127.30	814.15	213.30	900.15
11	11	127.30	702.85	213.30	788.85
12	12	127.45	555.50	213.45	641.50
13	13	127.30	435.50	213.30	521.50
14	14	127.30	324.20	213.30	410.20
15	15	127.30	212.90	213.30	298.90
16	16	148.00	108.10	234.00	194.10
17	31	3385.20	61.50	3471.20	147.50
18	32	3472.20	172.75	3558.20	258.75
19	33	3472.20	326.75	3558.20	412.75
20	34	3472.20	480.75	3558.20	566.75
21	35	3472.20	634.75	3558.20	720.75
22	36	3472.20	788.75	3558.20	874.75
23	37	3472.20	942.75	3558.20	1028.75
24	38	3472.20	1096.75	3558.20	1182.75
25	39	3472.20	1250.75	3558.20	1336.75
26	40	3472.20	1404.75	3558.20	1490.75
27	41	3472.20	1558.75	3558.20	1644.75
28	42	3472.20	1712.75	3558.20	1798.75
29	43	3472.20	1866.75	3558.20	1952.75
30	44	3450.60	2026.15	3536.60	2112.15
31	45	3517.01	2165.85	3603.01	2251.85
32	46	3517.01	2319.91	3603.01	2405.91
33	47	3517.01	2473.95	3603.01	2559.95
34	48	3516.80	2583.45	3602.80	2669.45
35	49	3149.35	2581.75	3235.35	2667.75
36	64	97.30	2533.65	183.30	2619.65

Ordering Information

Part	Ordering P/N	Shipping P/N	Description
SC-604 DIE	**SC604-R**	65-xxxx-x	Tested, Singulated SC-604 die in waffle pack.
SC-604 LQFP	**SC604-RL1**	65-xxxx-x	SC-604 64 pin 10x10x1.4mm LQFP

The Interactive Speech™ Product Line

The Interactive Speech line of ICs and software was developed to "bring life to products" through advanced speech recognition and audio technology.
The Interactive Speech Product Line was designed for consumer telephony products and cost-sensitive consumer electronic applications such as home electronics, personal security, and personal communication.
The product line includes award-winning RSC series general-purpose microcontrollers and tools, SC series of speech microcontrollers, plus a line of easy-to-implement chips that can be pin-configured or controlled by an external host microcontroller. Sensory's software technologies run on a variety of microcontrollers and DSPs.

RSC Microcontrollers and Tools

The RSC product line contains low-cost 8-bit speech-optimized microcontrollers designed for use in consumer electronics. All members of the RSC family are fully integrated and include A/D, pre-amplifier, D/A, ROM, and RAM circuitry. The RSC family can perform a full range of speech/audio functions including speech recognition, speaker verification, speech and music synthesis, and voice record/playback. The family is supported by a complete suite of evaluation tools and development kits.

SC Microcontrollers and Tools

The SC-6x product line feature the highest quality speech synthesis ICs at the lowest data rate in the industry. The line includes a 12.32 MIPS processor for high-quality low data-rate speech compression and MIDI music synthesis, with plenty of power left over for other processor and control functions. Members of the SC-6x line can store as much as 37 minutes of speech on chip and include as much as 64 I/O pins for external interfacing. Integrating this broad range of features onto a single chip enables developers to create products with high quality, long duration speech at very competitive price points.

Application Specific Standard Products (ASSPs)

Voice Direct™ 364 provides inexpensive speaker-dependent speech recognition and speech synthesis. This easy-to-use, pin-configurable chip requires no custom programming and can recognize up to 60 trained words in slave mode, and 15 words in stand-alone mode. Ideal for speaker-dependent command and control of household consumer products, Voice Direct* 364 is part of a complete product line that includes the IC, module, and Voice Direct 364 Speech Recognition Kit.

Voice Extreme™ simplifies the creation of fully custom speech-enabled products by offering developers the capability of programming the chip in a high-level C-like language. Program code, speech data, and even record and playback information can be stored on a single off-chip Flash memory. Based on Sensory's RSC-364 speech processor, Voice Extreme includes a highly efficient on-chip code interpreter, and is supported by a comprehensive suite of low-cost development tools.

Software and Technology

Voice Activation™ micro footprint software provides advanced speech technology on a variety of microcontroller and DSP platforms. A flexible design with a broad range of technologies allows manufacturers to easily integrate speech functionality into consumer electronic products.

Fluent Speech™ small footprint software recognizes up to 50,000 words; offers Animated Speech with the ability to automate enunciation and articulation; performs text-to-speech synthesis in either male or female voices; provides noise and echo cancellation, performs Wordspotting for natural language usage; offers telephone barge-in; and provides continuous digit recognition.

Important notices

Reasonable efforts have been made to verify the accuracy of information contained herein, however no guarantee can be made of accuracy or applicability. Sensory reserves the right to change any specification or description contained herein. Sensory reserves the right to make changes to or to discontinue any product or service identified in this publication at any time without notice in order to improve design and supply the best possible product. Sensory does not assume responsibility for use of any circuitry other than circuitry entirely embodied in a Sensory product. Information contained herein is provided gratuitously and without liability to any user. Reasonable efforts have been made to verify the accuracy of this information but no guarantee whatsoever is given as to the accuracy or as to its applicability to particular uses. Applications described in this data sheet are for illustrative purposes only, and Sensory makes no warranties or representations that the RSC/SC series of products will be suitable for such applications. In every instance, it must be the responsibility of the user to determine the suitability of the products for each application. Sensory products are not authorized for use as critical components in life support devices or systems. Sensory conveys no license or title, either expressed or implied, under any patent, copyright, or mask work right to the RSC series of products, and Sensory makes balance between recognition and synthesis no warranties or representations that the RSC series of products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Nothing contained herein shall be construed as a recommendation to use any product in violation of existing patents or other rights of third parties. The sale of any Sensory product is subject to all Sensory Terms and Conditions of Sales and Sales Policies.

SENSORY®

1991 Russell Ave., Santa Clara, CA 95054
Tel: **(408) 327-9000** Fax: **(408) 727-4748**