SC0163D
ChiPhy™ Family

Charger Interface Physical Layer IC

PRELIMINARY

Product Highlights

- Supports Quick Charge 2.0 Class A specification
  - 5 V, 9 V, and 12 V output voltage
- Supports Quick Charge 3.0 Class A specification
  - 3.6 V to 12 V output voltage
- USB battery charging specification revision 1.2 compatible
  - Automatic USB DCP shorting D+ to D- line
  - Default 5 V mode operation
- Very low power consumption
  - Below 1 mW at 5 V output
- Fail safe operation
  - Adjacent pin-to-pin short-circuit fault
  - Open-circuit pin fault
- Supports InnoSwitch, TinySwitch and TOPSwitch

Typical Applications

- Battery chargers for smart phones, tablets, netbooks, digital cameras, and bluetooth accessories
- USB power output ports such as battery banks or car chargers

Description

SC0163D is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 3.0 specification. It incorporates all necessary functions to add Quick Charge 3.0 capability to Power Integrations' switcher ICs such as InnoSwitch, TinySwitch, TOPSwitch and other solutions employing traditional secondary-side feedback schemes.

SC0163D supports the full output voltage range of Class A per Quick Charge 3.0 specification.

SC0163D automatically detects whether a connected (PD) is Quick Charge 3.0 or Quick Charge 2.0 capable before enabling output voltage adjustment. If a PD not compliant to Quick Charge 2.0 or 3.0 is detected the SC0163D disables output voltage adjustment to ensure safe operation with legacy 5 V only USB PDs.
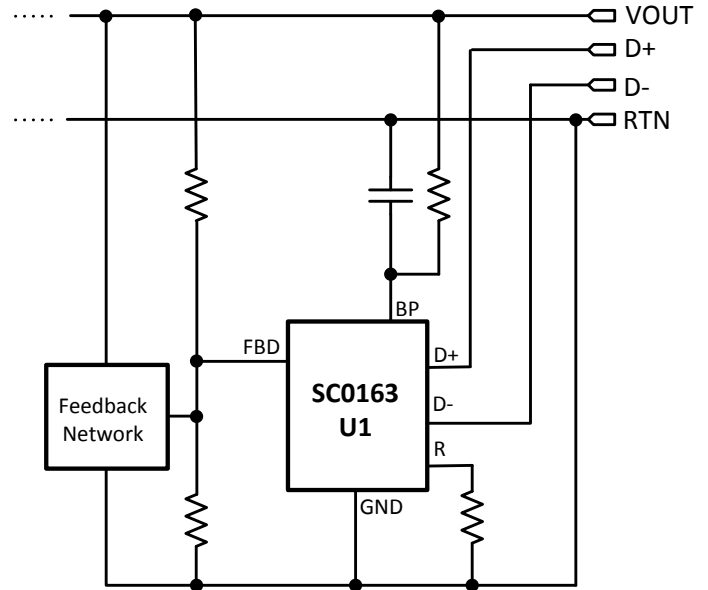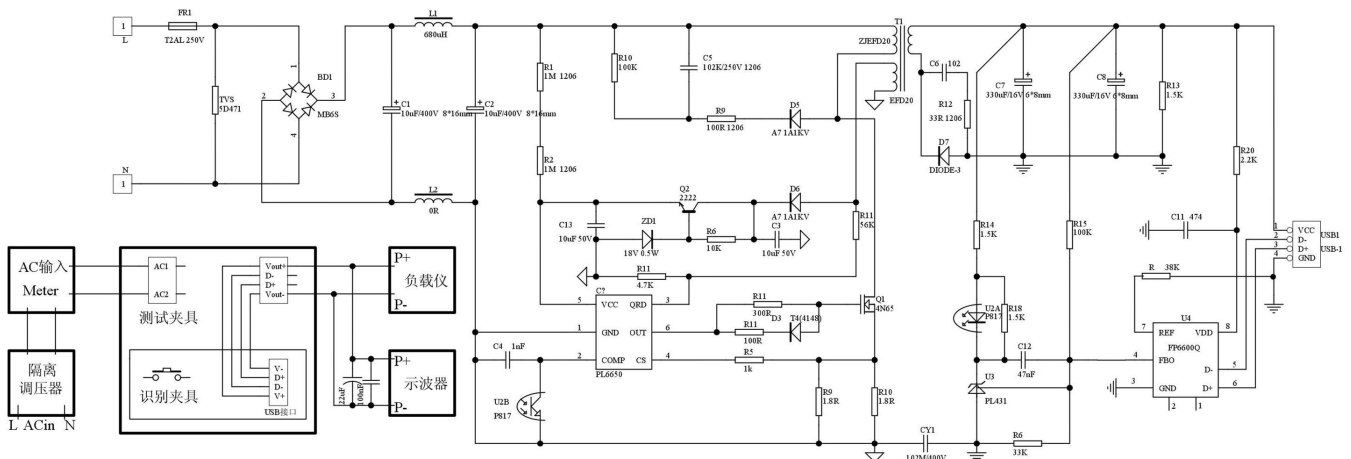

Figure 1. Typical Application Schematic.

FP6600Q CHY103D SC0163D
FCP 1A, 2A, 2.4A
SO-8 (D Package)

FP6600Q http://www.szparkson.net/product/214.html

Figure 2. Package Option.

QC3.0 PL6650＋FP6600Q原理图

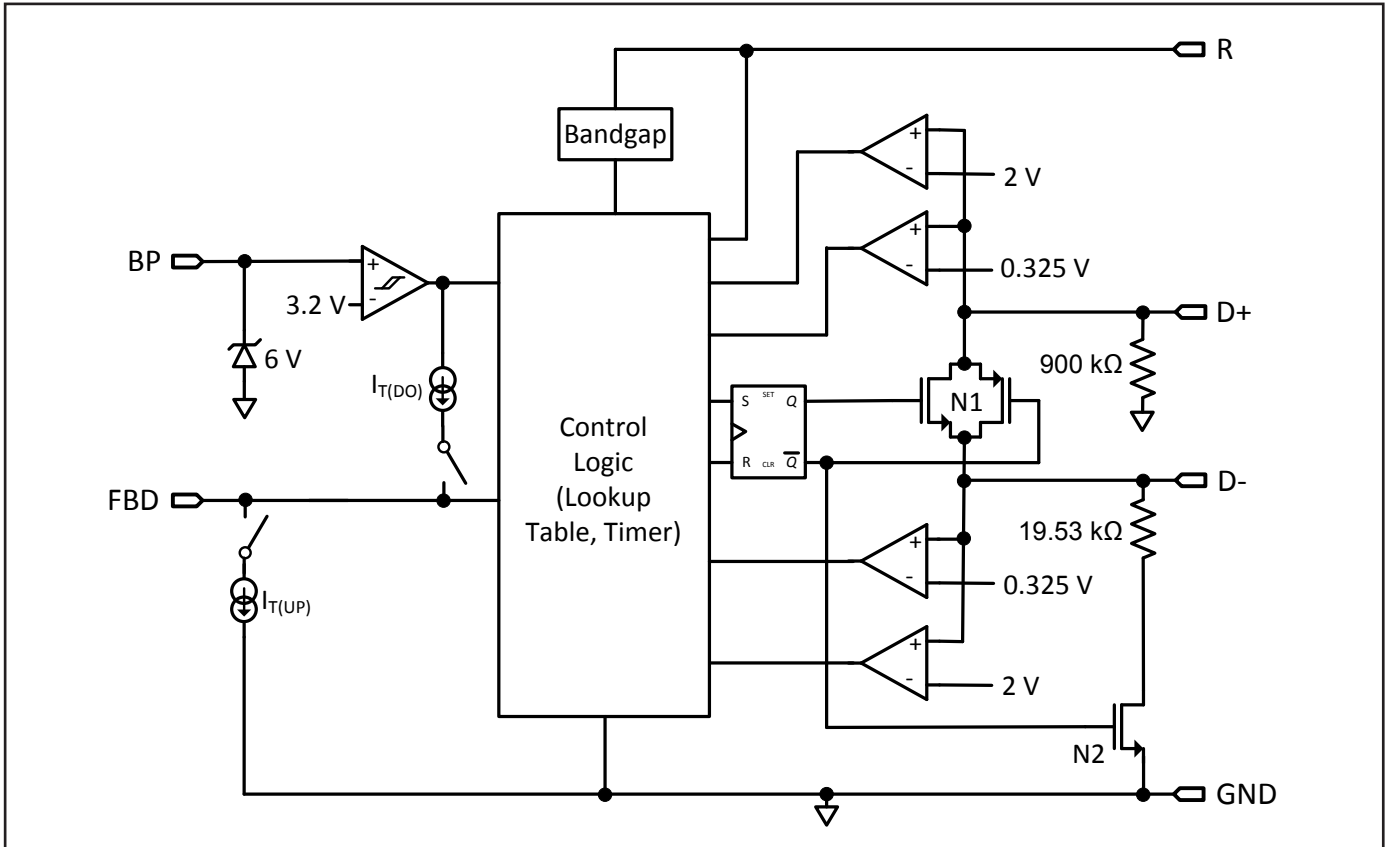*This Product is Covered by Patents and/or Pending Patent Applications.*

Figure 3.   Functional Block Diagram.

Pin Functional Description

GROUND (GND) Pin:
Ground.

FEEDBACK DRIVE (FBD) Pin:
Feedback loop drive output connected to reference input of external power supply error amplifier to set output voltage.

BYPASS (BP) Pin:
Connection point for an external bypass capacitor for the internally generated supply voltage.

REFERENCE (R) Pin:
Connected to internal band-gap reference. Provides reference current through connected resistor.

DATA LINE (D+) Pin:
USB D+ data line input.

DATA LINE (D-) Pin:
USB D- data lien input.

NOT CONNECTED (NC) Pins:
Pin 1 needs to be connected to BYPASS pin on the PCB.
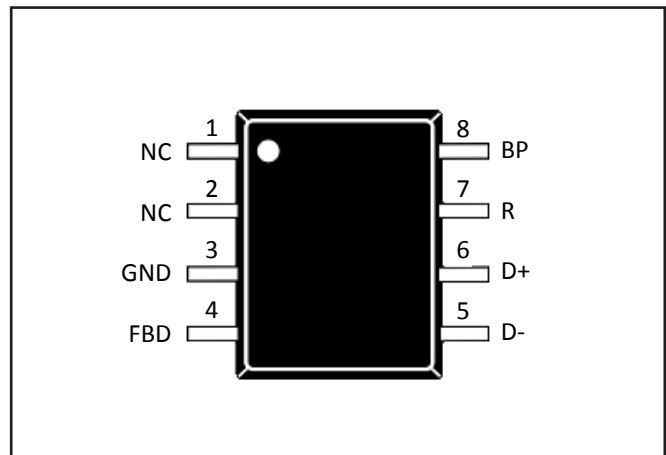Pin 2 needs to be connected to the GROUND pin on the PCB.

Figure 4.   Pin Configuration.

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Functional Description

SC0163D is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 3.0 specification. It incorporates all necessary functions to add Quick Charge 3.0 capability to Power Integrations' switcher ICs such as InnoSwitch, TinySwitch, and TOPSwitch.

SC0163D also supports other solutions with traditional secondary-side feedback schemes such as TL431 for instance.

Figure 5 depicts SC0163D interfacing with Power Integrations' InnoSwitch switcher IC.

SC0163D supports the full output range of Quick Charge 3.0 Class A (3.6 V to 12 V) and its subset Quick Charge 2.0 Class A (5 V, 9 V, or 12 V). It automatically detects either Quick Charge 3.0 or Quick Charge 2.0 capable powered devices (PD) or legacy PDs compliant with USB Battery Charging Specification revision 1.2 and only enables output voltage adjustments accordingly.

Shunt Regulator

The internal shunt regulator clamps the BYPASS pin at 6 V when current is provided through an external resistor (R_{BP} in Figure 5). This facilitates powering SC0163D externally over a wide output voltage range of 3.6 V to 20 V. Recommended values are R_{BP} = 2.21 kΩ ±1% and C_{BP} = 470 nF.

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry resets the SC0163D when the BYPASS pin voltage drops below 2.87 V. Once the BYPASS pin voltage drops below 2.87 V it must rise back to 3.1 V to commence correct operation.

Reference and Output Voltage Range Selection Input

Resistor R_{REF} at the REFERENCE pin is connected to an internal band gap reference and provides an accurate reference current for internal timing circuits. Recommended value is R_{REF} = 38.3 kΩ ±1%.

Quick Charge 3.0 Interface

At power-up SC0163D turns on switch N1 (see Figure 3) short-circuiting USB data lines D+ and D- for the initial handshake between

AC-DC adapter (DCP) and powered device (PD) as described in the USB Battery Charging specification revision 1.2. After the USB BC 1.2 handshake is completed, SC0163D will turn off switch N1 if it detects a Quick Charge 3.0 or Quick Charge 2.0 compliant PD. At this point the Quick Charge 2.0 handshake followed by the Quick Charge 3.0 handshake can take place as described in the Quick Charge 2.0 and Quick Charge 3.0 protocol specification. Upon completion of the Quick Charge 2.0 and Quick Charge 3.0 handshakes, SC0163D will turn on switch N2 (see Figure 3) connecting a 19.53 kΩ pull-down resistor to USB data line D-.

Table 1 summarizes the output voltage lookup and model select table and corresponding AC-DC adapter output voltages.

Portable Device (PD)		SC0163D	
D+	D-	Power Supply Output	Note
0.6 V	0.6 V	12 V	
3.3 V	0.6 V	9 V	
0.6 V	3.3 V	Continuous Mode	±0.2 V step size
0.6 V	GND	5 V	Default mode

Table 1.   Quick Charge 3.0 Output Voltage Lookup and Mode Select Table.

When the USB cable is unplugged the voltage level at D+ is pulled down by SC0163D's internal resistor (see Figure 3). Once it drops below 0.325 V SC0163D will enter default mode (switch N1 is on, switch N2 is off) and sets the default output voltage of 5 V.

Feedback Loop Drive

SC0163D sets the respective output power supply voltage regulation point by directly driving the reference input of the power supply control loop error amplifier through an internal current sink $I_{T(UP)}$ and source $I_{T(DO)}$ (see Figure 6).
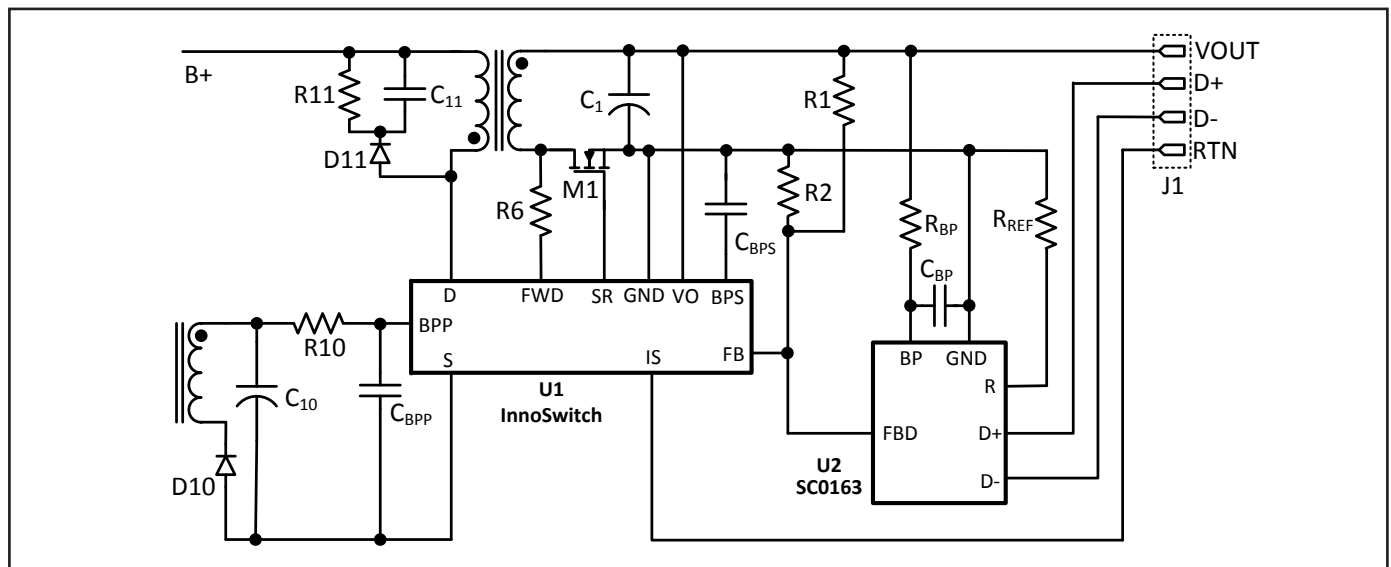
Figure 5.   SC0163D with Power Integrations InnoSwitch Switcher IC.

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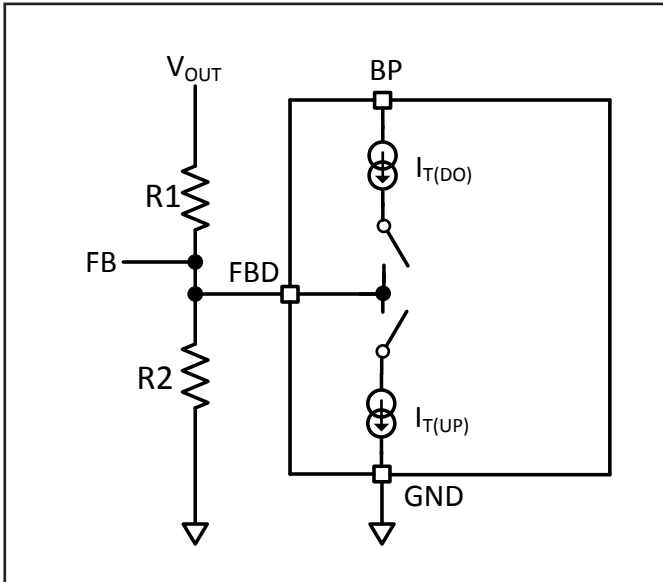
Figure 6.   SC0163D FEEDBACK Pin Drive Output.

In default mode with a 5 V output both, the internal current source and current sink are off. To meet the output voltage step size requirement of ±0.2 V in Quick Charge 3.0 continuous mode, the mandatory value for the upper resistor in the output sensing voltage divider is R1 = 100.0 kΩ ±1%. For a FEEDBACK pin reference voltage of 1.265 V for instance used by Power Integrations' Inno-Switch switcher IC the resulting value for R2 = 34.0 kΩ ±1% to set the default output voltage to 5 V.

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Absolute Maximum Ratings[3]

BYPASS Pin Voltage .... -0.3 to 9 V
REFERENCE Pin Voltage .... -0.3 to 9 V
FBD Pin Voltage .... -0.3 to 9 V
D+/D- Pin Voltage .... -0.3 to 5 V
BYPASS Pin Current ....25 mA
D+/D- Pin Current .... 1 mA[1]
Operating Junction Temperature........................... -40 °C to +150 °C
Operating Ambient Temperature........................... -40 °C to +105 °C

Storage Temperature ....-65 °C to 150 °C
Lead Temperature[2] ....260 °C
Notes:
1. Per USB BC 1.2 and HVDCP specifications.
2. 1/16 in. from case for 5 seconds.
3. The Absolute Maximum Ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Supply and Reference Function						
BYPASS Pin Voltage	V_{BP}	T_J = +25 °C	3.1	4.3	6.3	V
Power-Up Reset Threshold Voltage	$V_{BP(RESET)}$		TBD	2.7	TBD	V
BYPASS Pin Source Current	I_{BPSC}	V_{BP} = 4.3 V, R_{REF} = 38.3 kΩ, T_J = 25 °C			200	μA
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 8 mA	5.7	6	6.3	V
REFERENCE Pin Voltage	V_R	R_{REF} = 38.3 kΩ	TBD	0.383	TBD	V
Data Line D+ and D- Functions (HVDCP Interface)						
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output Voltage Selection Reference	$V_{SEL(REF)}$		1.8	2	2.2	V
Data Lines Short-Circuit Delay	$T_{DAT(SHORT)}$	V_{OUT} ≥ 0.8 V		10	20	ms
D+ High Glitch Filter Time	$T_{GLITCH(BC)DONE}$		1000		1500	ms
D- Low Glitch Filter Time	$T_{GLITCH(DM)LOW}$		1			ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)CHANGE}$		20	40	60	ms
Continuous Mode Glitch Filter Time	$T_{GLITCH(CONT)CHANGE}$		TBD	150	TBD	μs
Continuous Mode Output Change Time	$T_{V(CONT)CHANGE SINGLE}$				2	ms
D+ Leakage Resistance	$R_{DAT(LKG)}$	V_{BP} = 3.1-6.3 V, VD+ = 0.5-3.6 V Switch N1 is Off	300	900	1500	kΩ
D- Pull-Down Resistance	$R_{DM(DWN)}$		14.25	19.53	24.5	kΩ
Switch N1 On-Resistance	$R_{DS(ON)N1}$	V_{BP} = 4.3 V, V_{D+} ≤ 3.6 V, I_{DRAIN} = 200 μA		20	40	Ω
Data Line Capacitance	$C_{DCP(PWR)}$	See Note A			1	nF
FEEDBACK Pin Drive Functions						
Toggle Up Current Source Step	$\Delta I_{T(UP)}$			2		μA
Toggle Down Current Source Step	$\Delta I_{T(DO)}$			2		μA

NOTES:
A. Guaranteed by design. Not tested in production.

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SO-8 (D Package)

0.10 (0.004) C A-B 2X

B

4.90 (0.193) BSC

A

D

DETAIL A

8   5

3.90 (0.154) BSC

6.00 (0.236) BSC

GAUGE PLANE

SEATING PLANE

C

0 - 8°

0.25 (0.010) BSC

1.04 (0.041) REF

0.10 (0.004) C D
2X

Pin 1 ID

1   4

0.20 (0.008) C
2X

0.40 (0.016)
1.27 (0.050)

1.27 (0.050) BSC

7X 0.31 - 0.51 (0.012 - 0.020)

0.25 (0.010) M C A-B D

1.35 (0.053)
1.75 (0.069)

1.25 - 1.65
(0.049 - 0.065)

0.10 (0.004)
0.25 (0.010)

0.10 (0.004) C
7X

DETAIL A

H

SEATING PLANE
C

0.17 (0.007)
0.25 (0.010)

Reference Solder Pad Dimensions

1.45 (0.057) 4.00 (0.157) 5.45 (0.215)

Notes:
1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D08A

1.27 (0.050)   0.60 (0.024)

PI-5615-020515

Part Ordering Information

● **ChiPhy Product Family**
● **SC Series Number**
● **Package Identifier**

SC 0163 D   D │ SO-8

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Notes

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Revision	Notes	Date
A	Preliminary	05/15

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