# SC1406G
# Power Supply Controller for Portable Pentium ® II & III SpeedStep™ Processors



## Description

The SC1406G PowerStep™ controller is a High Speed, High Performance Hysteretic Mode PWM controller. Teamed with the SC1405 Smart™ Driver, it powers advanced Pentium® II and Pentium® III processors. The SC1406G features Intel Mobile Voltage Positioning (IMVP), which increases battery life by reducing the voltage at the processor when it is heavily loaded. It also directly supports Intel's SpeedStep™ processors for even longer battery life.

A 5-bit DAC, accurate to 0.85%, sets the output voltage reference, and implements the 0.925V to 2.00V range of the mobile Pentium® specifications. The hysteretic converter uses a comparator without an error amplifier, and therefore provides the fastest possible transient response, while avoiding the stability issues inherent to classical PWM controllers.

Two linear regulator controllers, coupled with appropriate external transistors, produce tightly regulated 1.5V and 2.5V to complete the processor power solution. The SC1406G also features separate soft-start controls for the converter and the regulators, a TTL-compatible power good indication, logic enable, and low battery undervoltage lockout. Programmable current limiting uses a separate comparator to protect against overloads and short-circuits.

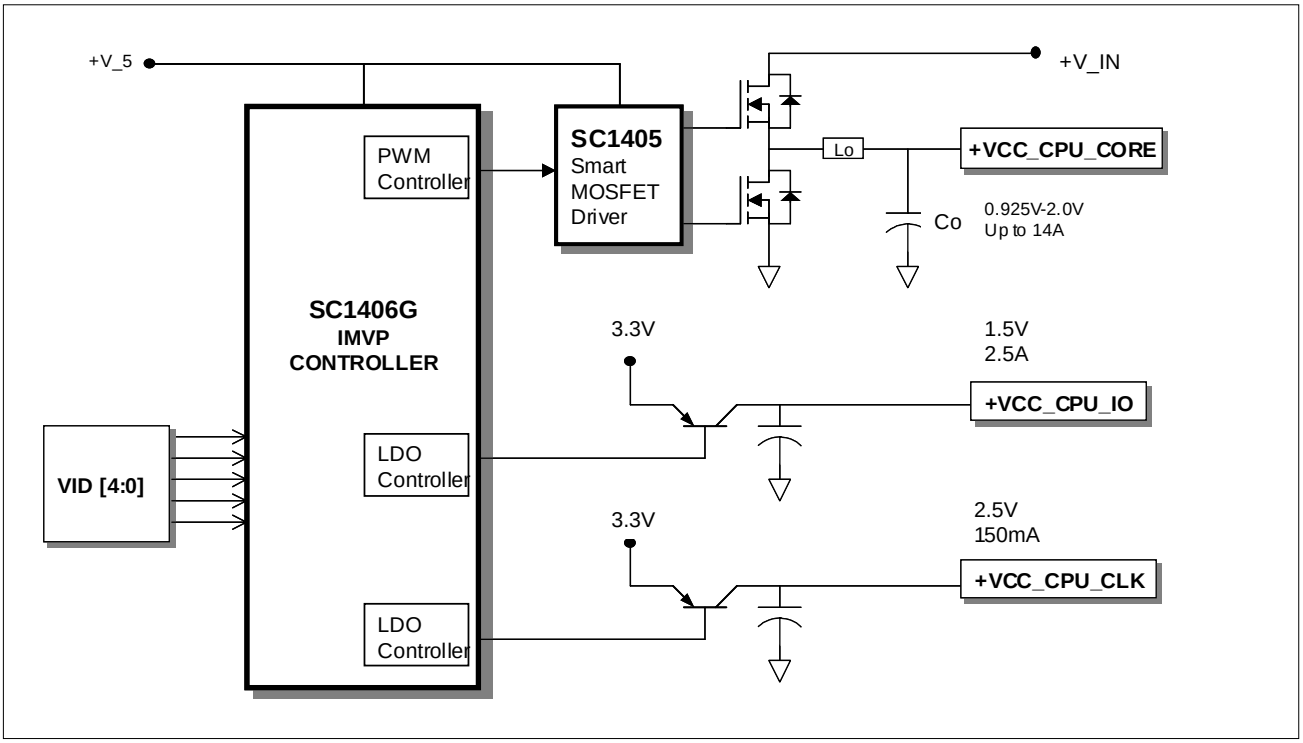
## Features

- High-speed hysteretic controller provides high efficiency over a wide operating load range
- Inherently stable
- Complete CPU power solution with two LDO drivers
- Programmable core voltage for Pentium® II & III processors
- Native Speed Step® support

## Applications

- Laptop and notebook computers
- High performance microprocessor-based systems
- High efficiency distributed power supplies

## Conceptual Application Circuit



## Absolute Maximum Rating

| PARAMETER | SYMBOL | MAXIMUM | UNITS |
|---|---|---|---|
| VCC Supply Voltage | | -0.3 to 7 | V |
| Low Battery Input | LBIN | -0.3 to 7 | V |
| Enable | EN | -0.3 to 7 | V |
| All other I/O pins | | GND - 0.3 to VCC + 0.3 | V |
| Operating Junction Temperature | $T_J$ | 0 to +125 | °C |
| Lead Temperature (Soldering 10 seconds) | $T_L$ | 300 | °C |
| Storage Temperature | $T_{STG}$ | -65 to 150 | °C |

## Electrical Characteristics

Unless specified: -0 < $T_A$ < 100°C; $V_{CC}$ = 3.3V (See test circuit)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply (VCC) | | | | | | |
| Input Supply Voltage Range | | | 3.0 | 3.3 | 6.0 | V |
| Quiescent Current | $I_{CCQ}$ | EN is low, 3.0V < $V_{CC}$ < 3.6V | | | 10 | µA |
| | | EN is high and the LBIN is in UVLO | | | 350 | |
| Operating Current | $I_{CC}$ | EN is high | | 4 | 15 | mA |
| Under Voltage Lock Out Threshold | | | 2.7 | | 2.95 | V |
| Under Voltage Lock Out Hysteresis | | | 20 | | | mV |
| Enable Input | | | | | | |
| Input High | | 3.0 < $V_{CC}$ < 5V | 0.7*$V_{CC}$ | | | V |
| Input Low | | | | | 0.8 | V |
| Low Battery Monitor (LBIN) | | | | | | |
| UVLO Threshold | $V_{THDC}$ | $V_{LBIN}$ > $V_{THDC}$ | 1.175 | 1.225 | 1.275 | V |
| Input Bias Current | | > $V_{THDC}$ | | | ±0.3 | µA |
| | | $V_{LBIN}$ < $V_{THDC}$ | 0.6 | 1.0 | 10.5 | |
| VCORE Power Good Generator: (Note that during the 50µs latency time of any VID code change, the $P_{WRGD}$ output signal may change state one or more times). | | | | | | |
| Over-Voltage Threshold | $V_{HCORE}$ | $V_{DAC}$ = 0.9V to 1.675V | 1.08*$V_{DAC}$ | | 1.12*$V_{DAC}$ | V |
| Under-Voltage Threshold | $V_{LCORE}$ | | 0.88*$V_{DAC}$ | | 0.92*$V_{DAC}$ | V |
| Output Voltage, High | | $I_{PWRGD}$ = 10µA (source) EN is high | 0.95*$V_{CC}$ | | | V |
| Output Voltage, Low | | $I_{PWRGD}$ = 10µA (sink), EN is high | | | 0.4 | V |
| | | $I_{PWRGD}$ = 10µA (sink), the battery is in UVLO | | | 0.8 | V |

## Electrical Characteristics Continued

Unless specified: -0 < $T_A$ < 100°C; $V_{CC}$ = 3.3V (See test circuit)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Core Converter Soft Start Current | | | | | | |
| Core Converter Soft-Start Current | $I_{SSCORE}$ | Charge (Source) current | 0.6 | 1 | 1.45 | µA |
| | | Discharge (Sink) current | 0.30 | 1 | | mA |
| VSSCORE Soft-Start Termination | | | 1.90 | 2.00 | 2.10 | V |
| VSSCORE Discharge Threshold | | | | 150 | 400 | mV |
| VID DAC | | | | | | |
| VID Input High Threshold | | 3.0V < VCC < 3.6V | 0.7*Vc | | | V |
| VID Input Low Threshold | | | | | 0.8 | |
| VID Input Pull-Up Current,VID (0-4) | | VID (0-4) = 00000...11111 | 6 | | 40 | µA |
| Output Voltage Accuracy | | $I_{DAC}$ = 0, VID(0-4) = 00000...11111 | -0.85 | | +0.85 | % |
| Settling Time* | | $C_{DAC}$ = 1000pF<br>VID is set to change VCORE from | | | 35 | µs |
| CORE Comparator (CMP, CMPREF, HYS, CO) | | | | | | |
| Input Bias Current | | $V_{CMP}$ = $V_{CMPREF}$ = 1.3V | | | ±2 | µA |
| Input Offset Voltage | | $V_{CMPREF}$ = 1.3V | | ±1.5 | ±3 | mV |
| Hysteresis Setting Current | $I_{CMPREF}$ | $R_{HYS}$ = open | | | ±2 | µA |
| | | $R_{HYS}$ = 170kΩ | ±7 | ±10 | ±13 | |
| | | $R_{HYS}$ = 17kΩ | ±85 | ±100 | ±115 | |
| Output Voltage High | | Load Impedance = 100k in parallel with 10pF, VCC = 3.0V | 2.5 | | | V |
| Output Voltage Low | | Load Impedance = 100k in parallel with 10pF, VCC = 3.6V | | | 0.4 | V |
| Propagation Delay Time**<br>Measured at device pins, from the trip point to 50% of CO transition. | | $V_{CMPREF}$ = 1.3V, D VCMP = ± 40mV (±20mV overdrive)<br>$T_A$ = 25°C<br>$T_A$ = full range | | | 20<br>30 | ns |
| Output Rise/Fall Times**<br>Measured between 30% and 70% points of CO transition | $T_R$ | $C_{CO}$ = 10pF<br>$V_{CC}$ = 3.0V<br>$R_{CO}$ = 100K | | 7 | 10 | ns |

## Electrical Characteristics Continued

Unless specified: -0 < $T_A$ < 100°C; $V_{CC}$ = 3.3V (See test circuit)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Current Limit Comparator (CL, CLREF, CLSET) | | | | | | | |
| Input Bias Current | | $V_{CL}$ = 1.3V | | | | 5 | µA |
| Current Limit Setting Current | $\|I_{CLREF}\|$ | $R_{CLSET}$ = open | $V_{CLREF}$ - $V_{CL}$ = 10mV | | | 7.5 | µA |
| | | | $V_{CLREF}$ - $V_{CL}$ = -10mV | | | 5.0 | |
| | | $R_{CLSET}$ = 170kΩ | $V_{CLREF}$ - $V_{CL}$ = 10mV | 19.5 | 30 | 40.5 | µA |
| | | | $V_{CLREF}$ - $V_{CL}$ = -10mV | 13 | 20 | 27 | |
| | | $R_{CLSET}$ = 42.5kΩ | $V_{CLREF}$ - $V_{CL}$ = 10mV | 100.5 | 120 | 139.5 | µA |
| | | | $V_{CLREF}$ - $V_{CL}$ = -10mV | 67 | 80 | 93 | |
| | | $R_{CLSET}$ = 20kΩ | $V_{CLREF}$ - $V_{CL}$ = 10mV | 222 | 255 | 288 | µA |
| | | | $V_{CLREF}$ - $V_{CL}$ = -10mV | 148 | 170 | 192 | |
| | | $R_{CLSET}$ = 17kΩ | $V_{CLREF}$ - $V_{CL}$ = 10mV | 262.5 | 300 | 337.5 | µA |
| | | | $V_{CLREF}$ - $V_{CL}$ = -10mV | 175 | 200 | 225 | |
| Input Offset Voltage | $V_{CL}$ - $V_{CLREF}$ | $V_{CLREF}$ = 1.3V | | | ±4 | ±6 | mV |
| Propagation Delay Time** Measured at the device pins, from the trip point to 50% of CO transition | | $V_{CLREF}$ = 1.3V, Δ VCMP = ±50mV (±20mV overdrive) $T_A$ = 25°C | | | | 100<br>150 | ns |

## Electrical Characteristics Continued

Unless specified: -0 < $T_A$ < 100°C; $V_{CC}$ = 3.3V (See test circuit)

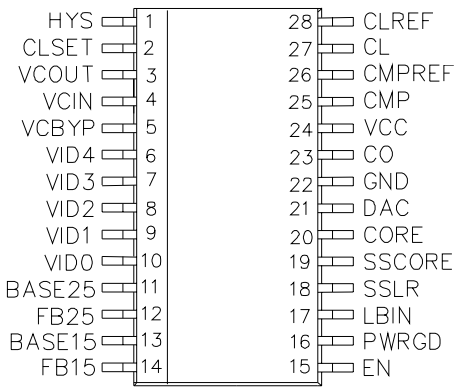
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| 1.5V Linear Regulator Controller | | | | | | | |
| Input Bias Current | | $V_{FB15}$ = 1.5V | | | | 1 | mA |
| Output Voltage, $V_{FB15}$<br>$C_{O\_1.5}$ = 56µF, 20mW ESR max<br>or 150µF, 45mW ESR max<br>Capacitance tolerance = 20% | | External pnp BJT with $B_{MIN}$ > 50 @<br>$I_C$ = 500mA<br>$I_O$ = 0mA to 500mA | | 1.47 | 1.50 | 1.54 | V |
| Base Drive Output Current | | $T_A$ = 25°C | | 10 | | 120 | mA |
| 2.5V Linear Regulator Controller | | | | | | | |
| Input Bias Current | | $V_{FB15}$ = 2.5V | | | | 1 | mA |
| Output Voltage, $V_{FB15}$<br>$C_{O\_1.5}$ = 56µF, 20mW ESR max<br>or 150µF, 45mW ESR max<br>Capacitance tolerance = 20% | | External pnp BJT with $B_{MIN}$ > 50 @<br>$I_C$ = 100mA<br>$I_O$ = 0mA to 100mA | | 2.45 | 2.50 | 2.55 | V |
| Base Drive Output Current | | $T_A$ = 25°C | | 2.5 | | 20 | mA |
| Linear Regulator Soft Start (LRSS) | | | | | | | |
| Linear Reg Soft Start Current | $I_{LRSS}$ | Charge Current = $V_{LRSS}$ = 0V | | -0.6 | -1 | -1.45 | µA |
| | | Discharge Current, $V_{LRSS}$ = 1.50V,<br>EN is low or the battery is in UVLO | | 0.3 | 1 | | mA |
| Enable Threshold | | | | | 150 | 400 | mA |
| Soft-Start Termination Threshold | | | | 1.53 | 1.70 | 1.87 | V |
| Voltage Clamp (VCIN, VCOUT, VCBYP) (Note: This circuit section is rarely used). | | | | | | | |
| Input Voltage | | | | 0.93 | 1.5 | 1.60 | V |
| Output Voltage | | $R_{VCOUT}$ = 150W<br>tied to $V_S$ = 2.5V<br>$I_{VCIN}$ = -10µA | $V_{CIN}$ is Open | 0.8Vs | | Vs | V |
| | | | $V_{VCIN}$ = 0.175V | | | 0.375 | |
| Progagation Delay** | | $R_{VCOUT}$ = 150W tied to VS = 2.5V<br>$C_{VCBYP}$ = 1500pF, VCIN steps from<br>0.175V to 1.50V and back.<br>Measured from 50% of VCIN step to<br>50% of VCOUT transient | | | | 10 | nS |

* Guaranteed by design.

**Guaranteed by characterization.

## Pin Configuration

Top View



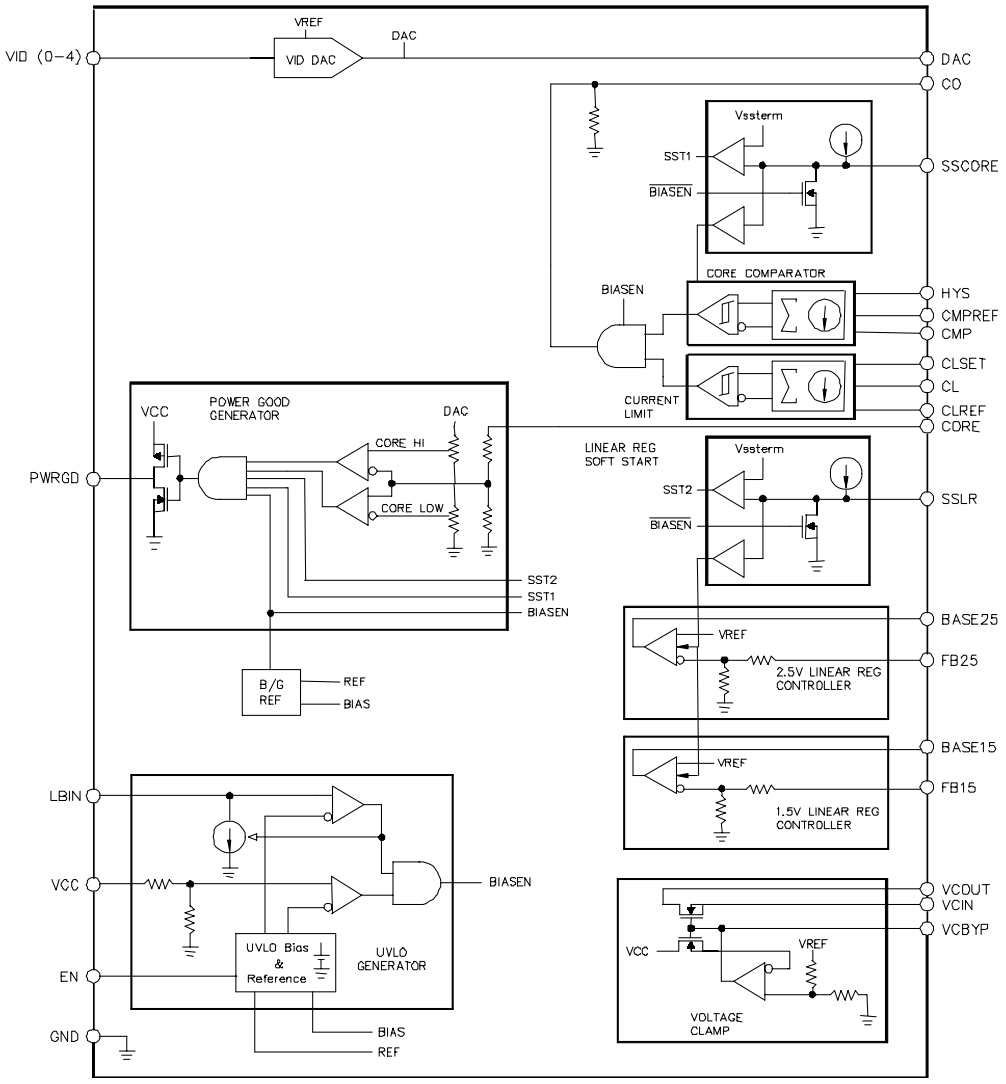

TSSOP - 28

## Ordering Information

| DEVICE | PACKAGE | TEMP. ($T_J$) |
|---|---|---|
| SC1406GCTSTR | TSSOP-28 | 0 to 125°C |

Note:
Only available in tape and reel packaging. A reel contains 2500 devices.

## Block Diagram



## Pin Descriptions

| Pin | Pin Name | Pin Function |
|---|---|---|
| 1 | HYS | Core comparator hysteresis setting. |
| 2 | CLSET | Current limit setting. |
| 3 | VCOUT | Voltage clamp output. Leave open if not used. |
| 4 | VCIN | Voltage clamp input. Tie to GND if not used. |
| 5 | VCBYP | Voltage clamp bypass pin. Requires a 1500pF cap from this pin to GND. Leave open if not used. |
| 6 | VID4 | VID (voltage identification) most significant bit. |
| 7 | VID3 | VID input |
| 8 | VID2 | VID input |
| 9 | VID1 | VID input |
| 10 | VID0 | VID least significant bit. |
| 11 | BASE 25 | 2.5V Linear regulator drive. |
| 12 | FB25 | 2.5V Linear regulator output feedback. |
| 13 | BASE 15 | 1.5V Linear regulator drive. |
| 14 | FB15 | 1.5V Linear regulator output feedback. |
| 15 | EN | Enable. SC1406G is enabled when this logic signal is High. Teamed with the SC1405 driver, this pin can be connected to the PWRDY pin of the SC1405. |
| 16 | PWRGD | Power Good. When the main converter output approaches and stays within ±10% of the VID DAC setting, and both soft-start periods terminate, this signal is pulled up to VCC. During under-voltage lockout, this signal is undefined. During a SpeedStep™ transition, PWRGD may toggle one or more times. |
| 17 | LBIN | Low battery input. This pin is used to set the minimum voltage to the converter through an external resistor divider. When the input to this pin is less than 1.225V the SC1406G is held in UVLO regardless of the status of EN. |
| 18 | SSLR | Linear regulators soft start. During a normal power-up the external soft-start capacitor (1200pF, typ) is charged by an internal 1µA current source to set the ramp-up time of the linear regulator outputs, 1.5V and 2.5V. This ramp-up time is typically 2ms, 6ms max. The capacitor is discharged through an internal switch when EN is low or the VCC or LBIN pins are under voltage. A new soft-start cycle will not begin until the pin voltage drops below a threshold of 150mV typical (200mV max). (The linear regulator soft-start current and the core soft-start current track each other to within ±10%.) |
| 19 | SSCORE | Main controller CORE output soft start. During a normal power-up the external soft-start capacitor (1800pF, typ) is charged by an internal 1µA current source to set the ramp-up time of the linear regulator outputs, 1.5V and 2.5V. This ramp-up time is typically 3ms, 6ms max. The capacitor is discharged through an internal switch when EN is low or the VCC or LBIN pins are under voltage. A new soft-start cycle will not begin until the pin voltage drops below a threshold of 150mV typical (200mV max). (The linear regulator soft-start current and the core soft-start current track each other to within ±10%.) |
| 20 | CORE | Main CORE converter output feedback. |
| 21 | DAC | Main controller digital to analog output. |
| 22 | GND | Ground |
| 23 | CO | Comparator output. Main regulator controller output used to drive the input of the MOSFET driver IC, such as the SC1405. |
| 24 | VCC | Supply voltage input. This input is capable of accepting 3.3V or 5.0V supply voltage. |
| 25 | CMP | Core comparator input. |
| 26 | CMPREF | Core comparator reference input. |
| 27 | CL | Current limit input. |
| 28 | CLREF | Current limit reference input. |

## VID vs. $V_{DAC}$ Voltage

| VID4 | VID3 | VID2 | VID1 | VID0 | $V_{DAC}$ (volts) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 2.00 |
| 0 | 0 | 0 | 0 | 1 | 1.95 |
| 0 | 0 | 0 | 1 | 0 | 1.90 |
| 0 | 0 | 0 | 1 | 1 | 1.85 |
| 0 | 0 | 1 | 0 | 0 | 1.80 |
| 0 | 0 | 1 | 0 | 1 | 1.75 |
| 0 | 0 | 1 | 1 | 0 | 1.70 |
| 0 | 0 | 1 | 1 | 1 | 1.65 |
| 0 | 1 | 0 | 0 | 0 | 1.60 |
| 0 | 1 | 0 | 0 | 1 | 1.55 |
| 0 | 1 | 0 | 1 | 0 | 1.50 |
| 0 | 1 | 0 | 1 | 1 | 1.45 |
| 0 | 1 | 1 | 0 | 0 | 1.40 |
| 0 | 1 | 1 | 0 | 1 | 1.35 |
| 0 | 1 | 1 | 1 | 0 | 1.30 |
| 0 | 1 | 1 | 1 | 1 | NO CPU* |
| 1 | 0 | 0 | 0 | 0 | 1.275 |
| 1 | 0 | 0 | 0 | 1 | 1.250 |
| 1 | 0 | 0 | 1 | 0 | 1.225 |
| 1 | 0 | 0 | 1 | 1 | 1.200 |
| 1 | 0 | 1 | 0 | 0 | 1.175 |
| 1 | 0 | 1 | 0 | 1 | 1.150 |
| 1 | 0 | 1 | 1 | 0 | 1.125 |
| 1 | 0 | 1 | 1 | 1 | 1.100 |
| 1 | 1 | 0 | 0 | 0 | 1.075 |
| 1 | 1 | 0 | 0 | 1 | 1.050 |
| 1 | 1 | 0 | 1 | 0 | 1.025 |
| 1 | 1 | 0 | 1 | 1 | 1.000 |
| 1 | 1 | 1 | 0 | 0 | 0.975 |
| 1 | 1 | 1 | 0 | 1 | 0.950 |
| 1 | 1 | 1 | 1 | 0 | 0.925 |
| 1 | 1 | 1 | 1 | 1 | NO CPU* |

* output is disabled

## Functional Description

### SUPPLY

The chip is optimized to operate from a 3.3V ± 5% rail but is also designed to work up to 6V maximum supply voltage.

### UNDER VOLTAGE LOCK-OUT CIRCUIT

The under voltage lockout (UVLO) circuit consists of two comparators, the low battery and low $V_{CC}$ (low supply voltage) comparators. The output of the comparator, gated with the Enable signal, turns on or off the internal bias, enables or disables the CO output, and initiates or resets the soft start timers.

### POWER GOOD GENERATOR

If the chip is enabled but not in UVLO condition, and the core voltage gets within ±10% of the VID programmed value, then a high level Power Good signal is generated on the PWRGD pin to trigger the CPU power up sequence. If the chip is either disabled or enabled in UVLO condition, then PWRGD stays low. This condition is satisfied by the presence of an internal 200kW pull-down resistor connected from PWRGD to ground.

During soft start, PWRGD stays low independently from the status of Vcore voltage.

PWRGD is high when all of the following conditions are true:

1. EN is high
2. Soft-start has completed
3. LBIN and VCC are above their under-voltage trip levels.

### BAND GAP REFERENCE

A better than ±1% precision band-gap reference acts as the internal reference voltage standard of the chip, which all critical biasing voltages and currents are derived from. All references to VREF in the equations to follow will assume $V_{REF}$ = 1.7V.

### CORE CONVERTER CONTROLLER

#### Precision VID DAC Reference

The 5-bit digital to analog converter (DAC) serves as the programmable reference source of the core comparator. Programming is accomplished by CMOS logic level VID code applied to the DAC inputs. The VID code vs. the DAC output is shown in the Output Voltage Table. The accuracy of the VID DAC is maintained on the same level as the band gap reference. There is a 10µA pull-up current on each DAC input when EN is high.

#### Core Comparator

This is an ultra-fast hysteretic comparator with a typical propagation delay of approximately 20ns at a 20mV overdrive.

This chip can be used in a standard hysteretic mode controller configuration and in an IMVP hysteretic controller scheme.

Detailed instructions for the IMVP solution are found in the PowerStep™ solution design procedure section of this datasheet.

#### Current Limit Comparator

The current limit comparator monitors the core converter output current and turns the high side switch off when the current exceeds the upper current limit threshold, VHCL and re-enable only if the load current drops below the lower current limit threshold, VLCL. The current is sensed by monitoring the voltage drop across the current sense resistor, $R_{CS}$, connected in series with the core converter main inductor (the same resistor used for IMVP input signal generation). The thresholds have the following relationships:

$$V_{HCL} = 3 \bullet \frac{R_{CLOH}}{R_{CLSET}} \bullet V_{REF}$$

$$V_{LCL} = 2 \bullet \frac{R_{CLOH}}{R_{CLSET}} \bullet V_{REF}$$

$$V_{HYSCL} = \frac{R_{CLOH}}{R_{CLSET}} \bullet V_{REF}$$

#### Core Converter Soft Start Timer

This circuit controls the ramp-up time of the core voltage in order to reduce the initial inrush current on the core input voltage (battery) rail. The soft-start circuit consists of an internal current source, external soft-start timing capacitor, internal discharge switch across the capacitor, and a comparator monitoring the capacitor voltage.

### LINEAR REGULATOR CONTROLLERS

#### 1.5V Linear Regulator

This block is a low drop-out (LDO) linear-regulator controller, which drives an external PNP bipolar transistor as a pass element. The linear regulator is capable of delivering 500mA steady-state DC current and can support transient currents of greater than 1A, depending on pass element and output capacitor selection.

#### 2.5V Linear Regulator

This block is a low drop-out (LDO) linear regulator controller, which drives an external PNP bipolar transistor as a pass element. The LDO linear regulator is capable of delivering 100mA steady-state DC current and can support transient currents greater than 200mA, depending on pass element and output capacitor selection.

#### Linear Regulator Soft-Start

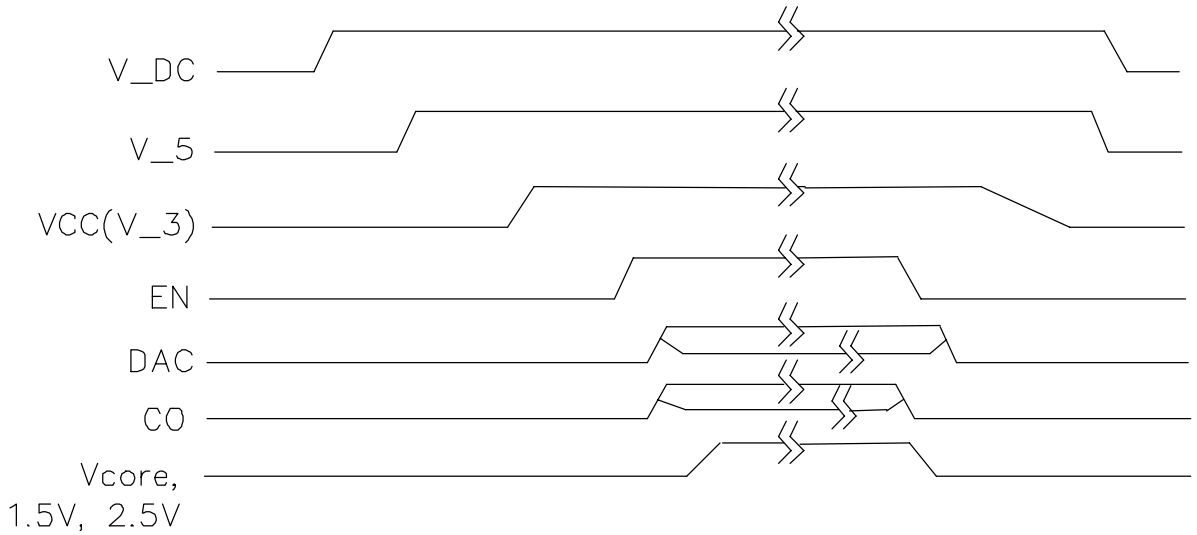
The soft-start circuit of the linear regulators is similar to that of the core converter, and is used to control the ramp-up time of the linear regulator output voltages. For maximum flexibility in controlling the start-up sequence, the soft-start function of the linear regulators is separated from that of the core converter.

VOLTAGE CLAMP

This level translator converts an input voltage swing on the IO rail, into a voltage swing on the CL or VCC rail depending on where the open-drain output of the translator is tied to through an external pull-up resistor. The level translator tracks the input in phase, and switches in 5ns (typical) following an input threshold intercept.

## Applications Information

**Power on/off Sequence**




### PowerStep™ Solution Design Procedure

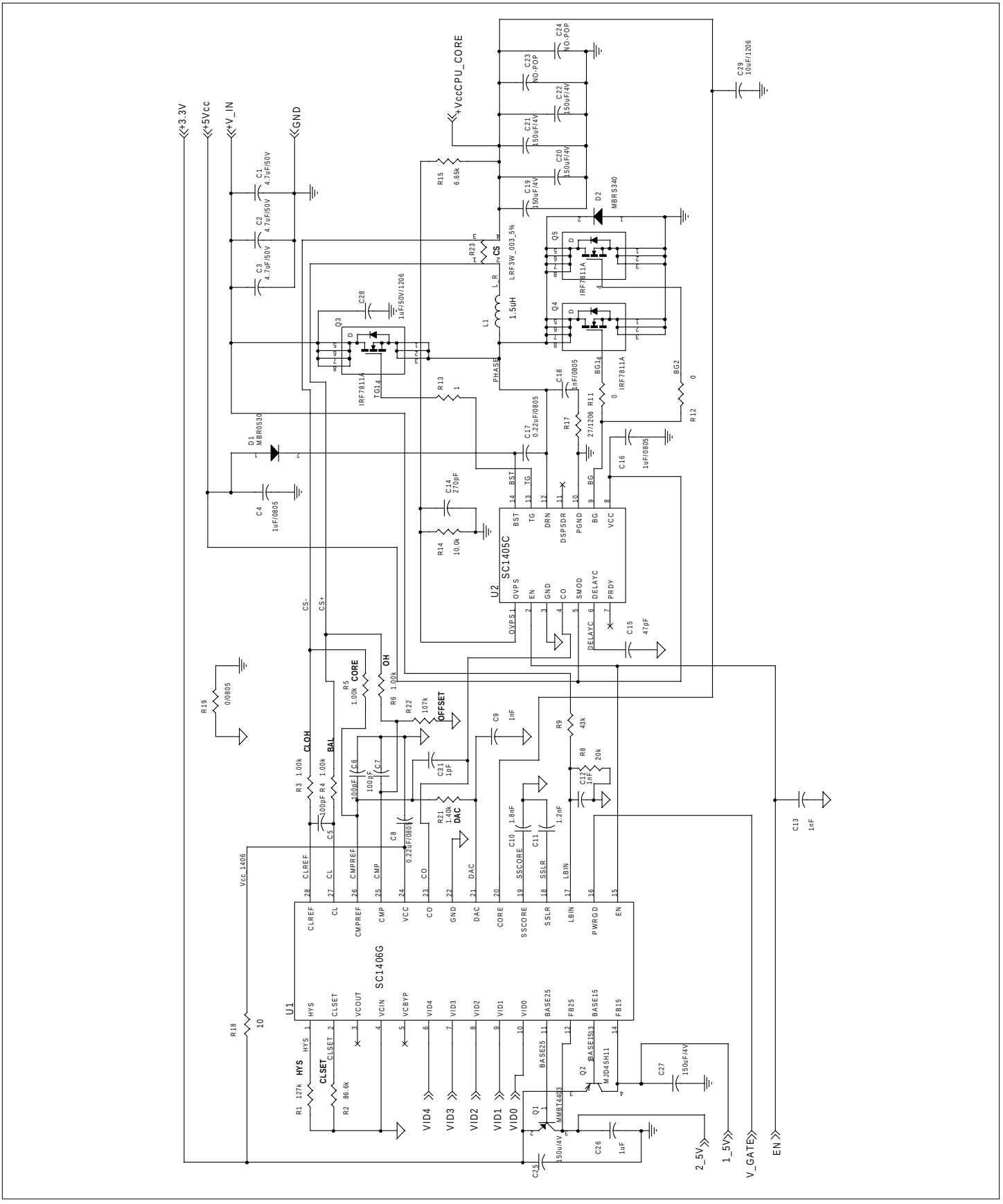
Introduction:

The SC1406G (PowerStep™ for SpeedStep™) and SC1405 Smart™ Driver power chip set provides a flexible, high performance power solution to the requirements of Intel® mobile SpeedStep™ processors.

The SC1406G is a control IC that integrates a synchronous step-down controller for $V_{CORE}$ and two low-dropout regulator (LDO) controllers for $V_{I/O}$, and $V_{CLK}$. In addition, the SC1406G also has a low-battery detector and a clamp circuit. The SC1405 is a Smart™ Driver IC with programmable dead time and industry-leading speed.

The synchronous step-down converter is a hysteretic type, where the output voltage is compared against a VID programmable reference ($V_{DAC}$) with a resistor programmable offset, $V_{HYS}$. The basic operation of the converter is very simple: Referring to Figure 1, with the voltage at the reference, $Q_H$ is off, $Q_L$ is on and the output filter (L and C) discharge into load R. When the output voltage hits the lower hysteresis point, the switches reverse state, and the RLC network charges up to the upper hysteresis value.

## Typical Application Schematic



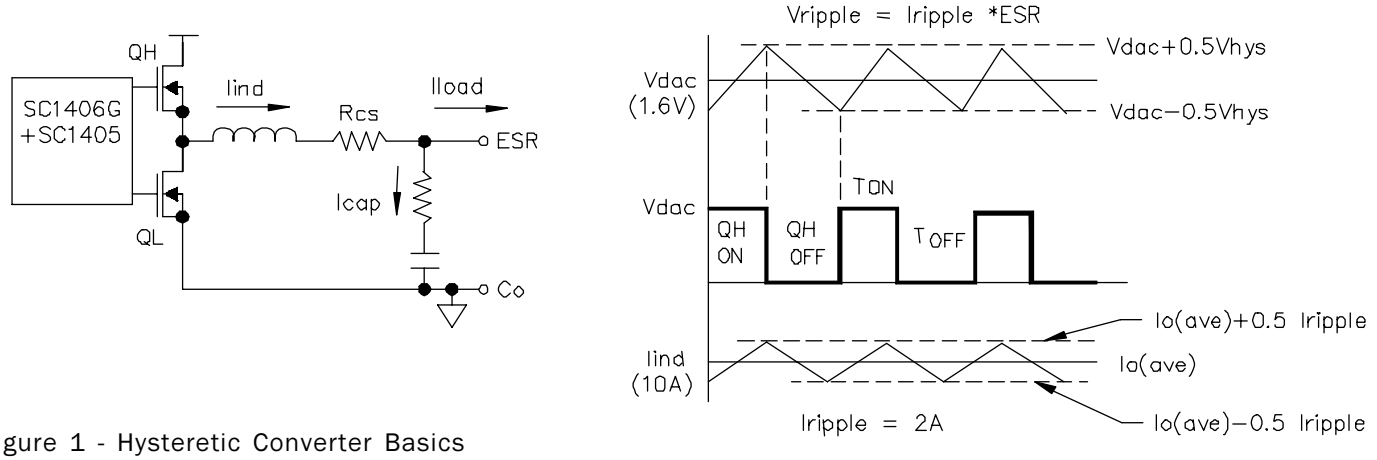



Figure 1 - Hysteretic Converter Basics

The major advantages of this approach are simplicity, inherent stability (there are no reactive elements in the control circuit to provide the phase shift required for classical stability problems), and the fastest possible transient response. Any transient which takes the voltage out of the hysteretic range forces the converter immediately into the proper response. There are no error voltages to slew, and no maximum or minimum duty cycle limits to slow the transient response as in most other control schemes. A significant benefit of the controller/driver architecture is that low-level analog control functions do not have to coexist in an environment of thousands of volts and amps per microsecond, reducing noise problems.

The SC1406G also supports the Intel Mobile Voltage Positioning (IMVP) functions. In short, IMVP allows notebook designers to reduce the output voltage with increasing load current. This has two potential benefits:

- IMVP minimizes power by reducing the voltage under heavy loads; processor power is proportional to $V^2$, so a 5% reduction in voltage results in a nearly 10% reduction in power drawn by the processor.
- IMVP can reduce the number of capacitors required to respond to transients by producing a larger allowable transient; briefly, the no-load voltage is positioned above nominal, so when a transient occurs, the load has farther to drop before hitting the regulation limit. The loaded voltage is allowed to remain below the nominal so that when the load returns to zero, the voltage can rise farther without reaching the transient specification. Since the allowable transient voltages are larger, less capacitance and higher ESR can provide the required performance.

The SC1406G provides the precise voltage positioning required by IMVP because it employs a current-sense resistor, multiplied by a gain set by external resistors to very accurately set the voltage as a function of load current.

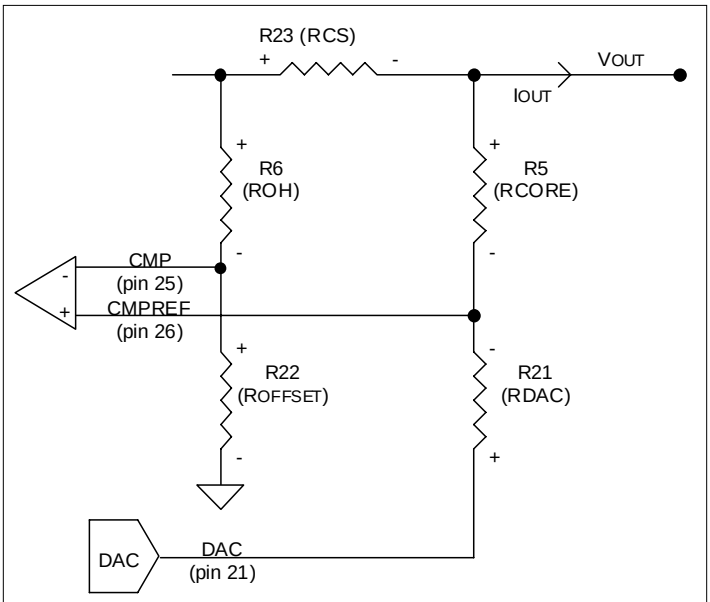



Figure 2—IMVP Example Illustration

The SC1406G implements IMVP, previously named DSPS (dynamic set-point switching) in the following manner: Please see Figure 2 above, and assume, for simplicity:

- $R_{OFFSET}$ is open
- The current into the CMP and CMPREF pins is zero.

Then, please note:

- The SC1406G regulates to the "+" side of the current sense resistor, because that is where the CMP pin is tied, and,
- No current flows through $R_{OH}$, since the input current of the comparator is ~0; $V(R_{OH}) = 0$.
- The difference in voltage between CMP and CMPREF is ~0V in order for the controller to be in regulation

In these conditions:

- At zero load, $V_{OUT} = V_{DAC}$ and the voltage across the current sense resistor is also zero;
- As the load increases, a voltage is developed across

$R_{CS}$; $V(R_{CS}) = I_{OUT} * R_{CS}$.
- In order to keep the voltage between CMP and CMPREF = 0V, $V(R_{CS})$ appears across $R_{CORE}$.
- $V(R_{CS}) + V(R_{CORE}) = 0$, so $V(R_{CORE}) = -V(R_{CS})$; therefore, a current flows through $R_{CORE}$ from $V_{OUT}$ to CMPREF.
- $I(R_{CORE}) = I_{OUT} * R_{CS} / R_{CORE}$
- An equal, but opposite current must flow in $R_{DAC}$, so the voltage at CMPREF is reduced by $I(R_{CORE})$ I $R_{DAC}$, so $V_{CMPREF} = V_{DAC} - I(R_{CORE}) * R_{DAC}$
- Substituting the equations from above: $V_{CMPREF} = V_{DAC} - I_{OUT} * R_{CS} * R_{DAC} / R_{CORE}$
- Since $V_{OUT} = V_{CMPREF} - V(R_{CS})$, with a little algebra:
- $V_{OUT} = V_{DAC} - I_{OUT} * R_{CS} (1 + R_{DAC} / R_{CORE})$

So, with the SC1406G, you get an accurate, linear droop greater than the drop across the current sense resistor, without the efficiency penalty of a large $R_{CS}$, with a gain that is set by 1% resistors! Adding $R_{OFFSET}$ shifts the position at zero current, as described later.

For further information on IMVP, consult the Intel yellow-cover document "Intel® Mobile Voltage Positioning Voltage Regulation Controller Application Note", Reference Number OR-2101.

The SC1405, a smart MOSFET driver, provides industry-leading performance, driving a 3000pF load in under 15nS, typically. Not only does the SC1405 offer built-in shoot-through protection, but also has externally programmable dead time. In addition, it provides other protection and performance features, such as under-voltage lock-out (UVLO), programmable adaptive over-voltage protection (OVP), and the SMOD pin, which may be used to force the low-side gate drive LO during very light load conditions to prevent negative circulating current in the inductor. It comes in the small TSSOP-14 package.

## DESIGN PROCEDURE:

### Requirements:

The first step in designing any converter is in defining the requirements, which can come from many sources. For the SC1406G, you need to determine the minimum and maximum input voltages, which are determined by the battery and AC adapter characteristics, unless you plan to use an existing regulated voltage, such as +5V. The processor determines other requirements; they are:

- Maximum output voltage
- Minimum output voltage
- Maximum output current
- Minimum output current
- Maximum transient current
- Transient voltage requirements

One decision you need to make is whether a positive offset voltage at zero current is desirable. Providing this offset results in having a larger transient response band to work with, thereby providing a solution with the fewest output capacitors. On the other hand, this also means that at low currents, the processor will burn more power than without the offset, since $CV^2F$ still applies, so battery life will be reduced.

The numbers in the sample calculations are taken from the Intel Mobile Pentium III Processor in BGA2 and Micro-PGA2 Packages Datasheet, Revision 1.0, Document Number: 245302-002. Please consult the data for your specific processor.

### Hysteretic Converter Design Equations:

The "Typical Application Schematic on Page 12 is a schematic of the sample converter. Note that several of the resistors have annotations along with reference designators and values. These resistors set the basic functions and IMVP.

Referring to Figure 1, the basic equations for a hysteretic converter are:

$$1)\quad V_{HYS} := d \cdot \frac{(V_{IN} - V_{OUT}) \cdot (ESR + R_{CS})}{F_S \cdot L}$$

where,

$$2)\quad d := \frac{T_{ON}}{(T_{ON} + T_{OFF})} \qquad d := \frac{V_{OUT}}{V_{IN}}$$

IIn equation 2), "d" is commonly referred to as the duty cycle. The output voltage of the SC1406G is set digitally by the VID (0:4) inputs, producing a voltage at the DAC output (pin 21) accurate to better than 0.85%. The DAC voltage requirements are given in the referenced Intel document and the SC1406G datasheet. A similarly accurate fixed voltage internal bandgap reference, Vref, has a nominal value of 1.70V, and is used for setting voltage hysteresis and current limiting levels. In addition, these references are used to provide active voltage positioning — adjusting the output voltage as a function of load current scaled by external resistors.

The output voltage of an IMVP converter has three components:

- The programmed DAC voltage, $V_{DAC}$
- The load dependent droop $V_{IMVP}$
- An optional positive offset, $V_{OFFSET}$

In equation form,

$$3)\quad V_{OUT} := V_{DAC} - V_{IMVP} + V_{OFFSET}$$

The full equations for the IMVP converter are:

$$4)\ V_{OUT} := \frac{V_{DAC} \cdot (R_{OFFSET} + R_{OH}) \cdot R_{CORE} - I_{OUT} \cdot R_{CS} \cdot R_{OFFSET} \cdot (R_{CORE} + R_{DAC})}{R_{CORE} \cdot R_{OFFSET} + R_{DAC} \cdot R_{OH}}$$

5) $$V_{RIPPLE} := 2 \cdot V_{HYS} \cdot \frac{R_{CORE} \cdot (R_{OFFSET} + R_{OH})}{R_{CORE} \cdot R_{OFFSET} + R_{DAC} \cdot R_{OH}} \cdot \frac{ESR}{ESR + \frac{R_{CORE} \cdot (R_{OFFSET} + R_{OH})}{R_{CORE} \cdot R_{OFFSET} + R_{DAC} \cdot R_{OH}} \cdot R_{CS}}$$

For customers familiar with the Intel IMVP application notes, the above schematic has the IMVP resistors denoted using bold lettering. To these resistors, Semtech has added one additional resistor, $R_{BAL}$, which is used to balance the impedance at the current limit comparator for improved noise performance. A cross-reference between the IMVP nomenclature and the reference designator in the schematic above is provided in the table below.

| Intel Nomenclature | Schematic Reference Designator |
|---|---|
| $R_{HSY}$ | R1 |
| $R_{CLSET}$ | R2 |
| $R_{CORE}$ | R5 |
| $R_{OH}$ | R6 |
| $R_{CLOH}$ | R3 |
| $R_{DAC}$ | R21 |
| $R_{OFFSET}$ | R22 |
| $R_{CS}$ | R23 |

Without IMVP, the $R_{OH}$ (R6) and $R_{HYS}$ (R1) resistors set the hysteresis voltage via the following equation:

6) $$V_{HYS} := 2 \cdot V_{REF} \cdot \frac{R_{OH}}{R_{HYS}}$$

The factor of 2 is due to the fact that half of the total hysteresis occurs above the DC set point, half below, per Figure 1. Because output ripple is fed back to CMPREF via the R5/R21 divider, the uncorrected output ripple is increased. We correct for this later when selecting R1.

The no load offset in a non-IMVP converter is set by R6 and R22. The zero load voltage is:

7) $$V_{NL} := V_{DAC} \cdot \left(1 + \frac{R_{OH}}{R_{OFFSET}}\right)$$

As in the case of the hysteresis resistor, IMVP requires an adjustment of the offset resistor value because at zero current, the current drawn by the offset resistor divider is mirrored into the R5/R21 divider, and increases the offset just as it increases the ripple. R22 is calculated by solving equation 4) for $I_{OUT}$ = 0A.

8) $$R_{OFF} := \frac{R_{OH} + \frac{V_{NL} \cdot R_{DAC}}{V_{DAC}}}{\frac{V_{NL}}{V_{DAC}} - 1}$$

To disable the no-load positive offset, leave R22 unpopulated. Negative offsets are also possible — contact Semtech Applications Engineering for details.

The current sense resistor, $R_{CS}$ (R23), $R_{DAC}$ resistor (R21), and $R_{CORE}$ (R5) set the IMVP gain. $V_{IMVP}$ is a function of current, and is subtracted from the zero current output voltage.

9) $$V_{IMVP} := I_{OUT} \cdot R_{CS} \cdot \left(1 + \frac{R_{DAC}}{R_{CORE}}\right)$$

Note that the SC1406G regulates to the "+" side of R23; as a result, the minimum load dependent drop is Iout x R23. In addition, the ripple voltage across R23 provides a minimum input to the hysteretic comparator, so the SC1406G works well with very low ESR capacitors.

The constant-current type of over current protection is provided via R23, $R_{CLOH}$ (R3), and $R_{CLSET}$ (R2). Current limiting will cycle from $I_{CLMAX}$ to $I_{CLMIN}$ until the load becomes less than $I_{CLMAX}$:

10) $$I_{CLMIN} := 2 \cdot V_{REF} \cdot \frac{R_{CLOH}}{R_{CLSET} \cdot R_{CS}}$$

11) $$I_{CLMAX} := 3 \cdot V_{REF} \cdot \frac{R_{CLOH}}{R_{CLSET} \cdot R_{CS}}$$

Design Example – SC1406G:

We can use the above equations to design a mobile voltage regulator circuit to meet the requirements of the Intel® 650/500MHz SpeedStep™ processor using values from the processor datasheet. This example is for reference only; your requirements, parts availability, and newer processors may require different component values. Contact Intel for the latest processor requirements. Note that in the calculations, results have been rounded to the nearest commonly available component value.

*Requirements:*

The critical processor requirements are:

1. $V_{CC650MAXDC}$ = 1.65V
2. $V_{CC650MINDC}$ = 1.485V
3. $V_{CC650MAXTRANS}$ = 1.715V
4. $V_{CC650MINTRANS}$ = 1.485V
5. $V_{CC500MAXDC}$ = 1.45V
6. $V_{CC500MINDC}$ = 1.25V
7. $V_{CC500MAXTRANS}$ = 1.45V
8. $V_{CC500MINTRANS}$ = 1.25V
9. $I_{CC650MAX}$ = 13.6A
10. $I_{CC650SG}$ = 2.2A
11. $I_{CC500MAX}$ = 9.5A
12. $I_{CC500SG}$ = 1.7A
13. $dI_{CC}/dt$ = 1400A/mS (at the processor. Local decoupling reduces the requirement at the regulator.)

The system requirements are to minimize the number of capacitors, and:

1. $V_{ADAPTERMAX}$ = 21V
2. $V_{BATTMIN}$ = 10V

*Basic Calculations:*

The 0.85% DAC output voltage accuracy accounts for an uncertainty of 14mV at the 1.60V setting. In addition, 20mV of resistive drop is expected in the power distribution from the current sense resistor to the processor. A footnote in the processor specification reads that the long-term voltage should never exceed 1.65V. As a result, the nominal value of the no-load voltage [V (0)] should be set accordingly.

A. $V_{NL} := V_{CC650MAXDC} - V_{TOL}$ $V_{NL} = 1.636\,V$

The full-load voltage (V (fl)) is set similarly, including tolerance and DC drop.

B. $V_{FL} := V_{CC650MINDC} + V_{TOL} + V_{DIST}$ $V_{FL} = 1.519\,V$

The regulator is to be designed with 40mV of output ripple, so the effective IMVP voltage drop ($V_{IMVP}$) is:

C. $V_{IMVP} := V_{NL} - V_{FL} - \frac{V_{RIPPLE}}{2}$ $V_{IMVP} = 0.098\,V$

*Output Inductor and Capacitor Selection:*

Output capacitance and ESR values are a function of transient requirements and output inductor value. The following figure illustrates the response of a hysteretic converter to a positive transient:

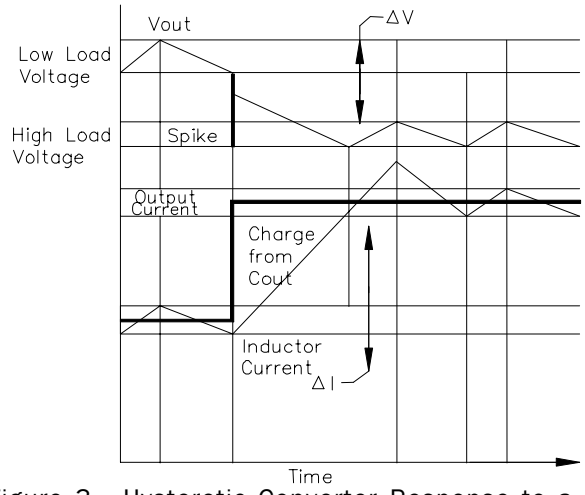



Figure 3 - Hysteretic Converter Response to a Positive Transient

In a hysteretic converter with adaptive voltage positioning, like the SC1406, two conditions determine if you meet the positive transient requirements:

D. $V_{IMVP} \geq (I_{CC650MAX} - I_{CC650SG}) \cdot ESR$

E. $V_{IMVP} \geq deltaV(C_{OUT})$

The first condition is easy to see — if the ESR is too high, the transient response will fail.

In the second condition, because the hysteretic converter responds in < 100ns, the capacitor does not droop very far before the inductor current starts ramping up. (This is not true of control schemes where time constants in the error amplifier cause delays.) Once the inductor current starts to rise, the increasing DV of the capacitor is offset by reduced DV from the ESR, so DV is constant. If the DV due to the charge taken from the capacitor before the inductor current reaches the load current (see the shaded area above) is less than $V_{IMVP}$, then the transient response will pass.

The maximum ESR requirement is:

F. $ESR_{MAX} := \frac{V_{IMVP}}{(I_{CC650MAX} - I_{CC650SG})}$

$ESR_{MAX} = 8.579 \times 10^{-3}\,\Omega$

For the second condition, we need to know the inductor value, which is a function of the highest desired switching frequency. The maximum frequency occurs at the highest input voltage. As a reasonable compromise between efficiency and component size, a maximum switching frequency of 300kHz is desired.

Rearranging equation 1), we select the minimum inductor value.

G. $L_{MIN} := d_{MIN} \cdot \frac{(V_{INMAX} - V_{DAC}) \cdot (ESR_{MAX} + R_{CS})}{F_S \cdot V_{RIPPLE}}$

$L_{MIN} = 1.426 \times 10^{-6}\,H$

This value of inductance is required up to maximum load. Inductors with a "swinging choke" characteristic, where the zero current value of inductance is much less than the full load current inductance can be used, as long as the above restriction is met. A value of 1.5uH is used to allow tolerances. Then, the worst-case (low input voltage) response time (the time for the current to reach the new transient value) is:

H. $dT := \frac{L_{MIN} \cdot (I_{CC650MAX} - I_{CC650SG})}{V_{INMIN} - V_{DAC}}$

$dT = 1.936 \times 10^{-6}\,s$

Add ~100ns for the SC1405/06 response. Since the shaded area is triangular, the total charge taken out of the capacitor = (DI ? Dt) / 2. Q = C ? DV = (DI ? Dt) / 2, therefore;

I. $C_{MINP} := \frac{(I_{CC650MAX} - I_{CC650SG}) \cdot (dT + 100 \cdot 10^{-9} \cdot sec)}{2 \cdot V_{IMVP}}$

$C = 1.186 \times 10^{-4}\,F$

This condition applies only to the positive transient. For negative load steps, the capacitance also has to be large enough to absorb the energy in the inductance. Since:

J. $C_{MINN} := L_{MIN} \cdot \frac{\left(I_{CC650MAX}^{2} - I_{CC650SG}^{2}\right)}{\left(V_{CC650MAXTRANS}^{2} - V_{FL}^{2}\right)}$

$C_{MINN} = 4.045 \times 10^{-4}\,F$

Using Panasonic SP-Caps, the EEFUE0E221R is 220uF at 2.5V with 15mW ESR. Two are sufficient to meet ESR requirements, but three are required to meet the capacitance requirement, when tolerances are considered. The Sanyo POSCAP 4TPC150 is a 150uF capacitor with a maximum ESR specification of 45mW; six are required to meet the ESR requirement. The resulting 900mF exceeds the capacitance requirement.

*Other Component Selection:*

As a compromise between current sensing accuracy, efficiency, and availability, a current sense resistor of 3mW is used. The power dissipation is $I^2xR$, or 555mW, so choose a 1W or larger resistor for design margin.

The connections to CMP, CMPREF, CL, and CLREF (pins 25 through 28) are two differential pairs connected to the current sense resistor. In order to cancel out common-mode noise, resistor pairs R3-R4 and R5-R6 should be equal. For the time being, assume R3=R4=R5=R6=1kW. These values may be adjusted later if required.

The current limit is a function of peak current and should be set at about 125% of the peak to allow for some overshoot of inductor current during transients. For L=1.5uH, and F=300kHz:

K. $I_{PEAK} := I_{CC650MAX} + \frac{(V_{INMAX} - V_{DAC}) \cdot d_{MIN}}{2 \cdot L_{MIN} \cdot F_S}$

$I_{PEAK} = 15.327\,A$

So, set the current limit at approximately 18.5A. Using equation 10):

L. $I_{CLMAX} := I_{PEAK} \cdot 1.25$ $I_{CLMAX} = 19.159\,A$

M. $R_{CLSET} := \frac{3 \cdot V_{REF} \cdot R_{CLOH}}{R_{CS} \cdot I_{CLMAX}}$

$R_{CLSET} = 8.873 \times 10^{4}\,\Omega$

Using equation 6) we calculate $R_{DAC}$:

N. $R_{DAC} := \frac{(V_{IMVP} - I_{CC650MAX} \cdot R_{CS}) \cdot R_{CORE}}{I_{CC650MAX} \cdot R_{CS}}$

$R_{DAC} = 1.397 \times 10^{3}\,\Omega$

The offset resistor, R22, is calculated from equation 8):

O. $R_{OFF} := \frac{R_{OH} + \frac{V_{NL} \cdot R_{DAC}}{V_{DAC}}}{\left(\frac{V_{NL}}{V_{DAC}} - 1\right)}$

$R_{OFF} = 1.068 \times 10^{5}\,\Omega$

Equation 5) is used to calculate R1 by calculating a new value of $V_{HYS}$ which accounts for the IMVP and offset dividers, and then plugging the resulting value into equation 3).

P. $V_{HYS} := V_{RIPPLE} \cdot (R_{CORE} \cdot R_{OFF} - R_{OH} \cdot R_{DAC}) \cdot \frac{\left[ESR + R_{CS} \cdot R_{CORE} \cdot \frac{(R_{OFF} + R_{OH})}{R_{CORE} \cdot R_{OFF} - R_{DAC} \cdot R_{OH}}\right]}{[2 \cdot ESR \cdot R_{CORE} \cdot (R_{OFF} + R_{OH})]}$

$V_{HYS} = 0.027\,V$

Q. $R_{HYS} := 2 \cdot \frac{V_{REF} \cdot R_{OH}}{V_{HYS}}$

$R_{HYS} = 1.281 \times 10^{5}\,\Omega$

The 55nS maximum delay from CO to the turn-off of the high-side driver will result in somewhat larger than calculated ripple, especially at high line, high ESR, and low inductor values. For the example, the increase in output ripple is about 6mV. R1 can be adjusted for this, if desired.

Once the design is complete, rerun the calculations for 1.35V to be sure the low voltage requirements are being met.

Several small capacitors are required for signal filtering. Use SMT ceramic capacitors with an X7R or better temperature coefficient. C0G is preferred.

C6 and C7, which filter the output voltage feedback, are sized to provide filtering beyond the fifth harmonic of the fundamental. The R5/R6 and C5/C6 components are balanced differential pairs that effectively filter both common-mode and differential noise sources that are troublesome in any high-performance switching converter:

$$\text{R.}\quad C6_{MAX} := \frac{1}{2 \cdot \Pi \cdot R_{CORE} \cdot F_S \cdot 5}$$

$$C6_{MAX} = 1.061 \times 10^{-10}\ \text{F}$$

Occasionally, due to layout-dependent noise on the CMP pin, the value of C6 and C7 must be increased. If multiple high frequency pulses are seen on the CO pin (pin 23), then additional capacitance is required. An additional capacitor is tied from the CO pin to the CMPREF pin to provide AC hysteresis during switching, and also helps to eliminate multiple pulses. Use a 1pF NPO capacitor for this purpose.

C5 is sized similarly, using R3 and R4. Since the current-limit comparator does not affect the normal operation of the converter, the frequency requirement is only to the second harmonic, so as not to attenuate the fundamental.

$$\text{S.}\quad C5_{MAX} := \frac{1}{2 \cdot \Pi \cdot (R_{CORE} + R_{BAL}) \cdot F_S \cdot 2}$$

$$C5_{MAX} = 1.326 \times 10^{-10}\ \text{F}$$

The DAC output requires a similar 1nF, X7R or C0G capacitor (C9) for high frequency noise filtering.

*Powering the SC1406:*

Vcc to the SC1406 can be either 5V, or 3.3V +/- 10%. 3.3V is recommended for lower power consumption, and because the UVLO function of the SC1406G provides protection for LDO outputs. Filter Vcc with an RC network; R18 should be 10W, C8, 0.1uF or greater.

Linear Regulator Design:

The SC1406G includes two linear regulator controllers, preset to 1.5V ($V_{I/O}$) and 2.5V ($V_{CLK}$), and sized to drive PNP pass elements sized for the required currents: 2.5A peak @ 1.5V, and 150mA peak @ 2.5V.

PNP regulators are somewhat harder to stabilize than NPN regulators. They require low source impedance, with input decoupling <0.5 inches from the emitter of the pass element; one capacitor suffices if the pass elements are close enough together. The size of capacitor required varies according to the impedance back to the 3.3V source. If the bulk decoupling is within two inches, and the 3.3V is distributed using a trace of at least 1 inch in width, then a 22mF capacitor is sufficient. Otherwise, use at least 100mF. PNP regulators generally require some ESR in the output capacitors for stability purposes, but excess ESR can also create problems. The allowable range of output capacitor and ESR values, based on simulation and testing is shown in Figure 4 for the 1.5V output and Figure 5 for the 2.5V output.

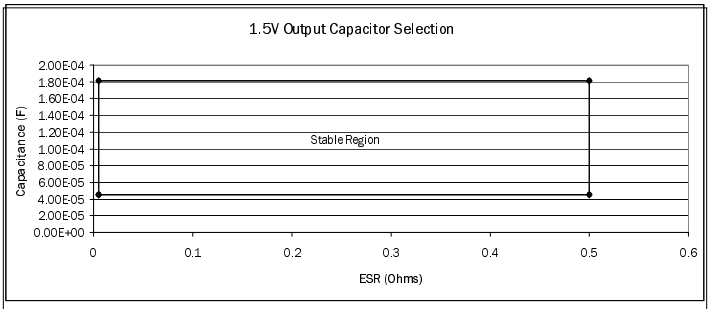



Figure 4 - Recommended output C and ESR values (1.5V output)

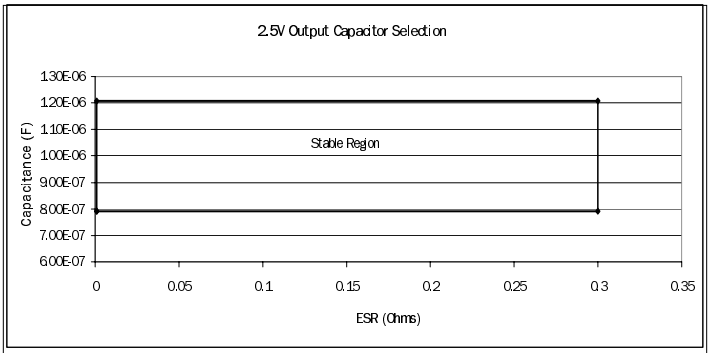



Figure 5 - Recommended output C and ESR values (2.5V output)

Pass Elements:

The last thing to consider is the pass elements themselves. The drivers are sized to provide peak output current with a minimum beta of 50. The MMBT4403 is one choice for the 2.5V pass element, and the MJD45H11 for the 1.5V output, although there are many acceptable choices. Do not use a Darlington transistor; the high gain and extra poles create stability problems, and defeat the beta current limiting scheme.

Soft-Start Design:

The three outputs have two soft-start controls, with the two linear regulators sharing one of them. The soft-start timing is controlled with a capacitor charged by a nominal 1mA current source. The soft-start period is the time to charge the soft-start capacitors to Vref (though the voltage eventually terminates near Vcc). The soft-start capacitor value is calculated for a 2ms nominal time by:

T. $$C_{SS} := \frac{I_{CSS} \cdot t_{SS}}{V_{REF}} \quad C_{SS} = 1.176 \times 10^{-9}\,F$$

The soft-start period for $V_{CORE}$ should be somewhat longer due to the higher power and larger amount of output capacitance to charge. Choosing 3ms results in C10=1800pF.

Low Battery Design:

The SC1406G provides a low-battery indication with a hysteresis current feature. That is, when the voltage at the LBIN pin is above the reference, the input bias current is very low. Once the threshold (a 1.225V bandgap) is reached and LBIN trips, a 0.6mA to 10mA current source must be overcome by the battery and divider before the converter is allowed to come on again. For the sample converter, assume $V_{TRIP}$ = 9.5V. Ignoring bias currents, and assuming R8=20kW.

U. $$V_{LBTRIP} := V_{LBREF} \cdot \frac{R8 + R9}{R8}$$

In the example schematic, R9 = 43kW to accommodate operation down to 4.5VDC. The rounded value gives a $V_{TRIPLO}$ of 9.62V. In order for LBIN to reset, the current source must be overpowered, so:

V. $$V_{TRIPHIMAX} := V_{LBREF} + R9 \cdot \left( 10 \cdot \mu A + \frac{V_{LBREF}}{R8} \right)$$

$$V_{TRIPHIMAX} = 10.986\,V$$

W. $$V_{TRIPHIMIN} := V_{LBREF} + R9 \cdot \left( 6 \cdot \mu A + \frac{V_{LBREF}}{R8} \right)$$

$$V_{TRIPHIMIN} = 10.438\,V$$

The hysteresis current, in this case provides a voltage hysteresis of 0.82V to 1.38V.

C10 provides noise filtering at the LBIN input. The 1nF value is intended to provide attenuation at the lowest frequency load of the battery. To disable this feature, tie LBIN (pin 17) to Vcc of the SC1406 through a resistor (10kW is a good nominal value).

Clamp Design:

The clamp circuit is an open-collector uni-directional level shifter capable of driving a 16mA load with a 5ns typical delay time. VCIN (pin 4) must be referenced to the $V_{IO}$ rail; VCOUT (pin 3) can be tied to either $V_{CLK}$ or $V_{CC}$, depending on the connection of the pull-up resistor. The clamp circuit has a dedicated reference, VCBYP (pin 5) that requires a 1.5nF capacitor for proper operation. The clamp circuit is not normally used in Pentium III mobile computers. To disable this function, tie VCIN to analog ground, with VCOUT and VCBYP open.

Other Features and Functions:

ENABLE is a 5V-safe CMOS input with an upper threshold voltage at 70% of Vcc and a lower threshold of 0.8V. It can be used in two different ways. One is to tie ENABLE to the PWRDY pin of the SC1405; this will bring both the SC1405 and SC1406 up properly even if ENABLE can be active before the system 5V supply is stable. Alternately, the ENABLE lines of both devices can be tied together.

CO is the clock output from the SC1406 to the SC1405. POWERGOOD is LO (inactive) whenever any of the following conditions is present:

1. Vcore is more than 10% higher or lower than its set-point,
2. Either soft-start pin is lower than its threshold
3. Vcc is below the UVLO threshold
4. LBIN is active

POWERGOOD is HI (active) when none of the above is true, as during normal operating conditions.

SC1405 Design Example:

The main function of SC1405 is to rapidly drive the power MOSFETs on and off on using a “break before make” algorithm to prevent cross conduction in the FETs.

*FET selection:*

The duty cycle (d) of the converter is a function of the input voltage. In most applications, where the converter runs directly from the battery, AC adapter, or even a regulated +5V source, d is always going to be much less than 50%. The low-side (or synchronous) FET, therefore, is conducting most of the time; further, because the diode clamps the voltage across the low-side FET, it switches with virtually zero voltage across it. The high-side (or control) FET conducts for a relatively small amount of time, but has to switch the entire voltage. Therefore, the control FET can have a relatively high $R_{DS(ON)}$, but needs to have low capacitive losses, and the synchronous FET needs to have a low $R_{DS(ON)}$, and can have higher capacitance. To accomplish this, one can use a single FET type, with two or more in parallel in the low-side, or one can use FET sets with individually optimized devices.

The current in the control FET is approximately:

X. $I_{Q3RMS} := I_{CC650MAX} \cdot \sqrt{d_{MAX}}$

$I_{Q3RMS} = 5.44\,A$

This current also should be used to size input capacitors; the three input capacitors need a ripple current rating of 1.8A each, to meet this requirement. The synchronous FET should be sized for the full output current. Since the drive is derived from 5V, both FETs should be sized using $R_{DS(ON)}$ and current ratings for Vgs=4.5V.

Gate resistors are always recommended, and are required for the control FET and for multiple synchronous FETs (one resistor per gate). The value is dependent on FET selection and layout. Generally, start with 2.2W to 4.7W for R11 -13 to evaluate the circuit for EMI performance and Miller (gate to drain) capacitance effects. Increasing the high-side FET gate resistor value will lessen both problems, but at the expense of higher switching losses.

Miller capacitance in the low-side FET can cause it to turn ON as the high-side FET turns on. It acts as a charge-pump capacitor to couple the current from the fast dV/dt on the drain into the gate. The voltage that appears on the low-side FET gate is:

Y. $V_G := Z_{DRIVE} \cdot \frac{C_{DS}}{C_{GS}} \cdot \frac{dV}{dT}$

If the voltage is sufficient to conduct significant current, then efficiency is poor, and in extreme cases, the devices can be damaged. For a given FET, Cgs is fixed, so one possible solution is to slow down dV/dt; another is to reduce Zdrive. Reducing Zdrive is primarily a function of layout and FET selection, since the internal Rg of the FET can be on the order of 10W. The SC1405 driver is typically 1W; so, given the short (10-20ns) dt, Zdrive can be dominated by trace inductance. For long gate drive traces, this inductance can resonate with the gate capacitance; in this case, a few ohms of gate resistance can damp the circuit and actually reduce the peak gate voltage. However, the best practice is to locate the SC1405 as near as possible to the low-side FET and run wide traces to the gate.

Other potential solutions are to choose FETs with a low Cds/Cgs ratio, low Rg, or add a capacitor from the low-side gate drive to ground to externally lower the Cds/Cgs ratio.

*Charge Pump Design:*

The high-side drive circuit is tied to the source of the FET at DRN (pin 12) and rides along the switching (phase) node rather than being hard referenced to ground. The drive circuit makes use of this switching action to "pump" charge from the 5V source up to the BST pin (pin 14) to drive the control FET. When Q4 and Q5 are ON, C17 is charged through D1 to nearly 5V; when Q4 and Q5 turn off, this voltage is available to turn Q3 on. C17 rides along with the source, maintaining the drive level.

The charge pump capacitor needs to be low impedance, with a value at least 100 times the gate capacitance it has to charge. Ceramic capacitors are recommended. Schottky diodes are recommended for D1. Wide traces are also required for the charge pump traces.

In very low power situations, the low side drive may be disabled via use of the SMOD pin (pin 5). This pin effectively prevents reverse current from flowing in the inductor, so the inductor current becomes discontinuous and the operating frequency is reduced. The reduced losses related to circulating current and faster switching need to be compared with the additional loss in using the diode rather than the synchronous rectifier to determine whether it improves low load efficiency in the system application. In addition, the system must supply the SMOD signal at the appropriate time.

*Phase Node Design:*

The phase node is one of the most critical nodes in the converter design, and must be treated with care. When neither Q3 nor Q4 is on, the inductor current flows through D2. D2 should be a Schottky diode with a forward voltage at the peak inductor current less than the forward voltage of the parasitic diode of the FET, to keep it from conducting, and improving efficiency. Holding the gate of Q4 low until the phase node reaches 1V for a high to low transition provides shoot-through protection. For a low to high transition, the high-side driver is held off by an internal 20ns delay. This period may be extended using C15, connected to pin 6, to provide an additional delay of approximately 1ns/pF. Size C15 to provide dead time for the worst-case drive conditions given the choice of control FET and gate drive resistor.

The phase node voltage at DRN (pin 12) must not go below -2V; very short (<25nS) pulses to -5V can be tolerated. Excessive negative transients may result in double pulsing of the gate drive, and in severe cases, device damage.

The phase node, since it switches at very high rates of speed, is generally the largest source of common-mode noise in the converter circuit. For this reason, it should be kept to a minimum size consistent with its connectivity and current carrying requirements. Occasionally, a snubber network (R17/C18) is required to dampen parasitic ringing on the phase node caused by parasitic inductance and capacitance excited by the switching. One approach to snubber design is to record the frequency and amplitude of ringing before the snubber, then add pure capacitance until the frequency is reduced, then adding resistance until the required damping is achieved.

*Additional Functions:*

The SC1405 also provides two voltage protection functions:

1 A drive voltage under voltage lockout (UVLO) with output on PRDY, pin 7
2 An output over voltage protection (OVP) using input OVPS, pin 1

UVLO shuts off the drivers when Vcc is less than 4.4Vdc; in this condition, PRDY is driven low, and may be used to disable the SC1406G as well. OVP is implemented using a resistive divider to a 1.20V +/- 55mV reference. In order to keep the voltage within the 2.1V processor specification:

Z. $$V_{REFMAX} := V_{OVPMAX} \frac{R14}{R14 + R15}$$

With R14=10kW, R15=6.65kW. Solving this equation for the minimum trip voltage yields $V_{OVPMIN}$=1.906V. Since this is only ~250mV from the zero load voltage, a noise filter capacitor (C14) is required, and should be chosen that the R14||C15 time constant is longer than the minimum switching period. The OVP input has very fast response, so C14 needs to be located directly at the pin, and the length of the OVP trace should be minimized.. Ground pin 1 to disable OVP.

A logic output signal DPSPDR (pin11) mirrors BG when SMOD is HI; it is HI when SMOD is LO.

*Additional notes:*

Since the SC1405 puts out large, sharp pulses, decoupling and grounding are very important. The Vcc decoupling capacitor, C16 should be at least 1uF ceramic, and located right at the chip with the "+" terminal connected directly to Vcc (pin 8) and the "–" terminal connected directly to PGND (pin 10). Note that the SC1405 connects to both the power and analog grounds. Grounding is described in the following section.

LAYOUT GUIDELINES:

As with any high-speed switching converter, the area of high current loops needs to be minimized. The two major loops are (referring to Figure 2):

1. From the input capacitors, through Q3, L1, and C19 – C24, returning through PGND;
2. From Q4/Q5 through L1 and C19 – C24, returning through PGND.

Secondary loops are in the gate drive circuitry:

1. From C17 through the SC1405, R13 and Q3, returning through the phase node.
2. From C16 through the SC1405, R11/R12 and Q4/Q5, returning through PGND.

In addition:

1. Separate the noisy and quiet areas of the circuit. A significant benefit of the controller/driver architecture is that the control circuit does not have to coexist in an environment of thousands of volts and amps per microsecond.
2. Place the SC1405 so as to reduce the trace length to the synchronous rectifier(s).
3. Place the current-sense resistor as close as possible to the output capacitors; inductance from the voltage sense point to ground results in extra output ripple.
4. Connections and routing of the differential pairs are critical. The first three items are essential; the others are suggested for additional guidance.
   a. Run the traces as close together as possible.
   b. Use minimum width traces to reduce capacitive coupling.
   c. Run a single pair as far as possible; split them at the resistors as close as possible to the SC1406; put the filter capacitors as close as possible to the device.
   d. In noisy environments, use a guard ring (ground trace around the differential pair). Tie the ring to ground every 2-4 cm.
   e. Run the traces in a quiet layer; use the minimum number of vias.
5. Minimize the area of the switching node and any other high-speed nodes.
6. Layout the protection circuitry (OVP, LBIN) keeping noise in mind:
   a. Minimize the length and area of traces to the pins.
   b. Put the noise filter capacitor next to the pin.

## Sample Layout

The following shows the layout of the SpeedStep™ VRM. Additional data, including electronic format schematic and layout files, as well as experienced layout assistance is available from your local Semtech field applications engineer.

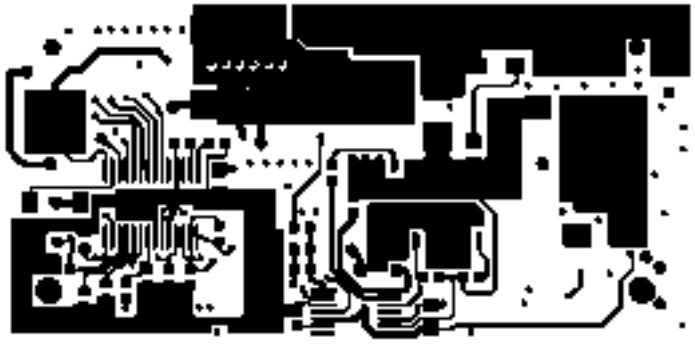


Figure 6 - PowerStep™ VRM — Top Layer

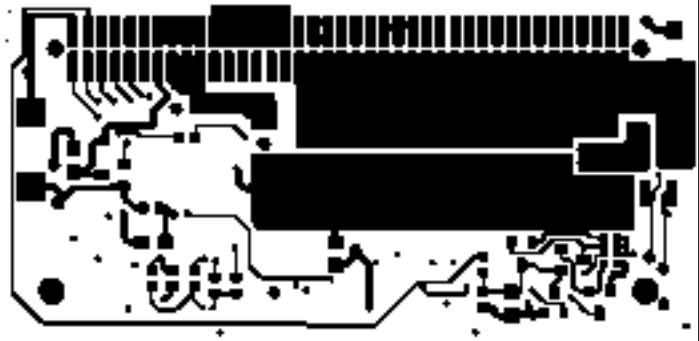


Figure 7 - PowerStep™ VRM - Bottom Layer

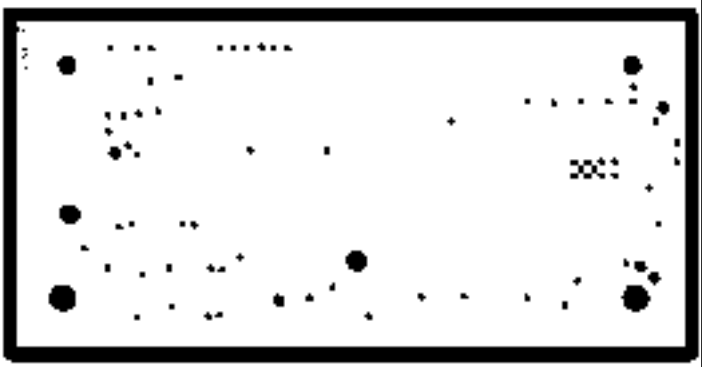


Figure 8 - PowerStep™ VRM - Ground Layer

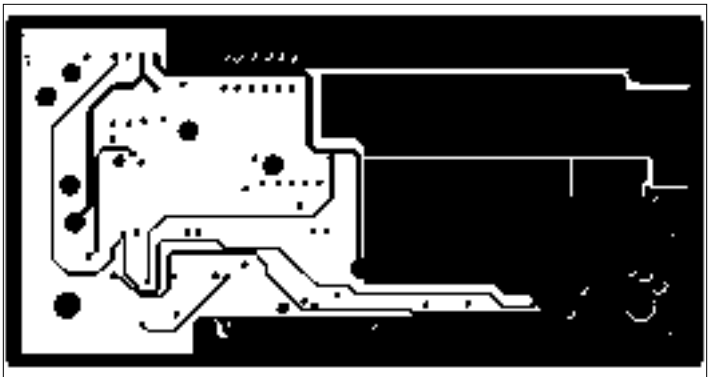


Figure 9 - PowerStep™ VRM - Inner Layer

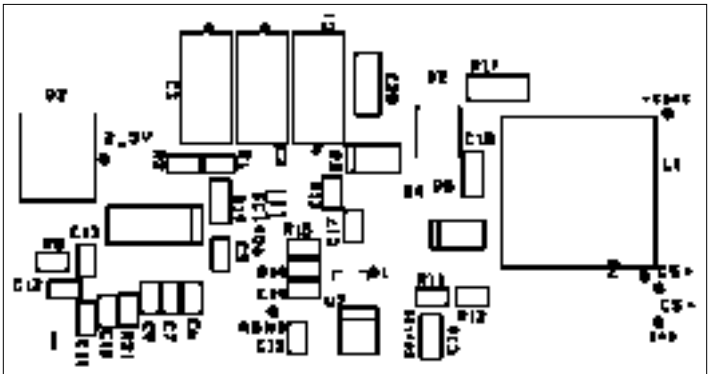


Figure 10 - PowerStep™ VRM - Top Silkscreen

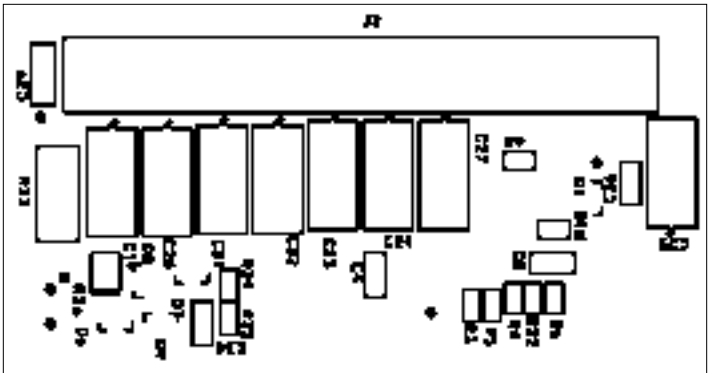


Figure 11 - PowerStep™ VRM - Bottom Silkscreen

## Bill of Materials

Critical Component Recommendations:

A list of components used successfully in this and/or similar circuits appears below. Listing does not necessarily indicate available supply.

Table 2 - Critical Components Supplies

| Component | Manufacturers | Series or Part Number |
|---|---|---|
| Output Inductor | Panasonic<br>Sumida | Series PCC-N6, PCC-S1<br>Series CDEP134 (H) |
| Output Capacitors | Kernet<br>Panasonic<br>Sanyo | KO Cap, Series T520<br>SP Cap, Series CB<br>POSCAP, Series TPx |
| Power MOSFETS | International Rectifier<br>Vishay/Siliconis | IRF7809A, IRF7811A<br>Si4874, Si4884 |
| Current Sense Resistor | IRC<br>Panasonic<br>Vishay/Dale | Series LRF3W, LRF2010<br>Series ERJM-1WST<br>Series WSL, WSR |

Table 3 - Critical Supplier Contacts

| COMPANY | CONTACT |
|---|---|
| International Rectifier | Web: http://www.irf.com/product-info/<br>Phone: (310) 726-8000 |
| IRC | Web: http://www.irctt.com/<br>Phone: (888) 472-4376 |
| Kernet | Web: http://www.kernet.com/<br>Phone: (864) 963-6300 |
| Panasonic | Web: http://www.panasonic.com/pic/ecg/<br>Phone: (201) 348-7522 |
| Sanyo | Web: http://www.sanyovideo.com/<br>Phone: (619) 661-6835 |
| Sumida | Web: http://www.sumida.com/<br>Phone: (847) 956-0666 |
| TDK | Web: http://www.component.tdk.com/components/components.html<br>Phone: (847) 390-4373 |
| Vishay/Dale | Web: http://www.vishay.com/brands/dale<br>Phone: (402) 564-3131 |
| Vishay/Siliconix | Web: http://www.vishay.com/brands/siliconix/<br>Phone: (800) 554-5565 |

CONCLUSION:

The SC1405/06G PowerStep™ chip set provides a complete, optimized solution for the power requirements of Intel's SpeedStep™ processors. Evaluation kits and application notes are available. For further information, please see the Semtech website (www.semtech.com), or contact your local Semtech field applications engineer.

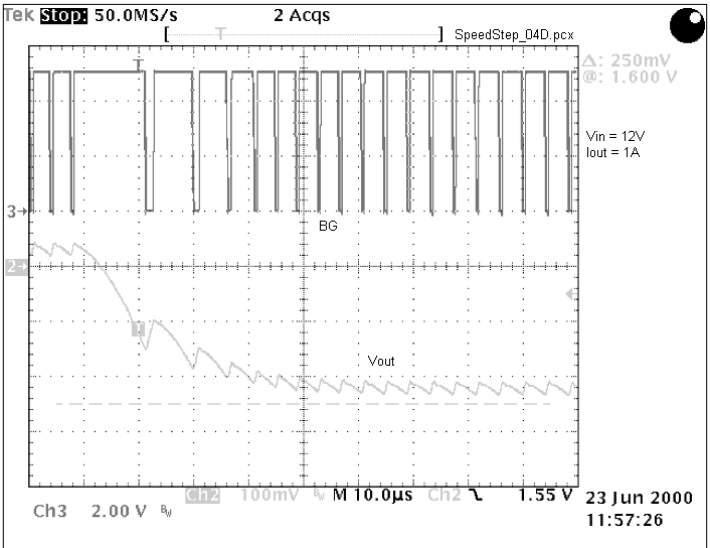



Figure 12 - SpeedStep Transition, 1.60V to 1.35V

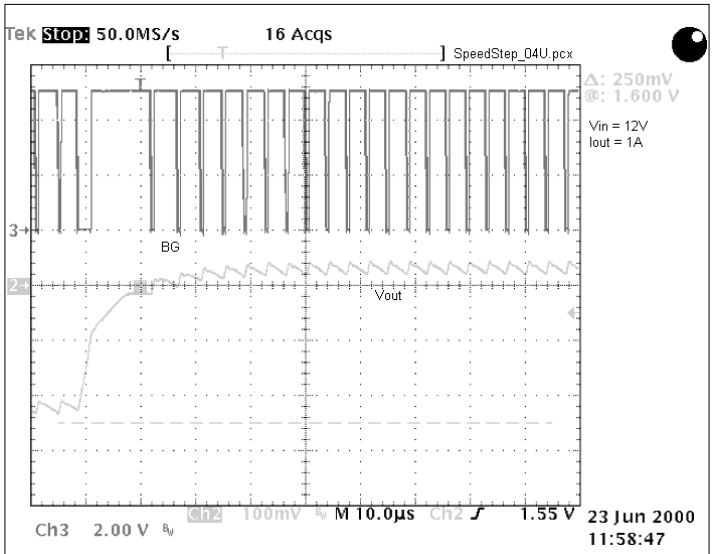



Figure 13 - SpeedStep Transition, 1.35V to 1.60V

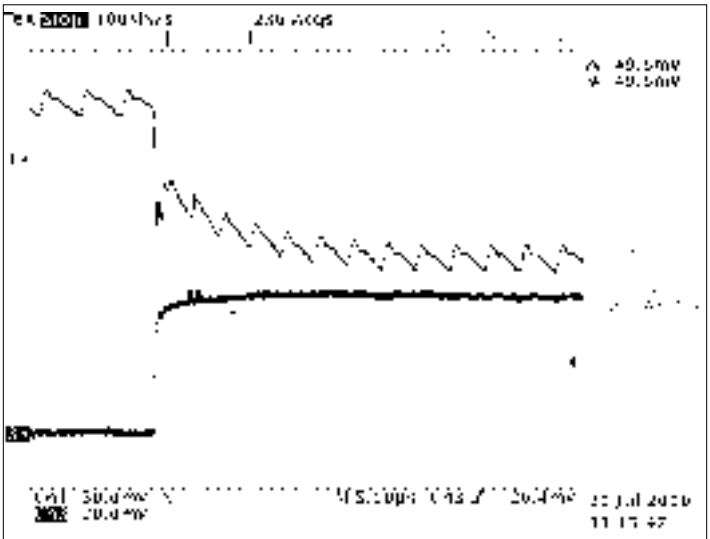


Figure 14 - 0A to 12A Transient Load Response

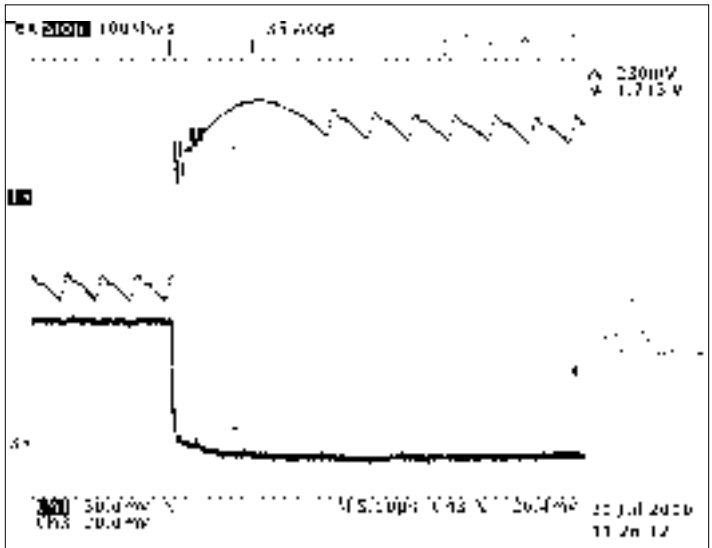


Figure 15 - 12A to 0A Transient Load Response

Output Ripple Voltage @ $V_{IN}$ = 6.0V

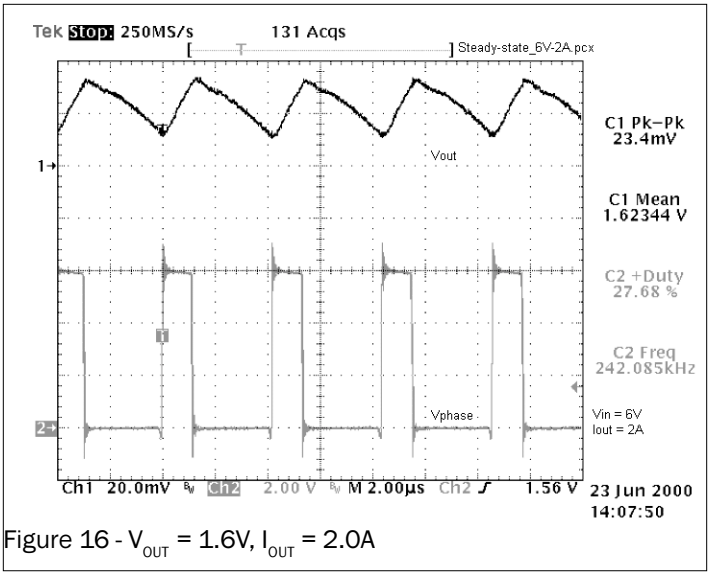



Figure 16 - $V_{OUT}$ = 1.6V, $I_{OUT}$ = 2.0A

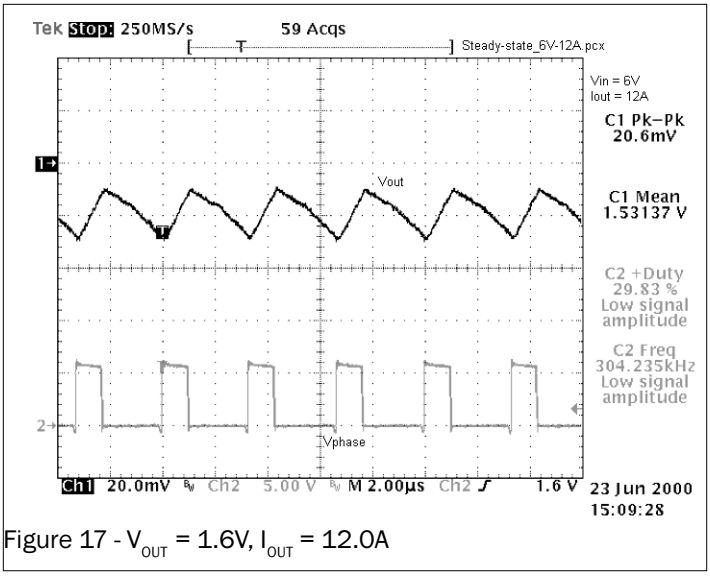



Figure 17 - $V_{OUT}$ = 1.6V, $I_{OUT}$ = 12.0A

Output Ripple Voltage @ $V_{IN}$ = 18V

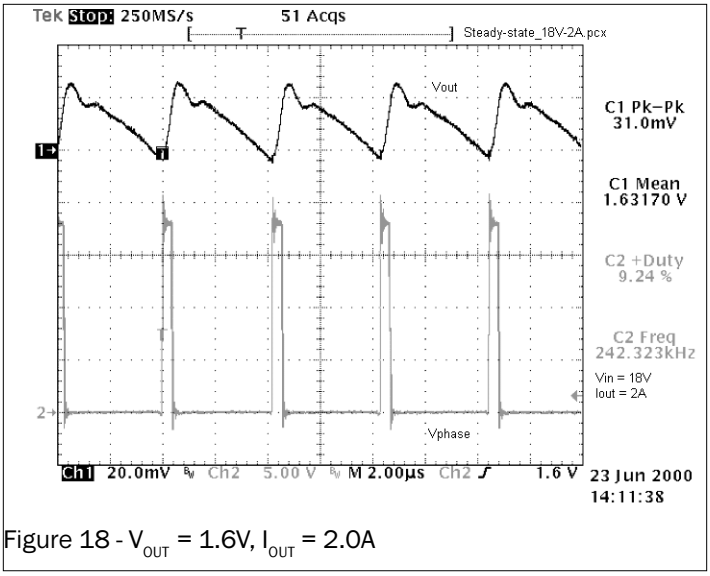



Figure 18 - $V_{OUT}$ = 1.6V, $I_{OUT}$ = 2.0A

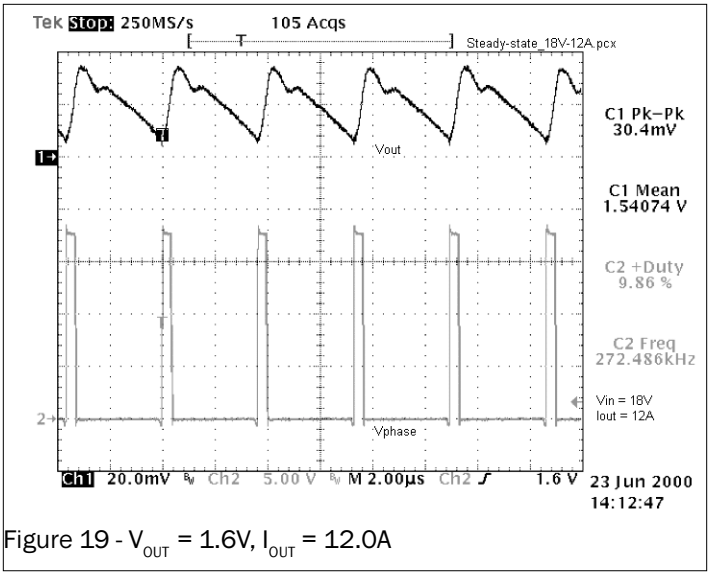



Figure 19 - $V_{OUT}$ = 1.6V, $I_{OUT}$ = 12.0A

Load Regulation & Efficiency

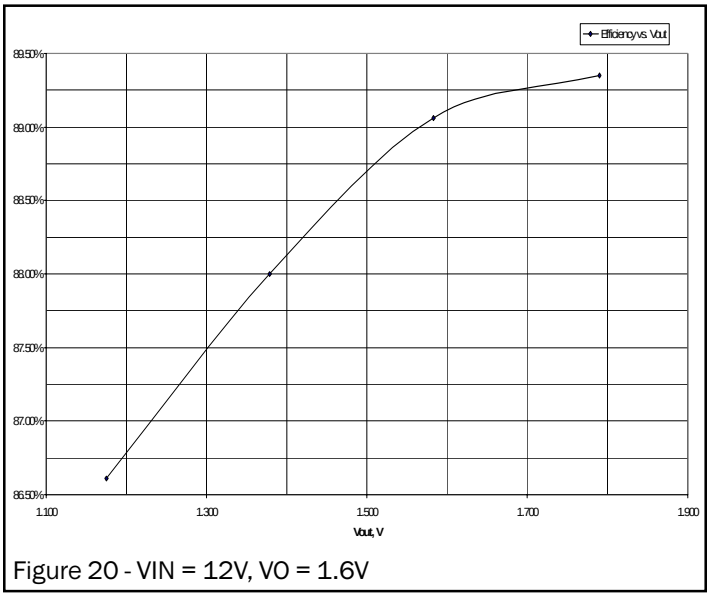



Figure 20 - VIN = 12V, VO = 1.6V

Line Regulation & Efficiency

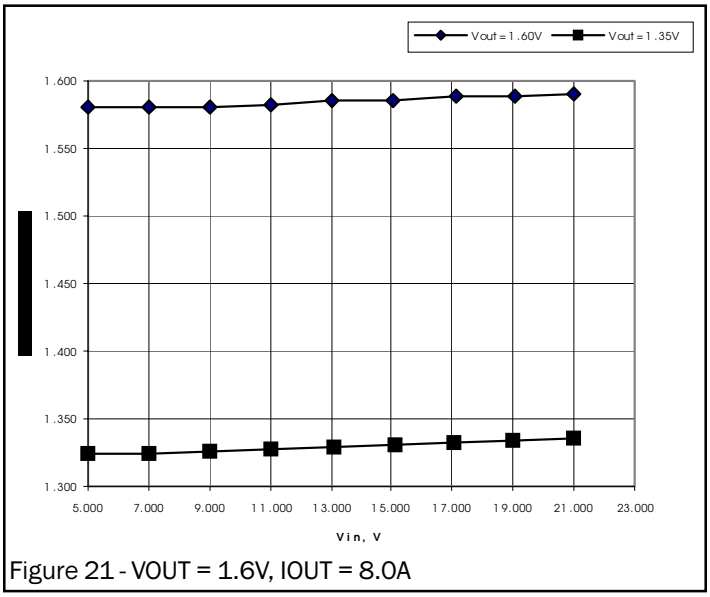



Figure 21 - VOUT = 1.6V, IOUT = 8.0A

Efficiency vs Output Voltage

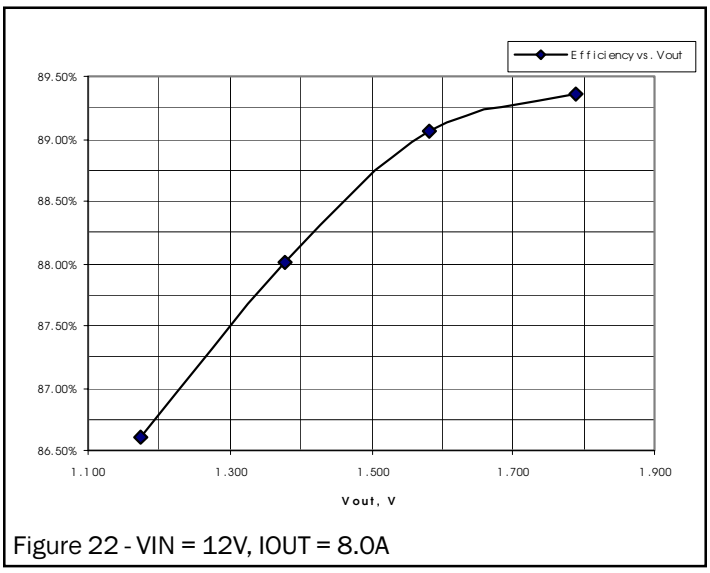



Figure 22 - VIN = 12V, IOUT = 8.0A

Efficiency vs Input Voltage

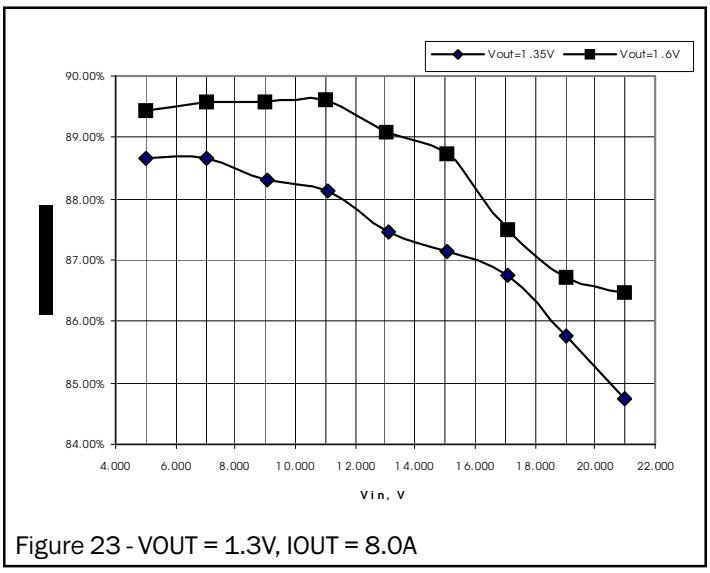



Figure 23 - VOUT = 1.3V, IOUT = 8.0A

Supply Current vs $V_{IN}$, Temperature @ UVLO mode

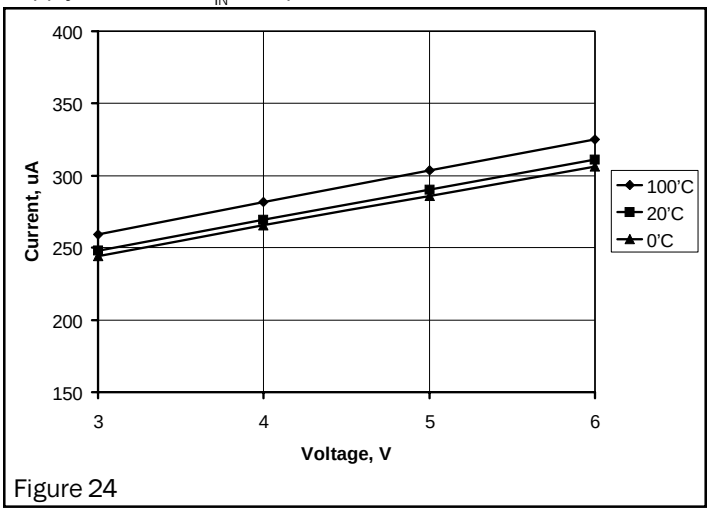



Figure 24

Supply Current vs $V_{IN}$. Temperature @ Operating mode

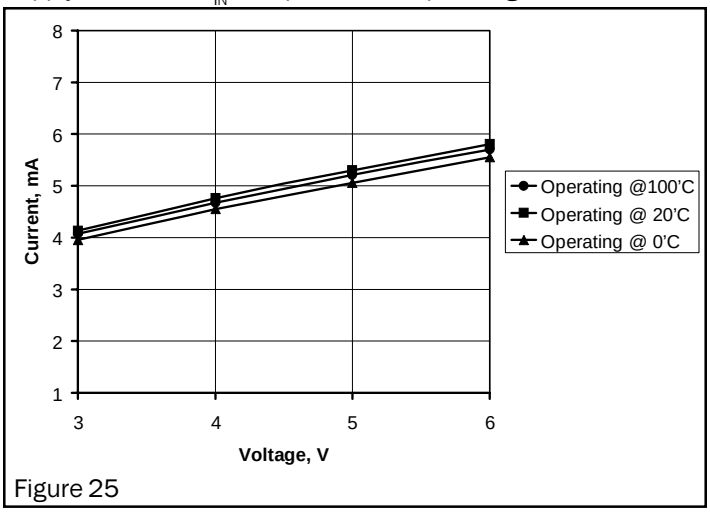



Figure 25

DAC Output vs Temperature

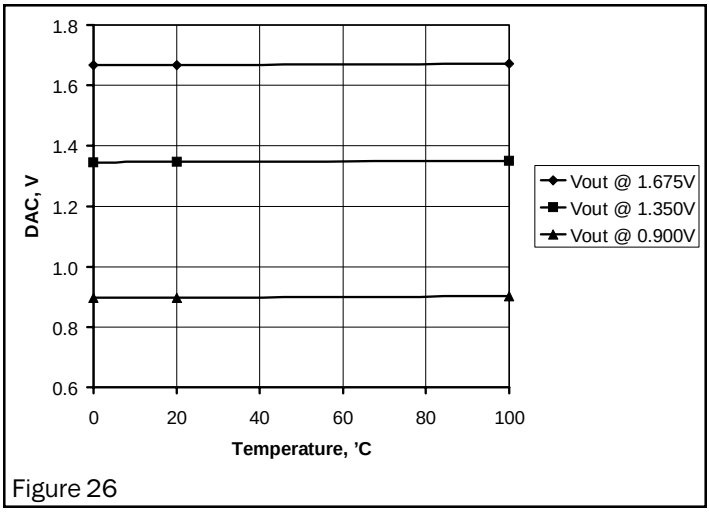



Figure 26

Power Good Threshold vs Temperature

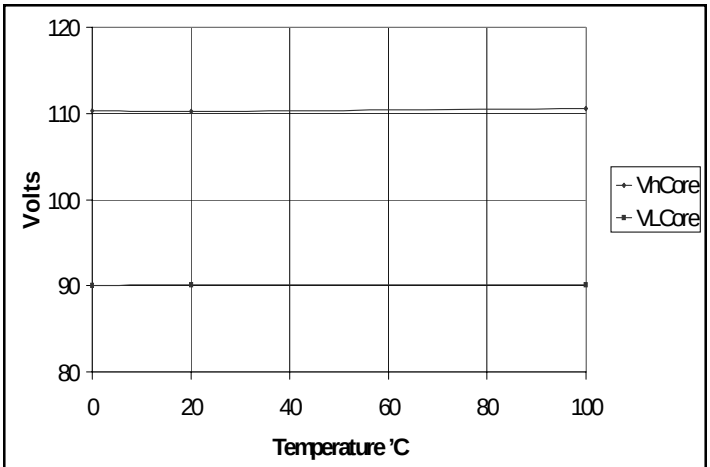



Figure 27

Hysteresis Setting Current vs Temperature

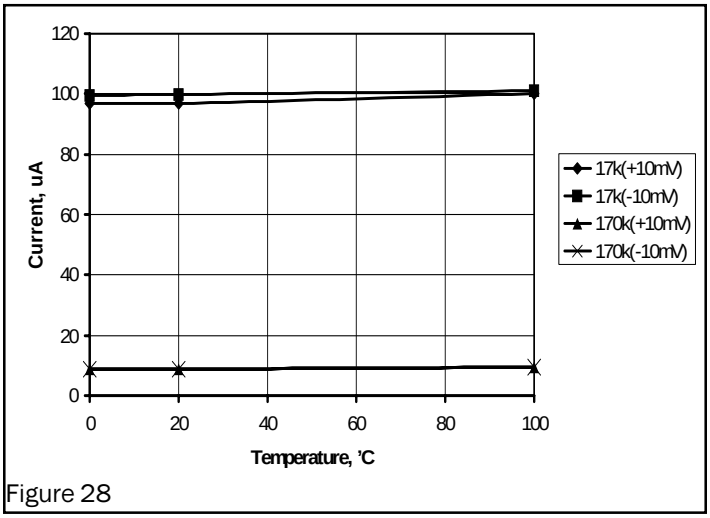



Figure 28

Current Limit Threshold vs Temperature

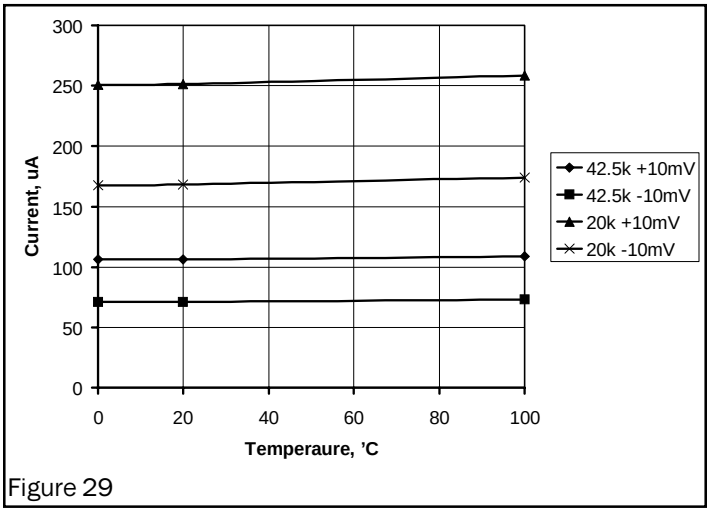



Figure 29

Core Soft-Start Current vs Temperature

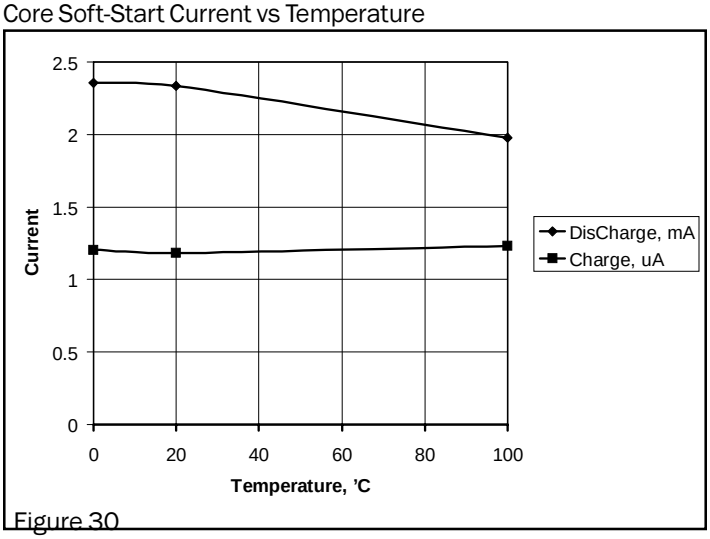



Figure 30

LDOs Soft-Start Current vs Temperature

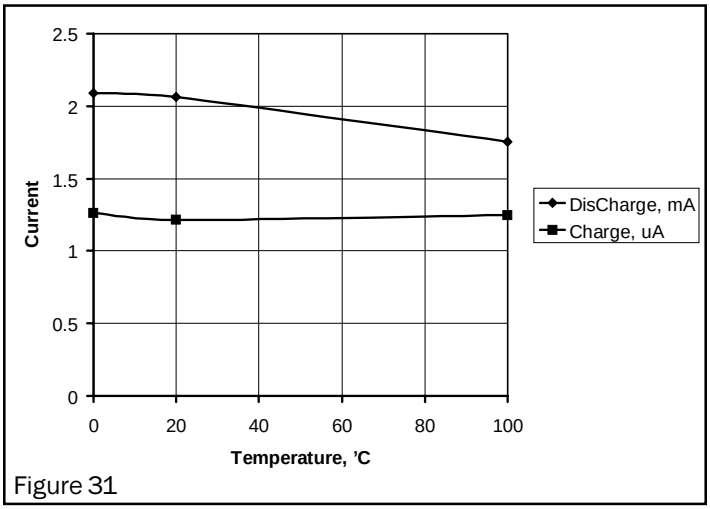



Figure 31

Low Battery Monitor Threshold vs Temperature

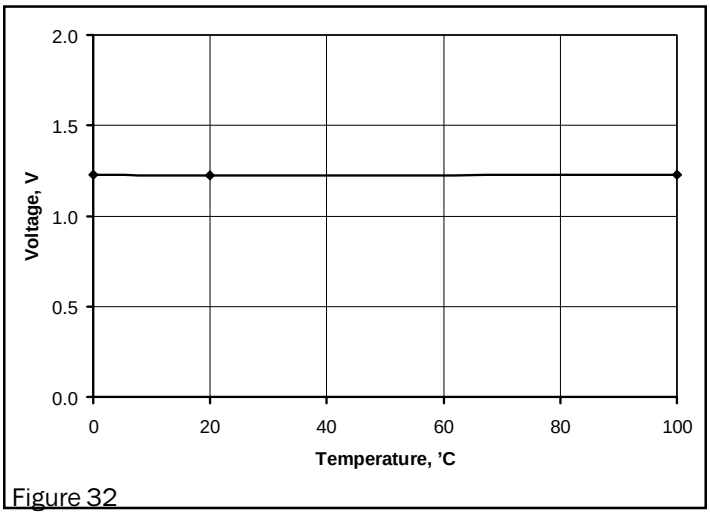



Figure 32

LDOs Drive Currents vs Temperature

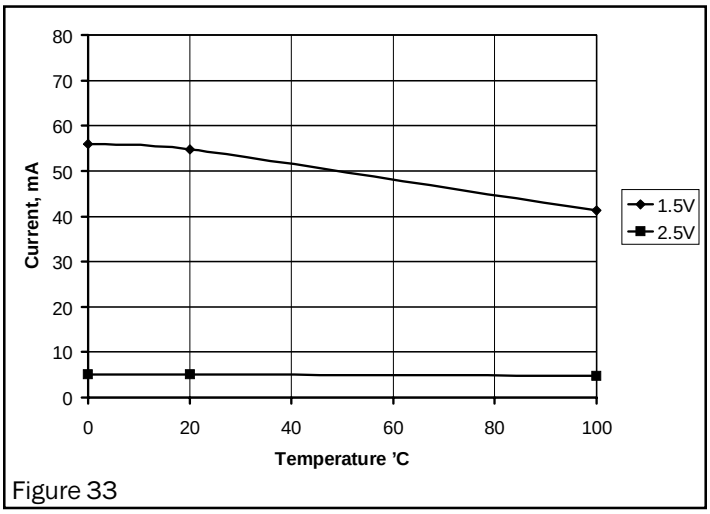



Figure 33

I/O LDO Load Regulation-Normalized for 1A

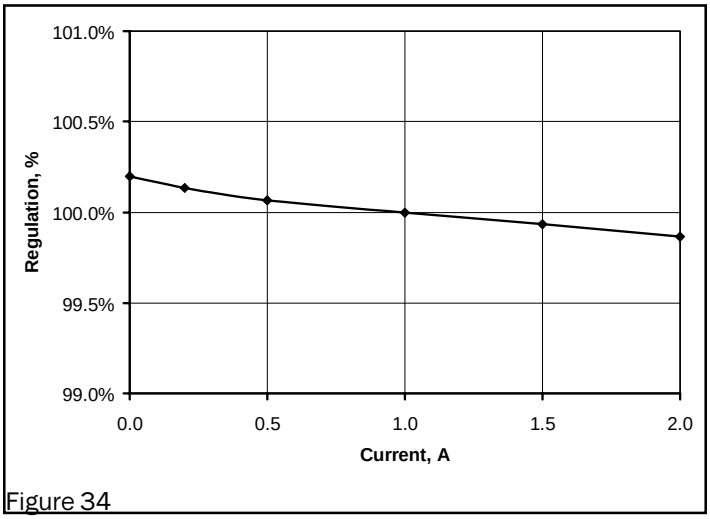



Figure 34

CLK LDO Load Regulation-Normalized for 100mA

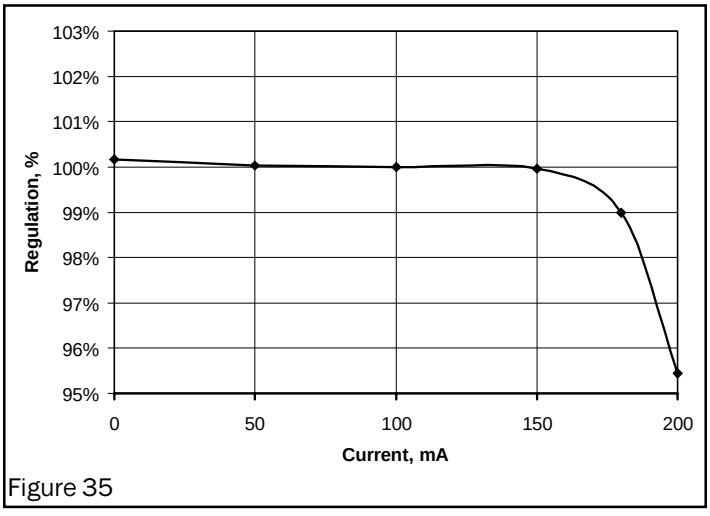
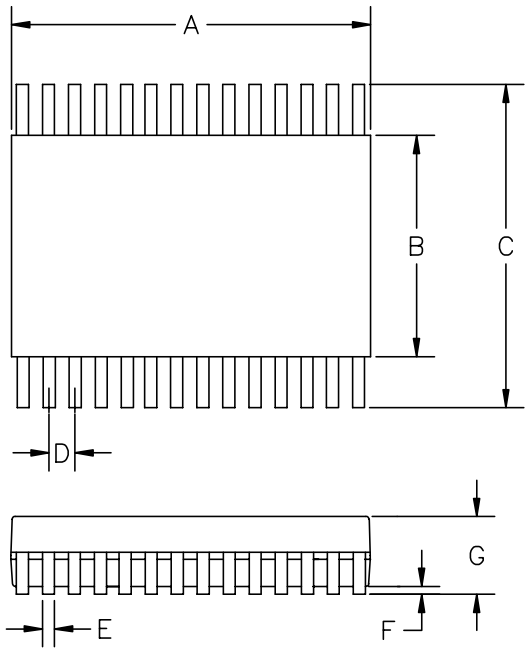
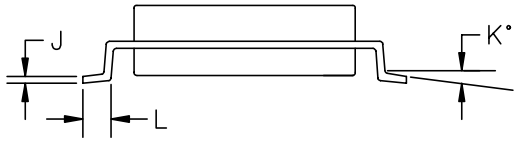



Figure 35

## Outline Drawing - TSSOP-28




| DIM | INCHES | | MM | | NOTE |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | .3779 | .3858 | 9.60 | 9.80 | |
| B | .169 | .177 | 4.30 | 4.50 | |
| C | .252 BSC | | 6.40 BSC | | — |
| D | .026 BSC | | .65 BSC | | — |
| E | .007 | .012 | .19 | .30 | — |
| F | .0015 | .0080 | .05 | .15 | — |
| G | | .078 | | 1.20 | — |
| J | .0040 | .0100 | .09 | .20 | — |
| K | 0° | 8° | 0° | 8° | — |
| L | .022 | .037 | .45 | .75 | — |

JEDEC MO-153AE

NOTE: DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

## Contact Information

Semtech Corporation
Power Management Products Division
652 Mitchell Rd., Newbury Park, CA 91320
Phone: (805)498-2111 FAX (805)498-3804

ECN 00-1128