



GENERAL DESCRIPTION

The SC1001 series product is a poly gate CMOS integrated circuit which is designed to drive an electroluminescence Lamp (EL) to light. It supplies three pins for trigger input: one is active at low (ALM) and other two are active at high (TG&FLSH). 3 seconds display delay function is implemented by internal divider. Only ALM and TG will generate 3seconds delay but FLSH not. The switching and EL driving frequency is decided by an intimae RC oscillator. The driving capability for IND output and frequency for EL output are different options, the detail information shown in the OPTION LIST.

SC1001 series product can be widely used in the back light of digital watch, analogy watch, calculator etc.

FUNCTIONS

- Single 3V or 1.5V battery operation.
- DC to AC conversion.
- Built-in RC oscillator.
- Built-in delay function.
- Three independent trigger inputs: ALM (L) makes EL display for 3 second delay.
TG (H) makes EL display for 3 second delay.
FLSH (H) makes EL flash companied with the pluse from FLSH without any delay.
(See Tining Diagram)

FEATURES

- Economical solution for EL display.
- CMOS process and low power consumption.
- No external component needed for delay function.
- Min. external components application.

COIL OPTION LIST FOR SC1001

VDD (V)	COIL		EL AREA (cm squ.)	EL VOLTAGE (V)	COLOUR
	MIN	OHM			
3.0	3	37	1.5×2.5	140	Blue
	2	14	1.5×2.5	165	Blue
	2	14	2.5×2.5	130	Blue
	1	11	2.5×2.5	160	Blue
	1	11	3.5×6.0	110	Green
1.5	2	14	1.5×2.5	105	Blue
	1	11	1.5×2.5	120	Blue
	1	11	1.1×2.3	160	Green- Blue
	1	11	2.5×2.5	100	Green



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits
Power supply voltage range	VDD-VSS	-0.3V to +5.0V
Input voltage range	Vin	Vss-0.3 to VDD+0.3
Operating temperature range	TA	0 to +60°C
Storage temperature range	Tstg	-40 to +70°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, Ta=25°C, VDD=3.0V, Vss=0V

Characteristics	Symbol	Min	Typ	Max	Unit	Test conditions
Operating voltage range	VDD	1.3	3.0	4.5	V	-
Standard current	IDD	-	0.1	1	uA	*on load
IND output source current	IOH1	1.3	2.6	-	mA	VOH=0.8V
EL output source current	IOH2	1.0	2.2	-	mA	VOH=0.8V
IND output sink current	IOL1	10	20	-	mA	VOH=0.8V
EL output sink current	IOL2	2.0	4.0	-	mA	VOH=0.8V
Oscillator stating voltage	VSTP	1.3	-	-	V	-
Oscillator frequency	***FOSC	400	500	670	KHz	VDD=3.0V

Unless otherwise specified, Ta=25°C, VDD=1.5V, Vss=0V

Characteristics	Symbol	Min	Typ	Max	Unit	Test conditions
Operating voltage range	VDD	1.3	1.5	4.5	V	-
Standard current	IDD	-	0.1	1	uA	*on load
IND output source current	IOH1	0.3	0.5	-	mA	VOH=0.8V
EL output source current	IOH2	0.2	0.4	-	mA	VOH=0.8V
IND output sink current	IOL1	3.0	10	-	mA	VOH=0.8V
EL output sink current	IOL2	0.3	0.8	-	mA	VOH=0.8V
Oscillator stating voltage	VSTP	1.3	-	-	V	-
Oscillator frequency	***FOSC	400	500	670	KHz	VDD=1.5V

Note: * refers to EL & IND open, all trigger input open.

**The Max. IND source current IOH1 can be enlarged to 4 ma by mask option. The value in the above table refers to SC10013 OPTION. Others can be found in the OPTION LIST.

***The parameter Fosc in the above table refers to option SC10013. others can be found in the OPTION LIST.

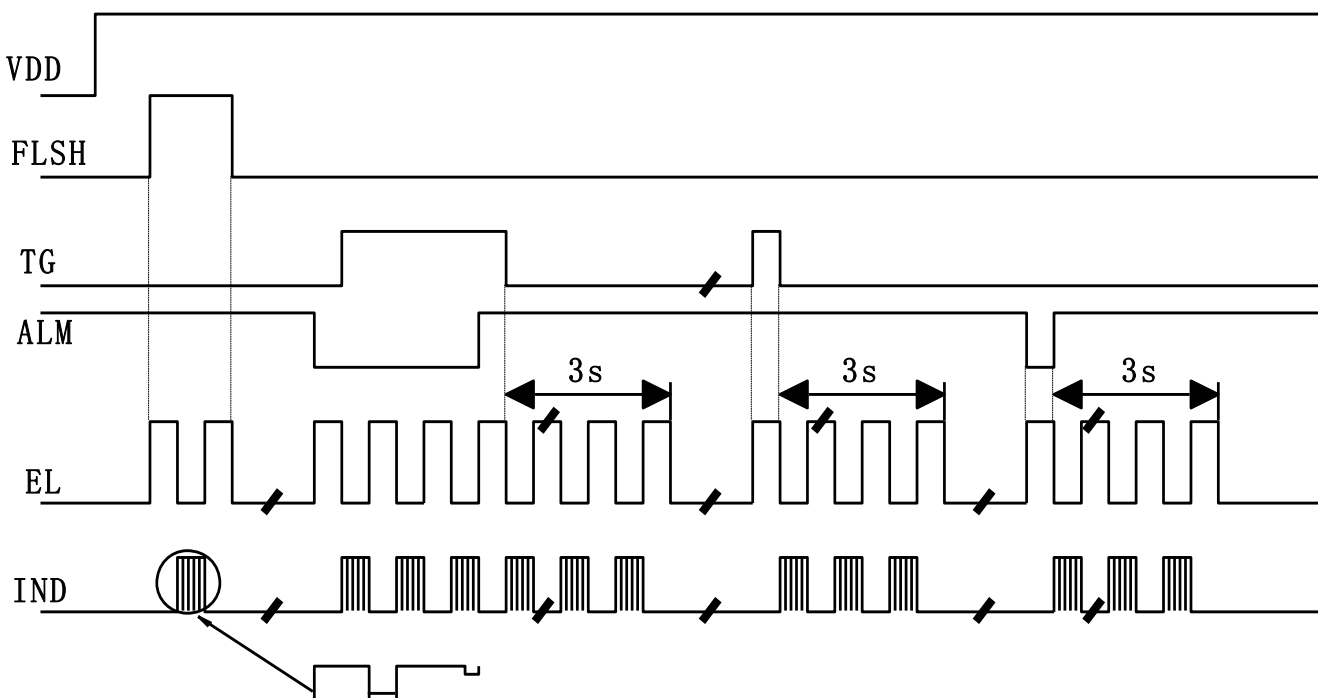


PAD DIAGRAM



PAD No	PAD Name	X	Y
1	IND	-315.50	183.50
2	EL	-315.50	53.50
3	VDD	-315.50	-76.50
4	TG	-315.50	-206.50
5	VSS	315.45	-206.50
6	ALM	315.45	-76.50
7	FLSH	315.45	55.60
8	TST2	315.45	185.60
9	TST1	156.45	204.85

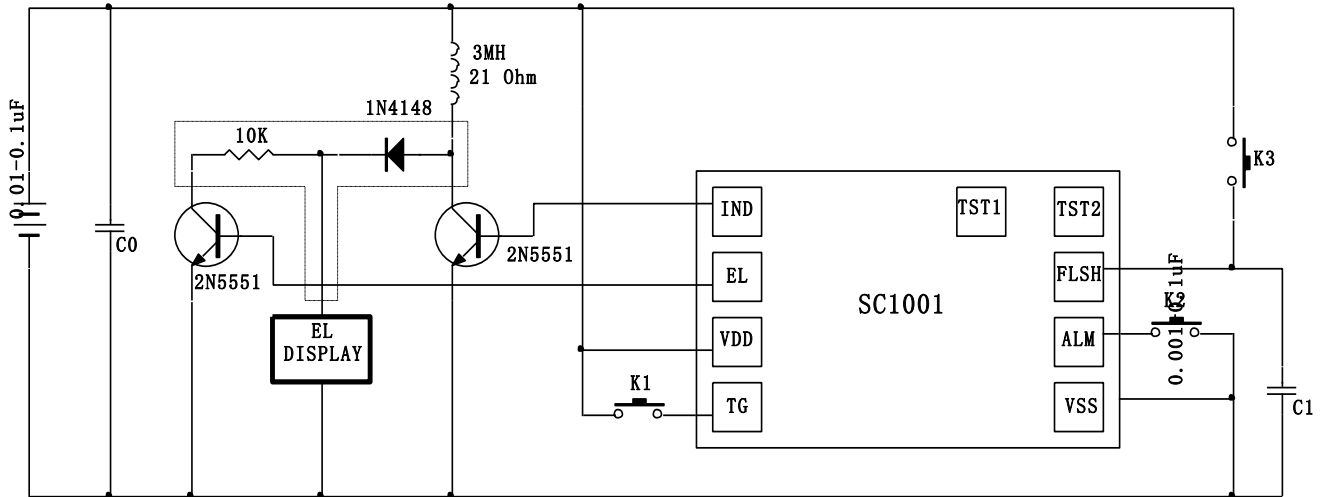
TIMING DIAGRAM





TYPICAL APPLICATION CIRCUIT

(Selection of K1, K2 AND K3 for different applications)



Note: 1. Substrate is connector to VDD.

2. The wires connected to TG and ALM cannot cross the lines Inside the black dot line box. Furthermore, these wires should be separated from the lines Inside the black dot line box by Vss or Vdd.

3. The capacitor C1 can be connected to Vss or Vdd.

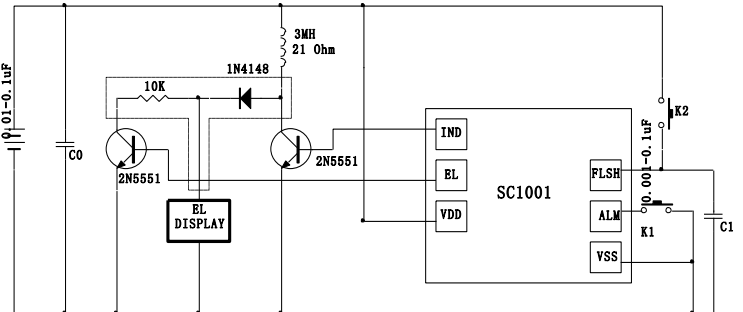
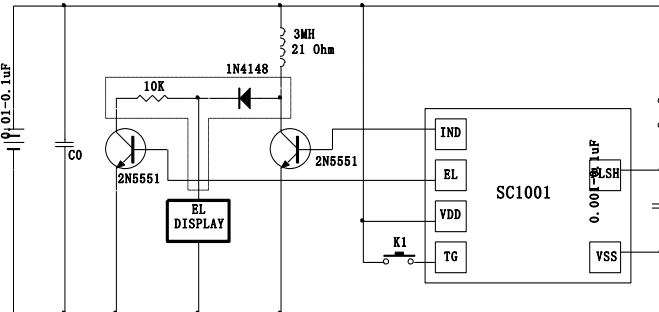
4. During the watch application, the two wires connected to crystal are better to be surrounded by Vss or Vdd, and they are the farer the better away from the wire connected to EL.

5. The items 2, 3, 4 are very Important for PCB layout. The above items are also applied to the following applications (A-H) and will not be rementioned again.

ALL KINDS OF APPLICATION CIRCUIT

A. Application with 3 Second Delay using Vdd Trigger & without Delay using FLSH Trigger

B. Application with 3 Second Delay using Vss Trigger & without Delay using FLSH Trigger



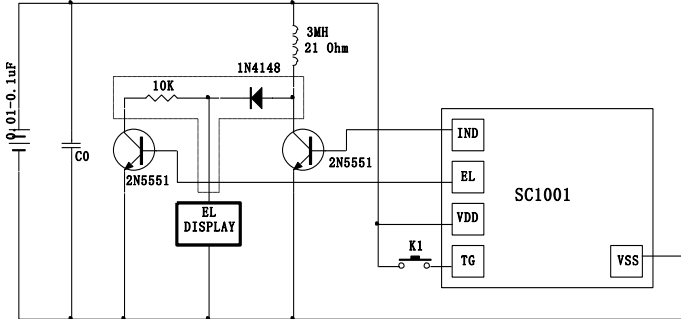
Note: Substrate is connector to VDD



SC1001 (文件编号: S&CIC0549)

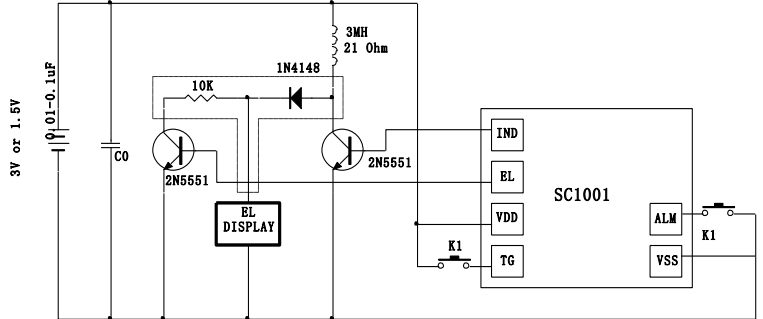
EL LAMP DRIVER IC

C. Application with 3 second delay using Vdd trigger

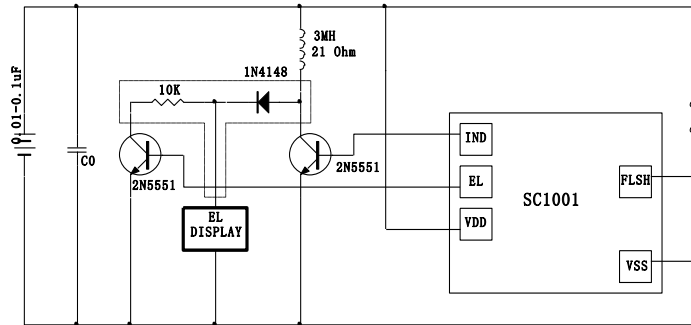


Note: Substrate is connector to VDD

D. Application with 3 second delay using Vss trigger

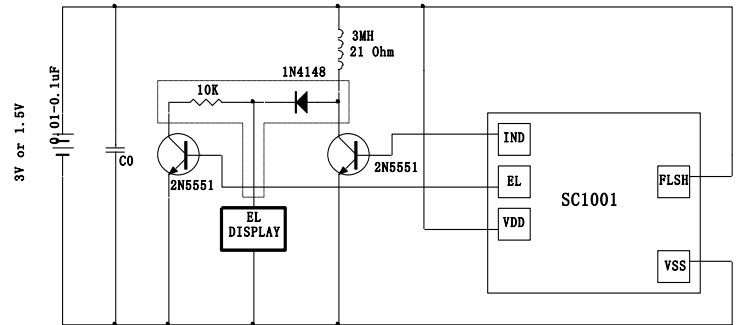


E. Application without delay using FLSH trigger



Note: Substrate is connector to VDD

F. Application without delay using Power Button



Note: 1. Substrate is connector to VDD.

2. L* and R* are adjustable to enlarge the driving capability.