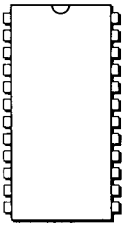
FEATURES

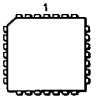
- ☐ All modulators, demodulators, and filters with compromise equalizers on chip
- ☐ Call progress mode, tone generators for DTMF, V.22 guard and calling tones
- ☐ On-chip hybrid
- ☐ Bell 212A and CCITT V.22 compatible; includes notch filter
- ☐ SC11014 supports V.21
- ☐ Serial control interface
- ☐ Programmable audio port
- ☐ All loopback diagnostics

24-PIN DIP PACKAGE



SC11004CN
SC11014CN

28-PIN PLCC PACKAGE



SC11004CV
SC11014CV

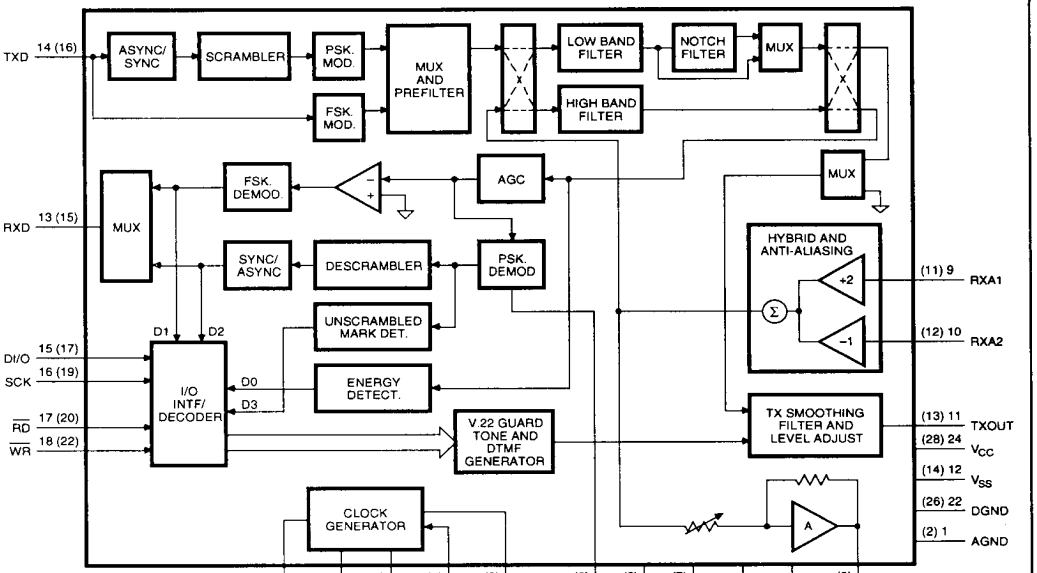
GENERAL DESCRIPTION

The SC11004 is a complete 300/1200 Bit Per Second (bps) modem. All signal processing functions needed for a full duplex, 300/1200 bps, Bell 103/212A or V.22 compatible modem, including the FSK and PSK modulators and demodulators and high-band and low-band filters with compromise amplitude and group delay equalizers are integrated on a single chip.

Built with Sierra's proprietary CMOS process that allows analog and digital functions to be combined on the same chip, the SC11004 features call progress monitoring and DTMF generation and V.22 guard tones. A two-to-four wire hybrid is also included on chip, simplifying the interface to a data access arrangement (DAA). An external hybrid may also be used, if desired. The SC11004 also includes analog, digital, and remote digital loopback diagnostics for self testing. The SC11014 contains all of the features of the SC11004 and, in addition, supports V.21 operation.

With the addition of a digital controller, such as an 8-bit microcontroller and a DAA, a highly cost effective, integrated, intelligent modem can be built. When used with the Sierra SC11007 modem controller—an 8-bit processor combined with a UART—a complete Hayes command set compatible modem can be configured, occupying minimum board area. All that is needed for stand-alone applications is the SC11004/14 modem, the SC11008 controller, a DAA and an RS232-interface. They operate in synchronous or asynchronous mode and handle 8, 9, 10 or 11 bit words.

BLOCK DIAGRAM



NOTES: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINS; NUMBERS IN ( ) ARE PLCC PINS. PINS (1), (6), (10), (18), (21) & (23) ARE NOT CONNECTED.

(27) 23	(24) 20	(25) 21	(4) 3	(3) 2	(8) 6	(5) 4	(7) 5	8	19	(9) 7
CKOUT	XTAL1	XTAL2	TXCK1	TXCK0	RXCK	TEST 1	TEST 2	NC	NC	AUDIO OUT

This Material Copyrighted By Its Respective Manufacturer

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1 (2)	AGND	Analog ground
2 (3)	TXCK0	Transmitter clock output. In high speed, synchronous, internal mode, this output supplies a 1200 Hz clock to the DTE.
3 (4)	TXCK1	In high speed, synchronous, external mode, this pin is an input for receiving a 1200 Hz clock from the DTE.
4 (5) 5 (7)	TEST 1, TEST 2	Used by Sierra for testing. Make no connection to these pins—they MUST be left floating.
6, (8)	RXCK	Receiver clock output. In high speed, synchronous mode, the modem supplies a 1200 Hz clock on this output.
7, (9)	Audio Out	Output of the hybrid is passed through a programmable attenuator and brought out on this pin. 4 levels of received signal can be programmed using the control codes listed in Table 1 (Page 8).
8,19 (1,6, 10,18,21,23)	NC	No Connect. These pins must be left floating. Do NOT ground these pins or tie them to V_{CC} or V_{SS}.
9 (11) 10 (12)	RXA1, RXA2	Received data carrier
11 (13)	TXOUT	Transmit data carrier output
12 (14)	V_{SS}	–5 V power supply
13 (15)	RXD	Receive data. The modem demodulates the received carrier and outputs data on the pin. A logic low level is space and a logic high level is mark. The controller can force the demodulator output to the mark state by sending the code 02.
14 (16)	TXD	Transmit data. Data on this input is modulated by the modem and output on TXOUT pin. A logic low is space and a logic high is mark.
15 (17)	D I/O	Data I/O pin. Data is shifted in serially when $\overline{WR}$ is low on rising edges of SCK clock. Data is transferred to a latch when $\overline{WR}$ goes high. Up to 7 data bits can be sent. Input codes are defined in Table 1. Data is read from the modem serially when $\overline{RD}$ is low, on rising edges of SCK clock. Up to 4 data bits can be read. Output codes are defined in Table 1 (Page 8).
16 (19)	SCK	Serial shift clock is applied to this pin. It is normally high until data is sent to or read from the modem.
17 (20)	$\overline{RD}$	Strobe output from controller for serially reading data from the modem.
18 (22)	$\overline{WR}$	Strobe output from the controller for shifting data to the modem.
20 (24) 21 (25)	XTAL1, XTAL2	Pins for connecting a 7.3728 MHz crystal. An external CMOS (+5 V) clock signal can be applied to the XTAL1 pin, with XTAL2 left open. If a TTL clock is used, it must be capacitively (100 pF) coupled into XTAL1.
22 (26)	DGND	Digital ground
23 (27)	CKOUT	Buffered crystal oscillator signal is output on this pin. It can drive one LS TTL load.
24 (28)	V_{CC}	+5 V power supply

Numbers in ( ) refer to 28-Pin PLCC Package.

This Material Copyrighted By Its Respective Manufacturer

FUNCTIONAL DESCRIPTION OF THE SC11004/14 MODEM

Major sections of the SC11004/14 modem are a transmitter, a receiver, low-band and high-band filters, a two-to-four wire hybrid, tone generators and interface logic. It also contains an energy detector that's used for detecting the carrier and call progress monitoring and an audio output for monitoring the line.

The SC11004/14 modem requires ±5 V and is available in a 24-pin DIP as well as a 28-lead plastic chip carrier with 'J' leads for surface mount applications. The transmitter section consists of an async/sync convertor, scrambler, PSK modulator and FSK modulator. In the high speed mode (1200 bps), the PSK modulator is connected to the filter. In the low speed mode (300 bps), the FSK modulator is connected to the filter.

Transmitter

Since data terminal and computers may not have the timing accuracy required for 1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync convertor accepts asynchronous serial data clocked at a rate between 1200 Hz + 1%, – 2.5%. It outputs serial data at a fixed rate of 1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync convertor is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first two stages of the shift register form the dibit that is applied to the PSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band centered at 2400 Hz or the low band, centered at 1200 Hz. A 1200 bps modem actually sends two bits at a time, called a dibit; dibits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

The dibit applied to the PSK modulator produces one of four differential phase shifts of the square wave carrier signal (1200 Hz or 2400 Hz) at the 600 Hz baud rate. The resultant waveform is passed through a wave shaping circuit that performs a raised cosine function (this is the shape factor called out in the CCITT V.22 spec, and it also meets the Bell 212A requirement for optimum transmission). The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on orignate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21 and 212A modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the Call Progress Monitoring mode, the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog

This Material Copyrighted By Its Respective Manufacturer

loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF or V.22 guard tones. It also provides a 3 dB per step programmable gain function to set the output level.

Receiver

The receiver section consists of an energy detector, AGC, PSK demodulator, FSK demodulator, descrambler, and sync/async convertor.

The received signal is routed through the appropriate band-pass filter and applied to both the energy detector and AGC circuit. The energy detector is based on a peak detection algorithm. It provides a detection within 17 to 24 ms. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels.

The AGC circuit is a programmable gain amplifier that covers a wide range. Output of the AGC amplifier is rectified and compared with two preset levels corresponding to desired high and low limits. Outputs of the comparators control an up/down counter such that the received signal is amplified to the desired level. Receive signal input range is 0 to –45 dBm measured at the chip.

The PSK demodulator uses a coherent demodulation technique. Output of the AGC amplifier is applied to a dual phase splitter that produces an in-phase and 90 degree out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by the recovered carrier. The baseband components are low-pass filtered to produce I and Q channel outputs. (In phase and Quadrature). The I and Q channel outputs are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. The signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled to produce the received dibit data. The recovered carrier for the demodulator is generated by another PLL which is controlled by the amplitude of the error signal formed by the difference of the I and Q outputs.

The descrambler is similar to the scrambler. The received dibit data is applied to the D input of a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with input data to produce received data.

In the asynchronous mode, data from the descrambler is applied to the sync/async convertor to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (over-speed data), these stop bits are reinserted. Underspeed data is passed essentially unchanged. Output of the sync/async convertor along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. The output of the AGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, this matching is provided by an external resistor connected between the RXA1 and RXA2 pins on the SC11004/14. The filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass anti-aliasing filter.

Internal Hybrid

The SC11004/14 internal hybrid, shown in Figure 1, is intended to simplify the phone line interface. In addition, there is a gain select feature to compensate for the loss in the line coupling transformer used in the DAA. By tying this pin to V_{SS}, ground or V_{DD}, compensation levels of 0, +2 or +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. With a 3 dB loss transformer for example, the energy detect on/off levels measured at the line will be in the range of –40/–45 dB rather than –43/–48 dB as specified at the chip. An external hybrid circuit, shown in Figure 2, can be used to overcome these losses and achieve maximum performance.

This Material Copyrighted By Its Respective Manufacturer

External Hybrid

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC110104/14 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. For example, if the TLC1, TLC0 level control codes are set to 0 and 1 respectively so as to obtain –9 dBm at the line, the chip actually puts out –3 dBm at the TXOUT pin (pin 11). Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired –9 dBm. In practice however there is impedance mismatch and a loss in the coupling transformer. Therefore it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain G_R and transmit gain G_T are set by the ratios of resistors R2, R1 and R6, R5 respectively (Figure 2).

The circuit can be analyzed as follows:

$$V_R = -\frac{R2}{R1}\left(V_{TR}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)V_y$$

$$V_y = -\frac{R6}{R5}V_x$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_Y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_Y = 2\,V_{TX}$,

$$V_R = -\frac{R2}{R1}\left(V_{TX}+V_{RX}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$

$$= -\frac{R2}{R1}\,V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) = \frac{R2}{R1}$$

Solving for R3/R4

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:
R1=20 kΩ, R2=27 kΩ, R3=13 kΩ, R4=5.1 kΩ, R5=20 kΩ and R6=27 kΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6 and capacitor C1 can be eliminated and point X connected to point Y in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The SC11004/14 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, RXA2 is connected to ground and the receive signal is connected to RXA1. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator and a V.22 guard tone generator. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and * and # keys. The V.22 guard tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50 kΩ is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation — no attenuation, 6 dB attenuation, 12 dB attenuation and squelch are provided through the ALC1, ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Crystal Oscillator

The SC11004/14 includes an inverting amplifier between pins 20 and 21 with an internal bias resistor to simplify the design of the crystal oscillator. The parallel resonant, 7.3728 MHz ±0.001% crystal, designed for a load capacitance of 20 pF, should be connected across pins 20 and 21. Two capacitors of typical values 27 pF from pin 20 to digital ground (DGND pin 22) and 47 pF from pin 21 to DGND should be connected. With the recommended crystal, Saronix, NYMPH, NYP073-20 and these capacitor values, a highly accurate and stable crystal oscillator can be designed. Since the carrier frequency must be within ±0.01% of the normal 1200/2400 Hz, it is important to measure the actual crystal oscillator frequency at CKOUT (pin 23) and adjust the external capacitors for a given circuit board layout, if necessary.

This Material Copyrighted By Its Respective Manufacturer

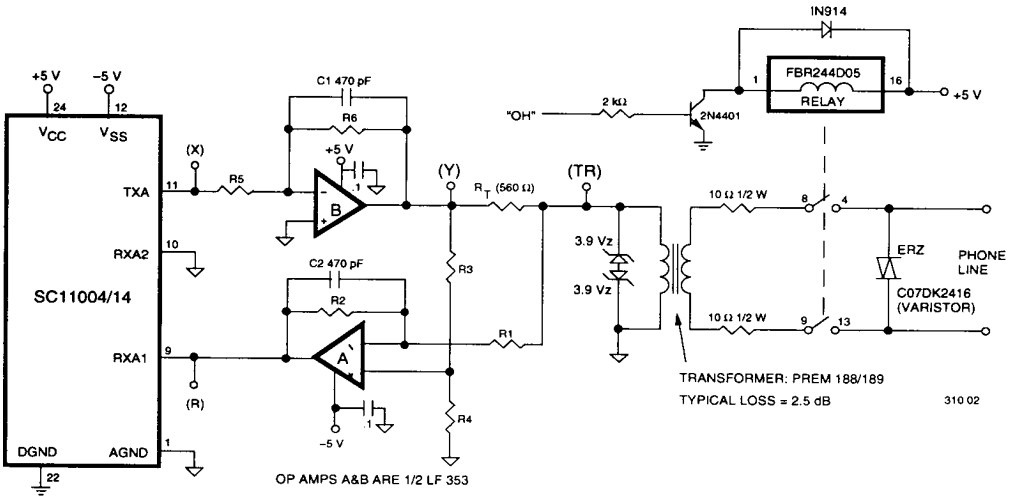


Figure 2. Using an External Hybrid with the SC11004/14

FUNCTIONAL DESCRIPTION OF THE SC11007 AND SC11008 CONTROLLERS

The SC11007 modem controller, implemented in Sierra's two micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including an 8-bit microprocessor, 8k by 8 bytes of ROM and 128 by 8 bytes of RAM, it also contains the functionality of an 8250B UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem for the PC consists of the SC11007 controller, the SC11004/14 modem and the DAA. All of the popular communications software written for the PC will work with the SC11004/14/SC11007 set.

Another version of the controller, the SC11008, is intended for RS-232 applications. It contains the same processor, memory and UART as the SC11007 and has the same interface to the modem chip. The difference is that the UART is turned around so the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The SC11008 provides a standard 5 V logic level interface—RS-232 drivers are required to interface to the port. Like the SC11007, the SC11008 comes preprogrammed with the Hayes 'AT' command set, and when used with the SC11004/14 modem, emulates a Hayes-type stand-alone modem. The SC11007 and SC11015 emulates a Hayes-type IBM PC plug-in card modem.

But the chip set is by no means limited to implementing a Hayes-type smart modem. Sierra is in the custom IC business and both chips were designed with this in mind. For example, only about 6k bytes of the SC11007's ROM is used for the handshaking and smart modem code, leaving 2k bytes for additional features that a customer may specify. And since the controller is ROM programmable, any command set, not just the Hayes 'AT' set, can be implemented.

Both the SC11007 and SC11008 require +5 V and are available in either a 28-pin DIP or a 28-lead plastic chip carrier with 'J' leads for surface mount applications. Besides the four-line interface for the SC11004/14 modem, the SC11007 controller has an 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control lines for ring indication, the off-hook relay and data/voice relay; these three lines connect to the DAA.

In the SC11008, the 8-bit port becomes the switch input lines and the address, chip select, DIST and DOST lines become the six lines for the RS-232 interface. These six lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control—so the main difference between the

This Material Copyrighted By Its Respective Manufacturer

SC11007 and SC11008 is the ROM code. It also contains the same modem and DAA interface lines as the SC11007.

The SC11007 and SC11008 are truly ASIC controllers—they are designed to control a modem or other peripheral that operates at a moderately slow rate up to 1200 bits per second. What's unique about the SC11007, for example is that it allows a slow peripheral to interface to a high speed bus, without making the main processor slow down.

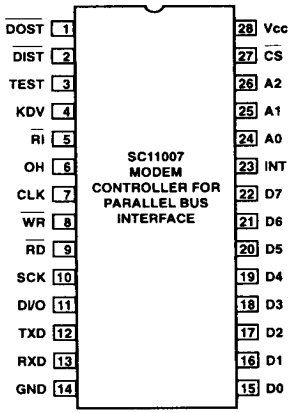
This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11007 compatible with this software, the registers were included.

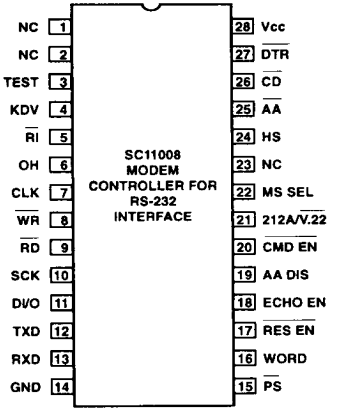
The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like in a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in software.

The actual processor contains an 8-bit data path and can execute 19 instructions with five different addressing modes: direct, indirect, immediate, register direct and register indirect. There is 8k by 8 of ROM on chip for program storage.

To the system bus, the SC11007 looks and acts just like an 8250B UART. Communications software written for this UART will work with the SC11007 and SC11008. The Sierra chip set is truly a Hayes-type modem in two chips.

CONNECTION DIAGRAMS—SC11007 AND SC11008 CONTROLLERS





THE SC11004/14 & SC11007/SC11008 SYSTEM

The only external components required by the SC11004/14 are the 600 Ω line matching resistor, a 7.3728 MHz crystal—a standard frequency—and a 20 pF capacitor from each leg of the crystal to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11004/14 can directly drive a high impedance (50 kΩ) earphone-type transducer.

The SC11007 modem controller's clock in line is driven by the SC11004/14's clock out line, so only one crystal is needed. The SC11007 interfaces directly to an IBM PC bus—no buffers are required. The only external parts may be a 8 input NAND gate for COM1 and COM2 decoding inside the PC.

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA or data access arrangement is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω; a relay for disconnecting the modem from the line; a ring

This Material Copyrighted By Its Respective Manufacturer

detector, typically an optoisolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by any of many consultants and labs around the country. The fee is typically $2,000 and it takes several months. Another alternative is to buy a DAA, supplied by several manufacturers.

212A is a Bell specification that calls for 1200 bit per second, full or half duplex data transmission with a fallback mode of 300 baud (Bell 103). It is not 1200 baud; the spec calls for transmission of dibits—2 bits per baud so the 1200 bps transmission takes place at 600 baud. The same is true for V.22—it's 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; there is a CCITT standard for 300 and that's V.21.

V.22 also calls for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11004/14 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone when in the receive mode.

All modems require a Hybrid. Hybrid is a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the SC11004/14, this is done with op amps, but the separate signals—TXOUT and RXA2—are also brought out so an external hybrid can be used, if desired. The combined signal comes out on the RXA1 pin and matching resistor—typically 600 Ω — is connected between RXA1 and RXA2.

SC11004/14 SPECIFICATIONS

Table 1. Definition of I/O Codes

1. Instructions to the modem IC (See Note 1 and 2). Data on the D I/O pin shifted into the modem when $\overline{WR}$ is low, on rising edges of the SCK clock. Data is transferred into a latch when $\overline{WR}$ goes high. (See Figure 2 for write cycle waveforms). Up to 7 data bits (D0–D6) can be sent to the device. These bits control the operating modes of the modem as shown below:

D6	D5	D4	D3–D0	HEX CODE	MODE/FUNCTION
Non tone mode:					
0	1/0	0	0	20/00	Reset (set default values)
0	1/0	0	1	21/01	Tone On/Off (tone mode enable/disable)
0	1/0	0	2	22/02	Force Receive Data to Mark Off/On (forces RXD pin High if On)
0	1/0	0	3	23/03	TLC0 Transmit Level Control bit 0 (default 0)
0	1/0	0	4	24/04	TLC1 Transmit Level Control bit 1 (default 0)
0	1/0	0	5	25/05	TX Transmitter On/Off (if Off, TXOUT is grounded)
0	1/0	0	6	26/06	ALB Analog Loopback On/Off
0	1/0	0	7	27/07	CPM Call Progress Monitor mode On/Off
0	1/0	0	8	28/08	Connection Indicator (CI) On/Off (see note 4 below)
0	1/0	0	9	29/09	ALC0 Audio Output Level Control bit 0 (default 0)
0	1/0	0	A	2A/0A	ALC1 Audio Output Level Control bit 1 (default 0)
0	1/0	0	B	2B/0B	WLS0 Word Length Select 0 (default 0)
0	1/0	0	C	2C/0C	WLS1 Word Length Select 1 (default 1)
0	1/0	0	D	2D/0D	Sync/Async
0	1/0	0	E	2E/0E	LS/HS: Low Speed/High Speed (FSK/PSK)
0	1/0	0	F	2F/0F	A/O: Answer/Originate
0	1/0	1	0	30/10	Transmit Mark On/Off
0	1/0	1	1	31/11	Transmit Space On/Off
0	1/0	1	2	32/12	Scrambler Off/On
0	1/0	1	3	33/13	DLB Digital Loopback On/Off (also sets Synchronous, Slave Mode)
0	1/0	1	4	34/14	TXDP Transit Dotting Pattern On/Off (Not valid for V.21 mode)
0	1/0	1	5	35/15	Sync Mode Transmit Timing Locked/Free Running
0	1/0	1	6	36/16	Sync Mode Transmit Timing Source External/Slave
0	1/0	1	7	37/17	2100 Hz tone On/Off. Must select low speed mode for operation.
0	2/0	1	8	38/18	1300 Hz tone On/Off. Must select low speed mode for operation.
0	1/0	1	9	39/19	V.21 mode. Must select low speed mode for operation.

This Material Copyrighted By Its Respective Manufacturer

D6	D5	D4	D3–D0	HEX CODE	MODE/FUNCTION
Tone mode:					
1	1/0	0	0	60/40	Dial 0
1	1/0	0	1	61/41	Dial 1
1	1/0	0	2	62/42	Dial 2
1	1/0	0	3	63/43	Dial 3
1	1/0	0	4	64/44	Dial 4
1	1/0	0	5	65/45	Dial 5
1	1/0	0	6	66/46	Dial 6
1	1/0	0	7	67/47	Dial 7
1	1/0	0	8	68/48	Dial 8
1	1/0	0	9	69/49	Dial 9
1	1/0	0	A	6A/4A	Dial *
1	1/0	0	B	6B/4B	Dial #
1	1/0	0	C	6C/4C	Output 550 Hz and insert 550 Hz notch in low-band filter
1	1/0	0	D	6D/4D	Output 1800 Hz and insert 1800 Hz notch in low-band filter
1	1/0	0	E	6E/4E	Row disable On/Off (For DTMF test only)
1	1/0	0	F	6F/4F	Column disable On/Off (For DTMF test only)

WLS1	WLS0	Word Length
0	0	8 bits
0	1	9 bits
1	0	10 bits (default)
1	1	11 bits

TLC1	TLC0	Transmitter Output Level (dBm) (Note 3).
0	0	–6 (default)
0	1	–3
1	0	0
1	1	+6

ALC1	ALC0	Audio Output Level
0	0	Output Off (default)
0	1	12 dB attenuation
1	0	6 dB attenuation
1	1	No attenuation

Notes: 1. Default values for the operating modes on power up are those shown to the right of the '/' unless otherwise specified.
2. Data is shifted in and out of the modem with LSB first.
3. SC11014 only.
4. Using the internal hybrid and a 600 Ω resistor, these levels will be 6 dB lower at the input to the transformer.
5. After a connection is established, turn CI on to disable unnecessary functions, i.e. if a PSK connection is established, turning CI on will turn off the FSK demodulator.

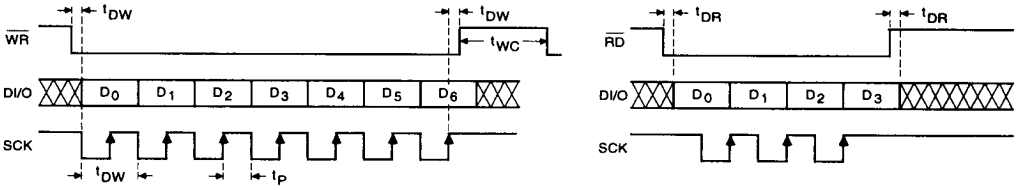
2. Information from the modem IC. Data is read serially from the modem when $\overline{RD}$ is low, on rising edges of the SCK clock. (See Figure 3 for read cycle waveforms). Up to 4 data bits (D0–D3) can be read as defined below:

D0 Energy Detect 0—no energy 1—energy present

In the CPM mode, the energy detector is connected to the output of the high band filter, if ALB is off, or the scaled low band filter, if ALB is on.

D1	Received data (FSK)	1—Mark	0—Space
D2	Received data (PSK)	1—Mark	0—Space
D3	Unscrambled Mark	1—Detected	0—Not Detected

This Material Copyrighted By Its Respective Manufacturer



t_{WC} = 4 µsec
t_{DW} = 200 nsec Min.
t_{PW} = 1 µsec Min.
t_P = 30% to 70% duty cycle
t_{DR} = 200 nsec Min.

Figure 3. Waveforms for Write and Read Cycles

Serial Interface — The 4 line serial interface consists of a bidirectional data pin (DI/O), a write control pin ($\overline{WR}$), a read control pin ($\overline{RD}$) and a clock pin (SCK). In the inactive state, $\overline{WR}$, $\overline{RD}$ and SCK lines must be held in the high state. The read and write functions are controlled only by the mircocomputer. To write data into the SC11004/14 (see timing waveforms of Figure 2), the controller must first make the $\overline{WR}$ line low. The least significant bit D0 of the data is then placed on the DI/O line. The SCK line is then toggled low and then high to shift the data bit into the SC11004/14 input register. Data is shifted into the input register on the rising edge of SCK.

There is no special requirement on the duty cycle of the clock signal. The minimum pulse width and data setup times specified in the specifications table must be met. The remaining data bits D1 thru D6 are shifted by repeating the above procedure. Only 7 data bits should be sent. If an 8th data bit is sent, the first data bit D0 will be lost from the input register. The received data will then be D7–D1 rather than D6–D0. To read data from the SC11004/14 (see timing waveforms of Figure 3), the $\overline{RD}$ line is first made low. The least significant bit D0 is now available on the DI/O line. The SCK line is toggled low and then high to shift the next data bit out of the SC11004/14 output register. The SC11004/14 shifts the data out on the rising edges of SCK. The controller should read data on the falling edges of SCK when it will be stable. Note that D0 appears on the DI/O line as soon as $\overline{RD}$ is taken low. If the controller only wants to read the status of the energy detector, there is no need to toggle SCK line. By making $\overline{RD}$ low, the energy detector level can be read by reading DI/O. $\overline{RD}$ can then be taken high. Read operation is terminated by making the $\overline{RD}$ line high. If more than 4 bits are read, the additional bits are returned as 0's.

In the READ mode, the values of D0, D1, D2 and D3 do not change as long as $\overline{RD}$ is low, even though the chip status may be changing. To read out the updated values of these bits, $\overline{RD}$ must be pulled high for at least 1 ms and then taken low again to initiate another read cycle.

The read and write operations can be performed by two simple I/O drivers shown in table 2. The RDMO–DEM subroutine reads data from the SC11004/14 and places it in the accumulator with the high nibble set to zero. The WTMODEM subroutine sends data placed in the accumulator to the SC11004/14. Both subroutines use register R7 in bank 1 as a data bit counter.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1 — SC11004/14 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 4.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11004/14 in the synchronous mode (2D). This provides a 1200 Hz clock on the TXCK0 Pin that can be used as a clock source for the DTE to synchronize its TXD to. The Transmit Phase-Locked-Loop (TX PLL) of the SC11004/14 will be in free-runing mode. As a result, External/Slave input codes will be ignored by the chip.

Case 2 —SC11004/14 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode (2D), also select "Locked" (35) and "External" (36) modes.

The TX PLL of SC11004/14 will then synchronize itself to the clock provided on its "TXCK1" pin.

Receiver Timing

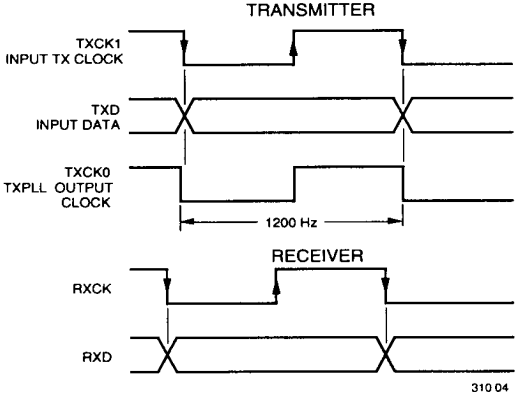
In synchronous mode, the recovered clock will be provided on the RXCK pin and the transitions of RXD will be on the falling edges of this clock.

This Material Copyrighted By Its Respective Manufacturer

SYNCHRONOUS MODE CHART

Transmitter Timing

Locked (35)	External (36)	TX PLL locks to clock provided on TXCK1
	Slave (16)	TX PLL locks to receiver timing. Should be used in DLB mode only.
Free Running (15)	External/Slave	TXPLL is free running and ignores External or Slave inputs.



NOTE: SC11004/14 will sample the data on the rising edge of TXCK1 clock.

Figure 4. SC11004/14 Synchronous Mode Diagrams

ABSOLUTE MAXIMUM RATINGS (NOTES 1, 2 AND 3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{CC}+0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{CC}+0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 s)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
F_C	Crystal Frequency		7.37243	7.37280	7.37317	MHz
T_R, T_F	Input Rise or Fall Time	(Note 4)			500	ns

Notes: 4. Does not apply to CKOUT.

This Material Copyrighted By Its Respective Manufacturer

DC ELECTRICAL CHRACTERISTICS (NOTE 5)

PARAM.	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	V_{CC} = 5 V			15		mA
I_{SS}	Quiescent Current	V_{SS} = –5 V			15		mA
V_{IH}	High Level Input Voltage	Digital Signal Pins $\overline{RD}$, $\overline{WR}$, D I/O, SCK, TXCK1, TXD		2.0			V
V_{IL}	Low Level Input Voltage	Digital Signal Pins $\overline{RD}$, $\overline{WR}$, D I/O, SCK, TXCK1, TXD				0.8	V
V_{OH}	High Level Input Voltage	Digital Signal Pins D I/O, RXD, TXCK0, RXCK	I_{OH} = 40 µA	4.0			V
			I_{OH} = 500 µA	2.0			V
V_{OL}	Low Level Input Voltage	Digital Signal Pins D I/O, RXD, TXCK0, RXCK	I_{OL} = 1.6 mA		0.4	0.6	V
V_{OM}	Maximum Output Signal	TXOUT, RL = 1200 Ω (TLC = 1, TLC0 = 0)		4.0			V_{p-p}
V_{IM}	Maximum Input Signal	RXA1, RXA2 (Using Internal Hybrid)				4.0	V_{p-p}

Note: 5. Min and max values are valid over the full temperature and operating voltage range. Typical values are from 25°C and ±5 V operation.

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQ.	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	+0.17%
Row 2	770 Hz	±1%	–0.26%
Row 3	852 Hz	±1%	+0.16%
Row 4	941 Hz	±1%	–0.47%
Column 1	1209 Hz	±1%	–0.74%
Column 2	1336 Hz	±1%	–0.89%
Column 3	1477 Hz	±1%	–0.01%
Guard Tones	550 Hz	±20 Hz	–1.4 Hz
	1800 Hz	±20 Hz	+7 Hz

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion			–40		dB
Row Output Level	V_{CC} = +5 V V_{SS} = –5 V TLC0 = 1 TLC1 = 1 Measured at TXOUT Pin		0		dBm
Column Output Level			2		dBm
550 Hz Guard Tone			–3		dB (Note 2)
1800 Hz Guard Tone			–6		dB (Note 2)

Notes: 1. This assumes a crystal of exactly 7.372800 MHz.
2. These levels are referenced to the TX signal level. When guard tones are added, the TXOUT level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

This Material Copyrighted By Its Respective Manufacturer

Modem Transmit Signals—Hz (Assume 7.372800 MHz Crystal)

MODE		BELL 103		CCITT V.21		212A/V.22	
		NOMINAL	ACTUAL	NOMINAL	ACTUAL	NOMINAL	ACTUAL
Answer	Mark	2225	2226	1650	1649.4	2400	2400
	Space	2025	2024.4	1850	1850.6		
Originate	Mark	1270	1269.4	980	978.34	1200	1200
	Space	1070	1070.4	1180	1181.53		
Calling Tone				1300	1301.7	1300	1301.7
Answer Tone				2100	2096.9	2100	2096.9

Transmitter

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Character Length	Start Bit + Data Bit + Stop Bit	8		11	bits
Intra-Character Bit Rate	AT TXD (Pin 14)	1170	1200	1212	bps
Input Break Sequence Length	M = Character Length	2M + 3			bits
Output Level Tolerance			±1		dB

Receiver

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Signal Range	AT RXA1	–45		0	dBm
Intra-Character Bit Rate	AT RXD (Pin 13)	1170	1200	1224	bps
Carrier Detect	AT RXA1 (Pin 9)	–48		–43	dBm
Carrier Detect Hysteresis		2			dB
Carrier Detect Delay	For 103, 212A and V.22	10	20	30	ms
Carrier Detect Hold	For 103, 212A and V.22	15	20	24	ms
Carrier Detect Delay	For V.21 Mode	15	30	40	ms
Carrier Detect Hold	For V.21 Mode	20	30	50	ms

This Material Copyrighted By Its Respective Manufacturer

APPLICATIONS INFORMATION

Why a Modem/What's a Modem

The voice frequency channels of the general switched telephone network have been used extensively for the transmission of digital data. To use these channels, the data must be put in a form that can be sent over a limited bandwidth line. In voice grade telephone networks, transformers, carrier systems and loaded lines attenuate all signals below 300 Hz and above 3400 Hz.

While the bandwidth from 300 Hz to 3400 Hz is fine for voice transmission, it is not suitable for the transmission of digital data because the data has many frequency components outside this range. To transmit data over phone lines, it is necessary to convert the digital data into a signal that is totally within the voice frequency range. This conversion is performed by a MODEM (MODulator DEModulator).

In full duplex data transmission—the simultaneous sending and receiving of data—Frequency Division Multiplexing (FDM) can be used for data rates up to 2400 bits per second. In FDM, the voice channel is divided into upper and lower bands (called the high band and the low band); one is used for sending and the other for receiving data. The originating terminal transmits in the low band and receives in the high band, while the answering terminal transmits in the high band and receives in the low band.

In low speed modems (300 bit per second transmission rate), the modulation technique commonly employed is called Frequency Shift Keying (FSK). In FSK modems, four separate frequencies are used; 1070 Hz for a zero (also called a space) in the low band, 1270 Hz for a one (a mark) in the low band, 2025 Hz for a zero in the high band and 2225 Hz for a one in the high band. The transmitting modem takes the digital ones and zeros from the terminal and converts them into the proper tones which are then sent over the phone line. The receiving modem takes the tones and converts them back to ones and zeros and sends them to the receiving terminal. Since four frequencies are used, simultaneous transmitting and receiving of data can be accomplished.

Because of the limited bandwidth of the phone line, FSK modems only work up to 600 bits per second for full duplex transmission. This is due to the fact that when the modem shifts between the two frequencies (for mark and space) it generates a frequency spectrum (it is a type of FM—frequency modulation—transmission). The faster the data rate, the wider the spectrum. The limit for full duplex FSK transmission is 600 bits per second, before the available audio spectrum is used up—allowing for enough separation between the frequency bands to reliably decode or demodulate the data. There are 1200 bps FSK modems, but these are half duplex—they can only send OR receive data at 1200 bps.

In higher speed, full duplex modems (1200 bit per second transmission rate) a different modulation technique is employed. Called PSK (for Phase Shift Keying), this technique uses one carrier frequency for the high band—2400 Hz—and one for the low band—1200 Hz—for sending and receiving data. For each carrier frequency (one for transmitting and one for receiving), one of four phase angles is used: 0, 90, 180, or 270 degrees. The data is sent two bits at a time, or in dibits. Since there are four ways to send two bits at a time—00, 01, 10 or 11—each of the four phases represents one unique dibit. While the data rate is 1200 bits per second, the baud rate (the rate at which information packets are sent) is 600 because two bits (dibits) are sent in each packet. Again, 600 packets per second (600 baud and, in this case, 1200 bps) is the limit for transmitting full duplex data over the general switched telephone network using FDM.

Call Progress Monitor Operation

The modem controller uses the high-band and low-band filters in the SC11004/14 for call progress monitoring. When the SC11004/14 is put in the CPM mode, the ALB mode provides a means of connecting either the high-band filter (ALB = 0) or the scaled low-band filter (290–660 Hz) (ALB = 1) to the energy detector. Output of the energy detector is monitored by reading bit D0 for detection of call progress or voice/answer information, using the duration and repetition rate as the criteria for detection.

A typical call establishment sequence is as follows:

Dial tone detection — The controller puts the SC11004/14 in the Originate, CPM mode with ALB = 1 and operates the off-hook relay in the DAA by making the OH output high. After a short delay (typically 300 ms), it monitors the output of the energy detector (ED). If the output is continuously high for at least 1 second; it is recognized as a valid dial tone. If the output is not continuous then the controller continues to monitor until a timeout occurs (typically 5 seconds). If a dial tone is not detected within this timeout, the controller returns a 'NO DIAL TONE' message to the DTE and aborts the call. If a dial tone is detected, it proceeds to dial the number as follows.

Dialing—The controller will use the specified format (tone or pulse) or determine the best way, if not specified. Assuming that the format is not specified, the controller will dial the first digit in the tone format. It will wait for a short time

This Material Copyrighted By Its Respective Manufacturer

(typically 80 ms) after dialing and check the output of the ED. If the output is low, it will mean that the dialing can proceed in the tone format. If the output is high, it will mean the dial tone is still present. The controller will then revert to the pulse format and redial the first digit. In all cases, the controller will check for loss of dial tone after a short delay (typically 80 ms) after dialing the first digit. If the dial tone is absent it will proceed to dial the remainder of the number. During the inter-digit pause (IDP), the controller will monitor the ED output after waiting for a short time (typically 80 ms). If the ED output is high, it will halt dialing, abort the call and return 'BUSY' message to the DTE.

If a pause is required in the dialing sequence for a second dial tone, the controller will repeat the above process. After dialing is done, the controller will wait for approximately 2.5 seconds and then start to monitor the ED output by alternately toggling the ALB mode at a rate of approximately 200 ms. This allows detection of ringback/busy call progress tones or voice/answer tone. The toggling rate is based on the settling times of the filters as well as the response time of the ED. Once energy is detected at the output of the ED, the controller will maintain the selected ALB mode until detection is made. The criteria for various detections are described below.

Ringback tone detection—Both duration and repetition rate are used to determine ringback tone. If the ED output is high for a cumulative duration of at least 0.7 second, but less than 3.8 seconds, with the number of transitions less than 7 over a period of 5 seconds, it is recognized as a valid ringback tone. The 5 second window is started when the ED output first goes high. Once the ringback is detected, the controller counts the number of ringback cycles and compares to the value stored in the ringback counter register (S1). If the ringback tone continues to be present after the preset number of cycles, the controller will abort the call and return 'NO ANSWER' message to the DTE.

If the ringback tone is removed prior to the preset value, the controller will switch the ALB to 0 to monitor the voice/answer tone. During the silent portion of the ringback cycle, the controller will also switch to monitor the high-band filter output to see if there is an answer. This speeds the response to an answer condition.

Busy tone detection—If the number of transitions of the ED output exceeds 7 over the 5 second window when looking for ringback tone, it will be assumed to be a busy signal. The controller will then abort the call and return a 'BUSY' message to the DTE.

Answer tone detection—If the output of the high-band filter is continously high for at least 2 seconds, the controller will assume it to be an answer tone from the distant modem, return a 'connect' message to the DTE and proceed with handshaking sequence necessary to establish a data call.

Voice detection—If the output of the ED is not continuously high over a 2 second period, it will be assumed to be voice and the controller will return a 'VOICE' message to the DTE and abort the call.

Silence detection—If the cumulative duration over the 5 second window is less than 0.7 second, once the window is started, it is recognized as silence. The controller then returns a 'NO ANSWER' message to the DTE and aborts the call.

Specific Applications

The SC11004/14 modem performs all the signal processing functions required in a 212A/V.22 modem. Like all modems, it requires an external controller to implement the handshaking protocols and control functions. The controller's task is simplified by the use of a 4 line serial interface as opposed to a multiline parallel interface. In particular, only I/O pins are used on a single chip microcomputer. More pins are then available for other interfaces such as DAA, RS-232, switches and lights. In most modem applications this will eliminate the need for external latches and buffers for additional I/O pins.

Figure 5 shows the SC11004/14 modem IC used with the SC11007 controller to make a complete parallel bus Hayes-type smart modem.

Figure 6 shows the SC11004/14 modem IC used with the SC11008 controller to make a complete RS-232 serial interface Hayes-type smart modem.

Figure 7 shows the schematic of a stand-alone smart modem implemented with the SC11004/14 and the 8031—the ROMless version of the 8051 microcomputer. Even though 16-port I/O pins are used up on the 8031 for interfacing with the external ROM, enough pins are still available for the other interfaces because of the serial interface used on the SC11004/14. The 8031 microcomputer was selected because of its wide use in current stand-alone and integrated smart modems.

Oscillator—The SC11004/14 includes an inverting amplifier and a bias resistor so that a crystal oscillator can be designed by connecting a 7.3728 MHz crystal and two capacitors (27 pF and 47 pF) to XTAL1 and XTAL2 pins as shown in the schematic. A buffered TTL compatible clock output is available on the CLOCK OUT pin to drive the microcomputer.

This Material Copyrighted By Its Respective Manufacturer

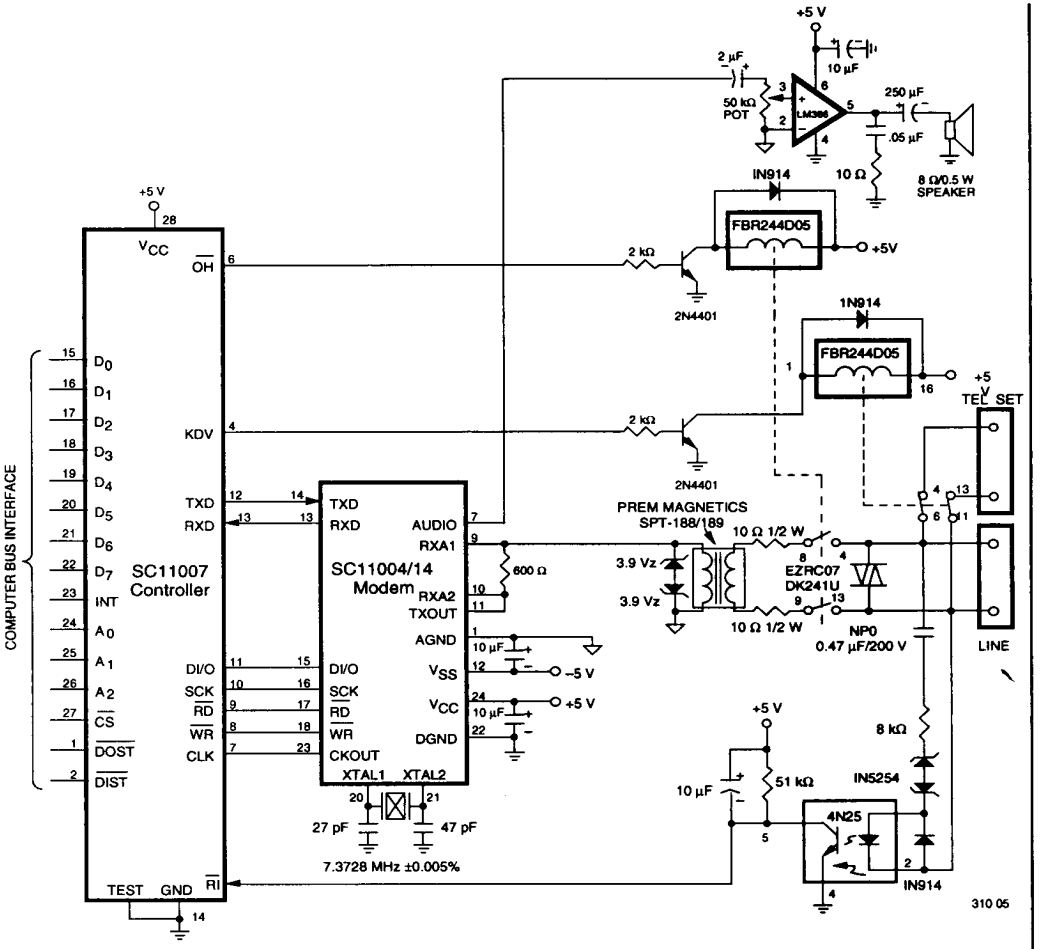


Figure 5. Internal 212A/V.22 Smart Modem Using the SC11004/14 Modem IC and the SC11007 Controller

This Material Copyrighted By Its Respective Manufacturer

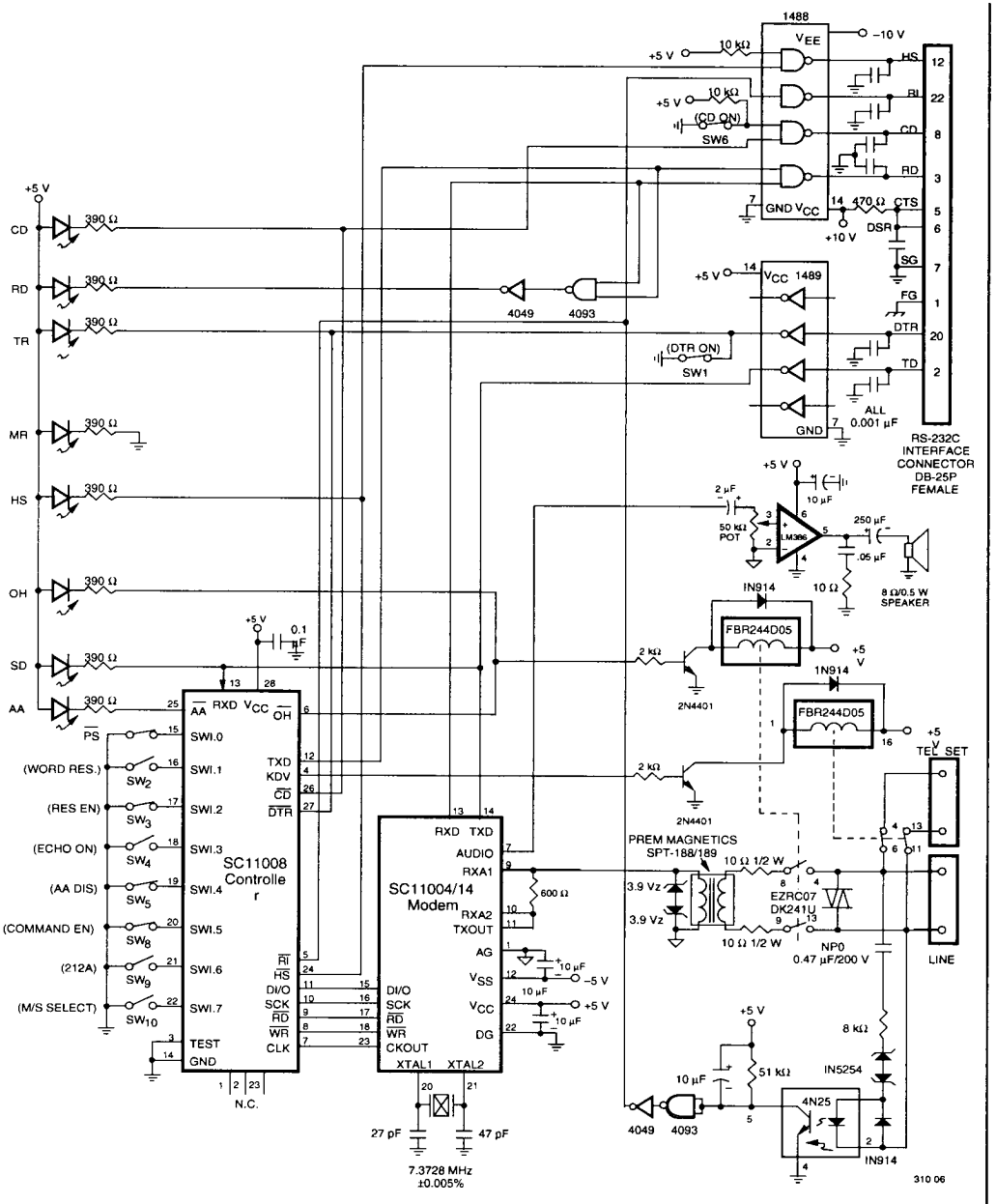


Figure 6. 212A/V.22 Stand-Alone Intelligent Modem Using the SC11004/14 Modem IC and the SC11008 Controller

This Material Copyrighted By Its Respective Manufacturer

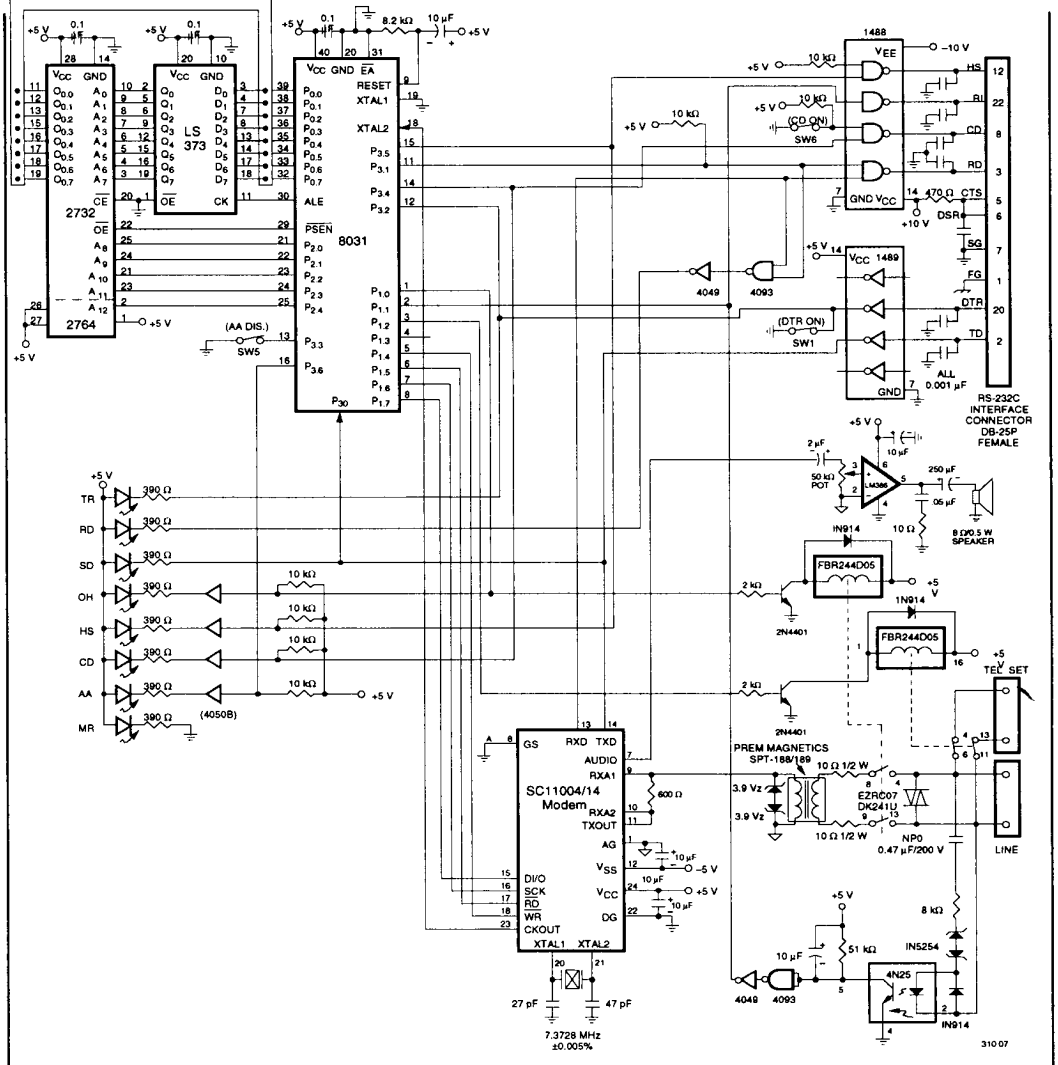


Figure 7. 212A/V.22 Stand-Alone Smart Modem Using the 8031 Controller with SC11004/14 Modem

This Material Copyrighted By Its Respective Manufacturer

```
WTMODEM:   CLR     P1.4          ;WR → 0;  Initiate Write Cycle
           SETB    RS0           ;Select Bank 1
           MOV     R7, #7        ;Set Data Bit Counter to 7

OUTNEXT:   RRC     A             ;Bit → Carry
           CLR     P1.6          ;Toggle Clock Line Low
           JC      SETPB         ;Set/Clear DI/O Line on Carry
           CLR     P1.7
           LJMP    OUTPUT

SETPB:     SETB    P1.7

OUTPUT:    SETB    P1.6          ;Toggle Clock Line High
           DJNZ    R7, OUTNEXT   ;Loop Till Data Bit Counter is Zero
           SETB    P1.7          ;Return to Initial Condition
           SETB    P1.4
           CLR     RS0
           RET

RDMODEM:   CLR     P1.5          ;RD → 0 ; Initiate Read Cycle
           SETB    RS0
           MOV     R7, #8

INNEXT:    CLR     P1.6
           MOV     C, P1.7       ;Data Bit → Carry
           RRC     A             ;And into Accumulator
           SETB    P1.6
           DJNZ    R7, INNEXT    ;Loop Till Data Bit Counter is Zero
           SETB    P1.5          ;Return to Initial Condition
           CLR     RS0
           RET
```

To dial a digit, the sequence shown below can be used. It is assumed that register R2 holds the digit to be dialed and memory location S11 holds the on/off duration of the tines in milliseconds.

```
TDIAL:     MOV     A, #21H       ;Turn on Tone Mode
           LCALL   WTMODEM
           MOV     A, R2         ;Read Digit
           ORL     A, #60H       ;Form Digit On Command
           LCALL   WTMODEM
           MOV     A, S11
           MOV     B, #10
           DIV     AB            ;Find Number of 10 ms Increments
           MOV     R1, A         ;Save It
           LCALL   DLOOP         ;Wait 10 ms Times Number in R1
           MOV     R1, A         ;Restore R1
           MOV     A, R2         ;Form Digit Off Command
           ORL     A, #40H
           LCALL   WTMODEM
           LCALL   DLOOP         ;Wait 10 ms Times Number in R1
           LJMP    NEXTDG        ;Go for Next Digit
```

Table 2. Serial I/O Driver Routines

This Material Copyrighted By Its Respective Manufacturer

In the following examples it is assumed that the clock frequency for the 8031 is 7.3728 MHz and that timer 0 is set in the auto-reload mode cycling at the rate of 416.66 µs. References are also made to certain registers used in Hayes compatible smart modems.

Initialization—The SC11004/14 does not have a power on reset circuit. The controller must put the device into the proper operating mode on power turn on. By sending a reset code, the device will enter a default mode as follows: high speed, asynchronous, originate, transmitter off, RX data clamped to mark, transmit level = –12 dBm, audio off and scrambler on. This mode is set up by the following lines of code:

```
MOV     A, #0        ;Reset Code
LCALL   WTMODEM      ;Write It
```

Dialing—The SC11004/14 includes an on chip DTMF dialer. It is necessary to adjust the transmit level during dialing since the tone level is internally set to be 6 dB below the transmitted carrier level. The following lines of code will set the tone level at the line to be –6 dBm for low group and –4 dBm for the high group tone:

```
MOV     A, #23H      ;TLC0 = 1
LCALL   WTMODEM
MOV     A, #24H      ;TLC1 = 1
LCALL   WTMODEM
```

Call Progress Monitoring—The progress tones can be monitored readily by activating the call progress monitor (code = 27H) and analog loopback (code = 26H) modes. The low band filter is then scaled down by a factor of 2.5 to center over the frequency range of 300 Hz to 660 Hz. Output of the energy detector monitored on the D0 bit then provides the necessary cadence information for detection of various call progress conditions. For example, dialtone is detected if the energy detector output is continuously high for at least 1 second. Busy line condition is recognized if the number of transitions of the energy detector output exceeds 7 over a period of 5 seconds and if the cumulative on duration exceeds 2 seconds.

Handshaking Sequences—Sequences necessary for establishing calls in various operating modes are provided in the following paragraphs. Numbers in parentheses indicate the hex code values sent to the SC11004/14 to implement that function of data bit received from the SC11004/14 for monitoring a given function.

A. Originating call in high speed (212A) mode:

1. Clamp receive data to mark condition (2)
2. Sample energy detector output (D0) to see if answer tone is present.
3. If continuous answer tone is detected for time set in register S9 (typically 600 ms) prior to timeout set in register S7 (typically 30 s) proceed with handshaking. Otherwise output NO CARRIER to data terminal and abort call.
4. Transmit mark (30).
5. Turn transmitter on (25).
6. Wiat for 300 ms.
7. Sample PSK data output (D2) at twice the bit rate (every 416.66 µs).
8. If continuous PSK data mark signal is received for 64 bit intervals, proceed to step 9. If PSK data mark signal is not received prior to timeout set in S7, output NO CARRIER to data terminal and abort call.
9. Wait for 700 ms.
10. Turn connection indicator on (28).
11. Turn transmitter mark off (10).
12. Unclamp receive data (22).
13. Turn on carrier detect output.
14. Send CONNECT or CONNECT 1200 message to data terminal.

B. Originating call in low speed (103) mode:

1. Perform steps 1 thru 3 as in A) above.
2. Put SC11015 in low speed mode (2E).
3. Carry out steps 4 thru 6 as in A) above.
4. Go to step 11 in A) above.

C. Answering call (212A–103) mode:

1. Put SC11004/14 in answer mode (2F).
2. Wait 2.1 seconds (billing timeout).
3. Put SC11004/14 in low speed mode (2E).
4. Transmit mark (30).
5. Turn transmitter on (25).
6. Sample energy detector output (D0) to see if carrier is present. If carrier is received continuously for 200 ms, proceed to step 7. If timeout set in S7 occurs, output NO CARRIER and abort call.
7. Sample PSK detector output (D2) at twice the bit rate (every 416.66 µs).
8. If continuous PSK data mark is received for 64 bit intervals, prior to one second timeout, proceed to step 9. If continuous FSK data mark is received for 256 bit intervals, proceed to step 10 in A) above. If neither PSK or FSK data mark is received prior to timeout set in S7, output NO CARRIER to data terminal and abort call.
9. Put SC11004/14 in high speed mode (0E).
10. Go to step 9 in A) above.

This Material Copyrighted By Its Respective Manufacturer

D. Originating call in high speed (V.22) mode:

1. Clamp receive data to mark condition (02).
2. Select low speed mode (2E), V.21 mode (39).
3. Turn on calling tone (38) for 0.6 seconds followed by 1.5 seconds of off period until answer tone is detected.
4. Turn off calling tone (18) and V.21 mode (19).
5. Select high speed mode (0E).
6. Wait for unscrambled mark.
7. Wait 456 ms, then proceed to step 4 in A) above.

E. Originating call in low speed (V.21) mode:

1. Perform steps 1 thru 4 as in D) above.
2. Wait for 1 second, then send FSK mark.
3. Wait for carrier to drop. Start a 3 second timer. If carrier drops prior to timeout proceed to step 4. Otherwise proceed to step 4 after timeout.
4. Wait for FSK mark.
5. Turn on connection indicator (28).
6. Turn transmit mark off (10).
7. Unclamp receive data (22).
8. Turn on carrier detect output.
9. Send CONNECT message to terminal.

F. Answering call (CCITT mode) with auto speed detection (V.22/V.21):

1. Select answer mode (2F).
2. Turn scrambler off (32).
3. Wait for 2.1 second billing timeout.
4. Select low speed mode (2E); V.21 mode (39).
5. Turn on 2100 Hz answer tone (37). Start 3.3 second timer.
6. Turn off 2100 Hz answer tone (17) after timeout.
7. Turn transmitter off (05).
8. Wait 60 ms.
9. For next 20 ms look for carrier and continuous FSK mark. If detected, assume low speed and proceed to step 14.
10. Turn transmitter on (25).
11. Select high speed mode (0E). Turn off V.21 mode (19).
12. Turn on 1800 Hz guard tone; (21), (6D).
13. Start 1 second timer. Look for continuous PSK mark for 64 bit intervals over 1 second period. If PSK mark is not detected within 1 second, turn off high speed mode, (select low speed mode), turn off guard tone, turn on V.21 mode and look for continuous FSK mark for 64 bit intervals over the next 1 second period. If FSK mark is not detected, repeat from start. If timeout set in S7 occurs prior to detecting either PSK or FSK mark, output NO CARRIER and abort call. If either PSK or FSK mark is detected, go to step 10 in A).
14. Turn transmitter on (25).
15. Send CONNECT message to terminal.
16. Turn connection indicator on (28).
17. Turn carrier detector on.

G. Requesting remote digital loopback to far end modem:

1. Clamp receive data to mark condition (2).
2. Force transmitter to mark (30).
3. Disable scrambler (32).
4. Wait for 180 ms (send unscrambled mark).
5. Sample PSK detector output (D2) to see if dotting pattern (alternating 1/0 pattern) is received. If dotting pattern is not received within 212 ms, output ERROR to data terminal and return to on line state.
6. Turn scrambler on (12).
7. Wait 270 ms (send scrambled mark).
8. Go to step 11 in A) above.

H. Terminating remote digital loopback:

1. Force transmitter to mark (30).
2. Clamp receive data to mark (2).
3. Turn transmitter off (5).
4. Wait 80 ms.
5. Turn transmitter on (25).
6. Wait 270 ms (send scrambled mark).
7. Go to step 11 in A) above.

I. Response to remote digital loopback request:

1. In on line state monitor unscrambled mark detector output (D3). Go to step 2 if unscrambled mark is detected.
2. Clamp receive data to mark (2).
3. Transmit dotting pattern (34).
4. Wait until unscrambled mark detector turns off.
5. Turn off dotting pattern (14).
6. Put SC11015 in digital loopback (33).
7. Remain in digital loopback until loss of carrier is detected.
8. Terminate digital loopback.
9. Return to on line state.

This Material Copyrighted By Its Respective Manufacturer