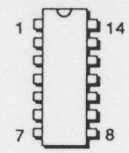
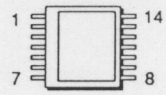
FEATURES

- ☐ On-chip Ring Detection
- ☐ Highly integrated solution
- ☐ Energy Detection for Qualification of Valid Data
- ☐ Low Power Consumption

14-PIN DIP PACKAGE



14-PIN SOIC PACKAGE



GENERAL DESCRIPTION

Caller Identification Service is provided by the local telephone companies. Customers who subscribe to this service receive the calling party's phone number while the phone is still on-hook. The phone number is transmitted from the central office to the subscriber during the silent interval between the first and second ring. The signaling interface is arranged to allow simplex data transmission on the voice channel to the customer premises and conforms to the specifications listed in Table 1.

The SC11212 Caller Identification Circuit is a highly integrated analog front end that is used to support Caller Number Delivery (CND) in the General Switched Telephone Network (GSTN). The SC11212 integrates ring detection, a 4 pole filter, an FSK demodulator, and energy detection on a single die (see Figure 1). The ring detection scheme incorporates a 2 step algorithm for qualifying a valid ring. This algorithm is especially useful in low power applications.

BLOCK DIAGRAM

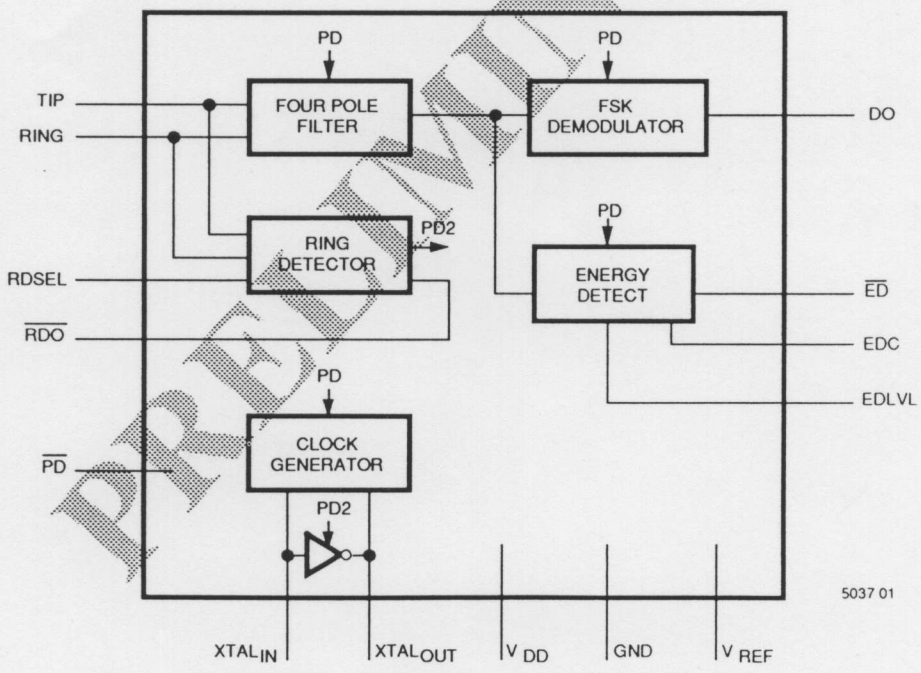
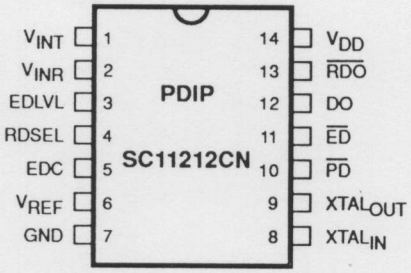


Figure 1.

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
DO	12	The output of the FSK demodulator appears at this pin.
$\overline{ED}$	11	Energy-Detect output. Goes low when inband energy is present and detected by the energy detect circuit.
EDC	5	Energy-Detect Capacitor. A 0.1µF capacitor should be connected between this pin and ground.
EDLVL	3	Energy detect level control.
GND	7	Ground pin (0V).
$\overline{PD}$	10	Power down input control. When pulled low the chip will go into a power down mode.
$\overline{RDO}$	13	Ring Detect output. Goes low when ringing signal is detected.
RDSEL	4	Ring detector control input.
V_{DD}	14	Positive power supply (+5V).
V_{INT}	1	Tip input of the telephone line.
V_{INR}	2	Ring input of the telephone line.
V_{REF}	6	Reference ground pin. For improved performance a 1µF capacitor should be connected between this pin and ground. This voltage is nominally halfway between the positive supply and ground.
$XTAL_{IN}$	8	Crystal input or 3.5795454 MHz input from external clock source.
$XTAL_{OUT}$	9	Crystal output.

CONNECTION DIAGRAMS



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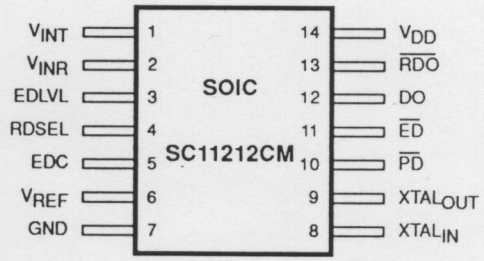

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FUNCTIONAL DESCRIPTION

The Caller Identification (SC11212) is a CMOS device that operates with a single 5V power supply. A block diagram of the chip is shown in Figure 1. It consists of an input differential buffer, a 4-pole bandpass filter, an FSK demodulator, and energy detect circuit, a clock generator and a ring-detect circuit. The chip has an onboard crystal oscillator, but it can also accept a 3.5795454 MHz clock and use it to generate timing for the internal blocks. The energy detect has two detect levels which are controlled by the EDLVL input pin. The chip has a power-down mode which is controlled by the $\overline{PD}$ input pin. During power down, the four pole filter, the FSK demodulator, the energy detect, the oscillator and part of the ring detect circuit is deactivated. The first time the tip and ring inputs make a transition, the ring detector becomes active and begins qualifying the ringing input. The presence of ring signal is transferred to the controller by the $\overline{RDO}$ pin. The controller subsequently can power up the chip and look for the demodulated data from the DO pin. The chip is available in a 14 pin package.

Analog Input Section

The analog input section accepts a differential signal which should be AC coupled to the V_{INT} and V_{INR} input pins. Since the chip operates with a single power supply, an analog reference ground is generated internally which is nominally halfway between the positive supply and ground. A conceptual circuit diagram of the input section and the external circuit elements are shown in Figure 2. The analog input operates in two different modes. In the ring detect mode the ringing high voltage signal which is ac coupled to the V_{INT} and V_{INR} inputs, is attenuated by the combination of the external and onchip resistors by closing the two S1 and S2 switches. In the Normal FSK demodulation mode the S1 and S2 switches are open, and the signal is applied to the FSK demodulator, without being attenuated. The FSK modulated signal passes through a 4 pole filter with frequency response as shown in Figure 3.

Link Type:	Simplex, two wire
Transmission Scheme:	Analog, phase-coherent frequency shift keying (FSK)
Logical 1 (Mark):	1200 plus or minus 12Hz
Logical 0 (Space):	2200 plus or minus 22Hz
Transmission Rate:	1200 bits per second
Application of Data:	Serial, binary, asynchronous
Transmission Level:	-13.5 Plus or minus 1 dBm at the point of data application into a resistive load of 900 Ohms
Insertion Loss @ 3KHz:	10-14dB

Table 1.

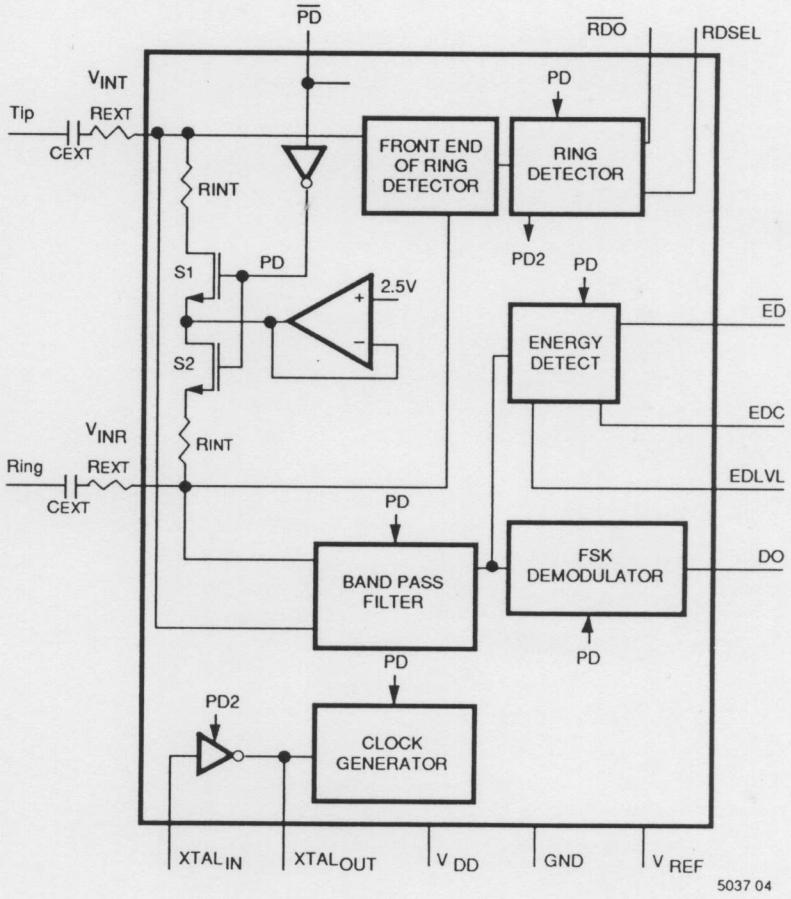


Figure 2.

Energy Detect Circuit

The energy detect circuit takes its input from the output of the bandpass filter. It rectifies the signal and uses an averaging circuit to determine the energy level. It needs an external capacitor for its operation. With the external capacitor equal to 0.1µF, the on-to-off and off-to-on response times of the energy detect will nominally be 5msec. The energy detect level has two distinct values and is controlled

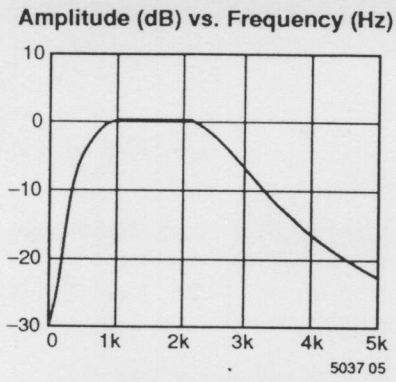


Figure 3. SC11212 Bandpass Filter

by the EDLVL control pin according to the following table:

EDLVL	Detect Level
Low	–32dBm on –35dBm off
High	–35dBm on –38dBm off

These levels are valid for the positive power supply equal to 5V DC.

Power-Down Mode

The $\overline{PD}$ input pin controls the power-down function. When this signal is pulled low the chip will be power-downed and the supply current will reach its minimum level. During power-down, the input section of the ring detect circuit remains active and the rest of the chip is deactiviated.

Ring-Detect Circuit

The data corresponding to the caller number is transmitted to the customer premises during the silent period of the first and second ringing signal. The caller ID circuit should monitor the line during the on-hook condition. When the ringing signal is detected, the microcontroller will be informed, which in turn will turn on the FSK demodulator and look for the caller ID signal. During the period that the Caller ID chip is monitoring the telephone line for the ringing signal, part of the ring detect circuit which draws minimum current (less than 15 µA) will be active. The ringing signal is normally a differential signal with a magnitude equal to 140-175Vrms, which is superimposed on a DC voltage. In order to prevent the high voltage from damaging the chip the signal is AC coupled to the input pins through an attenuator. The attenuator is formed by the external resistor Rext and the on-chip resistor Rint shown in Figure 2. During ring detection, when the $\overline{PD}$ pin is low and the rest of the circuit is in the power down mode, the two switches in series to the internal resistors are turned on and they bias the midpoint of the resistors to halfway between the power supply and ground. The first time that the differential voltage betweeen the Tip and Ring is greater than 40 Vrms, the oscillator will start and the rest of the ring detector will be powered up and will start measuring the period of the incoming alternating ringing voltage. If the frequency of the input signal is determined to be between 14-65Hz by validating the period for one or two cycles of the ringing signal, the $\overline{RDO}$ pin will be pulled low, indicating the presence of a valid ringing signal. The choice between validating the period for one or two cycles is determined by the state of the input pin RDSEL. If RDSEL="Ø" one cycle will be validated, if RDSEL="1" two consecutive cycles should be validated before valid ringing signal is detected. When the ring detector circuit is powered up, a timer is also started which is reset every time a valid ringing edge occurs. In the absence of an edge the timer will expire in 500msec and the ringing circuit will return to its power down mode. Once the processor receives a valid ring detect signal by detecting a low level on the $\overline{RDO}$ pin, it will continue monitoring the $\overline{RDO}$ pin until it returns to a high level again. This action will be interpreted by the processor as the completion of the first ringing cycle, and the beginning of the first silent period. After this, the processor will wait for a known period, after which time it will power up the chip by pulling the $\overline{PD}$ pin to a high level and will start monitoring the energy detect output. When the $\overline{PD}$ pin is pulled high, the switches in series to the two internal resistors will open, causing the full line signal to be applied to the FSK demodulator without being attenuated. The high to low transition of the energy detect is an indication of the presence of FSK tones, after which time the processor should read the incoming data from the DO pin. After the chip is powered up, the processor should give the energy detect and the demodulator some time (approx. 5msec) to settle, before it attempts to read the relevant data.

Crystal Oscillator

The crystal oscillator only requires an external crystal to run. The oscillator will only start when $\overline{PD}$ is high or at the reception of a voltage greater than 40Vrms between the Tip and Ring (see Figure 4).

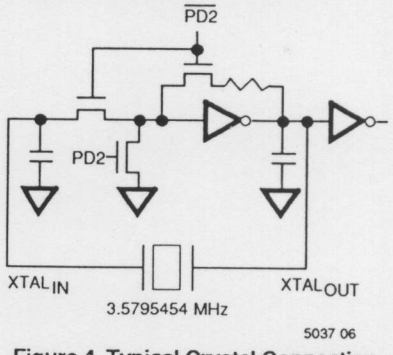


Figure 4. Typical Crystal Connection

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, & 3)

Supply Voltage, V_{CC} – GND	+6V
Voltage on any Pin	GND – 0.3 to V_{CC} + 0.3 V
Current at any Pin	10 mA
Storage Temperature	–65 to +150°C
Power Dissipation (Note 3)	100 mW
Lead Temperature (Soldering 10 sec)	300°C

OPERATING CONDITIONS (Note 4)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
GND	Ground			0		V
F_C	Crystal Frequency		3.576	3.579545	3.583	MHz

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Unless otherwise specified all voltages are referenced to ground.

NOTE 3: Power dissipation temperature derating: Plastic package: –12mW/C from 65°C to 85°C.
Ceramic package: –12mW/C from 100°C to 125°C.

NOTE 4: Min and max values are valid over the full temperature and operating voltage range. Typical values are for 25 °C and 5 V operations.

DC ELECTRICAL CHARACTERISTICS (Notes 1 and 2)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
V_{CC}	Operating Supply Voltage		4.5		5.5	V
I_{CC}	Operating Supply Current				7	mA
P_O	Power Consumption $\overline{PD}$ = 1	f = 3.579 MHz; V_{CC} = 5 V			35	mW
PD	Power Consumption $\overline{PD}$ = 0				15	µA
INPUTS						
V_{IL}	Low Level Input Voltage				.8	V
V_{IH}	High Level Input Voltage		2			V
I_{IH}/I_{IL}	Input Leakage Current	V_{IN} = GND or V_{CC}		0.1		µA
$\overline{PD}$	Pull Up (Source) Current			100		µA
EDLVL	Pull Down (Sink) Current			100		µA
CLK_{IN}	Load Capacitance			20		pF
CLK_{IN}	High Level Input Leakage Current		3	50	µA	
CLK_{IN}	Low Level Input Leakage Current		3	50	µA	
OUTPUTS						
I_{OL}	Output Low (Sink) Current	V_{OUT} = 0.4 V	1.0	2.5		mA
I_{OH}	Output High (Source) Current	V_{OUT} = 4.6 V	0.4	0.8		mA
CLK_{OUT}	Driving Capacitance				100	µA
CLK_{OUT}	High Level	V_{OUT} = 2.8V			200	µA
CLK_{OUT}	Low Level	V_{OUT} = 0.4V			20	pF

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Unless otherwise specified all voltages are referenced to ground.

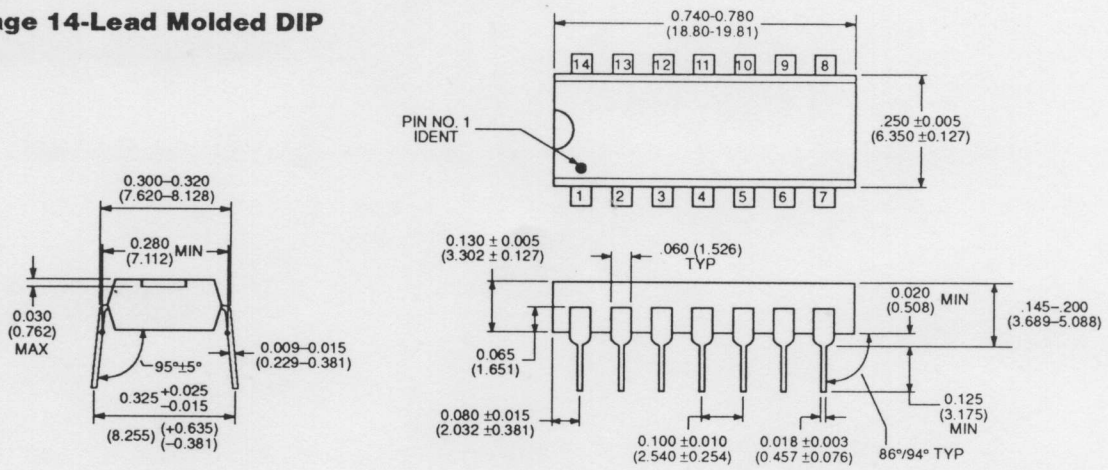
AC CHARACTERISTICS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{INT} to GND	Impedance ($\overline{PD}$ = 1)	75	100	125	kΩ
V_{INR} to GND	Impedance ($\overline{PD}$ = 0)		3.3		kΩ
V_{INT} to	Impedance ($\overline{PD}$ = 1)	150	200	250	kΩ
V_{INR} .	Impedance ($\overline{PD}$ = 0)		6.6		kΩ
V_{INT} V_{INR}	Differential Voltage on High Input Imp. ($\overline{PD}$ = 1)	24.5			mV[1]
V_{INT} V_{INR}	Differential Input Level into 600Ω ($\overline{PD}$ = 1)	–30			dBm[1]
V_{INT} V_{INR}	Voltage on either tip or ring (14 to 65 Hz) ($\overline{PD}$ = 0)	600			mVRMS

NOTE 1: Maximum Differential Input Voltage Peak to Peak: 0.75 V

PHYSICAL DIMENSIONS—Inches (Millimeters)

Package 14-Lead Molded DIP



Package 14-Lead Molded SOIC