SC1404
Mobile Multi-Output PWM Controller with Virtual Current Sense™

POWER MANAGEMENT

Description

The SC1404 is a multiple-output power supply controller designed to power battery operated systems. The SC1404 provides synchronous rectified buck converter control for two power supplies. An efficiency of 95% can be achieved. The SC1404 uses Semtech's proprietary Virtual Current Sense™ technology along with external error amplifier compensation to achieve enhanced stability and DC accuracy over a wide range of output filter components while maintaining fixed frequency operation. The SC1404 also provides two linear regulators for system housekeeping. The 5V linear regulator takes its input from the battery; for efficiency, the output is switched to the 5V output when available. The 12V linear regulator output is generated from a coupled inductor off the 5V switching regulator.

Control functions include: power up sequencing, soft start, power-good signaling, and frequency synchronization. Line and load regulation is to +/-1% of the output voltage. The internal oscillator can be adjusted to 200 kHz or 300 kHz or synchronized to an external clock. The MOSFET drivers provide >1A peak drive current for fast MOSFET switching.

The SC1404 includes a PSAVE# input to select pulse skipping mode for high efficiency at light load, or fixed frequency mode for low noise operation.

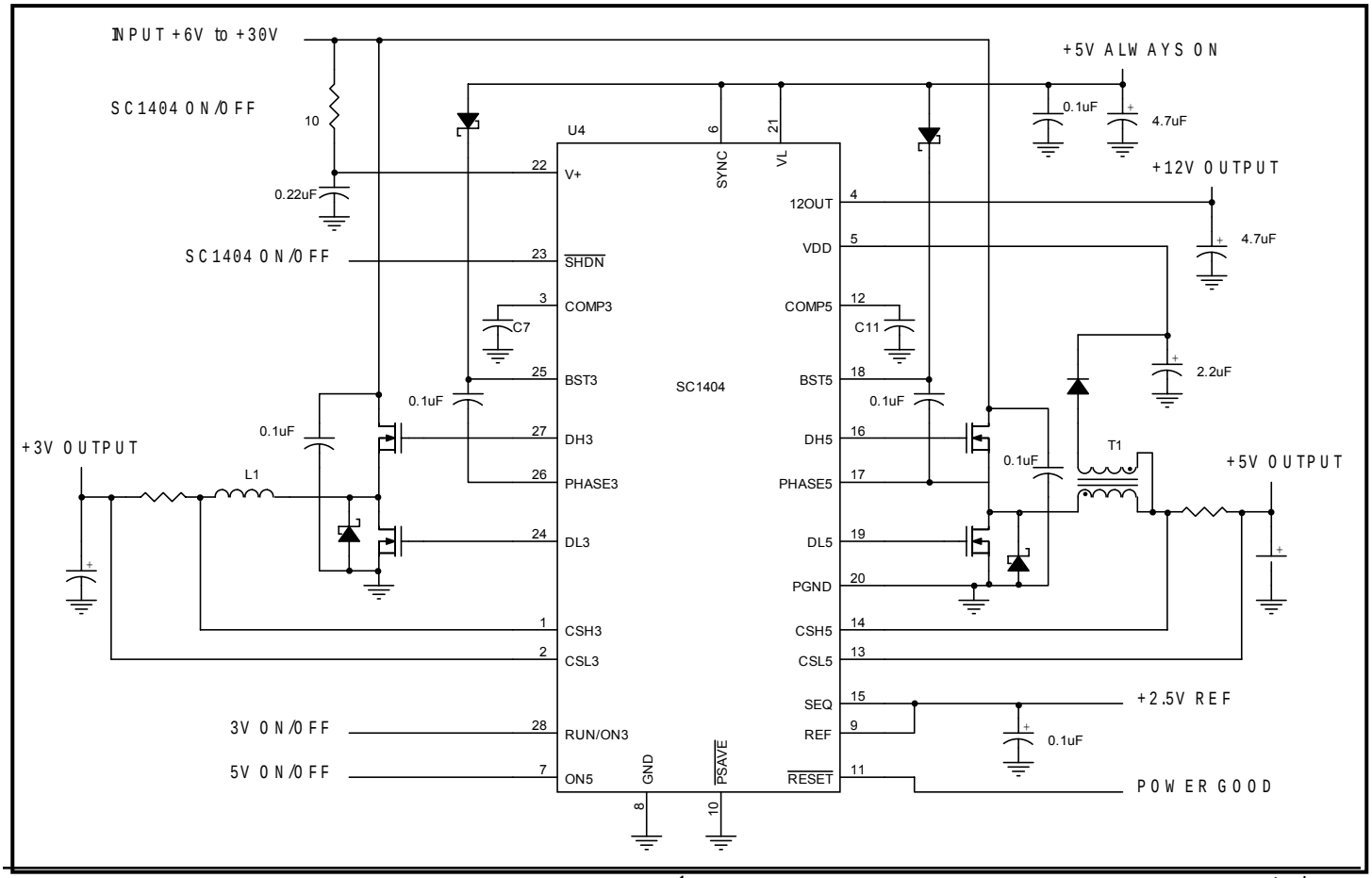
Features

- 6 to 30V input range (operation possible below 6V)
- 3.3V and 5V dual synchronous outputs
- Fixed-frequency or PSAVE for maximum efficiency over wide load current range
- 5V/50mA linear regulator
- 12V/200mA linear regulator
- Virtual Current Sense™ for enhanced stability
- Accurate low-loss current limiting
- Out-of-phase switching reduces input capacitance
- External compensation supports wide range of output filter components for reduced cost
- Programmable power-up sequence
- Power Good output
- Output overvoltage & overcurrent protection with output undervoltage shutdown
- 4µA typical shutdown current
- 6mW typical quiescent power

Applications

- Notebook and Subnotebook Computers
- Automotive Electronics
- Desktop DC-DC Converters

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

PARAMETER	DESCRIPTION	MAXIMUM	UNITS
VDD, V+, PHASE3, PHASE5 to GND	Supply and Phase Voltages	-0.3 to +30	V
PHASE3, PHASE5 to GND	Phase Voltages	-2.0 (transient - 100 nsec)	V
BST3, BST5, DH3, DH5 to GND	Boost voltages	-0.3 to +36	V
PGND to GND	Power Ground to Signal Ground	± 0.3	V
VL to GND	Logic Supply	-0.3 to +6	V
BST3 to PHASE3; BST5 to PHASE5;	High-side Gate Drive Supply	-0.3 to +6	V
DH3 to PHASE3; DH5 to PHASE5	High-side Gate Drive Outputs	-0.3 to (+BSTx + 0.3)	V
DL3, DL5 to GND CSL5, CSH5, CSL3, CSH3 to GND	Low-side Gate Drive Outputs and Current Sense inputs	-0.3 to +(VL + 0.3)	V
REF, SYNC, SEQ, PSAVE#, ON5, RESET#, VL, FB3, FB5, COMP3, COMP5 to GND	Logic inputs/outputs	-0.3 to +(VL + 0.3)	V
ON3, SHDN# to GND		-0.3 to +(V+ + 0.3V)	V
VL, REF Short to GND		Continuous	
REF Current		+5	mA
VL Current		+50	mA
12OUT to GND		-0.3 to (+VDD + 0.3)	V
12OUT Short to GND		Continuous	
12OUT Current	12V output current	+200	mA
T_J	Junction Temperature Range	+150	°C
Package Thermal Resistance	junction to ambient	76	°C/Watt
T_S	Storage Temperature Range	-65 to +200	°C
T_L	Lead Temperature	+300 °C, 10 second max.	°C

Electrical Characteristics

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A =-40 to 85°C.
Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CODE	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SMPS CONTROLLERS						
Input Voltage Range	VIN		6		30.0	V
3V Output Voltage	V3OUT	V+ = 6.0 to 30V, 3V load = 0A to current limit	3.23	3.3	3.37	V
5V Output Voltage	V5OUT	V+ = 6.0 to 30V, 5V load = 0A to current limit	4.9	5.0	5.1	V
Load Regulation	V3LDRG V5LDRG	Either SMPS, 0A to current limit, PSAVE# = VL		-0.4		%
Line Regulation	V3LIRG V5LIRG	Either SMPS, 6.0 < V+ < 30V, PSAVE# = VL		0.05		%/V

Electrical Characteristics Cont.

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A =-40 to 85°C.
Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CODE	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Thresholds (Note 2)	I3LIMP I5LIMP I3LIMN I5LIMN	CSH_X - CSL_X (positive current) CSH_X - CSL_X (negative current)	40	55 -50	70	mV
Zero Crossing Threshold	ZC3 ZC5	CSH_X - CSL_X PSAVE# = 0V, not tested		5		mV
Soft-Start Ramp Time		From enable to 95% full current limit, with respect to f_{OSC}		512		clks
Oscillator Frequency	FOSCHI FOSCLO	SYNC = VL SYNC = 0V	220 170	300 200	380 230	kHz
Maximum Duty Factor	DF3MAX DF5MAX	SYNC = VL SYNC = 0V	92 94	94 96		%
SYNC Input High Pulse		Not tested		300		ns
SYNC Input Low Pulse Width		Not tested		300		
SYNC Rise/Fall Time		Not tested		200		
SYNC Input Frequency Range	SYNCRG			240 - 350		kHz
Current-Sense Input Leakage Current	ICSH3 ICSH5	CSH3 = 3.3V, CSH5 = 5.0V		3	10	µA
ERROR AMP						
DC Loop Gain	DCG3, DCG5	From internal feedback node to COMP3/COMP5		18		V/V
Gain Bandwidth Product				8		MHz
Output Resistance	RC3, RC5	COMP3, COMP5		25		Kohms
INTERNAL REGULATOR AND REFERENCE						
VL Output Voltage	VLOUT	SHDN# = V+; 6V < V+ <30V, 0mA <I_{LOAD}< 30mA, ON3 = ON5 = 0V	4.6		5.25	V
VL Undervoltage Lockout Fault Threshold	VLUV	Falling edge, hysteresis = 0.7V	3.5	3.7	4.1	
VL Switchover Lockout	VLSW	Switchover at startup - rising edge		4.5		
REF Output Voltage	REFOUT	No external load	2.45	2.5	2.55	
REF Load Regulation	REFLD1	0µA < I_{LOAD} < 50µA			12.5	mV
	REFLD2	0mA < I_{LOAD} < 5mA			50	

Electrical Characteristics Cont.

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A =-40 to 85°C.
Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CODE	CONDITIONS	MIN	TYP	MAX	UNITS
REF Sink Current	IREFSK	10mV rise in REF voltage		10		µA
REF Fault Lockout Voltage	REFUV	Falling edge	1.8		2.2	V
V+ Operating Supply Current	IVPOP	VL switched over to VOUT5, 5V SMPS on, I_{LOAD5} = I_{LOAD3} = 0A, PSAVE# = 0V		10	50	µA
V+ Standby Supply Current	IVPSB	V+ = 6V to 30V, both SMPS off, PSAVE# = 0V; includes current into SHDN#		300		
V+ Shutdown Supply Current	IVPSD	V+ = 6V to 30V, SHDN# = 0V	-1	3	15	
Quiescent Power Consumption	PQ	SMPS enabled, No Load on SMPS		6		mW
FAULT DETECTION						
Overvoltage Trip Threshold	V3OV, V5OV	With respect to unloaded output voltage	7	10	15	%
Overvoltage-Fault Propagation Delay		Output driven 2% above overvoltage trip V_{TH}		1.5		µs
Output Undervoltage Threshold	V3UV, V5UV	With respect to unloaded output voltage	65	75	85	%
Output Undervoltage Lockout Time	V3UVTO V5UVTO	From each SMPS enabled, with respect to f_{OSC}	5000	6144	7000	clks
Thermal Shutdown Threshold		Typical hysteresis = 10°C		+150		°C
RESET#						
RESET# Trip Threshold	V3RST V5RST	With respect to unloaded output voltage, falling edge; typical hysteresis = 1%	-12	-9	-5	%
RESET# Propagation Delay		Falling edge, output driven 2% below RESET# trip threshold		1.5		µs
RESET# Delay Time	T3RSDL T5RSDL	With respect to f_{OSC}	27,000	32,000	37,000	clks
INPUTS AND OUTPUTS						
Logic Input Low Voltage	VIO3, VIOP, VIO5, VIOSD, VIOSN	ON3, PSAVE#, ON5, SHDN#, SYNC (SEQ = REF)			0.6	V
Logic Input High Voltage	VIH3, VIHP, VIH5, VIHSD, VIHSN	ON3, PSAVE#, ON5, SHDN#, SYNC (SEQ = REF)	2.4			V

Electrical Characteristics Cont.

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A =-40 to 85°C.
Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CODE	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current PSAVE#, ON5, SYNC	ILP, IL5, ILSN	SEQ = REF	-1		+1	µA
Input Leakage Current - ON3	IL3	ON3 = 15V	-2		+2	µA
Input Leakage Current SHDN#	ILSD	SHDN# = 15V	-1	3	+10	µA
Logic Output Low Voltage	VORSTL	RESET#, ISINK = 4mA			0.4	V
Logic Output High Current	IORSTH	RESET# = 3.5V		1		mA
ON5 Pull-down Resistance	RON5	ON5, ON3 = 0V, (SEQ = REF)		100		Ω
Gate Driver Sink/Source Current	IDL3, IDH3, IDL5, IDH5	DL3, DH3, DL5, DH5, forced to 2.5V		1		A
Gate Driver On-Resistance	RGBH3, RGHP3, RGBH5, RGHP5, RGVL3, RGLG3 RGVL5, RGLG5	BST3 to DH3, DH3 to PHASE3, BST5 to DH5, DH5 to PHASE5, VL to DL3, DL3 to PGND, VL to DL5, DL5 to PGND		1.5	7	Ω
Non-Overlap Threshold	ZNOVT	PHASE3, PHASE5 to GND		1.0		V
Shoot-through (Non-Overlap) Delay		DHx falling edge to DLx rising edge DLx falling edge to DHx rising edge (1V threshold on DHx and DLx, no external capacitance on DL or DH)	10 35	17 75	25 115	nsec nsec
12V LINEAR REGULATOR						
VDD Shunt Threshold	VDDSHN	Rising edge, hysteresis = 5%	17		21	V
VDD Shunt Current	IVDDST	VDD = 20V	5	10	30	mA
VDD Leakage Current	IVDDLK	VDD = 5V, Standby mode			30	µA
12OUT Output Voltage	VOUT12	0mA < Load < 200mA	11.55	12.1	12.75	V
12OUT Current Limit	ILIM12	12OUT forced to 11V, VDD = 13V	200			mA
12OUT Regulation Threshold	V12THR	Falling edge		11.9		V
Quiescent VDD Current	I12Q	VDD = 18V, run mode, no 12OUT load		80	100	µA

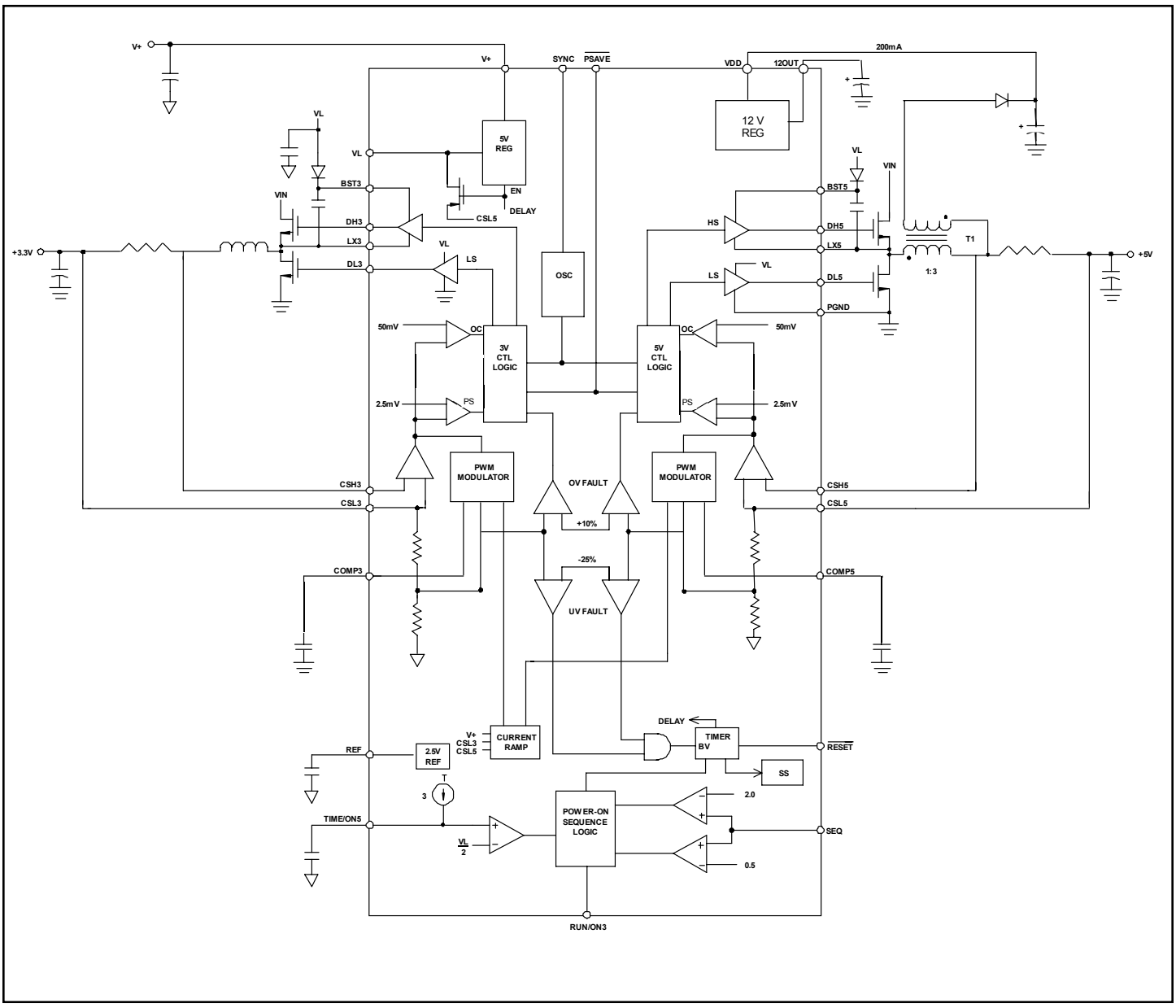
Notes:
(1) This device is ESD sensitive. Use of standard ESD handling procedures required.
(2) Applicable from 0 to +85°C.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	CSH3	Current limit sense input for 3V SMPS. Connect to the inductor side of a current sense resistor.
2	CSL3	Output voltage sense input for 3V SMPS. Connect to the output side of a current sense resistor.
3	COMP3	The output of the 3.3V SMPS error amplifier.
4	12OUT	12V internal linear regulator output.
5	VDD	Supply voltage input for the 12OUT linear regulator. Also connects internally to a 18V overvoltage shunt regulator clamp.
6	SYNC	Oscillator Synchronization and Frequency Select. Tie to VL for 300 kHz operation; tie to GND for 200 kHz. Drive externally to synchronize to an external oscillator between 240 kHz and 350 kHz.
7	ON5	5V ON/OFF Control Input.
8	GND	Low noise Analog Ground and Feedback reference point.
9	REF	2.5 V Reference Voltage output. Bypass to GND with 1 µF minimum.
10	PSAVE#	Logic input that disables PSAVE Mode when high. Connect to GND for normal use.
11	RESET#	Active-low timed Reset output. RESET# swings from GND to VL. RESET# goes high after a fixed 32,000 clock cycle delay following power up.
12	COMP5	The output of the 5V SMPS error amplifier.
13	CSL5	Output voltage sense input for 5V SMPS. Connect to the output side of a current sense resistor.
14	CSH5	Current limit sense input for 5V SMPS. Connect to the inductor side of a current sense resistor.
15	SEQ	Input that selects SMPS power-up sequence and selects monitor voltage(s) used by RESET#.
16	DH5	Gate Drive Output for the 5V, high-side N-Channel switch.
17	PHASE5	5V switching node (inductor) connection.
18	BST5	Boost capacitor connection for 5V high-side gate drive.
19	DL5	Gate drive output for the 5V low-side synchronous rectifier MOSFET
20	PGND	Power Ground.
21	VL	5 V internal linear regulator output.
22	V+	Battery Voltage input.
23	SHDN#	Shutdown control input - active low.
24	DL3	Gate drive output for the 3V low-side synchronous rectifier MOSFET.
25	BST3	Boost capacitor connection for 3V high-side gate drive.
26	PHASE3	3V switching node (inductor) connection.
27	DH3	Gate drive output for the 3V high-side N-Channel switch.
28	ON3	3V ON/OFF Control Input.

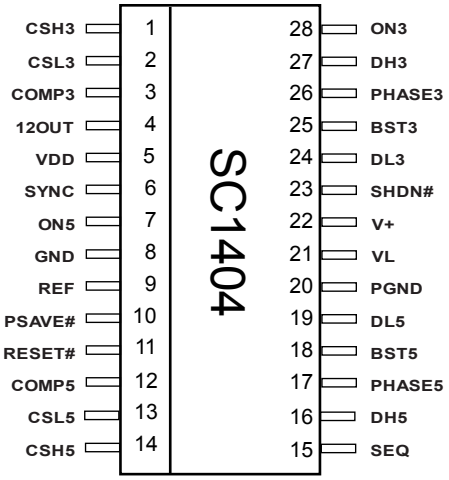
Note: All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Pin Configuration

Top View



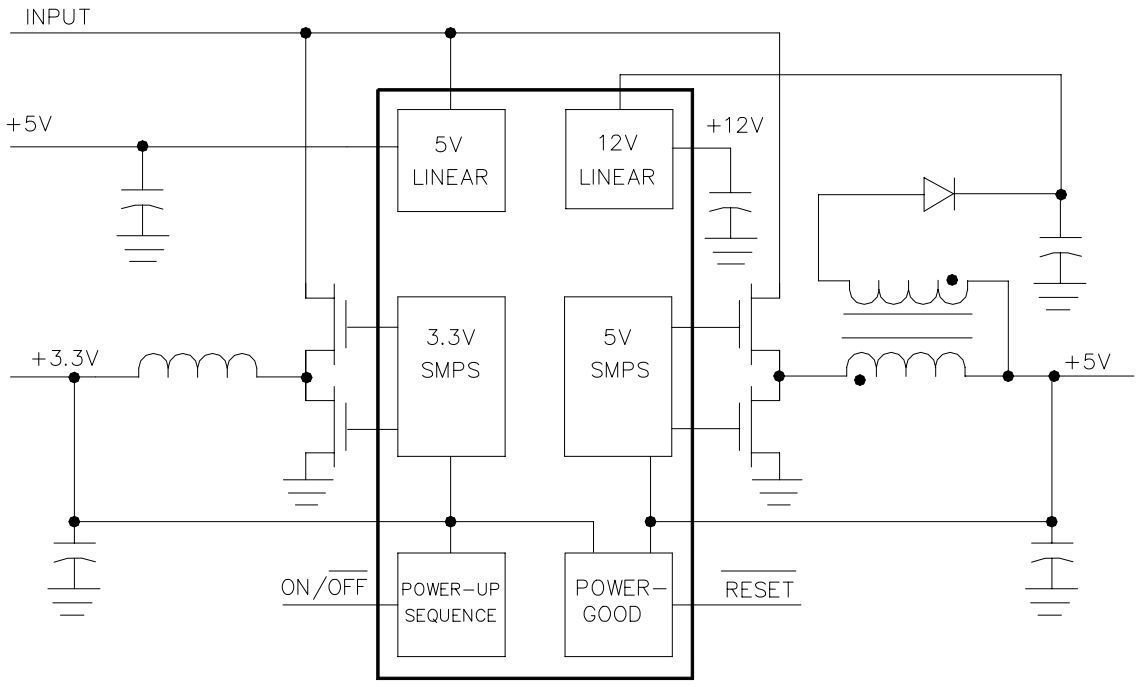
TSSOP-28/SSOP-28

Ordering Information

DEVICE	PACKAGE	TEMP. (T_{AMB})
SC1404ITSTR	TSSOP-28	-40 - +85°C
SC1404ISSTR	SSOP-28	

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Block Diagram



Functional Information

Detailed Description

The SC1404 is a versatile multiple-output power supply controller designed to power battery operated systems. Out-of-phase switching improves signal quality and reduces input RMS current, thereby reducing the size of input filter capacitors (see Out-of-Phase Switching). The SC1404 provides synchronous rectified buck control in fixed-frequency forced-continuous mode and in hysteretic PSAVE mode, for two switching converters over a wide load range. The two switchers have on-chip preset output voltages of 5.0V and 3.3V. The control and fault monitoring circuitry for each PWM controller includes digital softstart, turn-on sequencing, voltage error amplifier with built-in slope compensation, pulse width modulator, power save, over-current, over-voltage and under-voltage fault protection. Two linear regulators and a precision reference voltage are also provided. The 5V/50mA linear regulator (VL supply) which powers the SC1404 and gate drivers operates from the battery (V+ supply). If the 5V converter is running, the SC1404 disables the linear regulator and connects the VL supply to the 5V output through an internal switch. The operating current for the SC1404 and gate drivers then comes from the more efficient 5V converter. The 12V/200mA linear regulator can supply 200mA. Semtech's proprietary Virtual Current Sense™ provides advantages in stability and signal to noise ratio compared to conventional current sensing.

PWM control

There are two separate PWM control blocks for the 3V and 5V switchers. They are switched out-of-phase with each other. The interleaved topology offers advantages over in-phase solutions. It reduces steady state input filter requirements by reducing current drawn from the filter capacitors. To avoid both switchers switching simultaneously, there is a built-in time delay between the two switchers, the amount of which depends on the input voltage (see Out-of-Phase Switching). The PWM provides two modes of control over the entire load range: 1 - Forced continuous conduction mode as a fixed-frequency peak current mode controller with falling edge modulation, and 2 - Hysteretic Power-save mode. Current sense is done differently than that in the conventional peak current mode control. Semtech's proprietary Virtual Current Sense™ emulates the necessary inductor current information for proper functioning of the IC.

When the switcher operates in continuous conduction mode, the high-side MOSFET turns on the beginning of each switching cycle. It is turned off when the desired duty cycle is reached. Active shoot-through protection will delay the low-side MOSFET turn-on until the phase node drops below 1.0 V. The low-side MOSFET then remains on until the beginning of the next switching cycle. Again, active shoot-through protection ensures that the gate to the low-side MOSFET has dropped low before the high-side MOSFET is turned on.

Under light load conditions when the PSAVE pin is low, the SC1404 operates as a hysteretic controller in discontinuous conduction mode to reduce switching frequency and switching bias current. The switching frequency then is determined by the hysteretic trip voltage set around the reference. When entering PSAVE# mode, if the minimum (valley) inductor current as measured across the CSH and CSL pins is below the PSAVE# threshold for four switching cycles, the virtual current sense circuitry is shutdown and PWM control switches from forced continuous to hysteretic mode. If the minimum (valley) inductor current is above the threshold for four switching cycles, PWM control changes from hysteretic to forced continuous mode. The SC1404 provides built-in hysteresis to prevent chattering between the two modes of operation.

Gate Drive / Control

The SC1404 gate drivers are designed to switch large MOSFETs up to 350KHz. The high-side gate driver is required to drive the gate of high-side MOSFETs above the V+ input. The supply for the gate drivers is generated by charging a boostrap capacitor from the VL supply while the low-side driver is on. Monitoring circuitry ensures that the bootstrap capacitor is charged when coming out of shutdown or fault conditions where the bootstrap capacitor may be depleted. In continuous conduction mode, the low-side driver output that controls the low-side MOSFET is on when the high-side driver is off. Under light load conditions when the PSAVE# input is low, the inductor ripple current will approach the point where it reverses polarity. This is detected by the low-side driver control and the low-side MOSFET is turned off before the current goes significantly negative and causes energy drain from the output. The low-side driver operation is also affected by various fault conditions as described in the Fault Protection section.

External Compensation

The COMP pin allows external compensation of the feedback loop. This allows greater flexibility when choosing output filters, resulting in reduced cost and smaller size compared to a fixed compensation approach. A nominal gain of 18 for the error amplifier improves the system loop gain and output transient response.

Internal Bias Supply

The VL linear regulator provides a 5V output that powers the gate drivers, 2.5V reference, and internal controls of the SC1404. The VL supply can provide up to 50mA, but this must include MOSFET gate drive current. The VL pin should be bypassed to GND with 4.7uF to supply the peak gate drive curents. The VL regulator receives input power from the V+ battery input. Efficiency is improved by providing a boot-strap for the VL bias. When the 5V SMPS output voltage reaches 5V, internal circuitry detects this condition and turns on a PMOS pass device between CSL5 and VL. The internal VL regulator is then disabled and the VL bias is provided by the high efficiency 5V switcher.

Functional Information

The REF output is accurate to +/- 2% over temperature. It is capable of delivering 5mA max and should be bypassed with 1uF minimum. Loading the REF pin will reduce the REF voltage slightly.

Loading Resistance (Ω)	511	2.67K	49.9K	255K	1Meg
Deviation from Vref = 2.4920V	8.3mV	3.1mV	0.5mV	0.3mV	0mV

Current Sense (CSH, CSL)

The output current of the power supply is sensed as the voltage drop across an external resistor between the CSH and CSL pins. Overcurrent is detected when the current sense voltage exceeds +/- 50mV. A positive overcurrent will turn off the high-side driver, a negative overcurrent will turn off the low-side driver; each on a cycle-by-cycle basis.

Oscillator

When the SYNC pin is set high the oscillator runs at 300KHz; when SYNC is set low the frequency is 200KHz. The oscillator can also be synchronized to the falling edge of a clock on the SYNC pin with a frequency between 240KHz and 350KHz. In general, 200KHz operation is used for highest efficiency while 300KHz leads to less output ripple and/or smaller filter components.

Fault Protection

In addition to cycle-by-cycle current limit, the SC1404 monitors over-temperature, and output overvoltage and undervoltage conditions. The overtemperature detection will shut the part down if the die temperature exceeds 150°C with 10°C of hysteresis.

If either SMPS output is more than 10% above its nominal value, both SMPS are latched off and the low-side MOSFETS are latched on. To prevent the output from ringing too far below ground in a fault condition, a 1A Schottky diode should be placed across each output. Two different levels of undervoltage are detected. If the output falls 10% below its nominal output, the RESET# output is pulled low.If the output falls 25% below its nominal output following a start-up delay, both SMPS are latched off. Both of the latched fault modes persist until SHDN# or ON3 is toggled, or the V+ input is brought below 1V.

Shutdown and Operating Modes

Holding the SHDN# pin low disables the SC1404, reducing the V+ input current to less than 10uA. When SHDN goes high, the part enters a standby mode where the VL regulator and VREF are enabled. Turning on either SMPS will put the SC1404 in run mode.

SHDN#	ON3	ON5	MODE	DESCRIPTION
Low	X	X	Shut-down	Minimum bias current
High	Low	Low	Standby	VREF and VL regulator enable
High	High	High	Run Mode	Both SMPS Running

Power up Controls and Soft Start

The user has control of the SC1404 RESET# by setting the SEQ, ON3 and ON5 pins as described in the following table.

At startup, the RESET# pin is held low for 32K switching cycles. Another timer is used to enable the undervoltage protection. The undervoltage protection circuitry is enabled after 6144 switching cycles, at which time the SMPS should be in regulation.

When SEQ is set to REF, the RESET# only monitors the 3.3V SMPS and the 5V SMPS is ignored.

Each SMPS contains its own counter and DAC to gradually increase the current limit at startup to prevent surge currents. The current limit is increased from 0, 20%, 40%, 60%, 80%, to 100% linearly over the course of 512 switching cycles.

12OUT Supply

The 12OUT linear regulator is capable of supplying 200mA. The input voltage to the 12OUT regulator is generated by a secondary winding on the 5V SMPS inductor.

A heavy load on the 12OUT regulator when the 5V SMPS is in PSAVE will cause the VDD input to drop, browning out the regulator. If the output drops 0.8% from its nominal value, the 5V SMPS is forced out of PSAVE mode and into continuous conduction mode for several cycles. This recharges the bulk input capacitor on the VDD. The 12OUT linear regulator also has a current limit to prevent damage under short circuit conditions.

Over-voltage protection is provided on the VDD input. If the VDD input is above 19V, an over-voltage is detected and a 10mA current shunt load is applied to VDD. The over-voltage threshold has a 0.5V hysteresis.

Functional Information

SC1404 Startup Sequence Chart

SEQ	ON3	ON5	RESET#	DESCRIPTION
REF	LOW	LOW	Follows 3.3V SMPS.	Independant start control mode. Both SMPSs off.
REF	LOW	HIGH	Low.	5V SMPS ON, 3.3V SMPS OFF.
REF	HIGH	LOW	Follows 3.3V SMPS.	3.3V SMPS ON, 5V SMPS OFF.
REF	HIGH	HIGH	Follows 3.3V SMPS.	Both SMPSs on.
GND	LOW	X	Low.	Both SMPSs off.
GND	HIGH	HIGH/LOW	High after both outputs are in regulation.	5V starts when ON3 goes high. If ON5= HIGH, 3V is on. IF ON5 = LOW, 3V is off.
VL	LOW	X	Low.	Both SMPSs off.
VL	HIGH	HIGH/LOW	High after both outputs are in regulation.	3V starts when ON3 goes high. If ON5 = HIGH, 5V is on. IF ON5 = LOW, 5V is off.

Applications Information

Reference Circuit Design

Introduction

The SC1404 is a versatile dual switching regulator with fixed 5V and 3.3V outputs . In addition, there is an on-chip 5V linear regulator capable of supplying 50mA output current and a 12V linear regulator able to provide 200mA. The SC1404 is designed for notebook applications but has is suited to applications where high efficiency, small package, and low cost are required.

Design Guidelines

The schematic for the reference circuit is shown on page 22. The reference circuit is configured as follows:

Switching Regulator 1	Vout1 = 3.3V @ 6A
Switching Regulator 2	Vout2 = 5.0V @ 6A
Linear Regulator 1	Vout3 = 12V, 200mA
Linear Regulator 2	Vout3 = 5.0V @ 50mA

Designing the Output Filter

Before calculating the output filter inductance and output capacitance, an acceptable amount of output ripple current must be determined. The maximum allowable ripple current depends on the transient requirement of the power supply. Under normal situation, the ripple current is usually set around 10 to 20% of the maximum load. However, in order to speed up the output transient response, ripple current can be much higher. In this design, we are going to set the ripple current to be 40% of maximum load. So once the ripple voltage specification is determined, the capacitor ESR is chosen. The output ripple voltage is usually specified at +/- 1% of the output voltage.

For the reference circuit 3.3V switcher, we selected a maximum ripple voltage of 33mV. Choosing one 180uF, 4V Panasonic SP Polymer Aluminum Electrolytic Cap, of which ESR is 15 $m\Omega$, sets the maximum ripple current as follows:

$$\Delta I_O = \frac{\Delta V_{O\_MAX}}{ESR} \qquad \Delta I_O = \frac{0.033V}{0.015\Omega} = 2.2A$$

Checking to see if the maximum RMS current can be met by the SP cap.

$$I_{RMS} = \sqrt{\frac{I_1^2 + I_1 \cdot I_2 + I_2^2}{3}} \qquad I_1 = -\frac{\Delta I_O}{2} \qquad I_2 = +\frac{\Delta I_O}{2}$$

Irms=0.635 A << Irms_rated=3.0A

The output inductance can now be found by:

$$L_O = \frac{(V_{IN\_NOM} - V_O) \cdot D_{NOM} \cdot T_S}{\Delta I_O}$$

Applications Information

where Vin_nom=15V, Vo=3.3V, D=Vo/Vin_nom, Fs=300KHz, Ts=3.33uS and **Δ**Io=2.2 A. Lo is then calculated to be 3.9uH. For the interest of this design, Lo is chosen to be 4.7uH for the 3.3V output. For the 5V output, a coupled inductor with 6.4uH primary (5V winding) inductance is used.

Choosing Current Sense Resistor

Since the SC1404 implements Virtual Current Sense™, an external current sense resistor is not needed by the control loop. But it is required for cycle-by-cycle current limit. Cycle-by-cycle current limit is reached when the voltage across the current sense resistor exceeds 50mV nominal. Depending on the system requirement, this current limit can vary, it is usually 10 to 30% higher than the maximum load. Taking into consideration lower limit of the 50mV, the value of the current sense resistor can be calculated using the following equation:

$$R_{SENSE} = \frac{40mV_{(min)}}{I_{PK\_OC}}$$

For a DC OC trip point between 8 to 12A, Rsense is chosen to be 5m Ω.

Choosing the Main Switching MOSFET

Before choosing the main switch MOSFET, we need to know two critical parameters: voltage and current rating. In order to minimize the conduction loss, we recommend using the lowest Rds(on) for the same voltage and current rating. The maximum drain to source voltage of the switch MOSFET is mainly decided by the topology of the switcher. Since this is a buck topology,

$V_{DS\_MAX} = V_{IN\_MAX} = 21V$

Applying a derating of 70%, a 30V MOSFET is used in the design. The peak current of the MOSFET is determined by

$$I_{PEAK} = \frac{60mV}{5.5m\Omega} = 11A$$

According to the calculated voltage and current rating, Si4886DY, IRF7413, FDS9412 or STS12NF30L meets the requirement. The specs for these MOSFETs are listed in the table below. For the purpose of this exercise, STS12NF30L is chosen. Next step is to determine its power handling capability. Based on 85 °C ambient temperature, 150 °C junction temperature and 50 °C /W thermal resistance, its power handling is calculated as follows:

T_J = 150°C; T_A = 85°C; θ_{JA}= 50°C/W

$$P_T = \frac{T_J - T_A}{\theta_{JA}} = \frac{150 - 85}{50} = 1.30W$$

Vendor P/N	VDS (V)	ID (A)	Rds(On) @ 4.5V (ohm)	Package
Si4886DY	30	13	0.0135	so-8
IRF7413	30	13	0.011	so-8
FDS9412	30	7.9	0.036	so-8
STS12NF3-0L	30	12	0.0085	so-8

The following calculations are done to verify that the power dissipation of the main switch MOSFET is well within 1.86W, which is the maximum allowable power dissipation for the package.

$$P_{TOTAL\_DISS} = P_{CONDUCTION} + P_{SWITCHING} + P_{GATE}$$

$$P_{CONDUCTION} = R_{ds(on)} \cdot I_{RMS}^2 \cdot D_{nom}$$

where Rds(on) = 0.01 Ω @Tj=25 °C and Vgs = 4.5V. In order to find Rds(on)@ Tj=100 °C, use 1.40*Rds(on)@25 °C. Therefore, Rds(on) @ Tj = 100 °C is equal to 0.014 Ω.

$$I_{RMS} = \sqrt{\left(\frac{I_1^2 + I_1 \cdot I_2 + I_2^2}{3}\right) \cdot D_{nom}}$$

where

$$I_1 = I_{MAX} + \frac{\Delta I_{O\_MAX}}{2} = 7.1A, \quad I_2 = I_{MAX} - \frac{\Delta I_{O\_MAX}}{2} = 4.9A \text{ and}$$

$$D_{nom} = \frac{V_{OUT}}{V_{IN\_NOM}}$$

The worst case conduction loss is calculated to be 25mW. And the switching loss of the MOSFET is given by,

$$P_{SWITCHING} = \frac{C_{RSS} \cdot V_{IN}^2 \cdot f_S \cdot I_{OUT}}{I_G}$$

where Crss is the reverse transfer capacitance of the MOSFET; it is equal to 200pF for STS12NF30L, Ig is the gate driver current; it is equal to 1A for SC1404. And Vin_nom = 15V, fs = 300KHz. The switching loss is calculated to 81mW. And the gate loss is given by,

$$P_{GATE} = \frac{1}{2} \cdot C_G \cdot V^2 \cdot f_S$$

where Cg=11nF, V=5V and fs=300KHz. The gate loss is calculated to be 41mW.

So the total power dissipation is calculated to be 147mW and is well within the maximum power dissipation allowance of the MOSFET. No special heating sinking is required when laying out the MOSFET.

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Designing the Loop

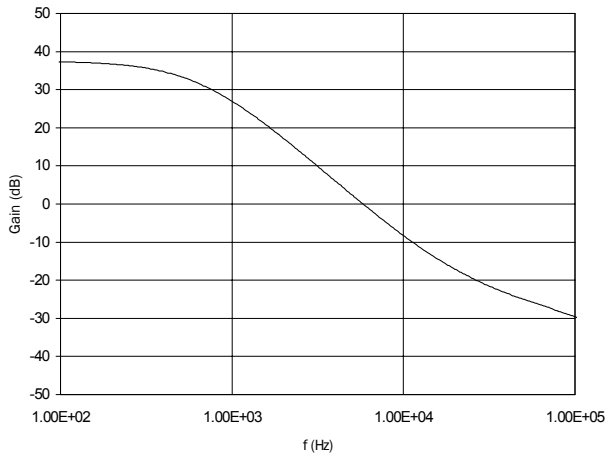
There are two aspects concerning the loop design. One is the power train design and the other is the external compensation design. A good loop design is a combination of the two. In the SC1404, the control-to-output/power train response is dominated by the load impedance, the effective current sense resistor, output capacitance, and the ESR of the output caps. The low frequency gain is dominated by the output load impedance and the effective current sense resistor. Inherent to Virtual Current Sense™, there is one additional low frequency pole sitting between 100Hz and 1KHz and a zero between 15KHz and 25KHz. To compensate for the SC1404 is easy since the output of error amplifier COMP pin is available for external compensation. A traditional pole-zero-pole compensation is not necessary in the design using SC1404. To ensure high phase margin at crossover frequency while minimizing the component count, a simple high frequency pole is often sufficient. In the reference design below, single-pole compensation method is demonstrated. And the loop measurement results are compared to that obtained from the simulation model. Transient response is also done to validate the model. Also, to help speeding up the design process, a list of recommended output caps vs. compensation caps value is given in table I.

Single-Pole compensation Method

Given parameters:
Vin = 19V, Vout = 3.3V @ 2.2A,
Output impedance, Ro = 3.3V/2.2A = 1.5 Ω ,
Panasonic SP cap, Co = 180uF, Resr = 15 mΩ ,
Output inductor, Lo = 4.7uH
Switching frequency, Fs = 300KHz

Simulated Control-to-Output gain & phase response (up to 100KHz) is plotted below

.



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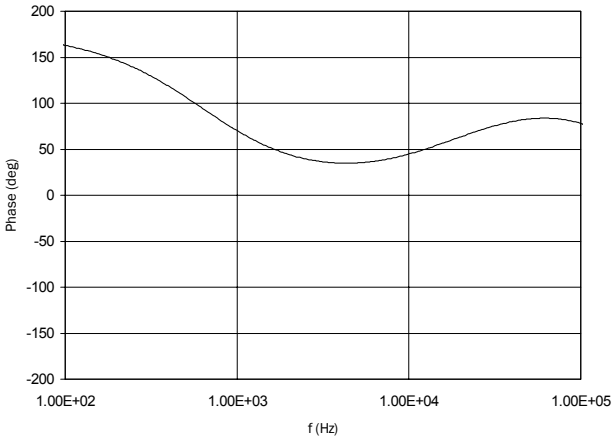
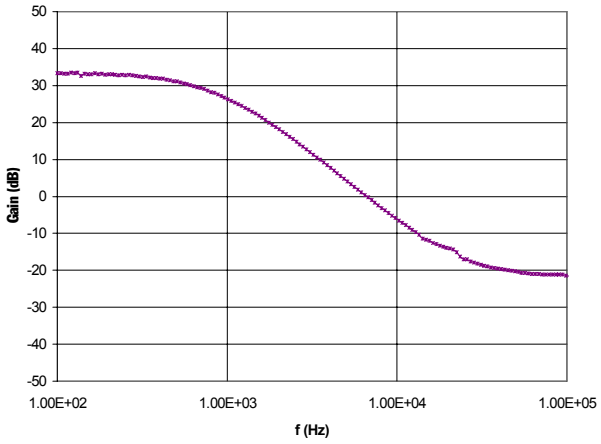
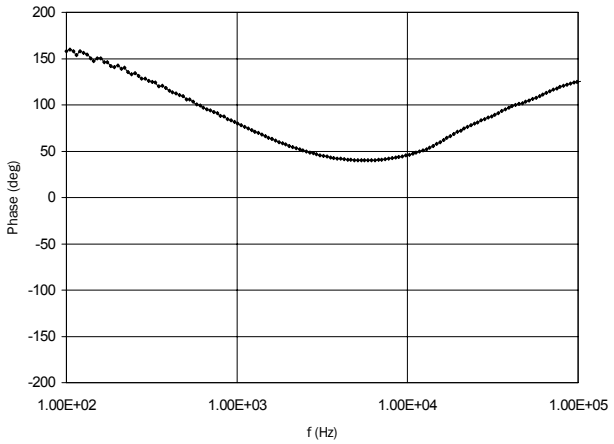


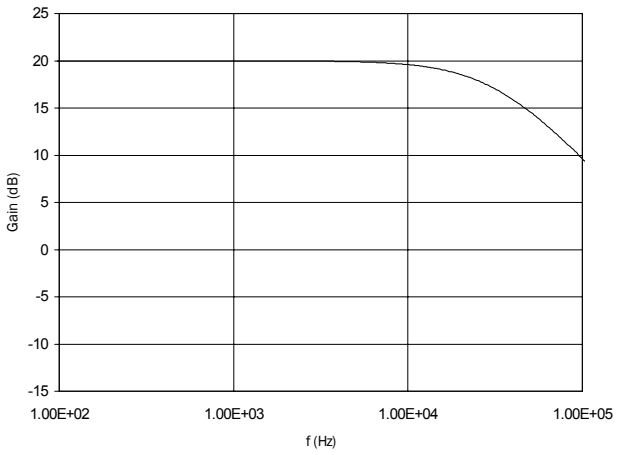
Measured Control-to-Output gain & phase response (up to 100KHz) is plotted below.

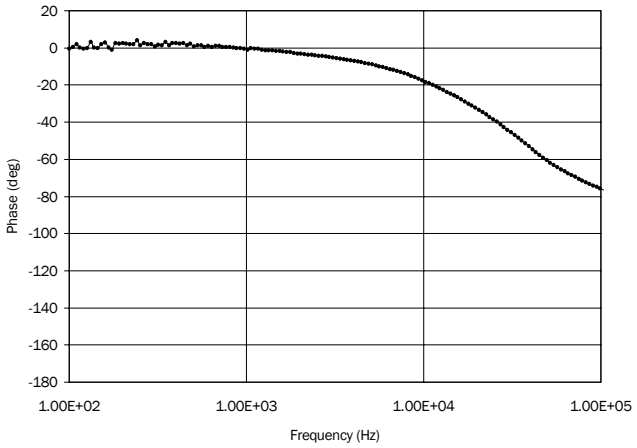




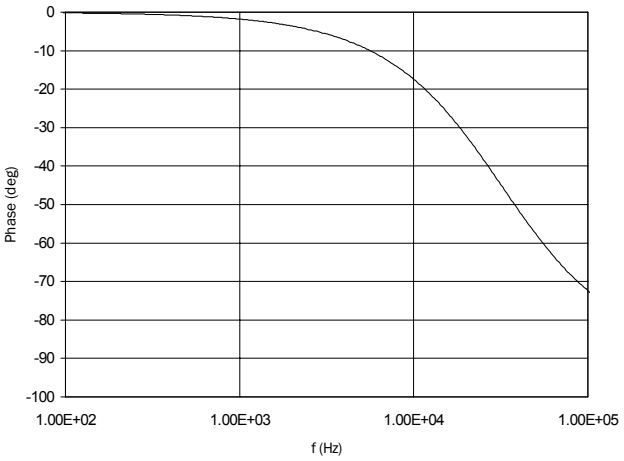
Single-pole compensation of the error amplifier is achieved by connecting a 100pF capacitor from the COMP pin of the SC1404 to ground. The simulated feedback gain & phase response (up to 100KHz) is plotted below.

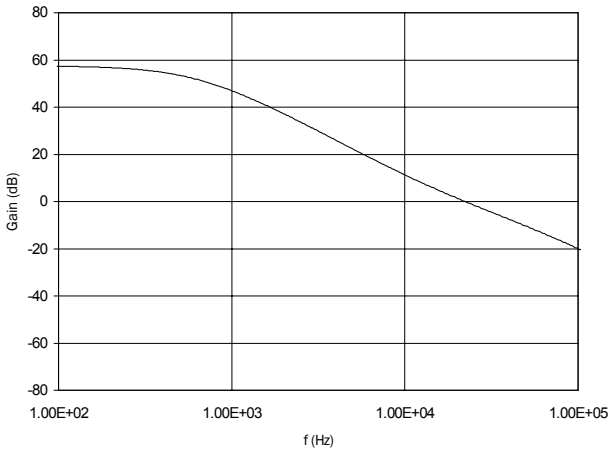
Applications Information



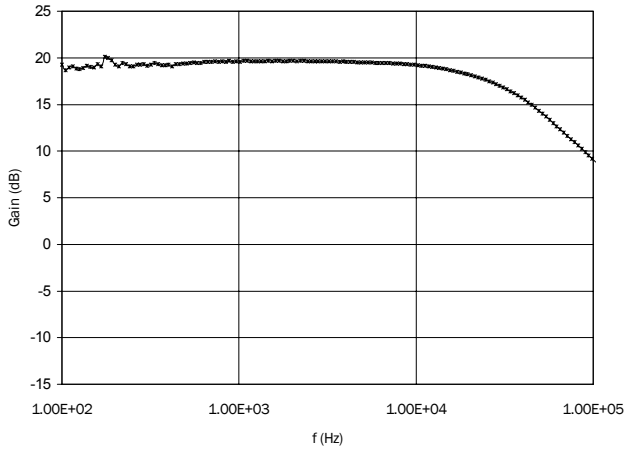


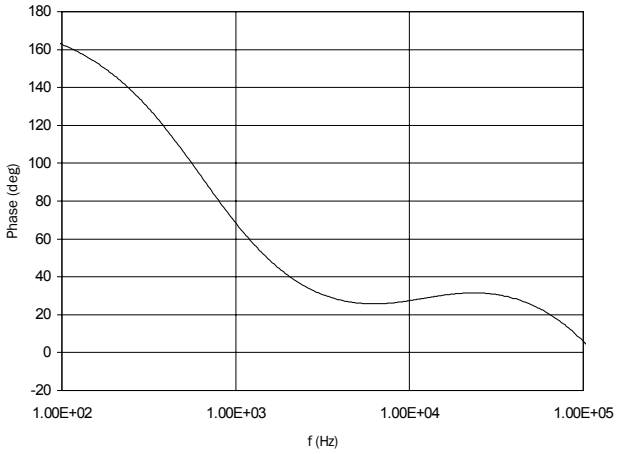
Simulated overall gain & phase responses (up to 100KHz) is plotted below.





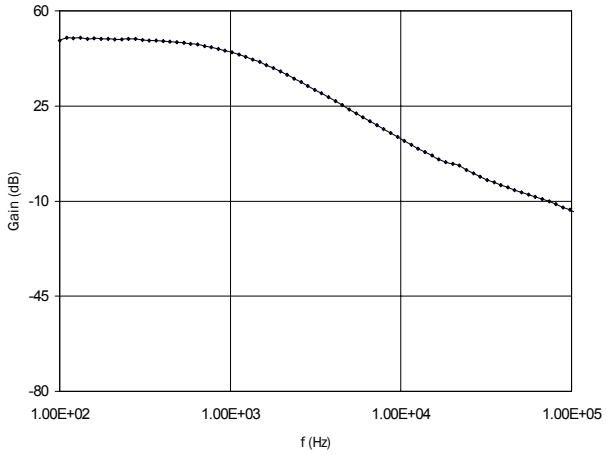
Measured feedback gain & phase responses (up to 100KHz) is plotted below.





Applications Information

Measured overall gain & phase response of the single-pole compensation using SC1404 is plotted below.



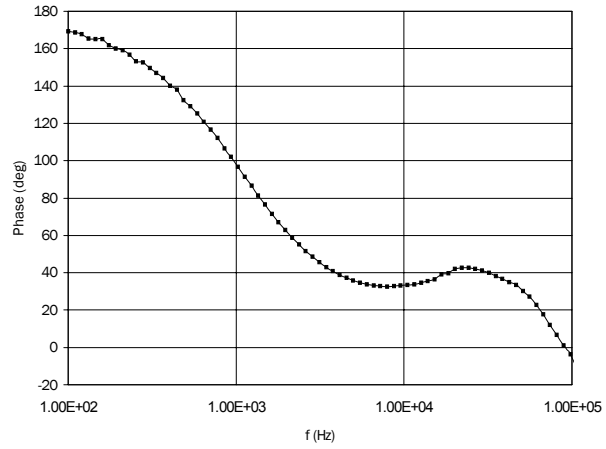


Table I. Recommended compensation cap for different output capacitance.

Output Cap	Recommended Compensation Cap Value
<= 180uF	100pF
>180uF & < 1000uF	200pF
>1000uF	330pF

Table I. is useful only if the following ESR condition is satisfied.

$$f_O = \frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_O}$$

fo > 50KHz

where Resr is the equivalent ESR of the total output caps. For instance, if two Panasonic SP cap 180uF, 15 $m\Omega$ are used. The equivalent Resr = ESR(single)/2 = 7.5 $m\Omega$.

The error amplifier compensation is set by the internal output resistance of the amplifier (25 Kohms typical) and the external impedance attached to the COMP pin. Connecting a single capacitor to the COMP pin places a R-C pole into the error amplifier.

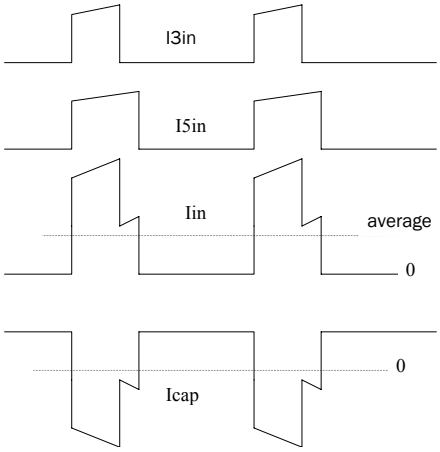
Applications Information

Input Capacitor Selection/Out-of-phase Switching

The SC1404 uses out-of-phase switching between the two converters to reduce input ripple current, enabling the use of smaller, cheaper input capacitors when compared to in-phase switching. The two approaches are shown in the following figures.

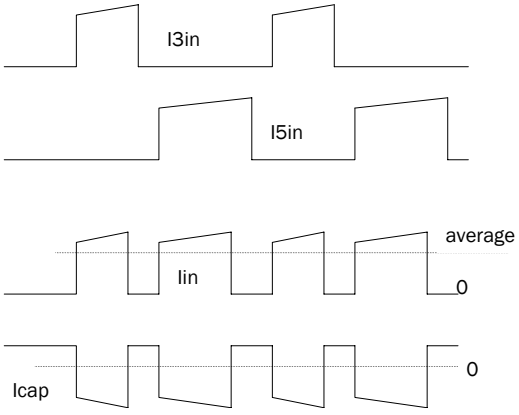
The first figure shows in-phase switching: I3in is the input current drawn by the 3.3V converter, I5in is the input current drawn by the 5V converter. The two converters start each switching cycle simultaneously, resulting in a significant amount of overlap. This overlap increases the peak current. The total input current to the converter is the third trace Iin, which shows how the two currents add together. The fourth trace shows the current flowing in and out of the input capacitors.

In-phase Switching

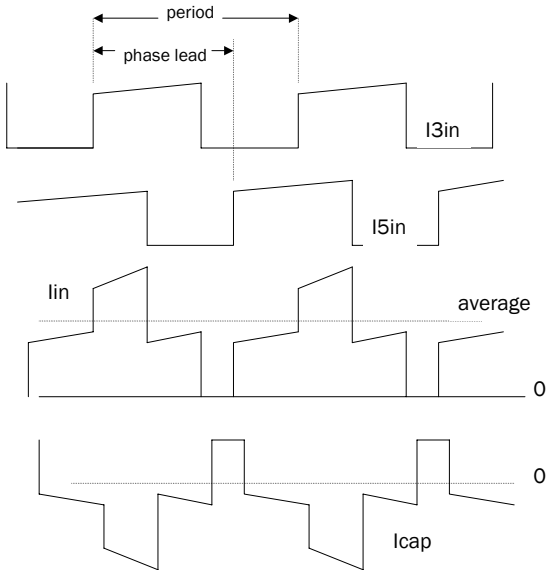


The next figure shows out-of-phase switching. Since the 3.3V and 5V converters are spaced apart, there is no resulting overlap. This results in a two benefits; the peak current is reduced and the frequency content is higher, both of which make filtering easier. The third trace shows the total input current, and the fourth trace shows the current in and out of the input capacitors. The RMS value of this current is significantly lower than the in-phase case and allows for smaller capacitors due to reduced RMS current ratings.

Out-of-phase Switching



As the input voltage is reduced, the duty cycle of both converters increases, as shown in the following figure. For inputs less than 8.3 volts it is impossible to prevent overlap when producing 3.3V and 5V outputs, regardless of the phase relationship between the converters.



From an input filter standpoint it is desirable to minimize the overlap, but it is also desirable to keep the turn-on and turn-off transitions of the two converters separated in time, otherwise the two converters may affect each other due to switching noise. The SC1404 implements this by changing the phase relationship between the converter depending on the input voltage.

Input voltage	Phase lead from 3V converter rising edge to 5V converter rising edge
Vin > 9.6 V	41% of switching period
9.6V > Vin > 6.7V	59% of switching period
6.7 > Vin	64% of switching period

Vin > 9.6V: 3.3V turn-on leads 5V turn-on by 41% of the switching period. With Vin > 9.6V it is always possible to achieve no overlap, which minimizes the input ripple current. At Vin = 9.6V there is no overlap, but the 3.3V turn-on is nearing the 5V turn-off.

6.7 < Vin < 9.6V: 3.3V turn-on leads 5V turn-on by 59% of the period. To prevent the 3V turn-on from coinciding with the 5V turn-off (which could adversely affect either output), the 5V pulse is delayed in time slightly such that the 3V turn-on occurs before the 5V turn-off. This creates a small overlap between the 3V turn-on and the 5V turn-off, with a resulting slight increase in RMS input ripple, but this is preferred since it greatly reduces noise problems caused by simultaneous transitions. Note that at Vin = 6.7, the 3V turn-off is nearing the 5V turn-on.

Vin < 6.7 volts: 3.3V turn-on leads 5V turn-on by 64% of the period. The 5V turn-on is delayed slightly more to add separation between the 3V turn-off and 5V turn-on. This leads to more overlap, but at this point overlap is unavoidable.

Input ripple current calculations: The following equations provide quick approximations for input ripple current:

D3 = 3.3V duty cycle = 3.3/Vin
D5 = 5V duty cycle = 5/Vin
I3 = 3.3V load current
I5 = 5V load current

Dovl = overlapping duty cycle of the 3V and 5V pulses, which varies according to input voltage:

Vin > 9.6V:	Dovl = 0
9.6V > Vin > 6.7V:	Dovl = D5 - 0.41
6.7V > Vin	Dovl = D5 - 0.36

Iin = D3 · I3 + D5 · I5 (average current drawn from Vin)

Isw_rms = rms current flowing into 3V and 5V SMPS

$$(Isw\_rms)^2 = Dovl \cdot (I3 + I5)^2 + (D3 - Dovl) \cdot I3^2 + (D5 - Dovl) \cdot I5^2$$

$$Irms\_cap = \sqrt{Isw\_rms^2 + Iin^2}$$

The worst-case ripple current varies by application. For the case of I3 = I5 = 6A, the worst-case ripple occurs at Vin = 7.5V, at which point the rms capacitor ripple current is 4.2 amps. To handle this the reference design uses 4 paralleled ceramic capacitors, (Murata GRM32NF51E106Z, 10 uF 25V, size 1210). Each capacitor is rated at 2.2 Amps, allowing for derating at higher temperatures.

Choosing Synchronous MOSFET and Schottky diode

Since this is a buck topology, the voltage and current ratings of the synchronous MOSFET are similar to the high-side MOSFET. It makes sense cost-volume-wise to use the same MOSFET for both the main switch and synchronous MOSFET. Therefore, STS12NF30L is used again in the design for synchronous MOSFET. To improve overall efficiency, an external schottky diode is used in parallel to the synchronous MOSFET. The freewheeling current goes into the schottky diode instead of the body diode of the synchronous MOSFET, which usually has very high forward drop and slow transient behavior. It is important when laying out the board to place both the synchronous MOSFET and Schottky diode close to each other to reduce the current ramp-up and ramp-down time due to parasitic inductance between the channel of the MOSFET and the Schottky diode. The current rating of the Schottky diode can be determined by the following equation.

$$I_{F\_AVG} = I_{LOAD} \cdot \frac{100n}{Ts} = 0.2A$$

where 100nsec is the estimated time between the MOSFET turning off and the Schottky diode taking over and Ts = 3.33uS. Therefore a Schottky diode with a forward current of 0.5A is sufficient for this design.

Operation below 6V input

The SC1404 will operate below 6V input voltage with careful design, but there are limitations. The first limitation is the maximum available duty cycle from the SC1404, which limits the obtainable output voltage. The design should minimize all circuit losses through the system in order to deliver maximum power to the output.

A second limitation with operation below 6V is transient response. When load current increases rapidly, the output voltage drops slightly; the feedback loop normally increases duty cycle briefly to bring the output voltage back up. If duty cycle is already near the maximum limit, the duty cycle cannot increase enough to meet the demand, and the output voltage sags more than normal. This problem can not be solved by changing the feedback compensation, it is a function of the input voltage, duty cycle, and inductor and capacitor values.

If an application requires 5V output from an input voltage below 6V, the following guidelines should be used:

1 - Set the switching frequency to 200 kHz (Tie SYNC to GND). This increases the maximum duty cycle compared to 300 kHz operation.

2 - Minimize the resistance in the power train. Select MOSFETs, inductor, and current sense resistor to provide the lowest resistance as is practical.

3 - Minimize the pcb resistance for all traces carrying high current. This includes traces to the input capacitors, MOSFETS and diodes, inductor, current sense resistor, and output capacitor.

4 - Minimize the resistance between the SC1404 circuit and the power source (battery, battery charger, AC adaptor).

5 - Use low ESR capacitors on the input to prevent the input voltage dropping during on-time.

6 - If large load transients are expected, high capacitance and low ESR capacitors should be used on both the input and output.

5V Start-up with slow Vin ramp.

Proper startup of the 5V output can be hampered by slow dV/dt on the input. The SC1404 will power up and attempt to generate an output when the input voltage exceeds 4.5 volts. If the input has a slow dV/dt, the input voltage will not rise significantly during the start-up sequence, leading to two conditions. First, the VL supply can be hundreds of mV below 5V, since the input may not yet be above 5V. Second, the duty cycle will be at maximum, leading to very small off-times. These two conditions tend to reduce the BOOST voltage; if continued indefinitely, the BOOST capacitor may be unable to recharge fully, and eventually the high-side driver loses its BOOST bias.

To avoid this the following steps should be taken:

1. If possible the dV/dt of the input supply should exceed .02V/usec. This dV/dt condition only applies when the input passes between 4 and 6 volts, the point at which the SC1404 begins a startup sequence. An alternative is to make sure the input voltage reaches 6 volts within 100 usec of SC1404 startup at approximately 4.2 volts. This is sufficiently fast to allow VL and duty cycle to achieve normal levels and will prevents the BOOST voltage from falling.

2. If the dV/dt of the input cannot meet condition 1, the startup of the SC1404 should be delayed until the input voltage reaches 6V. This can be done using either the SHDN# or ON5 pin. If the dV/dt is moderate (slews from 4 to 6 volts in several msecs), an RC delay on either the SHDN# or ON5 pin should be enough to delay turn-on until the input reaches 6V.

3. For slow dV/dt on the input (10's of msec), the SC1404 should be held off until the input reaches 6V. This can be done using a comparator or external logic to hold the SHDN# or ON5 pin low until the input reaches 6V.

12V Load Limitations

The 12V regulator derives input power from a secondary winding on the 5V inductor. During the 5V off-time, the inductor transfers energy from the 5V winding to the secondary winding, thereby providing a crudely regulated 15V that feeds the 12V regulator. Note that duty cycle increases at low input voltages, and therefore the on-time decreases.

At low input voltages, the duty cycle increases to maintain the 5V output. The off-time consequently decreases, which has two detrimental effects. It allows less time to recharge the raw 15V capacitor, and it also raises the peak 15V current required to maintain the average 12V load. The 15V winding needs higher peak current, delivered in less time. But the stray (leakage) inductance of the inductor resists rapid changes in winding current, and ultimately limits how much current can be drawn from 15V before the voltage falls.

The following guidelines for 12V loading apply to the typical circuit, page 22.

Vin range	12V load conditions
>10V	12V load < 1/2 * 5V load 12V load = 200mA max
7V - 10V	12V load < 1/2 * 5V load Linearly derate 12V load: 200mA at 10V 100mA at 7V
6V - 7V	12V load < 1/2 * 5V load Linearly derate 12V load: 100mA at 10V 25mA at 7V

PSAVE operation

The SC1404 enters power-save operation if the load is sufficiently light, and if PSAVE is tied low. In PSAVE operation, the switching frequency is no longer fixed, and the converter operates as a hysteretic converter. This reduces gate drive losses and other switching losses to improve efficiency. Each converter willl enter or exit PSAVE operation independently, based on load current. The hysteresis (output ripple) on the 5V output is typically 70mV, and the 3V hysteresis is typically 35mV.

Overvoltage Test

Measuring the overvoltage trip point can be problematic. Any buck converter with synchronous MOSFETS can act as a boost converter, sending energy from output to input. In some cases the energy sent to the input is enough to drive the input voltage beyond normal levels, causing input overvoltage. To prevent this, enable the SC1404 PSAVE# feature, which effectively disables the low side MOSFET drive so that little energy, if any, is transferred back to the input.

Semtech recommends the following circuit for measuring the overvoltage trip point. D1 prevents the output voltage from damaging lab supply 1. R1 limits the amount of energy that can be cycled from the output to the input. R2 absorbs the energy that might flow from output to input, and D2 protects lab supply from possible damage. The ON5 signal is monitored to indicate when overvoltage occurs.

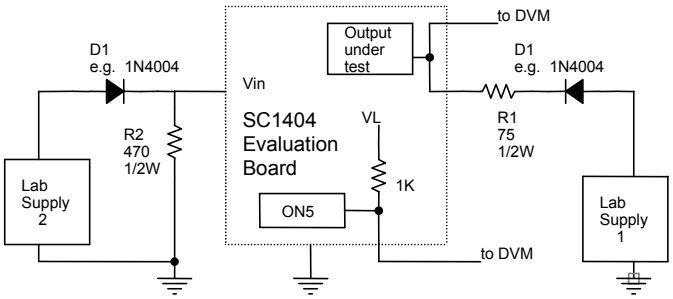
Initial conditions:

Both lab supplies set to zero volts
No load connected to 3V or 5V
PSAVE# enabled (PSAVE# tied to GND)
ON5 enabled
ON3 enabled
DVMs monitoring ON5 and the output under test.
Oscilloscope probe connected to Phase Node
of the output under test (not strictly required).

Set Lab Supply 2 to provide 10V at the SC1404 input. The phase node of the output being tested should show some switching activity. The ON5 pin should be above 4V.

Slowly increase Lab Supply 1 until the output under test rises slightly above it's normal DC level. As Lab Supply 1 increases, switching activity at the phase node will cease. The ON5 pin should remain above 4V.

Increase Lab Supply 1 in very small increments, monitoring both ON5 and the output under test. The overvoltage trip point is the highest voltage seen at the output before ON5 pulls low (approximately 0.3V). Do not record the voltage seen at the output after ON5 has pulled low; when ON5 pulls low, the current flowing in D1 changes, corrupting the voltage seen at the output.



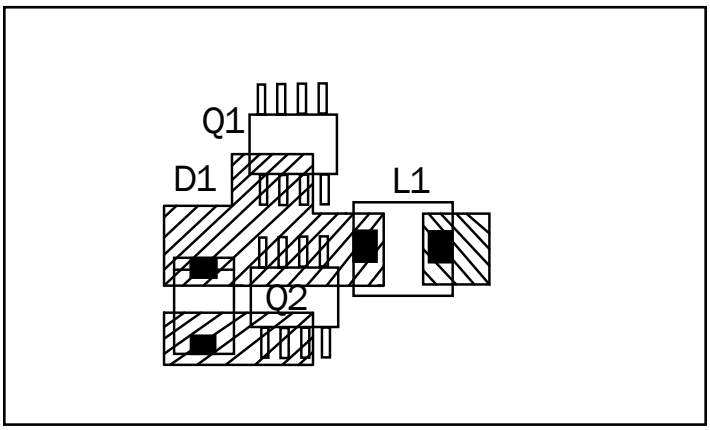
Layout Guidelines

As with any high frequency switching regulator design, a good PCB layout is very essential in order to achieve optimum noise, efficiency, and stability performance of the converter. Before starting to layout the PCB, a careful layout strategy is strongly recommended. See the PCB layout in the SC1404 Evaluation Kit manual for example. In most applications, we recommend to use FR4 with 4 or more layers and at least 2 oz copper (for output current up to 6A). Use at least one inner layer for ground connection. And it is always a good practice to tie signal ground and power ground at one single point so that the signal ground is not easily contaminated. Also be sure that high current paths have low inductance and resistance by making trace widths as wide as possible and lengths as short as possible. Properly decouple lines that pull large amounts of current in short periods of time. The following step by step layout strategy should be used in order to fully utilize the potential of SC1404.

Step #1. Power train components placement.

a. Power train arrangement.

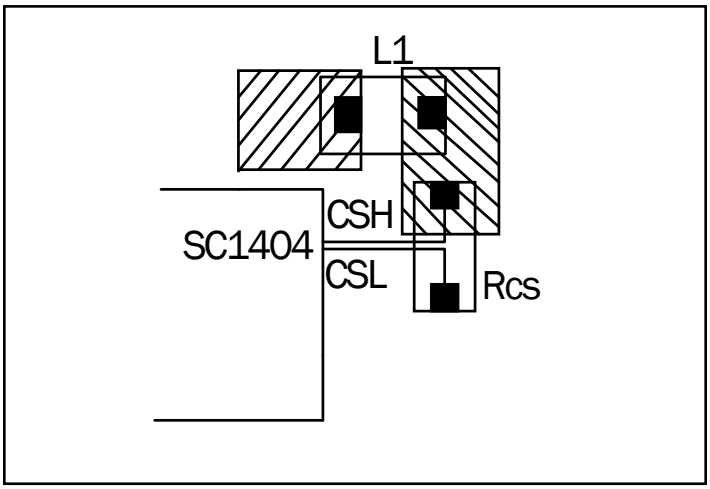
Place power train components first. The figure below shows the recommended power train arrangement. Q1 is the main switching FET, Q2 is the synchronous Rectifier FET, D1 is the Schottky diode and L1 is the output inductor. The phase node, where the source



of the upper switching FET and the drain of the synchronous rectifier meets, since it switches at very high rate of speed, is generally the largest source of common-mode noise in the converter circuit. It should be kept to a minimum size consistent with its connectivity and current carrying requirements. Also place the Schottky diode as close to the phase node as possible to minimize the trace inductance, to reduce the efficiency loss due to the current ramp-up and down time. This becomes extremely important when the converter needs to handle high di/dt requirements.

b. Current Sense.

Minimize the length of current sense signal trace. Keep it less than 15mm. Kelvin connections should be used; try to keep the traces parallel to each other and route them close to each other as much as possible. Even though SC1404 implements Virtual Current Sense scheme, the current sense signal is sampled by the SC1404 to determine the PSAVE threshold. See the following figure for a Kelvin connection of the current sense signal.



c. Gate Drive.

SC1404 has built-in gate drivers capable of sinking/sourcing 1A peaks. Upper gate drive signals are noisier than the lower ones. Therefore, place them away from sensitive analog circuitries. Make sure the lower gate traces are as close as possible to the IC pins and both upper and lower gate traces as wide as possible.

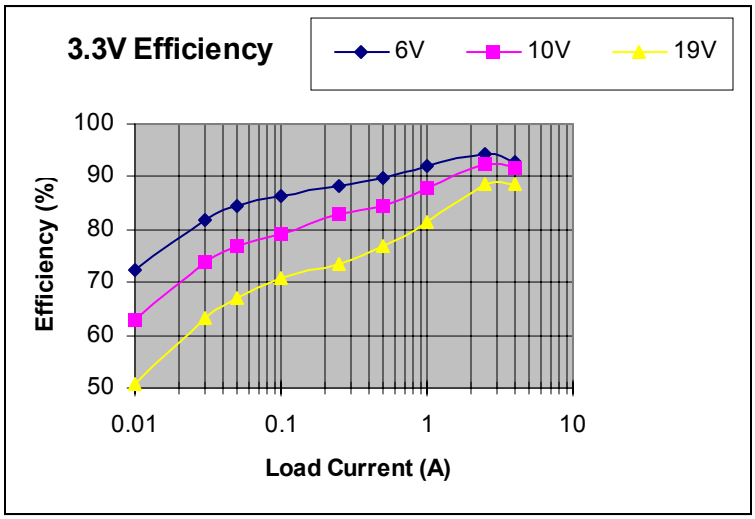
Step #2: PWM controller placement (pins) and signal ground island.

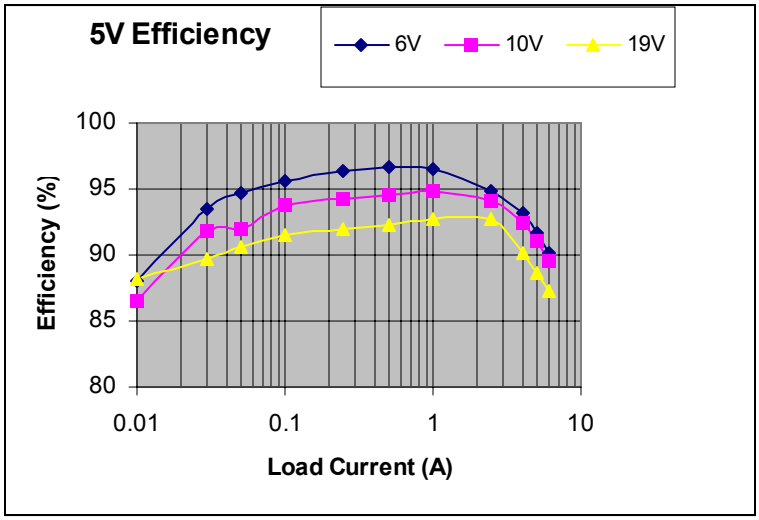
Connect all analog grounds to a separate solid copper island plane, which connects to the SC1404's GND pin. This includes REF, COMP3, COMP5, SYNC, RUN/ON3, ON5, PSV# and RESET#.

Step #3: Ground plane arrangement.

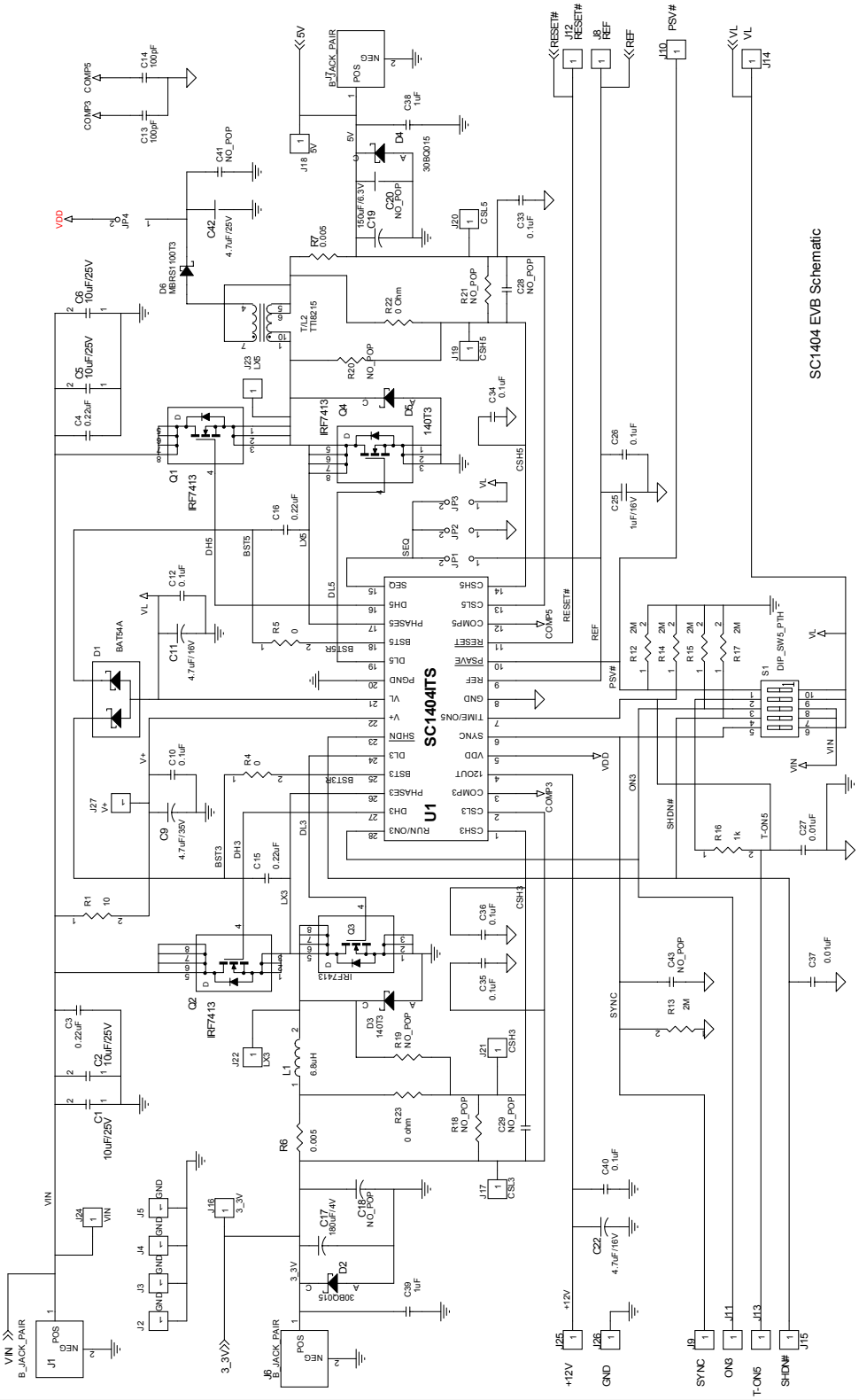
There are several ways to tie the different grounds together. Since this is a buck topology converter, the output ground is relatively quieter than the input ground. Therefore connect analog ground to power ground at the output side. Often it is useful to use a separate ground symbol for the two grounds, and tie the two grounds together at a single point through a 0Ω resistor. The power ground for the input side and the power ground for the output side is the same ground and they can be tied together using internal planes.

Typical Characteristics





Evaluation Board Schematic



Evaluation Board Bill of Materials

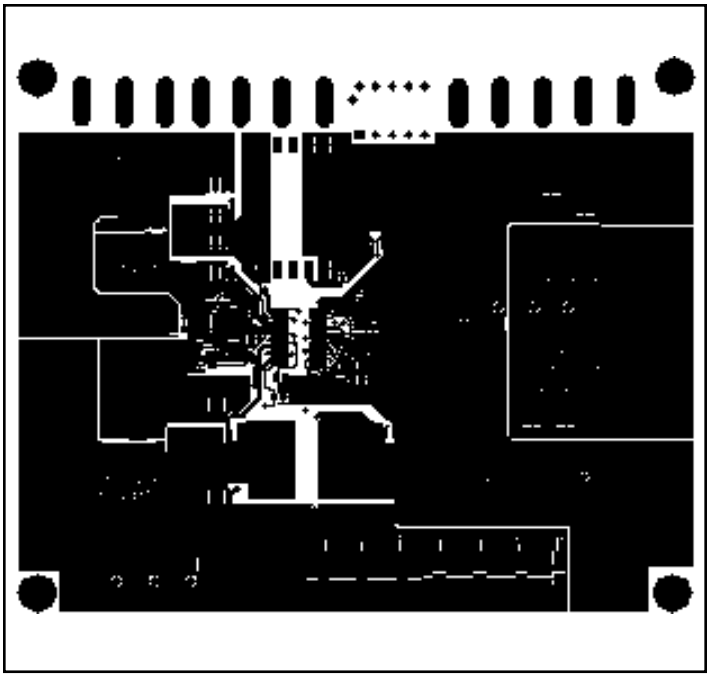
ITEM	QTY	DESIGNATION	PART NUMBER	DESCRIPTION	MANUFACTURER	FORM FACTOR
1	4	C1,C2,C5,C6	GRM230Y5V106Z025	10uF, 25V	Murata	1210
2	1	C3, C4, C15, C16		0.22uF, 50V, Y5V	Panasonic	805
3		C9		4.7uF, 35V		B_case
4		C10,C12,C26,C33,C34,C3-5,C36,C40		0.1uF,50V, X7R	Panasonic	0603
5		C11,C22	Y475M250N	4.7uF, 16V	Novacap	1812
6		C14,C13	ECJ1VC1H101K	100pF, 50V	Panasonic	0603
7		C17	EEF-UE0G181R	180uF, 4V	Panasonic	D_Case_7343
8		C19	EEF-UE0J151R	150uF, 6.3V	Panasonic	D_Case_7343
9		C25	ECJ3FB1C105	1uF, 16V	Panasonic	1206
10		C37,C27	ECJ1VB1C104K	0.01uF, 50V	Panasonic	0603
11		C39,C38		1uF		0603
12		C42		4.7uF, 25V		
13	1	D1	BAT54A	30V, 200ma, dual C_Anode	Zetex	SOT-23
14	2	D2, D4	30BQ015		I. R.	SMC
15	2	D3, D5	MBRS140T3	40V, 1A Schottky	Motorola	SMB
16	1	D6	MBRS1100T3		Motorola	SMB

Evaluation Board Bill of Materials Cont.

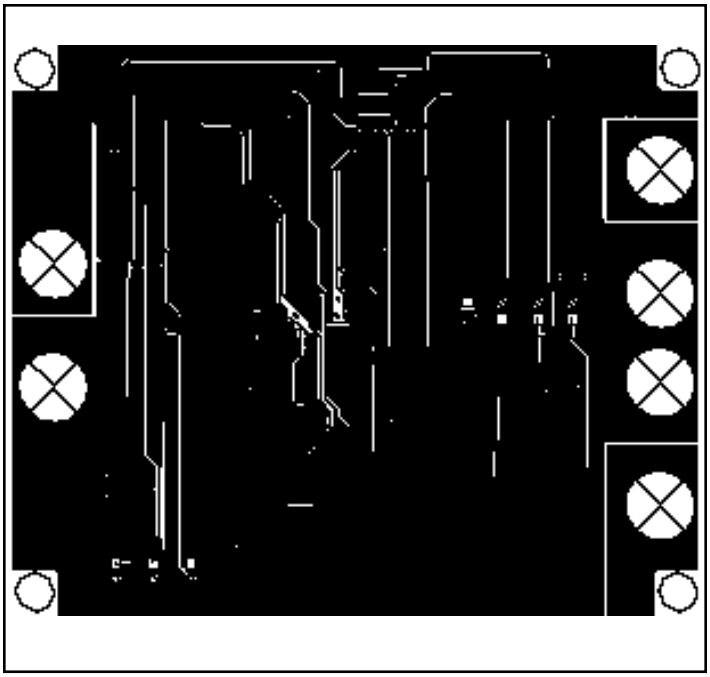
ITEM	QTY	DESIGNATION	PART NUMBER	DESCRIPTION	MANUFACTURER	FORM FACTOR
17	4	JP1, JP2, JP3, JP4		2 Pin Berg Connector	Berg	
18	3	J1, J6, J7		Banana Jack Pair		
19	24	J2-J5, J8-J27		Test Points		
20	1	L1	DR127-6R8	SMT Inductor 6.8uH	Coiltronics	
21	4	Q1, Q2, Q3, Q4	IRF7413	30V N-channel MOSFET	International Rectifier	SO8
22	1	R1	Any	10ohm	Any	0603
23	4	R4, R5, R22, R23	Any	0ohm	Any	0603
24	2	R6, R7	WSL2512R005FB43	5mohm	Vishay Dale	2512
25	5	R12, R13, R14, R15, R17	Any	2Megohm	Any	0603
26	1	R16	Any	1Kohm	Any	0603
27	1	SW1		5-position Dipswitch	Any	
28	1	T/L2	TTI-8215		Transpower Technologies	
29	1	U1	SC1404ITS		Semtech	

Evaluation Board Gerber Plots

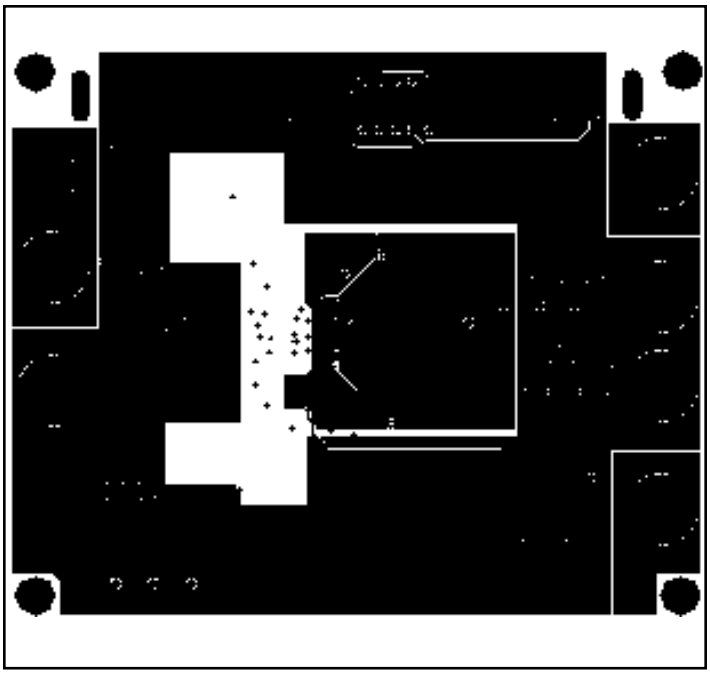
Top



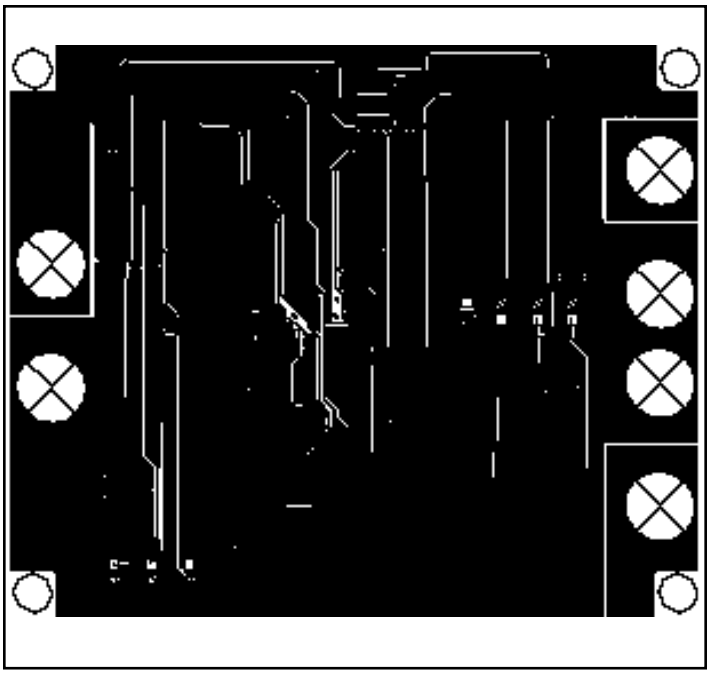
Inner2



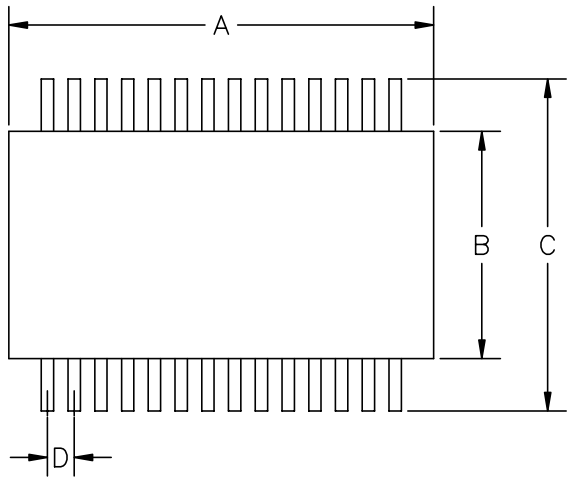
Inner1

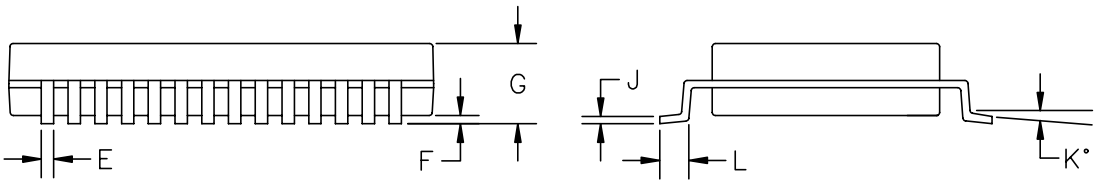


Bottom



Outline Drawing - SSOP-28



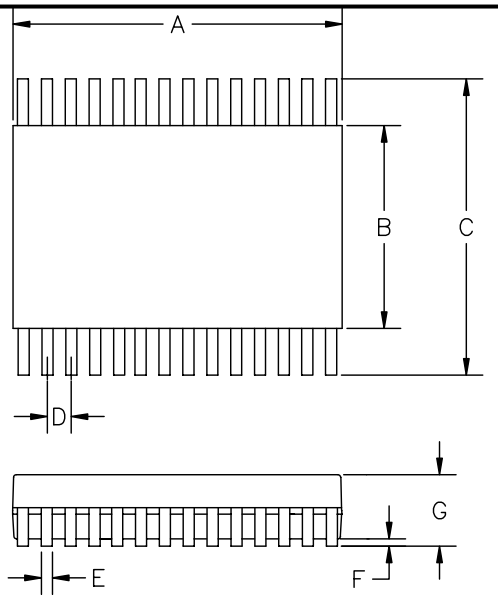


DIMENSIONS [1]					
DIM^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.390	.413	9.90	10.50	[2]
B	.197	.221	5.00	5.60	[2]
C	.291	.323	7.40	8.20	–
D	.026 BSC		.65 BSC		–
E	.009	.015	.22	.38	–
F	.002	.008	.05	.20	–
G	.068	.078	1.73	2.00	–
J	.004	.010	.09	.25	–
K	0°	8°	0°	8°	–
L	.022	.037	.55	.95	–

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Outline Drawing - TSSOP-28



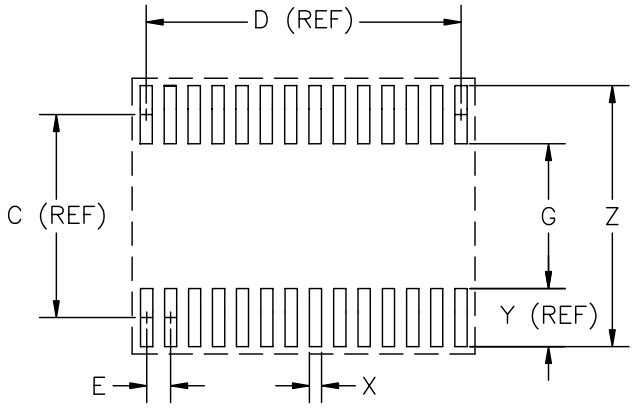
DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	[2]
B	.169	.177	4.30	4.50	[2]
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0020	.0060	.05	.15	—
G		.047		1.20	—
J	.0035	.0079	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

JEDEC MO-153AE

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-28



DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.218	—	5.53	REF
D	—	.333	—	8.45	REF
E	—	.026	—	0.65	BSC
G	.155	—	3.947	—	—
X	—	.013	—	0.323	—
Y	—	.062	—	1.583	REF
Z	—	.280	—	7.113	—

[2] GRID PLACEMENT COURTYARD IS 18 X 15 ELEMENTS (9mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

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