SC1486
Dual Synchronous Buck Pseudo Fixed Frequency DDR Power Supply Controller

Description

The SC1486 is a dual output constant on synchronous-buck PWM controller optimized for cost effective mobile DDR applications. Features include high efficiency, a fast dynamic response with no minimum on time, a REFIN input and a buffered REFOUT pin capable of sourcing 3mA. The excellent transient response means that SC1486 based solutions will require less output capacitance than competing fixed frequency converters.

The frequency is constant until a step in load or line voltage occurs at which time the pulse density and frequency will increase or decrease to counter the change in output or input voltage.

The output voltage of the first controller can be adjusted from 0.5V to VCCA. In DDR applications, this voltage is set to 2.5 volts. A resistor divider from the 2.5 volt supply is used to drive the REFIN pin of the second controller. A unity gain buffer drives the REFOUT pin to the same potential as REFIN. The second controller regulates its output to REFOUT. Two frequency setting resistors set the on-time for each buck controller. The frequency can thus be tailored to minimize crosstalk. The integrated gate drivers feature adaptive shoot-through protection and soft switching. Additional features include cycle-by-cycle current limit, digital soft-start, overvoltage and under-voltage protection, and a PGOOD output for each controller.

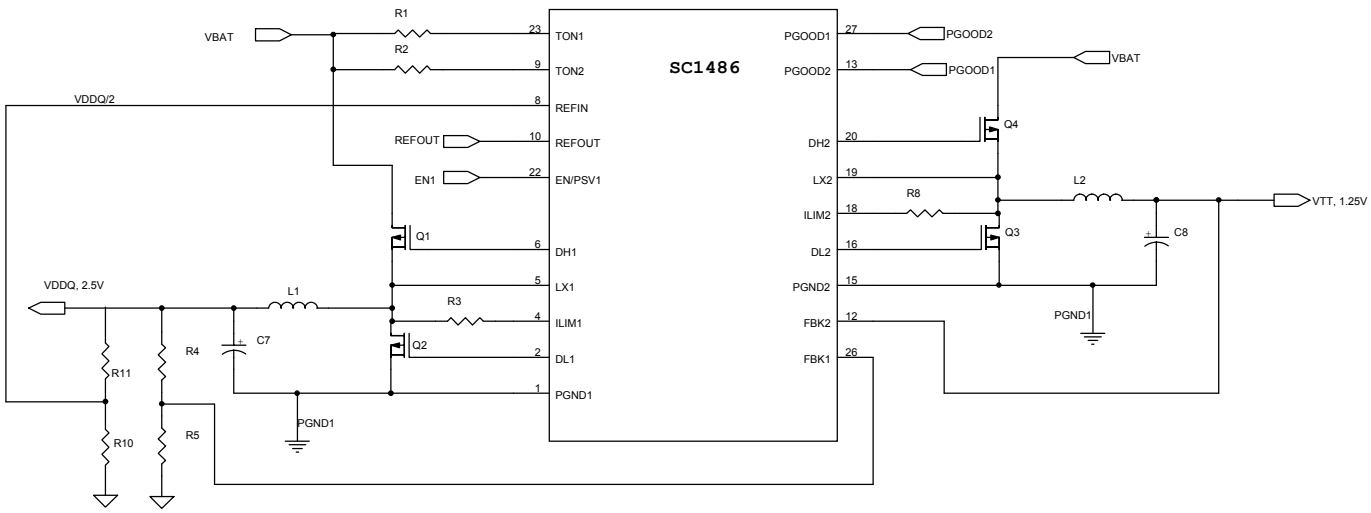
Features

- Constant on-time for fast dynamic response
- VIN range = 1.8V – 25V
- DC current sense using low-side RDS(ON) sensing or sense resistor
- Integrated reference buffer for VTT
- Low power S3 state
- Resistor programmable frequency
- Cycle-by-cycle current limit
- Digital soft-start
- PSAVE option for VDDQ
- Over-voltage/under-voltage fault protection
- <20uA shutdown current
- Low quiescent power dissipation
- Two separate PGOOD indicators
- Separate enable of each switcher
- Integrated gate drivers with soft switching
- Efficiency >90%
- 1% Internal reference
- 28 Lead TSSOP
- Industrial temperature range

Applications

- Notebook computers
- CPU I/O supplies
- Handheld terminals and PDAs
- LCD monitors
- Network power supplies

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
TON1 to AGND1, TON2 to AGND2		-0.3 to +25.0	V
DH1, BST1 to AGND1 and DH2, BST2 to AGND2		-0.3 to +30.0	V
LX1 to AGND1 and LX2 to AGND2		-2.0 to +25.0	V
AGND1 to PGND1, and AGND2 to PGND2		-0.3 to +0.3	V
BST1 to LX1 and BST2 to LX2		-0.3 to +6.0	V
VCCA1, VDDP1 to AGND1 and VCCA2, VDDP2 to AGND2		-0.3 to +6.0	V
FB1, PGOOD1, EN/PSV1, ILIM1, VOUT1, DL1 to PGND1		-0.3 to +6.0	V
FB2, PGOOD2, REFIN, ILIM2, REFOUT, DL2 to PGND2		-0.3 to +6.0	V
Thermal Resistance Junction to Ambient(5)	θ_{JA}	37	°C/W
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C

Electrical Characteristics

Test Conditions: V_{BAT} = 15V, EN/PSV1 = 5V, REFIN=1.25V, VCCA1 = VDDP1 = VCCA2 =VDDP2= 5.0V, V_{VDDQ} = 2.5, V_{VTT} = 1.25, R_{TON1} = 1M, R_{TON2} = 1M

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VCCA1, VCCA2			5.0		4.5	5.5	V
VDDP1, VDDP2			5.0		4.5	5.5	V
VDDP2 Undervoltage Threshold	VDDP2 falling		3.5				V
VDDP2 Undervoltage Hysteresis			250				mV
VDDP1 Operating Current	FB > regulation point, I_{LOAD} = 0A		1			5	µA
VDDP2 Operating Current			5			10	
VCCA1, VCCA2 Operating Current	FB > regulation point, I_{LOAD} = 0A		700			1100	µA
VCCA2 Standby Current	VDDP2 < VDDP2 UV threshold, no load on REFOUT		125				µA
TON1, TON2 Operating Current	R_{TON} = 1M		15				µA
REFIN Bias Current	REFIN = 1.25					1	µA
Shutdown Current	EN/PSV1 = 0V		-5			-10	µA
	VCCA1, VCCA2		5			10	µA
	TON1, TON2, VDDP1		0			1	µA

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, EN/PSV1 = 5V, REFIN=1.25V, VCCA1 = VDDP1 = VCCA2 =VDDP2= 5.0V, V_{VDDQ} = 2.5, V_{VTT} = 1.25, R_{TON1} = 1M, R_{TON2} = 1M

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Controller							
Error Comparator Threshold (FBK1 Turn ON Threshold)	VCCA = 4.5V to 5.5V VBAT = 2V to 25V		0.500		0.495	0.505	V
VDDQ Output Voltage Range					0.5	VCCA	V
REFOUT Source Capability					3		mA
REFOUT DC Accuracy	no load, REFIN = 1.25	1.24		1.26	1.238	1.262	V
Error Comparator Threshold (FBK2 Turn ON Threshold)	VCCA = 4.5V to 5.5V VBAT = 2V to 25V		REFOUT		REFOUT -10mV	REFOUT +10mV	V
On-Time, VBAT = 2.5V	R_{TON} = 1M (300kHz), V_{OUT} = 1.25V		1660		1411	1909	ns
	R_{TON} = 500K (600kHz), V_{OUT} = 1.25V		913		776	1050	ns
Minimum Off Time			400			550	ns
VOUT Input Resistance (VDDQ Controller)			500				kΩ
Line Regulation Error	VCCA, VDDP = 4.5V to 5.5V VBAT = 4.5V to 25V		0.04				%/V
Load Regulation Error	ILIM - PGND = 0V to OC Limit EN/PSV1 = Open		0.3				%
FBK1 Input Bias Current					-1.0	+1.0	µA
FBK2 Input Bias Current			2.5				µA
Over-Current Sensing							
ILIM Current			10		9	11	µA
Current Comparator Offset	PGND - ILIM				-10	+10	mV
PSAVE							
Zero-Crossing Threshold	PGND - LX EN/PSV1 = 5V		5				mV
Fault Protection							
Current Limit (Positive) (2) (PGND-LX)	R_{ILIM} = 5kΩ		50		-35	65	mV
	R_{ILIM} = 10kΩ		100		80	120	mV
	R_{ILIM} = 20kΩ		200		170	230	mV
Current Limit (Negative) (PGND-LX)			-140		-200	-100	mV

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, EN/PSV1 = 5V, REFIN=1.25V, VCCA1 = VDDP1 = VCCA2 =VDDP2= 5.0V, V_{VDDQ} = 2.5, V_{VTT} = 1.25, R_{TON1} = 1M, R_{TON2} = 1M

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Fault Protection (Cont.)							
VDDQ - Output Under-Voltage Fault	With respect to internal reference		-30		-40	-25	%
VTT - Output Under-Voltage Fault	With respect to REFOUT		-20		-28	-15	%
VDDQ/VTT Output Over-Voltage Fault	VDDQ with respect to internal reference, VTT with respect to REFOUT		+10		+8	+12	%
Over-Voltage Fault Delay	FB forced above OV threshold		2				µs
PGOOD Low Output Voltage	Sink 1mA					0.4	V
PGOOD Leakage Current	FB in regulation, PGOOD = 5V					1	µA
PGOOD UV Threshold	With respect to internal reference for VDDQ and REFOUT for VTT		-10		-15	-8	%
PGOOD Fault Delay	FB forced outside PGOOD window.		2				µs
VCCA1,VCCA2 Under Voltage	Falling (100mV hysteresis)		4.0		3.7	4.3	V
Over Temperature Lockout	10°C Hysteresis		165				°C
Inputs/Outputs							
Logic Input Low Voltage	EN/PSV1 low					1.2	V
Logic Input High Voltage	EN High, PSV low (Pin Floating)		2.0		1.2	2.4	V
Logic Input High Voltage	EN/PSV1 high				2.4		V
REFIN EN Threshold			0.80		0.55	1.00	V
REFIN EN Hysteresis			40				mV
EN/PSV1 Input Resistance	Pullup resistance		1.5				MΩ
	Pulldown resistance		1.0				
Soft Start							
Soft-Start Ramp Time	EN/PSV1 high to full current limit.		1.6				ms
Under-Voltage Blank Time	SMPS turn-on		2				ms

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, EN/PSV1 = 5V, REFIN=1.25V, VCCA1 = VDDP1 = VCCA2 =VDDP2= 5.0V, V_{VDDQ} = 2.5, V_{VTT} = 1.25, R_{TON1} = 1M, R_{TON2} = 1M

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Gate Drivers							
Shoot-Through Delay (4)	DH or DL rising		30				ns
DL Pull-Down Resistance	DL low		0.8			1.6	Ω
DL Pull-Up Resistance	DL high		2			4	Ω
DH Pull-Down Resistance	DH low, BST - LX = 5V		2			4	Ω
DH Pull-Up Resistance	DH high, BST - LX = 5V		2			4	Ω

Notes:

(1) The output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple voltage.

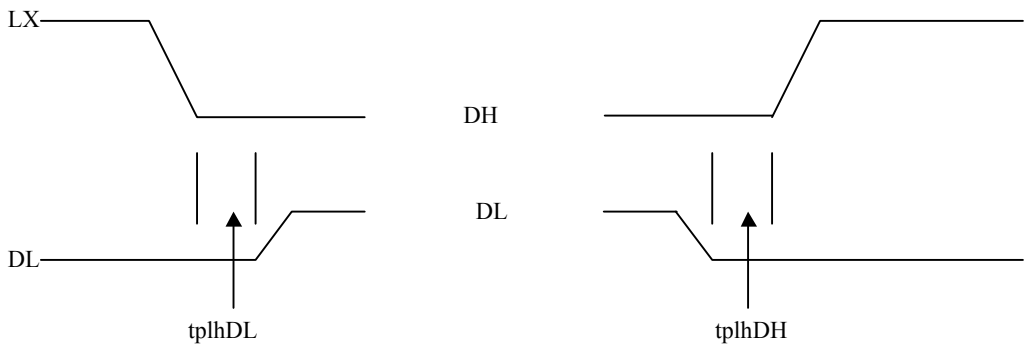
(2) Using a current sense resistor, this measurement relates to PGND minus the voltage of the source on the low-side MOSFET.

(3) This device is ESD sensitive. Use of standard ESD handling precautions is required.

(4) Guaranteed by design. See Shoot-Through Delay Timing Diagram below.

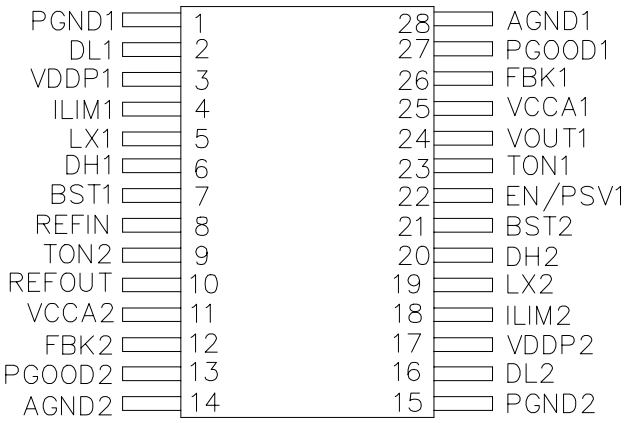
(5) Measured in accordance with JESD51-1, JESD51-2 and JESD51-7.

Shoot-Through Delay Timing Diagram



Pin Configuration

Top View



(TSSOP-28)

Ordering Information

DEVICE	PACKAGE(1)
SC1486ITSTR	TSSOP-28
SC1486ITSTRT(2)	TSSOP-28

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free option.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	PGND1	Power ground.
2	DL1	Gate drive output for the low side MOSFET switch.
3	VDDP1	+5V supply voltage input for the gate drivers.
4	ILIM1	Current limit input pin. Connect to drain of low-side MOSFET for RDS(on) sensing or the source for resistor sensing through a threshold sensing resistor. See applications section for more information.
5	LX1	Switching node inductor connection.
6	DH1	Gate drive output for the high side MOSFET switch.
7	BST1	Boost capacitor connection for the high side gate drive.
8	REFIN	Reference input. A resistor divider from the 2.5 volt supply sets this voltage. A 0.1 µF input filter capacitor is reccomended.
9	TON2	Battery input voltage and sets on-time of upper MOSFET by series resistor between input supply and VIN.
10	REFOUT	Buffered REFIN output. The second controller regulates to this voltage.
11	VCCA2	Supply voltage input for the analog supply. Connect through a RC filter.
12	FBK2	Feedback input for the SMPS. Connect from resistive divider at output to select output voltage from 0.5V to VCCA.
13	PGOOD2	Power Good output. Goes high after a fixed clock cycle delay following power up.
14	AGND2	Analog ground.

Pin Descriptions (Cont)

15	PGND2	Power ground.
16	DL2	Gate drive output for the low side MOSFET switch.
17	VDDP2	+5V supply voltage input for the gate drivers.
18	ILIM2	Current limit input pin. Connect to drain of low-side MOSFET for RDS(on) sensing or the source for resistor sensing through a threshold sensing resistor. See applications section for more information.
19	LX2	Switching node inductor connection.
20	DH2	Gate drive output for the high side MOSFET switch.
21	BST2	Boost capacitor connection for the high side gate drive.
22	EN/PSV1	Enable/Power Save input pin. Tie to ground to disable SMPS. Tie to +5V to enable SMPS and activate PSAVE mode. Float to Enable SMPS and activate continous conduction mode.
23	TON1	Battery input voltage and sets on-time of upper MOSFET by series resistor between input supply and VIN.
24	VOUT1	Output voltage sense input for the SMPS output. Connect to the output of the SMPS.
25	VCCA1	Supply voltage input for the analog supply. Connect through a RC filter.
26	FBK1	Feedback input for the SMPS. Connect from resistive divider at output to select output voltage from 0.5V to VCCA.
27	PGOOD1	Power Good output. Goes high after a fixed clock cycle delay following power up.
28	AGND1	Analog ground.

Block Diagram

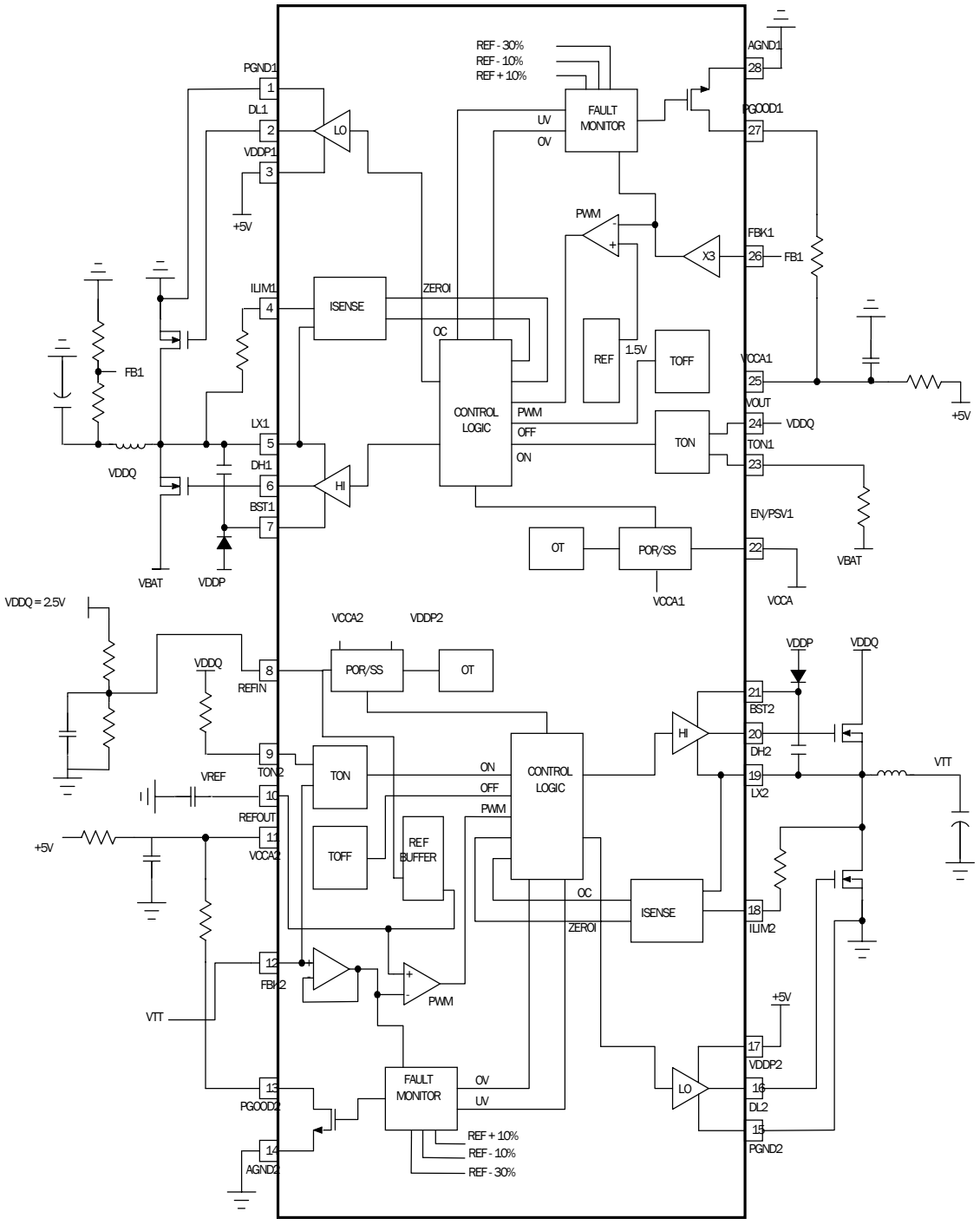


FIGURE 1 - SC1486 Block Diagram

Application Information

+5V Bias Supplies

The SC1486 requires an external +5V bias supply in addition to the battery. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator such as the Semtech LP2951A. To minimize channel to channel crosstalk, each controller has 4 supply pins, VDDP, PGND, VCCA and AGND.

To avoid ground loops, separate AGND planes are recommended. Each contoller requires its own AGND plane which should be tied by a single trace to the negative terminal of that controller's output capacitor. All external components referenced to AGND in the schematic should then be connected to the appropriate AGND plane. The supply decoupling capacitor for controller 1 should be tied between VCCA1 and AGND1. Likewise, the supply decoupling capacitor for controller 2 should be tied between VCCA2 and AGND2. A single 10 ohms resistor should be used to decouple the VCCA supplies from the main VDDP supplies. PGND can then be a separate plane which is not used for routing traces. All PGND connections are connected directly to this plane with special attention given to avoiding indirect connections which may create ground loops. As mentioned above, the two AGND planes must be connected to the PGND plane at the negative terminal of the respective output capacitors. The VDDP1 and VDDP2 input provides power to the upper and lower gate drivers. A decoupling capacitor for each supply is recommended. No series resistor between VDDP and the 5 volt bias is required.

Pseudo-fixed Frequency Constant On-Time PWM Controller

The PWM control architecture consists of a constant-on-time, pseudo fixed frequency PWM controller, (Figure 1). The output ripple voltage developed across the output filter capacitor's ESR provides the PWM ramp signal eliminating the need for a current sense resistor. The high-side switch on-time is determined by a one-shot whose period is directly proportional to output voltage and inversely proportional to input voltage. A second one-shot sets the minimum off-time which is typically 400ns.

On-Time One-Shot (T_{ON})

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The TON time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a nearly constant switching frequency without the need of a clock generator.

$$T_{ON} = 3.3x10^{-12} \bullet (R_{TON} + 37x10^{3}) \bullet \left(\frac{V_{OUT}}{V_{IN}} \right) + 50ns$$

R_{TON} is a resistor connected from the input supply to the TON pin.

Enable & Psave

The EN/PSV pin enables the VDDQ (2.5 volt) supply. REFIN and VDDP2 enable the VTT (1.25 volt) supply. The VTT and VDDQ supplies may be enabled independently. When EN/PSV is tied to VCCA the VDDQ controller is enabled and power save will also be enabled. When the EN/PSV pin is tristated, an internal pulled-up will activate the VDDQ controller and power save will be disabled. If PSAVE is enabled, the SC1486 PSAVE comparator will look for the inductor current to cross zero on eight consecutive cycles. Once observed, the controller will enter power save and turn off the low side MOSFET when the current crosses zero. To improve the efficiency and add hysteresis, the on time is increased by 50% in power save. The efficiency improvement at light loads more than offsets the disadvantage of slighlty higher output ripple. If the inductor current does not cross zero on any switching cycle, the controller will immediately exit power save. Since the controller counts crossings, the converter can sink current as long as the current does not cross zero on eight consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps even when psave is enabled.Since the VTT supply must sink current, this controller does not have a power save option. If REFIN is low, the VTT controller shuts down to a low bias current. If Refin is greater than 1 volt, and VDDP2 is low, the reference buffer is active, but the VTT buck converter is disabled (S3 state). If REFIN is greater than 1 volt and VDDP is greater than 4 volts, the VTT supply is active.

Output Voltage Selection

The output voltage selection is set by the feedback resistors R2 & R3 of Figure 3. The internal reference is 1.5V. The internal feedback pin is multiplied by three to match the 1.5V reference. Therefore the output can beselected to a minimum of 0.5V. The equation for setting he output voltage based on Figure 3 is:

Application Information (Cont.)

$$Vout=\left(1+\frac{R2}{R3}\right)\bullet 0.5$$

Current Limit Circuit

Current limiting of the SC1486 can be accomplished in two ways. The on-state resistance of the low-side MOSFETs can be used as the current sensing element or sense resistors in the low-side sources can be used if greater accuracy is desired. RDSON sensing is more efficient and less expensive. In both cases, the R_{ILIM} resistors between the ILIM pin and LX set the over current threshold. This resistor R_{ILIM} is connected to a 10uA current source within the SC1486 which is turned on when the low side MOSFET turns on. When the voltage drop across the sense resistor or low side MOSFET equals the voltage across the R_{ILIM} resistor, current limit will activate. The high side will not be allowed to turn on until the voltage drop across the sense element (resistor or MOSFET) falls below the voltage across the R_{ILIM} resistor.

The current sensing circuit actually regulates the inductor valley current (see Figure 2). This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 10A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are shown below:

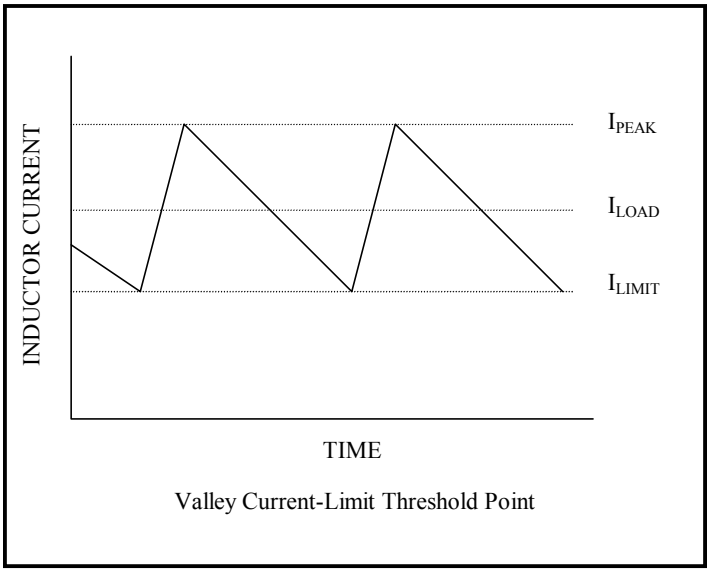


FIGURE 2

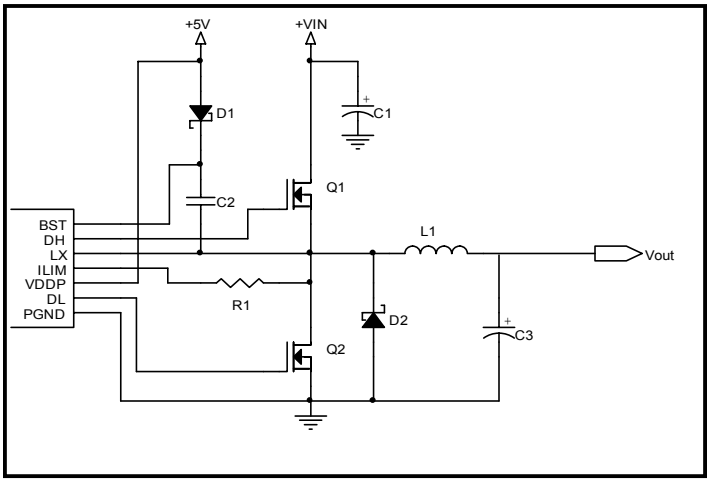


FIGURE 3

The schematic of RDS_{ON} sensing circuit is shown in Figure 3 with R_{ILIM} = R1 and RDS_{ON} of Q2.

Similarly, for resistor sensing, the current through the lower MOSFET and the source sense resistor develops a voltage that opposes the voltage developed across R_{ILIM}. When the voltage developed across the R_{SENSE} resistor reaches voltage drop across $R_{ILIM,}$ an over-current exists and the high side MOSFET will not be allowed to turn on. The over-current equation when using an external sense resistor is:

$$IL_{OC}(Valley)=10\mu A\bullet\frac{R_{ILIM}}{R_{SENSE}}$$

Schematic of resistor sensing circuit is shown in Figure 4 with R_{ILIM} = R1 and R_{SENSE} = R4.

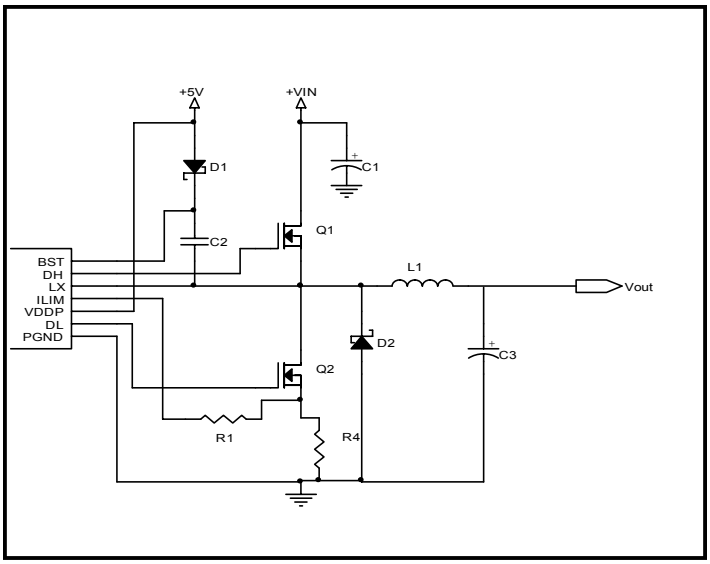


FIGURE 4

Application Information (Cont.)

Power Good Output

Each controller has its own PGOOD. Power good is an open-drain output and requires a pull-up resistor. When the output voltage is 10% above or below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within 10% of the output set voltage. PGOOD is also held low during start-up and will not be allowed to transition high until soft start is over and the output reaches 90% of its set voltage. There is a 2us delay built into the PGOOD circuit to prevent false transitions.

Output Overvoltage Protection

When the output exceeds 10% of the its set voltage the low-side MOSFET is latched on. It stays latched and the SMPS is off until the enable input, REFIN or VCCA is toggled. There is a 2us delay built into the OV protection circuit to prevent false transitions. A OV fault in either controller will not cause the other one to shutdown. Note: to reset VDDQ from a fault, VCCA1 or EN/PSV must be togled. To reset VTT from a fault, VCCA2 or REFIN must be togled.

Output Undervoltage Protection

When the output is 30% below its set voltage the output is latched in a tristated condition, and the SMPS is off until the enable input is toggled. There is a 2us delay built into the UV protection circuit to prevent false transitions. An UV fault in either controller will not effect the other controller.

POR, UVLO and Softstart

An internal power-on reset (POR) occurs when VCCA1 and VCCA2 exceed 3V, resetting the fault latch and soft-start counter, and preparing the PWM for switching. VCCA undervoltage lockout (UVLO) circuitry inhibits switching and forces the DL gate driver high until VCCA rises above 4.2V. At this time the circuit will come out of UVLO and begin switching, and the softstart circuit being enabled, will progressively limit the output current over a predetermined time period. The ramp occurs in four steps: 25%, 50%, 75% and 100%, thereby limiting the slew rate of the output voltage. There is 100mV of hysteresis built into the UVLO circuit and when the VCCA falls to 4.1V the output drivers are shutdown and tristated.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on, until DL is fully off, and conversely, monitors the DH output and prevents the low-side MOSFET from turning on until DH is fully off. Be sure there is low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

Design Procedure

Prior to any design of a switch mode power supply (SMPS) for notebook computers, determination of input voltage, load current, switching frequency and inductor ripple current must be specified.

Input Voltage Range

The maximum input voltage (VIN_{MAX}) is determined by the highest AC adaptor voltage. The minimum input voltage (VIN_{MIN}) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches.

Maximum Load Current

There are two values of load current to consider. Continuous load current and peak load current. Continuous load current has more to do with thermal stresses and therefore drives the selection of input capacitors, MOSFETs and commutation diodes. Whereas, peak load current determines instantaneous component stresses and filtering requirements such as, inductor saturation, output capacitors and design of the current limit circuit.

Switching Frequency

Switching frequency determines the trade-off between size and efficiency. Increased frequency increases the switching losses in the MOSFETs, since losses are a function of VIN^2. Knowing the maximum input voltage and budget for MOSFET switches usually dictates where the design ends up.

Inductor Ripple Current

Low inductor values create higher ripple current, resulting in smaller size, but are less efficient because of the high AC currents flowing through the inductor. Higher inductor values do reduce the ripple current and are more efficient, but are larger and more costly. The selection of the ripple current is based on the maximum output current and tends to be between 20% to 50% of the maximum load current. Again, cost, size and efficiency all play a part in the selection process.

Application Information (Cont.)

Stability Considerations

Unstable operation shows up in two related but distinctly different ways: double pulsing and fast-feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is too low, causing not enough voltage ramp in the output signal. This causes the error amplifier to trigger prematurely after the 400ns minimum off-time has expired. Double-pulsing will result in higher ripple voltage at the output, but in most cases is harmless. However, in some cases double-pulsing can indicate the presence of loop instability, which is caused by insufficient ESR. One simple way to solve this problem is to add some trace resistance in the high current output path. A side effect of doing this is output voltage droop with load. Another way to eliminate doubling-pulsing is to add a 10pF capacitor across the upper feedback resistor divider network. This is shown below in Figure 5, by capacitor C4 in the schematic. This capacitance should be left out until confirmation that double-pulsing exists. Adding this capacitance will add a zero in the transfer function and should eliminate the problem. It is best to leave a spot on the PCB in case it is needed.

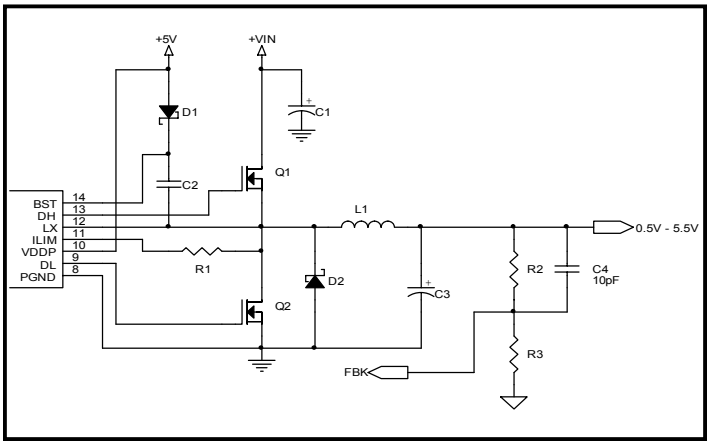


FIGURE 5

Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit.

The best way for checking stability is to apply a zero to full load transient and observe the output voltage ripple envelope for overshoot and ringing. Over one cycle of ringing after the initial step is sign that the ESR should be increased.

SC1486 ESR Requirements

The constant on-time control used in the SC1486 regulates the ripple voltage at the output capacitor. This signal consists of a term generated by the output ESR of the capacitor and a term based on the increase in voltage across the capacitor due to charging and discharging during the switching cycle. The minimum ESR is set to generate the required ripple voltage for regulation. For most applications the minimum ESR ripple voltage is dominated by PCB layout and the properties of SP or POSCAP type output capacitors. For applications using ceramic output capacitors the absolute minimum ESR must be considered. Existing literature describing the ESR requirements to prevent double pulsing does not accurately predict the performance of constant on-time controllers. A time domain model of the converter was developed to generate equations for the minimum ESR empirically. If the ESR is low enough the ripple voltage is dominated by the charging of the output capacitor. This ripple voltage lags the on-time due to the LC poles and can cause double pulsing if the phase delay exceeds the off-time of the converter. Refering to Figure 5, the equation for the minimum ESR as a function of output capacitance and switching frequency and duty cycle is;

$$ESR > \left(\frac{R2+R3}{R3}\right) \bullet \left(\frac{1+3\bullet\left(\frac{Fs-200000}{Fs}\right)}{2\bullet\pi\bullet Cout\bullet Fs\bullet(1-D)^2}\right)$$

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 500nS (maximum) minimum off-time one-shot. For best dropout performance, use the slowest on-time setting of 200KHz. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The IC duty-factor limitation is given by:

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

Layout Guidelines (TBD)

Application Information (Cont.)

SC1486 System DC Accuracy (VTT Controller)

Two IC parameters effect system DC accuracy, the error comparator offset voltage, and the switching frequency variation with line and load. The 1486 regulates to the REFOUT voltage not the REFIN voltage. Since DDR specifications are written with respect to REFOUT, the offset of the reference buffer does not create a regulation error.

The error comparator offset is trimmed so that it trips when VOUT is 1.25 volts at room temperature. This offset does not drift significantly with supply and temperature. Thus, the error comparator contributes 1% or less to DC system inaccuracy.

The on pulse in the SC1486 is calculated to give a pseudo fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant on regulators regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if REFOUT=1.25 volts, then the valley of the output ripple will be 1.25 volts. If the ripple is 20mv with VIN=6, then the DC output voltage will be 1.26 volts. If the ripple is 40mv with VIN=25 volts, then the DC output voltage will be 1.27 volts. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation is usually desirable to use passive droop. Take the feedback directly from the output side of the inductor incorporating a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced. Passive droops also improves stability so it should be used when possible.

1486 System DC Accuracy (VVDQ Controller)

Three IC parameters affect system DC accuracy, the internal band gap reference, the error comparator offset voltage, and the switching frequency variation with line and load.

The internal 1% 1.5V reference contains two error components, a 0.5% DC error and a 0.5% supply and temperature error. The error comparator offset is trimmed so that it trips when the feedback pin is nominally 0.5 volts +/-1% at room temperature. The comparator offset trim compensates for any DC error in the reference. Thus, the percentage error is the sum of the reference variation over supply and temperature and the offset in the error comparator or 1.5%.

The on pulse in the SC1486 is calculated to give a pseudo fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant on regulators regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the feedback resistors are chosen to divide down the output by a factor of five, the valley of the output ripple will be 2.5V. If the ripple is 50mv with VIN = 6 volts, then the measured DC output will be 2.525 volts. If the ripple increases to 80mv with VIN = 25 volts, then the measured DC output will be 2.540. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation is usually desirable to use passive droop. Take the feedback directly from the output side of the inductor incorporating a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced.

Board components and layout also influence DC accuracy. The use of 1% feedback resistors contribute 1%. If tighter DC accuracy is required use 0.1% feedback resistors.

The output inductor value may change with current. This will change the output ripple and thus the DC output voltage.It will not change the frequency.

Switching frequency variation with load can be minimized by choosing lower RDSON MOSFETs. High RDSON MOSFETS will cause the switching frequency to increase as the load current increases. This will reduce the ripple and thus the DC output voltage. This inherent droop should be considered when deciding if passive droop is required. If the output ripple some passive droop may be desirable to further reduce the output capacitance.

Application Information (Cont.)

DDR Supply Selection

The SC1486 can be configured so that VTT and VDQ are generated directly from the battery. Alternatively, the VTT supply can be generated from the VDDQ supply. Since the battery configuration generally yields better efficiency and performance, the eval board is configured to generate both supplies from the battery.

DDR Reference Buffer

The reference buffer is capable of driving 3ma and sinking 25ua. Since the output is class A, if additional sinking i s required an external pulldown resistor can be added. Make sure that the ground side of this pulldown is tied to the VTT AGND plane near the AGND2 pin of the SC1486.

As with most opamps, a small resistor is required when driving a capacitive load. To ensure stability use either a 10 ohm resistor in series with a 1uf capacitor or a 100 ohm resistor in series with a 0.1uF capacitor from REFOUT to AGND2.

REFIN should also be filtered so that VDDQ ripple does not appear at the REFIN pin. If a resistor divider is used to create REFIN from VDDQ, then a 0.1uF capacitor from REFIN to AGND2 will provide adequate filtering.

Thermal Considerations

The junction temperature of the device may be calculated as follows:

$$T_J = T_A + P_D \bullet \theta_{JA} \quad °C$$

Where:
T_A = ambient temperature (°C)
P_D = power dissipation in (W)
θ_{JA} = thermal impedance junction to ambient from absolute maximum ratings (°C/W)

The power dissipation may be calculated as follows:

$$P_D = 2 \bullet \left(VCCA \bullet I_{VCCA} + V_g \bullet Q_g \bullet f\right) \quad W$$

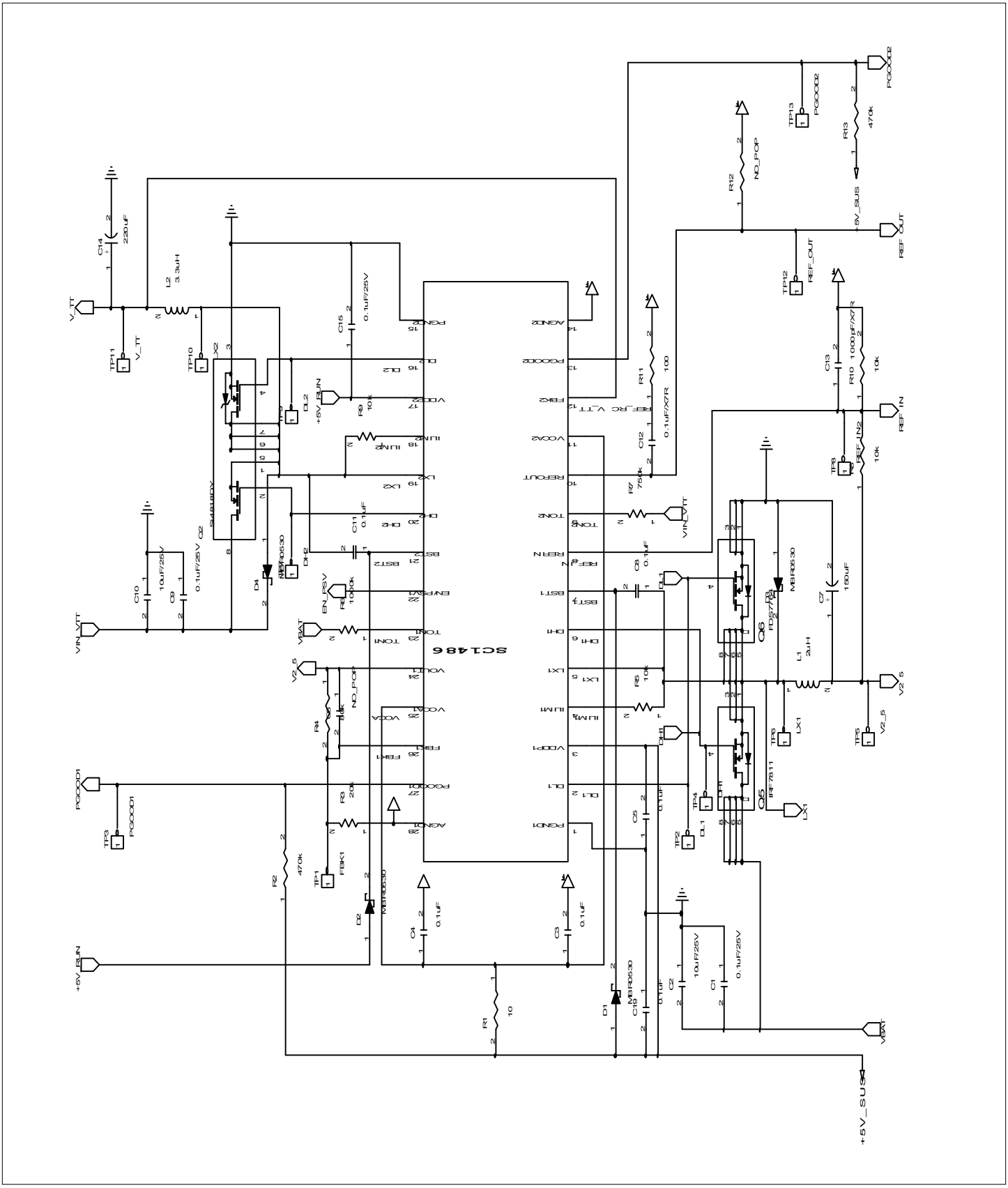
Where:
VCCA = chip supply voltage (V)
I_{VCCA} = operating current (A)
V_g = gate drive voltage, typically 5V (V)
Q_g = FET gate charge, from the FET datasheet (C)
f = switching frequency (kHz)

Inserting the following values as an example:
T_A = 85°C
θ_{JA} = 37°C/W
VCCA = 5V
I_{VCCA} = 1100µA (data sheet maximum)
V_g = 5V
Q_g = 60nC
f = 300kHz (enter the higher of the two set frequencies here)
gives us:

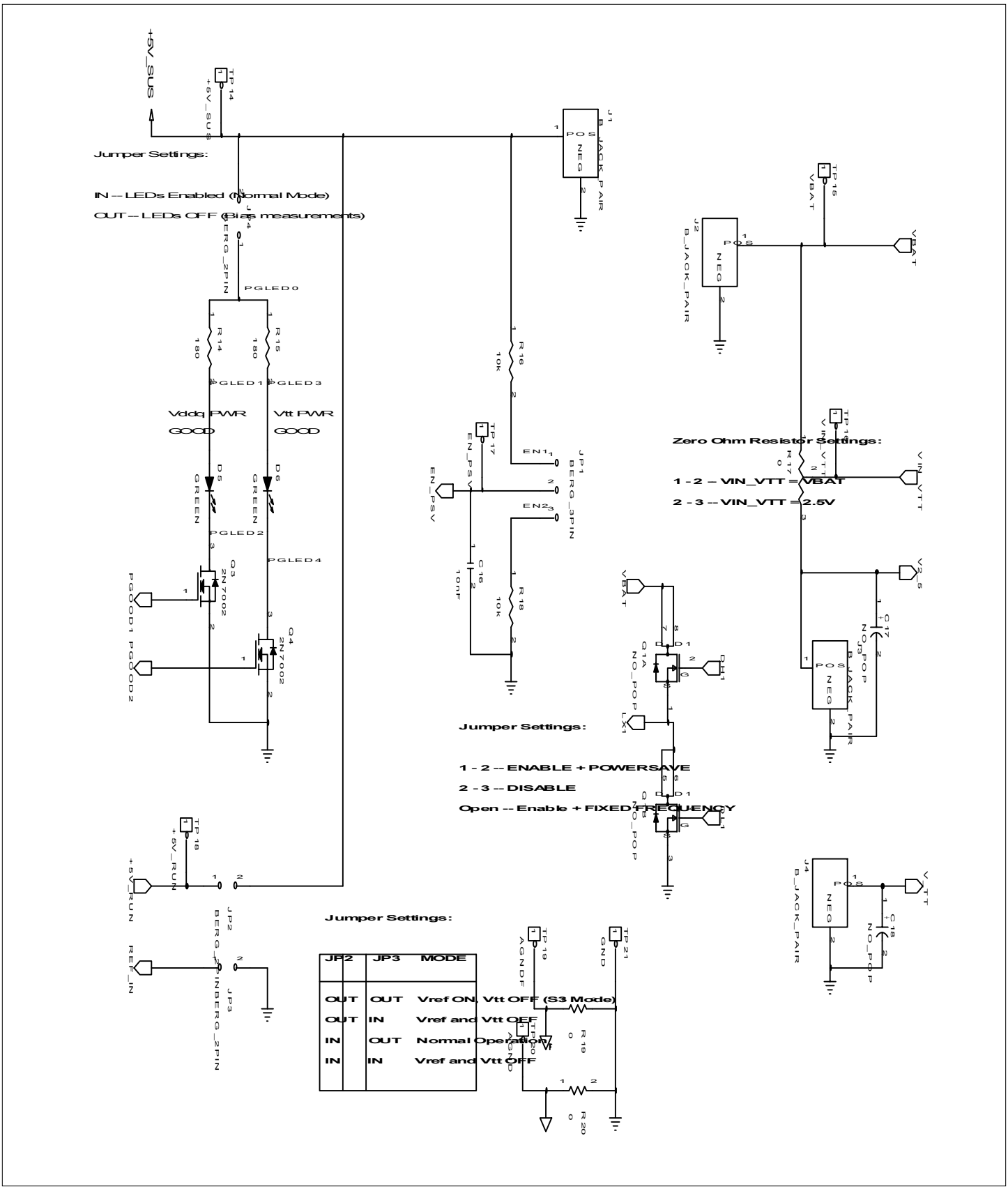
$$T_J = 85 + 2 \bullet \left(5 \bullet 1100 \bullet 10^{-6} + 5 \bullet 60 \bullet 10^{-9} \bullet 300 \bullet 10^{3}\right) \bullet 37 = 92 \quad °C$$

As can be seen, the heating effects due to internal power dissipation are practically negligible, thus requiring no special consideration thermally during layout.

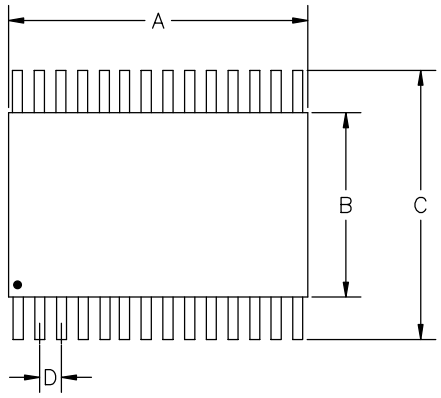
Application Schematic

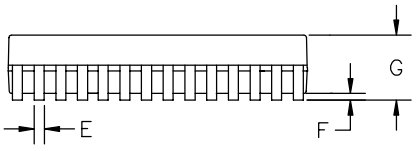


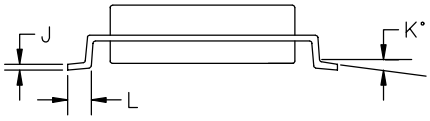
Application Schematic



Outline Drawing - TSSOP-28







DIMENSIONS ①					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	②
B	.169	.177	4.30	4.50	②
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0020	.0060	.05	.15	—
G		.047		1.20	—
J	.0035	.0079	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

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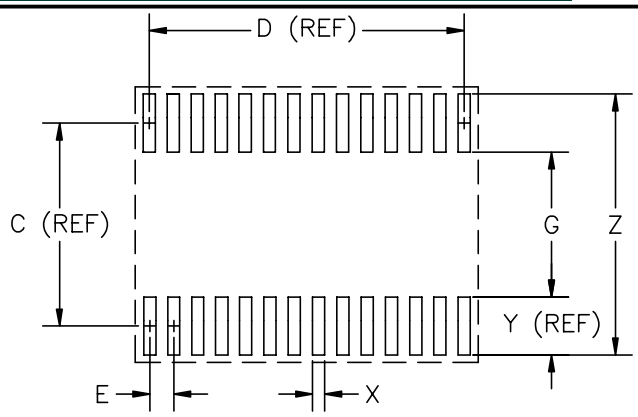
② DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

① CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-28



DIMENSIONS ①					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.218	—	5.53	REF
D	—	.333	—	8.45	REF
E	—	.026	—	0.65	BSC
G	.155	—	3.947	—	—
X	—	.013	—	0.323	—
Y	—	.062	—	1.583	REF
Z	—	.280	—	7.113	—

2 GRID PLACEMENT COURTYARD IS 18 X 15 ELEMENTS (9mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

① CONTROLLING DIMENSIONS: MILLIMETERS.

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